August, 1989

HITACHI®

LCD CONTROLLER/DRIVER LSI DATA BOOK

Including:

- DATA SHEETS
- APPLICATION NOTES
- HD63645/HD64645/HD64646 USER'S MANUAL

#U74

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LCD CONTROLLER/DRIVER LSI DATA BOOK

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8/89

LCD
CONTROLLER/DRIVER LSI
DATA BOOK

(Including):

- HD66300T Horizontal Driver for TFT-Type LCD Color TV
- HD66840 Video Interface Controller (LVIC) Application Note
- HD63645F/HD64645F LCD Timing Controller (LCTC) Application Note
- HD63645/HD64645/HD64646 LCD Timing Controller (LCTC) User's Manual

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HITACHI®

ADE-407-001C

September 1989

Printed in U.S.A.

Section One

LCD Controller/
Driver LSI
Data Book

SECTION
1

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LCD Controller/ Driver LSI Data Book

For additional information reference:

Section 2. HD66300T Horizontal Driver for TFT-Type LCD Color TV
Section 3. HD66840 Video Interface Controller (LVIC) Application Note
Section 4. HD63645F/HD64645F LCD Timing Controller (LCTC) Application Note
Section 5. HD63645/HD64645/HD64646 LCD Timing Controller (LCTC) User's Manual

LCD Controller/Driver LSI Data Book

SECTION ONE
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■ GENERAL INFORMATION

General Information

Quick Reference Guide

Type		**Column Driver**							
Type Number		**HD44100H**	**HD66100**	**HD61100A**	**HD61200**	**HD61104**	**HD61104A**	**HD66106**	**HD66107T**
Power supply for internal circuits (V)		5	5	5	5	5	5	5	5
Power supply for LCD Drive Circuit (V)		11	6	17	17	26	28	37	37
Power Dissipation (mW)		5	5	5	5	5	5	5	5
Operating Temperature (°C)		-20 to +75*1	-20 to +75*1	-20 to +75*1	-20 to +75	-20 to +75	-20 to +75	-20 to +75	-20 to +75
Memory	ROM (bit)	–	–	–	–	–	–	–	–
	RAM (bit)	–	–	–	–	–	–	–	–
LCD Driver	Common	20	–	–	–	–	–	80	160
	Column	40 (20)	80	80	80	80	80	80	160
Instraction Set		–	–	–	–	–	–	–	–
Operation Frequency (MHz)		0.4	1	2.5	2.5	3.5	3.5	6	8
Duty		Static-1/32	Static-1/16	Static-1/100	1/32-1/128	1/64-1/200	1/64-1/240	1/100-1/480	1/100-1/480
Package		FP-60	FP-100	FP-100	FP-100	FP-100	FP-100	FP-100	192pin TAB

Type		**Column Driver (RAM)**			**Segment Display**			
Type Number		**HD44102CH**	**HD61102**	**HD61202**	**HD61602**	**HD61603**	**HD61604**	**HD61605**
Power supply for internal circuits (V)		5	5	5	3 to 5	3 to 5	3 to 5	3 to 5
Power supply for LCD Drive Circuit (V)		11	15.5	17	5	5	5	5
Power Dissipation (mW)		5	5	5	0.5	0.5	0.5	0.5
Operating Temperature (°C)		-20 to +75	-20 to +75	-20 to +75	-20 to +75*1	-20 to +75*1	-20 to +75*1	-20 to +75*1
Memory	ROM (bit)	–	–	–	–	–	–	–
	RAM (bit)	200×8	512×8	512×8	204	64	204	64
LCD Driver	Common	–	–	–	4	1	4	1
	Column	50	64	64	51	64	51	64
Instraction Set		6	7	7	4	4	4	4
Operation Frequency (MHz)		0.28	0.4	0.4	0.52	0.52	0.52	0.52
Duty		1/8,1/12, 1/16,1/24, 1/32	Static-1/64	1/48,1/64, 1/96,1/128	Static,1/2, 1/3,1/4	Static	Static,1/2, 1/3,1/4	Static
Package		FP-80	FP-100	FP-100	FP-80, FP-80A	FP-80	FP-80	FP-80

*1 -40 to +85°C (Special request). Please contact Hitachi agents.

Quick Reference Guide

Type		**Common Driver**				
Type Number		**HD44103CH**	**HD44105H**	**HD61103A**	**HD61203**	**HD61105**
Power supply for internal circuits (V)		5	5	5	5	5
Power supply for LCD Drive Circuit (V)		11	11	17	17	26
Power Dissipation (mW)		4.4	4.4	5	5	5
Operating Temperature (°C)		−20 to +75	−20 to +75	−20 to +75	−20 to +75	−20 to +75
Memory	ROM (bit)	–	–	–	–	–
	RAM (bit)	–	–	–	–	–
LCD Driver	Common	20	32	64	64	80
	Column	–	–	–	–	–
Instraction Set		–	–	–	–	–
Operation Frequency (MHz)		1	1	2.5	2.5	0.1
Duty		1/8,1/12, 1/16,1/24, 1/32	1/8,1/12, 1/32,1/48	Static-1/10, 1/64	1/32-1/128	1/64-1/200
Package		FP-60	FP-60	FP-100	FP-100	FP-100

Type		**Character Display**				**Graphic Display**			
Type Number		**HD61105A**	**HD43160AH**	**HD44780 (LCD-II)**	**HD66780 (LCD-IIA)**	**HD61830**	**HD61830B**	**HD63645 HD64645 HD64646 LCTC**	**HD66840 LVIC**
Power supply for internal circuits (V)		5	5	5	5	5	5	5	5
Power supply for LCD Drive Circuit (V)		28	–	11	5	–	–	–	–
Power Dissipation (mW)		5	10	2	2	30	50	50	250
Operating Temperature (°C)		−20 to +75	−20 to +75	−20 to +75*1	−20 to +75	−20 to +75	−20 to +75*1	−20 to +75	−20 to +75
Memory	ROM (bit)	–	6420	7200	12000	7360	7360	–	–
	RAM (bit)	–	80×8	80×8, 64×8	16	–	–	–	–
LCD Driver	Common	80	–	16	16	–	–	–	–
	Column	–	–	40	40	–	–	–	–
Instraction Set		–	6	11	11	12	12	–	–
Operation Frequency (MHz)		0.1	0.25/0.375	0.25	0.25	1.1	2.4	10	25(30)
Duty		1/64-1/240	1/8,1/12, 1/16	1/8,1/11, 1/16	1/8,1/11, 1/16	Static -1/128	Static -1/128	Static -1/512	4-1/1024
Package		FP-100	FP-54	FP-80, FP-80A	FP-80A FP-80B	FP-60	FP-60	FP-80, FP-80B	FP-100A

*1 -40 to +85°C (Special request). Please contact Hitachi agents.

Type Number Order

Type	Function	Reference Page
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HD44100H	LCD Driver with 40 Channel Output	61
HD44102CH	LCD Column Driver with 50 Channel Output	205
HD44103CH	LCD Common Driver with 20 Channel Output	230
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HD61100A	LCD Column Driver with 80 Channel Output	248
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HD61103A	LCD Common Driver with 64 Channel Output	291
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HD61105	LCD Common Driver with 80 Channel Output	433
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HD61203	LCD Common Driver with 64 Channel Output	361
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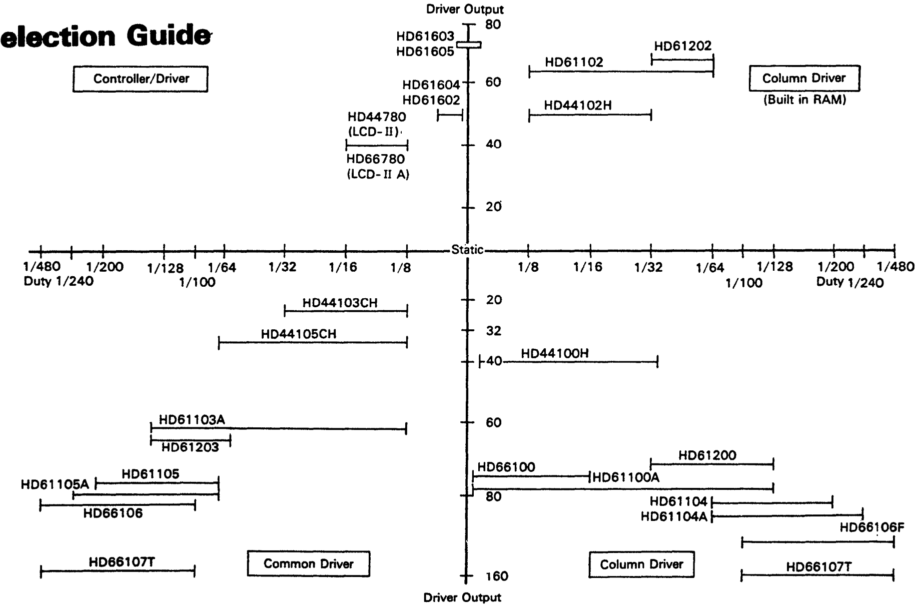
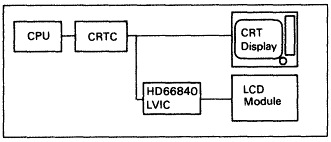
HD66840F LVIC	LCD Video Interface Controller	552

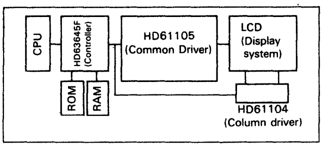
Selection Guide

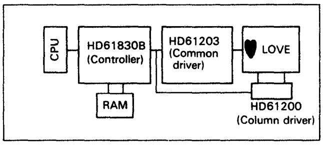


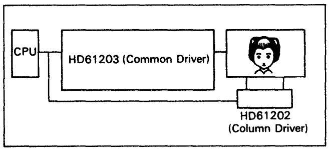
Hitachi LCD Driver System

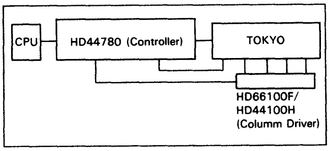
Type	Reference Figure	Screen Size (max)	Lineup	Application

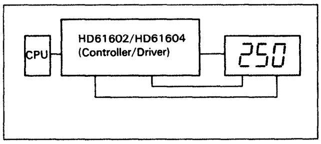
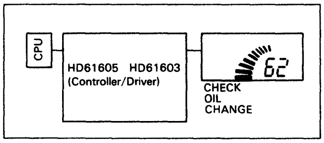
Video to LCD converter		720×512 dots	HD66840,
			HD66106(Driver)
			HD66107(Driver),
			HD61104(Column)
			HD61105(Common)
				Personal Computer, Terminal, OHP

Display System for CRT Compatible	 CPU
	HD63645F (Controller)
	HD61105 (Common Driver)
	LCD (Display system)
	ROM
	RAM
	HD61104 (Column driver)
		640×400 dots	HD63645/64645/
			64646(Controller)
			HD61104(Column)/
			61105(Common)
			HD66106(Driver)
				Personal Computer, Wordprocessor, Terminal

Graphic Display System	 CPU
	HD61830B (Controller)
	HD61203 (Common driver)
	LOVE
	RAM
	HD61200 (Column driver)
		Character 80×16
		Graphic 480×128 dots
			HD61100A(Column),
			HD61830B(Controller)
			HD61200(Column)
			HD61103A(Common),
			HD61203(Common)
				Laptop Computer, Facsimile, Telex, Copy machine

Graphic Display System (Bitmap)		480×128 dots	HD44102CH(Column)/
			61102(Column)
			HD44103CH(Common)
			HD61202(Column)
			HD44105H(Common)/
			61103A(Common)
			HD61203(Common)
				Laptop Computer, Handy Wordprocessor, Toy

Character Display System	 CPU
	HD44780 (Controller)
	TOKYO
	HD66100F/
	HD44100H
	(Columm Driver)
		40 Characters ×2 Columns
		80 Characters ×1 Column
			HD44780(LCD-II)
			(Controller/Driver)
			HD66780(LCD-II A)
			(Controller/Driver)
			HD44100H(Column)
			HD66100F(Column)
				Electrical Typewriter, Multifunction Telephone, Handy Terminal

Segment Display System		25 Digits ×1 Column	HD61602 (Controller/Driver) HD61604 (Controller/Driver)	ECR, Measurement System, Telephone
Static Display System	 CPU HD61605 HD61603 (Controller/Driver) 62 CHECK OIL CHANGE	64 Segments	HD61603 (Controller/Driver) HD61605 (Controller/Driver)	Industrial Measurement System

Application

Character and Graphic Display

1 character=7 × 8dot (15× 7 dot +cursor)

Line \ Character	8	16	20	24	32	40	Over 80
1		HD66100					
2							
3				HD44100H			
4							
6 to 8							
12 to 15	HD61200 (Column) + HD61203 (Common)						
16 to 25	HD61104 (Column) + HD61105 (Common)						
26 to 50	HD66106, HD66107						

Graphic Display

Vertical \ Horizontal	48	96	120	180	240	480	Over 640
16	HD61202 (Column) + HD61203 (Common)						
32							
48							
64							
128							
400	HD61104 (Column) + HD61105 (Common)						
Over 400	HD66106, HD66107						

Note: Applications in this page are mere example, and this combination of devices is not the best.

Differences Between Products

1. HD66100F and HD44100H

	HD66100F	HD44100H
LCD drive circuits	80	20×2
Power supply for internal logic (V)	3 to 6	4.5 to 11
Display duty	Static to 1/16	Static to 1/32
Package	100 pin plastic QFP	60 pin plastic QFP

2. HD61100A and HD61200

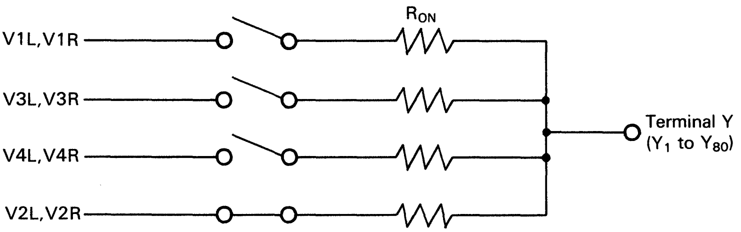
		HD61100A	HD61200
LCD drive circuits	common	–	–
	column	80	80
Display duty		static to 1/128	1/32 to 1/128
Power supply for LCD drive circuits (V)		0 to 17	8 to 17
Power supply limits of LCD driver circuit voltage		V_{CC} to V_{EE} (no limit)	shown in figures below

Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V3L, V3R, V4L, and V4R) when load current flows through one of the terminals Y_1 to Y_{80}. This value is specified under the following condition.

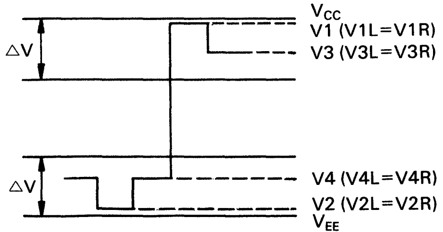
$V_{CC}-V_{EE}=17V$

$V1L=V1R$, $V3L=V3R=V_{CC}-2/7\ (V_{CC}-V_{EE})$

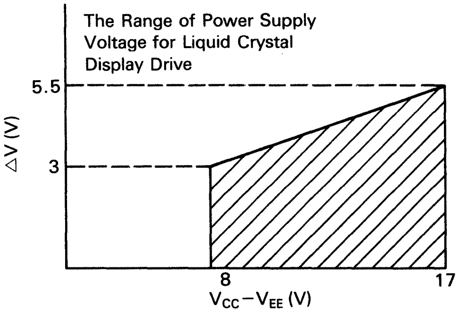
$V2L=V2R$, $V4L=V4R=V_{EE}+2/7\ (V_{CC}-V_{EE})$



Here is a description of the range of power supply voltage for linquid crystal display drive. Apply positive voltage to V1L=V1R and V3L=V3R and negative voltage to V2L=V2R and V4L=V4R within the ΔV range. This range allows stable impedance on driver output (R_{ON}). Notice the ΔV depends on power supply voltage $V_{CC}-V_{EE}$.



Correlation between Driver Output Waveform and Power supply Voltages for Liquid Crystal Display Drive



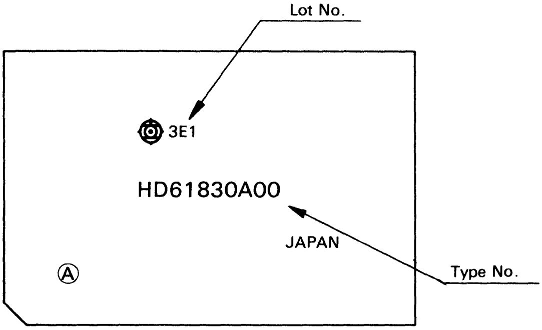
Correlation between Power Supply Voltage $V_{CC}-V_{EE}$ and ΔV

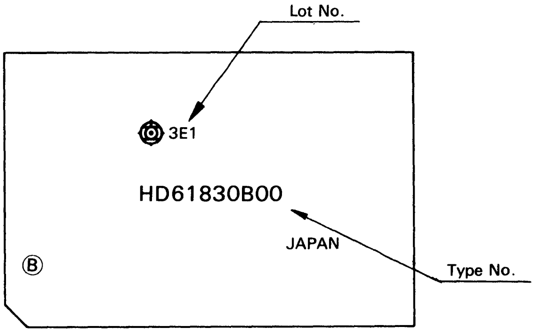
3. HD66100F and HD61100A

		HD66100F	HD61100A
LCD driver circuits	common	–	–
	column	80	80
Power supply for LCD drive circuits (V)		3 to 6	5.5 to 17.0
Display duty		static to 1/16	static to 1/128
Operating frequency (MHz)		1.0 MHz (max)	2.5 MHz (max)
Data fetch method		Shift	Latch
Package		100 pin Plastic QFP (FP-100)	100 pin plastic QFP (FP-100)

4. HD61830 and HD61830B

	HD61830	HD61830B
Oscillator	Internal	External
Operating frequency (MHz)	1.1 MHz	2.4 MHz
Display duty	static to 1/128	static to 1/128
Programmable screen size (Max)	64×240 dots (1/64 duty)	128×480 dots (1/64 duty)
Other	pin 6:C pin 7:R pin 9:CPO	pin 6:$\overline{CE}$ pin 7:$\overline{OE}$ pin 9:NC
Package Marking	Ⓐ	Ⓑ



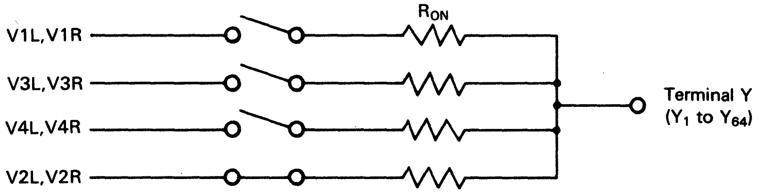


5. HD61102 and HD61202

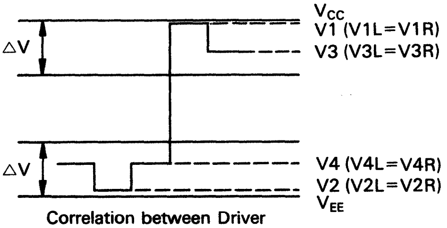
	HD61102	HD61202
Display duty	static to 1/64	1/32 to 1/64
Recommended voltage between V_{CC} and V_{EE} (V)	4.5 to 15.5	8 to 17
Power supply limits of LCD driver circuits voltage	V_{CC} to V_{EE} (no limit)	shown following figure
Pin 88	DY (output)	NC (non connection)
Absolute maximum rating of V_{EE} (V)	$V_{CC}-17.0$ to $V_{CC}+0.3$	$V_{CC}-19.0$ to $V_{CC}+0.3$

Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V3L, V3R, V4L and V4R) when load current flows through one of the terminals Y_1 to Y_{64}. This value is specified under the following condition.

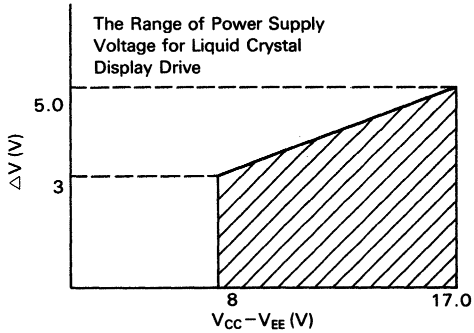
$V_{CC}-V_{EE}=15.5V$
$V1L=V1R,\ V3L=V3R=V_{CC}-2/7\ (V_{CC}-V_{EE})$
$V2L=V2R,\ V4L=V4R=V_{EE}+2/7\ (V_{CC}-V_{EE})$



Here is a description of the range of power supply voltage for liquid crystal display drive. Apply positive voltage to V1L=V1R and V3L=V3R and negative voltage to V2L=V2R and V4L=V4R within the ΔV range. This range allows stable impedance on driver output (R_{ON}). Notice that ΔV depends on power supply voltage $V_{CC}-V_{EE}$.



Correlation between Driver Output Waveform and Power supply Voltages for Liquid Crystal Display Drive



Correlation between Power Supply Voltage $V_{CC}-V_{EE}$ and ΔV

6. HD61103A and HD61203

	HD61103A	HD61203
Recommended voltage between V_{CC} and V_{EE} (V)	4.5 to 17	8 to 17
Power supply limits of LCD drive circuits voltage	V_{CC} to V_{EE} (no limit)	shown in figures below
Output terminal	shown in following figure 4	shown in following figure 5

Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V5L, V5R, V6L and V6R) when load current flows through one of the terminals X1 to X64. This value is specified under the following conditions:

$V_{CC}-V_{EE}=17V$
$V1L=V1R,\ V6L=V6R=V_{CC}-1/7\ (V_{CC}-V_{EE})$
$V2L=V2R,\ V5L=V5R=V_{EE}+1/7\ (V_{CC}-V_{EE})$

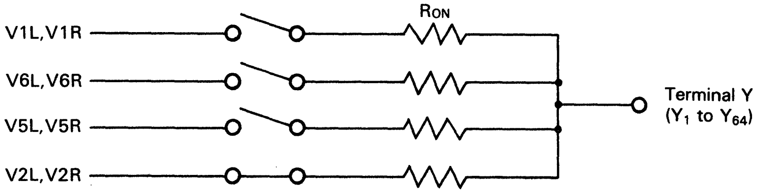
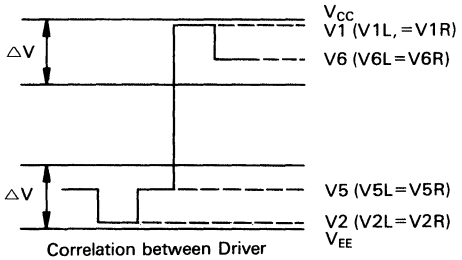


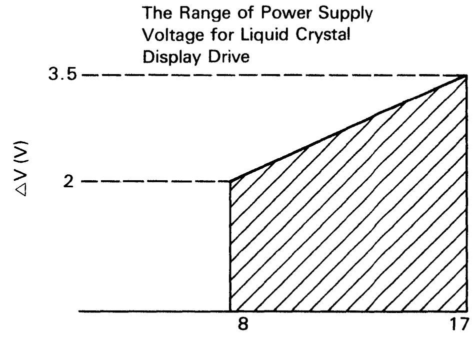
Figure 1.

Here is a description of the range of power supply voltage for liquid crystal display drive. Apply postive voltage to V1L=V1R and V6L=V6R and negative voltage to V2L=V2R and V5L=V5R within the ΔV range. This range allows stable impedance on driver output (R_{ON}). Notice that ΔV depends on power supply voltage $V_{CC}-V_{EE}$.



Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive

Figure 2.



Correlation between Power Supply Voltage $V_{CC}-V_{EE}$ and ΔV

Figure 3.

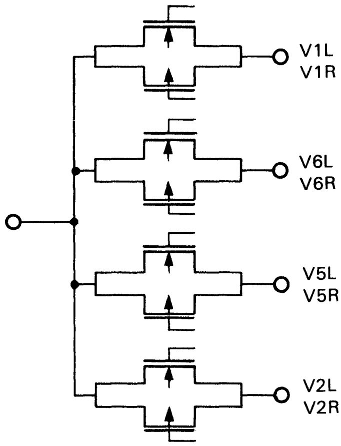


Figure 4.

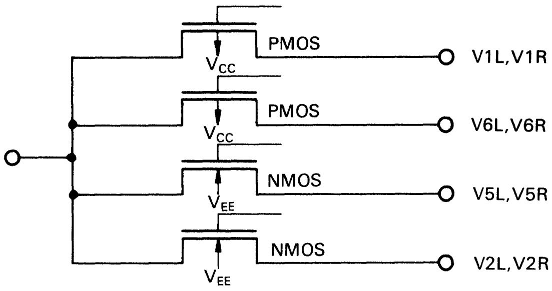


Figure 5.

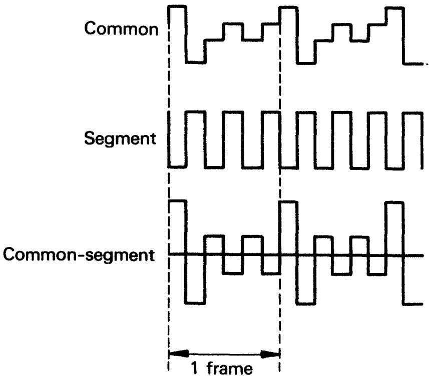
7. HD66106F and HD61104

	HD66106F	HD61104
LCD drive circuits voltage	+14 to +35 (V_{LCD}-GND)	-10 to -26 (V_{CC}-V_{EE})
Display Duty	1/100 to 1/400	1/64 to 1/200
Operating frequency (MHz)	6.0 MHz	3.5 MHz
Function	column and common driver	column driver

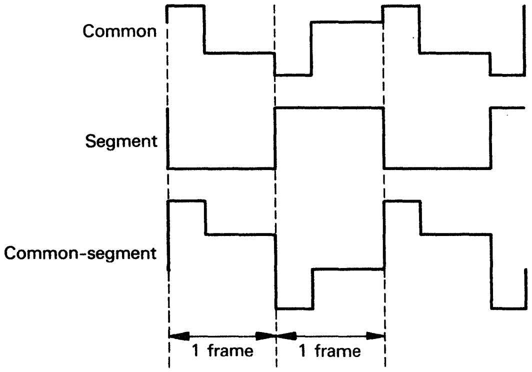
8. HD44780 LCD-II and HD66780 LCD-II A

Item		LCD-II (HD44780)	LCD-II A (HD66780)	Note
Display RAM (Maximum number of display characters)		80 bytes (80 characters)	Same as LCD-II	
*Character generator ROM (kinds of characters)		7200 bits 192 characters 5×7;160 characters 5×10;32 characters	12000 bits 240 characters 5×10;240 Characters	
Character generator RAM (Number of characters)		64 bytes (8 characters)	Same as LCD-II	
LCD driving terminals (Maximum number of display characters/ unit)		16 COMs 40 SEGs (16 characters)	Same as LCD-II	
Character font (with a cursor)		5x8 dots 5×11 dots	Same as LCD-II	
Multiplexing duty ratio		1/8, 1/11, 1/16	Same as LCD-II	
*LCD driving voltage	1/4 bias	3.0 to 11 (V)	3.0 to V_{CC} (V)	V_{CC} to V_5
	1/5 bias	4.6 to 11 (V)	3.0 to V_{CC} (V)	
*LCD driving waveform		waveform A	waveform B	Shown following figures
*Bus timing		1, 1.5MHz	2MHz	
Instruction codes		11 instructions	Same as LCD-II	
Power-on reset circuit		Yes	Same as LCD-II	
Oscillator (Frequency)		Ceramic filter, Rf, external clock (250 kHz)	Same as LCD-II	
Interface		HD44100H	HD44100H or HD66100F	
Package		FP-80, FP-80A	Same as LCD-II	

Note: *Indicates the modified items in LCD-II A.



Waveform A (1/3 Duty, 1/3 Bias)



Waveform B (1/3 Duty, 1/3 Bias)

9. HD61104 and HD61104A

	HD61104	HD61104A
LCD Drive Circuits	80	80
Data Transfer Rate (MHz)	3.5	3.5
Power Supply for LCD drive circuits (V)	10 to 26	10 to 28

10. HD61105 and HD61105A

	HD61105	HD61105A
LCD Drive Circuits	80	80
Power Supply for LCD drive circuits (V)	10 to 26	10 to 28

11. HD66106F and HD66107T

	HD66106F	HD66107T
LCD drive circuits	80	160
Data transfer	4-bits	4-bits/8-bits
Operating frequency (MHz)	6	8
Power supply for LCD drive circuits	14 to 37	14 to 37
Packge	100-Pin plastic QFP (FP-100A)	192-pin TAB

12. HD63645, HD64645 and HD64646

	HD63645	HD64645	HD64646
CPU interface	68 family	80 family	80 family
Package	80-pin plastic QFP (FP-80)	80-pin Plastic QFP (FP-80)	80-pin plastic QFP (FP-80A)
Other	–	–	HD64646 has another LCD drive interface in HD64645

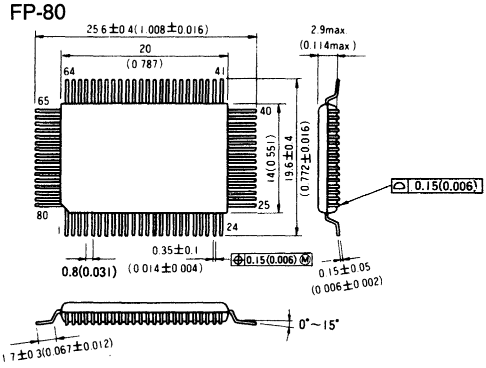
Package Information

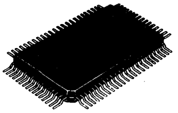
Package Information

The Hitachi LCD driver devices use plastic flat packages to make compact equipment in which they are incorporated and provide higher dencity mounting by utilizing the features of thin liquid crystal display elements.

Package Dimension

FP-80

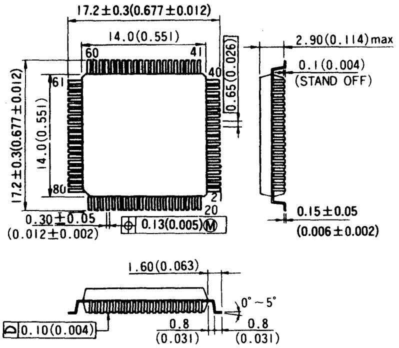


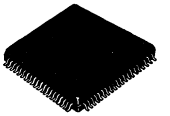


Code	FP-80
EIAJ	——
JEDEC	——

Applicable LSI	HD61602, HD61603, HD61604, HD61605, HD44780, HD66780, HD63645, HD64645, HD64646, HD644102CH

FP-80A

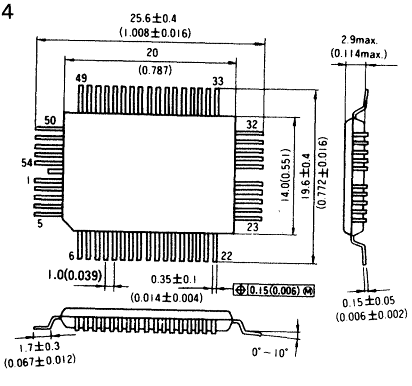


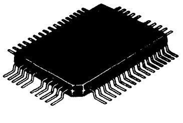


Code	FP-80A
EIAJ	——
JEDEC	——

Applicable LSI	HD66780, HD44780, HD61602

FP-54

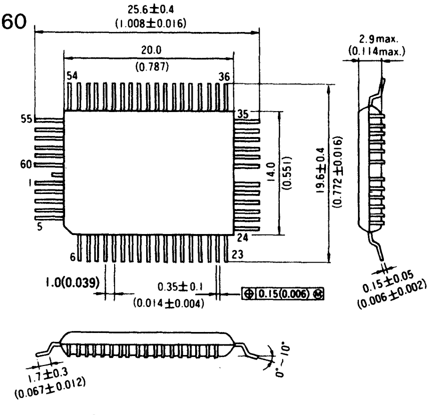


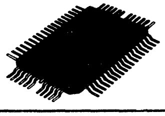


Code	FP-54
EIAJ	——
JEDEC	——

Applicable LSI	HD43160AH

FP-60

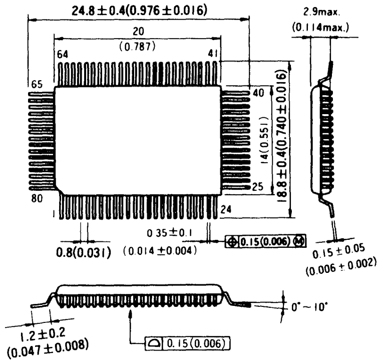


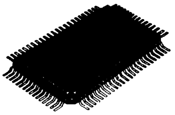


Code	FP-60
EIAJ	——
JEDEC	——

Applicable LSI	HD44100H, HD44103CH, HD44105H, HD61830, HD61830B

FP-80B

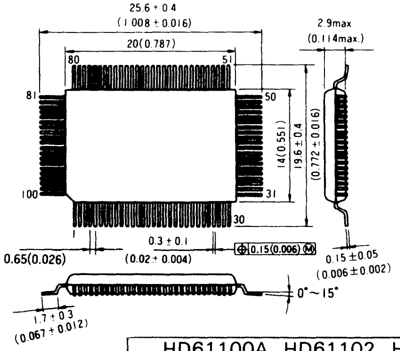


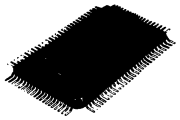


Code	FP-80B
EIAJ	——
JEDEC	——

Applicable LSI	HD64646, HD66780

FP-100

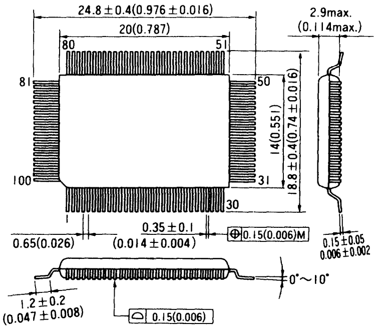


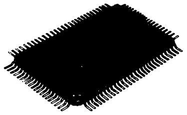


Code	FP -100
EIAJ	——
JEDEC	——

Applicable LSI	HD61100A, HD61102, HD61103A, HD61104 HD61105, HD61200, HD61202, HD61203 HD66100

FP-100A





Code	FP-100A
EIAJ	——
JEDEC	——

Applicable LSI	HD66106, HD66840

Reliability and Quality Assurance

1. VIEWS ON QUALITY AND RELIABILITY

Basic views on quality in Hitachi are to meet individual user's purchase purpose and quality required, and to be at the satisfied quality level considering general marketability. Quality required by users is specifically clear if the contract specification is provided. If not, quality required is not always definite. In both cases, efforts are made to assure the reliability so that semiconductor devices delivered can perform their ability in actual operating circumstances. To realize such quality in manufacturing process, the key points should be to establish quality control system in the process and to enhance moral for quality.

In addition, quality required by users on semiconductor devices is going toward higher level as performance of electronic system in the market is going toward higher one and is expanding size and application fields. To cover the situation, actual bases Hitachi is performing is as follows;

(1) Build the reliability in design at the stage of new product development.

(2) Build the quality at the sources of manufacturing process.

(3) Execute the harder inspection and reliability confirmation of final products.

(4) Make quality level higher with field data feed back.

(5) Cooperate with research laboratories for higher quality and reliability.

With the views and methods mentioned above, utmost efforts are made for users' requirements.

2. RELIABILITY DESIGN OF SEMICONDUCTOR DEVICES

2.1 Reliability Targets

Reliability target is the important factor in manufacture and sales as well as performance and price. It is not practical to rate reliability target with failure rate at the certain common test condition. The reliability target is determined corresponding to character of equipments taking design, manufacture, inner process quality control, screening and test method, etc. into consideration, and considering operating circumstances of equipments the semiconductor device used in, reliability target of system, derating applied in design, operating condition, maintenance, etc.

2.2 Reliability Design

To achieve the reliability required based on reliability targets, timely study and execution of design standardization, device design (including process design, structure design), design review, reliability test are essential.

(1) Design Standardization

Establishment of design rule, and standardization of parts, material and process are necessary. As for design rule, critical items on quality and reliability are always studied at circuit design, device design, layout design, etc. Therefore, as long as standardized process, material, etc. are used, reliability risk is extremely small even in new development devices, only except for in the case special requirements in function needed.

(2) Device Design

It is important for device design to consider total balance of process design, structure design, circuit and layout design. Especially in the case new process and new material are employed, technical study is deeply executed prior to device development.

(3) Reliability Evaluation by Test Site

Test site is sometimes called Test Pattern. It is useful method for design and process reliability evaluation of IC and LSI which have complicated functions.

1. Purposes of Test Site are as follows;
   - Making clear about fundamental failure mode
   - Analysis of relation between failure mode and manufacturing process condition
   - Search for failure mechanism analysis
   - Establishment of QC point in manufacturing
2. Effectiveness of evaluation by Test Site are as follows;
   - Common fundamental failure mode and failure mechanism in devices can be evaluated.

- Factors dominating failure mode can be picked up, and comparison can be made with process having been experienced in field.
- Able to analyze relation between failure causes and manufacturing factors.
- Easy to run tests.

etc.

2.3 Design Review

Design review is organized method to confirm that design satisfies the performance required including users' and design work follows the specified ways, and whether or not technical improved items accumulated in test data of individual major fields and field data are effectively built in. In addition, from the standpoint of enhancement of competitive power of products, the major purpose of design review is to ensure quality and reliability of the products. In Hitachi, design review is performed from the planning stage for new products and even for design changed products. Items discussed and determined at design review are as follows;

(1) Description of the products based on specified design documents.

(2) From the standpoint of specialty of individual participants, design documents are studied, and if unclear matter is found, sub-program of calculation, experiments, investigation, etc. will be carried out.

(3) Determine contents of reliability and methods, etc. based on design document and drawing.

(4) Check process ability of manufacturing line to achieve design goal.

(5) Discussion about preparation for production.

(6) Planning and execution of sub-programs for design change proposed by individual specialist, and for tests, experiments and calculation to confirm the design change.

(7) Reference of past failure experiences with similar devices, confirmation of method to prevent them, and planning and execution of test program for confirmation of them. These studies and decisions are made using check lists made individually depending on the objects.

3. QUALITY ASSURANCE SYSTEM OF SEMICONDUCTOR DEVICES

3.1 Activity of Quality Assurance

General views of overall quality assurance in Hitachi are as follows;

(1) Problems in individual process should be solved in the process. Therefore, at final product stage, the potential failure factors have been already removed.

(2) Feedback of information should be made to ensure satisfied level of process ability.

(3) To assure reliability required as an result of the things mentioned above is the purpose of quality assurance.

The followings are regarding device design, quality approval at mass production, inner process quality control, product inspection and reliability tests.

3.2 Quality Approval

To ensure quality and reliability required, quality approval is carried out at trial production stage of device design and mass production stage based on reliability design described at section 2.

The views on quality approval are as follows;

(1) The third party performs approval objectively from the standpoint of customers.

(2) Fully consider past failure experiences and information from field.

(3) Approval is needed for design change and work change.

(4) Intensive approval is executed on parts material and process.

(5) Study process ability and fluctuation factor, and set up control points at mass production stage.

Considering the views mentioned above, quality approval shown in Fig. 1 is performed.

3.3 Quality and Reliability Control at Mass Production

For quality assurance of products in mass production, quality control is executed with organic division of functions in manufacturing department, quality assurance department, which are major, and other departments related. The total function flow is shown in Fig. 2. The main points are described below.

3.3.1 Quality Control of Parts and Material

As the performance and the reliability of semiconductor devices are getting higher, importance is increasing in quality control of material and parts, which are crystal, lead frame, fine wire for wire bonding, package, to build products, and materials needed in manufacturing process, which are mask pattern and chemicals. Besides quality approval on parts and materials stated in section 3.2, the incoming inspection is, also, key in quality control of parts and materials. The incoming inspection is performed based on incoming inspection specification following purchase specification and drawing, and sampling inspection is executed based on MIL-STD-105D mainly.

The other activities of quality assurance are as follows:

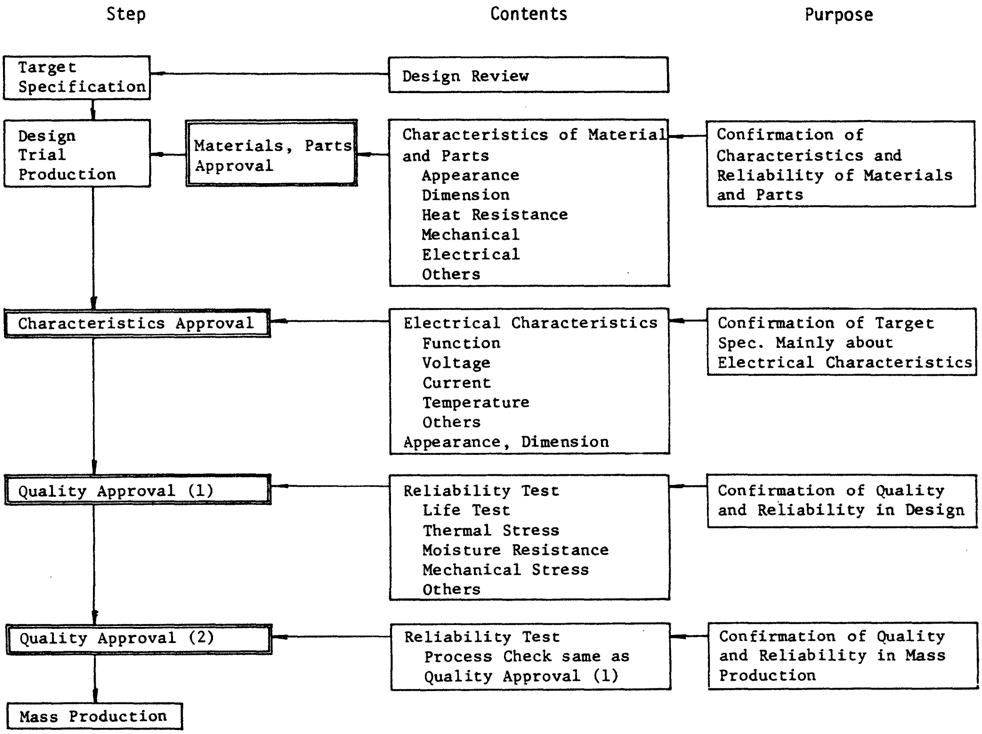

Step
Contents
Purpose
Target Specification
Design Review
Design Trial Production
Materials, Parts Approval
Characteristics of Material and Parts
Appearance
Dimension
Heat Resistance
Mechanical
Electrical
Others
Confirmation of Characteristics and Reliability of Materials and Parts
Characteristics Approval
Electrical Characteristics
Function
Voltage
Current
Temperature
Others
Appearance, Dimension
Confirmation of Target Spec. Mainly about Electrical Characteristics
Quality Approval (1)
Reliability Test
Life Test
Thermal Stress
Moisture Resistance
Mechanical Stress
Others
Confirmation of Quality and Reliability in Design
Quality Approval (2)
Reliability Test
Process Check same as Quality Approval (1)
Confirmation of Quality and Reliability in Mass Production
Mass Production

Fig. 1 Flow Chart of Quality Approval

(1) Outside Vendor Technical Information Meeting

(2) Approval on outside vendors, and guidance of outside vendors

(3) Physical chemical analysis and test

The typical check points of parts and materials are shown in Table 1.

3.3.2 Inner Process Quality Control

Inner process quality control is performing very important function in quality assurance of semiconductor devices. The following is description about control of semi-final products, final products, manufacturing facilities, measuring equipments, circumstances and sub-materials. The quality control in the manufacturing process is shown in Fig. 3 corresponding to the manufacturing process.

(1) Quality Control of Semi-final Products and Final Products

Potential failure factors of semiconductor devices should be removed preventively in manufacturing process. To achieve it, check points are set-up in each process, and products which have potential failure factor are not transfer to the next process. Especially, for high reliability semiconductor devices, manufacturing line is rigidly selected, and the quality control in the manufacturing process is tightly executed - rigid check in each process and each lot, 100% inspection in appropriate ways to remove failure factor caused by manufacturing fluctuation, and execution of screening needed, such as high temperature aging and temperature cycling. Contents of inner process quality control are as follows;

- Condition control on individual equipments and workers, and sampling check of semifinal products.
- Proposal and carrying-out improvement of work
- Education of workers
- Maintenance and improvement of yield
- Picking-up of quality problems, and execution of counter-measures
- Transmission of information about quality

(2) Quality Control of Manufacturing Facilities and Measuring Equipment

Equipments for manufacturing semiconductor devices have been developing extraordinarily with necessary high performance devices and improvement of production, and are important factors to determine quality and reliability. In Hitachi, automatization of manufacturing equipments are promoted to improve manufacturing fluctuation, and controls are made to maintain proper operation of high performance equipments and perform the proper function. As for maintenance inspection for quality control, there are daily inspection which is performed daily based on specification related, and periodical inspection which is performed periodically. At the inspection, inspection points listed in the specification are checked one by one not to make any omission. As for adjustment and

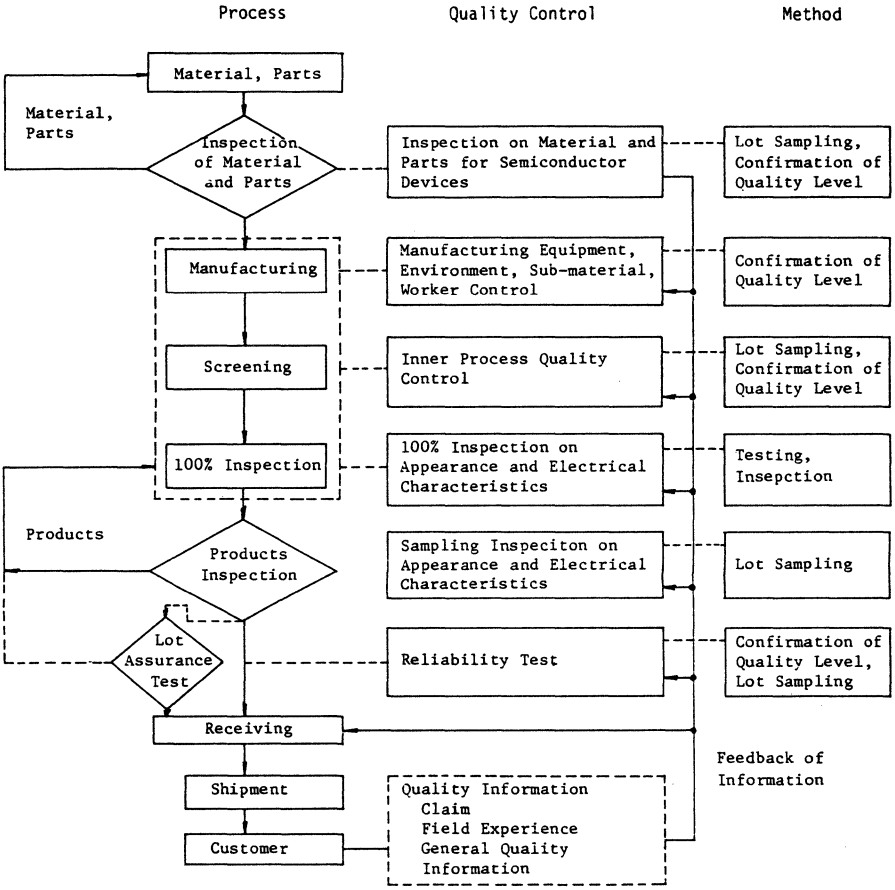

Process
Quality Control
Method
Material, Parts
Material, Parts
Inspection of Material and Parts
Inspection on Material and Parts for Semiconductor Devices
Lot Sampling, Confirmation of Quality Level
Manufacturing
Manufacturing Equipment, Environment, Sub-material, Worker Control
Confirmation of Quality Level
Screening
Inner Process Quality Control
Lot Sampling, Confirmation of Quality Level
100% Inspection
100% Inspection on Appearance and Electrical Characteristics
Testing, Insepction
Products
Products Inspection
Sampling Inspeciton on Appearance and Electrical Characteristics
Lot Sampling
Lot Assurance Test
Reliability Test
Confirmation of Quality Level, Lot Sampling
Receiving
Feedback of Information
Shipment
Customer
Quality Information
Claim
Field Experience
General Quaiity
Information

Fig. 2 Flow Chart of Quality Control in Manufacturing Process

maintenance of measuring equipments, maintenance number, specification are checked one by one to maintain and improve quality.

(3) Quality Control of Manufacturing Circumstances and Submaterials

Quality and reliability of semiconductor device is highly affected by manufacturing process. Therefore, the controls of manufacturing circumstances - temperature, humidity, dust - and the control of submaterials - gas, pure water - used in manufacturing process are intensively executed. Dust control is described in more detail below.

Dust control is essential to realize higher integration and higher reliability of devices. In Hitachi, maintenance and improvement of cleanness in manufacturing site are executed with paying intensive attention on buildings, facilities, airconditioning systems, materials delivered-in, clothes, work, etc., and periodical inspection on floating dust in room, falling dusts and dirtiness of floor.

3.3.3 Final Product Inspection and Reliability Assurance

(1) Final Product Inspection

Lot inspection is done by quality assurance department for products which were judged as good products in 100% test, which is final process in manufacturing department. Though 100% of good products is expected, sampling inspection is executed to prevent mixture of failed products by mistake of work, etc. The inspection is executed not only to confirm that the products meet users' requirement, but to consider potential factors. Lot inspection is executed based on MIL-STD-105D.

(2) Reliability Assurance Tests

To assure reliability of semiconductor devices, periodical reliability tests and reliability tests on individual manufacturing lot required by user are performed.

Table 1 Quality Control Check Points of Material and Parts (Example)

Material, parts	Important control items	Point for check
Wafer	Appearance	Damage and contamination on surface
	Dimension	Flatness
	Sheet resistance	Resistance
	Defect density	Defect numbers
	Crystal axis	
Mask	Appearance	Defect numbers, scratch
	Dimension	Dimension level
	Resistoration	
	Gradation	Uniformity of gradation
Fine wire for wire bonding	Appearance	Contamination, scratch, bend, twist
	Dimension	
	Purity	Purity level
	Elongation ratio	Mechanical strength
Frame	Appearance	Contamination, scratch
	Dimension	Dimension level
	Processing accuracy	
	Plating	Bondability, solderability
	Mounting characteristics	Heat resistance
Ceramic package	Appearance	Contamination, scratch
	Dimension	Dimension level
	Leak resistance	Airtightness
	Plating	Bondability, solderability
	Mounting characteristics	Heat resistance
	Electrical characteristics	
	Mechanical strength	Mechanical strength
Plastic	Composition	Characteristics of plastic material
	Electrical characteristics	
	Thermal characteristics	
	Molding performance	Molding performance
	Mounting characteristics	Mounting characteristics

Process		Control point	Purpose of control
▽ Purchase of material			
— Wafer —	Wafer	Characteristics, Appearance	Scratch, removal of crystal defect wafer
○ Surface oxidation	Oxidation		Assurance of resistance
□ Inspection on surface oxidation		Appearance, Thickness of oxide film	Pinhole, Scratch
○ Photo resist	Photo resist		
□ Inspection on photo resist		Dimension, Appearance	Dimension level
PQC level check			Check of photo resist
○ Diffusion	Diffusion	Diffusion depth, Sheet resistance	Diffusion status
□ Inspection on diffusion		Gate width	Control of basic parameters (V_{TH}, etc.) cleanness of surface
PQC level check		Characteristics of oxide film, Breakdown voltage	Prior check of V_{TH} Breakdown voltage check
○ Evaporation	Evaporation	Thickness of vapor film, Scratch, Contamination	Assurance of standard thickness
□ Inspection on evaporation			
PQC level check			
□ Wafer inspection	Wafer	Thickness, V_{TH} characteristics	Prevention of crack, Quality assurance of scribe
□ Inspection on chip electrical characteristics	Chip	Electrical characteristics	
○ Chip Scribe		Appearance of chip	
□ Inspection on chip appearance			
PQC lot judgement			
— Frame —			
○ Assembling	Assembling	Appearance after chip bonding Appearance after wire bonding	Quality check of chip Bonding Quality check of wire Bonding
PQC level check		Pull strength, Compression width, Shear strength	Prevention of open and short
□ Inspection after assembling		Appearance after assembling	
PQC lot judgement			
— Package —			
○ Sealing	Sealing	Appearance after sealing Outline, Dimension	Guarantee of Appearance and Dimension
PQC level check	Marking	Marking strength	
○ Final electrical inspection			
Failure analysis		Analysis of failures, Failure mode, Mechanism	Feedback of analysis information
□ Appearance inspection			
△ Sampling inspection on products			
○ Receiving			
Shipment			

Fig. 3 Example of Inner Process Quality Control

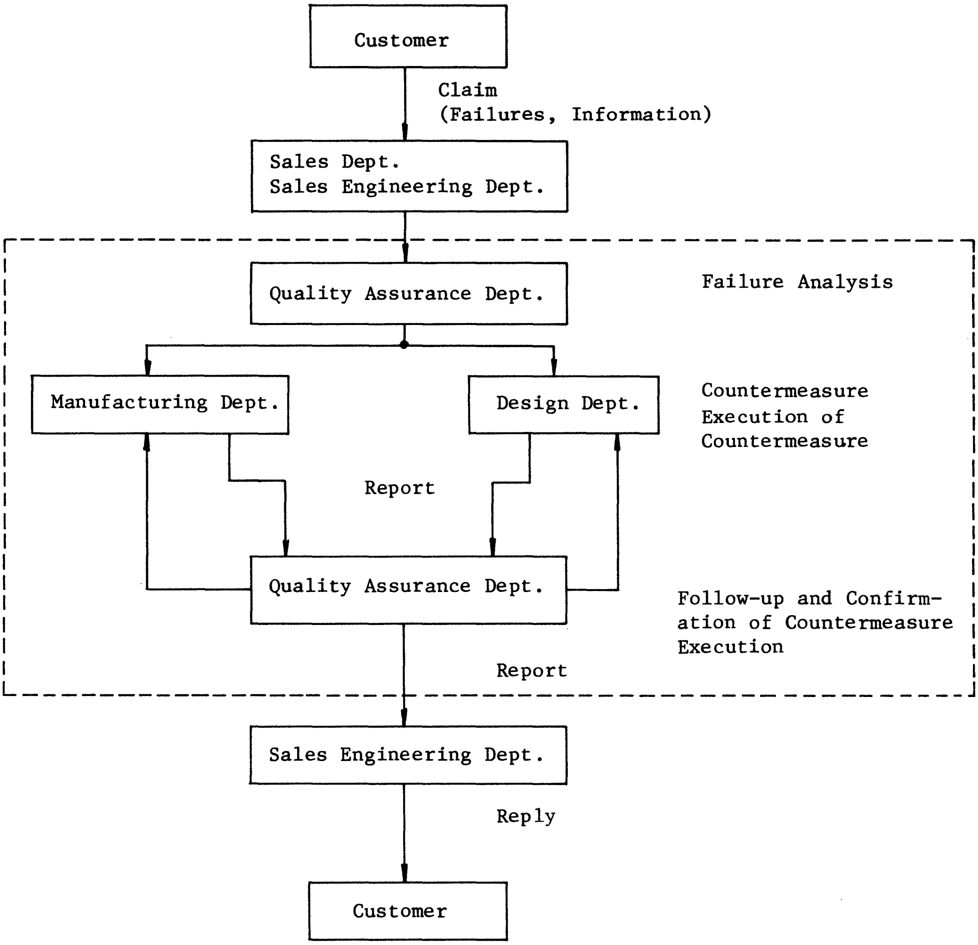


Fig. 4 Process Flow Chart of Field Failure

RELIABILITY TEST DATA OF LCD DRIVERS

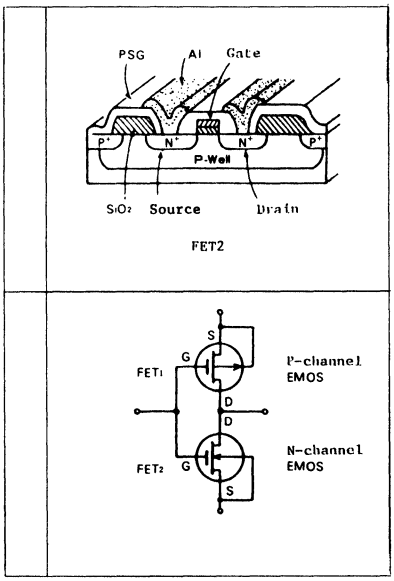
1. INTRODUCTION

The use of liquid crystal displays with microcomputer application systems has been increasing, because of their merits such as low power consumption, freedom in display pattern design, and thin shape. Low power consumption and high density packaging have been achieved through the use of the CMOS process and the flat plastic packages, respectively.

This chapter describes reliability and quality assurance data for Hitachi LCD driver LSIs based on test data and failure analysis results.

2. CHIP AND PACKAGE STRUCTURE

Hitachi LCD driver LSI family are produced in low power CMOS technology and flat plastic package. Si-gate process is used for high reliability and high density. Chip structure and basic circuit are shown in Fig. 1, and package structure is shown in Fig. 2.



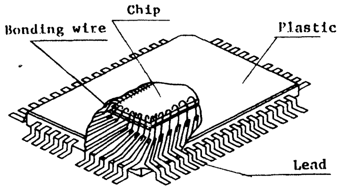


Fig. 2 Package Structure

Fig. 1 Chip Structure and Basic Circuit

3. RELIABILITY TEST RESULTS

The test results of LCD Driver LSI family are shown in Table 1, 2 and 3.

Table 1 Test Result (1), High Temperature Operation
($Ta=125°C$, $V_{CC}=5.5V$)

Device	Sample size	Component hour	Failure
HD44100H	40	40,000	0
HD44102CH	40	40,000	0
HD44103CH	40	40,000	0
HD44780	90	90,000	0
HD66100F	45	45,000	0
HD61100A	80	80,000	0
HD61102	50	50,000	0
HD61103A	50	50,000	0
HD61200	40	40,000	0
HD61202	50	50,000	0
HD61203	40	40,000	0
HD61104	45	45,000	0
HD61105	45	45,000	0
HD61830	40	40,000	0
HD61830B	40	40,000	0
HD63645	32	32,000	0
HD64645	32	32,000	0
HD61602	38	38,000	0
HD61603	32	32,000	0
HD61604	32	32,000	0
HD61605	32	32,000	0

Table 2 Test Result (2)

Test item	Test condition	Sample size	Component hour	Failure
High temp, storage	Ta=150°C, 1000 hrs.	180	1,800,000	0
Low temp, storage	Ta=-55°C, 1000 hrs.	140	1,400,000	0
Steady state humidity	65°C, 95% RH, 1000 hrs.	860	860,000	1*1
Steady state humidity biased	85°C, 90% RH, 1000 hrs.	165	170,000	2*2
Pressure cooker	121°C, 2 atm.100 hrs.	200	20,000	0

*1, *2: Aluminum corrosion

Table 3 Test Results (3)

Test items	Test condition	Sample size	Failure
Thermal shock	0 to 100°C 10 cycles	108	0
Temperature cycling	-55°C to 150°C 10 cycles	678	0
Soldering heat	260°C 10 sec.	283	0
Solderability	230°C 5 sec.	140	0

4. QUALITY DATA FROM FIELD USE

Field failure rate is estimated in advance through production process evaluation and reliability tests. Past field data on similar devices provides the basis for this estimation. Quality information from the users are indispensable to the improvement of products quality. Therefore, field data on products delivered to the users are followed up carefully. On the basis of information furnished by the user, failure analysis is conducted and the results are quickly fed back to the design and production divisions.

Failure analysis result on MOS LSI returned to Hitachi is shown in Fig. 3.

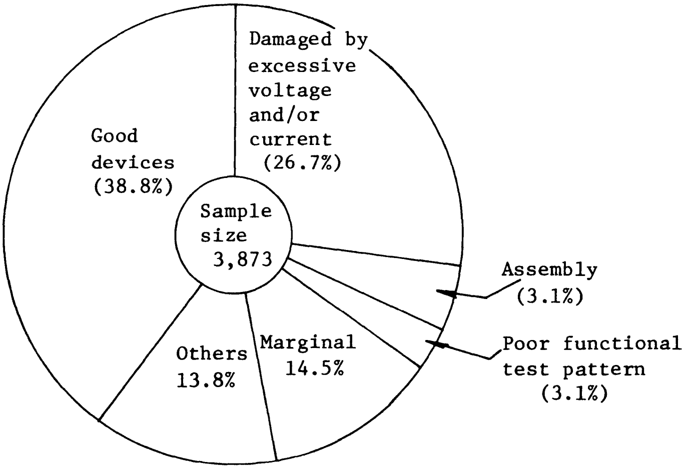


Fig. 3 Failure Analysis Result

5. PRECAUTION

5.1 Storage

It is preferable to store semiconductor devices in the following ways to prevent detrioration in their electrical characteristics, solderability, and appearance, or breakage.

(1) Store in an ambient temperature of 5 to 30°C, and in a relative humidity of 40 to 60%.

(2) Store in a clean air environment, free from dust and active gas.

(3) Store in a container which does not induce static electricity.

(4) Store without any physical load.

(5) If semiconductor devices are stored for a long time, store them in the unfabricated form. If their lead wires are formed beforehand, bent parts may corrode during storage.

(6) If the chips are unsealed, store them in a cool, dry, dark, and dustless place. Assemble them within 5 days after unpacking. Storage in nitrogen gas is desirable. They can be stored for 20 days or less in dry nitrogen gas with a dew point at -30°C or lower. Unpacked devices must not be stored for over 3 months.

(7) Take care not to allow condensation during storage due to rapid temperature changes.

5.2 Transportation

As with storage methods, general precautions for other electronic component parts are applicable to the transportation of semiconductors, semiconductor-incorporating units and other similar systems. In addition, the following considerations must be given, too:

(1) Use containers or jigs which will not induce static electricity as the result of vibration during transportation. It is desirable to use an electrically conductive container or aluminium foil.

(2) In order to prevent device breakage from clothes-induced static electricity, workers should be properly grounded with a resistor while handling devices. The resistor of about 1 M ohm must be provided near the worker to protect from electric shock.

(3) When transporting the printed circuit boards on which semiconductor devices are mounted, suitable preventive measures against static electricity induction must be taken; for example, voltage built-up is

prevented by shorting terminal circuit. When a belt conveyor is used, prevent the conveyor belt from being electrically charged by applying some surface treatment.

(4) When transporting semiconductor devices or printed circuit boards, minimize mechanical vibration and shock.

5.3 Handling for Measurement

Avoid static electricity, noise and surge-voltage when semiconductor devices are measured. It is possible to prevent breakage by shorting their terminal circuits to equalize electrical potential during transportation. However, when the devices are to be measured or mounted, their terminals are left open to provide the possibility that they may be accidentally touched by a worker, measuring instrument, work bench, soldering iron, belt conveyor, etc. The device will fail if it touches something which leaks current or has a static charge. Take care not to allow curve tracers, synchroscopes, pulse generators, D.C. stabilizing power supply units etc. to leak current through their terminals or housings.

Especially, while the devices are being tested, take care not to apply surge voltage from the tester, to attach a clamping circuit to the tester, or not to apply any abnormal voltage through a bad contact from a current source.

During measurement, avoid miswiring and short-circuiting. When inspecting a printed circuit board, make sure that no soldering bridge of foreign matter exists before turning on the power switch.

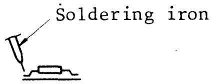
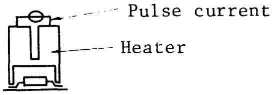
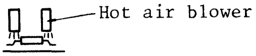
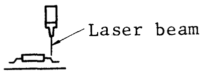
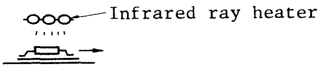
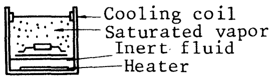
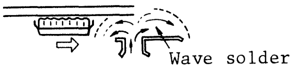
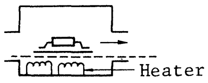
Since these precautions depend upon the types of semiconductor devices, contact Hitachi for further details.

6.0 METHODS AND STANDARD CONDITIONS FOR SOLDERING

Table 6-1 lists the major methods for soldering surface mount packages. The methods can be grouped into two broad categories: partial heat application methods whereby only the outer leads are heated, and overall heat application methods by which the PCB assembly including the packages, are heated.

The standard conditions with brief descriptions of each method are given 6.1 and 6.2. When selecting the best method, consider all advantages and disadvantages. Refer to the recommended method in 7.0 for each particular package type.

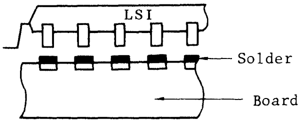
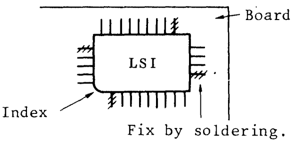
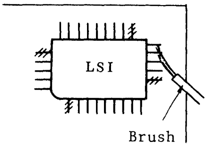
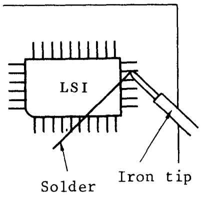
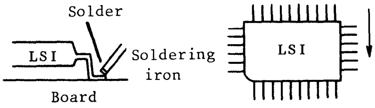
Table 6-1 Methods for Soldering Surface Mount Packages

	Method Name	Setup	Reference
Partial Heat Application Methods	Manual soldering		6.1
	Pulse heater soldering		
	Hot air soldering		
	Laser soldering		
Overall Heat Application Methods	Infrared reflow soldering		6.2
	Vapor phase reflow soldering		
	Dip soldering	 (solder vessel for surface mounting)	
	Furnace soldering		

6.1 Partial Heat Application Methods

Manual Soldering: A package is fixed to the predetermined position with flux or adhesive. With the package held in place, the leads are soldered. A pointed tip iron at 350°C is used with solder in narrow wire form typically 0.5 mm or less in diameter. Soldering time should be three seconds or less per pin. Table 6-2 shows typical processes for soldering an QFP.

Table 6-2 Typical Processes for QFP Soldering

Process	Procedure
Presoldering  	1. Solder-dip the footprint on the board. 2. Remove all bridges developed in dipping.
Positioning and temporary fixing  	1. Align the index markings. 2. Place a package on the footprint. 3. Check that the leads on four sides have been placed accurately on the footprint. 4. Fix four corners of the package by soldering. Any bridges between leads may be left as they are.
Flux application  	1. Using a brush, apply flux (rosin-based) to the leads and pattern. 2. Put a small quantity of flux into a container for use in each short session of flux application (approx. 4 hours). 3. At the end of each applying session, discard all the flux left in the container. Do not mix residual with replenished flux.
Soldering  	1. Move the soldering iron across leads while melting the solder.  Move soldering iron this way.

Pulse Heater Soldering: (source: Textbook for Internepcon JAPAN Seminar No. 10, Jan. 26, 1985). A pulse current is allowed to flow in a heater chip (collet). As Joule heat develops and flows in the chip, a prepared solder piece is melted instantaneously and pressed onto the required position by the chip. This method is noted for a minimum rise in the temperature of the entire package, but may not be suitable for mass production. It is suited for packages with their leads extending outward (gull-wing type), but not for those with leads bent inward (J-bend leads). Figure 6-1 shows typical structures of heater chips, and Table 6-3 lists representative conditions for pulse heater soldering.

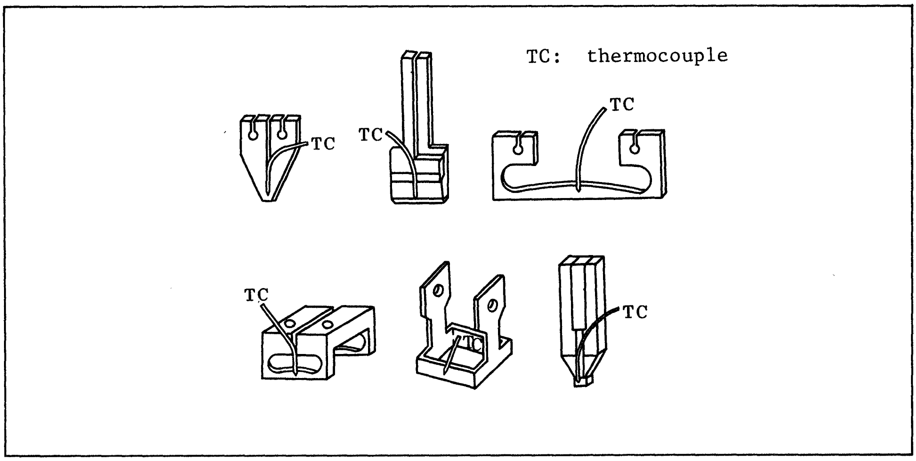


Figure 6-1 Typical Heater Chip Structures

Table 6-3 Typical Conditions for Pulse Heater Soldering

Item	Condition
Heating temperature	100 - 260°C
Heating time	5 - 10 sec.
Cooling time	5 - 10 sec.
Soldering pressure	8 - 28 kg*
Stroke	50 mm

*: From a compressed-air source of 4 kg/cm^2

Hot Air Soldering: Air or nitrogen gas is heated, and hot blasts are applied through a nozzle to melt-solder devices in place. This method requires gas at high flow rates because gas as a heat medium has low thermal conductivity and heat capacity. It is difficult to apply hot air under stabilized conditions. Figure 6-2 sketches a hot air soldering setup, and table 6-4 lists typical conditions for hot air soldering.

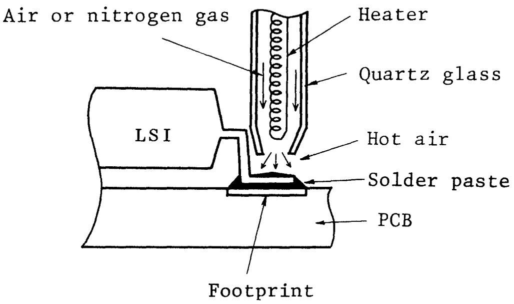


Figure 6-2 Setup for Hot Air Soldering

Table 6-4 Typical Conditions for Hot Air Soldering

Item	Condition
Hot air temperature	230 - 260°C
Air flow rate	25 - 30 ℓ/min
Soldering time*	3 - 10 s
Cooling time	5 - 10 s

*: Duration of hot air application

Laser Soldering: (source: Textbook for Internepcon JAPAN Seminar No. 10, Jan. 26, 1985) A laser beam is applied to the target position to melt solder. Laser sources include a ruby type, YAG (yttrium aluminum garnet) type, glass-fixed laser, and CO_2 (carbon dioxide gas) laser. Currently, CO_2 and YAG lasers are used. Table 6-5 compares the characteristics of the two laser types. The YAG laser may be more suitable than the CO_2 type since it provides higher heat exchange effectiveness over the metal surface to be soldered and a lower absorption factor for the board than the CO_2 laser.

Table 6-5 Comparing the CO_2 Laser and YAG Laser Characteristics

	Polyimide substrate	Tin-lead solder	Initial investment	Laser efficiency
CO_2 laser (10.6 μm)	2% in reflection factor (98% in absorption factor)	74% in reflection factor (26% in absorption factor)	1	10 - 15 %
YAG laser (1.06 μm)	27% in reflection factor (73% in absorption factor)	21% in reflection factor (79% in absorption factor)	2	1 %

Figure 6-3 illustrates a typical YAG laser soldering arrangement. The YAG laser output in continuous oscillation is from 50 W to 600 W depending on the lamp capacity and the volume of YAG crystal.

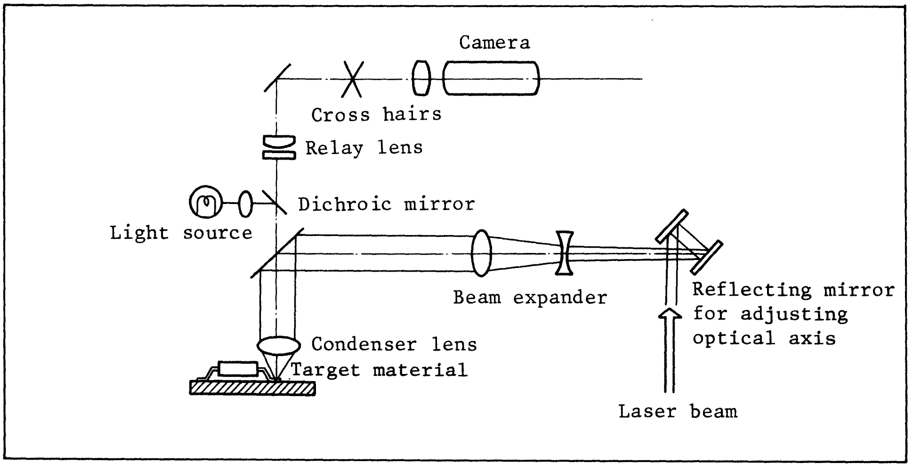


Figure 6-3 Typical YAG Laser Soldering Arrangement

6.2 Overall Heat Application Methods

Infrared Reflow Soldering: The infrared ray from a halogen lamp is condensed by a reflecting mirror into a hot beam for soldering. Because both point and line ray sources can be used, this method allows a large number of packages to be soldered at the same time. It is therefore suitable for mass production.

Infrared rays are divided into three groups: far infrared radiation (λ = 5.6-1000 μm), intermediate infrared radiation (λ = 1.5-5.6 μm) and near infrared radiation (λ = 0.7-1.5 μm). In many infrared ray reflow soldering setups, the preliminary heater emits far infrared (or intermediate) rays infrared and the main heater releases near infrared (or intermediate) rays.

Reflow conditions vary with the package shape, board configuration and soldering equipment. Figure 6-4 shows an example of infrared ray reflow soldering conditions for IC/LSI packages. The temperature measurement point in infrared reflow soldering varies depending on the package type and applicable chip. At Hitachi, the criteria for determining the position are set forth as follows:

- For temperature measurement on the package surface, the measuring position is a MOS package that incorporates a relatively large chip.
- For measurement on the board or lead surfaces, the measuring position is a bipolar package that incorporates a relatively small chip.
- Where MOS and bipolar packages coexist, the temperature is to be measured on MOS package surfaces.

Since plastic molded surface mount packages are black, the portion exposed to infrared rays readily absorbs heat, boosting the temperature of that portion higher than that of the leads. This problem is bypassed by two measures: cooling the package during reflowing, or placing a white metal reflector on the surface of the package to subdue the energy absorption and create a lower temperature inside the package. Figure 6-5 illustrates a typical temperature profile when a reflector is used.

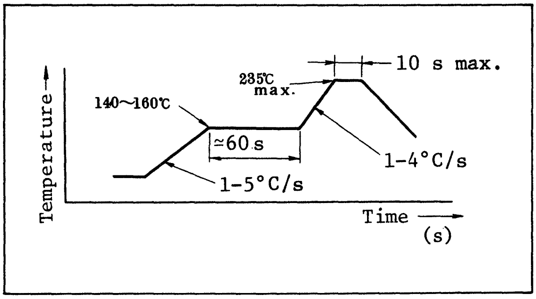


Figure 6-4 Typical Conditions for Infrared Reflow Soldering

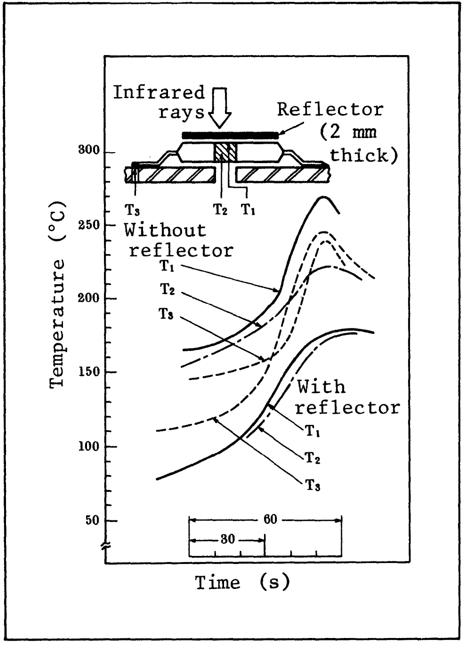


Figure 6-5 Typical Temperature Profile with Reflector Used

Figure 6-6 and table 6-6 depict typical reflow conditions for transistor packages.

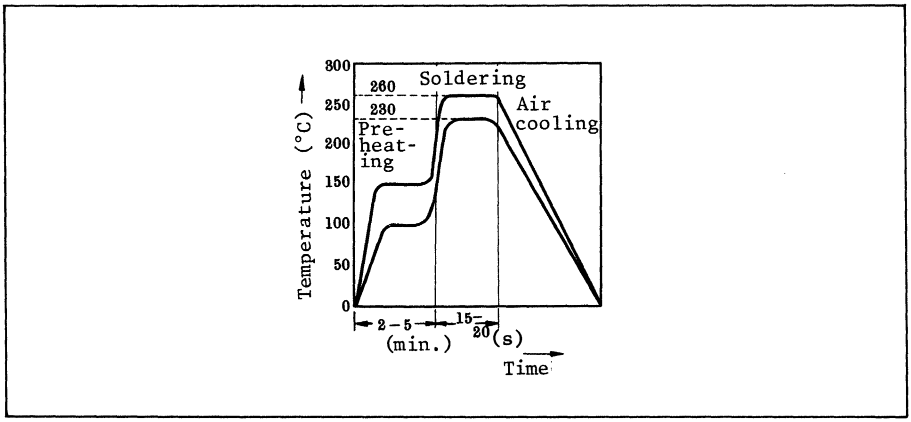


Figure 6-6 Example of Temperature Profile

Table 6-6 Typical Reflow Conditions

Item	CMPAK, MPAK, MPAK-4 FPAK, UPAK	DPAK
Soldering temperature (board temperature)	230 - 260°C (reference solder melting point + 50°C)	220°C max.
Soldering time	15 - 20 sec.	40 s. max
Preheating temperature	100 - 150°C	160°C
Preheating time	2 - 5 min.	5 min.

Vapor Phase Reflow Soldering: A special high boiling point solvent (for example fluorocarbon type) is heated to generate a vapor layer. As the entire board is passed through the layer, the latent heat of vaporation causes the solder to reflow. This method offers the following advantages:

- o The temperature can be kept constant. Since the solvent vapor is used, the reflow temperature is determined by the boiling point of the solvent to eliminate the likelihood of overheating.
- o Damage to components and boards can be avoided due to virtually uniform thermal conduction regardless of the configuration of the solderable assemblies.
- o Numerous components of different shapes can be subjected to simultaneous reflow soldering. The use of solvent vapor permits reflow soldering at multiple positions simultaneously that eliminate most constraints from different component shapes. This feature applies particularly to J-bend type devices whose leads are partially located under the package.
- o The inert reflow atmosphere prevents solder oxidation or flux baking. Any residual flux can be readily removed by conventional techniques.

Figure 6-7 shows typical conditions for vapor phase reflow soldering.

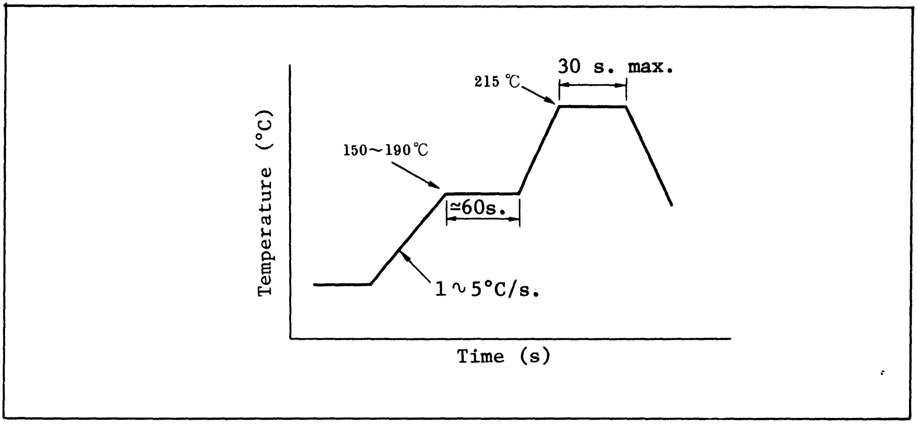
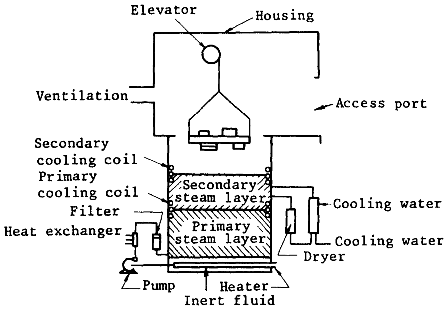


Figure 6-7 Typical Conditions for Vapor Phase Reflow Soldering

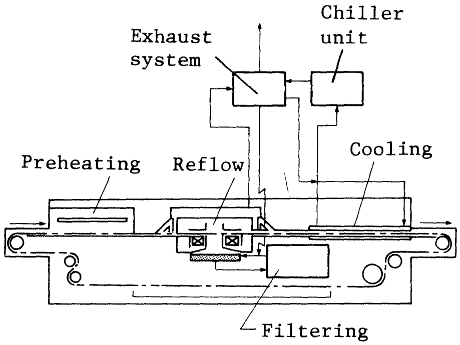
Table 6-7 Properties of Solvents for Vapor Phase Reflow Soldering (source: manufacturers catalogs)

Product name	FC-70	FC 5311	GALDEN LS230	GALDEN HS260
Manufacturer	3M (U.S.A.)	ISC chemical (UK)	Montefluos S.P.A. (Italy)	Montefluos S.P.A. (Italy)
Distributor	Sumitomo 3M	Sumitomo 3M	Montedison Japan	Montedison Japan
Molecular formula	$(C_5F_{11})_3N$ tributylamine		$CF_3-(O-\overset{CF_3}{CF}-CF_2)n-(O-CF_2)m-OCF_3$ Perfloralkyl-polyether	
Molecular weight	820	624	800	900
Boiling point (°C)	215	215	220 - 235	250 - 265
Specific gravity (g/mℓ)	1.94	2.03	1.824	1.840
Vapor pressure (mmHg)	<0.1	<0.1	5×10^{-3}	5×10^{-4}
Specific heat (cal/°C.g)	0.25	0.25	0.24	0.24
Thermal conductivity (cal/g.°C.s)	1.6×10^{-4}	1.26×10^{-4}	1.67×10^{-4}	1.67×10^{-4}
Surface tension (dyne/cm)	18	19	18	18
PFIB generation	Less than 5 ppm in solvent, less than 0.03 ppm at opening	<1 ppb	<0.5 ppb	<0.5 ppb

Figure 6-8 sketches two types of vapor phase reflow soldering equipment (in-line and batch type), and table 6-7 lists the properties of solvents available for vapor phase reflow soldering. The in-line type is suited for mass production, and the batch type for low or medium production as well as for research and development purposes. Both types need adequate ventilation during operation. Consult the equipment manufacturer, material vendor and appropriate occupational operating standards for ventilation requirements.



Structure of Batch Type Equipment



In-line System Configuration (source: Catalog of Hitachi Technoengineering, Ltd.)

Figure 6-8 Vapor Phase Reflow System

Dip Soldering: A package is fixed temporarily on the board by adhesive. With the component side facing downward, the package is passed through molten solder. Figure 6-9 depicts the process flow for dip-soldering 18- and 28-pin MSPs. Compared with reflow methods, this method exerts extremely high thermal stress on semiconductor chips. Adverse effects from the stress should be avoided by providing a preheating zone to soften thermal shock and minimizing the soldering time. Figure 6-10 shows a typical temperature profile for dip soldering.

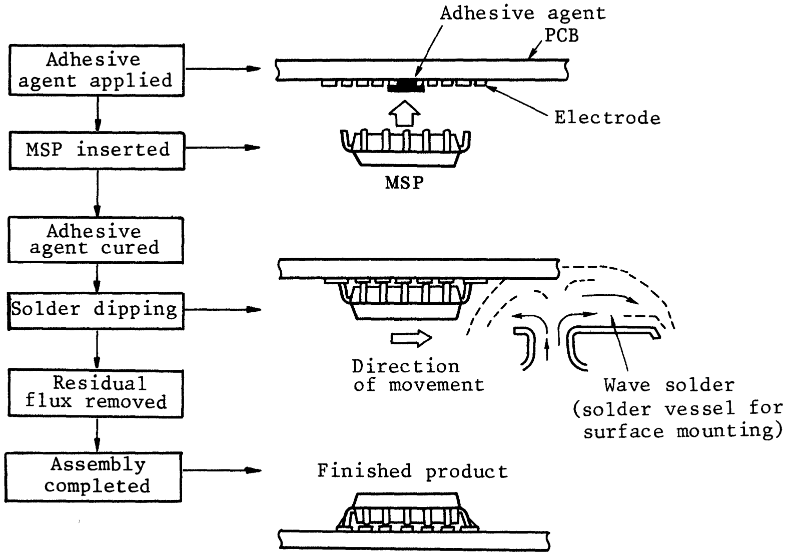


Figure 6-9 Flow of Processes for Solder-Dipping 18- and 28-Pin MSPs

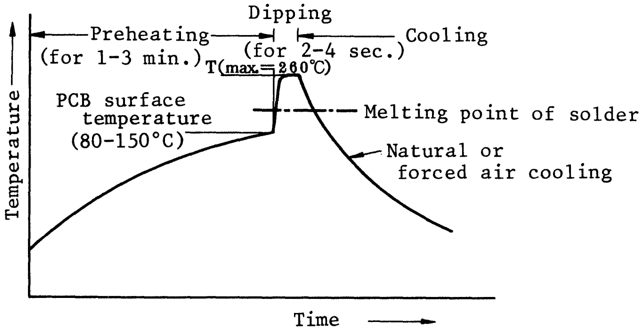


Figure 6-10 Temperature Profile of Solder-Dipped Soldering

Furnace Soldering: (source: technical information from Senju Metal Co.) The PCB is placed on a thin heat-resistant belt. As the PCB advances, the belt is heated from below by hot plates to reflow the solder. This method provides high processing capacity, and the equipment required is relatively inexpensive. This method, however, is not suitable for boards with low resistance to heat, poor thermal conductivity or complicated shapes. Figure 6-11 outlines a typical furnace soldering setup, and figure 6-12 depicts a typical temperature profile of this method.

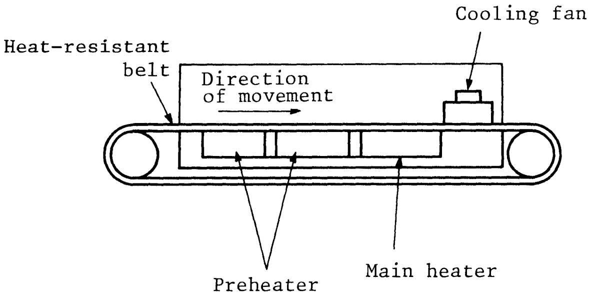


Figure 6-11 Furnace Soldering Setup

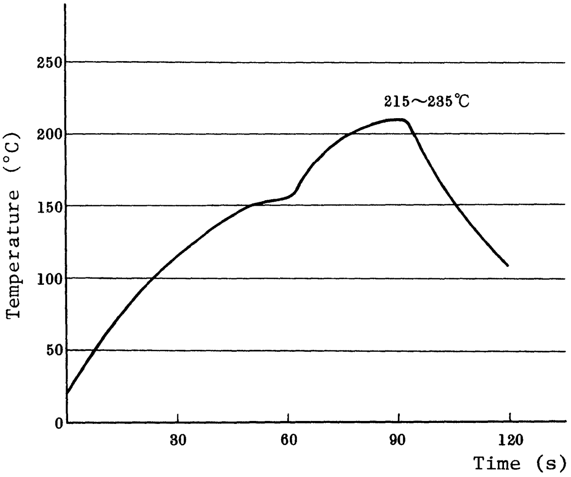


Figure 6-12 Typical Temperature Profile of Furnace Soldering

7.0 RECOMMENDED MOUNTING METHODS FOR EACH PACKAGE TYPE

Table 7-1 lists the recommended mounting methods for each of the package types now on the market.

Table 7-1 Recommended Mounting Methods for Each Package

Mounting methods		IC/LSI packages						Discrete packages					
		QFP (plastic)	SOP	MSP	PLCC /SOJ	QFP (ceramic)	LCC	MPAK	UPAK	FPAK	DPAK	LLD	SRP
Partial heat application methods	Manual soldering	○	○	○	○	○	×	○	○	○	○	○	○
	Pulse heater soldering	○	○	×	×	○	×	○	○	○	○	○	○
	Hot air soldering	○	○	○	○	○	○	○	○	○	○	○	○
	Laser soldering	○	○	○	○	○	×	○	○	○	○	○	○
Overall heat application methods	Infrared reflow soldering	○	○	○	○	○	○	○	○	○	○	○	○
	Vapor phase reflow soldering	○	○	○	○	○	○	○	○	○	○	○	○
	Dip-soldering	×	Note 1	Note 2	×	×	×	○	○	○	× Note 3	○	○
	Furnace soldering	○	○	○	○	○	○	○	○	○	○	○	○

Notes 1. Recommended for SOPs with 20 pins or less, but unsuitable for SOPs with 24 or 28 pins.

2. Recommended, or possible for MSPs with 44 or more pins.

3. Methods indicated as unsuitable may apply depending on the specific product. For more information, consult your Hitachi representative.

4. (○ : Suitable; × : unsuitable)

When determining conditions for the mounting method selected, refer to the temperature profile examples in 6.0. The symbols used in the table have the following meanings:

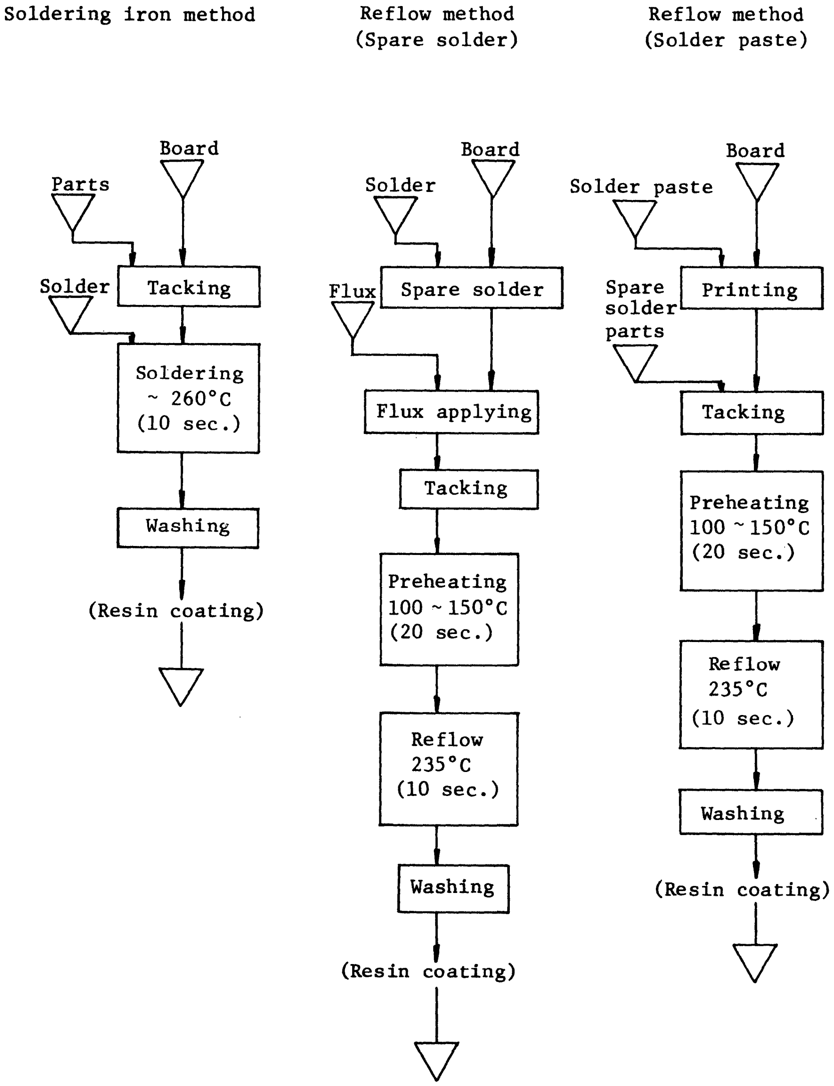
○ (suitable): Use this method by considering the temperature profile inside the package, temperature rise gradient, change in soldering conditions, and solderability.

× (unsuitable): Do not use this method.

The soldering methods are divided into the three groups above with emphasis placed on thermal stress on components and solderability. Productivity and the costs also be analyzed.

Notice that methods are recommended for each package type. Where different package types coexist, select the soldering method suitable for the package type most vulnerable to thermal stress.

Flowcharts of Mounting Methods



Liquid Crystal Driving Methods

Driving a liquid crystal at direct current triggers electrode reaction inside the liquid cell, deteriorating display quality rapidly. The liquid crystal must be driven at alternating current. The AC driving method includes the static driving method and the multiplex driving method, each of which has the features and can be used for applications. Hitachi has been developping the LCD driver devices corresponding to the static driving method and the multiplex driving method. The following sections describe the features of each driving method, the driving waveforms and how to apply bias.

STATIC DRIVING METHOD

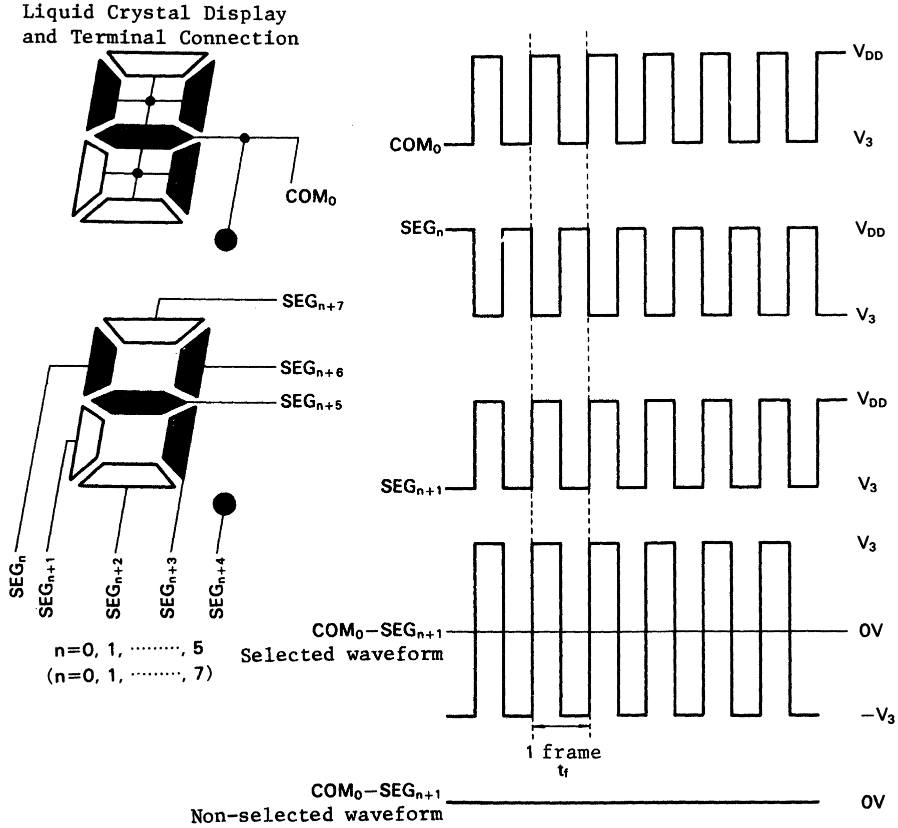


Fig. 1 Example of Static Drive Waveforms
(Example of HD61602/HD61603)

Fig. 1 shows the driving waveforms of the static driving method and an example in which "4" is displayed in the segment method. The static driving method is the most basic method in which good display quality can be obtained. However, it is not suitable for the display of the liquid crystal with many segments because one liquid crystal driver circuit is required per segment. The static driving method is used at the frame frequency ($1/t_f$) of several tens to several hundreds Hz.

▌MULTIPLEX DRIVING METHOD

The multiplex driving method is effective in reducing the number of driver circuits, the number of connections between the circuit and the display cell, and the cost when driving many display picture elements. Fig. 2 shows the comparision of the static drive with the multiplex drive (1/3 duty) in 8-digit numeric display. The number of liquid crystal driver circuits required is 65 for the former and 27 for the latter. The multiplex drive reduces the number of driver circuits. However, the more multiplexed, the

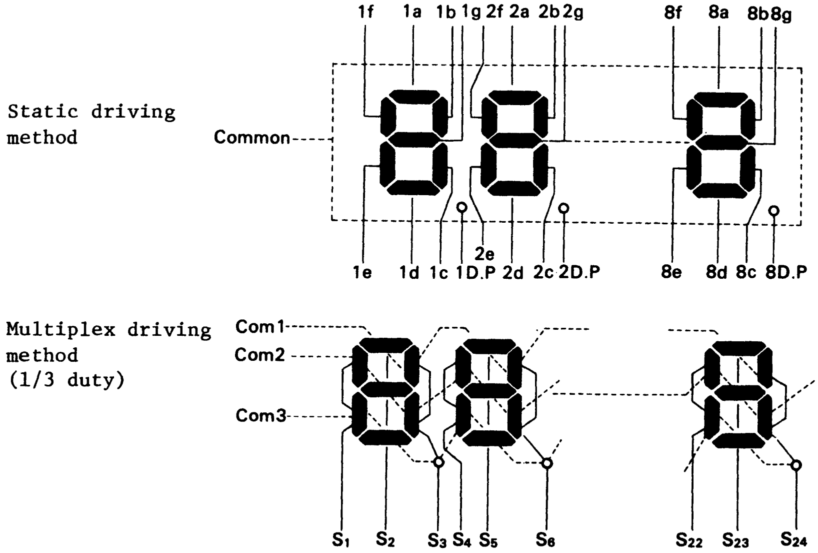


Fig. 2 Example of Comparision of Static Drive with Multiplex Drive

smaller the driving voltage tolerance. Thus, there are limits to extent of multiplexing.

There are two types of multiplex drive waveforms: A type and B type. A type, shown in Fig. 3, is used for alternation in 1 frame. B type is used for alternation in between 2 frames. B type has better display quality than A type in high multiplex drive.

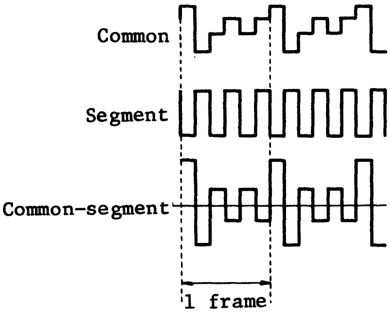


Fig. 3 A Type Waveforms
(1/3 duty, 1/3 bias)

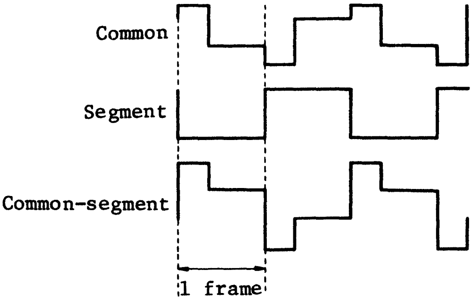


Fig. 4 B Type Waveforms
(1/3 duty, 1/3 bias)

● 1/2 Bias, 1/2 Duty Drive

In the 1/2 duty drive, 1 driver circuit drives 2 segments. Fig. 5 shows an example of the connection in displaying '4' on the liquid crystal display of 7-segment type, and the output waveforms.

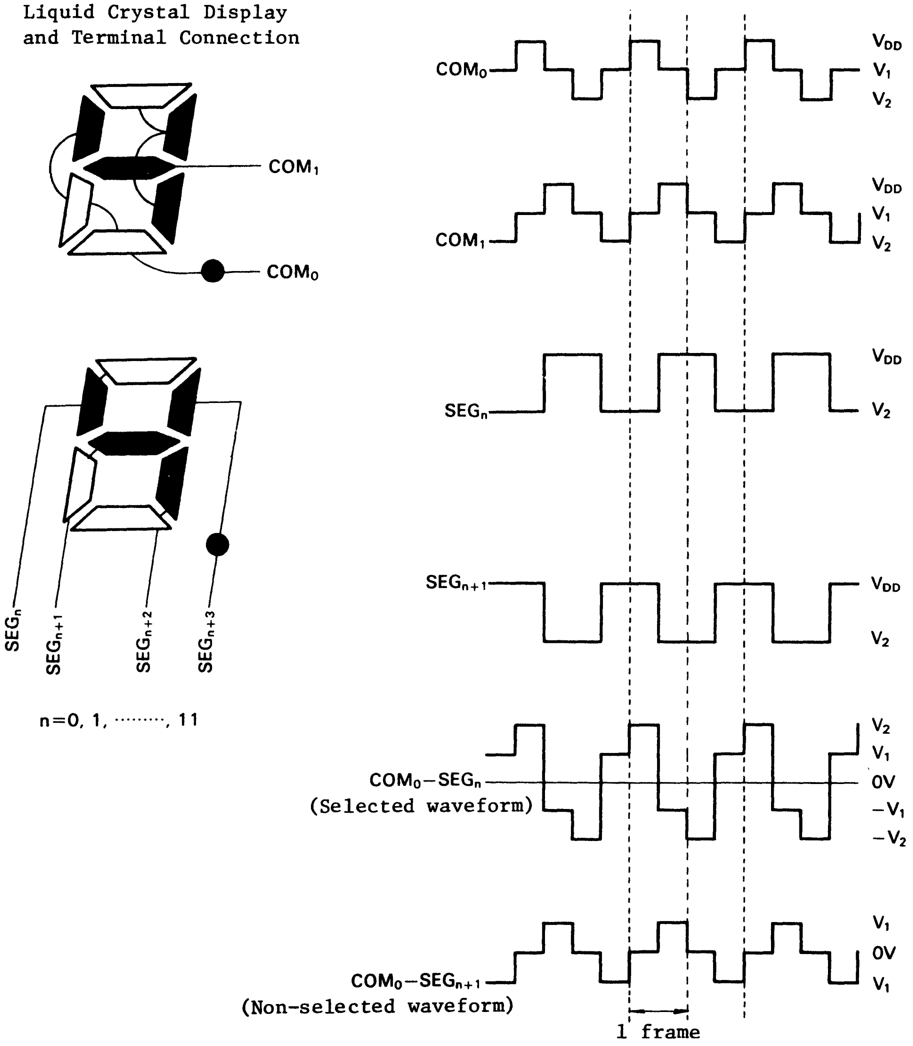


Fig. 5 Example of Waveforms in 1/2 Duty Drive (B type)
(Example of HD61602)

- **1/3 Bias, 1/3 Duty Drive**

In the 1/3 duty drive, 3 segments are driven by 1 segment output driver. Fig. 6 shows an example of the connection in displaying '4' on the liquid crystal display of 7-segment type, and the output waveforms.

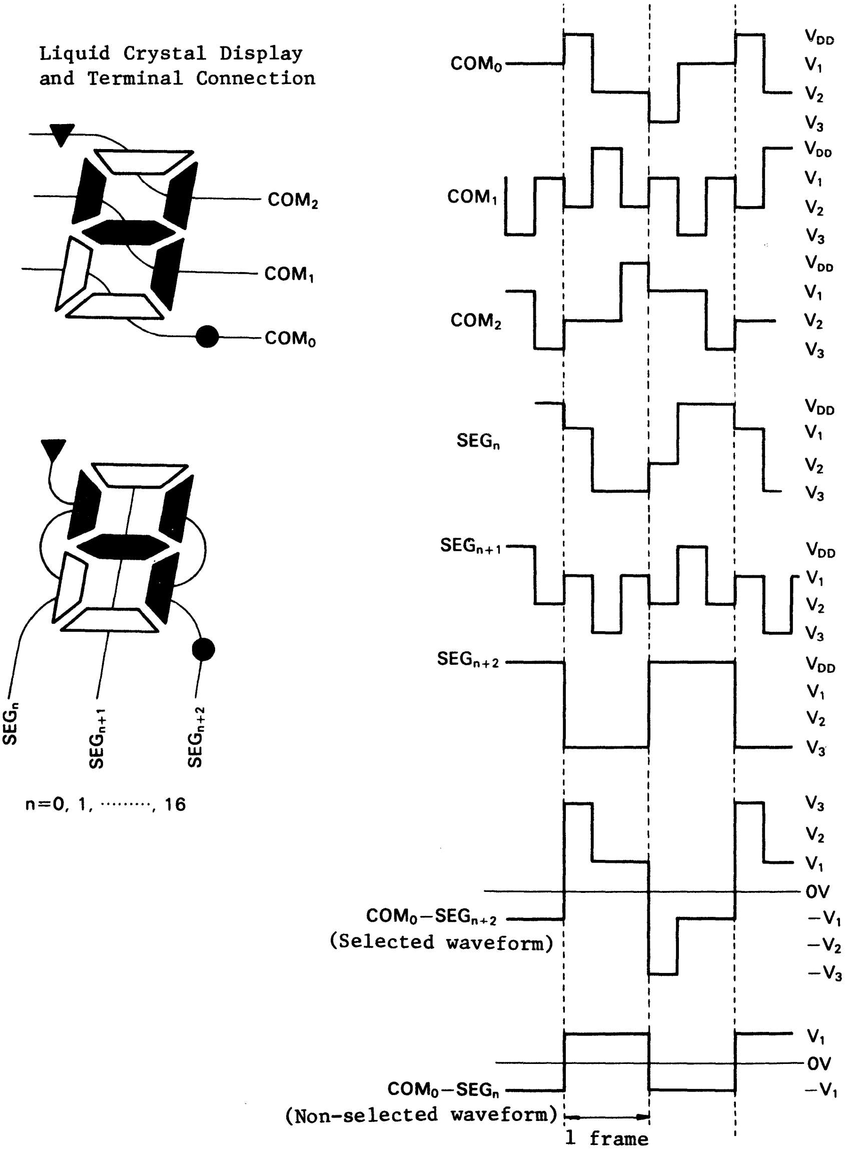

Liquid Crystal Display and Terminal Connection

Fig. 6 Example of Waveforms in 1/3 Duty Drive (B type)
(Example of HD61602)

●1/3 Bias, 1/4 Duty Drive

In the 1/4 duty drive, 4 segments are driven by 1 segment output driver. Fig. 7 shows an example of the connection in displaying '4' on the liquid crystal of 7-segment type, and the output waveforms.

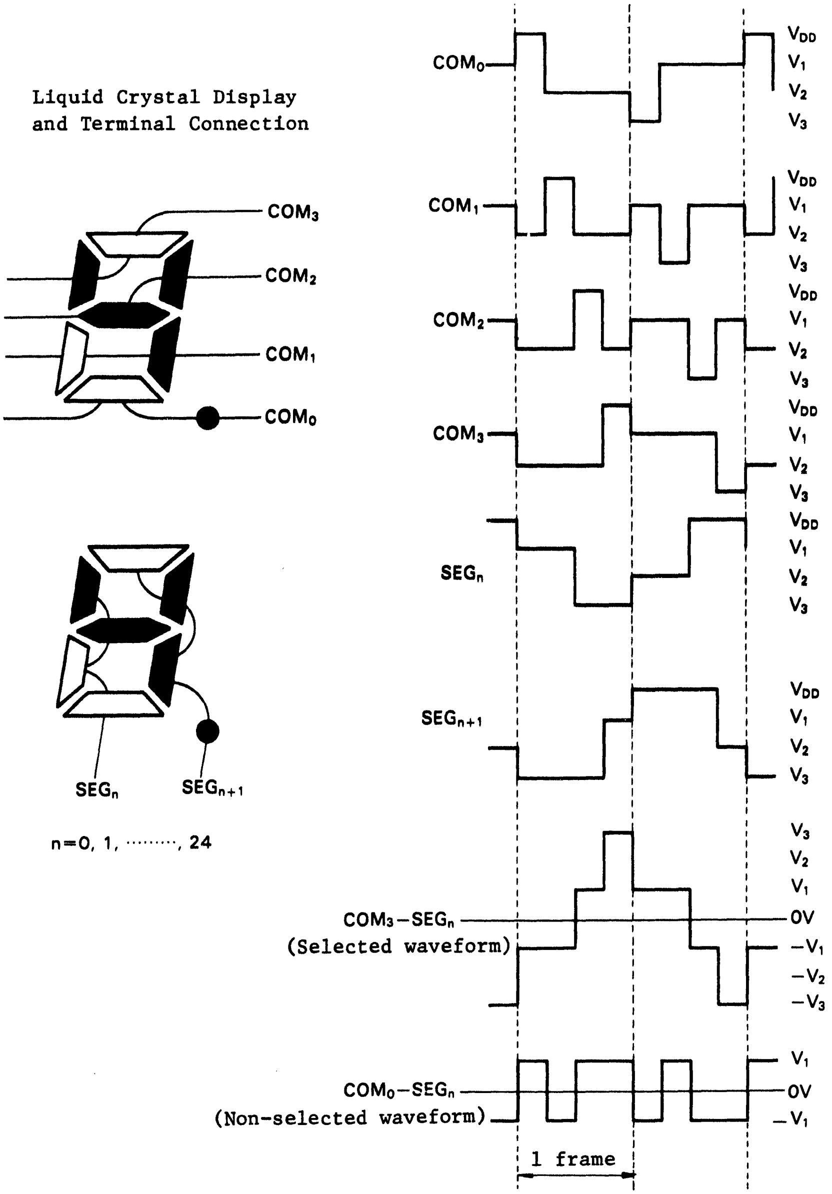
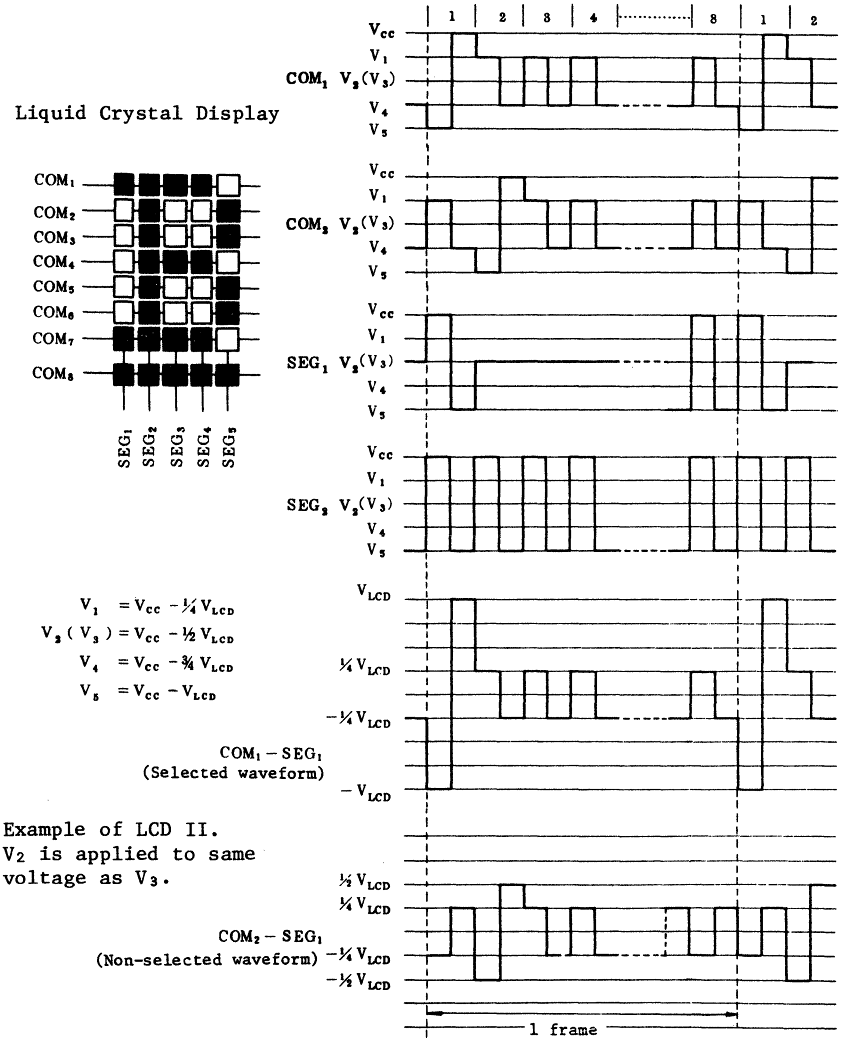


Fig. 7 Example of Waveforms in 1/4 Duty Drive (B type)
(Example of HD61602)

- 1/4 Bias, 1/8 Duty Drive



$V_1 = V_{cc} - \frac{1}{4} V_{LCD}$

$V_2 (V_3) = V_{cc} - \frac{1}{2} V_{LCD}$

$V_4 = V_{cc} - \frac{3}{4} V_{LCD}$

$V_5 = V_{cc} - V_{LCD}$

* Example of LCD II.
V_2 is applied to same
voltage as V_3.

Fig. 8 Example of Waveforms in 1/8 Duty Drive (A type)
(Example of LCD-II)

- 1/5 Bias, 1/8 Duty Drive

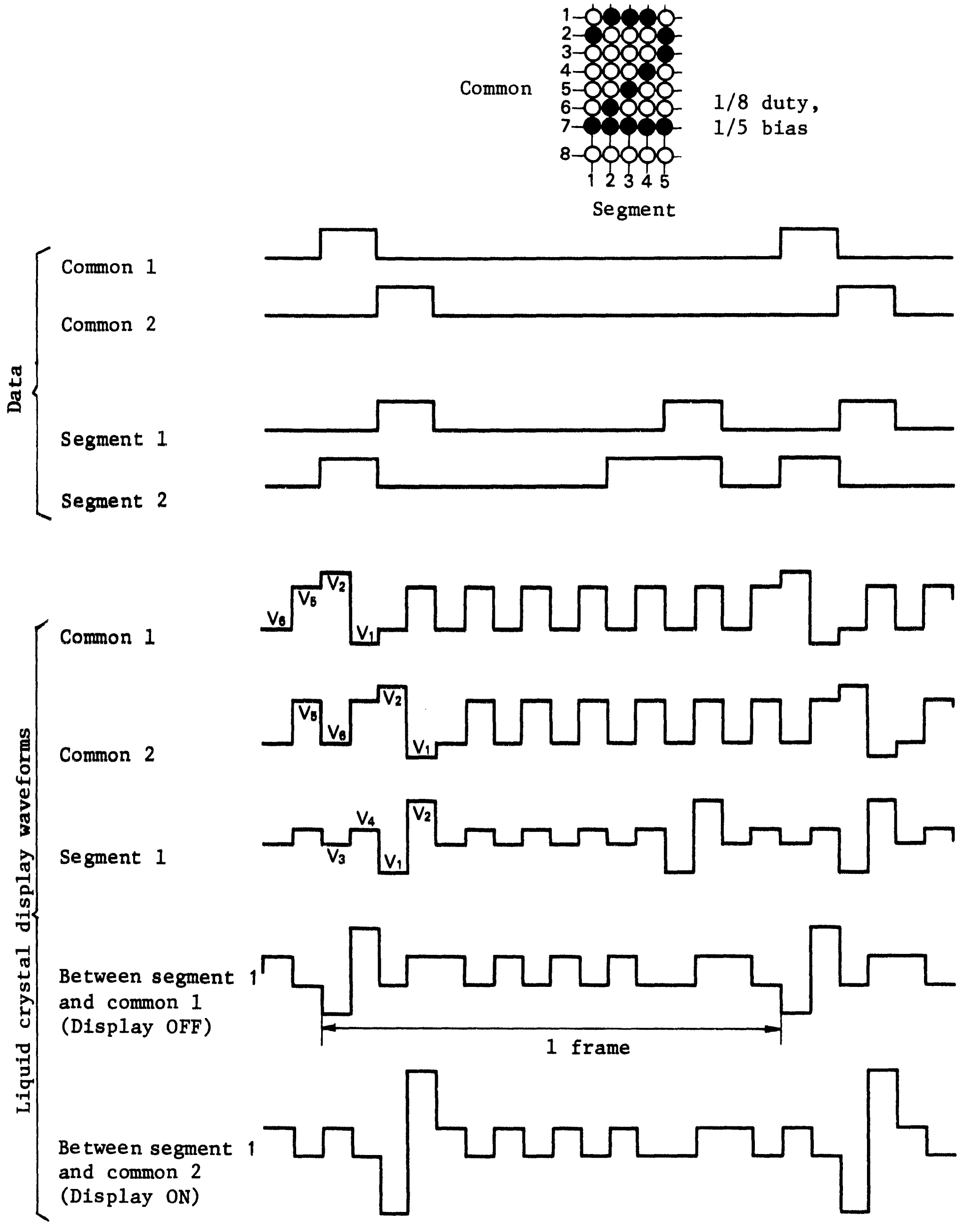
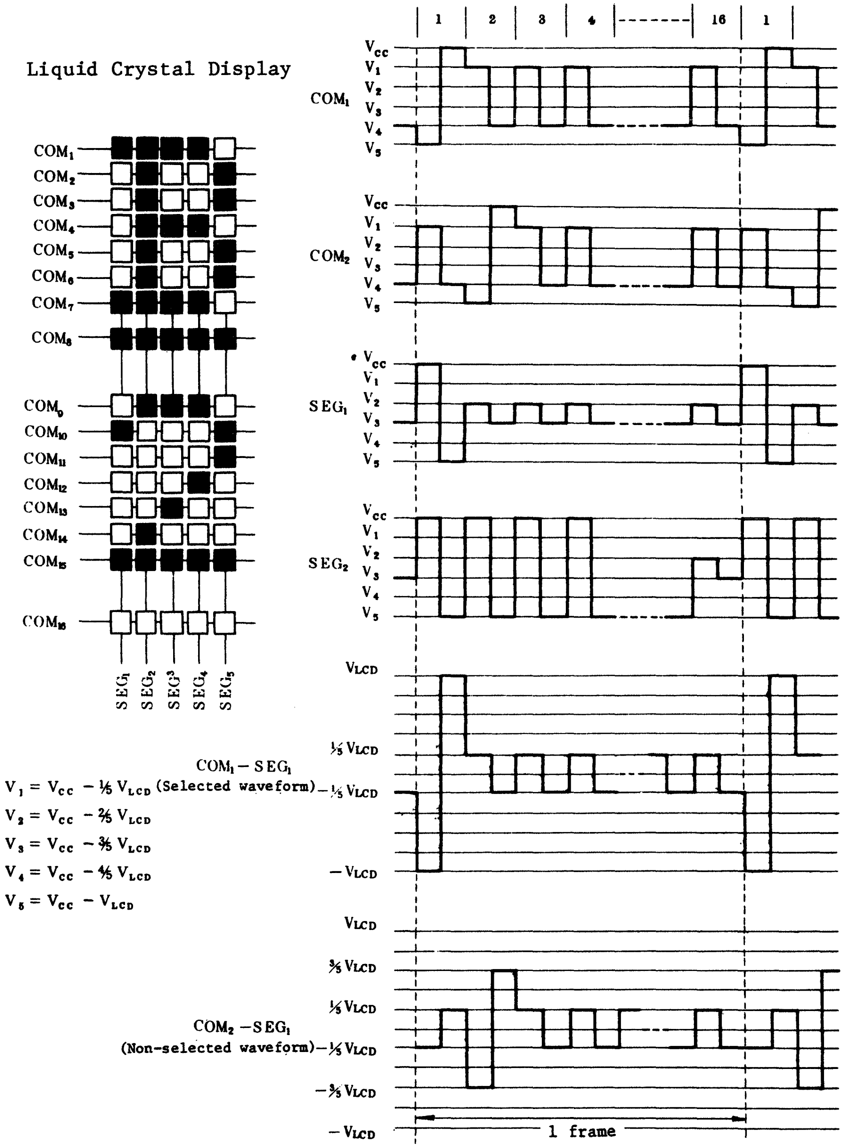


Fig. 9 Example of Waveforms in 1/8 Duty Drive (A type)
(Example of HD44100H)

- 1/5 Bias, 1/16 Duty Drive



$V_1 = V_{cc} - \frac{1}{5} V_{LCD}$

$V_2 = V_{cc} - \frac{2}{5} V_{LCD}$

$V_3 = V_{cc} - \frac{3}{5} V_{LCD}$

$V_4 = V_{cc} - \frac{4}{5} V_{LCD}$

$V_5 = V_{cc} - V_{LCD}$

Fig. 10 Example of Waveforms in 1/16 Duty Drive (A type)
(Example of LCD-II)

- 1/5 Bias, 1/32 Duty Drive

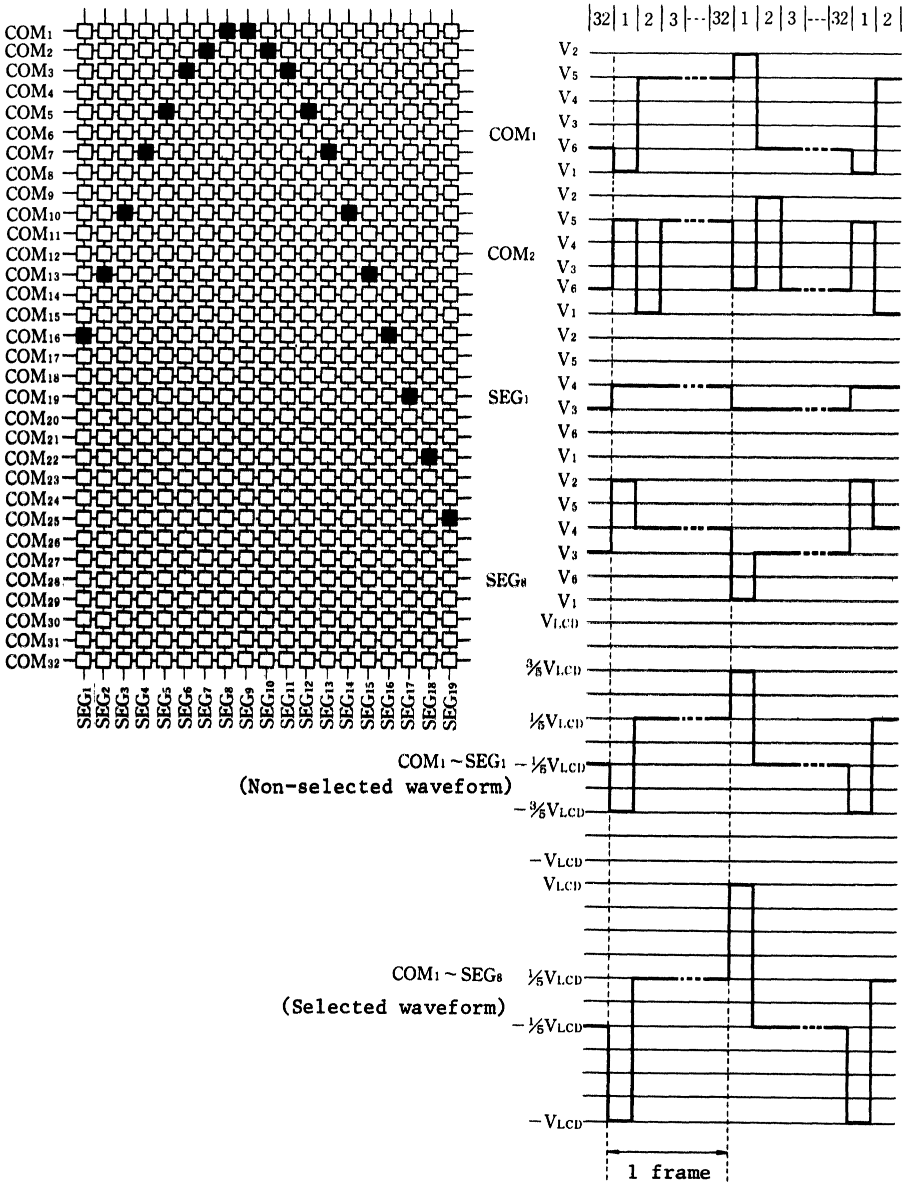


Fig. 11 Example of Waveforms in 1/32 Duty Drive
(Example of HD44102CH, HD44103CH)

POWER SUPPLY CIRCUIT FOR LIQUID CRYSTAL DRIVE

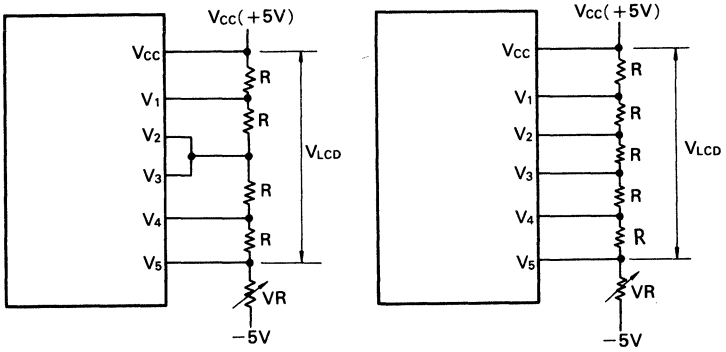
Table 1 shows the relationship between the number of driving biases and display duty ratios.

Table 1 Relationship between the Number of Dispaly Duties Ratio and the Number of Driving Biases

Display duty ratio	Static	1/2	1/3	1/4	1/7	1/8	1/11	1/12	1/14	1/16	1/24	1/32	1/64
Number of driving biases	2	3 (1/2 bias)	4 (1/3 bias)		5 (1/4 bias)				6 (1/5 bias)				

● Drive in Resistance Dividing

A driving bias is generally generated in resistance dividing.



(a) 1/4 Bias (1/8, 1/11 duty) (b) 1/5 Bias (1/16 duty)

Fig. 12 Example of Driving Voltage Supply

The setting of resistance value is determined by considering of operation margine and power consumption. Since the liquid crystal display load is capacitive, the drive waveform itself is distorted due to charge/discharge current when the liquid crystal display drive waveform is applied. To reduce distortion, the resistance value should be decreased but the power consumption increases because of the increase of the current through the dividing resistors. Since larger liquid crystal display panels have larger capacitance, the resistance value must be decreased.

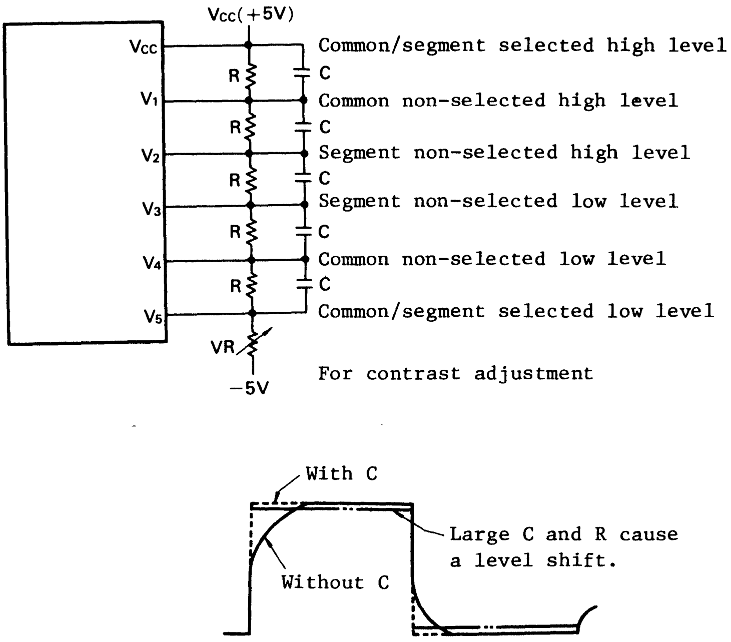

Vcc(+5V)
Vcc
V1
V2
V3
V4
V5
R
R
R
R
R
C
C
C
C
C
VR
-5V
Common/segment selected high level
Common non-selected high level
Segment non-selected high level
Segment non-selected low level
Common non-selected low level
Common/segment selected low level
For contrast adjustment
With C
Large C and R cause a level shift.
Without C

Fig. 13 Example of Capacitor Connection for Improvement of Liquid Crystal Display Drive Waveform Distortion (1/5 bias) (Example of LCD-II)

It is efficient to connect a capacitor to the resistors in parallel as shown in Fig. 13 in order to improve charge/discharge distortion. However, the effect is limited. Even if it is attempted to reduce the power consumption with a large resistor and improve waveform distortion with a large capacitor, a level shift occurs and the operating margine is not improved.

Since the liquid crystal display load is of matrix configuration, the path of the charge/discharge current through the load is complicated. Moreover, it varies depending on display condition. Thus, a value of resistance cannot be simply determined from the load capacitance of liquid crystal display. It must be experimentally determined according to the demand for the power consumption of the equipment in which the liquid crystal display is incorporated.

Generally, R is 1kΩ to 10kΩ, and VR is 5kΩ to 50kΩ. No capacitor is used. A capacitor of 0.1μF is usually used if necessary.

● Drive by Operational Amplifier

In graphic display, the size of liquid crystal becomes larger and the display duty ratio becomes smaller, then the stability of liquid crystal drive level is more important than small display system.

Since the liquid crystal for graphic display is large and has many picture elements, the load capacity becomes large. The high impedance of the power supply for liquid crystal drive produces distortion in the drive waveforms, and deteriorates display quality. For this reason, the liquid crystal drive level should be low impedance with operational amplifiers. Fig. 14 shows an example of operational amplifier configuration.

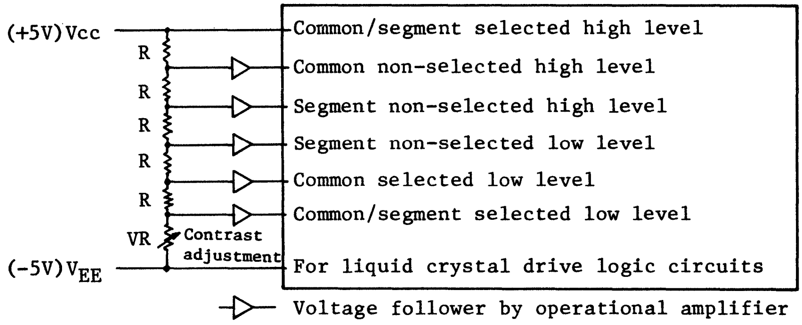

(+5V)Vcc
R
R
R
R
R
VR
Contrast adjustment
(-5V)V_{EE}
Common/segment selected high level
Common non-selected high level
Segment non-selected high level
Segment non-selected low level
Common selected low level
Common/segment selected low level
For liquid crystal drive logic circuits
Voltage follower by operational amplifier

Fig. 14 Drive by Operational Amplifier (1/5 bias)

No load current flows through the dividing resistors because of the high input impedance of operational amplifier. A high resistance of R = 10kΩ and VR = 50kΩ can be used.

● Generation of Liquid Crystal Drive Level in LSI

The power supply circuit for liquid crystal drive level may be incorporated in the LSI such as for portable calculator with liquid crystal display.

HD61602, HD61603 for small display system has built-in power supply circuit for liquid crystal drive level.

● Precaution on Power Supply Circuit

The LCD driver LSI has two types of power supplies: the one for logical circuits and the other for liquid crystal display drive circuit. The power supply system is complicated because of several liquid crystal drive levels.

For this reason, in the power supply design, take care not to deviate from the voltage range assured in the maximum rating at the rise of power supply and from the potential sequence of each power supply. If the input terminal level is indefinite, through current flows and the power consumption increases because of the use of CMOS process in the LCD driver. Simultaneously, the potential sequence of each power supply becomes wrong, and a latch-up phenomenon may be caused.

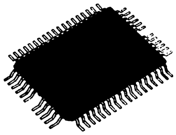
Data Sheet

HD44100H
(LCD Driver with 40-Channel Outputs)

DESCRIPTION

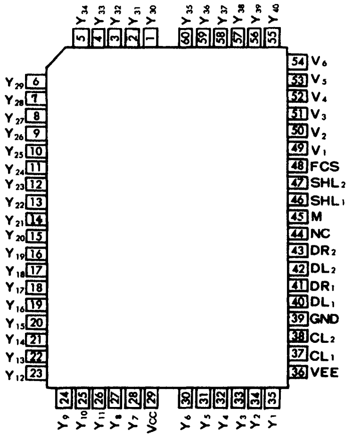
The HD44100H has two sets of 20-bit bidirectional shift registers, 20 data latch flip flops and 20 liquid crystal display driver circuits. It receives serial display data from a display control LSI, converts it into parallel data and supplies liquid crystal display waveforms to the liquid crystal.

The HD44100H is a liquid crystal display driver with high generalizability, which can drive a static drive liquid crystal and a dynamic drive liquid crystal, and can be applied to a common driver or segment driver.



(FP−60)

■ PIN ARRANGEMENT



(Top View)

■ FEATURES

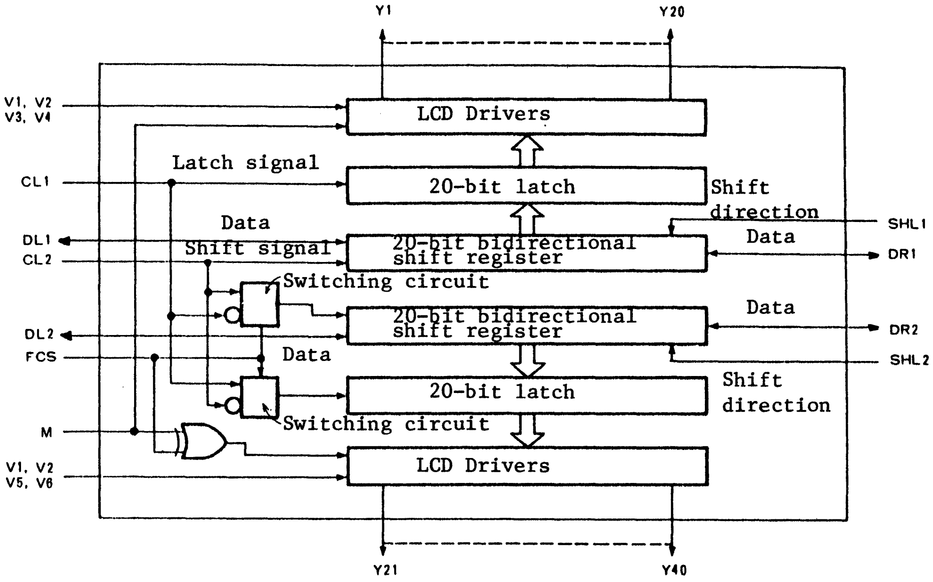
- Liquid crystal display driver with serial/parallel conversion function
- Serial transfer facilitates board design
- Capable of interfacing to liquid crystal display controllers: HD43160AH, LCTC (HD61830), LCD II (HD44780), LCDIII (HD44790).
- Internal liquid crystal display driver ... 40 drivers
- Internal serial/parallel conversion circuits
  20-bit shift register × 2
  20-bit data latch × 2
- Display bias: Static ∿ 1/5

- Power supply

  Internal logic: +5V
  Liquid crystal display driver circuit: -5V

- The separation of internal logic from liquid crystal display driver circuit allows applicable controllers and liquid crystal types to increase.
- CMOS process
- 60-pin flat plastic package

■BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Value	Unit
Supply voltage	Logic	V_{CC} *1	- 0.3 to + 7.0	V
	LCD drivers	V_{EE} *2	V_{CC} - 13.5 to V_{CC} + 0.3	V
Input voltage		V_{T1} *1	- 0.3 to V_{CC} + 0.3	V
Input voltage		V_{T2} *3	V_{CC}+0.3 to V_{EE}-0.3	V
Operating temperature		T_{opr}	- 20 to + 75	°C
Storage temperature		T_{stg}	-55 to +125	°C

*1 All voltage values are referred to GND.

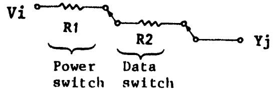
*2 Connect a protection resistor of 220Ω ± 5% to V_{EE} power supply in series.

*3 Applies to V_1 to V_6

■ ELECTRICAL CHARACTERISTICS
(V_{CC} = 5V ± 10%, V_{EE} = -5V ± 10%, GND = 0V, Ta = -20 to + 75°C)

Item	Symbol	Applicable terminal	Test condition	min	typ	max	Unit
Input voltage	V_{IH}	CL1, CL2, DL1, DL2, DR1, DR2, M, SHL1, SHL2, FCS		0.7 V_{CC}	-	V_{CC}	V
	V_{IL}			0	-	0.3 V_{CC}	V
Output voltage	V_{OH}	DL1, DL2, DR1, DR2	I_{OH} = -0.4mA	V_{CC} - 0.4	-	-	V
	V_{OL}		I_{OL} = +0.4mA	-	-	0.4	V
Vi-Yj voltage descending	V_{D1}	*1	I_{ON} = 0.1mA for one of Yj	-	-	1.1	V
	V_{D2}		I_{ON} = 0.05mA for each Yj	-	-	1.5	V
Input leakage current	I_{IL}	CL1, CL2, DL1, DL2, DR1, DR2, M, SHL1, SHL2, FCS, NC	Vin = 0 to V_{CC}	- 5.0	-	5.0	μA
Vi leakage current	I_{VL}	*3	V_{in} = V_{CC} to V_{EE}	-10.0	-	10.0	μA
Power supply current	I_{CC}	*2	f_{CL2} = 400kHz	-	-	1.0	mA
	I_{EE}		f_{CL1} = 1kHz	-	-	10	μA

*1 Vi - Yj (Vi=1 to 6, j=1 to 40) equivalent circuit



R1= 1kΩ max.
R2=10kΩ max.

*2 Input/output current is excluded; when input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low.

*3 Output Y1 to Y40 open.

■ TIMING CHARACTERISTICS

(V_{CC} = 5V ± 10%, V_{EE} = -5 ± 10%, GND = 0V, Ta = -20 to + 75°C)

Item		Symbol	Applicable terminal	Test condition	min	typ	max	Unit
Data shift frequency		f_{CL}	CL2		–	–	400	kHz
Clock width	High level	t_{CWH}	CL1, CL2		800	–	–	ns
	Low level	t_{CWL}	CL2		800	–	–	ns
Data set-up time		t_{SU}	DL1, DL2, DR1, DR2, FLM		300	–	–	ns
Clock set-up time		t_{SL}	CL1, CL2	(CL2→CL1)	500	–	–	ns
Clock set-up time		t_{LS}	CL1, CL2	(CL1→CL2)	500	–	–	ns
Data delay time		tpd	DL1, DL2, DR1, DR2	C_L = 15 pF	–	–	500	ns
Clock rise/fall time		tct	CL1, CL2		–	–	200	ns
Data Hold time		t_{DH}	DL1, DL2, DR1, DR2, FLM		300	–	–	ns

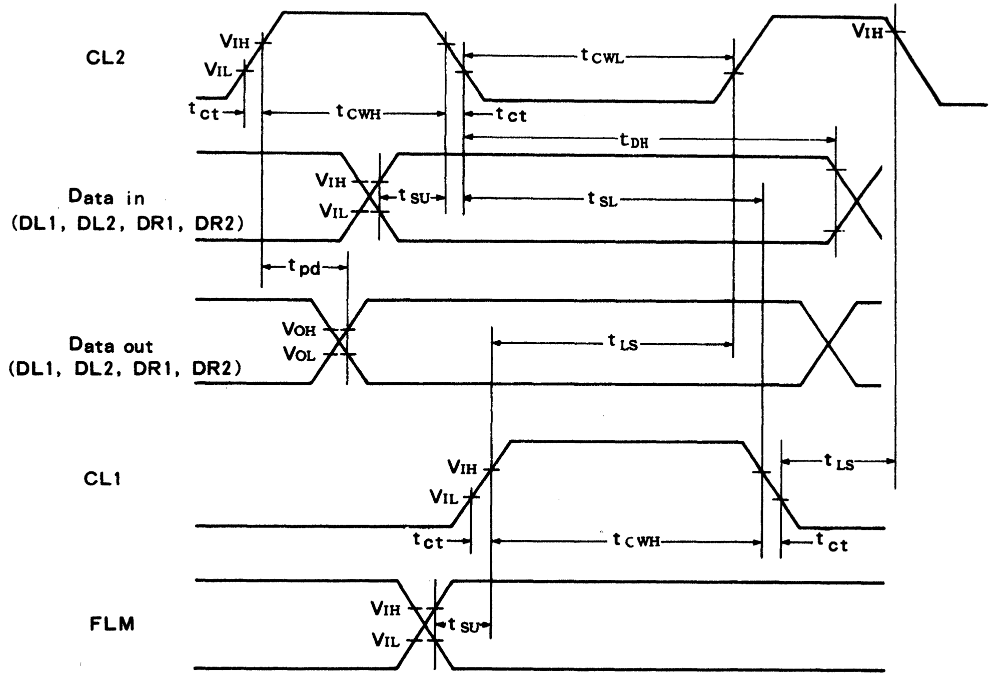


Fig. 1 Timing Waveform

TERMINAL FUNCTION

Table 1 Fucntional Description of Terminals

<table>
<tr><th>Signal name</th><th>Number of lines</th><th>Input/ Output</th><th>Connected to</th><th>Function</th></tr>
<tr><td>V_{CC}</td><td>1</td><td></td><td>Power supply</td><td>Power supply for logical circuit</td></tr>
<tr><td>GND</td><td>1</td><td></td><td>Power supply</td><td>0V</td></tr>
<tr><td>V_{EE}</td><td>1</td><td></td><td>Power supply</td><td>Power supply for liquid crystal display drive</td></tr>
<tr><td>$Y_1 \sim Y_{20}$</td><td>20</td><td>Output</td><td>Liquid crystal</td><td>Liquid crystal driver output (Channel 1)</td></tr>
<tr><td>$Y_{21} \sim Y_{40}$</td><td>20</td><td>Output</td><td>Liquid crystal</td><td>Liquid crystal driver output (Channel 2)</td></tr>
<tr><td>V_1, V_2</td><td>2</td><td>Input</td><td>Power supply</td><td>Power supply for liquid crystal display drive (Select level)</td></tr>
<tr><td>V_3, V_4</td><td>2</td><td>Input</td><td>Power supply</td><td>Power supply for liquid crystal dispaly drive
(Non-select level for channel 1)</td></tr>
<tr><td>V_5, V_6</td><td>2</td><td>Input</td><td>Power supply</td><td>Power supply for liquid crystal display drive
(Non-select level for channel 2)</td></tr>
<tr><td>SHL1</td><td>1</td><td>Input</td><td>V_{CC} or GND</td><td>Selection of the shift direction of channel 1 shift register
<table>
<tr><th>SHL1</th><th>DL1</th><th>DR1</th></tr>
<tr><td>V_{CC}</td><td>OUT</td><td>IN</td></tr>
<tr><td>GND</td><td>IN</td><td>OUT</td></tr>
</table></td></tr>
<tr><td>SHL2</td><td>1</td><td>Input</td><td>V_{CC} or GND</td><td>Selection of the shift direction of channel 2 shift register
<table>
<tr><th>SHL2</th><th>DL2</th><th>DR2</th></tr>
<tr><td>V_{CC}</td><td>OUT</td><td>IN</td></tr>
<tr><td>GND</td><td>IN</td><td>OUT</td></tr>
</table></td></tr>
<tr><td>DL1, DR1</td><td>2</td><td>Input/ output</td><td>Controller or HD44100H</td><td>Data input/output of channel 1 shift register</td></tr>
<tr><td>DL2, DR2</td><td>2</td><td>Input/ output</td><td>Controller or HD44100H</td><td>Data input/output of channel 2 shift register</td></tr>
<tr><td>M</td><td>1</td><td>Input</td><td>Controller</td><td>Alternated signal for liquid crystal driver output</td></tr>
<tr><td>CL1</td><td>1</td><td>Input</td><td>Controller</td><td>Latch signal for channel 1 (‾↓_) *1
This is used for channel 2 when FCS is GND.</td></tr>
<tr><td>CL2</td><td>1</td><td>Input</td><td>Controller</td><td>Shift signal for channel 1 (‾↓_) *1
This is used for channel 2 when FCS is GND.</td></tr>
<tr><td>FCS</td><td>1</td><td>Input</td><td>V_{CC} or GND</td><td>Mode select signal of channel 2. FCS signal exchanges the latch signal and the shift signal of channel 2 and inverts M for channel 2. Thus, this signal exchanges the purpose of channel 2.
<table>
<tr><th rowspan="2">FCS level</th><th colspan="2">Channel 2</th><th rowspan="2">M polarity</th><th rowspan="2">Purpose</th></tr>
<tr><th>Latch signal</th><th>Shift signal</th></tr>
<tr><td>V_{CC}</td><td>CL2 _↑‾</td><td>CL1 _↑‾</td><td>$\overline{M}$</td><td>For common drive</td></tr>
<tr><td>GND</td><td>CL1 ‾↓_</td><td>CL2 ‾↓_</td><td>M</td><td>For segment drive</td></tr>
<tr><td></td><td>*1</td><td>*1</td><td></td><td>*2</td></tr>
</table></td></tr>
<tr><td>NC</td><td>1</td><td></td><td></td><td>Don't connect any wires to this terminal.</td></tr>
</table>

*1 _↑‾ and ‾↓_ indicate the latches at rise and fall times respectively.

*2 The output level relationship between channel 1 and channel 2 based on the FCS signal level is as follows:

FCS	Data	M	Output level	
			Channel 1 ($Y_1 \sim Y_{20}$)	Channel 2 ($Y_{21} \sim Y_{40}$)
V_{CC} ("1")	"1" (Select)	"1"	V_1	V_2
		"0"	V_2	V_1
	"0" (Non-select)	"1"	V_3	V_6
		"0"	V_4	V_5
GND ("0")	"1" (Select)	"1"	V_1	V_1
		"0"	V_2	V_2
	"0" (Non-select)	"1"	V_3	V_5
		"0"	V_4	V_6

"1" and "0" indicate a high and low levels, respectively.

■ APPLICATIONS

• Segment Driver

When the HD44100H is used as a segment driver, the FCS is set to GND to transfer display data in the timing shown in Fig. 2. In this case, both of channel 1 and channel 2 shift data at the fall of CL2 and latch it at the fall of CL1. V_3 and V_5, V_4 and V_6 of power supply for liquid crystal display driver are short-circuited respectively.

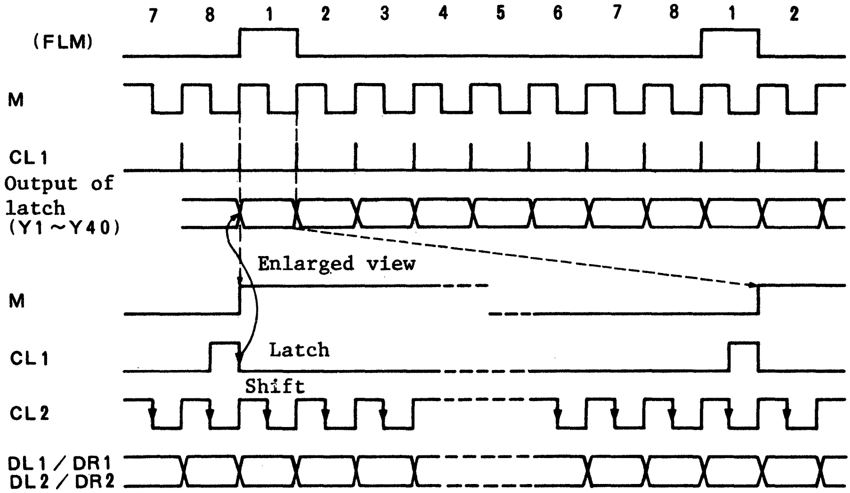


Fig. 2 Segment Data Waveforms (A type waveforms 1/8 duty)

- Common Driver

When channel 1 is used as a segment driver and channel 2 as a common driver.

When channel 2 of HD44100H is used as a common driver, the FCS is set to V_{CC} level to transfer display data in the timing shown in Fig. 3.

In this case, channel 2 shifts data at the rise of CL1 and latches it at the rise of CL2. Channel 1 shifts and latches as shown in Fig. 2.

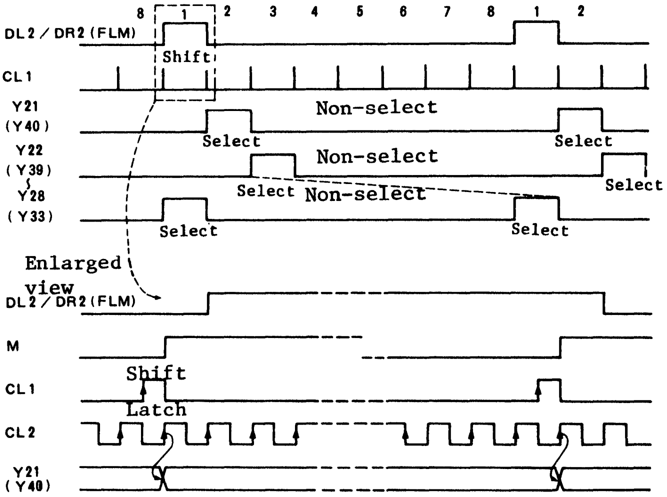


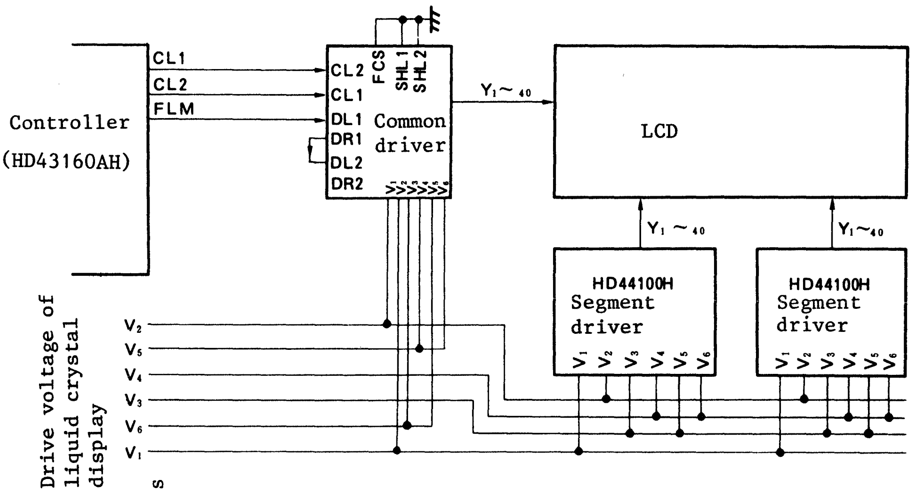
Fig. 3 Common Data Waveforms (A type waveforms of channel 2, 1/8 duty)

• When both Channel 1 and Channel 2 used as Common Drivers (FCS = GND)

When both of channel 1 and channel 2 of HD44100H are used a common driver, the FCS is set to GND and the signals (CL1, CL2, FLM) from the controller are connected as shown in following figure.

In this case, connection of power supply for liquid crystal display driver is different from that of segment driver, so refer to following figure.

V_1, V_2 ..... Select level of segment and common
V_3, V_4 ..... Non-select level of segment
V_5, V_6 ..... Non-select level of common

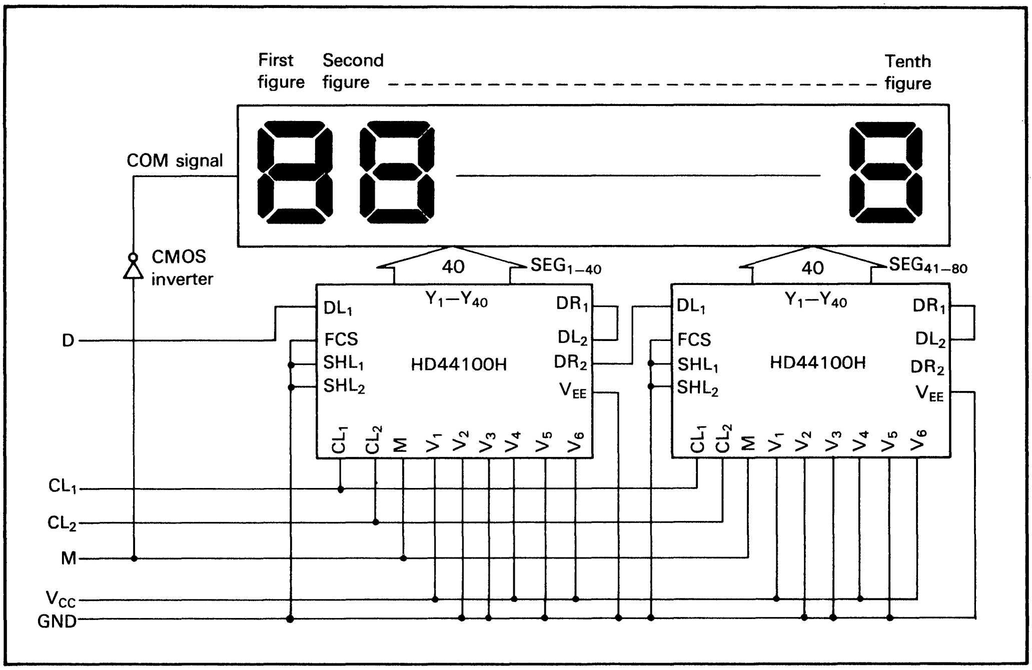


• Static Drive

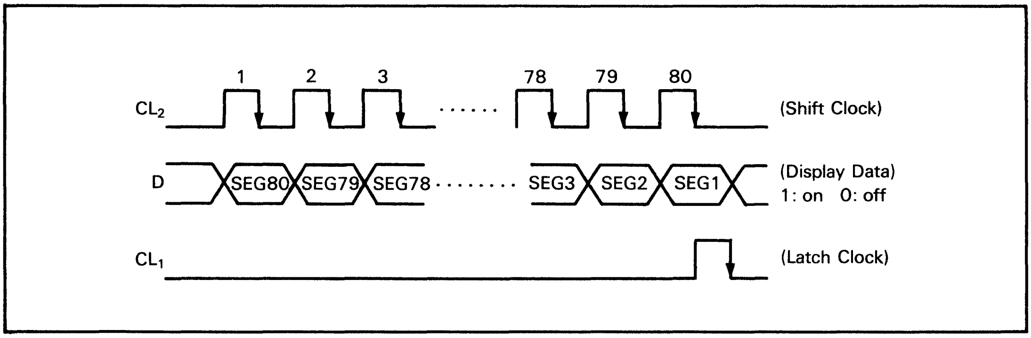
When the HD44100H is used in the static drive, data is transferred at the fall of CL2 and latched at the fall of CL1. The frequency of CL1 becomes the frame frequency of liquid crystal display driver. The signal applied into terminal M must be one that has the frequency twice that of CL1 and is synchronized at the fall of CL1. The power supply for liquid crystal display driver is used by short-circuiting three of V_1, V_4 and V_6, and three of V_2, V_3 and V_5 respectively.

One of liquid crystal display driver output terminals can be used for a common output. In this case, the FCS is set to GND and data is transferred so that "0" can be always latched in the latch corresponding to the liquid crystal display driver output terminal used as the common output. If the latch signal corresponding to the segment output is "1", the segments of LCD light. They also light with common side = "1", and segment side "0".

Static Drive

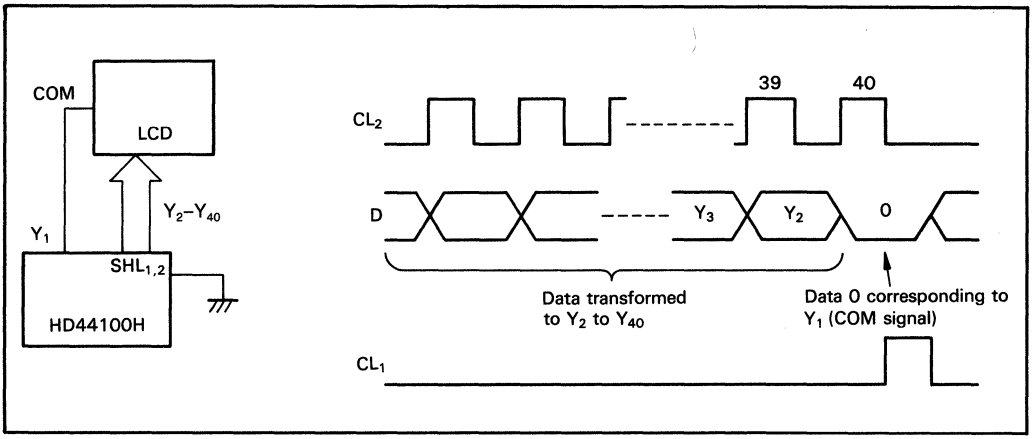


Timing Chart of Input Waveforms



Notes:

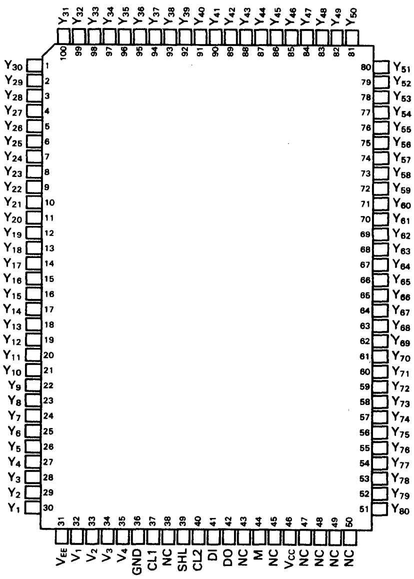
1. Input square waves of 50% duty (about 30-500 Hz) to M. The frequency depends on the specifications of LCD panels.
2. The drive waveforms corresponding to the new displayed data output at the fall of CL1. Therefore, when the alternating signal M and CL1 donot fall synchronously, DC elements are produced on the LCD drive waveforms. These DC elements may shorten the life span of the LCD, if the displayed data frequently changes (e.g.display of hours, minutes, and seconds of a clock). To avoid it, set CL1 falling synchronously with the one edge of M.
3. In this example, the CMOS inverter is used as a COM signal driver in consideration of a large display area. (The load capacitance on COM is large because it is common to all the displayed segments.)
   Usually, one of the HD44100H outputs can be used as a COM signal. The displayed data corresponding to the terminal should be 0 in that case.


COM
LCD
Y1
Y2–Y40
SHL1,2
HD44100H
39
40
CL2
D
Y3
Y2
0
Data transformed to Y2 to Y40
Data 0 corresponding to Y1 (COM signal)
CL1

HD66100
(LCD Driver with 80-Channel Outputs)

Description

The HD66100 is a segment driver with 80 LCD drive circuits and is the improved version of the current LCD driver HD44100H with 40 circuits.
It is composed of a shift register, a 80-bit latch circuit, and 80 LCD drive circuits. Its interface is compatible with the HD44100H.
It enables lessening the number of LSI's and lowering cost of a LCD module.



(FP-100)

(Top View)

Features

- LCD driver with serial/parallel converting function
- Interface compatible with the HD44100H; connectable with HD43160AH, HD61830, HD61830B, LCD-II (HD44780), LCD-III (HD44790)
- Internal output circuits for LCD drive-80
- Internal serial/parallel converting circuits;
  - 80-bit bidirectional shift register
  - 80-bit latch circuit
- Power supply
  Internal logic circuit; +5 V ±10%
  LCD drive circuit; 3.0 V to 6.0 V
- CMOS process
- 100-pin plastic QFP (FP-100)

Comparison with HD44100H

Table 1 shows the main differences between HD66100 and HD44100H.

Table 1. Comparison of HD66100 and HD44100H

	HD66100	HD44100H
LCD Drive Outputs	80×1 Channel	20×2 channels
Supply Voltage for LCD Drive Circuits	3 to 6V	4.5 to 11V
Multiplexing Duty Ratio	Static to 1/16 duty	static to 1/32 duty
Package	100-pin flat Plastic package	60-pin flat plastic package

Pin Description

V_{CC}, GND, V_{EE}: V_{CC} supplies power to the internal logic circuit. GND is the logic and drive ground. V_{EE} supplies power to the LCD drive circuit.

V_1, V_2, V_3, and V_4: V_1 to V_4 supply power for driving an LCD (figure 2).

CL1: Latches data at the negative adge of CL1.

CL2: Receives shift data at the negative edge of CL2.

M: Changes LCD drive outputs to AC.

DI: Receives data of the shift register.

DO: Output data of the shift register.

SHL: Selects a shift direction of serial data. When the serial data is input in order of D_1, D_2 ......D_{79}, D_{80}, the relation between the data and the output Y is as table 3.

Y_1-Y_{80}: Each Y outputs one of the four voltage levels-V_1, V_2, V_3, or V_4-according to the combination of M and display data (figure 2).

NC: Do not connect any wire with these terminals.

Table 2. Pin Function

Symbol	Pin No.	Pin Name	I/O
V_{CC}	46	V_{CC}	–
GND	36	Ground	–
V_{EE}	31	V_{EE}	–
V_1	32	V_1	–
V_2	33	V_2	–
V_3	34	V_3	–
V_4	35	V_4	–
CL1	37	Clock 1	I
CL2	40	Clock 2	I
M	44	M	I
DI	41	Date In	I
DO	42	Date Out	O
SHL	39	Shift Left	I
Y_1-Y_{80}	1-30,51-100	Y_1-Y_{80}	O
NC	38,43,45,47-50	Non Connection	–

Table 3. Relation Between SHL and Data Output

SHL	Y_1	Y_2	Y_3....Y_{79}		Y_{80}
High	D1	D2	D3......	D79	D80
Low	D80	D79	D78.....	D2	D1

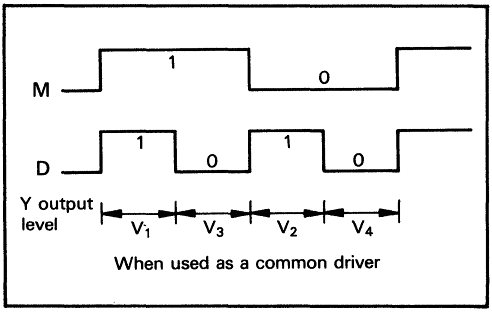


Figure 1. Selection of LCD Drive Output

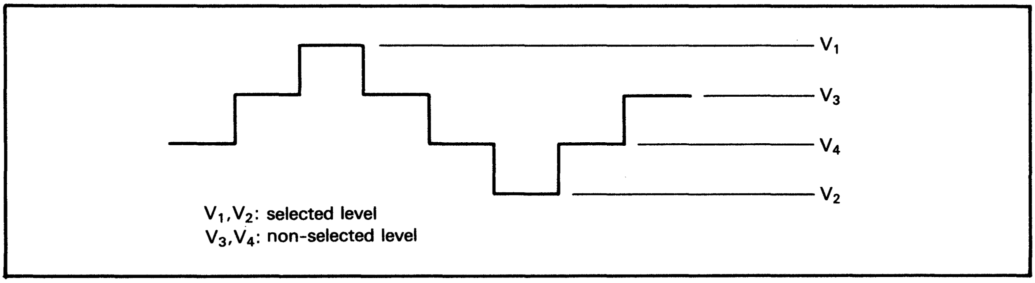


Figure 2. Power Supply for Driving an LCD

Block Functions

LCD Drive Circuits

These circuits select one of four levels of voltage V_1, V_2, V_3, and V_4 for driving a LCD and transfer it to the output terminals according to the combination of M and the data in the latch circuit.

Latch Circuit

This circuit latches the data input from the bidirectional shift register at the fall of CL1 and transfer its outputs to the LCD drive circuits.

Bidirectional Shift Reigster

This register shifts the serial data at the fall of CL2 and transfer the output of each bit of the register to the latch circuit. When SHL = GND, the data input from DI shifts from the bit 1 to the bit 80 in order of entry. On the contrary, when SHL = V_{CC}, the data shifts from the bit 80 to the bit 1. In both cases, the data of the last bit of the register is latched to be output from DO at the rise of CL2.

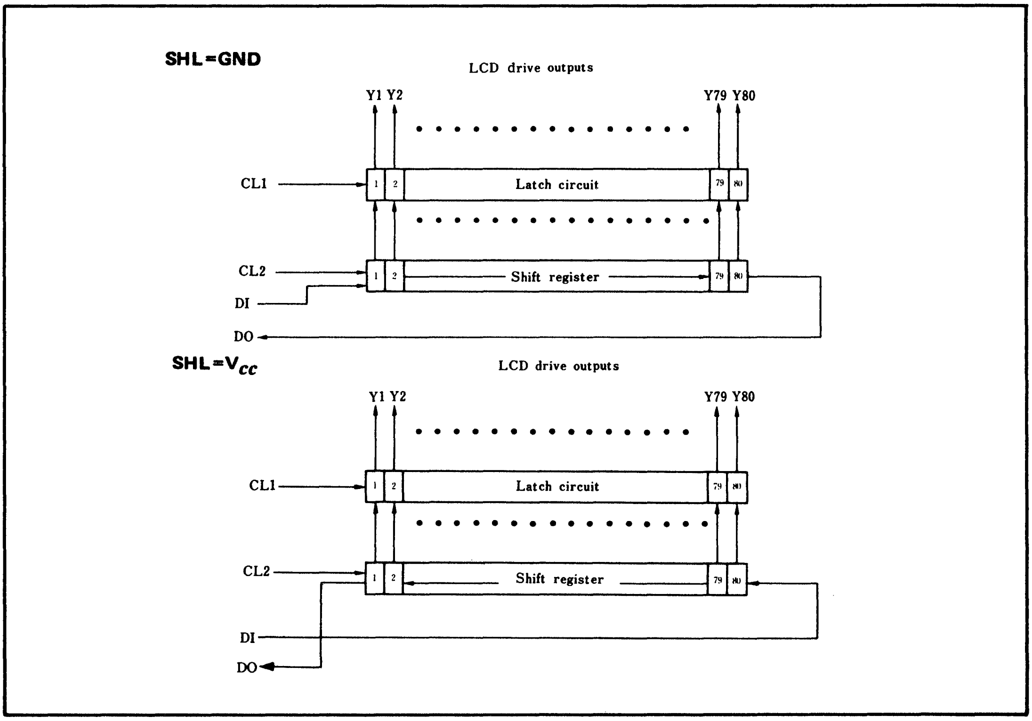


Figure 3. Relation between SHL and the Shift Direction

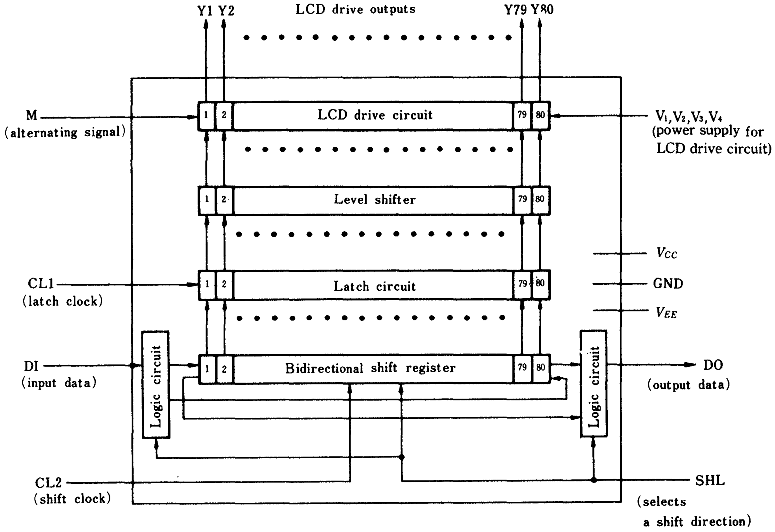


Figure 4. Block Diagram

Primary Operations

Shifting Data

The input data DI shifts at the fall of CL2 and the data delayed 80 bits by the shift register outputs from the DO terminal. The output of DO changes synchronously with the rise of CL2. This operation is completely unaffected by the latch clock CL1.

Latching Data

The data of the shift register is latched at the negative edge of the latch clock CL1. Thus, the outputs Y_1-Y_{80} change synchronously with the fall of CL1.

Switching Data Shift Direction

When the shift direction switching signal SHL is connected with GND, the data D80, immediately before the negative edge of CL1, outputs from the output terminal Y_1 and when SHL is connected with V_{CC}, it outputs from Y_{80}.

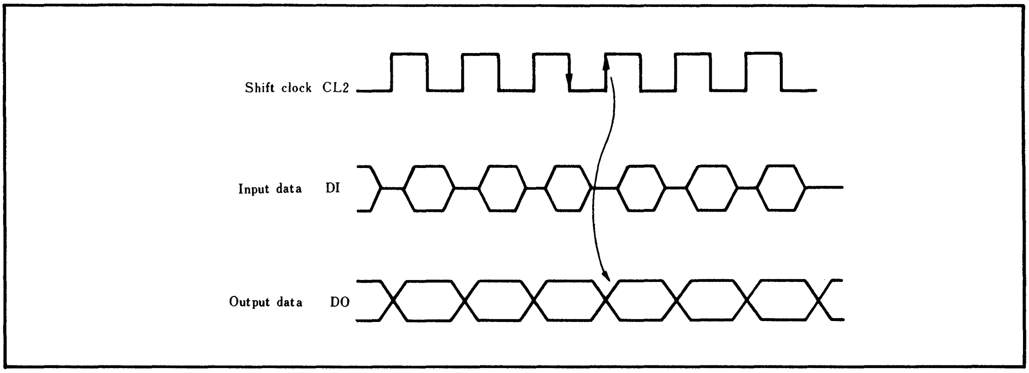


Figure 5. Timing of Receiving and Outputting Data

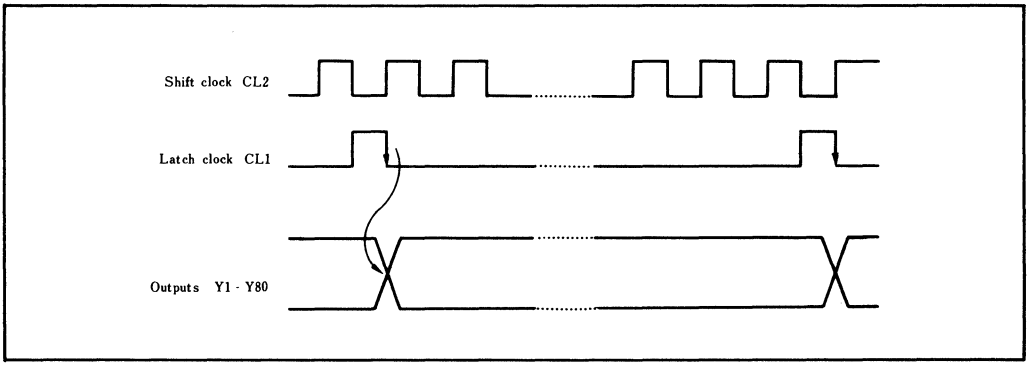


Figure 6. Timing of Latching Data

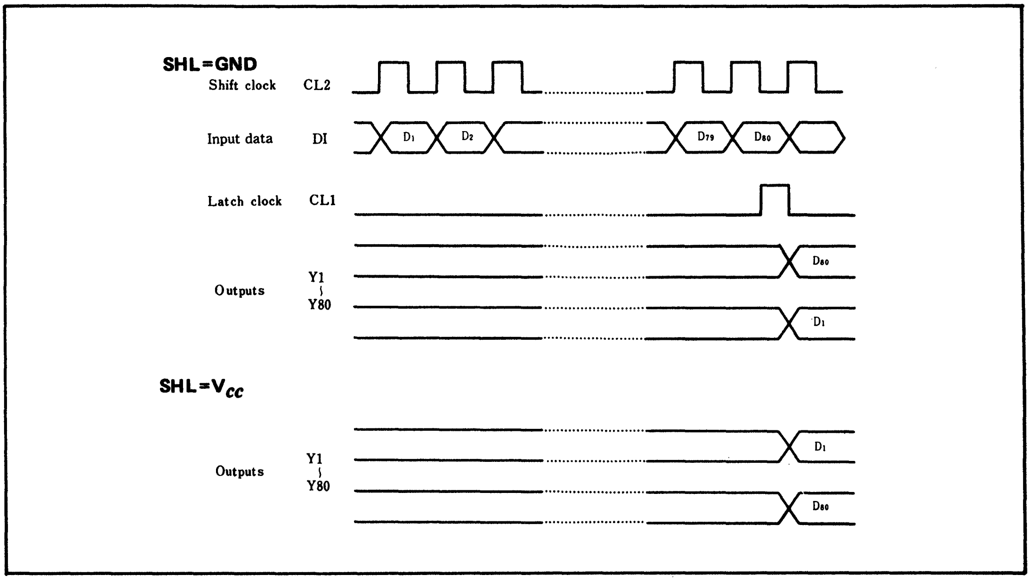


Figure 7. SHL and Waveforms of Data Shift

Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Note
Supply Voltage	Logic Circuits	V_{CC}	−0.3 to +7.0	V	*1
	LCD Drive Circuits	V_{CC}-V_{EE}	−0.3 to +7.0	V	
Input Voltage (1)		V_{T1}	−0.3 to V_{CC}+0.3	V	*1
Input Voltage (2)		V_{T2}	V_{CC}+0.3 to V_{EE}−0.3	V	*2
Operation Temperature		T_{opr}	+20 to +75	°C	
Storage Temperature		T_{stg}	−55 to +125	°C	

*1 A reference point is GND (=0V.)

*2 Applies to $V_1 - V_4$.

Note) If used beyond the absolute maximum ratings, LSI's may be permanently destroyed. It is desired to use ones on the electrical characteristics for normal operations, and if not used on these conditions, it may affect the reliability of the device.

Electrical Characteristics

1. DC Characteristics
(V_{CC}=5V±10%, V_{CC}-V_{EE}=3.0 to 6.0V, GND=0V, T_a=−20 to +75°C)

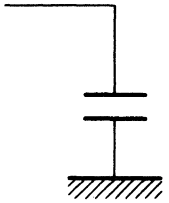
Item	Symbol	Terminals	Min.	Typ.	Max.	Unit	Test condition	Note
Input High Voltage	V_{IH}	CL1,CL2	0.8×V_{CC}	–	V_{CC}	V		
Input Low Voltage	V_{IL}	M,DI,SHL	0	–	0.2×V_{CC}	V		
Output High Voltage	V_{OH}	DO	V_{CC}-0.4	–	–	V	I_{OH}=-0.4mA	
Output Low Voltage	V_{OL}		–	–	0.4	V	I_{OL}=+0.4mA	
ON Resistance Vi-Vj	R_{ON1}	Y_1-Y_{80}	–	–	11	kΩ	I_{ON}=0.1mA to one of Y terminals	
	R_{ON2}	V_1-V_4	–	–	30	kΩ	I_{ON}=0.05mA to each Y terminal	
Input Leakage Current	I_{IL}	CL1, CL2, M, DI, SHL	−5.0	–	5.0	μA	V_{in}=0V to V_{CC}	
Vi Leakage Current	I_{VL}	V_1-V_4	−5.0	–	5.0	μA	Output Y_1-Y_{80} open V_{in}=V_{CC} to V_{EE}	
Current Dissipation	I_{GND}		–	–	2.0	mA	f_{CL2}=1.0MHz	*1
	I_{EE}		–	–	0.1	mA	f_{CL1}=2.5kHz	

*1 Input/output currents are excluded; when an input is at the intermediate level in CMOS, the excessive current flows from the power supply through the input circuit.
To avoid it, V_{IH} and V_{IL} must be fixed at V_{CC} and GND level respectively.

2. AC Characteristics
(V_{CC}=5V±10%, V_{CC}-V_{EE}=3.0 to 6.0V, GND=0V, T_a=−20 to +75°C)

Item	Symbol	Terminals	Min.	Typ.	Max.	Unit	Note
Data Shift Frequency	f_{CL}	CL2	–	–	1	MHz	
Clock High level Width	t_{CWH}	CL1,CL2	450	–	–	ns	
Clock Low level Width	t_{CWL}	CL2	450	–	–	ns	
Data Set-up Time	f_{SU}	DI	100	–	–	ns	
Clock Set-up Time (1)	t_{SL}	CL2	200	–	–	ns	*1
Clock Set-up Time (2)	t_{LS}	CL1	200	–	–	ns	*2
Output Delay Time	t_{pd}	DO	–	–	250	ns	*3
Data Hold Time	t_{DH}	DI	100	–	–	ns	
Clock Rise/Fall Time	f_{CT}	CL1,CL2	–	–	50	ns	

*1 Set-up time from the fall of CL2 to that of CL1.
*2 Set-up time from the fall CL1 to that of CL2.
*3 Test terminal



C_L (Load capacitance on outputs)=30pF
(Including jig capacitance)

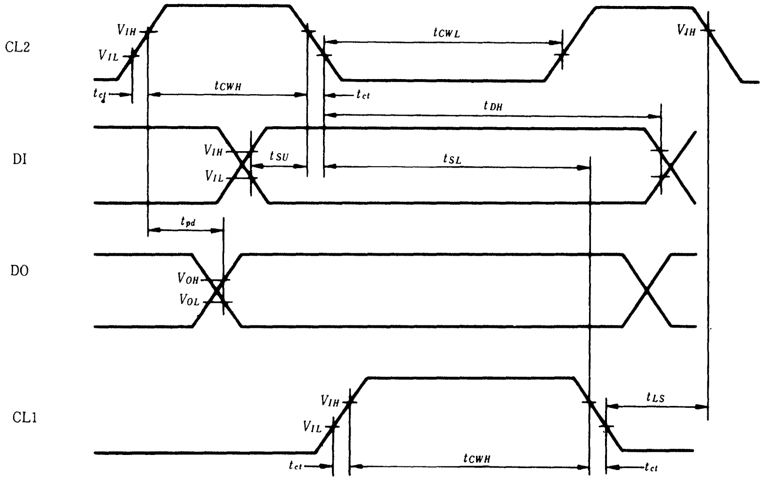


Figure 8. Timing Chart of HD66100F

Typical Applications

1. Connection with the LCD Controller HD44780

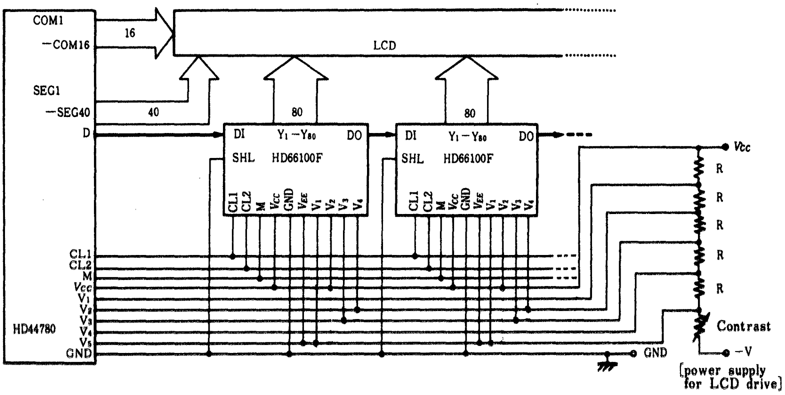


Figure 9. Example of Connection (1/16 duty, 1/5bias)

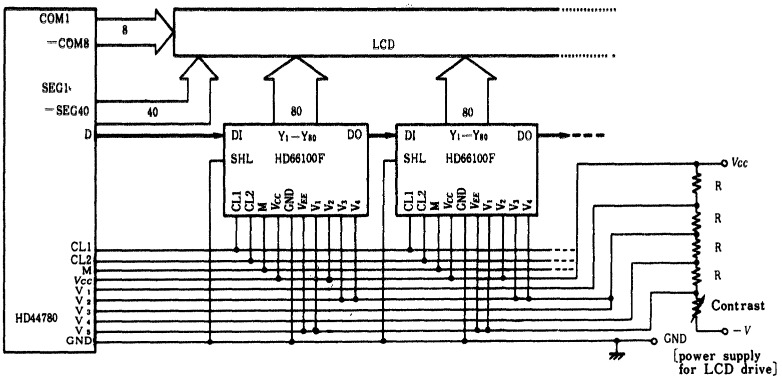


Figure 10. Example of Connection (1/8 duty, 1/4bias)

2. Connection with LCD III (HD44790)

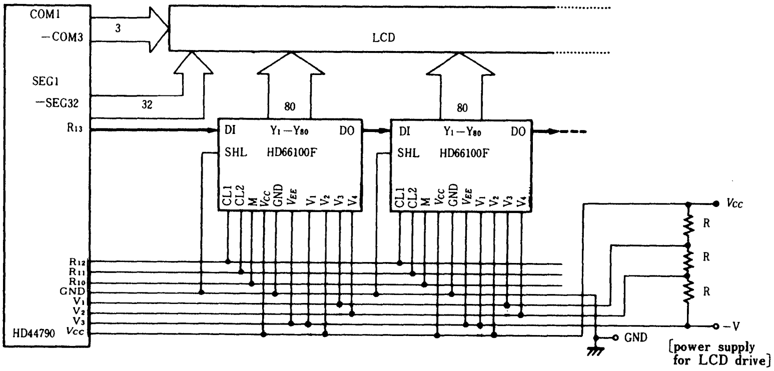


Figure 11. Example of Connection (1/3 duty, 1/3bias)

3. Static Drive

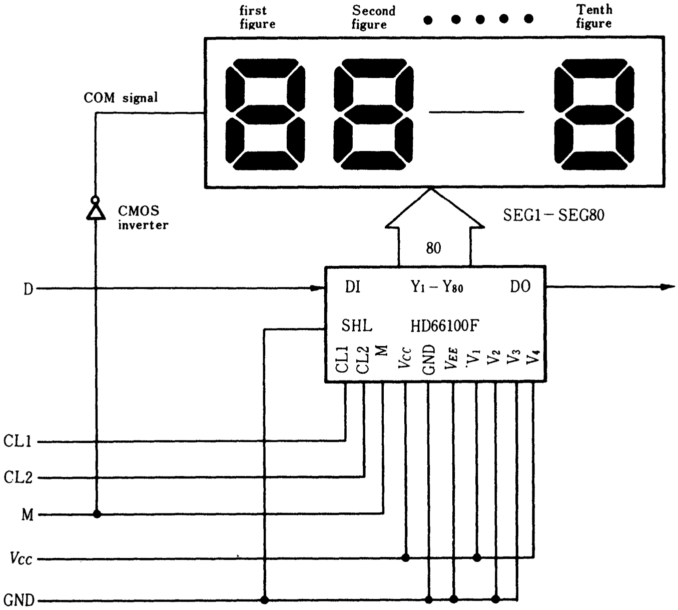


Figure 12. Example of Connection (80-segment display)

- **Timing Chart of Input Waveforms**

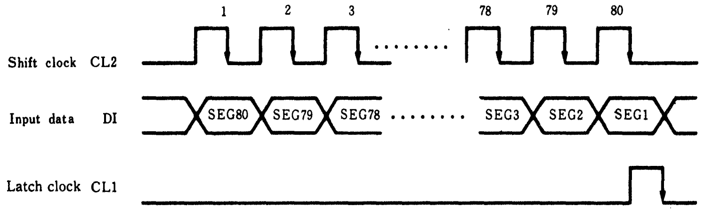


Figure 13. Timing Chart of Input Waveforms

Notes

(a) Input square waves of 50% duty (about 30-500Hz) to M. The frequency depends on the specifications of LCD panels.

(b) The drive waveforms corresponding to the new displayed data output at the fall of CL1. Therefore, when the alternating signal M and CL1 do not fall synchronously, DC elements are produced on the LCD drive waveforms. These DC elements may shorten the life span of the LCD, if the displayed data frequently changes (e.g. display of hours, minutes, and seconds of a clock). To avoid it, set CL1 falling synchronously with the one edge of M.

(C) In this example, the CMOS inverter is used as a COM signal driver in consideration of a large display area. (The load capacitance on COM is large because it is common to all the displayed segments.)
Usually, one of the HD66100F outputs can be used as a COM signal. The displayed data corresponding to the terminal should be 0 in that case.

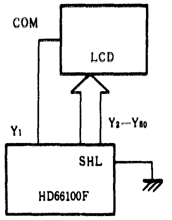


Figure 14. Example of Connection

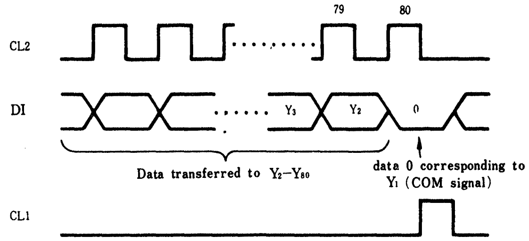

79
80
CL2
DI
Y_3
Y_2
0
Data transferred to Y_2—Y_{80}
data 0 corresponding to Y_1 (COM signal)
CL1

Figure 15. Timing Chart (When Y_1 is used as a COM signal)

HD43160AH
(Controller with Built-in Character Generator)

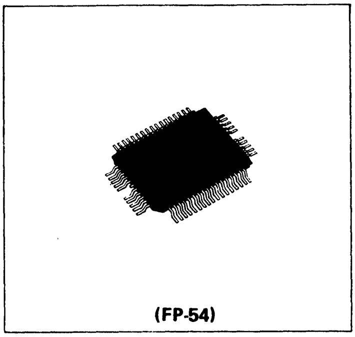
DISPLAY CONTROLLER AND CHARACTER GENERATOR
FOR DOT MATRIX LIQUID CRYSTAL DISPLAY SYSTEM

DESCRIPTION

The HD43160AH receives character data written in the ASCII code or JIS code from microcomputer and stores them in its RAM which has 80 words capacity.

The HD43160AH converts these data into serial character pattern, then transfers them to LCD drivers.

It also generates other control signals for LCD. Available LCD driver for combination with this is HD44100H.



(FP-54)

■ SORTS OF DISPLAY CHARACTERS

- Alphanumeric character; A ~ Z, a ~ z, @, #, %, &, etc.
- Japanese Character (katakana)
- 160 characters by internal character generator (ROM).
  (Max 256 characters by external ROM)

■ NUMBER OF CHARACTERS

- 4, 8, 16, 24, 32, 40, 64 or 80 characters in 1 or 2 lines

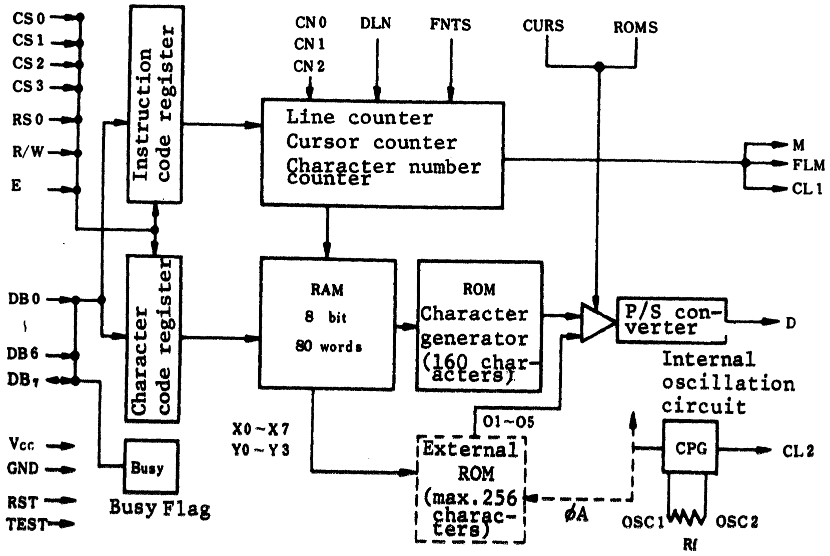
■ FONT

- 5 × 7 + Cursor or 5 × 11 + Cursor

■ OTHER FUNCTION CONTROLLED BY MICROCOMPUTER

- Display clear
- Cursor ON/OFF
- Cursor position preset (Character position)
- Cursor return

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_T	-0.3 to V_{CC} +0.3	V
Operating temperature	T_{opr}	-20 to +75	°C
Storage temperature	T_{stg}	-55 to +125	°C

■ ELECTRICAL CHARACTERISTICS (V_{CC}=5V±5%, GND=0V, Ta=-20 to +75°C)

Item	Symbol	Terminal No.	Test condition	min	typ	max	Unit
Input voltage	V_{IH}	CS0 ~ CS3, E, R/W,		2.0	-	V_{CC}	V
(TTL compatible)	V_{IL}	DB0 ~ DB7, **RS0**		0	-	0.8	V
Input voltage	V_{IHC}	OSC1,TEST,RST,FNTS, CURS,DLN,ROMS, CN0 ~ CN2, O_1 ~ O_5		0.7 V_{CC}	-	**Vcc**	V
	V_{ILC}			0	-	0.3 V_{CC}	V
Output voltage (TTL compatible)	V_{OH}	DB7	I_{OH}=-0.205mA	2.4	-	-	V
	V_{OL}		I_{OL}=1.6mA	-	-	0.4	V
Output voltage	V_{OHC}	FLM,M,D,CL1,CL2,	I_{load}=±0.4mA	VCC-1.0	-	-	V
	V_{OLC}	X0 ~ X7, Y0 ~ Y3		-	-	1.0	V
Input leak current	I_{in}	All inputs		-5	-	5	μA
Output leak current	I_{LO}	DB7		-10	-	10	μA
Oscillation frequency	f_{CP1}		R_f=200kΩ±2%, 5×7+Cursor	130	192	250	kHz
	f_{CP2}		R_f=130kΩ±2%, 5×11+Cursor	200	288	375	kHz
Input pull up current	I_{PL}	CS0 ~ CS3, RS0, R/W, DB0 ~ DB7	V_{in}=0V	2	10	20	μA
Power dissipation	P_T	*	Ta=25c, f_{CP}=400kHz (external clock)	-	-	10	mW

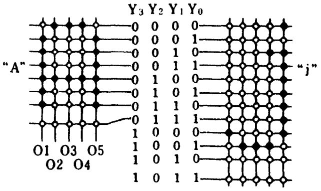
* Input/output current is excluded. When input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low, but CS0 ~ CS3, RS0, R/W, DB0 ~ DB7 are **excluded.**

■ PIN ARRANGEMENT

Pin No.	Power sup. OSC.	Input	Output	Pin No.	Power sup. OSC.	Input	Output	Pin No.	Power sup. OSC.	Input	Output
1	GND (-)			19			D	37		DB3	
2			X4	20			FLM	38		DB4	
3			X3	21			φA	39		DB5	
4			X2	22	OSC1			40		DB6	
5			X1	23	OSC2			41		DB7	DB7
6			X0	24		RST		42		ROMS	
7		N.C.		25		TEST		43		O5	
8		N.C.		26		E		44		O4	
9		N.C.		27	V_{CC}(+)			45		O3	
10		CURS		28		R/W		46		O2	
11		FNTS		29		RS0		47		O1	
12		DLN		30		CS0		48			Y3
13		CN0		31		CS1		49			Y2
14		CN1		32		CS2		50			Y1
15		CN2		33		CS3		51			Y0
16			CL2	34		DB0		52			X7
17			CL1	35		DB1		53			X6
18			M	36		DB2		54			X5

■ PIN FUNCTION

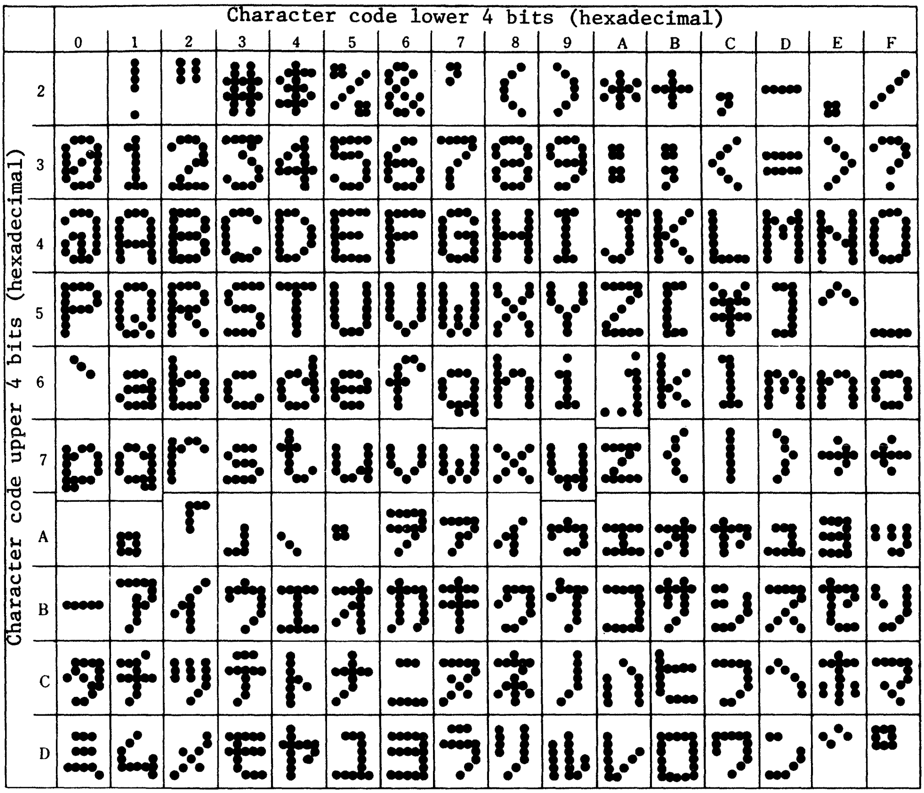
<table>
<tr><th>Pin name</th><th>Number of terminals</th><th>Connected to</th><th>I/O</th><th>Function</th></tr>
<tr><td>V_{CC}
GND</td><td>2</td><td>Power supply</td><td></td><td>+5V ± 10% Power supply
0V</td></tr>
<tr><td>CN0
CN1
CN2</td><td>3</td><td>GND or V_{CC}</td><td>I</td><td>Total displayed character number select.
<table>
<tr><td>No.</td><td>4</td><td>8</td><td>16</td><td>24</td><td>32</td><td>40</td><td>64</td><td>80</td></tr>
<tr><td>CN0</td><td>GND</td><td>V_{CC}</td><td>GND</td><td>V_{CC}</td><td>GND</td><td>V_{CC}</td><td>GND</td><td>V_{CC}</td></tr>
<tr><td>CN1</td><td>GND</td><td>GND</td><td>V_{CC}</td><td>V_{CC}</td><td>GND</td><td>GND</td><td>V_{CC}</td><td>V_{CC}</td></tr>
<tr><td>CN2</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>V_{CC}</td><td>V_{CC}</td><td>V_{CC}</td><td>V_{CC}</td></tr>
</table></td></tr>
<tr><td>CURS</td><td>1</td><td>GND or V_{CC}</td><td>I</td><td>Cursor select
V_{CC}: 5 dots. ●●●●●
GND: 1 dot. ●</td></tr>
<tr><td>DLN</td><td>1</td><td>GND or V_{CC}</td><td>I</td><td>Display line number select.
V_{CC}: 2 lines.
GND: 1 line.</td></tr>
<tr><td>FNTS</td><td>1</td><td>GND or V_{CC}</td><td>I</td><td>Font select.
V_{CC}: 5 × 11 + Cursor.
GND: 5 × 7 + Cursor.</td></tr>
<tr><td>RST</td><td>1</td><td>V_{CC}</td><td>I</td><td>Only for test. Normally V_{CC}</td></tr>
<tr><td>TEST</td><td>1</td><td>GND</td><td>I</td><td>Only for test. Normally GND</td></tr>
<tr><td>E</td><td>1</td><td>MPU</td><td>I</td><td>Strobe signal.
Write mode: The HD43160AH latches the data on DB0 ~ DB7 at the falling edge of this signal.
Read mode: Busy/Ready signal is active on DB7 while this signal is 'H'. (L:Ready, H:Busy)</td></tr>
<tr><td>R/W</td><td>1</td><td>MPU</td><td>I</td><td>Read/Write signal
L: HD43160AH gets the data from MPU.
H: MPU gets the Busy/Ready signal from HD43160AH.</td></tr>
<tr><td>CS0
CS1
CS2
CS3</td><td>4</td><td>MPU</td><td>I</td><td>Chip select
When all of CS0 ~ CS3 are 'H', HD43160AH is selected.</td></tr>
<tr><td>RS0</td><td>1</td><td>MPU</td><td>I</td><td>Register select.
HD43160AH has 2 registers. One is for Character code and another is for instruction code. Each register latches the data on DB0 ~ DB7 at the falling edge of 'E', when CS0 ~ CS3 are 'H' and R/W is 'L'.
H; Character code register is selected.
L; Instruction code register is selected.</td></tr>
<tr><td>DB0
~
DB7</td><td>8</td><td>MPU</td><td>I
I/O
(DB7)</td><td>Data bus.
Inputs for Character code and Instruction code from MPU.
Output for Busy/Ready flag (DB7).</td></tr>
<tr><td>D</td><td>1</td><td>HD44100H</td><td>O</td><td>Serial dot data of characters for LCD drivers</td></tr>
<tr><td>CL2</td><td>1</td><td>HD44100H</td><td>O</td><td>Dot data shift signal for LCD drivers.</td></tr>
<tr><td>CL1</td><td>1</td><td>HD44100H</td><td>O</td><td>Dot data latch signal for LCD drivers.</td></tr>
</table>

M	1	HD44100H	O	Alternate signal for LCD drivers.
FLM	1	HD44100H	O	Signal for common plates scanning.
X0 ≀ X7	8	ROM	O	Character code outputs for External character generator. (for Ext ROM) X7: MSB X0: LSB ex: character 'A' MSB LSB '1'='H' 0 1 0 0 0 0 0 1 '0'='L'
Y0 Y1 Y2 Y3	4	ROM	O	Character row code for External character generator. 5 ×7 + Cursor 5 ×11 + Cursor  Y_3 Y_2 Y_1 Y_0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 0 1 0 1 0 1 1 0 0 1 1 1 1 0 0 0 1 0 0 1 1 0 1 0 1 0 1 1 "A" "j" O1 O3 O5 O2 O4
φA	1	ROM	O	Clock signal for External character generator (dynamic ROM etc.) if necessary.
O1 ≀ O5	5	ROM	I	Dot data inputs from External character generator. 1(H): ON 0(L): OFF
ROMS	1	GND or V_{CC}	I	Select Internal or External ROM. H: External ROM L: Internal ROM
OSC1 OSC2	2		(I) (O)	Oscillator. 5 ×7 + Cursor : R_f=200kΩ (typ) 5 ×11 + Cursor: R_f=130kΩ (typ)
NC	3			Don't connect any wire to these terminals.

CHARACTER DOT PATTERNS

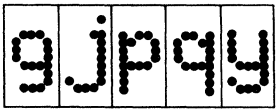
- 5 × 7

The bottom lines of the English small characters "g, i, p, q, y," are on the cursor line.


Character code lower 4 bits (hexadecimal)
0
1
2
3
4
5
6
7
8
9
A
B
C
D
E
F
Character code upper 4 bits (hexadecimal)
2
3
4
5
6
7
A
B
C
D

- 5 × 11

Only English small character "g, j, p, q, y," are displayed as below, the others are in the same way as that of 5 × 7.



- Cursor 5 dots: ●●●●●
  1 dot : ●

The cursor is displayed on the 8th or 12th line.

■ APPLICATION

• Setting Up

a) Total character number ..... (CN0 ~ CN2)

b) Cursor pattern .... (CURS)

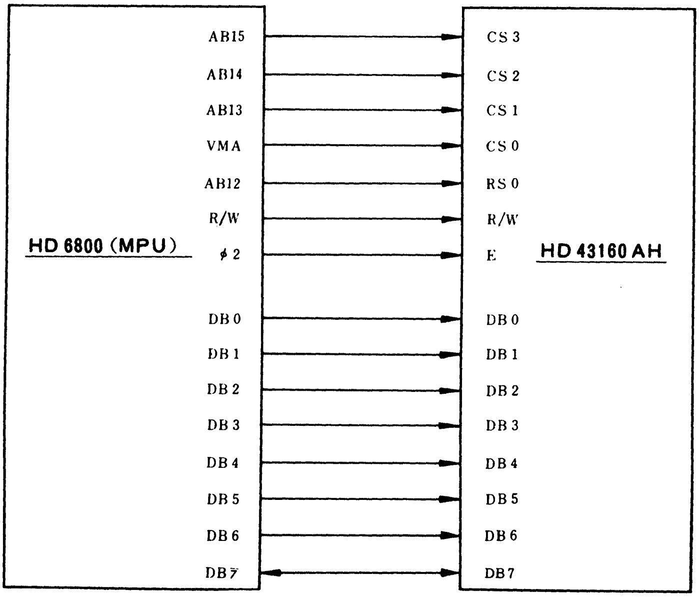
c) Display line number .... (DLN)

d) Font .... (FNTS)

These terminals should be connected to V_{CC} or GND according to the LCD display system. RST and TEST should be connected to V_{CC} and GND respectively.

• Interface to the Controller

a) Example 1 Interface to HD6800

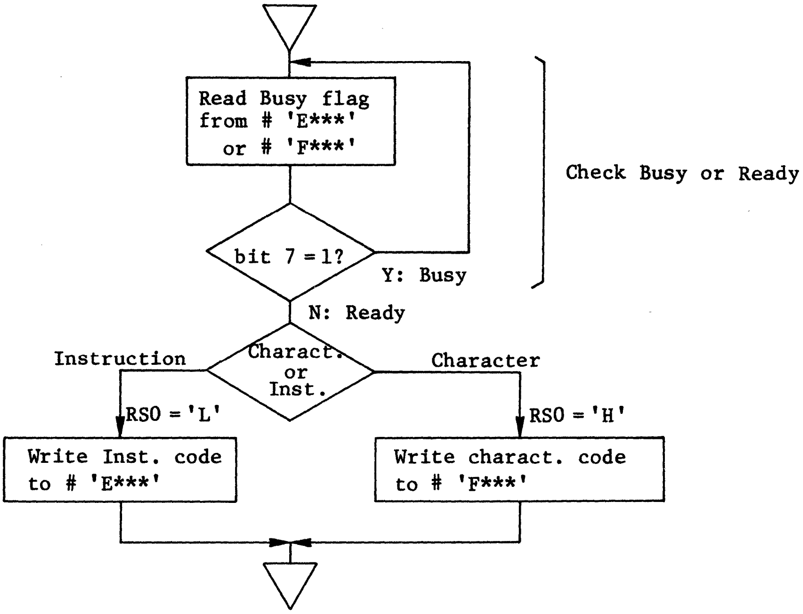


In this example, the addresses of HD43160AH in the address area of the HD6800 microcomputer are

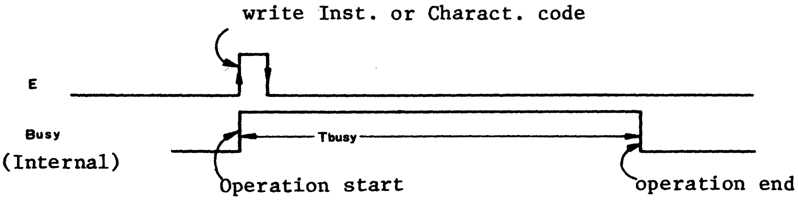
Instruction code register	#'E***'	(R/W=0)
Character code register	#'F***'	(R/W=0)
Busy flag	#'E***' or #'F***'	(R/W=1).

*: don't care
#'': hexadecimal

b) Example of display program



c) Time length of Busy



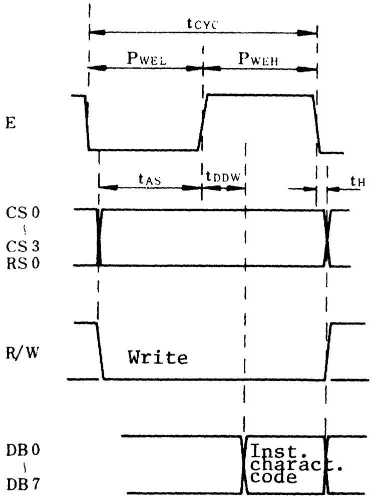
	T busy		
	MIN	MAX	Unit
Display clear	$\frac{400}{f_{cp}}$	$\frac{410}{f_{cp}}$	sec
Other function	$\frac{10}{f_{cp}}$	$\frac{20}{f_{cp}}$	sec

HD43160AH begins the operation from the rising edge of 'E'. Instruction code register and Character code register latch the data on DB0 ~ DB7 at the falling edge of 'E'.

d) Timing chart

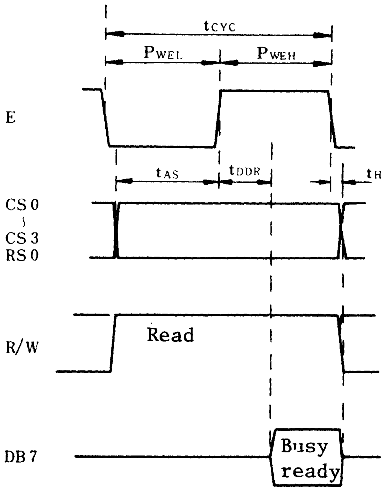
Write sequence

(MPU→HD43160AH)



Read sequence

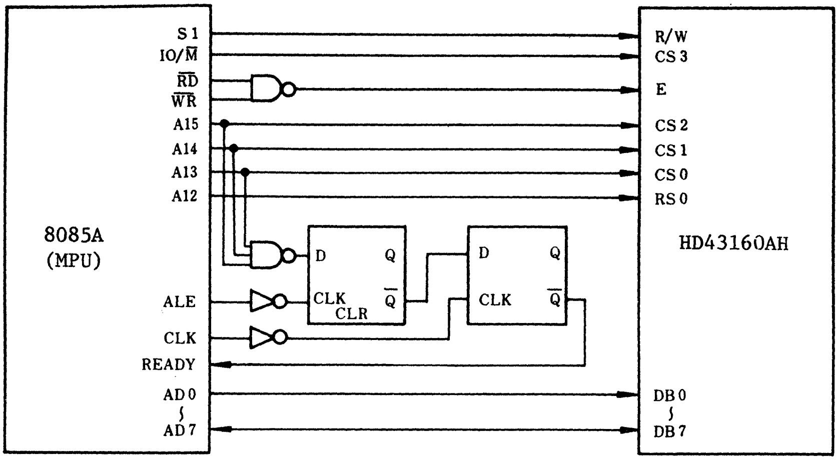
(MPU←HD43160AH)



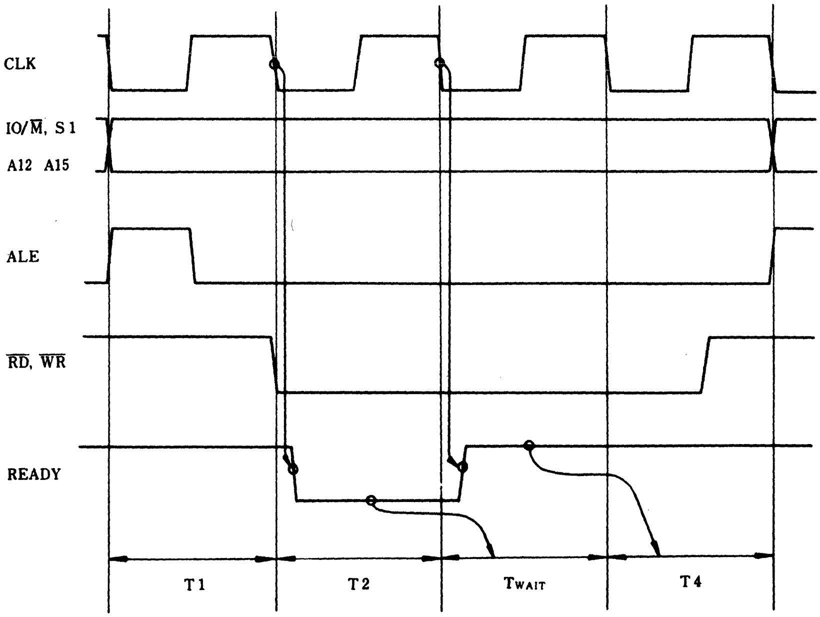
e) Timing characteristics

		Symbol	min	typ	max	Unit
Cycle time of 'E'		t_{cyc}	1.0	-	-	µs
Pulse width of 'E'	H level	P_{WEH}	0.45	-	25	µs
	L level	P_{WEL}	0.45	-	-	µs
Set up time of CS	Write	t_{AS}	140	-	-	ns
Deta delay time	Write	t_{DDW}	-	-	225	ns
	Read	t_{DDR}	-	-	300	ns
Hold time		t_H	10	-	-	ns

f) Example 2 Interface to 8085A (Intel)



g) Timing chart



Pulse widths of $\overline{RD}$ and $\overline{WR}$ signals of the 8085A are 400ns MIN, while the pulse width of E signal of the HD43160AH is 450 ns min. Therefore, in this example, $\overline{RD}$ and $\overline{WR}$ signal pulse widths are widened by using T_{WAIT} cycle.

■ DISPLAY COMMANDS

• Display Controll Instructions

These instructions should be written into the instruction register of HD43160AH by the microcomputer. (RS0='L', R/W='L')

a) Display clear

Code:

MSB							LSB
0	0	0	0	0	0	0	1

Operation: The screen is cleared and the cursor returns to the 1st digit.

b) Cursor return

Code:

MSB							LSB
0	0	0	0	0	0	1	0

Operation: The cursor returns to the 1st digit and the characters being displayed do not change.

c) Cursor ON/OFF

Code:

MSB							LSB	
0	0	0	0	0	1	0	0	(ON)
0	0	0	0	0	1	0	1	(OFF)

Operation: The cursor appears (ON) or disappears (OFF).

d) Set cursor position

Code:

		MSB		LSB
1 line		1	(N-1) binary	
2 lines	upper	1	0	(n-1) binary
	lower	1	1	(m-1) binary

N,n,m: digit number

Operation: The cursor moves to the Nth (nth, mth) digit.

N ≤ the total character number;

n,m ≤ 1/2 total character number.

ex 1 *1 line*

Set the cursor at 55 digit. The code is '10110110'.

ex 2 *2 lines*

Set the cursor at 35 digit of upper or lower line.

The code is '10100010' (upper).

'11100010' (lower),

- Display Character Command

When the character code is written into the character register of HD43160AH, the character of this code appears where the cursor was displayed and the cursor moves to the next digit. (RS0='H', R/W='L')

MSB LSB

code: (CHARACTER CODE)

ex. 1

before ABCD_

after ABCDE_

- Read Busy Flag

When CS0 ~ CS3='H', R/W='H' and E='H' (RS0='don't care'), the Busy/Ready signal appears on DB7.

DB7 'H': BUSY

'L': READY

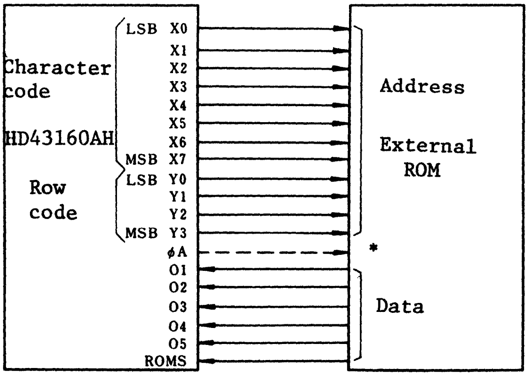
Time Length of Busy (oscillation frequency=200kHz)

	MIN	MAX	
Display clear	2.0	2.05	ms
Other operations	50	100	μs

(depends on the operating frequency)

- Interface to External ROM

a) Example

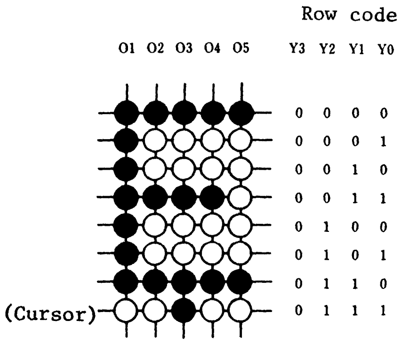


ROMS
1: Ext.
0: Int.

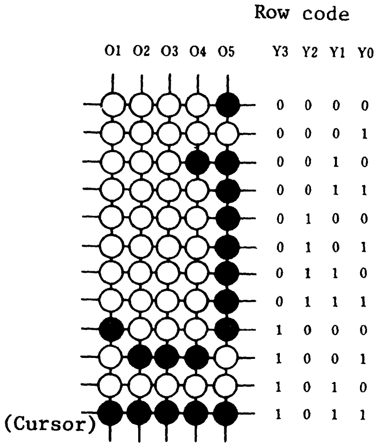
*φA is used as the precharge signal for Dynamic ROM if necessary.

Interface to External ROM

b) Row code

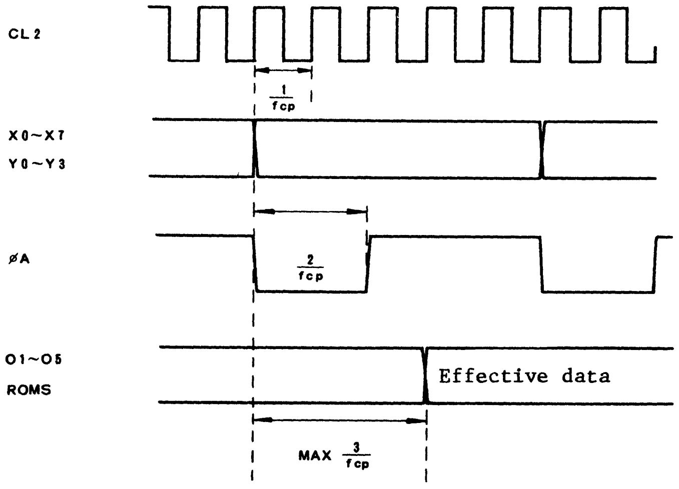


5 × 7 + Cursor



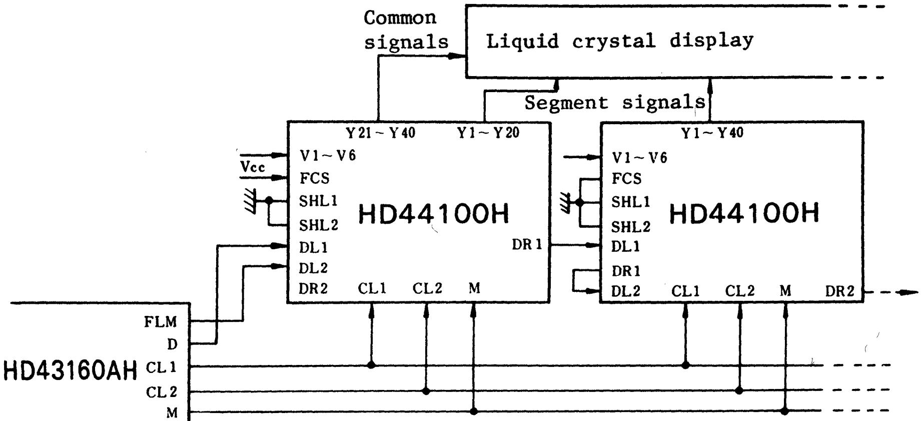
5 × 11 + Cursor

c) Timing chart



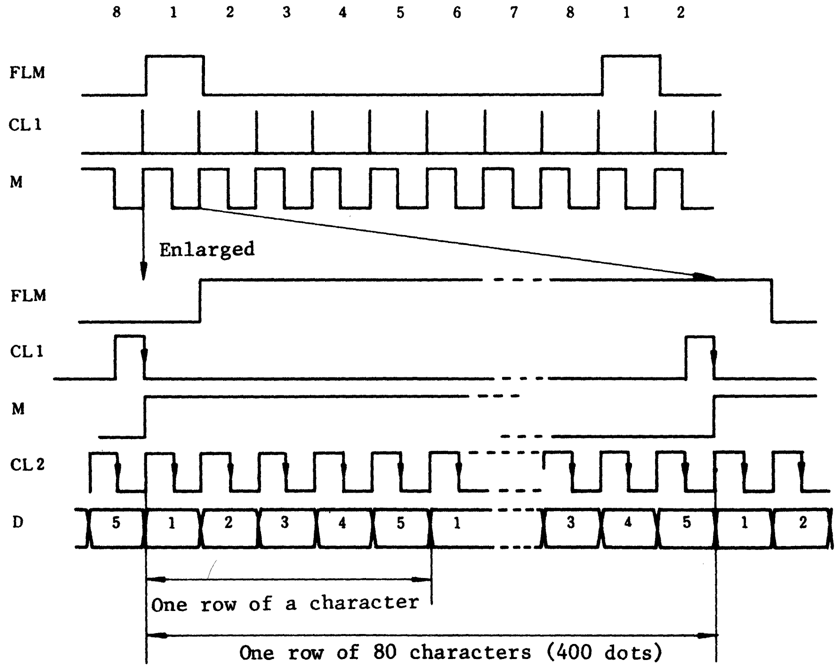
- Interface to LCD Drivers

a) Example



Interface to HD44100H

b) Wave forms (5 × 7 + Cursor 1 line)

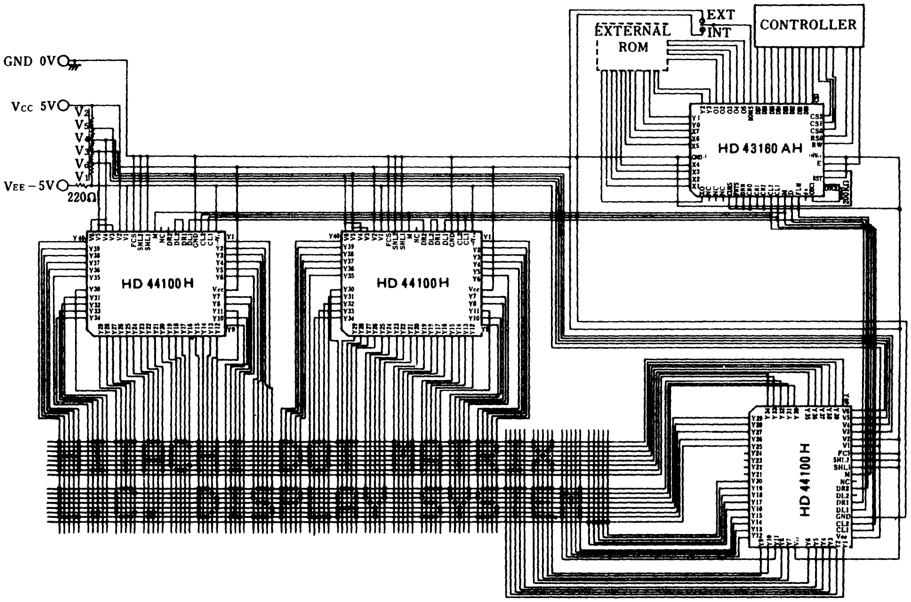


■ DOT MATRIX LIQUID CRYSTAL DISPLAY SYSTEM

Typical Application

5 ×7 +Cursor

2 Lines 40 Characters



HD44780, HD44780A (LCD-II)

(Dot Matrix Liquid Crystal Display Controller & Driver)

DESCRIPTION

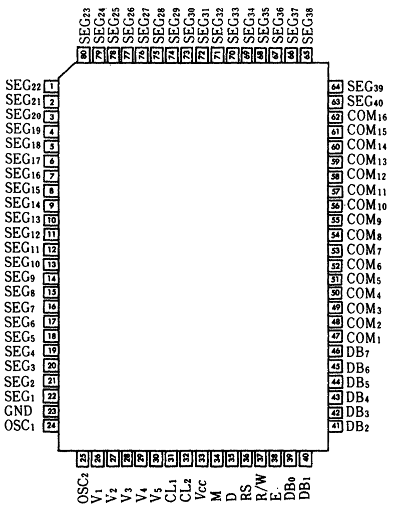
The LCD-II (HD44780, HD44780A) is a dot matrix liquid crystal display controller & driver LSI that displays alphanumerics, kana characters and symbols. It drives dot matrix liquid crystal display under 4-bit or 8-bit microcomputer or microprocessor control. All the functions required for dot matrix liquid crystal display drive are internally provided on one chip. The user can complete dot matrix liquid crystal display systems with less number of chips by using the LCD-II (HD44780, HD44780A). If a driver LSI HD44100H is externally connected to the HD44780, up to 80 characters can be displayed.

The LCD-II is produced in the CMOS process. Therefore, the combination of the LCD-II with a CMOS microcomputer or microprocessor can accomplish a portable battery-drive device with lower power dissipation.

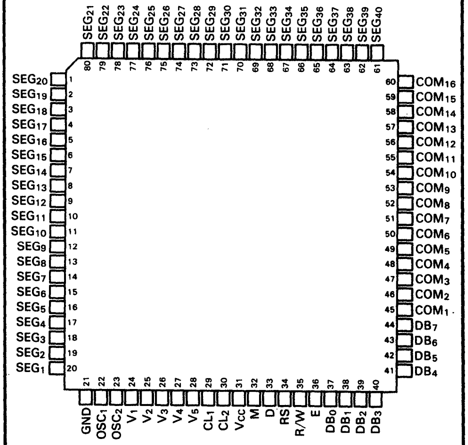
■ FEATURES

- 5 × 7 and 5 × 10 dot matrix liquid crystal display controller driver
- Capable of interfacing to 4-bit or 8-bit MPU.
- Display data RAM ... 80 × 8 bits (80 characters, max.)
- Character generator ROM ...
  Character font 5 × 7 dots: 160 characters
  Character font 5 × 10 dots: 32 characters

■ PIN ARRANGEMENT



(FP-80)
(Top View)



(FP-80A)
(Top View)

- Both display data and character generator RAMs can be read from the MPU.
- Internal liquid crystal display driver .....
  16 common signal drivers
  40 segment signal drivers (Can be externally extended to 360 segments by liquid crystal display driver HD44100H)
- Duty factor selection (selected by program) .....
  1/8 duty: 1 line of 5 × 7 dots + cursor
  1/11 duty: 1 line of 5 × 10 dots + cursor
  1/16 duty: 2 lines of 5 × 7 dots + cursor

  Maximum number of display characters

No. of display lines	Duty factory	Extension	LCD-II	HD44100H	No. of display characters
1-line display	1/8 1/11 duty	Not provided	1 pc.	—	8 characters ×1 line
		provided	1 pc.	9 pcs. (8 characters/pc.)	80 characters ×1 line
2-line display	1/16 duty	Not provided	1 pc.	—	8 characters ×2 lines
		provided	1 pc.	4 pcs.(8 characters ×2 lines/pc)	40 characters ×2 lines

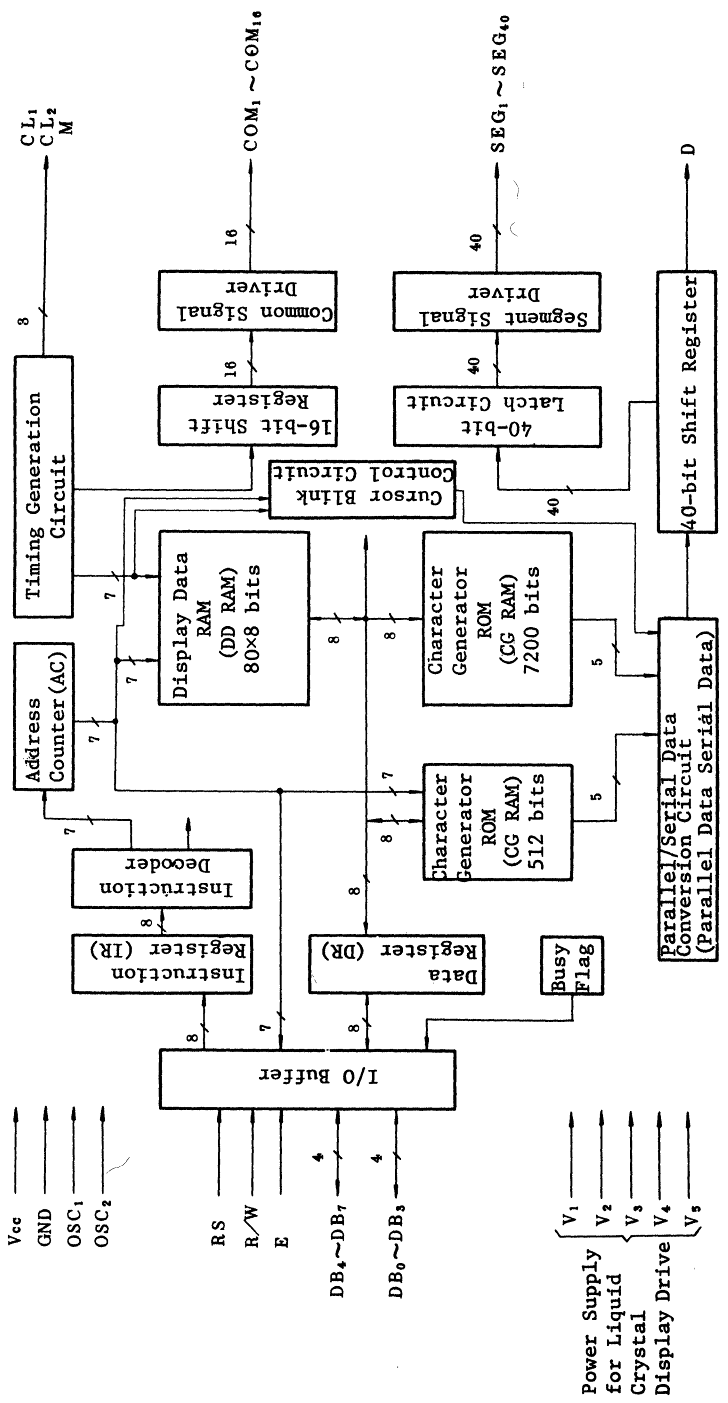
- Wide range of instruction functions
  Display clear, Cursor home, Display ON/OFF, Cursor ON/OFF,
  Display character blink, Cursor shift, Display shift
- Internal automatic reset circuit at power ON. (Internal reset circuit)
- Internal oscillation circuit (with external resistor or ceramic filter)
  (External clock operation possible)
- CMOS process
- Logic power supply: A single + 5V (excluding power for liquid crystal display drive)
- Operation temperature range: -20 ~ +75°C
  (Device for -40 ~ +85°C available upon request)
- 80-pin plastic QFP (FP-80, FP-80A)

■ ORDERING INFORMATION

Type No.	Operation Frequency	Package
HD44780SA**H	1.0 MHz	80-Pin plastic QFP (FP-80)
HD44780SA**FH		80-Pin plastic QFP (FP-80A)
HD44780SA**FA	1.5 MHz	80-Pin plastic QFP (FP-80)

Note: ** = ROM Code No.

■ BLOCK DIAGRAM (LCD-II INTERIOR)


Vcc
GND
OSC₁
OSC₂
RS
R/W
E
DB₄~DB₇
DB₀~DB₃
4
4
I/O Buffer
8
7
8
Instruction Register (IR)
8
Instruction Decoder
7
Data Register (DR)
8
Busy Flag
Address Counter (AC)
7
Timing Generation Circuit
3
CL₁
CL₂
M
7
7
Display Data RAM (DD RAM) 80×8 bits
8
8
8
7
Character Generator ROM (CG RAM) 512 bits
Character Generator ROM (CG RAM) 7200 bits
5
5
Cursor Blink Control Circuit
16-bit Shift Register
16
Common Signal Driver
16
COM₁~COM₁₆
40-bit Latch Circuit
40
Segment Signal Driver
40
SEG₁~SEG₄₀
40
Parallel/Serial Data Conversion Circuit (Parallel Data Serial Data)
40-bit Shift Register
D
Power Supply for Liquid Crystal Display Drive
V₁
V₂
V₃
V₄
V₅

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

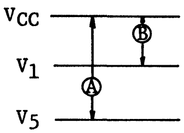
Item	Symbol	Limit	Unit	Note
Power Supply Voltage (1)	V_{CC}	-0.3 to +7.0	V	
Power Supply Voltage (2)	V1 to V5	V_{CC}-13.5 to V_{CC}+0.3	V	3
Input Voltage	V_T	-0.3 to V_{CC}+0.3	V	
Operating Temperature	Topr	-20 to +75	°C	
Storage Temperature	Tstg	-55 to +125	°C	

Note 1: If LSI's are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristic limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.

Note 2: All voltage values are referenced to GND=0V.

Note 3: Applies to V1 to V5. Must maintain $V_{CC} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$
(high ← → low)

- Electrical Characteristics (V_{CC} = 5V±10%, Ta = -20 to +75°C)



Ⓐ = $V_{CC}-V_5$
Ⓑ = $V_{CC}-V_1$
Ⓐ $\geqq$ 1.5V
Ⓑ $\leqq$ 0.25 ×A

[The conditions of V_1, V_5 voltages are for proper operation of the LSI and not for the LCD output level. The LCD drive voltage condition for the LCD output level is specified in "LCD voltage V_{LCD}".]

HD44780

Item	Symbol	Test condition	Limit min	Limit typ	Limit max	Unit	Note
Input "High" Voltage (1)	V_{IH1}		2.2	-	V_{CC}	V	(2)
Input "Low" Voltage (1)	V_{IL1}		-0.3	-	0.6	V	(2)
Output "High" Voltage (1)(TTL)	V_{OH1}	$-I_{OH}$=0.205mA	2.4	-	-	V	(3)
Output "Low" Voltage (1) (TTL)	V_{OL1}	I_{OL}=1.2mA	-	-	0.4	V	(3)
Output "High" Voltage (2)(CMOS)	V_{OH2}	$-I_{OH}$=0.04mA	$0.9V_{CC}$	-	-	V	(4)
Output "Low" Voltage (2) (CMOS)	V_{OL2}	L_{OL}=0.04mA	-	-	$0.1V_{CC}$	V	(4)
Driver Voltage Descending (COM)	V_{COM}	Id=0.05mA	-	-	2.9	V	(10)
Driver Voltage Descending (SEG)	V_{SEG}	Id=0.05mA	-	-	3.8	V	(10)
Input Leakage Current	I_{IL}	V_{in}=0 to V_{CC}	-1	-	1	μA	(5)
Pull up MOS Current	$-I_P$	V_{CC}=5V	50	125	250	μA	
Power Supply Current (1)	I_{CC1}	Ceramic filter oscillation V_{CC}=5V, f_{osc}= 250kHz	-	0.55	0.8	mA	(6)
Power Supply Current (2)	I_{CC2}	Rf oscillation External clock operation V_{CC}=5V, f_{osc}= fcp=270kHz	-	0.35	0.6	mA	(6) (11)
External Clock Operation							
External Clock Frequency	f_{cp}		125	270	350	kHz	(7)
External Clock Duty	Duty		45	50	55	%	(7)
External Clock Rise Time	t_{rcp}		-	-	0.2	μs	(7)
External Clock Fall Time	t_{fcp}		-	-	0.2	μs	(7)
Input "High" Voltage (2)	V_{IH2}		V_{CC}-1.0	-	-	V	(12)
Input "Low" Voltage (2)	V_{IL2}		-	-	1.0	V	(12)
Internal Clock Operation (Rf oscillation)							
Clock Oscillation Frequency	f_{osc}	Rf=91kΩ±2%	190	270	350	kHz	(8)
Internal Clock Operation (Ceramic filter oscillation)							
Clock Oscillation Frequency	f_{osc}	Ceramic filter	245	250	255	kHz	(9)
LCD Voltage	V_{LCD1}	$V_{CC}-V_5$ 1/5 bias	4.6	-	11	V	(13)
	V_{LCD2}	$V_{CC}-V_5$ 1/4 bias	3.0	-	11	V	(13)

HITACHI

HD44780A

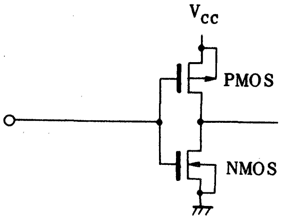
Item	Symbol	Test condition	Limit min	Limit typ	Limit max	Unit	Note
Input "High" Voltage (1)	V_{IH1}		2.2	-	V_{CC}	V	(2)
Input "Low" Voltage (1)	V_{IL1}		-0.3	-	0.6	V	(2)
Output "High" Voltage (1)(TTL)	V_{OH1}	$-I_{OH}$=0.205mA	2.4	-	-	V	(3)
Output "Low" Voltage (1) (TTL)	V_{OL1}	I_{OL}=1.2mA	-	-	0.4	V	(3)
Output "High" Voltage (2)(CMOS)	V_{OH2}	$-I_{OH}$=0.04mA	0.9V_{CC}	-	-	V	(4)
Output "Low" Voltage (2) (CMOS)	V_{OL2}	I_{OL}=0.04mA	-	-	0.1V_{CC}	V	(4)
Driver Voltage Descending (COM)	V_{COM}	Id=0.05mA	-	-	2.9	V	(10)
Driver Voltage Descending (SEG)	V_{SEG}	Id=0.05mA	-	-	3.8	V	(10)
Input Leakage Current	I_{IL}	V_{in}=0 to V_{CC}	-1	-	1	μA	(5)
Pull up MOS Current	$-I_P$	V_{CC}=5V	50	125	250	μA	
Power Supply Current (1)	I_{CC1}	Ceramic filter oscillation V_{CC}=5V, f_{osc}=250kHz	-	0.55	0.8	mA	(6)
Power Supply Current (2)	I_{CC2}	Rf oscillation External clock operation V_{CC}=5V, f_{osc}=fcp=270kHz	-	0.35	0.6	mA	(6) (11)
External Clock Operation							
External Clock Frequency	f_{cp}		125	270	350	kHz	(7)
External Clock Duty	Duty		45	50	55	%	(7)
External Clock Rise Time	t_{rcp}		-	-	0.2	μs	(7)
External Clock Fall Time	t_{fcp}		-	-	0.2	μs	(7)
Input "High" Voltage (2)	V_{IH2}		V_{CC}-1.0	-	-	V	(12)
Input "Low" Voltage (2)	V_{IL2}		-	-	1.0	V	(12)
Internal Clock Operation (Rf oscillation)							
Clock Oscillation Frequency	f_{osc}	Rf=91kΩ±2%	190	270	350	kHz	(8)
Internal Clock Operation (Ceramic filter oscillation)							
Clock Oscillation Frequency	f_{osc}	Ceramic filter	245	250	255	kHz	(9)
LCD Voltage.	V_{LCD1}	V_{CC}-V5 1/5 bias	4.6	-	11	V	(13)
	V_{LCD2}	V_{CC}-V5 1/4 bias	3.0	-	11	V	(13)

Note 1: The following are I/O terminal configurations except for liquid crystal display output.

- Input Terminal

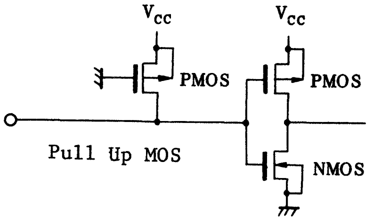
Applicable Terminals: E

(No pull up MOS)



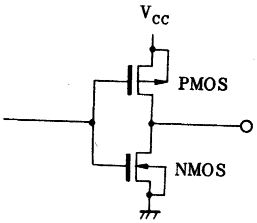
Applicable Terminals: RS, R/W

(With pull up MOS)



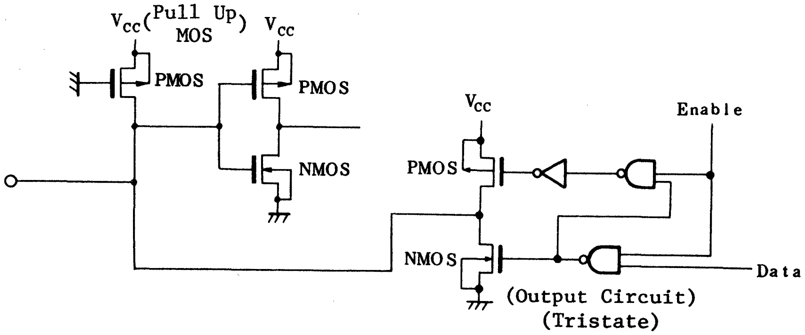
- Output Terminal

Applicable Terminals: CL_1, CL_2, M, D



- I/O Terminal

Applicable Terminals: DB_0 to DB_7



Note 2: Input terminals and I/O terminals. Excludes OSC_1 terminals.

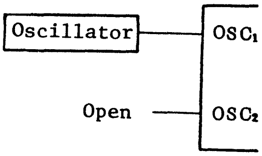
Note 3: I/O terminals.

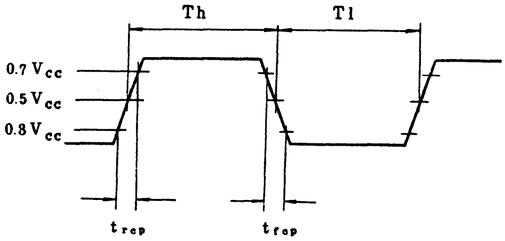
Note 4: Output terminals.

Note 5: Current flowing through pull-up MOS's and output drive MOS's is excluded.

Note 6: Input/Output current is excluded. When input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low.

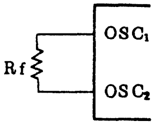
Note 7: External clock operation.





$$\mathrm{Duty} = \frac{Th}{Th + Tl} \times 100\%$$

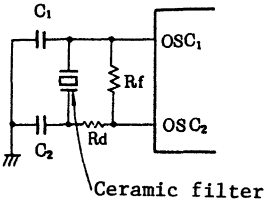
Note 8: Internal oscillator operation using oscillation resistor Rf.



Rf : 91kΩ± 2 %

Since oscillation frequency varies depending on OSC_1 and OSC_2 terminal capacity, wiring length for these terminals should be minimized.

Note 9: Internal oscillator operation using a ceramic filter.is used.



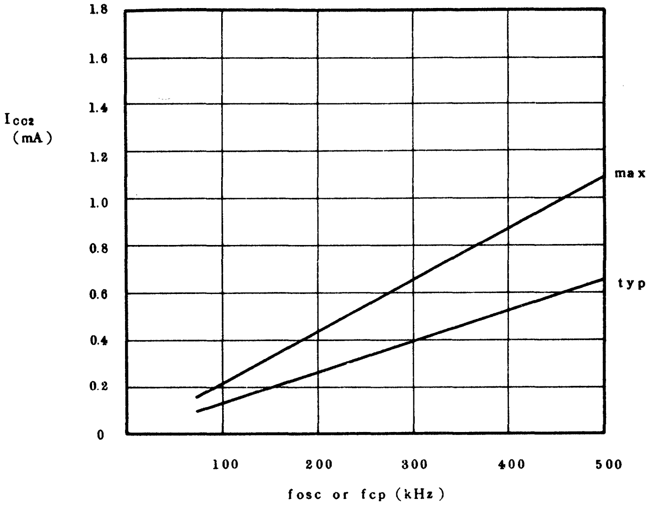
Ceramic filter: CSB250A (Murata)
Rf: 1MΩ ±10%
C_1: 680pF±10%
C_2: 680pF±10%
Rd: 3.3kΩ±5%

Note 10: Applies to both V_{COM} and V_{SEG} voltage drops.

V_{COM}: From poer supply terminal V_{CC}, V_1, V_4, V_5 to each common signal terminal (COM_1 to COM_{16})

V_{SEG}: From power supply terminal V_{CC}, V_2, V_3, V_5 to each segment signal terminal (SEG_1 to SEG_{40})

Note 11: Relation between operation frequency and current consumption is shown in this diagram. (V_{CC} = 5V)



Note 12: Applied to OSC_1 terminal.

Note 13: The condition for COM pin voltage drop (V_{COM}) and SEG pin voltage drop (V_{SEG}).

- **Timing Characteristics**

Write Operation

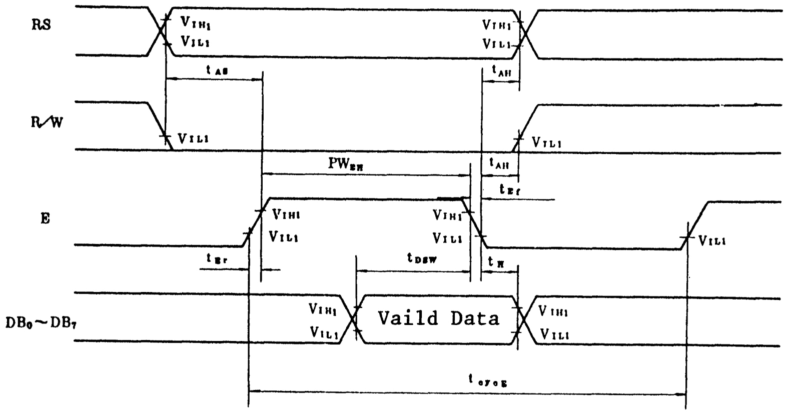


Fig. 1 Bus Write Operation Sequence
(Writing data from MPU to LCD-II)

Read Operation

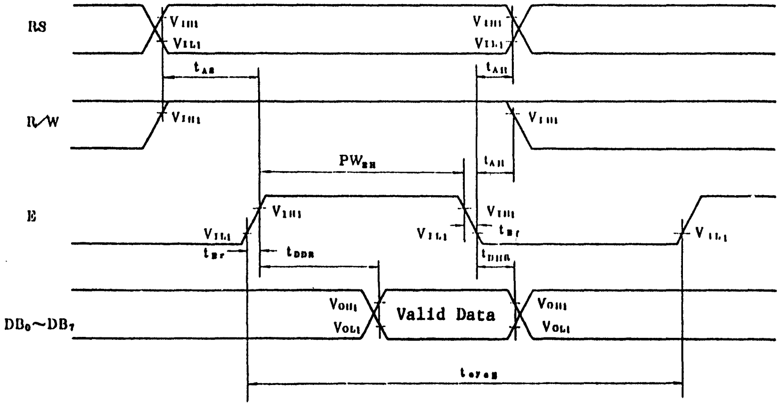


Fig. 2 Bus Read Operation Sequence
(Reading out data from LCD-II to MPU)

Interface Signal with Driver LSI HD44100H

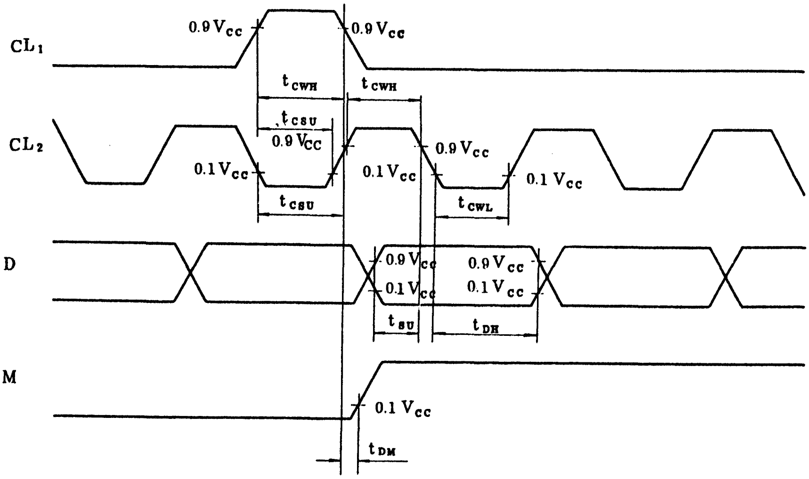


Fig. 3 Sending Data to Driver LSI HD44100H

- Bus Timing Characteristics (V_{CC} = 5.0V ± 10%, GND = 0V, Ta = -20 to +75°C)

o HD44780

Write Operation (Writing data from MPU to LCD-II)

Item		Symbol	Test condition	Limit		Unit
				min	max	
Enable Cycle Time		t_{cycE}	Fig. 1	1000	-	ns
Enable Pulse Width	"High" level	PW_{EH}	Fig. 1	450	-	ns
Enable Rise/Fall Time		t_{Er}, t_{Ef}	Fig. 1	-	25	ns
Address Set-up Time	RS, R/W —E	t_{AS}	Fig. 1	140	-	ns
Address Hold Time		t_{AH}	Fig. 1	10	-	ns
Data Set-up Time		t_{DSW}	Fig. 1	195	-	ns
Data Hold Time		t_H	Fig. 1	10	-	ns

Read Operation (Reading data from LCD-II to MPU)

Item		Symbol	Test condition	Limit		Unit
				min	max	
Enable Cycle Time		t_{cycE}	Fig. 2	1000	-	ns
Enable Pulse Width	"High" level	PW_{EH}	Fig. 2	450	-	ns
Enable Rise/Fall Time		t_{Er}, T_{Ef}	Fig. 2	-	25	ns
Address Set-up Time	RS, R/W —E	t_{AS}	Fig. 2	140	-	ns
Address Hold Time		t_{AH}	Fig. 2	10	-	ns
Data Delay Time		t_{DDR}	Fig. 2	-	320	ns
Data Hold Time		t_{DHR}	Fig. 2	20	-	ns

o HD44780A

Write Operation (Writing data from MPU to LCD-II)

Item		Symbol	Test condition	Limit		Unit
				min	max	
Enable Cycle Time		t_{cycE}	Fig. 1	666	-	ns
Enable Pulse Width	"High" level	PW_{EH}	Fig. 1	300	-	ns
Enable Rise/Fall Time		t_{Er}, t_{Ef}	Fig. 1	-	25	ns
Address Set-up Time	RS, R/W —E	t_{AS}	Fig. 1	60*1	-	ns
				100*2	-	ns
Address Hold Time		t_{AH}	Fig. 1	10	-	ns
Data Set-up Time		t_{DSW}	Fig. 1	100	-	ns
Data Hold Time		t_{H}	Fig. 1	10	-	ns

Read Operation (Reading data from LCD-II to MPU)

Item		Symbol	Test condition	Limit		Unit
				min	max	
Enable Cycle Time		t_{cycE}	Fig. 2	666	-	ns
Enable Pulse Width	"High" level	PW_{EH}	Fig. 2	300	-	ns
Enable Rise/Fall Time		t_{Er}, T_{Ef}	Fig. 2	-	25	ns
Address Set-up Time	RS, R/W —E	t_{AS}	Fig. 2	60*1		ns
				100*2		
Address Hold Time		t_{AH}	Fig. 2	10	-	ns
Data Delay Time		t_{DDR}	Fig. 2	-	190	ns
Data Hold Time		t_{DHR}	Fig. 2	20	-	ns

Notes: *1. *1, is 8-bit interface mode
*2. *2, is 4-bit interface mode

- **Interface Signal with HD44100H Timing Characteristics**
  (V_{CC} = 5.0V ± 10%, GND = 0V, Ta = -20 to +75°C)

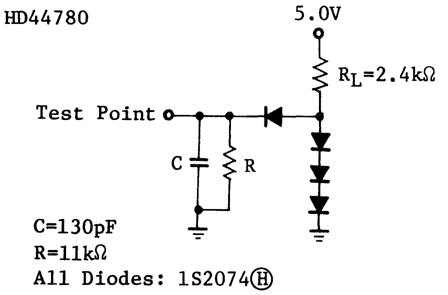
o HD44780

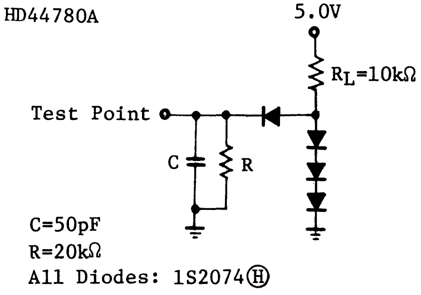
Item		Symbol	Test condition	Limit min	Limit max	Unit
Clock Pulse Width	"High" level	t_{CWH}	Fig. 3	800	-	ns
Clock Pulse Width	"Low" level	t_{CWL}	Fig. 3	800	-	ns
Clock Set-up Time		t_{CSU}	Fig. 3	500	-	ns
Data Set-up Time		t_{SU}	Fig. 3	300	-	ns
Data Hold Time		t_{DH}	Fig. 3	300	-	ns
M Delay Time		t_{DM}	Fig. 3	-1000	1000	ns

HD44780A

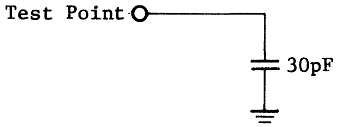
Item		Symbol	Test condition	Limit min	Limit max	Unit
Clock Pulse Width	"High" level	t_{CWH}	Fig. 3	800	-	ns
Clock Pulse Width	"Low" level	t_{CWL}	Fig. 3	800	-	ns
Clock Set-up Time		t_{CSU}	Fig. 3	500	-	ns
Data Set-up Time		t_{SU}	Fig. 3	300	-	ns
Data Hold Time		t_{DH}	Fig. 3	300	-	ns
M Delay Time		t_{DM}	Fig. 3	-1000	1000	ns

Loading Circuit (TTL Load); DB_0 to DB_7





Loading Circuit (CMOS Load); CL_1, CL_2, D, M

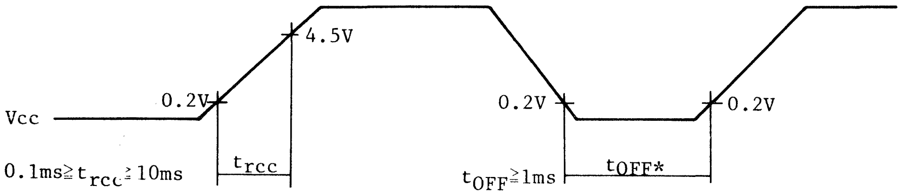


- **Power Supply Conditions Using Internal Reset Circuit**

LCD-II

Item	Symbol	Test condition	Limit		Unit
			min	max	
Power Supply Rise Time	trcc	-	0.1	10	ms
Power Supply OFF Time	t_{OFF}	-	1	-	ms

Since the internal reset circuit will not operate normally unless the preceding conditions are met, initialize by instruction. (Refer to "Initializing by Instruction")


4.5V
0.2V
Vcc
0.2V
0.2V
$0.1\text{ms} \leqq t_{rcc} \leqq 10\text{ms}$
t_{rcc}
$t_{OFF} \geqq 1\text{ms}$
t_{OFF}*

(Note) t_{OFF} stipulates the time of power OFF for power supply instantaneous dip or when power supply repeats ON and OFF.

Terminal Function

Table 1 Functional Description of Terminals

Signal name	No. of lines	Input/ Output	Connected to	Function
RS	1	Input	MPU	Signal to select registers "0": Instruction register (for write) Busy flag; address counter (for read) "1": Data register (for read and write)
R/W	1	Input	MPU	Signal to select read (R) and write (W) "0": Write "1": Read
E	1	Input	MPU	Operation start signal for data read/ write
DB$_4$ ~ DB$_7$	4	Input/ Output	MPU	Higher order 4 lines data bus with bidirectional three-state. Used for data transfer between the MPU and the LCD-II. DB$_7$ can be used as a BUSY flag.
DB$_0$ ~ DB$_3$	4	Input/ Output	MPU	Lower order 4 lines data bus with bidirectional three-state. Used for data transfer between the MPU and the LCD-II. These four are not used during 4-bit operation.
CL$_1$	1	Output	HD44100H	Clock to latch serial data D sent to the driver LSI HD44100H.
CL$_2$	1	Output	HD44100H	Clock to shift serial data D.
M	1	Output	HD44100H	Switch signal to convert liquid crystal drive waveform to AC.
D	1	Output	HD44100H	Character pattern data corresponding to each common signal is serially sent. "0": Non selection "1": Selection
COM$_1$ ~ COM$_{16}$	16	Output	Liquid crystal display	Common signals that are not used are charged to non-selection waveforms. That is, COM$_9$ ~ COM$_{16}$ are in non-selection waveform at 1/8 duty factor, and COM$_{12}$ ~ COM$_{16}$ are in non-selection waveform at 1/11 duty factor.
SEG$_1$ ~ SEG$_{40}$	40	Output	Liquid crystal display	Segment signal
V$_1$ ~ V$_5$	5		Power supply	Power supply for liquid crystal display drive
V$_{CC}$, GND	2		Power supply	V$_{CC}$; +5V, GND; 0V
OSC$_1$, OSC$_2$	2			Terminals connected to resister or ceramic filter for internal clock osillation. For external clock operation, the clock is input to OSC$_1$.

FUNCTION OF EACH BLOCK

(1) Register

The HD44780 has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes such as display clear and cursor shift, and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can be written from the MPU but not read by the MPU.

The DR temporarily stores data to be written into the DD RAM or the CG RAM and data to be read out from DD RAM or CG RAM. Data written into the DR from the MPU is automatically written into the DD RAM or the CG RAM by internal operation. The DR is also used for data storage when reading data from the DD RAM or the CG RAM. When address information is written into the IR, data is read into the DR from the DD RAM or the CG RAM by internal operation. Data transfer to the MPU is then completed by the MPU reading DR. After the MPU reads the DR, data in the DD RAM or CG RAM at the next address is sent to the DR for the next read from the MPU. Register selector (RS) signals make their selection from these two registers.

Table 2 Register Selection

RS	R/W	Operation
0	0	IR write as internal operation (Display clear, etc.)
0	1	Read busy flag (DB_7) and address counter ($DB_0 \sim DB_6$)
1	0	DR write as internal operation (DR to DD or CG RAM)
1	1	DR read as internal operation (DD or CG RAM to DR)

(2) Busy flag (BF)

When the busy flag is "1", the HD44780 is in the internal operation mode, and the next instruction will not be accepted. As Table 2 shows, the busy flag is output to DB_7 when RS=0 and R/W=1. The next instruction must be written after ensuring that the busy flag is "0".

(3) Address counter (AC)

The address counter (AC) assigns addresses to DD and CG RAMs. When an instruction for address is written in IR, the address information is sent from IR to AC. Selection of either DD or CG RAM is also determined concurrently by the instruction.

After writing into (or reading from) DD or CG RAM display data, AC is automatically incremented by +1 (or decremented by -1). AC contents are output to $DB_0 \sim DB_6$ when RS=0 and R/W=1, as shown in Table 2.

(4) Display data RAM (DD RAM)

The display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 80×8 bits, or 80 characters. The display data RAM (DD RAM) that is not used for display can be used as a general data RAM. Relations between DD RAM addresses and positions on the liquid crystal display are shown below.

The DD RAM address (A_{DD}) is set in the Address Counter (AC) and is represented in hexadecimal.

	← Upper Order Bits			Lower Order Bits →			
AC	AC6	AC5	AC4	AC3	AC2	AC1	AC0
	Hexadecimal			Hexadecimal			

(Example) DD RAM address "4E"

1	0	0	1	1	1	0
4			E			

1-line Display (N=0)

(digit)	1	2	3	4	5		79	80	← Display Position
1-line	00	01	02	03	04	······················	4E	4F	← DD RAM Address

(a) When the display characters are less than 80, the display begins at the head position. For example, 8 characters using 1 HD44780 are displayed as:

(digit)	1	2	3	4	5	6	7	8	← Display Position
1-line	00	01	02	03	04	05	06	07	← DD RAM Address

When the display shift operation is performed, the DD RAM address moves as:

(Left Shift Display)	01	02	03	04	05	06	07	08
(Right Shift Display)	4F	00	01	02	03	04	05	06

(b) 16-character display using an HD44780 and an HD44100H is as shown below:

(digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display Position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM Address
	HD44780 Display								HD44100H Display								

When the display shift operation is performed, the DD RAM address moves as:

(Left Shift Display	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
(Right Shift Display)	4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E

(c) The relation between display position and DD RAM address when the number of display digits is increased through the use of one HD44780 and two or more HD44100H's can be considered an extension of (b).

Since the increase can be 8 digits for each additional HD44100H, up to 80 digits can be displayed by externally connecting 9 HD44100H's.

(digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		73	74	75	76	77	78	79	80	← Display Position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	----	48	49	4A	4B	4C	4D	4E	4F	← DD RAM Address
	HD44780 Diaplay								HD44100H(1) Display								HD44100H (2)∿(8) Display					HD44100H(9) Display								

2-line Display (N=1)

(digit)	1	2	3	4	5		39	40	← Display Position
1-line	00	01	02	03	04	....	26	27	← DD RAM Address
2-line	40	41	42	43	44	....	66	67	

(a) When the number of display characters is less than 40 × 2 lines, the 2 lines from the head are displayed. Note that the first line end address and the second line start address are not consecutive. For example, when an HD44780 is used, 8 characters × 2 lines are displayed as:

(digit)	1	2	3	4	5	6	7	8	← Display Position
1-line	00	01	02	03	04	05	06	07	← DD RAM Address
2-line	40	41	42	43	44	45	46	47	

When display shift is performed, the DD RAM address moves as:

(Left Shift Display)	01	02	03	04	05	06	07	08
	41	42	43	44	45	46	47	48

(Right Shift Display)	27	00	01	02	03	04	05	06
	67	40	41	42	43	44	45	46

(b) 16 characters × 2 lines are displayed when an HD44780 and an HD44100H are used.

(digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display Position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM Address
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

└── HD44780 Display ──┘└── HD44100H Display ──┘

When display shift is performed, the DD RAM address moves as follows:

(Left Shift Display)	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50

(Right Shift Display)	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

(c) The relation between display position and DD RAM address when the number of display digits is increased by using one HD44780 and two or more HD44100H's, can be considered an extension of (b).

Since the increase can be 8 digits × 2 lines for each additional HD44100H, up to 40 digits 2 lines can be displayed by connecting 4 HD44780's externally.

(digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		33	34	35	36	37	38	39	40	←Display position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	------	20	21	22	23	24	25	26	27	←DD RAM address (Hexadecimal)
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	------	60	61	62	63	64	65	66	67	

HD44780 Display
HD44100H(1) Display
HD44100H (2)(3) Display
HD44100H(4) Display

(5) Character Generator ROM (CG ROM)

The character generator ROM generates 5 × 7 dot or 5 × 10 dot character patterns from 8-bit character codes. It can generate 160 types of 5 × 7 dot character patterns and 32 types of 5 × 10 dot character patterns. Table 3 and 4 show the relation between character codes and character patterns in the Hitachi standard HD44780A00. User defined character patterns are also available by mask-programming ROM.

(6) Character Generator RAM (CG RAM)

The character generator RAM is the RAM with which the user can rewrite character patterns by program. With 5 × 7 dots, 8 byptes of character patterns can be written and with 5 × 10 dots 4 types can be written. Write the character codes in the left columns of Tables 3 and 4 to display character patterns stored in CG RAM.

Table 5 shows the relation between CG RAM addresses and data and display patterns.

As Table 5 shows, an area that is not used for display can be used as a general data RAM.

Table 3 Correspondence between Character Codes and Character Pattern (Hitachi Standard HD44780A00)

Higher 4bit / Lower 4bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)		0	@	P	`	p		ー	タ	ミ	α	p
xxxx0001	(2)	!	1	A	Q	a	q	。	ア	チ	ム	ä	q
xxxx0010	(3)	"	2	B	R	b	r	「	イ	ツ	メ	β	θ
xxxx0011	(4)	#	3	C	S	c	s	」	ウ	テ	モ	ε	∞
xxxx0100	(5)	$	4	D	T	d	t	、	エ	ト	ヤ	μ	Ω
xxxx0101	(6)	%	5	E	U	e	u	・	オ	ナ	ユ	σ	ü
xxxx0110	(7)	&	6	F	V	f	v	ヲ	カ	ニ	ヨ	ρ	Σ
xxxx0111	(8)	'	7	G	W	g	w	ァ	キ	ヌ	ラ	g	π
xxxx1000	(1)	(	8	H	X	h	x	ィ	ク	ネ	リ	√	x̄
xxxx1001	(2)	)	9	I	Y	i	y	ゥ	ケ	ノ	ル	⁻¹	y
xxxx1010	(3)	*	:	J	Z	j	z	ェ	コ	ハ	レ	j	千
xxxx1011	(4)	+	;	K	[	k	{	ォ	サ	ヒ	ロ	ˣ	万
xxxx1100	(5)	,	<	L	¥	l	|	ャ	シ	フ	ワ	¢	円
xxxx1101	(6)	-	=	M	]	m	}	ュ	ス	ヘ	ン	£	÷
xxxx1110	(7)	.	>	N	^	n	→	ョ	セ	ホ	゛	ñ	
xxxx1111	(8)	/	?	O	_	o	←	ッ	ソ	マ	゜	ö	█

* The user can specify any pattern for character-generator ROM.

Table 4 Relation between CG RAM Addresses and Character Codes (DD RAM) and Character Patterns (CG RAM Data)

(a) For 5 × 7 dot character patterns

Character Codes (DD RAM Data)		CG RAM Address			Character Patterns (CG RAM Data)		
7 6 5 4 3 2 1 0 ← Higher Order Bits Lower Order Bits →		5 4 3 ← Higher Order Bits	2 1 0 Lower Order Bits →		7 6 5 ← Higher Order Bits	4 3 2 1 0 Lower Order Bits →	
0 0 0 0 * 0 0 0		0 0 0	0 0 0		* * *	1 1 1 1 0	Character Pattern Example (1)
			0 0 1			1 0 0 0 1	
			0 1 0			1 0 0 0 1	
			0 1 1			1 1 1 1 0	
			1 0 0			1 0 1 0 0	
			1 0 1			1 0 0 1 0	
			1 1 0			1 0 0 0 1	
			1 1 1		* * *	0 0 0 0 0	Cursor ← Position
0 0 0 0 * 0 0 1		0 0 1	0 0 0		* * *	1 0 0 0 1	Character Pattern Example (2)
			0 0 1			0 1 0 1 0	
			0 1 0			1 1 1 1 1	
			0 1 1			0 0 1 0 0	
			1 0 0			1 1 1 1 1	
			1 0 1			0 0 1 0 0	
			1 1 0			0 0 1 0 0	
			1 1 1		* * *	0 0 0 0 0	
			0 0 0		* * *		
			0 0 1				
0 0 0 0 * 1 1 1		1 1 1	1 0 0				*No effect
			1 0 1				
			1 1 0				
			1 1 1		* * *		

(Note) 1: Character code bits 0 ~ 2 correspond to CG RAM address bits 3 ~ 5 (3 bits: 8 types).

2: CG RAM address bits 0 ~ 2 designate character pattern line position. The 8th line is the cursor position and display is performed in logical OR by the cursor.

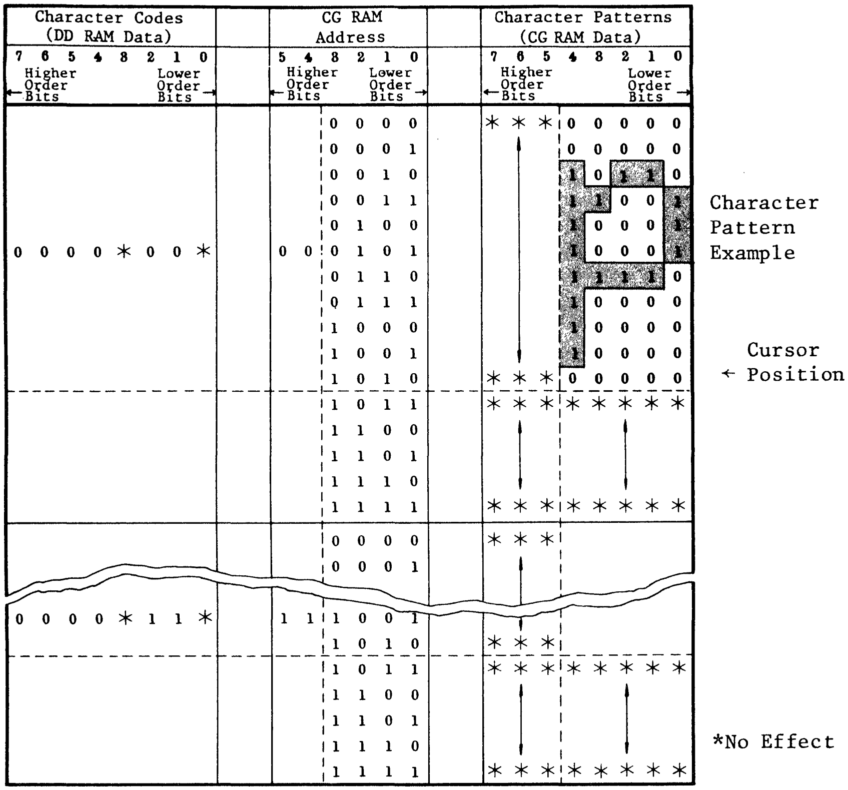
Maintain the 8th line data, corresponding to the cursor display position, in the "0" state for cursor display. When the 8th line data is "1", bit 1 lights up regardless of cursor existence.

3: Character pattern row positions correspond to CG RAM data bits 0 ~ 4, as shown in the figure (bit 4 being at the left end). Since CG RAM data bits 5 ~ 7 are not used for display, they can be used for the general data RAM.

4: As shown in Table 3 and 4, CG RAM character patterns are selected when character code bits 4 ~ 7 are all "0". However, since character code bit 3 is a ineffective bit,the "R" display in the character pattern example, is selected by character code "00" (hexadecimal) or "08" (hexadecimal).

5: "1" for CG RAM data corresponds to selection for display and "0" for non-selection.

(b) For 5 ×10 dot character patterns



Character Codes (DD RAM Data)	CG RAM Address		Character Patterns (CG RAM Data)	
7 6 5 4 3 2 1 0 ← Higher Order Bits — Lower Order Bits →	5 4 ← Higher Order Bits	3 2 1 0 Lower Order Bits →	7 6 5 ← Higher Order Bits	4 3 2 1 0 Lower Order Bits →
		0 0 0 0	* * *	0 0 0 0 0
		0 0 0 1	↕	0 0 0 0 0
		0 0 1 0		1 0 1 1 0
		0 0 1 1		1 1 0 0 1
		0 1 0 0		1 0 0 0 1
0 0 0 0 * 0 0 *	0 0	0 1 0 1		1 0 0 0 1
		0 1 1 0		1 1 1 1 0
		0 1 1 1		1 0 0 0 0
		1 0 0 0		1 0 0 0 0
		1 0 0 1		1 0 0 0 0
		1 0 1 0	* * *	0 0 0 0 0
		1 0 1 1	* * *	* * * * *
		1 1 0 0	↕	↕
		1 1 0 1		
		1 1 1 0		
		1 1 1 1	* * *	* * * * *
		0 0 0 0	* * *	
		0 0 0 1	↕	
0 0 0 0 * 1 1 *	1 1	1 0 0 1		
		1 0 1 0	* * *	
		1 0 1 1	* * *	* * * * *
		1 1 0 0	↕	↕
		1 1 0 1		
		1 1 1 0		
		1 1 1 1	* * *	* * * * *

Character Pattern Example

Cursor
← Position

*No Effect

(Note) 1: Character code bits 1, 2 correspond to CG RAM address bits 4, 5 (2 bits: 4 types).

2: CG RAM address bits 0 ~ 3 designate character pattern line position. The 11th line is the cursor position and display is performed in logical OR with cursor.

Maintain the 11th line data corresponding to the cursor display position in the "0" state for cursor display. When the 11th line data is "1", bit 1 lights up regardless of cursor existence. Since the 12th ~ 16th lines are not used for display, they can be used for the general data RAM.

3: Character pattern row positions are the same as 5 × 7 dot character pattern positions.

4: CG RAM character patterns are selected when character code bits 4 7 are all "0". However, since character code bit 0 and 3 are ineffective bits, "P" display in the character pattern example is selected by character code "00", "01", "08" and "09" (hexadecimal).

5: "1" for CG RAM data corresponds to selection for display and "0" for non-selection.

(7) Timing Generation Circuit

The timing generation circuit generates timing signals to operate internal circuits such as DD RAM, CG ROM and CG RAM. RAM read timing needed for display and internal operation timing by MPU access are separately generated so they do not interfere with each other. Therefore, when writing data to the DD RAM, for example, there will be no undersirable influence, such as flickering, in areas other than the display area. This circuit also generates timing signals to operate the externally connected driver LSI HD44100H.

(8) Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 16 common signal drivers and 40 segment signal drivers. When character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, the other common signal drivers continue to output non-selection waveforms.

The segment signal driver has essentially the same configuration as the driver LSI HD44100H. Character pattern data is sent serially through a 40-bit shift register and latched when all needed data has arrived. The latched data controls the driver for generating drive waveform outputs.

The serial data is sent to the HD44100H, externally connected in cascade, used for display digit number extension.

Send of serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM). Since serial data is latched when the display data character pattern, corresponding to the starting address, enters the internal shift register, the HD44780 drives the head display. The rest displays, corresponding to latter addresses, are added with each additional HD44100H.

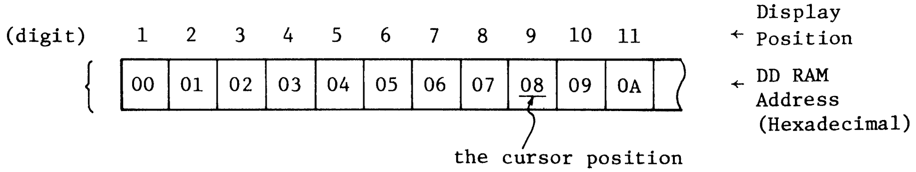
(9) Cursor/Blink Control Circuit

This is the circuit that generates the cursor or blink. The cursor or the blink appear in the digit residing at the display data RAM (DD RAM) address set in the address counter (AC).

When the address counter is $(08)_{16}$, a cursor position is:

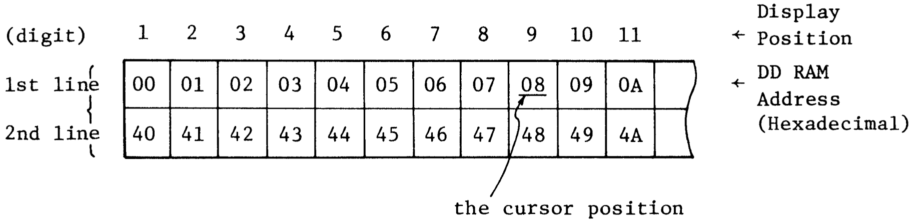
	AC6	AC5	AC4	AC3	AC2	AC1	AC0
AC	0	0	0	1	0	0	0

In a 1-line display



(digit)	1	2	3	4	5	6	7	8	9	10	11	
	00	01	02	03	04	05	06	07	08	09	0A	

In a 2-line display



(digit)	1	2	3	4	5	6	7	8	9	10	11	
1st line	00	01	02	03	04	05	06	07	08	09	0A	
2nd line	40	41	42	43	44	45	46	47	48	49	4A	

(Note) The cursor or blink appears when the address counter (AC) selects the character generator RAM (CG RAM). But the cursor and blink are meaningless.

The cursor or blink is displayed in the meaningless position when AC is the CG RAM address.

■ INTERFACING TO MPU

In the HD44780, data can be sent in either 4-bit 2-operation or 8-bit 1-operation so it can interace to both 4 and 8 bit MPU's.

(1) When interface data is 4-bits long, data is transferred using only 4 buses: $DB_4 \sim DB_7$. $DB_0 \sim DB_3$ are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of $DB_4 \sim DB_7$ when interface data is 8 bits long) is transferred first, then the lower order 4 bits (content of $DB_0 \sim DB_3$ when interface data is 8 bits long) is transferred.

Check the busy flag after 4-bit data has been transferred twice (one instruction). A 4-bit 2-operation will then transfer the busy flag and address counter data.

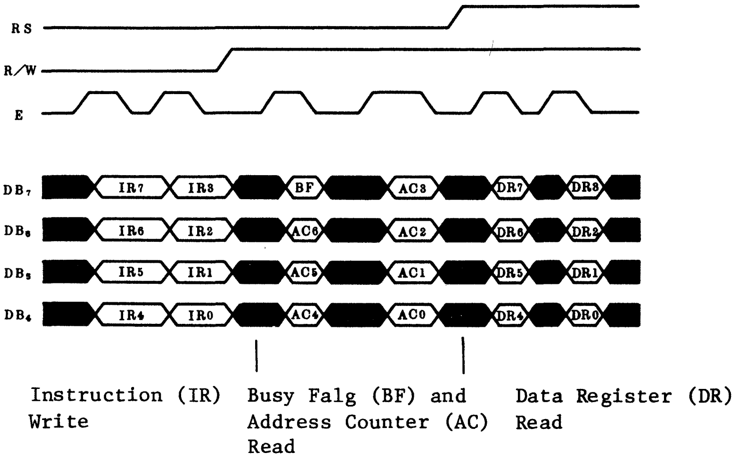


Fig. 4 4-bit Data Transfer Example

(2) When interface data is 8 bits long, data is transferred using the 8 data buses of $DB_0 \sim DB_7$.

■ RESET FUNCTION

● Initializing by Internal Reset Circuit

The HD44780 automatically initializes (resets) when power is turned on using the internal reset circuit. The following instructions are executed in initialization. The busy flag (BF) is kept in busy state until initialization ends. (BF=1) The busy state is 10 ms after V_{CC} rises to 4.5V.

(1) Display clear

(2) Function ser .... DL=1 : 8 bit long interface data
N =0 : 1-line display
F =0 : 5 ×7 dot character font

(3) Display ON/OFF control ...... D =0 : Display OFF
C =0 : Cursor OFF
B =0 : Blink OFF

(4) Entry mode set .... I/D=1: +1 (increment)
S =0 : No shift

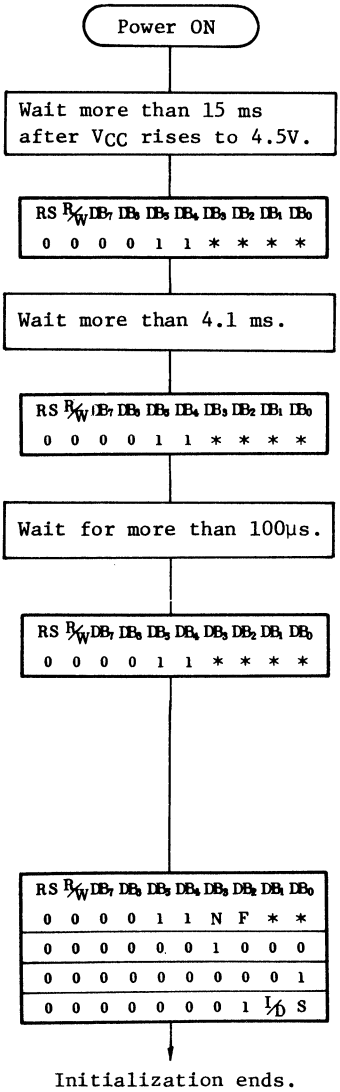
(Note) When conditions in "Power Supply Conditions Using Internal Reset Circuit" are not met, the internal reset circuit with not operate normally and initialization will not be performed. In this case initialize by MPU according to "Initializing by Instruction".

● Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instruction is required.

Use the following procedure for initialization.

(1) When interface is 8 bits long;



Power ON

Wait more than 15 ms after V_{CC} rises to 4.5V.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	*	*	*	*

BF cannot be checked before this instruction.

Function set (Interface is 8 bits long.)

Wait more than 4.1 ms.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	*	*	*	*

BF cannot be checked before this instruction.

Function set (Interface is 8 bits long.)

Wait for more than 100μs.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	*	*	*	*

BF cannot be checked before this instruction.

Function set (Interface is 8 bits long.)

BF can be checked after the following instructions. When BF is not checked, the waiting time between instructions is longer than the execution instruction time. (See Table 4-1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	N	F	*	*
0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	I/D	S

Function Set (Interface is 8 bits long. Specifiy the number of display lines and character font.)
The number of display lines and character font cannot be changed afterwards.

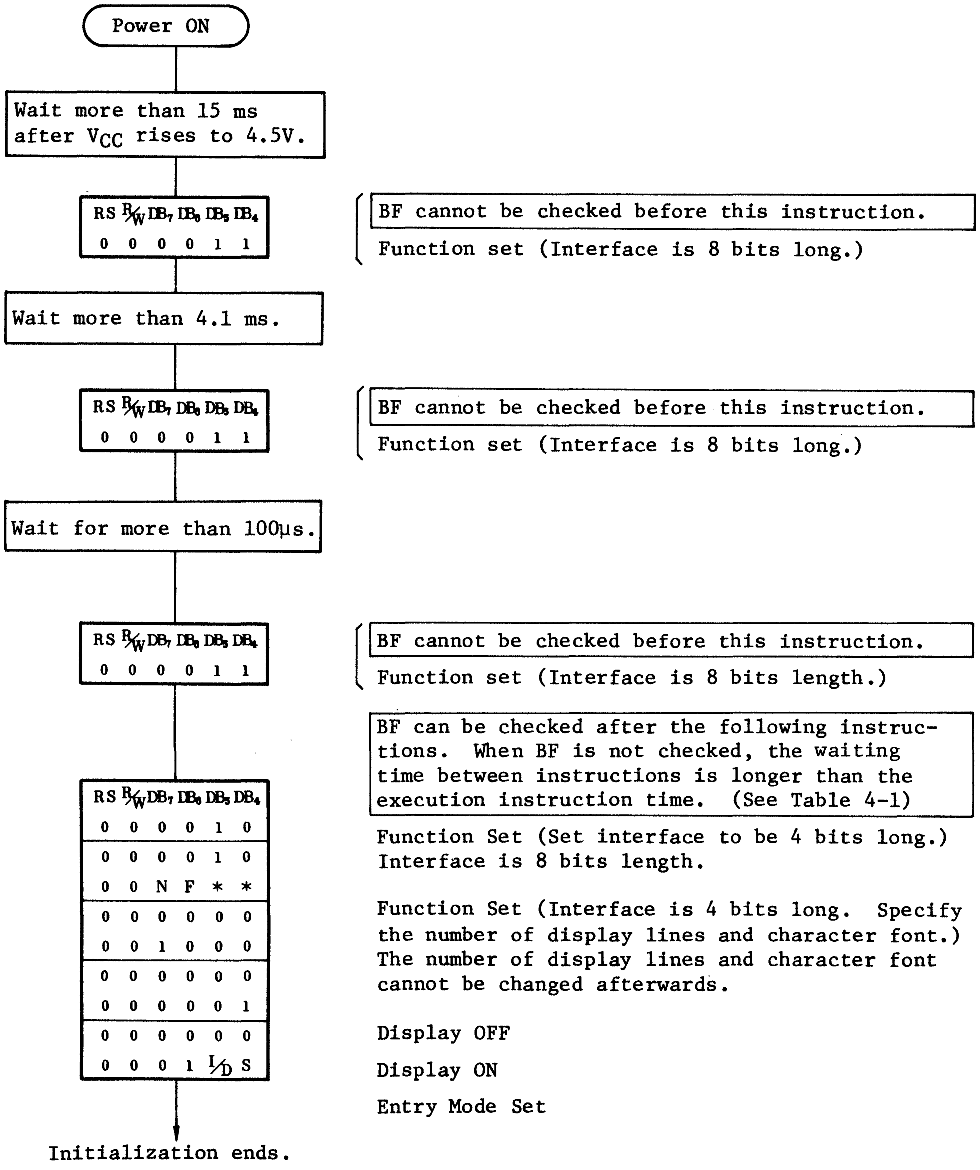
Display OFF

Display ON

Entry Mode Set

Initialization ends.

(2) When interface is 4 bits long;



BF cannot be checked before this instruction.

Function set (Interface is 8 bits long.)

BF cannot be checked before this instruction.

Function set (Interface is 8 bits long.)

BF cannot be checked before this instruction.

Function set (Interface is 8 bits length.)

BF can be checked after the following instructions. When BF is not checked, the waiting time between instructions is longer than the execution instruction time. (See Table 4-1)

Function Set (Set interface to be 4 bits long.) Interface is 8 bits length.

Function Set (Interface is 4 bits long. Specify the number of display lines and character font.) The number of display lines and character font cannot be changed afterwards.

Display OFF

Display ON

Entry Mode Set

■ INSTRUCTION

● Outline

Only two HD44780 registers, the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the MPU. Prior to internal operation start, control information is temporarily stored in these registers, to allow interface from HD44780 internal operation to various types of MPUs which operate in different speeds or to allow interface to peripheral control ICs. HD44780 internal operation is determined by signals sent from the MPU. These signals include register selection signals (RS), read/write signals (R/W) and data bus signals ($DB_0 \sim DB_7$), and are called instructions, here. Table 5 shows the instructions and their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that,

(1) Designate HD44780 functions such as display format, data length, etc.

(2) Give internal RAM addresses.

(3) Perform data transfer with internal RAM

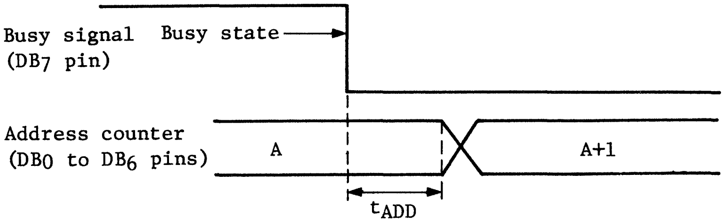
(4) Others

In normal use, category (3) instructions are used most frequently. However, automatic incrementing by +1 (or decrementing by -1) of HD44780 internal RAM addresses after each data write lessens the MPU program load. The display shift is especially able to perform concurrently with display data write, enabling the user to develop systems in minimum time with maximum programing efficiency. For an explanation of the shift function in its relation to display, see Table 7.

When an instruction is executing during internal operation, no instruction other than the busy flag/address read instruction will be executed. Because the busy flag is set to "1" while an instruction is being executed, check to make sure it is on "1" before sending an instruction from the MPU.

(Note) 1. Make sure the HD44780 is not in the busy state (BF=0) before sending the instruction from the MPU to the HD44780. If the instruction is sent without checking the busy flag, the time between first and next instructions is much longer than the instruction time. See Table 5 for a list of each instruction execution time.

2. After execution of a CG RAM/DD RAM data write or read instruction, the RAM address counter is increased or decreased by 1. The RAM address counter is updated after the busy flag turns off. Suppose that the time elapses after the busy flag turns off until the address counter is updated is t_{ADD}.



t_{ADD} depends on the operation frequency.

$t_{ADD}(sec) = 1.5/f_{cp}$ or f_{osc}

Table 5 Instructions

Instruction	Code										Description	Execution time (max) (when fcp or fosc is 250kHz)
	RS	R/W	DB$_7$	DB$_6$	DB$_5$	DB$_4$	DB$_3$	DB$_2$	DB$_1$	DB$_0$		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	1.64ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in adress counter. Also returns display being shifted to original position. DD RAM contents remain unchanged.	1.64ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read.	40µs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of entire display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40µs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents.	40µs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (L) and character font (F).	40µs
Set CG RAM Address	0	0	0	1	ACG						Sets CG RAM address. CG RAM data is sent and received after this setting.	40µs
Set DD RAM Address	0	0	1	ADD							Sets DD RAM address. DD RAM data is sent and received after this setting.	40µs
Read Busy Flag & Address	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0µs
Write Data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40µs t_{ADD}=6ns (Note 2)
Read Data from CG or DD RAM	1	0	Read Data								Reads data from DD RAM or CG RAM.	40µs t_{ADD}=6ns (Note 2)
	I/D=1 : Increment I/D=0 : Decrement S =1 : Accompanies display shift. S/C=1 : Display shift S/C=0 : Cursor move R/L=1 : Shift to the right. R/L=0 : Shifts to the left. DL =1 : 8 bits, DL=0 : 4 bits. N =1 : 2 lines, N=0 : 1 line F =1 : 5×10 dots, F=0 : 5×7 dots BF =1 : Internally operating BF =0 : Can accept instruction										DD RAM : Display data RAM CG RAM : Character generator RAM ACG : CG RAM address ADD : DD RAM address. Corresponds to cursor address. AC : Address counter used for both DD and CG RAM address.	Execution time changes when frequency changes. (Example) When fcp or fosc is 270kHz: $40\mu s \times \frac{250}{270} = 37\mu s$

* No Effect

Description of Details

(1) Clear Display

	RS	R/W	DB7							DB0
Code	0	0	0	0	0	0	0	0	0	1

Writes space code "20" (hexadecimal)(character pattern for character code "20" must be blank pattern) into all DD RAM addresses. Sets DD RAM address 0 in address counter. Returns display to its original status if it was shifted. In other words, the display disappears and the cursor or blink go to the left edge of the dispaly (the first line if 2 lines are displayed). Set I/D = 1 (Increment Mode) of Entry Mode. S of Entry Mode doesn't change.

(2) Return Home

	RS	R/W	DB7							DB0
Code	0	0	0	0	0	0	0	0	0	*

* Don't care

Sets the DD RAM address 0 in address counter. Returns display to its original status if it was shifted. DD RAM contents do not change. The cursor or blink go to the left edge of the display (the first line if 2 lines are displayed).

(3) Entry Mode Set

	RS	R/W	DB7							DB0
Code	0	0	0	0	0	0	0	0	I/D	S

I/D: Increments (I/D=1) or decrements (I/D=0) the DD RAM address by 1 when a character code is written into or read from the DD RAM. The cursor or blink moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S : Shifts the entire display either to the right or to the left when S is 1; to the left when I/D=1 and to the right when I/D=0. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM when writing into or reading out from the CG RAM does it shift when S=0.

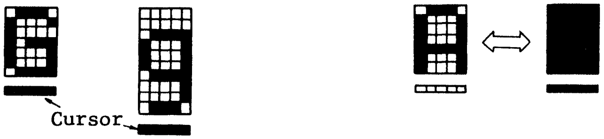
(4) Display ON/OFF Control

	RS	R/W	DB7							DB6
Code	0	0	0	0	0	0	1	D	C	B

D : The display is ON when D=1 and OFF when D=0. When off due to D=0, display data remains in the DD RAM. It can be displayed immediately by setting D=1.

C : The cursor displays when C=1 and does not display when C=0. Even if the cursor disappears, the function of I/D, etc. does not change during display data write. The cursor is displayed using 5 dots in the 8th line when the 5 × 7 dot character font is selected and 5 dots in the 11th line when the 5 × 10 dot character font is selected.

B : The character indicated by the cursor blinks when B=1. The blink is displayed by switching between all blank dots and display characters at 409.6ms interval when fcp or fosc=250kHz. The cursor and the blink can be set to display simultaneously. (The blink frequency changes according to the reciprocal of fcp or fosc. $409.6 \times \frac{250}{270} = 379.2$ms when fcp=270kHz.)



5 × 7 dot character font   5 × 10 dot character font   Alternating display

(a) Cursor Display Example   (b) Blink Display Example

(5) Cursor or Display Shift

	RS	R/W	DB7							DB0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* Don't care

Shifts cursor position or display to the right or left without writing or reading display data. This function is used to correct or search for the display. In a 2-line display, the cursor moves to the 2nd line when it passes the 40th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time. When the displayed data is shifted repeatedly each line only moves horizontally. The 2nd line display does not shift into the 1st line postion.

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

Address counter (AC) contents do not change if the only action performed is shift display.

(6) Function Set

	RS	R/W	DB7							DB0
Code	0	0	0	0	1	DL	N	F	*	*

* (Don't care)

DL : Sets interface data length. Data is sent or received in 8 bit lengths ($DB_7 \sim DB_0$) when DL=1 and in 4 bit lengths ($DB_7 \sim DB_4$) when DL=0.

When the 4 bit length is selected, data must be sent or received twice.

N : Sets number of display lines.

F : Sets character font.

(Note) Perform the function at the head of the program before executing all instructions (except "Busy flag/address read"). From this point, the function set instruction cannot be executed unless the interface data length is changed.

N F	No. of display lines	Character font	Duty factor	Remarks
0 0	1	5 ×7 dots	1/8	
0 1	1	5 ×10 dots	1/11	
1 *	2	5 ×7 dots	1/16	Cannot display 2 lines with 5 ×10 dot character font.

* (Don't care)

(7) Set CG RAM Address

	RS	R/W	DB7							DB0
Code	0	0	0	1	A	A	A	A	A	A

←Higher Order Bits Lower Order Bits→

Sets the CG RAM address into the address counter in binary AAAAAA. Data is then written or read from the MPU for the CG RAM.

(8) Set DD RAM Address

	RS	R/W	DB7							DB0
Code	0	0	1	A	A	A	A	A	A	A

←Higher Order Bits Lower Order Bits→

Sets the DD RAM address into the address counter in binary AAAAAAA. Data is then written or read from the MPU for the DD RAM.
However, when N=0 (1-line display), AAAAAAA is "00" ~ "4F" (hexadecimal).
when N=1 (2-line display), AAAAAAA is "00" ~ "27" (hexadecimal) for the first line, and "40" ~ "67" (hexadecimal) for the second line.

(9) Read Busy Flag and Address

	RS	R/W	DB7							DB0
Code	0	1	BF	A	A	A	A	A	A	A

←Higher Order Bits Lower Order Bits→

Reads the busy flag (BF) that indicates the system is now internally operating by a previously received instruction. BF=1 indicates that internal operation is in progress. The next instruction will not be accepted until BF is set to "0". Check the BF status before the next wire operation.

At the same time, the value of the address counter expressed in binary AAAAAAA is read out. The address counter is used by both CG and DD RAM addresses, and its value is determined by the previous instruction. Address contents are the same as in Items (7) and (8).

(10) Write Data to CG or DD RAM

	RS	R/W	DH7							DB_0
Code	1	0	D	D	D	D	D	D	D	D

←Higher Order Bits

Lower Order Bits→

Writes binary 8 bit data DDDDDDDD to the CG or the DD RAM.

Whether the CG or DD RAM is to be written into is determined by the previous specification of CG RAM or DD RAM address setting. After write, the address is automatically incremented or decremented by 1 according to entry mode. The entry mode also determines display shift.

(11) Read Data from CG or DD RAM

	RS	R/W	DB_7							DB_0
Code	1	1	D	D	D	D	D	D	D	D

←Higher Order Bits

Lower Order Bits→

Reads binary 8 bit data DDDDDDDD from the CG or DD RAM.

The previous designation determines whether the CG or DD RAM is to be read. Before entering the read instruction, you must execute either the CG RAM or DD RAM address set instruction. If you don't, the first read data will be invalidated. When serially executing the "read" instruction, the next address data is normally read from the second read. The "address set" instruction need not be executed just before the "read" instruction when shifting the cursor by cursor shift instruction (when reading out DD RAM). The cursor shift in struction operation is the same as that of the DD RAM's address set instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed no matter what the entry mode is.

(Note) The address counter (AC) is automatically incremented or decremented by 1 after "write" instructions to either CG RAM or DD RAM. RAM data selected by the AC cannot then be read out even if "read" instructions are executed. The conditions for correct data read out are: execute either the address set instruction or cursor shift instruction (only with DD RAM), just before reading out execute the "read" instruction from the second time the "read" instruction is serial.

■ HOW TO USE THE HD44780

● Interface to MPU

(1) Interface to 8-bit MPU

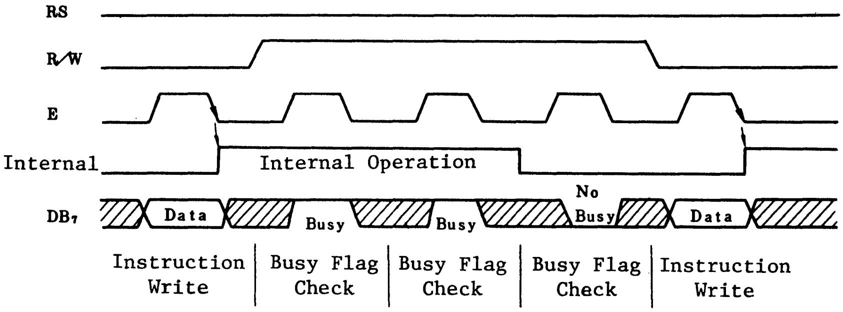
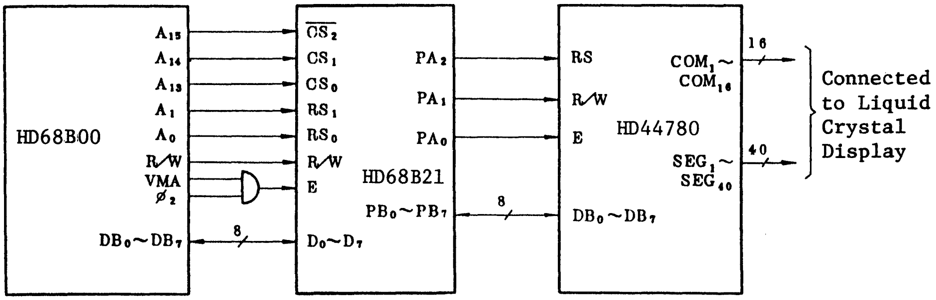


Fig. 5 Example of Busy Flag Check Timing Sequence

① When connecting to 8-bit MPU through PIA

Fig. 6-2 is an example of using a PIA or I/O port (for single chip microcomputer) as an interface device. Input and output of the device is TTL compatible.

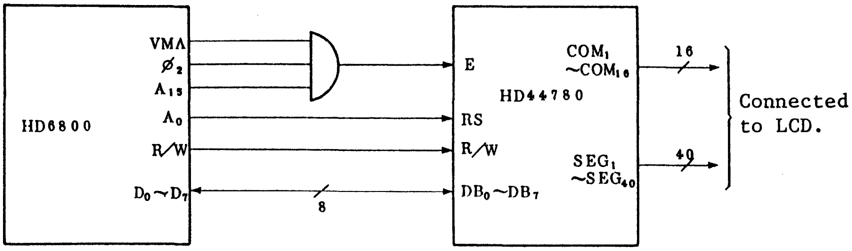
In the example, PB_0 to PB7 are connected to the data buses DB_0 to DB_7 and PA0 to PA2 are connected to E, R/W and RS respectively. Pay attention to the timing relation between E and other signals when reading or writing data and using PIA as an interface.



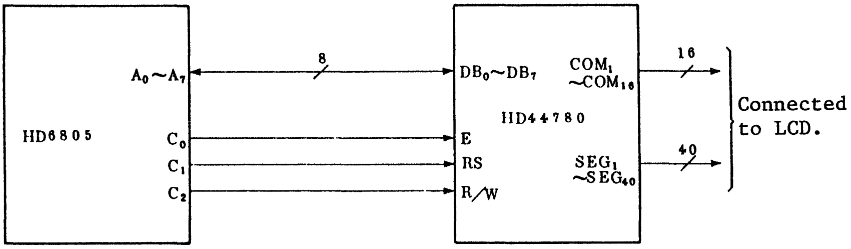
HD68B00: 8 bit CPU

Fig. 6 Example of Interface to HD68B00 Using PIA (HD68B21)

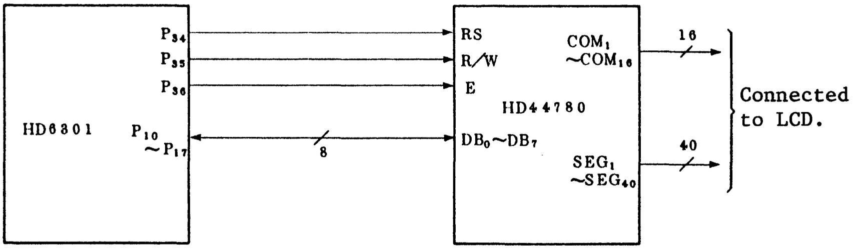
② Connecting directly to the 8-bit MPU bus line



③ Example of interfacing to the HD6805



④ Example of interfacing to the HD6301

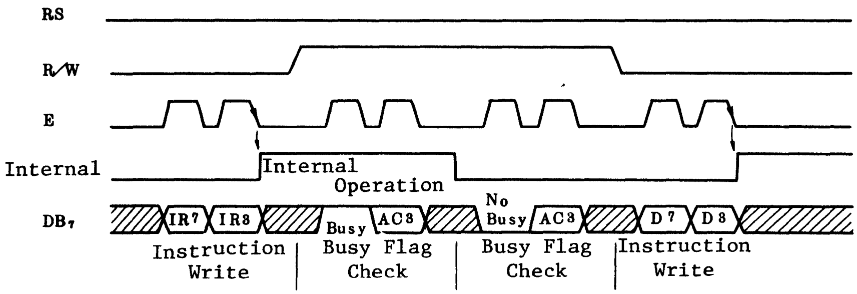


(2) Interface to 4-bit MPU

The HD44780 can be connected to a 4-bit MPU through the 4-bit MPU I/O port. If the I/O port has enough bits, data can be transferred in 8-bit lengths, but if the bits are insufficient, the transfer is made in two operations of 4 bits each (with designation of interface data length for 4 bits). In the latter case, the timing sequence becomes somewhat complex. (See Fig. 7)

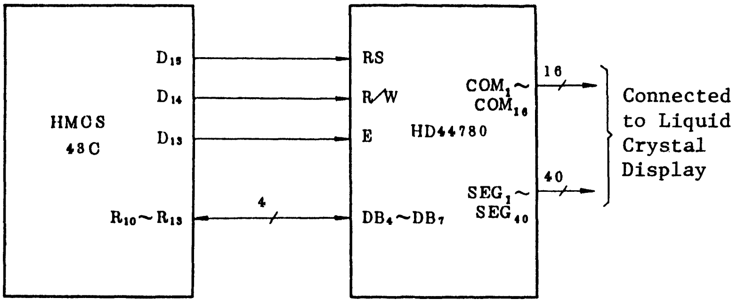
Fig. 8 shows an example of interface to the HMCS43C.

Note that 2 cycles are needed for the busy flag check as well as the data transfer. 4-bit operation is selected by program.



(Note) IR7, IR3: Instruction 7th bit, 3rd bit
AC3 : Address Counter 3rd bit

Fig. 7 An Example of 4-bit Data Transfer Timing Sequence



HMCS43C: Hitachi 4-bit single-chip microcomputer

Fig. 8 Example of Interface to the HMCS43C

Interface to Liquid Crystal Display

(1) Character Font and Number of Lines

The HD44780 can perform 2 types of display, 5 ×7 dots and 5 ×10 dots as character font, with a cursor on each.

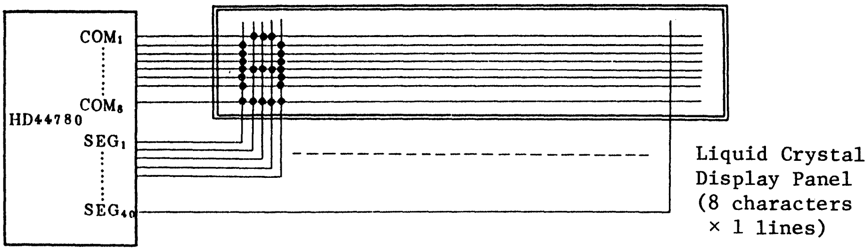
Up to 2 lines are displayed with 5 ×7 dots and 1 line with 5 ×10 dots. Therefore, three types of common signals are available:

Number of Lines	Character Font	Number of Common Signals	Duty Factor
1	5 ×7 dots + Cursor	8	1/8
1	5 ×10 dots + Cursor	11	1/11
2	5 ×7 dots + Cursor	16	1/16

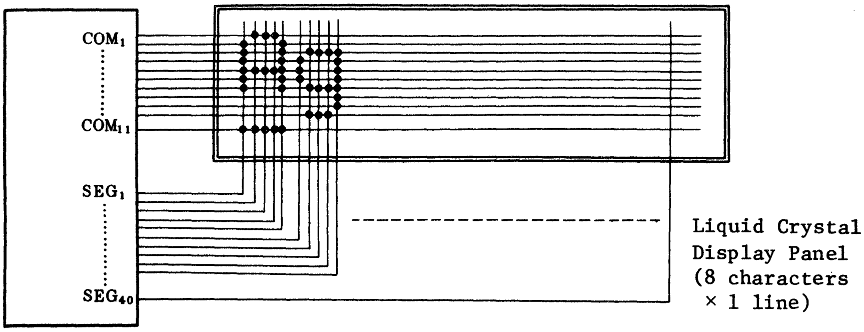
Number of lines and font types can be selected by program. (See to Table 5 Instruction)

(2) Connection to HD44780 and Liquid Crystal Display

Fig. 9 (1) and (2) show connection examples.

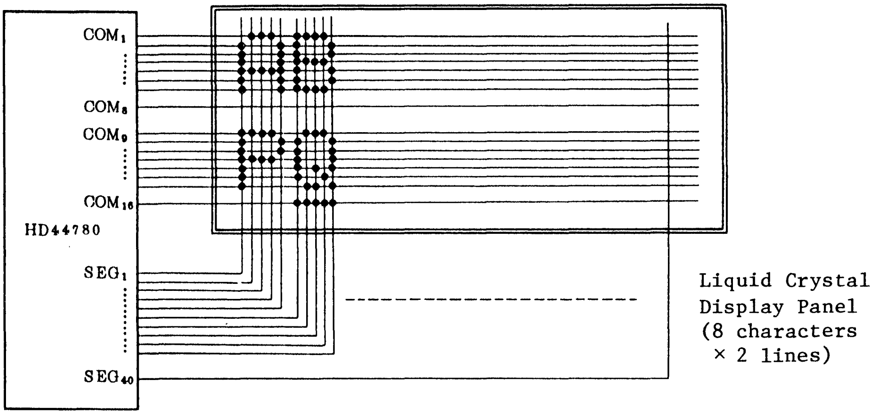


(a) Example of a 5 ×7 dot, 8 character × 1 line Display (1/4 Bias, 1/8 Duty)



(b) Example of a 5 ×10 dot, 8 character × 1 line Display (1/4 Bias, 1/8 Duty)

Fig. 9 (1) Liquid Crystal Display and Connections to HD44780

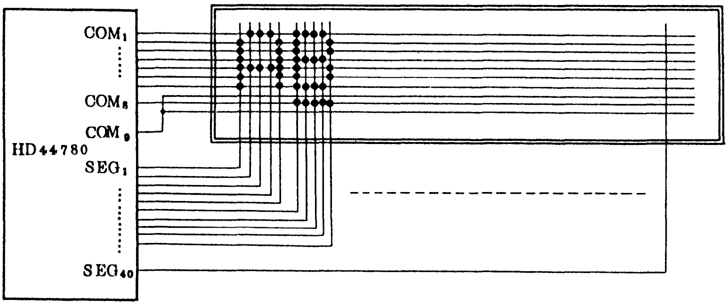


(c) Example of 5 × 7 dot, 8 character × 2 lines Display (1/5 Bias, 1/16 Duty)

Fig. 9 (2) Liquid Crystal Display and Connection to HD44780

Since 5 signal lines at the SEG can display one digit, one HD44780 can display up to 8 digits for 1-line display and 16 digits for 2-line display.

In Fig. 9 examples (a) and (b), there are unused common signal terminals, non-selection waveforms which always output. When the liquid crystal display panel has unused extra scanning lines, avoid undesirable influences due to cross-talk in the floating state by connecting the extra scanning lines to these common signal terminals.

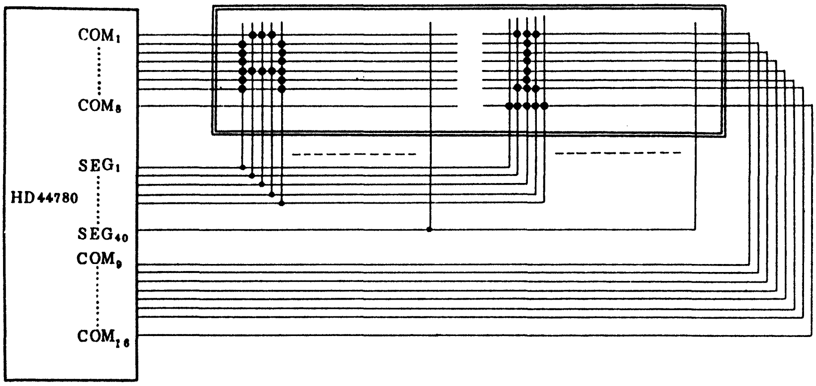


5 × 7 dot, 8 character × 1 line Display (1/4 Bias, 1/8 Duty)

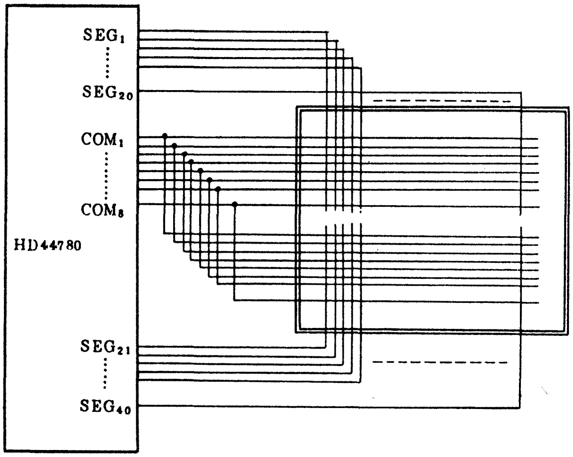
Fig. 10 Using COM9 to Avoid Cross-talk on Unneeded Scanning Line

(3) Connection of Changed Matrix Layout

In the preceding examples, the number of lines was matched to the number of scanning lines. The following display types are possible by changing the matrix layout in the liquid crystal display panel.



(a) 5 × 7 dot, 16 character × 1 line Display
(1/5 Bias, 1/16 Duty)



(b) 5 × 7 dot, 4 character × 2 line Display
(1/4 Bias, 1/8 Duty)

Fig. 11 Changed Matrix Layout Displays

In either case, the only change is the layout. Display characteristics and the number of liquid crystal display characters are dependent on the number of common signals (or duty factor). Note that the display data RAM (DD RAM) addresses for 8 characters × 2 lines and 16 characters × 1 line are the same as shown in Fig. 9.

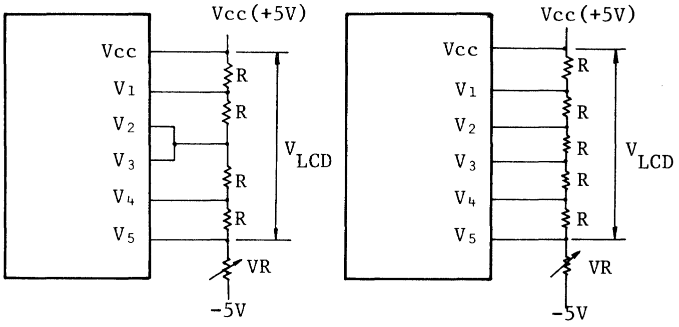
- Power Supply for Liquid Crystal Display Drive

Various voltage levels must be applied to HD44780 terminals V_1 to V_5 to obtain liquid crystal display drive waveforms. The voltages must be changed according to duty factor. Table 6 shows the relation.

Table 6 Duty Factor and Power Supply for Liquid Crystal Display Drive

Duty Factor	$\frac{1}{8}$, $\frac{1}{11}$	$\frac{1}{16}$
Power Supply \ Bias	$\frac{1}{4}$	$\frac{1}{5}$
V_1	$V_{CC} - \frac{1}{4}V_{LCD}$	$V_{CC} - \frac{1}{5}V_{LCD}$
V_2	$V_{CC} - \frac{1}{2}V_{LCD}$	$V_{CC} - \frac{2}{5}V_{LCD}$
V_3	$V_{CC} - \frac{1}{2}V_{LCD}$	$V_{CC} - \frac{3}{5}V_{LCD}$
V_4	$V_{CC} - \frac{3}{4}V_{LCD}$	$V_{CC} - \frac{4}{5}V_{LCD}$
V_5	$V_{CC} - V_{LCD}$	$V_{CC} - V_{LCD}$

V_{LCD} gives the peak values for liquid crystal display drive waveforms. Resistance dividing provides each voltage as shown in Fig. 13.



(a) 1/4 Bias
(1/8, 1/11 Duty)

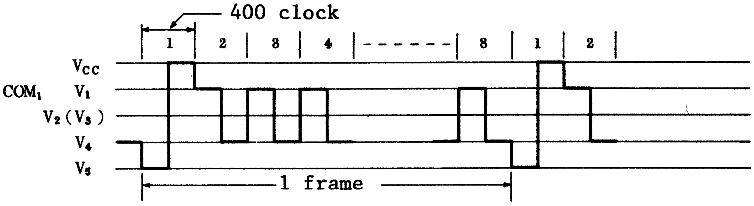
(b) 1/5 Bias
(1/16 Duty)

Fig. 13 Drive Voltage Supply Example

- **Relation between Oscillation Frequency and Liquid Crystal Display Frame Frequency**

The following examples of liquid crystal display frame frequency apply only when oscillation frequency is 250kHz. (1 clock = 4μs)

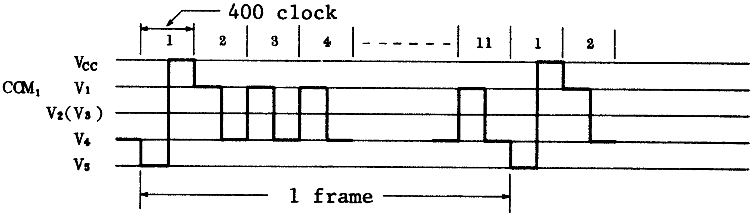
(1) 1/8 Duty



1 frame = 4 (μs) × 400 × 8 = 12800 (μs) = 12.8 (ms)

$$\text{Frame frequency} = \frac{1}{12.8\ (\text{ms})} = 78.1\ (\text{Hz})$$

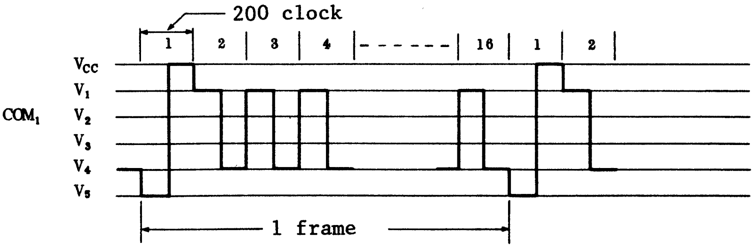
(2) 1/11 Duty



1 frame = 4 (μs) × 400 × 11 = 17600 (μs) = 17.6 (ms)

$$\text{Frame frequency} = \frac{1}{17.6\ (\text{ms})} = 56.8\ (\text{Hz})$$

(3) 1/16 Duty



1 frame = 4 (μs) × 200 × 16 = 12800 (μs) = 12.8 (ms)

$$\text{Frame frequency} = \frac{1}{12.8\ (\text{ms})} = 78.1\ (\text{Hz})$$

- **Connection with Driver LSI HD44100H**

You can increase the number of display digits by externally connecting a liquid crystal display driver LSI HD44100H to the HD44780.

When connected to the HD44780, the HD44100H is used as segment signal driver. The HD44100H can be connected to the HD44780 directly since it supplies CL_1, CL_2, M and D signals and power for liquid crystal display drive. Fig. 14 shows a connection example.

Caution: Connection of voltage supply terminals V_1 through V_6 for liquid crystal display drive is complicated.

Up to 9 units of the HD44100H can be connected for 1-line display (duty factor 1/8 or 1/11) and up to 4 units for the 2-line display (duty factor 1/16). RAM size limits the HD44780 to a maximum of 80 character display digits. The connection method in Fig. 14 remains unchanged for both 1-line and 2-line display or both 5 × 7 and 5 × 10 dot character fonts.

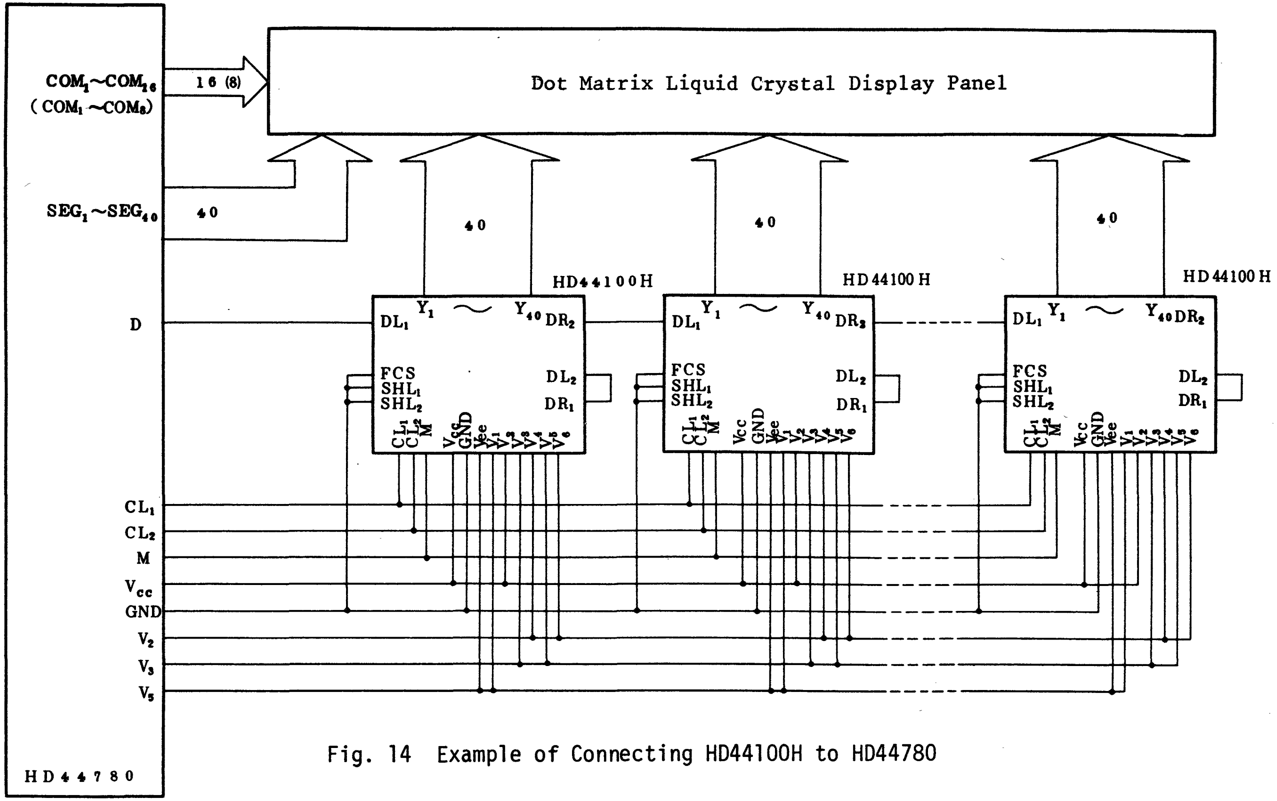


Fig. 14 Example of Connecting HD44100H to HD44780

- Instruction and Display Correspondence

(1) 8-bit operation, 8-digit × 1-line display (using internal reset)

Table 7 shows an example of 8-bit × 1-line display in 8-bit operation.

The HD44780 functions must be set by Function Set prior to display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for displays like the lightening board when combined with display shift operation.

Since the display shift operation changes display position only and DD RAM contents remain unchanged, display data entered first can be output when the return home operation is performed.

(2) 4-bit operation, 8-digit × 1-line display (using internal reset)

The program must set functions prior to 4-bit operation. Table 8 shows an example. When power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since nothing is connected to $DB_0 \sim DB_3$, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is needed as a function (see Table 8).

Thus, $DB_4 \sim DB_7$ of the function set is written twice.

(3) 8-bit operation, 8-digit × 2-line display

For 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the 1st line has been written. Thus, if there are only 8 characters in the first line, the DD RAM address must again be set after the 8th character is completed. (See Table 9) Note that the first and second lines of the display shift are performed. In the example, the display shift is performed when the cursor is on the second line. However, if shift operation is performed when the cursor is on the first line, both the first and second lines move together. When you repeat the shift, the display of the second line will not move to the first line, the same display will only move within each line many times.

(Note) When using the internal reset, the conditions in "Power Supply Condition Using Internal Reset Circuit" must be satisfied. If not, the HD44780 must be initialized by instruction. (See "Initializing by Instruction")

Table 7 8-bit Operation, 8-digit 1-line Display Example(Using Internal Reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 ——— DB_0 0 0 0 0 1 1 0 0 * *		Sets to 8-bit operation and selects 1-line display lines and character font. (Number of display lines and character fonts cannot be changed hereafter.)
3	Display ON/OFF Control 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Write "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HI_	Writes "I".
7	⋮	⋮	
8	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
9	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI_	Sets mode for display shift at the time of write.
10	Write Data to CG RAM/DD RAM 1 0 0 0 1 0 0 0 0 0	ITACHI _	Writes "Space".
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	TACHI M_	Writes "M".
12	⋮	⋮	

13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	MICROKO_	Writes "0".
14	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
15	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
16	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 0 0 1 1	ICROCO	Writes "C" (correction). The display moves to the left.
17	Cursor or Display Shift 0 0 0 0 0 1 1 1 * *	MICROCO	Shifts the display and cursor position to the right.
18	Cursor or Display Shift 0 0 0 0 0 1 0 1 * *	MICROCO_	Shifts display and cursor position to the right.
19	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ICROCOM_	Writes "M".
20	⋮	⋮	
21	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI	Returns both display and cursor to the original position (Address 0).

Table 8 4-bit Operation, 8-digit 1-line Display Example
(Using Internal Reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB7 ~ DB4 0 0 0 0 1 0		Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
3	Function Set 0 0 0 0 1 0 0 0 0 0 * *		Sets 4-bit operation and selects 1-line display and 5×7 dot character font. 4-bit operation starts from this point on and resetting is needed. (Number of display lines and character fonts cannot be changed hereafter.)
4	Display ON/OFF Control 0 0 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
5	Entry Mode Set 0 0 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 1 0 0 0	H_	Writes "H". The cursor is incremented by one and shifts to the right.

Hereafter, control is the same as 8-bit operation.

Table 9 8 bit Operation, 8-digit × 2 line Display Example (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is intialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB7 DB0 0 0 0 0 1 1 1 0 * *		Sets to 8-bit operation and selects 2-line display and 5×7 dot character font.
3	Display ON/OFF Control 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. All display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Writes "H". The DD RAM has has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	⋮	⋮	
7	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
8	Set DD RAM Address 0 0 1 1 0 0 0 0 0 0	HITACHI _	Sets RAM address so that the cursor is positioned at the head of the 2nd line.
9	Write Data co CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	HITACHI M_	Writes "M".
10	⋮	⋮	
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	HITACHI MICROCO_	Writes "O".
12	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI MICROCO_	Sets mode for display shift at the time of write.

13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ITACHI ICROCOM_	Writes "M". Display is shifted to the right. The first and second lines' shift are operated at the same time.
14	⋮	⋮	
15	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI MICROCOM	Returns both display and cursor to the original position (Address 0).

MODIFYING CHARACTER PATTERNS

(1) Character Pattern Development Procedure

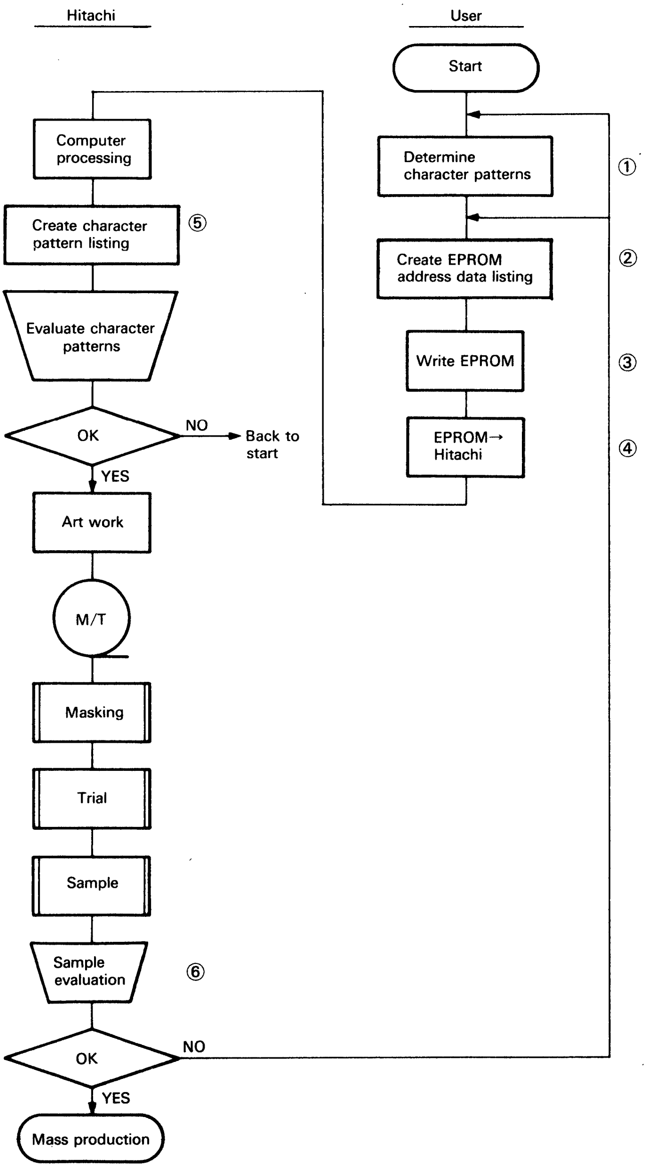


Fig. 15 Character Pattern Development Procedure

The numbers in the above figure correspond to the following operations:

(1) Determine the correspondence between character codes and character patterns.

(2) Create a listing indicating the correspondence between EPROM addresses and data.

(3) Program character patterns in the EPROM.

(4) Send the EPROM to Hitachi.

(5) Hitachi performs computer processing with the EPROM to create a character pattern listing and sends it to the user.

(6) If there is no problem in the character pattern listing, Hitachi creates LSI for trial and sends samples to the user. The user evaluates the samples. When it is confirmed that character patterns are correctly written, mass production of LSI is started.

2. Programming Character Patterns

This section explains the correspondence between addresses and data used to program character patterns in EPROM. The LCD-II character generator ROM can generate 160 5 × 7-dot character patterns and 32 5 × 10-dot character patterns in total of 192 different character patterns.

2.1 5 × 7-dot Character Pattern

For a 5 × 7-dot character pattern, EPROM address data and character pattern correspond with each other as shown below. Table 10 Example of correspondence between EPROM address data and character pattern (5 × 7 dots).

Table 10 Example of Correspondence between EPROM Address Data and Character Pattern (5 x 7 dots)

EPROM address											Data				
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	(LSB) O_0
0	1	0	1	0	0	1	0	0	0	0	1	1	1	1	0
								0	0	1	1	0	0	0	1
								0	1	0	1	0	0	0	1
								0	1	1	1	1	1	1	0
								1	0	0	1	0	1	0	0
								1	0	1	1	0	0	1	0
								1	1	0	1	0	0	0	1
								1	1	1	0	0	0	0	0
Character code								Line position							

Fill line 8 (cursor position) with 0.

(1) EPROM addresses A_{10} to A_3 correspond to a character code.

(2) EPROM addresses A_2 to A_0 specify a line position of character pattern.

(3) EPROM data O_4 to O_0 correspond to character pattern data.

(4) A lit display position (black) corresponds to "1".

(5) Fill line 8 (cursor position) of character pattern with 0.

(6) EPROM data O_5 to O_7 are not used.

2.2 5 × 10-dot Character Pattern

For a 5 × 10-dot character pattern, EPROM address data and character pattern correspond with each other as shown below.

Table 11 Example of Correspondence between EPROM Address Data and Character Pattern (5 x 10 dots)

EPROM address											Data				
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	O_0 (LSB)
1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0
								0	0	1	0	0	0	0	0
								0	1	0	0	1	1	0	1
								0	1	1	1	0	0	1	1
								1	0	0	1	0	0	0	1
								1	0	1	1	0	0	0	1
								1	1	0	0	1	1	1	1
								1	1	1	0	0	0	0	1
1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0

Fill line 11 (cursor position) with 0.

Character code　Line position

(1) EPROM addresses A_{10} to A_3 correspond to a character code. Set A_8 and A_9 of character pattern line 9 and later lines to 0.

(2) EPROM addresses A_2 to A_0 specify a line position of character pattern.

(3) EPROM data O_4 to O_0 correspond to character pattern data.

(4) A lit display position (black) corresponds to "1".

(5) Fill line 11 (cursor position) of character pattern with 0.

(6) EPROM data O_5 to O_7 are not used.

2.3 Handling Unused Character Patterns

(1) EPROM data outside the character pattern area

It is ignored by the character generator ROM for display operation so that it can be 0 or 1.

(2) EPROM data in CG RAM area

It is ignored by the character generator ROM for display operation so that it can be 0 or 1.

(3) EPROM data used when the user does not use any LCD-II character pattern

It is handled in one of the two ways explained below.
Select one of the two ways according to the user application.

1) When unused character patterns are not programed
   If an unused character code is written in the LCD-II DD RAM, all dots are lit. No programming for a character pattern is equivalent to all bits lit. (This is because EPROM is filled with 1 when the EPROM is erased.)

2) Program 0 for unused character patterns
   Nothing is displayed even if unused character codes are written in LCD-II DD RAM. (It is equivalent to space.)

HD66780 (LCD-IIA) (Dot Matrix Liquid Crystal Display Controller and Driver)

Description

The LCD-IIA (HD66780)is a dot matrix liquid crystal display controller and driver LSI that displays alphanumerics, kana characters, and symbols. It drives a dot matrix liquid crystal display under 4-bit or 8-bit microcontroller or microprocessor control. All the functions required for driving a dot matrix liquid crystal display are internally provided on one chip.

Designers can complete dot matrix liquid crystal display systems with fewer chips by using the LCD-IIA (HD66780). If a driver LSI (HD44100H or HD66100F) is connected to the HD66780, up to 80 characters can be displayed.

The LCD-IIA is produced by the CMOS process. Therefore, the combination of the LCD-IIA with a CMOS microcontroller or microprocessor can complete a portable battery-driven device with low power dissipation.

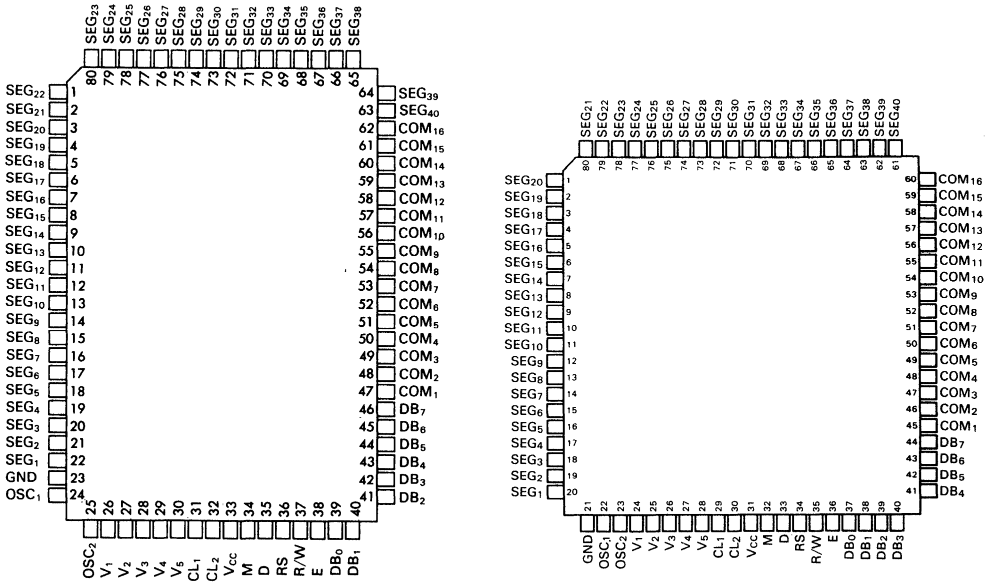
Features

- 5 × 7 and 5 × 10 dot matrix liquid crystal display controller driver
- Can interface to 4-bit or 8-bit MPU
- Display data RAM : 80 × 8 bits (80 characters, max)
- Character generator ROM : 12000 bits ; Character font 5×10 dots : 240 characters
- Character generator RAM : 64 × 8 bits ; Character font 5×8 dots : 8 characters or character font 5 × 11 dots : 4 characters
- Both display data and character generator RAMs can be read from the MPU.
- Internal liquid crystal display driver
  - −16 common signal drivers
  - −40 segment signal drivers (Can be externally extended to 360 segments by liquid crystal display driver HD44100H or HD66100F)
- Duty factor selection (selectable by program).
  - −1/8 duty: 1 line of 5 × 7 dots + cursor
  - −1/11 duty: 1 line of 5 × 10 dots + cursor
  - −1/16 duty: 2 lines of 5 × 7 dots + cursor
- Maximum number of display characters as shown in table 1
- Wide range of instruction functions : Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
- Internal automatic reset circuit at power on (internal reset circuit)
- Internal oscillation circuit
  - −External resistor or ceramic filter
  - −External clock operation possible
- CMOS process
- Single +5V logic power supply (excluding power for liquid crystal display drive)
- Operation temperature range : -20°C to +75°C (-40°C to +85°C device available upon request)
- 80-pin plastic flat package (FP-80, FP-80A)
- Low power consumption

Ordering Information

Type No.	Package
HD66780FS	80-pin plastic QFP (FP-80B)
HD66780FH	80-pin plastic QFP (FP-80A)

Pin Arrangement



(FP-80B)

(FP-80A)

(Top-View)

Pin Description

Signal	No. of Lines	I/O	Connected to	Function
RS	1	Input	MPU	Selects register
R/W	1	Input	MPU	Selects read or write
E	1	Input	MPU	Starts data read or write
DB_7-DB_0	8	I/O	MPU	Bidirectional data bus
CL_1	1	Output	Driver LSI	Serial data latch clock
CL_2	1	Output	Driver LSI	Serial data shift clock
M	1	Output	Driver LSI	LCD waveform AC switch signal
D	1	Output	Driver LSI	Character pattern data
COM_1-COM_{16}	16	Output	LCD	Common signals
SEG_1-SEG_{40}	40	Output	LCD	Segment signals
V_1-V_5	5		Power supply	LCD drive voltages
V_{CC},GND	2		Power supply	+5V and ground
OSC_1-OSC_2	2			System clock

Pin Function

RS (Register Select)

RS selects the register that the MPU is accessing. RS=0 selects the instruction register for MPU writes, and the busy flag and address counter for reads. RS=1 selects the data register for MPU reads and writes.

R/W (Read/Write)

R/W selects whether the MPU will read from (R/W=1) or write to (R/W=0) the LCD-IIA.

E (Enable)

The MPU sets the E input high to signal the start of the read/write operation.

DB_7-DB_0 (Data Bus)

The bidirectional, three-state data bus, DB_0-DB_7, transfers data between the MPU and the LCD-IIA. DB_7 can be used as the busy flag. The lower-order four lines, DB_0-DB_4, are not used in four-bit interface operation.

CL_1, CL_2 (Clock 1, Clock 2)

The CL_1 output signals the HD44100H or HD 66100F driver LSI to latch the serial data sent on line D. The CL_2 output signals it to shift the data.

M (Master AC Signal)

The HD44100H or HD66100F driver LSIs use the M output to convert the LCD drive waveform to AC.

D (Serial Data)

The LCD-IIA outputs serial character pattern data corresponding to the common signals to the HD44100H or HD66100F driver LSIs on D.

COM_1-COM_{16} (Common)

COM_1-COM_{16} are the LCD common lines. Common signals that are not used are deselected. At 1/8 duty factor COM_9-COM_{16} are not used, so they output non-selected waveforms. At 1/11 duty factor COM_{12}-COM_{16} are not used, so they output non-selected waveforms.

SEG_1-SEG_{40} (Segment)

SEG_1-SEG_{40} are the LCD segment lines.

V_1-V_5 (LCD Voltages)

The LCD-IIA requires the V_1-V_5 voltages to output LCD-driving waveforms.

V_{CC}, GND (Power Supply, Ground)

V_{CC} is the LCD-IIA's logic power supply. GND is the power supply ground.

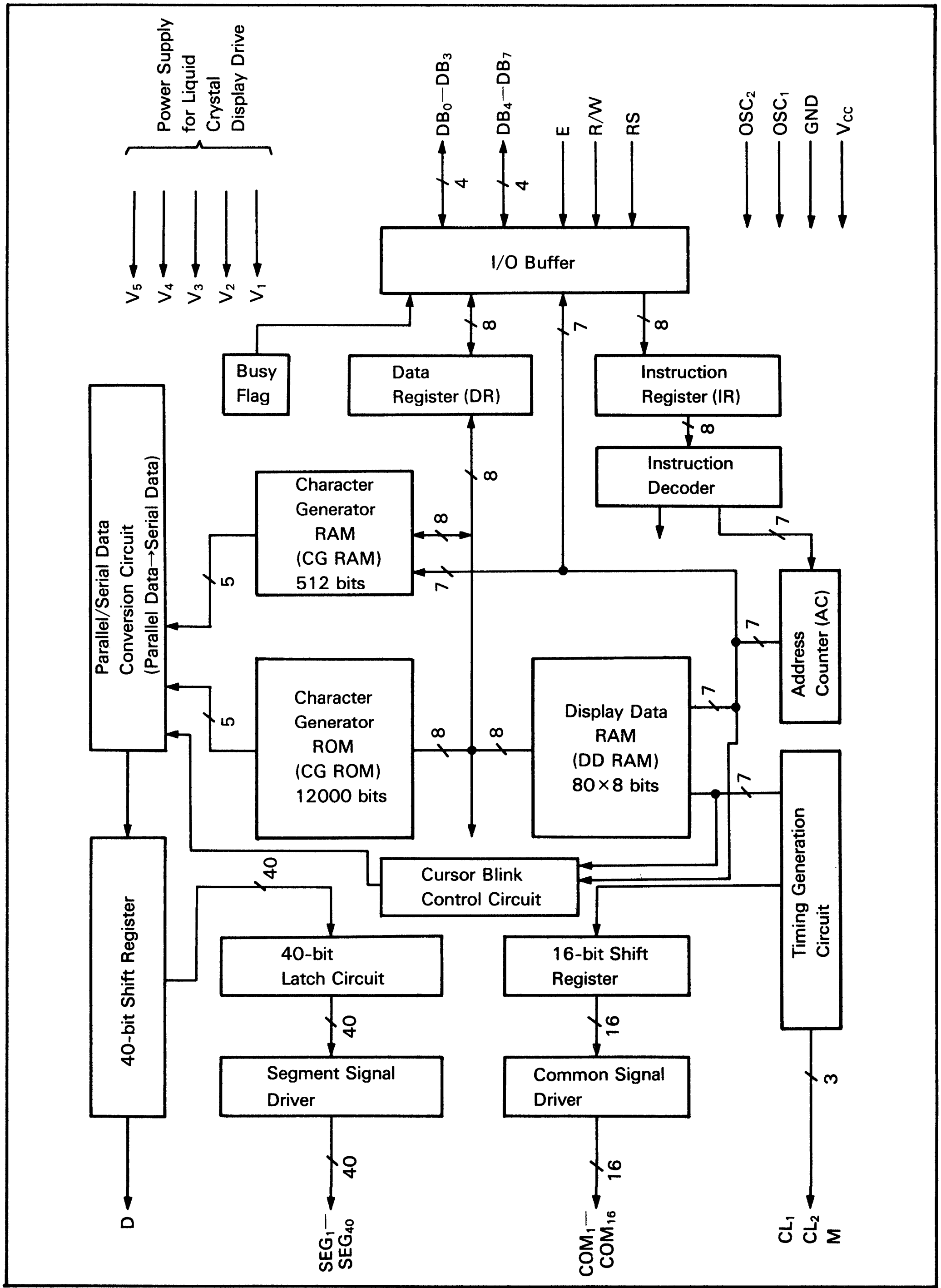
OSC_1, OSC_2 (Oscillator 1, Oscillator 2)

OSC_1 and OSC_2 are the connections for the LCD-IIA system clock. The LCD-IIA can use its internal oscillator if OSC_1 and OSC_2 are connected to a resistor or ceramic filter. An external clock can be input to OSC_1.

Table 1. Number of Display Characters

No. of Display Lines	Duty factor	Extension	HD44100H	HD66100F	No. of Display Characters
1-line display	1/8, 1/11 duty	Not provided	–	–	8 characters × 1 line
		Proveded	9 pcs. (8 characters/pc.)	5 pcs. (16 characters/pc.)	80 characters × 1 line
2-line display	1/16 duty	Not provided	–	–	8 characters × 2 lines
		Provided	4 pcs. (8 characters × 2 lines/pc.)	2 pcs. (16 characters × 2 lines/pc.)	40 characters × 2 lines

HD66780 Block Diagram


Power Supply for Liquid Crystal Display Drive
V5
V4
V3
V2
V1
DB0—DB3
4
DB4—DB7
4
E
R/W
RS
OSC2
OSC1
GND
VCC
I/O Buffer
8
7
8
Busy Flag
Data Register (DR)
Instruction Register (IR)
8
Instruction Decoder
7
8
Character Generator RAM (CG RAM) 512 bits
8
7
5
Parallel/Serial Data Conversion Circuit (Parallel Data→Serial Data)
Address Counter (AC)
7
Character Generator ROM (CG ROM) 12000 bits
5
8
8
Display Data RAM (DD RAM) 80×8 bits
7
7
Timing Generation Circuit
Cursor Blink Control Circuit
40
40-bit Shift Register
40-bit Latch Circuit
16-bit Shift Register
40
16
Segment Signal Driver
Common Signal Driver
3
40
16
D
SEG1—SEG40
COM1—COM16
CL1
CL2
M

Block Function

Registers

The HD66780 has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes such as display clear and cursor shift, and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can be written from the MPU but not read by the MPU.

The DR temporarily stores data to be written into the DD RAM or the CG RAM and data to be read out from DD RAM or CG RAM. Data written into the DR from the MPU is automatically written into the DD RAM or the CG RAM internally. The MPU also uses the DR for data storage when reading data from the DD RAM or the CG RAM. When the MPU writes address information into the IR, the LCD-IIA sends data to the DR from the DD RAM or the CG RAM by internal operation. Data transfer to the MPU is then completed by the MPU reading DR. After the MPU reads the DR, the LCD-IIA sends data in the DD RAM or CG RAM at the next address to the DR for the next read from the MPU. Register selector (RS) signals select these two registers (table 2).

Busy Flag (BF)

When the busy flag is 1, the HD66780 is in the internal operation mode, and instructions will not be accepted. As table 2 shows, the busy flag is output to DB_7 when RS=0 and R/W=1. The next instruction must be written after confirming that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to DD and CG RAM. When an instruction for address is written in IR, the address information is sent from IR to AC. Selection of either DD or CG RAM is also determined concurrently by the instruction.
After writing into (or reading from) DD or CG RAM display data, AC is automatically incremented by 1
(or decremented by 1). AC contents are output to DB_0-DB_6 when RS=0 and R/W=1, as shown in table 2.

Display Data RAM (DD RAM)

The display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 80 × 8 bits, or 80 characters. The display data RAM (DD RAM) that is not used for display can be used as general data RAM. Relations between DD RAM addresses and positions on the liquid crystal display are shown in figure 1.
The DD RAM adress (A_{DD}) is set in the address counter (AC) and is represented in hexadecimal.

When there are fewer then 80 display characters, the display begins at the head positon. For example, 8 characters using an HD66780 are displayed as shown in figure 2.

When the display shift operation is performed, the DD RAM address moves as shown in figure 3.

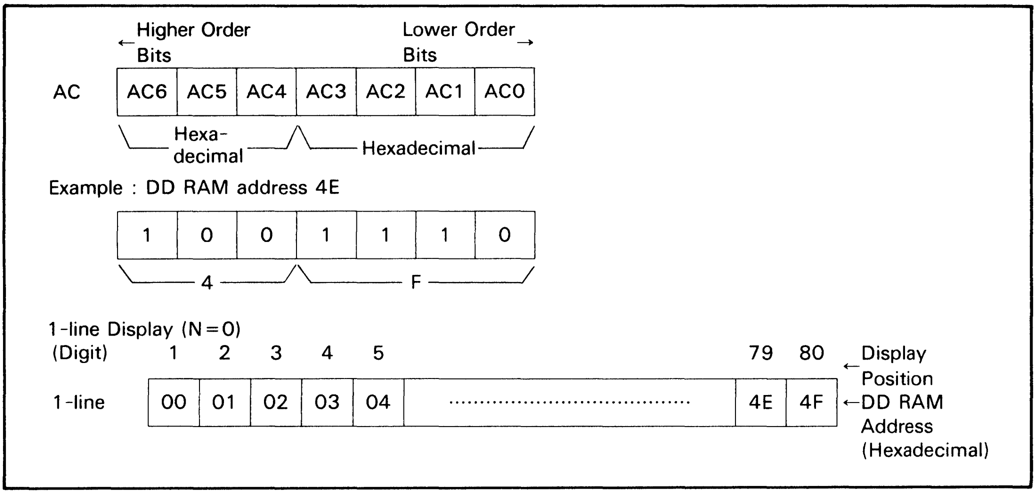
A 16-character display using an HD66780 and an HD44100H is shown in figure 4.

The relation between display position and DD RAM address when the number of display digits is increased through the use of one HD66780 and two or more HD44100Hs can be considered an extension of figure 4.

Since the increase can be 8 digits for each additional HD44100H, up to 80 digits can be

Table 2. Register Selection

RS	R/W	Operation
0	0	IR write as internal operation (Display clear, etc)
0	1	Read busy flag (DB_7) and address counter (DB_0-DB_6)
1	0	DR write as internal operation (DR to DD or CG RAM)
1	1	DR read as internal operation (DD or CG RAM to DR)



AC	AC6	AC5	AC4	AC3	AC2	AC1	AC0

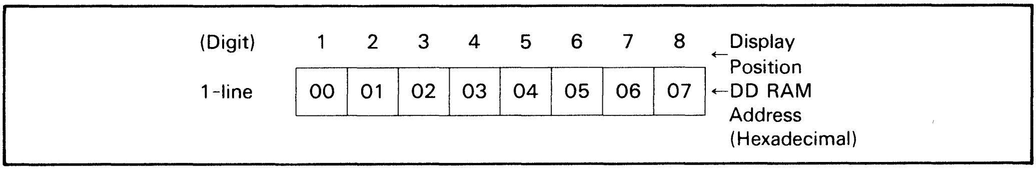
Example : DD RAM address 4E

1	0	0	1	1	1	0

1-line Display (N=0)

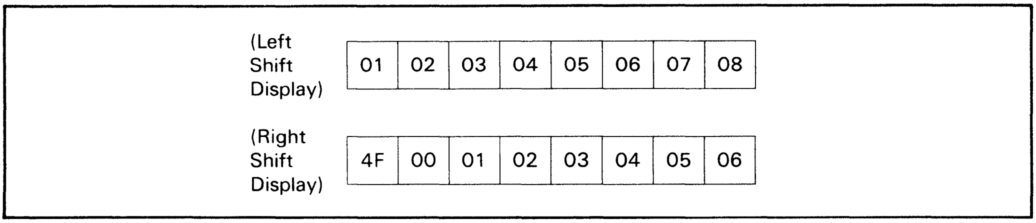
(Digit)	1	2	3	4	5		79	80
1-line	00	01	02	03	04	....	4E	4F

Figure 1. DD RAM Address



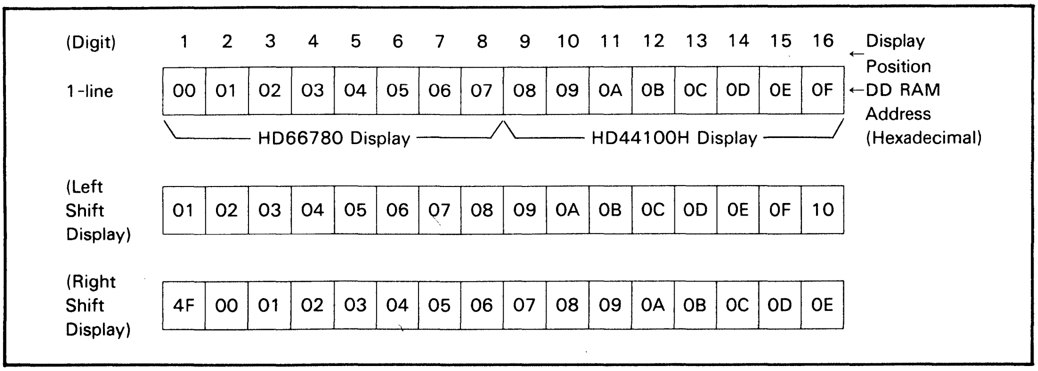
(Digit)	1	2	3	4	5	6	7	8
1-line	00	01	02	03	04	05	06	07

Figure 2. Eight-Character Display Example



(Left Shift Display)	01	02	03	04	05	06	07	08
(Right Shift Display)	4F	00	01	02	03	04	05	06

Figure 3. Display shift



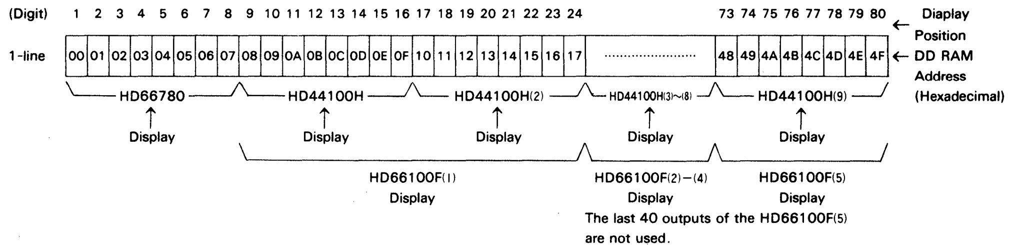
(Digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
(Left Shift Display)	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
(Right Shift Display)	4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E

Figure 4. Sixteen-Character Display Example

displayed by externally connecting 9 HD44100Hs.
The same holds when HD66100Fs are used as display drivers. Consisting of 80 outputs, one HD66100F can display 16 digits (figure 5).

When the number of display characters is fewer than 40×2 lines, the 2 lines from the head are displayed. Note that the first line end address and the second line start address are not consecutive. For example, when an HD66780 is used, 8 characters × 2 lines are displayed as shown in figure 6.

When display shift is performed, the DD RAM address moves as shown in figure 7.



2-line Display (N=1)

(Digit)	1	2	3	4	5		39	40	← Display Position
1-line	00	01	02	03	04	....	26	27	←DD RAM Address
2-line	40	41	42	43	44	....	66	67	(Hexadecimal)

Figure 5. Extended Display

(Digit)	1	2	3	4	5	6	7	8	← Display Position
1-line	00	01	02	03	04	05	06	07	←DD RAM Address
2-line	40	41	42	43	44	45	46	47	(Hexadecimal)

Figure 6. Two-Line by Eight-Charscter Display Example

(Left Shift Display)								
	01	02	03	04	05	06	07	08
	41	42	43	44	45	46	47	48

(Right Shift Display)								
	27	00	01	02	03	04	05	06
	67	40	41	42	43	44	45	46

Figure 7. Two-Line Display Shift

16 characters × 2 lines are displayed as in figure 8 when an HD66780 and an HD44100H are used.

The relation between diaplay position and DD RAM address when the number of display digits is increased by using one HD66780 and two or more HD44100Hs, can be considered an extension of figure 9.

Since the increase can be 8 digits × 2 lines for each additional HD44100H, up to 40 digits × 2 lines can be displayed by connecting 4 HD66780s (or 2 HD66100Fs) externally.

Character Generator ROM (CG ROM)

The character generator ROM generates 5 × 7 dot or 5 × 10 dot character patterns from 8-bit character codes. A CG ROM has 240 types of 5 × 10 dot character patterns built-in. (Note; In a 5 × 7 dot + cursor display, only the upper part, that is, 5 × 7 dots of 5 × 10 dots, is displayed.)

Table 3 shows the relation between character codes and character patterns in the Hitachi standard HD66780A00. User-defined character patterns are also available by mask-programming ROM.

Character Generator RAM (CG RAM)

With the character generator RAM, the user can rewrite character patterns by program. With 5 × 7 dots, 8 character patterns can be written and with 5 × 10 dots 4 patterns can be written.

Write the character codes in the left columns of table 3 to display character patterns stored in CG RAM.

(Digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display Position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	←DD RAM Address
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	(Hexadecimal)

HD66780 Display (digits 1–8) — HD44100H Display (digits 9–16)

(Left Shift Display)																
	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50

(Right Shift Display)																
	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

Figure 8. Two-Line by Sixteen-Charater Display Example

(Digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		33	34	35	36	37	38	39	40	← Display Position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	…………	20	21	22	23	24	25	26	27	←DD RAM address
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	…………	60	61	62	63	64	65	66	67	(Hexadecimal)

HD667780 Display — HD44100H(1) Display — HD44100H(2)(3) Display — HD44100H(4) Display

HD66100F(1) Display — HD66100F(2) Display

Figure 9. Two-Line Extended Display Example

Table 3. Correspondence between Character Codes and Character Pattern (Hitachi Standard HD66780A00)

Higher 4Bits Lower 4Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG＊ RAM (1)			0	@	P	`	p				ー	タ	ミ	α	p
xxxx0001	(2)		!	1	A	Q	a	q			。	ア	チ	ム	ä	q
xxxx0010	(3)		"	2	B	R	b	r			「	イ	ツ	メ	β	θ
xxxx0011	(4)		#	3	C	S	c	s			」	ウ	テ	モ	ε	∞
xxxx0100	(5)		$	4	D	T	d	t			、	エ	ト	ヤ	μ	Ω
xxxx0101	(6)		%	5	E	U	e	u			・	オ	ナ	ユ	σ	ü
xxxx0110	(7)		&	6	F	V	f	v			ヲ	カ	ニ	ヨ	ρ	Σ
xxxx0111	(8)		'	7	G	W	g	w			ァ	キ	ヌ	ラ	g	π
xxxx1000	(1)		(	8	H	X	h	x			ィ	ク	ネ	リ	√	x̄
xxxx1001	(2)		)	9	I	Y	i	y			ゥ	ケ	ノ	ル	⁻¹	y
xxxx1010	(3)		*	:	J	Z	j	z			ェ	コ	ハ	レ	j	千
xxxx1011	(4)		+	;	K	[	k	{			ォ	サ	ヒ	ロ	ˣ	万
xxxx1100	(5)		,	<	L	¥	l	|			ャ	シ	フ	ワ	¢	円
xxxx1101	(6)		-	=	M	]	m	}			ュ	ス	ヘ	ン	£	÷
xxxx1110	(7)		.	>	N	^	n	→			ョ	セ	ホ	゛	ñ	
xxxx1111	(8)		/	?	O	_	o	←			ッ	ソ	マ	゜	ö	█

Note: ＊ The user can specify any pattern for character-generator ROM.

Table 4 shows the relation between CG RAM addresses and data and display patterns.

As table 4 shows, an area that is not used for display can be used as general data RAM.

Table 4. Relation between CG RAM Address and Character Codes (DD RAM) and Character Patterns (CG RAM Data) (Cont)

For 5 × 7-dot character patterns

Character Codes (DD RAM Data)	CG RAM Address	Character Patterns (CG RAM Data)	
7 6 5 4 3 2 1 0	5 4 3 2 1 0	7 6 5 4 3 2 1 0	
Higher ←Order Bits / Lower Order → Bits	Higher ←Order Bits / Lower Order → Bits	Higher ←Order Bits / Lower Order → Bits	
0 0 0 0 * 0 0 0	0 0 0 0 0 0	* * * 1 1 1 1 0	
	0 0 1	1 0 0 0 1	
	0 1 0	1 0 0 0 1	Character Pattern Example (1)
	0 1 1	1 1 1 1 0	
	1 0 0	1 0 1 0 0	
	1 0 1	1 0 0 1 0	
	1 1 0	1 0 0 0 1	Cursor
	1 1 1	* * * 0 0 0 0 0	←Position
0 0 0 0 * 0 0 1	0 0 1 0 0 0	* * * 1 0 0 0 1	
	0 0 1	0 1 0 1 0	
	0 1 0	1 1 1 1 1	Character Pattern Example (2)
	0 1 0	0 0 1 0 0	
	1 0 0	1 1 1 1 1	
	1 0 1	0 0 1 0 0	
	1 1 0	0 0 1 0 0	
	1 1 1	* * * 0 0 0 0 0	
0 0 0 0 * 1 1 1	1 1 1 0 0 0	* * *	
	0 0 1		
	1 0 0		
	1 0 1		*No effect (Don't Care)
	1 1 0		
	1 1 1	* * *	

Notes: 1. Character code bits 0-2 correspond to CG RAM address bits 3-5 (3 bits: 8 types).

2. CG RAM address bits 0-2 designate character pattern line position. The 8th line is the cursor position and display is performed by logical OR with the cursor.
Maintain the 8th line data, corresponding to the cursor display position, in the 0 state for cursor display. When the 8th line data is 1, bit 1 lights up regardless of cursor existence.

3. Character pattern row positions correspond to CG RAM data bits 0-4, as shown in the figure (bit 4 being at the left end).
Since CG RAM data bits 5-7 are not used for display, they can be used for the general data RAM.

4. As shown in table 3 and 4, CG RAM character patterns are selected when character code bits 4-7 are all 0. However, since character code bit 3 is ineffective, the R display in the character pattern example, is selected by character code 00 (hexadecimal) or 08 (hexadecimal).

5. 1 for CG RAM data corresponds to selection for display and 0 for non-selection.

For 5 × 10 -dot character patterns

Character Codes (DD RAM Data)		**CG RAM Address**		**Character Patterns (CG RAM Data)**	
7 6 5 4 3 2 1 0 Higher ←Order Bits Lower Order → Bits		5 4 3 2 1 0 Higher ←Order Bits Lower Order → Bits		7 6 5 4 3 2 1 0 Higher ←Order Bits Lower Order → Bits	
0 0 0 0 * 0 0 *		0 0 0 0 0 0		* * * 0 0 0 0 0	
		0 0 0 1		0 0 0 0 0	
		0 0 1 0		1 0 1 1 0	
		0 0 1 1		1 1 0 0 1	Character
		0 1 0 0		1 0 0 0 1	Pattern
		0 1 1 0		1 0 0 0 1	Example
		0 1 1 0		1 1 1 1 0	
		0 1 1 1		1 0 0 0 0	
		1 0 0 0		1 0 0 0 0	
		1 0 0 1		1 0 0 0 0	Cursor
		1 0 1 0		* * * 0 0 0 0 0	←Position
		1 0 1 1		* * * * * * * *	
		1 1 0 0			
		1 1 0 1			
		1 1 1 0			
		1 1 1 1		* * * * * * * *	
0 0 0 0 * 1 1 *		1 1 0 0 0 0		* * *	
		0 0 0 1			
		1 0 0 1			
		1 0 1 0		* * *	
		1 0 1 1		* * * * * * * *	
		1 1 0 0			
		1 1 0 1			
		1 1 1 0			* No effect
		1 1 1 1		* * * * * * * *	(Don't care)

Notes: 1. Character code bits 1, 2 correspond to CG RAM address bits 4, 5 (2 bits: 4 patterns).

2. CG RAM address bits 0-3 designate character pattern line position. The 11th line is the cursor position and display is performed by logical OR with cursor.
Maintain the 11th line data corresponding to the cursor display position in the 0 state for cursor display. When the 11th line data is 1, bit 1 lights up regardless of cursor existence. Since the 12nd-16th lines are not used for display, they can be used for the general data RAM.

3. Character pattern row positions are the same as 5 × 7 dot character pattern positions.

4. CG RAM character patterns are selected when character code bits 4-7 are all 0. However, since character code bit 0 and 3 are ineffective, P display in the character pattern example is selected by character code 00, 01, 08 and 09 (hexadecimal).

5. 1 for CG RAM data corresponds to selection for display and 0 for non-selection.

Timing generation Circuit

The timing generation circuit generates timing signals to operate internal circuits such as DD RAM, CG ROM and CG RAM. RAM read timing needed for display and internal operation timing by MPU access are separately generated so that they may not interfere with each other. Therefore, when writing data to the DD RAM for example, there will be no undesirable influence, such as flickering, in areas other than the display area. This circuit also generates timing signals to operate the externally connected drivers (HD44100H or HD66100F).

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 16 common signal drivers and 40 segment signal drivers. When the character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms. The other common signal drivers continue to output non-selection waveforms.

The segment signal driver has essentially the same configuration as the driver LSI HD44100H. Character pattern data is sent serially through a 40-bit shift register and latched when all needed data has arrived. The latched data controls the driver for generating drive waveform outputs.

The serial data can be sent to HD44100H or HD66100Fs, externally connected in cascade, to diaplay an extended number of characters.

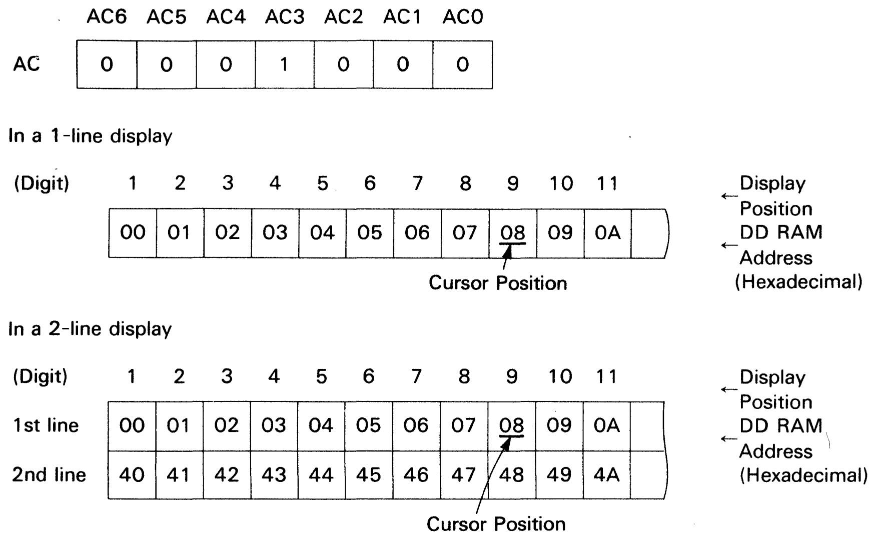
The LCD-IIA always starts sending serial data at the display data character pattern corresponding to the last address of the display data RAM (DD RAM).

Since serial data is latched when the display data character pattern, corresponding to the starting address, enters the internal shift register, the HD66780 drives the head of the display. The rest of the display, corresponding to later addresses, are added with each additional HD44100H or HD66100F.

Cursor/Blink Control Circuit

The cursor/blink control circuit generates the cursor or blinking. The cursor or blinking appear in the digit residing at the display data RAM (DD RAM) address set in the address counter (AC).

When the address counter is $(08)_{16}$, a cursor position is as shown in figure 10.



	AC6	AC5	AC4	AC3	AC2	AC1	AC0
AC	0	0	0	1	0	0	0

In a 1-line display

(Digit)	1	2	3	4	5	6	7	8	9	10	11	
	00	01	02	03	04	05	06	07	08	09	0A	

In a 2-line display

(Digit)	1	2	3	4	5	6	7	8	9	10	11	
1st line	00	01	02	03	04	05	06	07	08	09	0A	
2nd line	40	41	42	43	44	45	46	47	48	49	4A	

(Note) The cursor or blink appears when the address counter (AC) selects the character generator RAM (CG RAM). But the cursor and blink are meaningless.
The cursor or blink is displayed in the meaningless position when AC is the CG RAM address.

Figure 10. Cursor or Blink

MPU Interface

The HD66780 can send data in either 2 4-bit operations or 1 8-bit operation so it can interface to both 4-and 8-bit MPU's.

When interface data is 4 bits long, data is transferred using only 4 bus lines: DB_4-DB_7. DB_0-DB_3 are not used. Data transfer between the HD66780 and the MPU completes when 4-bit data is transferred twice.

Data of the higher order 4 bits (contents of DB_4-DB_7 when interface data is 8 bits long) is transfer-red first, then the lower order 4 bits (contents of DB_0-DB_3 when interface data is 8 bits long) is transferred.

Check the busy flag after 4-bits data has been transferred twice (one instruction). Two 4-bit operations will then transfer the busy flag and address counter data (figure 11).

When interface is 8 bits long, data is transferred using the 8 data bus lines DB_0-DB_7.

Reset Function

Initializing by Internal Reset Circuit

The HD66780 automatically initializes (resets) when power is turned on using the internal reset circuit. The following instructions are executed at initialization. The busy flag (BF) is kept in busy state until initialization ends (BF=1). The busy state lasts 10 ms after V_{CC} rises to 4.5 V.

1. Display clear
2. Function set
   a. DL = 1: 8-bit long interface data
   b. N = 0: 1-line display
   c. F = 0: 5×7-dot character font
3. Display on/off control
   a. D = 0: Display off
   b. C = 0: Cursor off
   c. B = 0: Blink off
4. Entry mode set
   a. I/D = 1: + 1(increment)
   b. S = 0: No shift

Note: When conditions in power supply conditions using internal reset circuit in the electircal characteristics are not met, the internal reset circuit will not operate normally and initialization will not be performed. In this case initialize by MPU according to initializing by instruction.

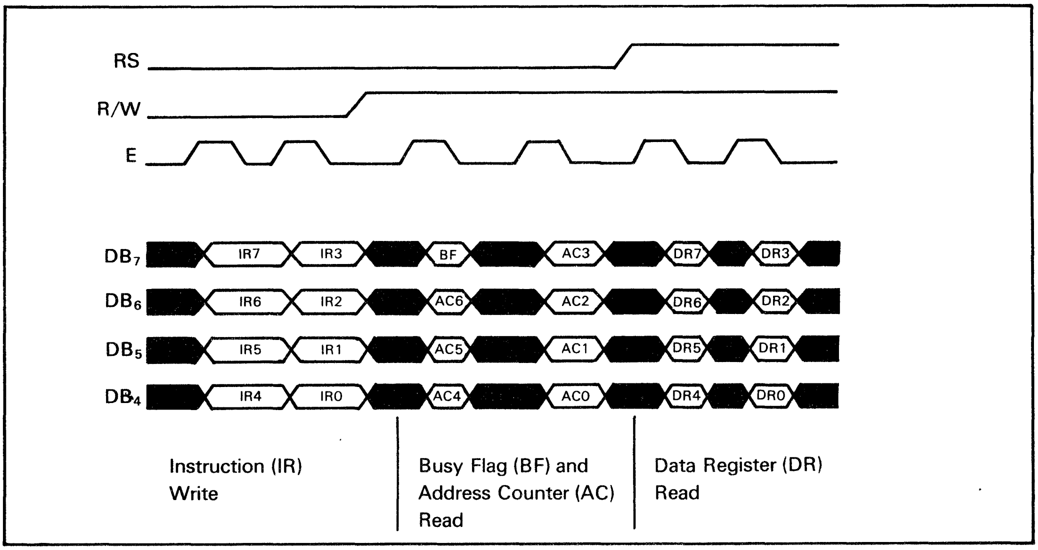


Figure 11. 4-Bits Data Transfer Example

Instructions

Only two HD66780 registers, the instruction register (IR) and the data register (DR) can be directly controlled by the MPU. Prior to internal operation start, control information is temporarily stored in these registers, to allow interface from HD66780 internal operation to various types of MPU's which operate at different speeds or to allow interface to peripheral control IC's. HD66780 internal operation is determined by signals sent from the MPU. These signals include register selection signals (RS), read/write signals (R/W), and data bus signals (DB_0-DB_7), and are here called instructions. Table 5 shows the instructions and their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that:

1. Designate HD66780 functions such as display format, data length, etc
2. Give internal RAM addresses
3. Perform data transfer with internal RAM
4. Others

In normal use, category 3 instructions are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of HD66780 internal RAM addresses after each data write lessens the MPU program load. The display shift especially can be performed concurrently with display data write, enabling the disigner to develop systems in minimum time with maximum programing efficiency. For an explanation of the shift function in its relation to display, see table 7.

During internal operation, no instruction other than the busy flag/address read instruction will be executed. Because the busy flag is set to 1 while an instruction is being executed, check to make sure it is on 0 before sending an instruction from the MPU.

Note: Make sure the HD66780 is not in the busy state (BF = 0) before sending the instruction from the MPU to the HD66780. If the instruction is sent without checking the busy flag, the time between first and next instructions is much longer than the instruction execution time. See table 5 for a list of each instruction's execution time.

Table 5. Instructions

	Code											Execution Time (Max) (fcp or fosc 250 kHz)
Instruction	**RS**	**R/W**	**DB_7**	**DB_6**	**DB_5**	**DB_4**	**DB_3**	**DB_2**	**DB_1**	**DB_0**	**Description**	
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter	1.64 ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in address counter. Also returns display being shifted to original position. DD RAM contents remain unchanged	1.64 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read	40 μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets entire display on/off (D), cursor on/off (C), and blink of cursor position character (B)	40 μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts diaplay without changing DD RAM contents	40 μs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (L) and character font (F)	40 μs
Set CG RAM Address	0	0	0	1	ACG						Sets CG RAM address. CG RAM data is sent and received after this setting.	40 μs
Set DD RAM Address	0	0	1	ADD							Set DD RAM address. DD RAM data is sent and received after this setting.	40 μs
Read Busy Flag & Address	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents	0 μs
Write Data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM	46 μs
Read Data from CG or DD RAM	1	0	Read Data								Reads data from DD RAM or CG RAM	46 μs

Notes: 1

I/D = 1: Increment
I/D = 0: Decrement
S = 1: Accompanies display shift
S = 1: Display shift
S/C = 0: Cursor move

BF = 1: Internally operating
BF = 0: Can accept instruction
DD RAM: Display data RAMA
CG RAM: Character generator RAM

A_{CG}: CG RAM address

R/L = 1: Shift to the right
R/L = 0: Shifts to the left
DL = 1: 8 bits, DL = 0: 4 bits
N = 1: 2 lines, N = 0: 1 line
F = 1: 5×10 dots, F = 0: 5×7 dots

A_{DD} :DD RAM address Corresponds to cursor address
AC : Address counter used for both DD and CG RAM

2. * No effect (Don't care)
3. Execution time changes when freguency changes. Example: When fcp or fosc is 270 kHz:

$$40\,\mu s \times \frac{250}{270} = 37\,\mu s$$

Clear Display

Clear display (figure 12) writes space code 20 (hexadecimal)(character pattern for character code 20 must be blank pattern) into all DD RAM addresses. Sets DD RAM address 0 in address counter. Returns display to its original status if it is shifted. In other words, the display disappears and the cursor or blink goes to the left edge of the display (the first line if 2 lines are displayed). Sets I/D = 1 (increment mode) of entry mode. S of entry mode does not change.

Return Home

Return home (figure 13) sets the DD RAM address 0 in address counter. Returns display to its original status if it was shifted. DD RAM contents do not change. The cursor or blink go to the left of the display (the first line if 2 lines are displayed).

Entry Mode Set

I/D: I/D (figure 14) increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from the DD RAM. The cursor or blink moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S: Shifts the entire display either to the right or to the left when S is 1; to the left when I/D = 1 and to the right when I/D = 0. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM. When writing into or reading out of the CG RAM does not shift. When S = 0, the display does not shift.

Display On/Off Control

D: The display is on when D = 1 and off when D = 0 (figure 15). When off due to D = 0, display data remains in the DD RAM. It can be displayed immediately by setting D = 1.

C: The cursor is displayed when C = 1 and is not displayed when C = 0. Even if the cursor disappears, the function of I/D, etc does not

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	0	1

Figure 12. Clear Display Instruction

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	1	*

* Don't care

Figure 13. Return Home Instruction

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Figure 14. Entry Mode Set Instruction

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	1	D	C	B

Figure 15. Display On/Off Control Instruction

change during display data write. The cursor is displayed using 5 dots in the 8th line when the 5 × 7-dot is selected and 5 dots in the 11th line when the 5 × 10-dot character font is selected (figure 16).

B: The character indicated by the cursor blinks when B = 1. The blink is displayed by switching between all blank dots and display characters at 409.6 ms intervals when fcp or fosc = 250 kHz (figure 15). The cursor and the blink can be set to display simultaneously. (The blink time changes according to the reciprocal of fcp or fosc. For example, $409.6 \times \frac{250}{270} = 379.2$ ms when fcp = 270 kHz.)

Cursor or Display Shift

Cursor or display shift (figure 17) shifts cursor position or display to the right or left without writing or reading display data. This function is used to correct or search the display. In a 2-line display, the cursor moves to the 2nd line when it passes the 40th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time. When the displayed data is shifted repeatedly each line only moves horizontally. The 2nd line display does not shift into the 1st line postion.

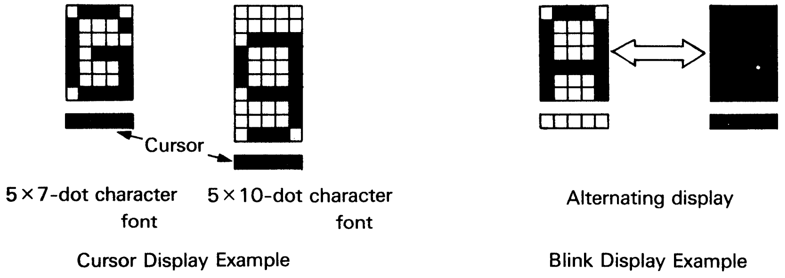
Table 6 shows how S/C and R/L control shifting.
Address counter (AC) contents do not change if the only action performed is shift display.

Function Set

DL: DL (figure 18) sets interface data length. Data is sent or received in 8-bit length (DB_7-DB_0) when DL = 1 and in 4-bit lengths (DB_7-DB_4) when DL = 0.

Table 6. Cursor or Display Shift Control

S/C	R/L	Function
0	0	Shifts the cursor position to the left (AC is decremented by one)
0	1	Shifts the cursor position to the right (AC is incremented by one)
1	0	Shifts the entire display to the left. The cursor follows the display shift
1	1	Shifts the entire display to the right. The cursor follows the display shift



5×7-dot character font

5×10-dot character font

Cursor Display Example

Alternating display

Blink Display Example

Figure 16. Cursor and Blink Display

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* Don't care

Figure 17. Corsor or Display Shift Instruction

When the 4-bit length is selected, data must be sent or received twice.

N: N sets number of display lines.
F: F sets character font. See table 7.

Note: Perform the function set at the head of the program before executing all instructions (except "Busy flag/address read"). From this point, the function set instruction cannot be executed unless the interface data length is changed.

Set CG RAM Address

Set CG RAM address (figure 19) sets the CG RAM address into the address counter in binary AAAAAA. Data is then written or read from the MPU for the CG RAM.

Set DD RAM Address

Set DD RAM address (figure 20) sets the DD RAM address into the address counter in binary (AAAAAAA). Data is then written or read from the MPU for the DD RAM.

However, when N = 0 (1-line display), AAAAAAA is 00-4F (hexadecimal), when N = 1 (2-line display), AAAAAAA is 00-27 (hexadecimal) for the first line, and 40-67 (hexadecimal) for the second line.

Read Busy Flag and Address

Read busy flag and address (figure 21) reads the busy flag (BF) that indicates the system is now internally operating on a previously received instruction. BF = 1 indicates that internal operation is in progress. The next

Table 7. Function Set N and F

N F	No. of Display Lines	Character Font	Duty Factor	Remarks
0 0	1	5×7 dots	1/8	
0 1	1	5×10 dots	1/11	
1 *	2	5×7 dots	1/16	Cannot display 2 lines with 5×10-dot character font.

Note: * Don't care

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	1	DL	N	F	*	*

* (Don't care)

Figure 18. Function Set Instruction

	RS	R/W	DB_7							DB_0
Code	0	0	0	1	A	A	A	A	A	A

← Higher Order Bits　Lower Order Bits →

Figure 19. Set CG RAM Address Instruction

	RS	R/W	DB_7							DB_0
Code	0	0	1	A	A	A	A	A	A	A

← Higher Order Bits　Lower Order Bits →

Figure 20. Set DD RAM Address Instruction

instruction will not be accepted until BF is set to 0. Check the BF status before the next write operation (figure 22).

At the same time, the value of the address counter expressed in binary (AAAAAAA) is read out. The address counter is used by both CG and DD RAM addresses, and its value is determined by the previous instruction. Address contents are the same as in set CG RAM address and set DD RAM address.

Write Data to CG or DD RAM

Write data to CG or DD RAM (figure 23) writes binary 8-bit data DDDDDDDD to the CG or the DD RAM.

Whether the CG or DD RAM is to be written into is determined by the previous specification of CG RAM or DD RAM address setting. After writing the LCD-IIA automatically increments or decrements the address by 1, according to entry mode.

Read Data from CG or DD RAM

Read data from CG or DD RAM (figure 24) reads binary 8-bit data DDDDDDDD from the CG or DD RAM.

The previous designation determines whether the CG or DD RAM is to be read. Before entering the read instruction, you must execute either the CG RAM or DD RAM address set instruction. If you do not the first read data will be invalidated. When serially executing read instructions, the next address data is normally read from the second read. The address set instruction need not be executed just before the read instruction when shifting the cursor by cursor shift instruction (when reading out of DD RAM). The cursor shift instruction operation is the

	RS	R/W	DB_7							DB_0
Code	0	1	BF	A	A	A	A	A	A	A

← Higher Order Bits   Lower Order Bits →

Figure 21. Read Busy Flag and Address Instruction

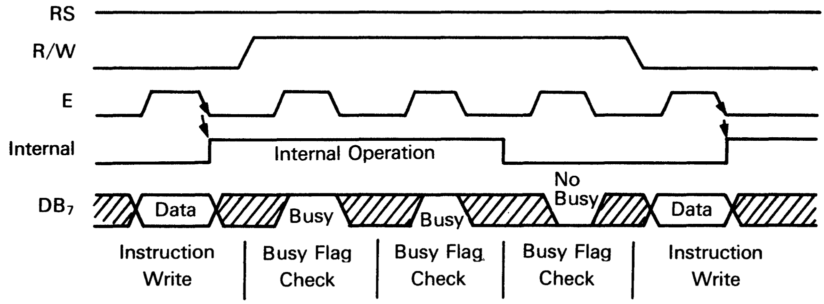


Figure 22. Example of Busy Flag Check Timing Sequence

	RS	R/W	DB_7							DB_0
Code	1	0	D	D	D	D	D	D	D	D

← Higher Order Bits   Lower Order Bits →

Figure 23. Write Data to CG or DD RAM Instruction

same as that of the DD RAM's address set instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display is not shifted no matter what the entry mode is.

Note: The address counter (AC) is automatically incremented or decremented by 1 after write instructions to either CG RAM or DD RAM. RAM data selected by the AC cannot then be read out even if read instructions are executed. The conditions for correct data read out are: execute either the address set instruction or cursor shift instruction (only with DD RAM), then just before reading out, execute the read instruction from the second time the read instruction is serial.

How to Use the HD66780

Interface to 8-Bit MPU

When Connecting to 8-Bit MPU Through PIA: Figure 25 is an example of using a PIA or I/O port (for a microcontroller) as an interface device. Input and output of the device is TTL compatible.
In the example, PB_0 to PB_7 are connected to the data buses DB_0 to DB_7 and PA_0 to PA_2 are connected to E, R/W and RS respectively.

Pay attention to the timing relation between E and other signals when reading or writing data and using PIA as an interface.

Connecting Directly to the 8-Bit MPU Bus: Figure 26 shows the LCD-IIA connected directly to an HD6800.

Example of Interfacing to the HD6805: Figure 27 shows the LCD-IIA connected directly to an HD6805.

Example of Interfacing to the HD6301: Figure 28 shows the LCD-IIA connected directly to an HD6301.

	RS	R/W	DB_7							DB_0
Code	1	1	D	D	D	D	D	D	D	D

← Higher Order Bits

Lower Order Bits →

Figure 24. Read Data from CG or DD RAM Instruction

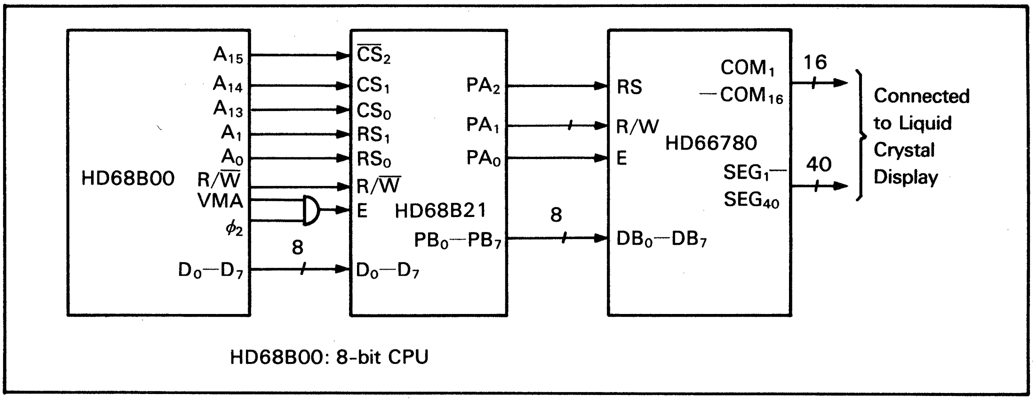


Figure 25. Example of Interface to HD68B00 using PIA (HD68B21)

Interface to 4-Bit MPU

The HD66780 can be connected to a 4-bit MPU through the 4-bit MPU I/O port. If the I/O port has enough bits, data can be transferred in 8-bit length, but if the bits are insufficient, the transfer is made in two operations of 4 bits each (designating the interface data length as 4 bits). In the latter case, the timing sequence becomes somewhat complex. (see figure 29)

Note that 2 cycles are needed for the busy flag check as well as the data transfer. 4-bit operation is selected by program.

Figure 30 shows an example of an interface to the 400 series.

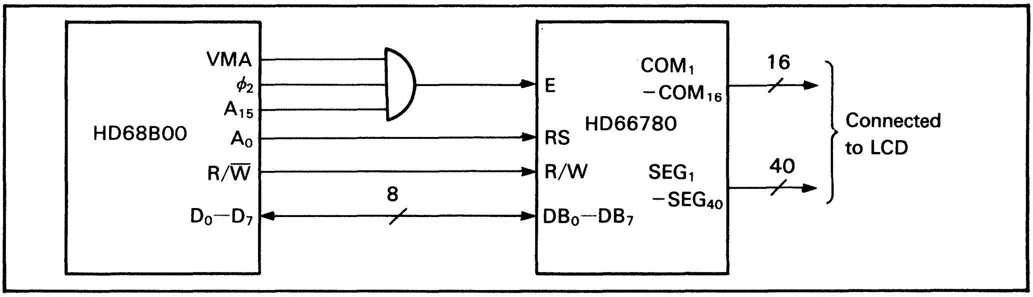


Figure 26. Direct Connection to HD68B00

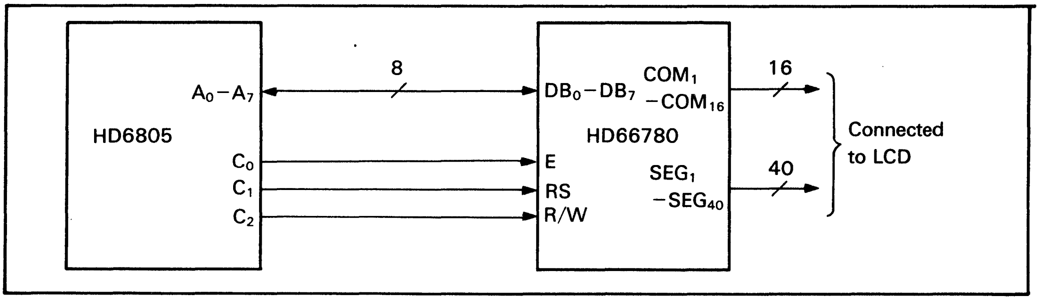


Figure 27. Direct Connection to HD6805

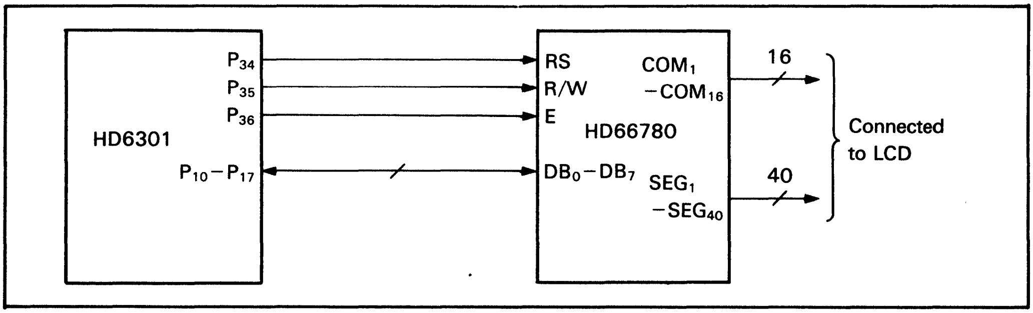


Figure 28. Direct Connection to HD6301

Interface to Liquid Crystal Display

Character Font and Number of Lines: The HD66780 can perform 2 types of display, using 5 × 7 dots or 5 × 10 dots for the character font, with a cursor on each.

Up to 2 lines can be displayed with 5 × 7 dots and 1 line with 5 × 10 dots.

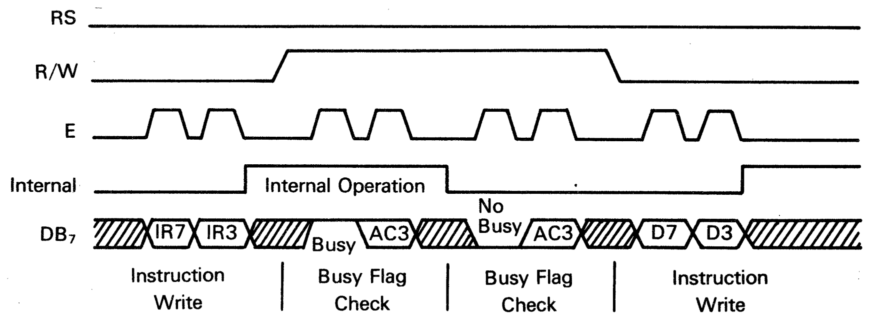
Therefore, three types of common signals are available (table 8).

Number of lines and font types can be selected by program (see table 5).

Connection to HD66780 and Liquid Crystal Display: Figure 31 shows connection examples. Since 5 SEG signal lines can display one digit, one HD66780 can display up to 8 digits

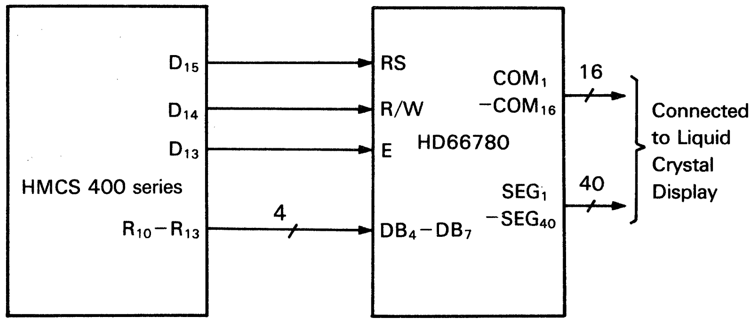
Table 8. Common Signals

Number of Lines	Character Font	Number of Common Signals	Duty Factor
1	5 × 7 dots + Cursor	8	1/8
1	5 ×10 dots + Cursor	11	1/11
2	5 × 7 dots + Cursor	16	1/16



Note: IR7, IR3: Instruction 7th bit, 3rd bit
AC3: Address Counter 3rd bit

Figure 29. An Example of 4-Bit Data Transfer Timing Sequence

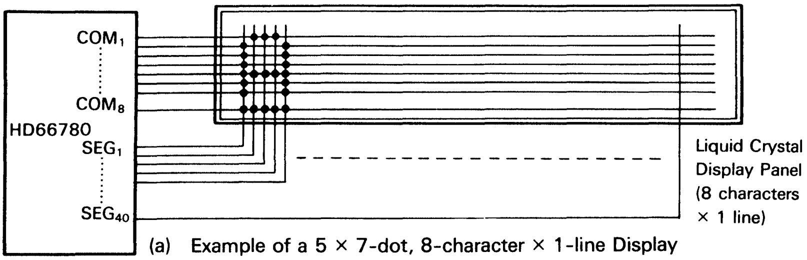


HMCS 400 series: Hitachi 4-bit microcontroller

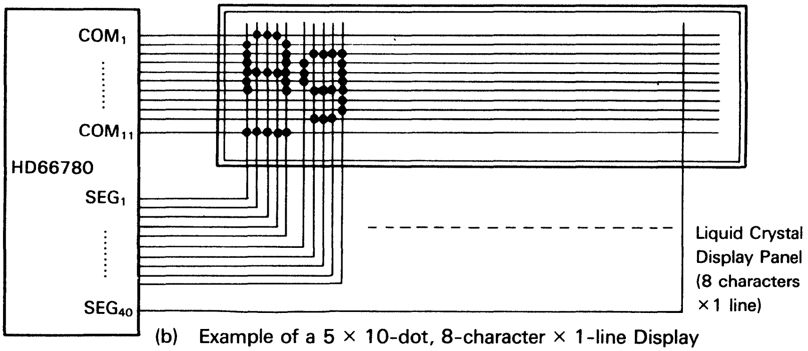
Figure 30. Example of Interface to the 400 Series

for a 1-line display and 16 digits for a 2-line display.

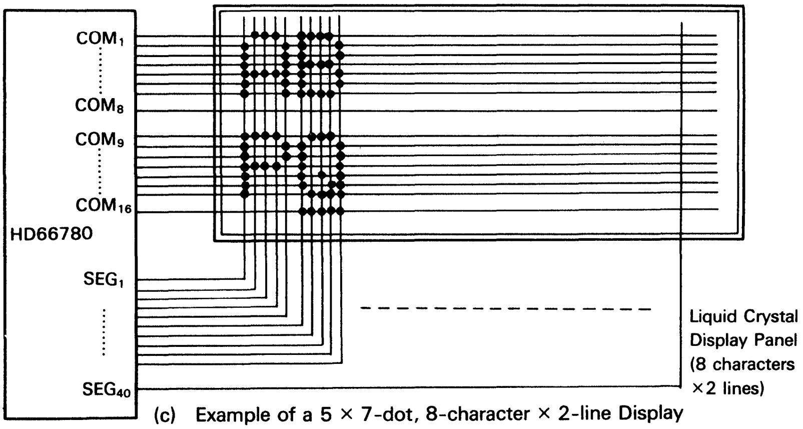
In figure 31 examples (a) and (b), there are unused common signal terminals, which always output non-selection waveforms. When the liquid crystal display panel has unused extra scanning lines, avoid undesirable influences due to cross-talk in the floating state by connecting the extra scanning lines to these common signal terminals (figure 32).



(a) Example of a 5 × 7-dot, 8-character × 1-line Display (1/4 Bias, 1/8 Duty)



(b) Example of a 5 × 10-dot, 8-character × 1-line Display (1/4 Bias, 1/11 Duty)



(c) Example of a 5 × 7-dot, 8-character × 2-line Display (1/5 Bias, 1/16 Duty)

Figure 31. Liquid Crystal Display and Connections to HD66780

Connection for Changed Matrix Layout: In the preceding examples, the number of lines was matched to the number of scanning lines. The display types in figure 33 are possible by changing the matrix layout in the liquid crystal display panel.

In either case, the only change is the layout. Display characteristics and the number of liquid crystal display characters depend on the number of common signals (or duty factor). Note that the display data RAM (DD RAM) address for 8 characters × 2 lines and 16 characters × 1 line are the same as shown in figure 31.

Power Supply for Liquid Crystal Display Drive

Various voltage levels must be applied to HD66780 terminals V_1 to V_5 to obtain liquid crystal display drive waveforms. The voltages must be changed according to duty factors. Table 9 shows the relation.

V_{LCD} gives the peak values for lipuid crystal display drive waveforms. Resistance dividing provides each voltage as shown in figure 34.

Relation between Oscillation Frequency and Liquid Crystal Display Frame Frequency

Figure 35 shows examples of liquid crystal display frame frequency when the oscillation frequency is 250 kHz. (1 clock = 4 μs)

Connection with Driver LSI HD44100H or HD66100F

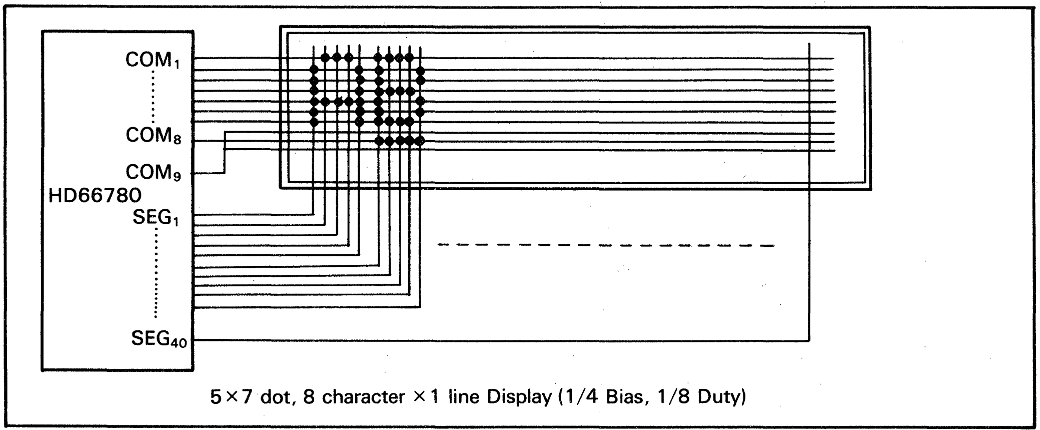
You can increase the number of display characters by externally connecting liquid crystal display driver LSI's HD44100H or HD66100F to the HD66780.

When connected to the HD66780, the HD44100H or HD66100F is used as a segment signal driver. The HD44100H and the HD66100F can be connected to the HD66780 directly since they supply CL_1, CL_2, M, and D signals and power for liquid crystal display drive. Figures 36 and 37 show connection examples.

Note: Connection of voltage supply terminals V_1 through V_6 for the liquid crystal display drive is complicated.

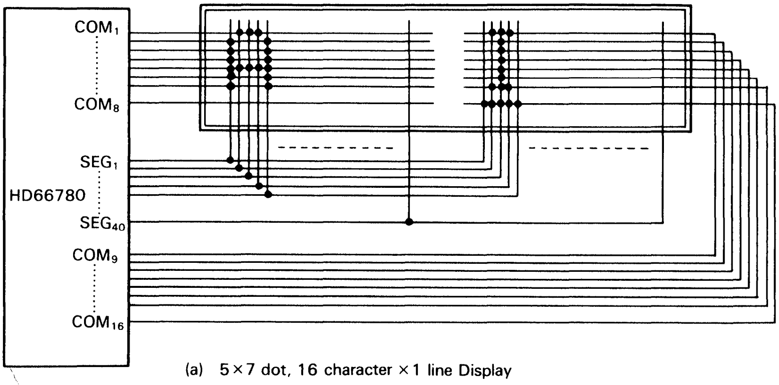
Table 9. Duty Factor and Power Supply for Liquid Crystal Display Drive

Duty Factor	Bias	Power Supply				
		V_1	V_2	V_3	V_4	V_5
1/8, 1/11	1/4	V_{CC} - (1/4)V_{LCD}	V_{CC} - (1/2)V_{LCD}	V_{CC} - (1/2)V_{LCD}	V_{CC} - (3/4)V_{LCD}	V_{CC} - V_{LCD}
1/16	1/5	V_{CC} - (1/5)V_{LCD}	V_{CC} - (2/5)V_{LCD}	V_{CC} - (3/5)V_{LCD}	V_{CC} - (4/5)V_{LCD}	V_{CC} - V_{LCD}

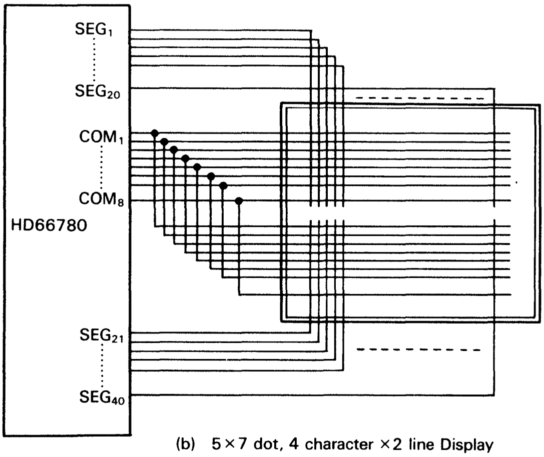


5×7 dot, 8 character ×1 line Display (1/4 Bias, 1/8 Duty)

Figure 32. Using COM_9 to Avoid Cross-Talk on Unneeded Scanning Line

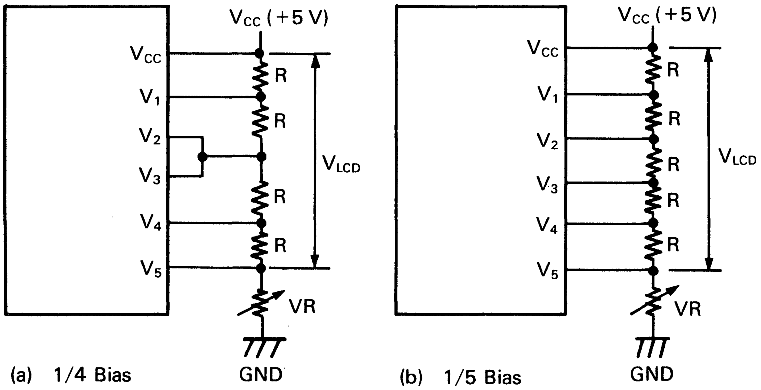


(a) 5×7 dot, 16 character ×1 line Display
(1/5 Bias, 1/16 Duty)



(b) 5×7 dot, 4 character ×2 line Display
(1/4 Bias, 1/8 Dury)

Figure 33. Changed Matrix Layout Displays



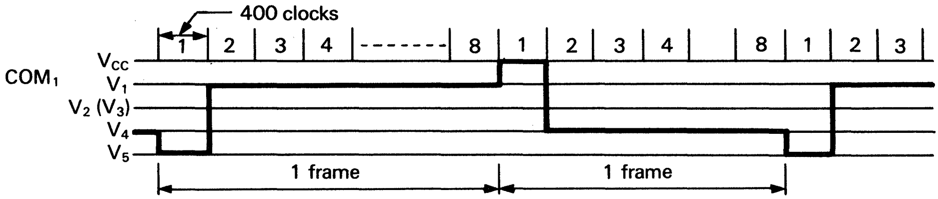
(a) 1/4 Bias
(1/8, 1/11 Duty)

(b) 1/5 Bias
(1/16 Duty)

Figure 34. Drive Voltage Supply Example

Up to 9 HD44100Hs can be connected for a 1-line display (duty factor 1/8 or 1/11) and up to 4 for a 2-line display (duty factor 1/16). (For the HD66100F, 5 and 2 units respectively.) RAM size limits the HD66780 to a maximum of 80 character diaplay digits. The connection method in figures 36 and 37 remains unchanged for both 1-line and 2-line display and both 5 × 7-and 5 × 10-dot character fonts.

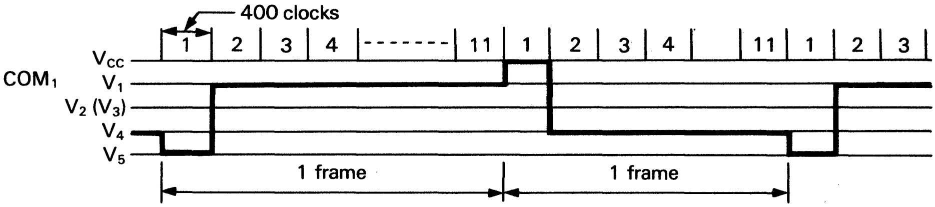
(1) 1/8 Duty



1 frame = 4 (μs) × 400 × 8 = 12800 (μs) = 12.8 (ms)

$$\text{Frame frequency} = \frac{1}{12.8\ (\text{ms})} = 78.1\ (\text{Hz})$$

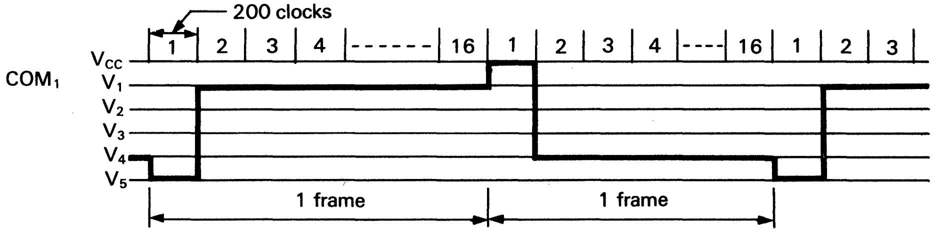
(2) 1/11 Duty



1 frame = 4 (μs) × 400 × 11 = 17600 (μs) = 17.6 (ms)

$$\text{Frame frequency} = \frac{1}{17.6\ (\text{ms})} = 56.8\ (\text{Hz})$$

(3) 1/16 Duty



1 frame = 4 (μs) × 200 × 16 = 12800 (μs) = 12.8 (ms)

$$\text{Frame frequency} = \frac{1}{12.8\ (\text{ms})} = 78.1\ (\text{Hz})$$

Figure 35. Liquid Crystal Display Waveforms (at f_{OSC} = 250kHz)

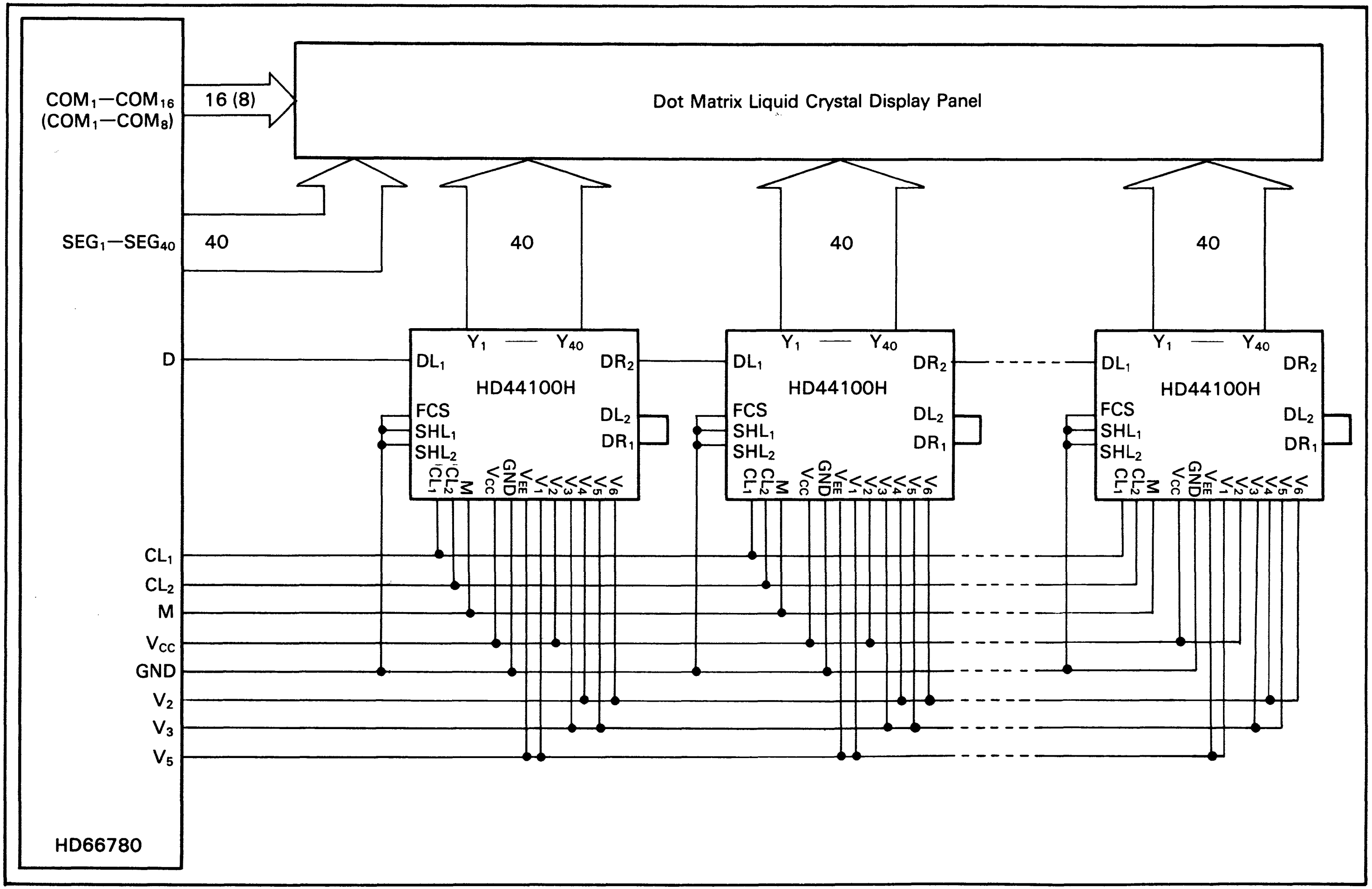


Figure 36. Example of Connecting HD44100H to HD66780

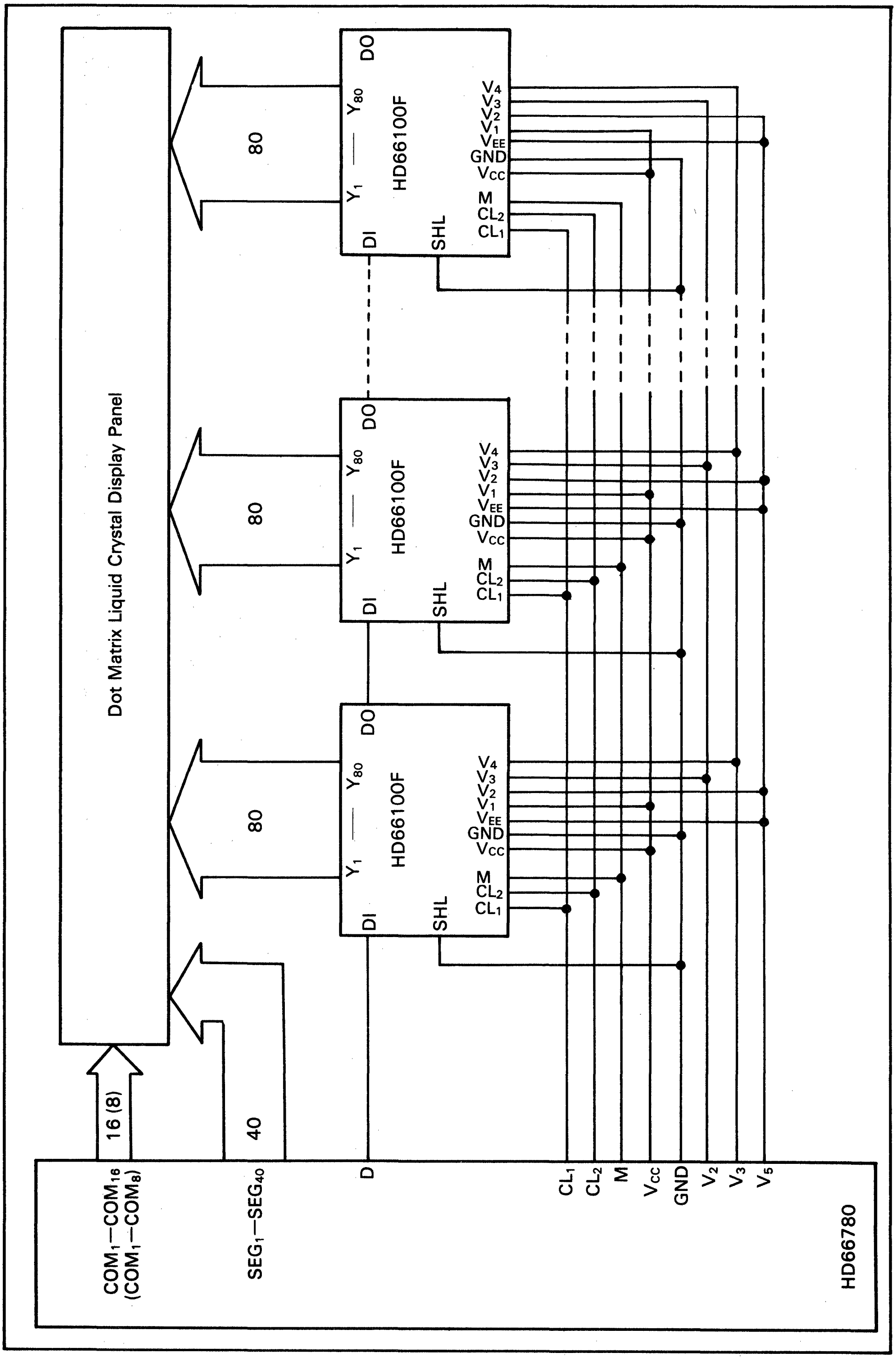


Figure 37. Example of Connecting HD66100F to HD66780

Instruction and Display Correspondence

8-bit Operation, 8-digit × 1-line Display (Using Internal Reset): Table 10 shows an example of an 8-bit × 1-line display in 8-bit operation. The HD66780 functions must be set by the function set instruction prior to display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for advertising displays when combined with display shift operation. Since the display shift operation changes display position only and DD RAM contents remain unchanged, display data entered first can be output when the return home operation is performed.

4-bit Operation, 8-digit × 1-line Display (Using Internal Reset): The program must set functions prior to 4-bit operation. Table 11 shows an example. When power is turned on, 8-bit operation is automatically selected and the LCD-IIA attempts to perform the first write as an 8-bit operation. Since nothing is connected to DB_0-DB_3, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is needed to set the functions (see table 11 step 3).

Thus, DB_4-DB_7 of the function set is written twice.

8-bit Operation, 8-digit × 2-line Display: For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DD RAM address must be set after the eighth character is completed (see table 12). Note that the first and second lines of the display are shifted.

In the example, the display is shifted when the cursor is on the second line. However, if the shift operation is performed when the cursor is on the first line, both the first and second lines move together. When you repeat the shift, the display of the second line will not move to the first line, the same display will only move within each line many times.

Note: When using the internal reset, the conditions in "Power Supply Condition Using Internal Reset Circuit" must be satisfied. If not, the HD66780 must be initialized by instruction. (See "Initializing by Instruction")

Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, the LCD-IIA must be initialized by instruction.
When interface is 8 bits long, use the initialization procedure in figure 38.

When interface is 4 bits long, use the initialization proceduer in figure 39.

Table 10. 8-bit Operation, 8-character × 1-line Display Example (Using Internal Reset)

Step No.	Instruction	Display	Operation
1	Power Supply On (HD66780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB7 · · · DB0 0 0 0 0 1 1 0 0 * *		Sets to 8-bits operation and selects 1-line display and one of the three character fonts. (Number of display lines and character font cannot be changed hereafter.)
3	Display On/Off Control 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. Entire display is on space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Writes "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HI_	Writes "I".
7	⋮	⋮	
8	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
9	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI_	Sets mode for display shift at the time of write.
10	Write Data to CG RAM/DD RAM 1 0 0 0 1 0 0 0 0 0	ITACHI _	Writes space.
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	TACHI M_	Writes "M".
12	⋮	⋮	
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	MICROKO_	Writes "O".
14	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
15	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
16	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 0 0 1 1	ICROCO	Writes "C" (correction). The display moves to the left.
17	Cursor or Display Shift 0 0 0 0 0 1 1 1 * *	MICROCO	Shifts the display and cursor position to the right.
18	Cursor or Display Shift 0 0 0 0 0 1 0 1 * *	MICROCO_	Shifts only the cursor position to the right.
19	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ICROCOM_	Writes "M".
20	⋮	⋮	
21	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI	Returns both display and cursor to the original position (address 0).

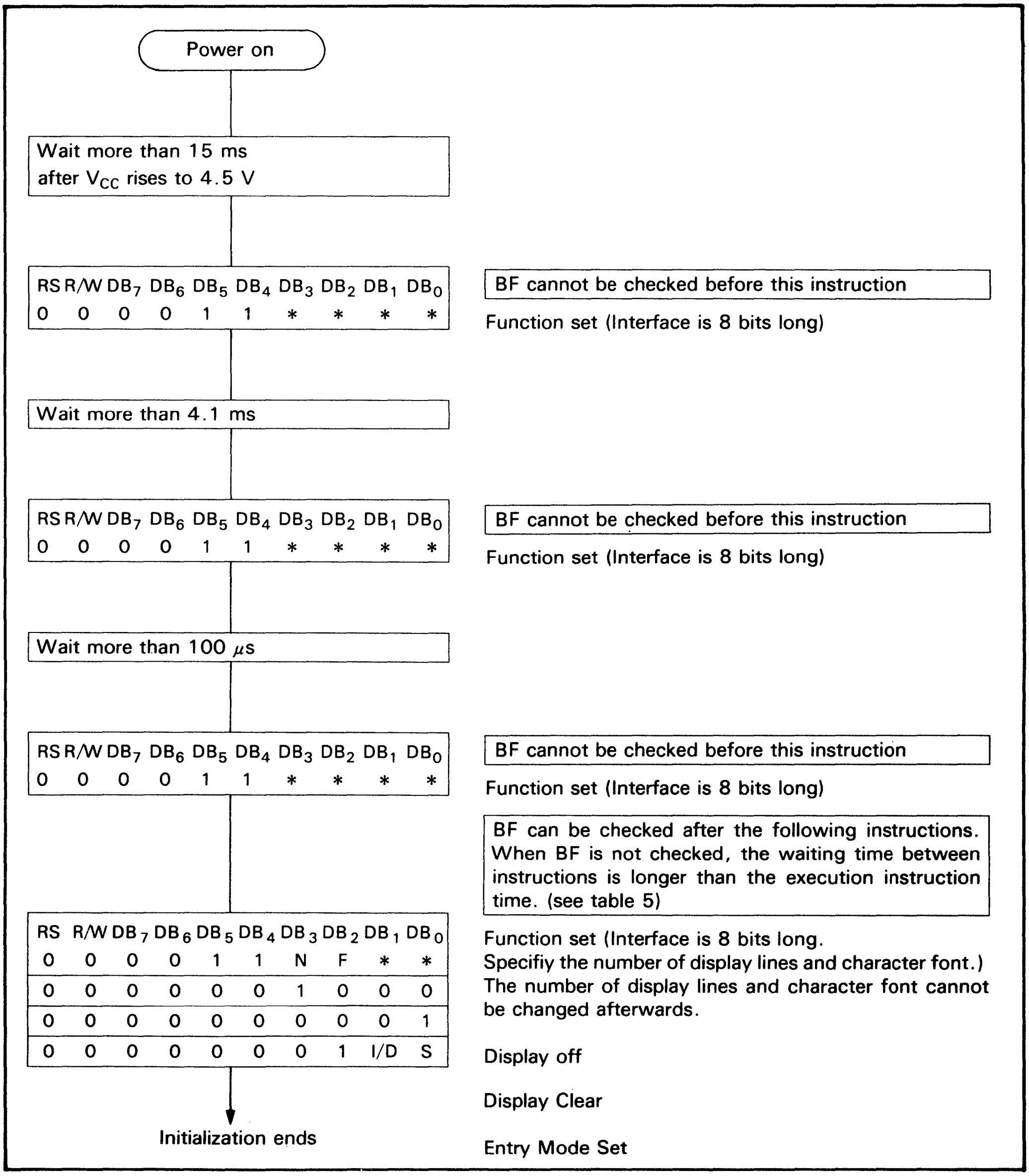
Table 11. 4-bit Operation, 8-character × 1-line Display Example (Using Internal Reset)

Step No.	Instruction	Display	Operation
1	Power Supply On (HD66780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 · · · DB_4 0 0 0 0 1 0		Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
3	Function Set 0 0 0 0 1 0 0 0 0 0 * *		Sets to 4-bit operation and selects 1-line display and one of the three character fonts. 4-bit operation starts from this point on and resetting is needed. (Number of display lines and character font cannot be changed hereafter.)
4	Display On/Off Control 0 0 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
5	Entry Mode Set 0 0 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 1 0 0 0	H_	Writes "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.

Hereafter, control is the same as 8-bit operation.

Table 12. 8-bit Operation, 8-character × 2-line Display Example (Using Internal Reset)

Step No.	Instruction	Display	Operation
1	Power Supply On (HD66780 is intialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB7 · · · DB0 0 0 0 0 1 1 1 0 * *		Sets to 8-bit operation and selects 2-line display and one of the three character fonts.
3	Display On/Off Control 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. All display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Writes "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	⋮	⋮	
7	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
8	Set DD RAM Address 0 0 1 1 0 0 0 0 0 0	HITACHI _	Sets RAM address so that the cursor may be positioned at the head of the 2nd line.
9	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	HITACHI M_	Writes "M".
10	⋮	⋮	
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	HITACHI MICROCO_	Writes "O".
12	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI MICROCO_	Sets mode for display shift at the time of write.
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ITACHI ICROCOM_	Writes "M". Display is shifted to the left. The first and second lines' shift is operated at the same time.
14	⋮	⋮	
15	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI MICROCOM	Returns both display and cursor to the original position (address 0).



Power on

Wait more than 15 ms
after V_{CC} rises to 4.5 V

RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	1	1	*	*	*	*

BF cannot be checked before this instruction

Function set (Interface is 8 bits long)

Wait more than 4.1 ms

RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	1	1	*	*	*	*

BF cannot be checked before this instruction

Function set (Interface is 8 bits long)

Wait more than 100 μs

RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	1	1	*	*	*	*

BF cannot be checked before this instruction

Function set (Interface is 8 bits long)

BF can be checked after the following instructions. When BF is not checked, the waiting time between instructions is longer than the execution instruction time. (see table 5)

RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	1	1	N	F	*	*
0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	I/D	S

Function set (Interface is 8 bits long.
Specifiy the number of display lines and character font.)
The number of display lines and character font cannot be changed afterwards.

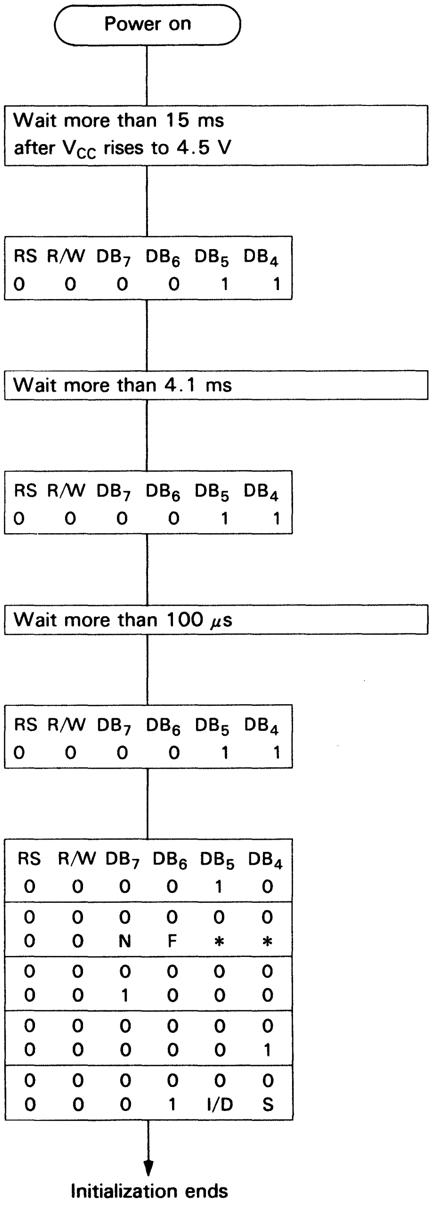
Display off

Display Clear

Entry Mode Set

Initialization ends

Figure 38. Initialization by Instruction, Eight-Bit Interface


Power on
Wait more than 15 ms after V_{CC} rises to 4.5 V
RS R/W DB_7 DB_6 DB_5 DB_4
0 0 0 0 1 1
Wait more than 4.1 ms
RS R/W DB_7 DB_6 DB_5 DB_4
0 0 0 0 1 1
Wait more than 100 μs
RS R/W DB_7 DB_6 DB_5 DB_4
0 0 0 0 1 1
RS R/W DB_7 DB_6 DB_5 DB_4
0 0 0 0 1 0
0 0 0 0 0 0
0 0 N F * *
0 0 0 0 0 0
0 0 1 0 0 0
0 0 0 0 0 0
0 0 0 0 0 1
0 0 0 0 0 0
0 0 0 1 I/D S
Initialization ends

BF cannot be checked before this instruction

Function set (Interface is 8 bits long)

BF cannot be checked before this instruction

Function set (Interface is 8 bits long)

BF cannot be checked before this instruction

Function set (Interface is 8 bits length)

BF can be checked after the following instructions. When BF is not checked, the waiting time between instructions is longer than the execution instruction time. (See table 5)

Function set (Set interface to be 4 bits long.)
Interface is 8 bits long.

Function set (Interface is 4 bits long. Specify the number of display lines and character font.)
The number of display lines and character font cannot be changed afterwards.

Display off

Display Clear

Entry Mode Set

Figure 39. Initialization by Instruction, Four-Bit Interface

LCD-II and LCD-IIA

Table 13 shows the differences between the LCD-II and LCA-IIA.

There are two types of multiplex waveforms for LCD driving; A and B. A type, shown in figure 40, is used for alternation in 1 frame, and B type, shown in figure 41, for alternation in 2 frames. B type has better display quality in high multiplex drive.

Table 13. Functions Comparison between LCD-II and LCD-IIA

Item		LCD-II (HD44780)	LCD-IIA (HD66780)	Note
Display RAM (Maximum number of display characters)		80 bytes (80 characters)	Same as LCD-II	
*Character generator ROM (Kinds of characters)		7200 bits 192 characters 5×7 ;160 characters 5×10; 32 characters	12000 bits 240 characters 5×10;240 characters	
Character generator RAM (Number of characters)		64 bytes (8 characters)	Same as LCD-II	
LCD driving terminals (Maximum number of display characters/ unit)		16 COM's 40 SEG's (16 characters)	Same as LCD-II	
Character font (with a cursor)		5×8 dots 5×11 dots	Same as LCD-II	
Multiplexing duty ratio		1/8, 1/11, 1/16		
*LCD driving voltage	1/4 bias	3.0 to 11 (v)	3.0 to V_{CC} (V)	V_{CC} to V_5 (V)
	1/5 bias	4.6 to 11 (v)	3.0 to V_{CC} (v)	
*LCD driving waveform		A waveform	B waveform	See figures 40,41
*Bus timing		1, 1.5 MHz	2 MHz	
Instruction codes		11 instructions	Same as LCD-II	
Power-on reset circuit		Yes	Same as LCD-II	
Oscillator (Frequency)		Ceramic filter, Rf, external clock (250 kHz)	Same as LCD-II	
Interface		HD44100H	HD44100H or HD66100F	
Package		FP-80, FP-80A	Same as LCD-II	
Pin arrangement		Refer to p.1	Same as LCD-II	

Note: * indicates the modified items on LCD-IIA.

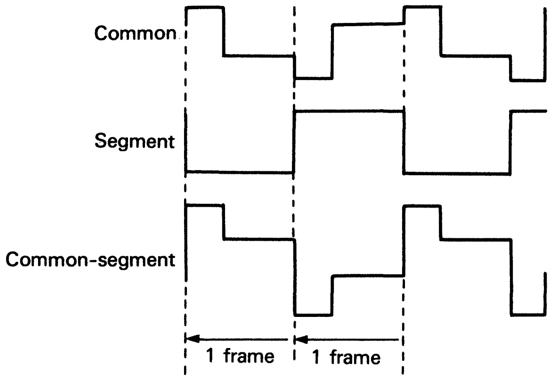


Figure 40. A-Type Waveforms (1/3 Duty, 1/3 Bias)

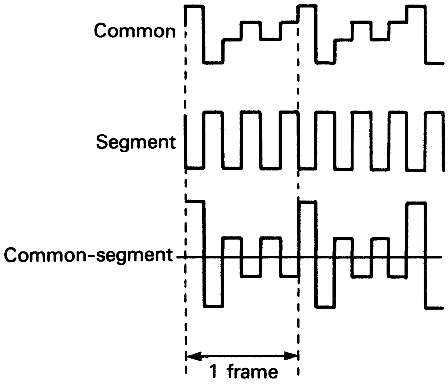


Figure 41. B-Type Waveforms (1/3 Duty, 1/3 Bias)

1. Character Pattern Development Procedure

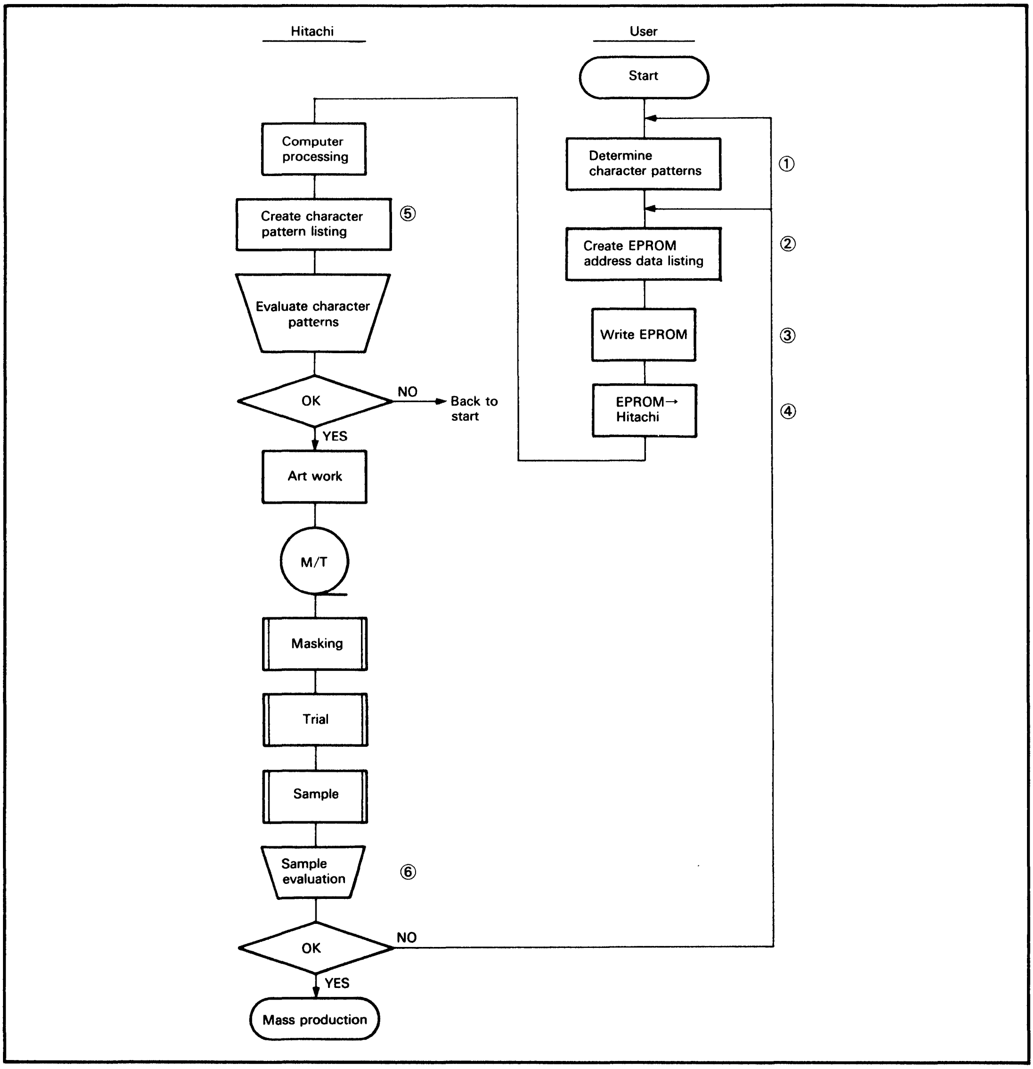


Figure 42. Character pattern development procedure

The numbers in the above figure correspond to the following operations:

(1) Determine the correspondence between character codes and character patterns.

(2) Create a listing indicating the correspondence between EPROM addresses and data.

(3) Program character patterns in the EPROM.

(4) Send the EPROM to Hitachi.

(5) Hitachi performs computer processing with the EPROM to create a character pattern listing and sends it to the user.

(6) If there is no problem in the character pattern listing, Hitachi creates LSI for trial and sends samples to the user.The user evaluates the samples. When it is confirmed that character patterns are correctly written, mass production of LSI is started.

- Character pattern program method

The relationship between the EPROM address and character pattern is as follows.

In order to evaluate ROM patterns, we recommend to use our LCD controller HD61830. We also supply LCD control board (CB1026R).

EPROM ADDRESS												DATA							
												(LSB)							
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0			
								0	0	0	1	0	0	0	0	0			
								0	0	1	0	0	1	1	0	1			
								0	0	1	1	1	0	0	1	1			
								0	1	0	0	1	0	0	0	1			
								0	1	0	1	1	0	0	0	1			
								0	1	1	0	0	1	1	1	1			
								0	1	1	1	0	0	0	0	1			
								1	0	0	0	0	0	0	0	1			
								1	0	0	1	0	0	0	0	1			
								1	0	1	0	0	0	0	0	0			
								1	0	1	1								
								1	1	0	0								
								1	1	0	1								
								1	1	1	0								
								1	1	1	1								

Character code — Line code

Note:
1. EPROM DATA O_5-O_7 are invalid
2. DATA "0" must be programed at 11 th line (cursor position).
3. DATA at 12-16 th line are invalid
4. DATA at O_0 locate at the left side of screen. (The relation between the bit No, and position is reversed, comparing with HD44780).

• Handling unused character patterns

(1) EPROM data outside the character pattern area
It is ignored by the character generator ROM for display operation so that it can be 0 or 1.

(2) EPROM data in CG RAM area
It is ignored by the character generator ROM for display operation so that it can be 0 or 1.

(3) EPROM data used when the user does not use any LCD-II character pattern
It is handled in one of the two ways explained below. Select one of two ways according to the user application.

1) When unused character patterns are not programed
If an unused character code is written in the LCD-II DD RAM, all dots are lit. No programming for a character pattern is equivalent to all bits lit. (This is because EPROM is filled with 1 when the EPROM is erased.)

2) Program 0 for unused character patterns
Nothing is displayed even if unused character codes are written in LCD-II DD RAM. (It is equivalent to space.)

Absolute Maximum Ratings

Item	Pating	Reting	Unit
Power Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature	Topr	-20 to +75	°C
Storage Temperature	Tstg	-55 to +125	°C

Notes: 1. If LSI's are used above the absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristic limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.
2. All voltage values are referred to GND = 0 V.
3. Applies to V1 to V5. The relation: $V_{CC} \geqq V1 \geqq V3 \geqq V4 \geqq V5 \geqq GND$ must be maintained.
(high to low)

Electrical Characteristics

DC Electrical Characteristics (V_{CC} = 5V±10% Ta = -20 to +75 °C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage (1)	V_{IH1}	2.0	–	V_{CC}	V		(2)
Input Low Voltage (1)	V_{IL1}	–	–	0.8	V		(2)
Input High Voltage (2)	V_{IH2}	V_{CC} - 1.0	–	V_{CC}	V		(12)
Input Low Voltage (2)	V_{IL2}	–	–	1.0	V		(12)
Output High Voltage (1)(TTL)	V_{OH1}	2.4	–	–	V	$-I_{OH}$ = 0.205 mA	(3)
Output Low Voltage (1)(TTL)	V_{OL1}	–	–	0.4	V	I_{OL} = 1.6 mA	(3)
Output High Voltage (2)(CMOS)	V_{OH2}	$0.9V_{CC}$	–	–	V	$-I_{OH}$ = 0.04 mA	(4)
Output Low Voltage (2)(CMOS)	V_{OL2}	–	–	$0.1V_{CC}$	V	I_{OL} = 0.04 mA	(4)
Driver On Resistance (COM)	R_{COM}	–	–	20	kΩ	±Id = 0.05 mA to each COM Pin	(10)
Driver On Resistance (SEG)	R_{SEG}	–	–	30	kΩ	±Id = 0.05 mA to each SEG Pin	(10)
Input Leakage Current	I_{IL}	-1	–	1	µA	V_{in} = 0 to V_{CC}	(5)
Pull up MOS Current	$-I_P$	50	125	250	µA	V_{CC} = 5 V	
Power Supply Current (1)	I_{CC1}	–	0.55	0.8	mA	Ceramic filter oscillation V_{CC} = 5 V, f_{OSC} = 250 kHz	(6)
Power Supply Current (2)	I_{CC2}	–	0.35	0.6	mA	Rf oscillation, External clock operation V_{CC} = 5 V, f_{OSC} = fcp = 270 kHz	(6) (11)
External Clock Operation							
External Clock Frequency	f_{cp}	125	250	350	kHz		(7)
External Clock Duty	Duty	45	50	55	%		(7)
External Clock Rise Time	t_{rcp}	–	–	0.2	µs		(7)
External Clock Fall Time	t_{fcp}	–	–	0.2	µs		(7)
Internal Clock Operation (Rf Oscillation)							
Clock Oscillation Frequency	f_{OSC}	190	270	350	kHz	Rf = 82 kΩ±2%	(8)
Internal Clock Operation (Ceramic Filter Oscillation)							
Clock Oscillation Frequency	f_{OSC}	245	250	255	kHz	Ceramic filter	(9)
LCD Voltage	V_{LCD1}	3.0	–	V_{CC}	V	V_{CC} - V_5 1/5 bias	(13)
	V_{LCD2}	3.0	–	V_{CC}	V	1/4 bias	(13)

Notes:
1. Figure 42 shows the I/O pin configurations except for liquid crystal display output.
2. Input pins and I/O pins. Excludes OSC_1 pin.
3. I/O pins.
4. Output pins.
5. Current flowing through pull-up MOS's and output drive MOS's is excluded.
6. Input/output current is excluded. When input is at an intermediate level with CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low.
7. External clock operation as shown in figure43.
8. Internal oscillator operation using oscillation resistor Rf (figure 44).
9. Internal oscillator operation using a ceramic filter (figure 45)
10. R_{COM} applies to the resistance between power supply pin (V_{CC}, V_1, V_4, V_5) and each common signal pin (COM_1 to COM_{16}).
    R_{SEG} applies to the resistance between power supply pin (V_{CC}, V_2, V_3, V_5) and each segment signal pin (SEG_1 to SEG_{40}).

11. Relation between operation frequency and current consumption is shown in figure 46. (V_{CC} = 5 V)
12. Applied to OSC_1 pin.
13. When each COM and SEG output voltage is within ±0.15 V of LCD voltage (V_{CC}, V_1, V_2, V_3, V_4, V_5) when there is no load.

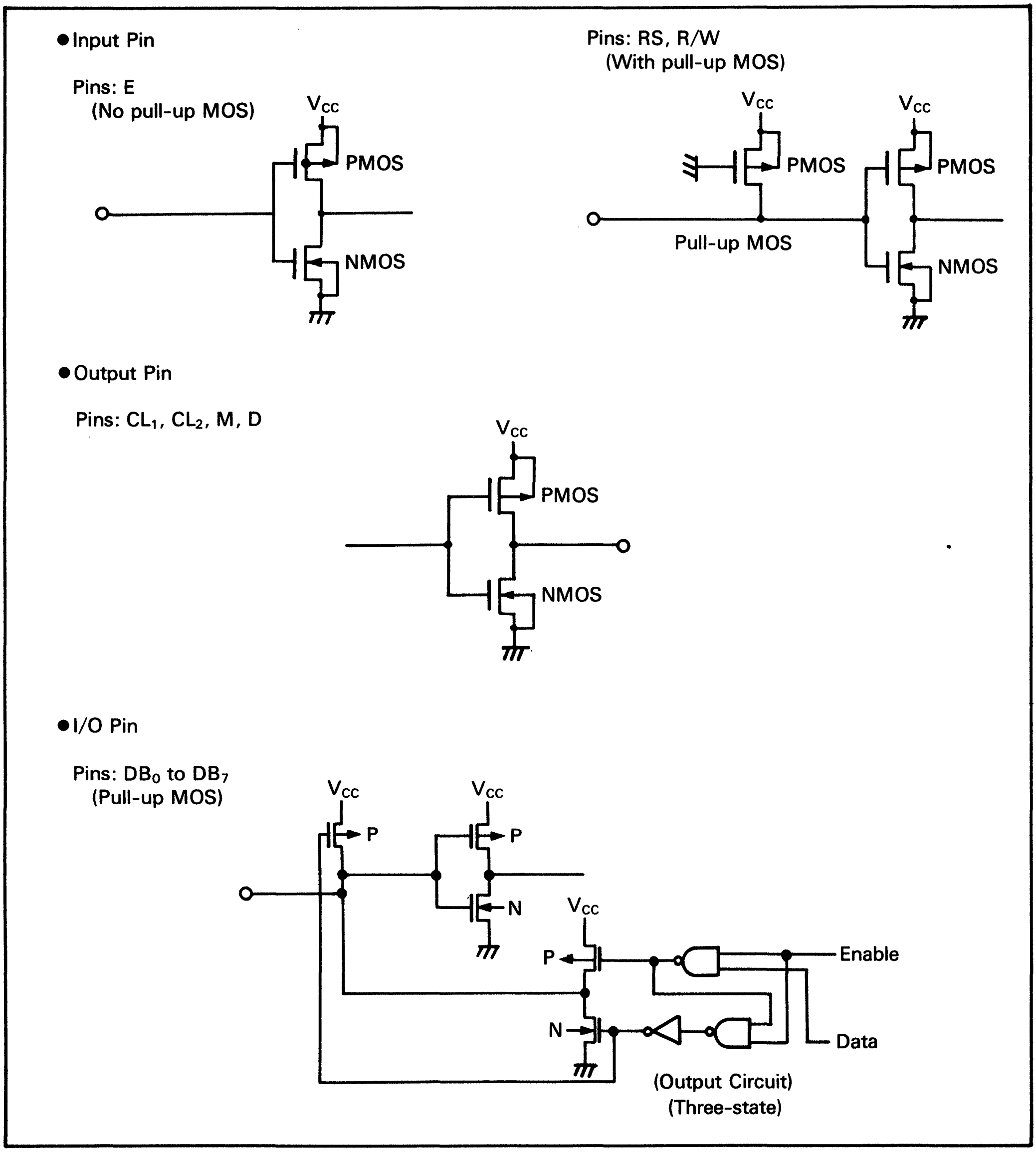
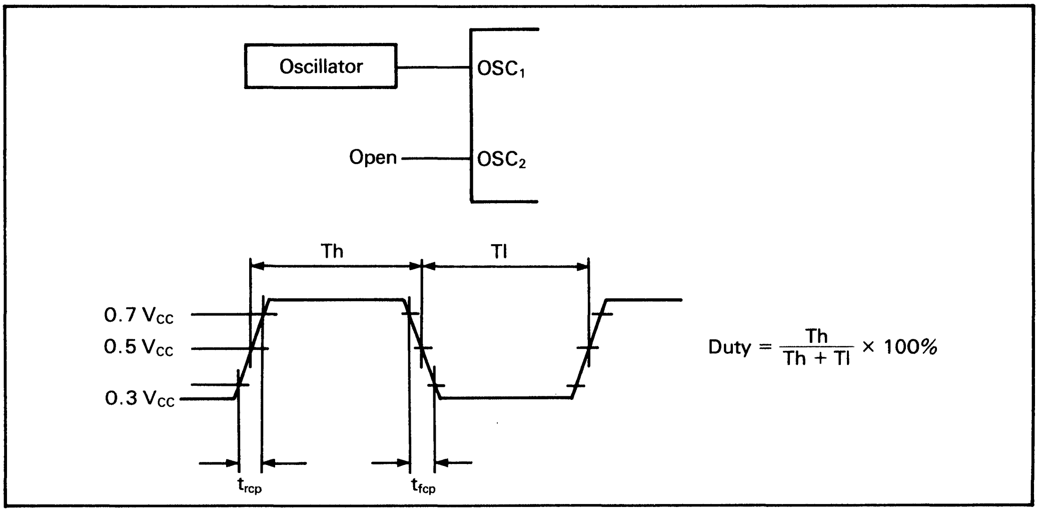
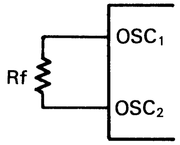


Figure 43. Pin Configuration



$$\text{Duty} = \frac{Th}{Th + Tl} \times 100\%$$

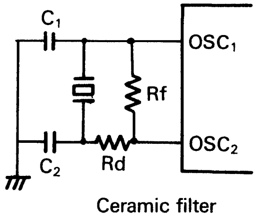
Figure 44. External Clock



Rf: 82 kΩ ± 2%

Since oscillation frequency varies depending on OSC_1 and OSC_2 terminal capacity, wiring length to these pin should be minimized.

Figure 45. Internal Oscillator, Resistor



Ceramic filter: CSB250A (Murata)
Rf: 1 MΩ ±10%
C_1 : 680 pF ±10%
C_2 : 680 pF ±10%
Rd: 3.3 kΩ ±5%

Note: This circuit is a standard one and we do not insure the oscillation frequency characteristics. Study the actual circuit ratings in using this circuit.

Figure 46. Internal Oscillator, Ceramic Filter

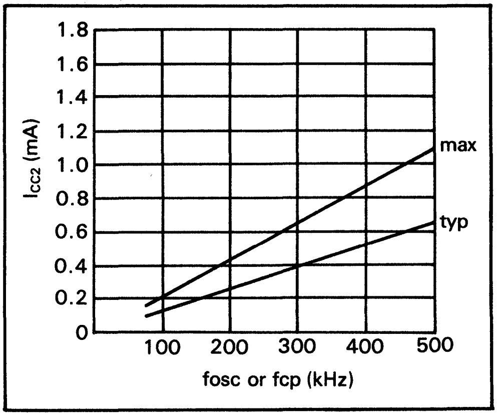
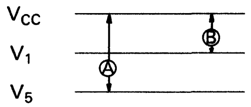


Figure 47. Frequency vs Current



Ⓐ = $V_{CC} - V_5$
Ⓑ = $V_{CC} - V_1$
Ⓐ $\geqq$ 1.5V
Ⓑ $\leqq 0.25 \times$ Ⓐ

Note: The conditions of V_1, V_5 voltages are for proper operation of the LSI and not for the LCD output level (figure 47). The LCD drive voltage condition for the LCD output level is specified in "LCD voltage V_{LCD}".

Figure 48. V_1, V_5 Voltages

Bus Timing Characteristics (V_{CC} = 5.0 V±10%, GND = 0 V, Ta = −20 to +75 °C)

Write Operation (Writing Data from MPU to HD66780)

Item	Symbol	Min	Max	Unit	Test Condition
Enable Cycle Time	t_{CYCE}	500	–	ns	Fig. 51
Enable Pulse Width (High level)	PW_{EH}	220	–	ns	Fig. 51
Enable Rise/Fall Time	t_{Er}, t_{Ef}	–	20	ns	Fig. 51
Address Set-up Time (RS, R/W−E)	t_{AS}	50	–	ns	Fig. 51
Address Hold Time	t_{AH}	10	–	ns	Fig. 51
Data Set-up Time	t_{DSW}	60	–	ns	Fig. 51
Data Hold Time	t_H	10	–	ns	Fig. 51

Read Operation (Reading Data from HD66780 to MPU)

Item	Symbol	Min	Max	Unit	Test Condition
Enable Cycle Time	t_{CYCE}	500	–	ns	Fig. 52
Enable Pulse Width (High level)	PW_{EH}	220	–	ns	Fig. 52
Enable Rise/Fall Time	t_{Er}, t_{Ef}	–	20	ns	Fig. 52
Address Set-up Time (RS, R/W −E)	t_{AS}	50	–	ns	Fig. 52
Address Hold Time	t_{AH}	10	–	ns	Fig. 52
Data Delay Time	t_{DDR}	–	150	ns	Fig. 52
Data Hold Time	t_{DHR}	20	100	ns	Fig. 52

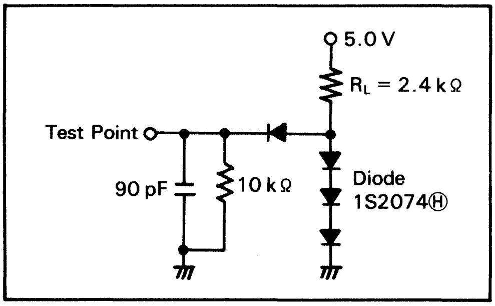


Figure 49. Load Circuit (DB_0−DB_7)

Interface Signal with HD44100H or HD66100F Timing Characteristics (V_{CC} = 5.0 V±10%, GND = 0 V, Ta = −20 to +75 °C)

Item		Symbol	Min	Max	Unit	Test Condition
Clock Pulse Width	(High level)	t_{CWH}	800	–	ns	Fig. 53
Clock Pulse Width	(Low level)	t_{CWL}	800	–	ns	Fig. 53
Clock Set-up Time		t_{CSU}	500	–	ns	Fig. 53
Data Set-up Time		t_{SU}	300	–	ns	Fig. 53
Data Hold Time		t_{DH}	300	–	ns	Fig. 53
M Delay Time		t_{DM}	-1000	1000	ns	Fig. 53
Clock Rise/Fall Time		t_{ct}	–	100	ns	Fig. 53

Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Min	Max	Unit	Test Condition
Power Supply Rise Time	t_{rCC}	0.1	10	ms	–
Power Supply Off Time	t_{OFF}	1	–	ms	–

Note: The internal reset circuit will not operate normally unless the preceding conditions are met. In that case, initialize by instruction. (Refer to Initializing by Instruction)

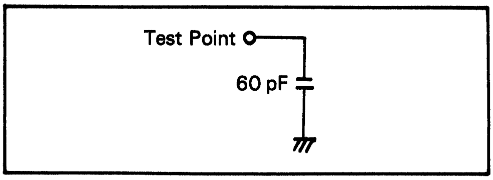
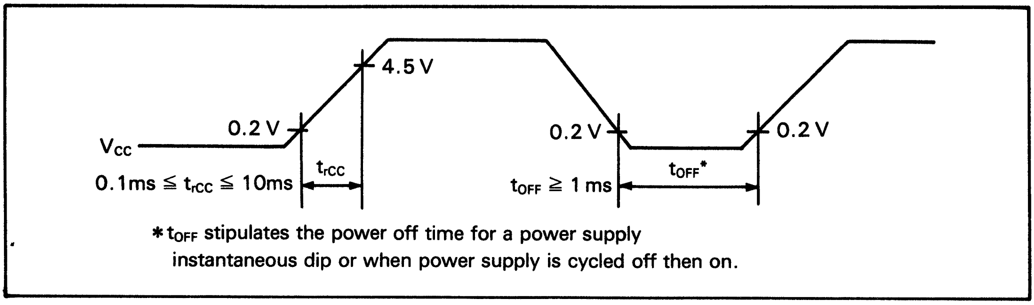


Figure 50. Interface Signal Load Circuit



* t_{OFF} stipulates the power off time for a power supply instantaneous dip or when power supply is cycled off then on.

Figure 51. Power Supply Timing

Timing Characteristics

Write Operation

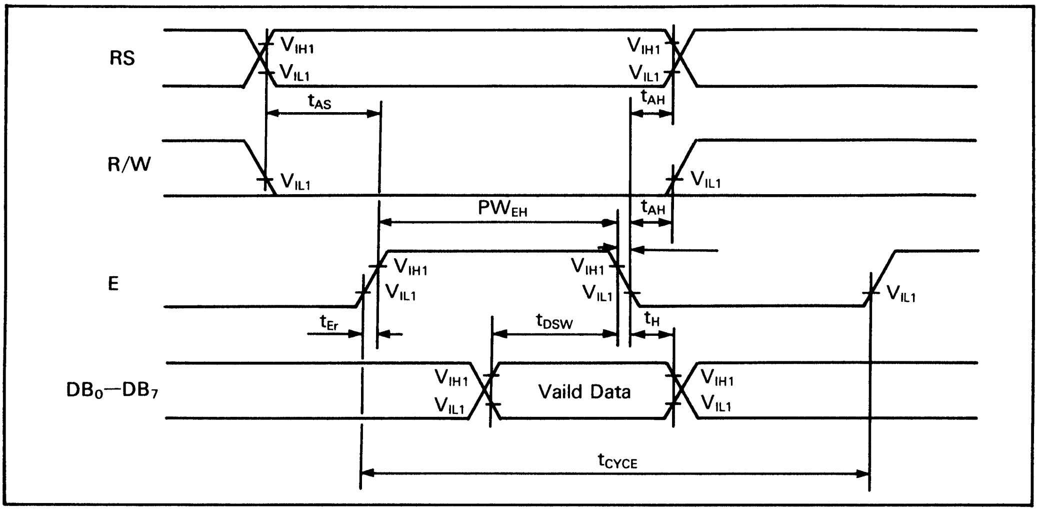


Figure 52. Bus Write Operation Sequence (Writing Data from MPU to HD66780)

Read Operation

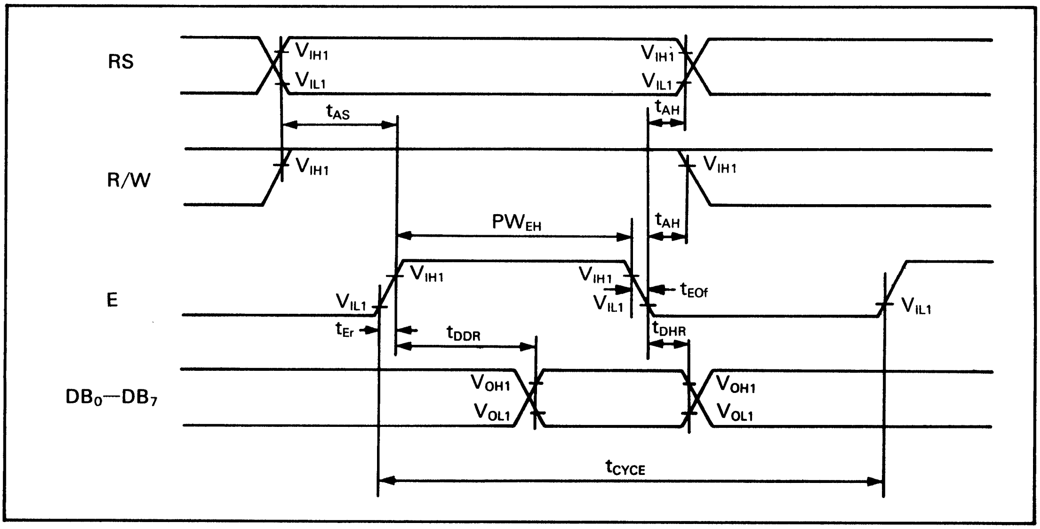


Figure 53. Bus Read Operation Sequence (Reading Data from HD66780 to MPU)

Interface signal with driver LSI HD44100H or HD66100F

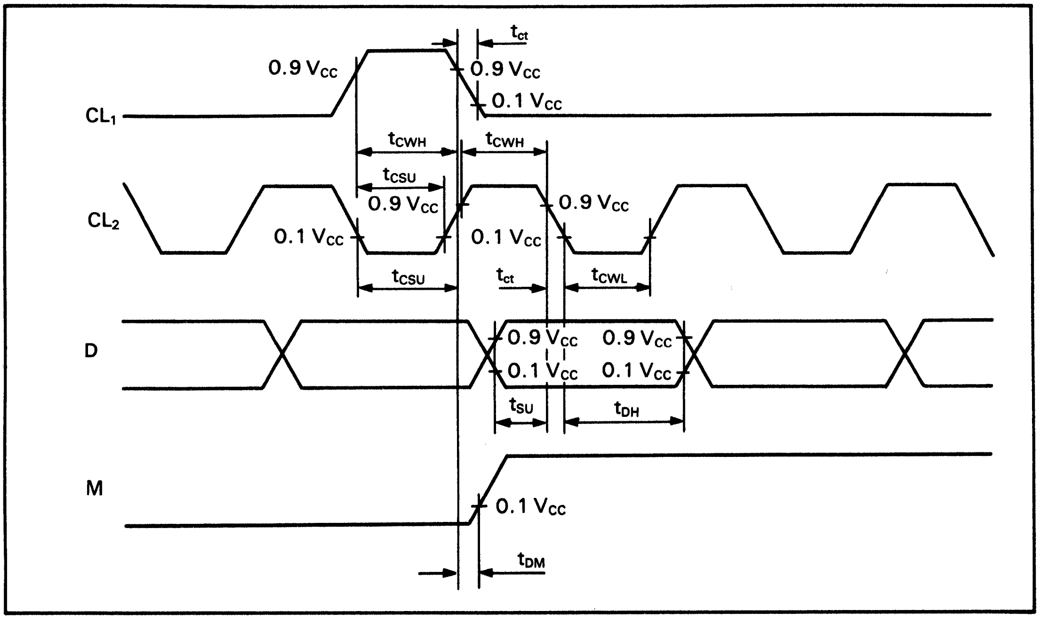


Figure 54. Sending Data to Driver LSI HD44100H or HD66100F

HD44102CH
(Dot Matrix Liquid Crystal Graphic Display Column Driver)

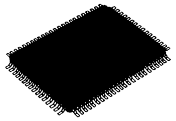
DESCRIPTION

The HD44102CH is a column (segment) driver for dot matrix liquid crystal graphic display systems, storing the display data transferred from a 4-bit or 8-bit micro-computer in the internal display RAM and generating dot matrix liquid crystal driving signals.

Each bit data of display RAM corresponds to ON/OFF of each dot of liquid crystal display to provide more flexible display

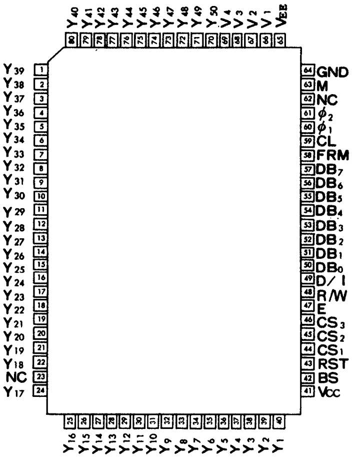
The HD44102CH is produced in the CMOS process. Therefore, the combination with a CMOS microcomputer can accomplish a portable battery drive equipment utilizing the liquid crystal display's lower power dissipation.

The combination of HD44102CH with the row (common) driver HD44103CH facilitates dot matrix liquid crystal graphic display system configuration.



(FP-80)

■PIN ARRANGEMENT

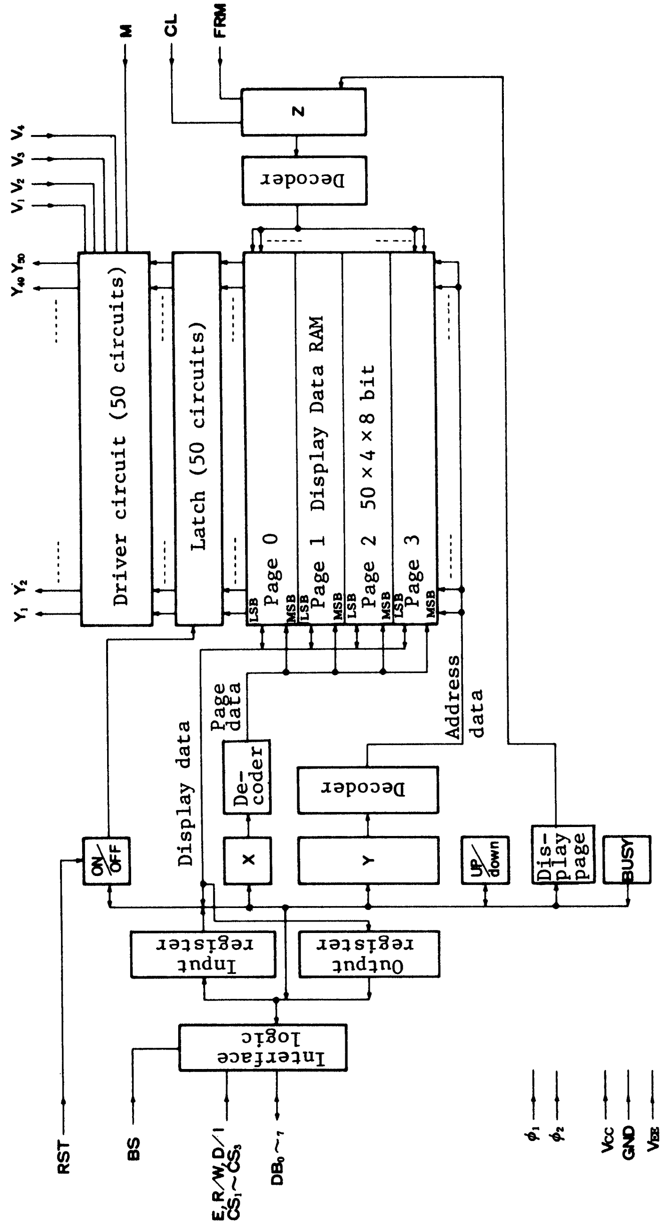


(TOP VIEW)

■ FEATURES

- Dot matrix liquid crystal graphic display column driver incorporating display RAM.
- Interfaceable to 4-bit or 8-bit MPU
- RAM data directly displayed by internal display RAM
  RAM bit data "1" ..... ON
  RAM bit data "0" ..... OFF
- Display RAM capacity ..... 50 × 8 × 4 (1600 bits)
- Internal liquid crystal display driver circuit (segment output) ..... 50 segment signal drivers
- Duty factor (can be controlled by external input waveform)
  Selectable duty factors 1/8, 1/12, 1/16, 1/24, 1/32
- Wide range of instruction functions
  Display Data Read/Write, Display ON/OFF, Set Address, Set Display Start Page, Set UP/DOWN, Read Status
- Low power dissipation
- Power supplies ..... V_{CC} 5V±10%, V_{EE} 0∿-5V
- CMOS process
- 80-pin flat plastic package

■BLOCK DIAGRAM



■TABLE OF PIN ASSIGNMENT

No.	Power supply, Clock	Input	Output	No.	Power supply Clock	Input	Output
1			Y39	41	Vcc		
2			Y38	42		BS	
3			Y37	43		RST	
4			Y36	44		CS1	
5			Y35	45		CS2	
6			Y34	46		CS3	
7			Y33	47		E	
8			Y32	48		R/W	
9			Y31	49		D/I	
10			Y30	50		DB$_0$	DB$_0$
11			Y29	51		DB$_1$	DB$_1$
12			Y28	52		DB$_2$	DB$_2$
13			Y27	53		DB$_3$	DB$_3$
14			Y26	54		DB$_4$	DB$_4$
15			Y25	55		DB$_5$	DB$_5$
16			Y24	56		DB$_6$	DB$_6$
17			Y23	57		DB$_7$	DB$_7$
18			Y22	58		FRM	
19			Y21	59		CL	
20			Y20	60	ϕ_1		
21			Y19	61	ϕ_2		
22			Y18	62	N. C.		
23	N. C.			63		M	
24			Y17	64	GND		
25			Y16	65	VEE		
26			Y15	66	V$_1$		
27			Y14	67	V$_2$		
28			Y13	68	V$_3$		
29			Y12	69	V$_4$		
30			Y11	70			Y50
31			Y10	71			Y49
32			Y9	72			Y48
33			Y8	73			Y47
34			Y7	74			Y46
35			Y6	75			Y45
36			Y5	76			Y44
37			Y4	77			Y43
38			Y3	78			Y42
39			Y2	79			Y41
40			Y1	80			Y40

(Note) N.C.: Nonconnection pin

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply voltage (1)	V_{CC}	−0.3 ∿ +7.0	V	1
Supply voltage (2)	V_{EE}	V_{CC}−13.5 ∿ V_{CC}+0.3	V	
Input voltage (1)	V_{T1}	−0.3 ∿ V_{CC}+0.3	V	1, 2
Input voltage (2)	V_{T2}	V_{EE}−0.3 ∿ V_{CC}+0.3	V	3
Operating temperature	T_{opr}	−20 ∿ +75	°C	
Storage temperature	T_{stg}	−55 ∿ +125	°C	

Note 1: Referred to GND=0.

Note 2: Applied to input terminals (except V1, V2, V3 and V4), and I/O common terminals.

Note 3: Applied to terminals V1, V2, V3 and V4.

■ ELECTRICAL CHARACTERISTICS

(V_{CC}=+5V±10%, GND=0V, V_{EE}=0∿−5.5V, Ta=−20∿+75°C) (Note 4)

Item	Symbol	Test condition	Min.	Typ	Max.	Unit	Note
Input "High" voltage(CMOS)	V_{IHC}		0.7×V_{CC}	-	V_{CC}	V	5
Input "Low" voltage (CMOS)	V_{ILC}		0	-	0.3×V_{CC}	V	5
Input "High" voltage (TTL)	V_{IHT}		2.0	-	V_{CC}	V	6
Input "Low" voltage (TTL)	V_{ILT}		0	-	+0.8	V	6
Output "High" voltage	V_{OH}	I_{OH}=−250μA	+3.5	-	-	V	7
Output "Low" voltage	V_{OL}	I_{OL}=+1.6mA	-	-	+0.4	V	7
Vi-Xj ON resistance	R_{ON}	V_{EE}=−5V±10%, Load current 100μA	-	-	7.5	kΩ	
Input leakage current (1)	I_{IL1}	V_{IN}=V_{CC}∿GND	-1	-	1	μA	8
Input leakage current (2)	I_{IL2}	V_{IN}=V_{CC}∿V_{EE}	-2	-	2	μA	9
Operating frequency	f_{CLK}	φ1,φ2 frequency	25	-	280	kHz	10
Dissipation current (1)	I_{CC1}	f_{clk}=200kHz frame= 65Hz during display	-	-	100	μA	11
Dissipation current (2)	I_{CC2}	Access cycle 1MHz at access	-	-	500	μA	12

Note 4: Specified within this range unless otherwise noted.

Note 5: Applied to M, FRM, CL, BS, RST, ϕ1, ϕ2.

Note 6: Applied to CS1 to CS3, E, D/I, R/W and DB0 to DB7.

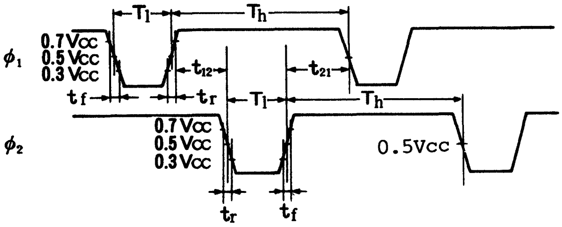
Note 7: Applied to DB0 to DB7.

Note 8: Applied to input terminals, M, FRM, CL, BS, RST, ϕ1, ϕ2, CS1 to CS3, E, D/I and R/W, and I/O common terminals DB0 to DB7 at high impedance.

Note 9: Applied to V1, V2, V3 and V4.

Note 10: ϕ1 and ϕ2 AC characteristics.

	Symbol	Min.	Typ	Max.	Unit
Duty	Duty	20	25	30	%
Fall time	t_f	-	-	100	ns
Rise time	t_r	-	-	100	ns
Phase difference time	t_{12}	0.8	-	-	μs
Phase difference time	t_{21}	0.8	-	-	μs
$T_l + T_h$		-	-	40	μs



$$f_{CLK} = \frac{1}{T_l + T_h}$$

$$Duty = \frac{T_l}{T_l + T_h} \times 100\ (\%)$$

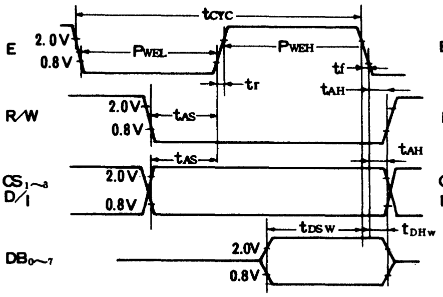
Note 11: Measured by V_{CC} terminal at no output load, at 1/32 duty, and frame frequency of 65Hz, in checker pattern display. Access from the CPU is stopping.

Note 12: Measured by V_{CC} terminal at no output load, 1/32 duty and frame frequency of 65Hz.

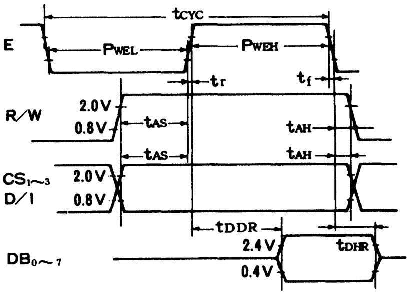
●INTERFACE AC CHARACTERISTICS

Item	Symbol	Min.	Typ	Max.	Unit	Note
E cycle time	t_{CYC}	1000	-	-	ns	13, 14
E high level width	PW_{EH}	450	-	-	ns	13, 14
E low level width	PW_{EL}	450	-	-	ns	13, 14
E rise time	t_r	-	-	25	ns	13, 14
E fall time	t_f	-	-	25	ns	13, 14
Address setup time	t_{AS}	140	-	-	ns	13, 14
Address hold time	t_{AH}	10	-	-	ns	13, 14
Data setup time	t_{DSW}	200	-	-	ns	13
Data delay time	t_{DDR}	-	-	320	ns	14, 15
Data hold time at write	t_{DHW}	10	-	-	ns	13
Data hold time at read	t_{DHR}	20	-	-	ns	14

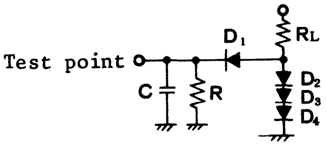
Note 13: At CPU write



Note 14: At CPU read



Note 15: DB0 to DB7 load circuits



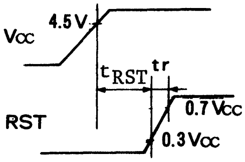
R_L = 2.4kΩ
R = 11kΩ
C = 130pF (including jig capacity)
Diodes D1 to D4 are all 1S2074Ⓗ

Note 16: Display OFF at initial power up.

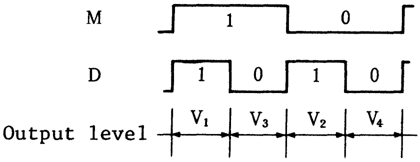
The HD44102CH can be placed in the display OFF state by setting terminal RST to "LOW" at initial power up.

No instruction other than the Read Status cannot be accepted while the RST is in the "Low" level.

	Symbol	Min.	Typ	Max.	Unit
Reset time	t_{RST}	1.0	-	-	µs
Rise time	t_r	-	-	200	ns



■TERMINAL FUNCTIONS DESCRIPTION

<table>
<tr><th>Signal name</th><th>Number of terminals</th><th>I/O</th><th>Function</th></tr>
<tr><td>Y1∿Y50</td><td>50</td><td>O</td><td>Liquid crystal display drive output.
Relationship among output level, M and display data (D):


M
1
0
D
1
0
1
0
Output level
V1
V3
V2
V4

</td></tr>
<tr><td>CS1∿CS3</td><td>3</td><td>I</td><td>Chip select<table>
<tr><th>CS1</th><th>CS2</th><th>CS3</th><th>State</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>Non-selected</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>Non-selected</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>Non-selected</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>Selected read/write enable</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>Selected write enable only</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>Selected write enable only</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>Selected write enable only</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>Selected read/write enable</td></tr>
</table></td></tr>
<tr><td>E</td><td>1</td><td>I</td><td>Enable
At write (R/W=L): Data of DB0 to DB7 is latched at the fall of E.
At read (R/W=H): Data appears at DB0 to DB7 while E is in "High" level.</td></tr>
</table>

<table>
<tr><th>Signal name</th><th>Number of terminals</th><th>I/O</th><th>Function</th></tr>
<tr><td>R/W</td><td>1</td><td>I</td><td>Read/Write
R/W=H: Data appears at DB0 to DB7 and can be read by the CPU when E=H and CS2, CS3="H".
R/W=L: DB0 to DB7 can accept input when CS2,CS3=H or CS1=H.</td></tr>
<tr><td>D/I</td><td>1</td><td>I</td><td>Data/Instruction
D/I=H: Indicates that the data of DB0 to DB7 is display data.
D/I=L: Indicates that the data of DB0 to DB7 is display control data.</td></tr>
<tr><td>DB0∿DB7</td><td>8</td><td>I/O</td><td>Data bus, Three-state I/O common terminal
<table>
<tr><th>E</th><th>R/W</th><th>CS1</th><th>CS2</th><th>CS3</th><th>State of DB0 to DB7</th></tr>
<tr><td>H</td><td>H</td><td>*</td><td>H</td><td>H</td><td>Output state</td></tr>
<tr><td>*</td><td>L</td><td>H</td><td>*</td><td>*</td><td rowspan="2">Input state, High impedance</td></tr>
<tr><td>*</td><td>L</td><td>*</td><td>H</td><td>H</td></tr>
<tr><td colspan="5">Others</td><td>High impedance</td></tr>
</table>
</td></tr>
<tr><td>M</td><td>1</td><td>I</td><td>Signal to convert liquid crystal display drive output to AC</td></tr>
<tr><td>CL</td><td>1</td><td>I</td><td>Display synchronous signal
At the rise of CL signal, the liquid crystal display drive signal corresponding to display data appears.</td></tr>
<tr><td>FRM</td><td>1</td><td>I</td><td>Display synchronous signal (frame signal)
This signal presets the 5-bit display line counter and synchronizes a common signal with the frame timing when the FRM signal becomes high.</td></tr>
<tr><td>ϕ1, ϕ2</td><td>2</td><td>I</td><td>2-phase clock signal for internal operation
The ϕ1 and ϕ2 clocks are used to perform the operations (input/output of display data and execution of instructions) other than display.</td></tr>
<tr><td>RST</td><td>1</td><td>I</td><td>Reset signal
The display disappears and Y address counter is set in the UP counter state by setting the RST signal to "Low" level. After releasing reset, the display OFF state and up mode is held until the state is changed by the instruction.</td></tr>
<tr><td>BS</td><td>1</td><td>I</td><td>Bus select signal
BS=L: DB0 to DB7 operate in 8-bit length.
BS=H: DB4 to DB7 are valid in 4-bit length only. 8-bit data is accessed twice in the high and low order.</td></tr>
</table>

Signal name	Number of terminals	I/O	Function
V1,V2, V3,V4	4		Power supply for liquid crystal display drive. V1 and V2: Selection voltage V3 and V4: Non-selection voltage
V_{CC} GND V_{EE}	3		Power supply. V_{CC}-GND: Power supply for internal logic V_{CC}-V_{EE}: Power supply for liquid crystal display drive circuit logic

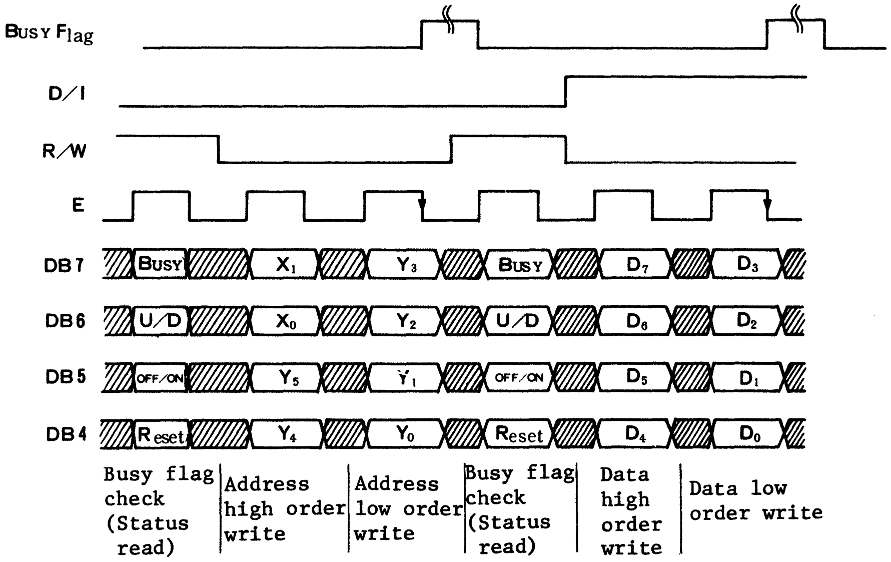
■FUNCTION OF EACH BLOCK

●Interface Logic

The HD44102CH can use the data bus in 4-bit or 8-bit word length to enable the interface to a 4-bit or 8-bit CPU.

(1) 4-bit mode (BS=H)

8-bit data is transferred twice for every 4 bits through the data bus when the BS signal is high. The data bus uses the high order 4 bits (DB4 to DB7). First, the high order 4 bits (DB4 to DB7 in 8-bit data length) is transferred and then the low order 4 bits (DB0 to DB3 in 8-bit data length).



(Note) Execute the instructions other than Status Read in 4-bit length each. The busy flag is set at the fall of the second E signal. The Status Read is executed once. After the execution of the Status Read, the first 4 bits are considered the high order 4 bits. Therefore, if the busy flag is checked after the transfer of the high order 4 bits, retransfer data from the higher order bits. No busy check is required in the transfer between the high and low order bits.

(2) 8-bit mode (BS=L)

If the BS signal is low, the 8 data buses (DB0 to DB7) are used for data transfer.

DB7 ... MSB (Most significant bit)
DB0 ... LSB (Least significant bit)

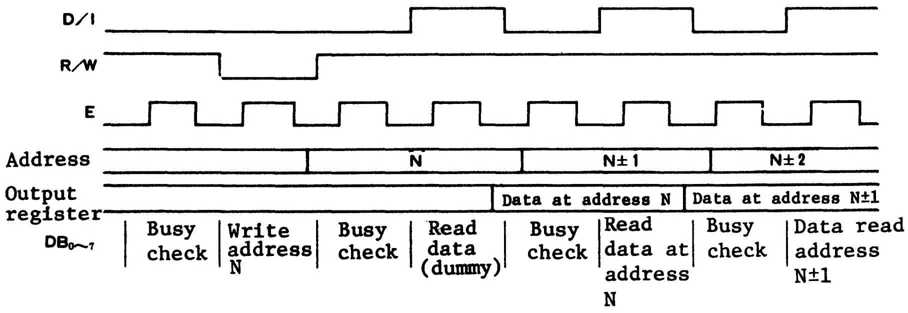
For AC timing, refer to (Note 12) to (Note 15) of "ELECTRICAL CHARACTERISTICS".

●Input Register

8-bit data is written into this register by the CPU. The instruction and display data are distinguished by the 8-bit data and D/I signal and then a given operation is performed. Data is received at the fall of E signal when the CS is in the select state and R/W is write state.

●Output Register

The output register holds the data read from the display data RAM. After display data is read, the display data at the address now indicated is set in this output register. After that, the address is increased or decreased by 1. Therefore, when an address is set, the correct data doesn't appear at the read of the first display data. The data at a specified address appears at the second read of data.



● X,Y Address Counter

The X,Y address counter holds an address for reading/writing display data RAM. An address is set in it by the instruction. The Y address register is composed of a 50-bit UP/DOWN counter. The address is increased or decreased by 1 by the read/write operation of display data. The UP/DOWN mode can be determined by the instruction or RST signal. The Y address register loops the values of 0 to 49 to count. The X address register has no count function.

●Display ON/OFF Flip Flop

This flip flop is set to ON/OFF state by the instruction or RST signal. In the OFF state, the latch of display data RAM output is held reset and the display data output is set to 0. Therefore, display disappears. In the ON state, the display data appears according to the data in the RAM and is displayed. The display data in the RAM is independent of the display ON/OFF.

●UP/DOWN Flip Flop

This flip flop determines the count mode of the Y address counter. In the UP mode, the Y address register is increased by 1. 0 follows 49. In the DOWN mode, the register is decreased by 1. 0 is followed by 49.

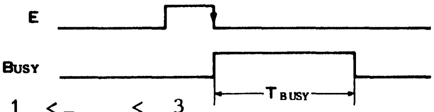
●Display Page Register

The display page register holds the 2-bit data that indicates a display start page. This value is preset to the high order 2 bits of the Z address counter by the FRM signal. This value indicates the value of the display RAM page displayed at the top of the screen.

●Busy Flag

After the instruction other than Status Read is accepted, the busy flag is set during its effective period, and reset when the instruction is not effective. The value can be read out on DB7 by the Status Read instruction.

The HD44102CH cannot accept any other instructions than the Status Read in the busy state. Make sure the busy flag is reset before the issue of instruction.



$$\frac{1}{F\phi} \leqq T_{BUSY} \leqq \frac{3}{F\phi}$$

Fϕ is ϕ1, ϕ2 frequency (half of HD44103CH oscillation frequency)

- Z Address Counter

The Z address counter is a 5-bit counter that counts up at the fall of CL signal and generates an address for outputing the display data synchronized with the common signal. 0 is preset to the low order 3 bits and a display start page to the high order 2 bits by the FRM signal.

- Latch

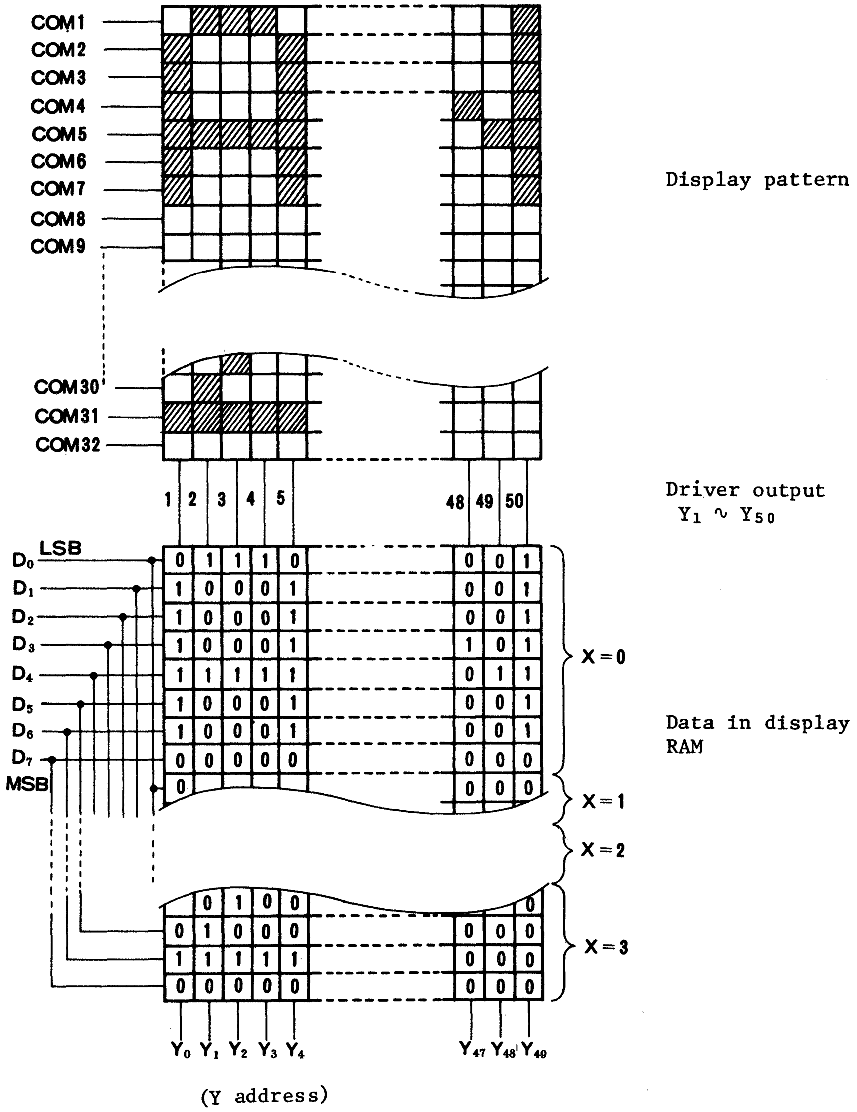
The display data from the display data RAM is latched at the rise of CL signal.

- Liquid Crystal Driver Circuit

Each of 50 driver circuits is a multiplex circuit composed of 4 CMOS switches. The combination of display data from latchs and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3 and V4 to be output.

- **Display RAM**

Relationship between Data in RAM and Display
(Display start page 0, 1/32 duty)



		Y0	Y1	Y2	Y3	Y4	Y47	Y48	Y49
X=0	D0	0	1	1	1	0	0	0	1
	D1	1	0	0	0	1	0	0	1
	D2	1	0	0	0	1	0	0	1
	D3	1	0	0	0	1	1	0	1
	D4	1	1	1	1	1	0	1	1
	D5	1	0	0	0	1	0	0	1
	D6	1	0	0	0	1	0	0	1
	D7	0	0	0	0	0	0	0	0
X=1	D0	0					0	0	0
X=3	D4		0	1	0	0			0
	D5	0	1	0	0	0	0	0	0
	D6	1	1	1	1	1	0	0	0
	D7	0	0	0	0	0	0	0	0

■DISPLAY CONTROL INSTRUCTIONS

(1) Read/Write Display Data

		MSB			DB				LSB	
R/W	D/I	7	6	5	4	3	2	1	0	
1	1	(Display data)								Read (CPU ← HD44102CH)
0	1	(Display data)								Write (CPU → HD44102CH)

Sends or receives data to or from the address of the display RAM specified in advance. However, the dummy read may be required for reading display data. Refer to the description of the output register in the FUNCTION OF EACH BLOCK.

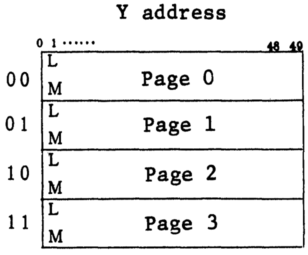
(2) Display ON/OFF

		MSB			DB				LSB	
R/W	D/I	7	6	5	4	3	2	1	0	
0	0	0	0	1	1	1	0	0	1	Display ON
0	0	0	0	1	1	1	0	0	0	Display OFF

Controls the ON/OFF of display. RAM data is not affected.

(3) Set X/Y Address

		MSB			DB				LSB
R/W	D/I	7	6	5	4	3	2	1	0
0	0	0	0						
0	0	0	1	Binary numbers of 0∿49					
0	0	1	0						
0	0	1	1						
		X address (page)		Y address (address)					



Display Data RAM

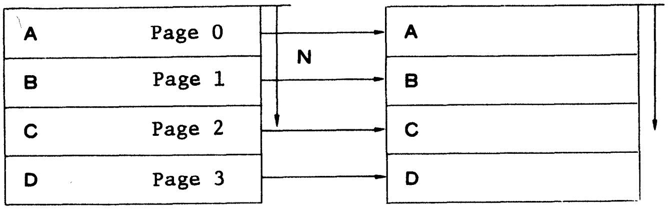
(4) Display Start Page

		MSB			DB				LSB	
R/W	D/I	7	6	5	4	3	2	1	0	
0	0	0	0	1	1	1	1	1	0	..... Refer to Fig. A.
0	0	0	1	1	1	1	1	1	0	..... Refer to Fig. B.
0	0	1	0	1	1	1	1	1	0	..... Refer to Fig. C.
0	0	1	1	1	1	1	1	1	0	..... Refer to Fig. D.
		Display start page								

Specifies a RAM page displayed at the top of the screen. Display is as shown in Figs. A, B, C and D respectively. When the display duty is more than 1/32 (For example, 1/24, 1/16), display begins at a page specified by the display start page only by the number of lines.

Start page = page 0

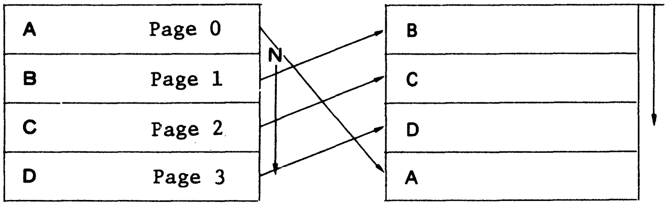
Fig. A



Displayed up to here when display duty is 1/N. (N=8, 12, 16, 24, 32)

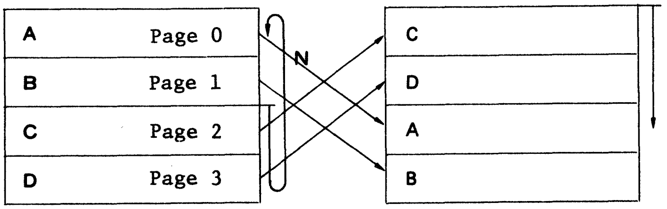
Start page = page 1

Fig. B



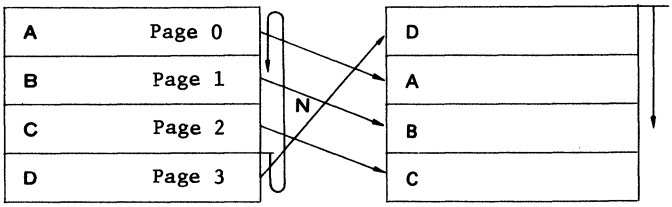
Start page = page 2

Fig. C



Start page = page 3

Fig. D



(5) UP/DOWN Set

		MSB			DB				LSB	
R/W	D/I	7	6	5	4	3	2	1	0	
0	0	0	0	1	1	1	0	1	1	UP mode
0	0	0	0	1	1	1	0	1	0	DOWN mode

Sets Y address register in the UP/DOWN counter mode.

(6) Status Read

		MSB			DB				LSB
R/W	D/I	7	6	5	4	3	2	1	0
1	0	BUSY	UP/DOWN	OFF/ON	RESET	0	0	0	0

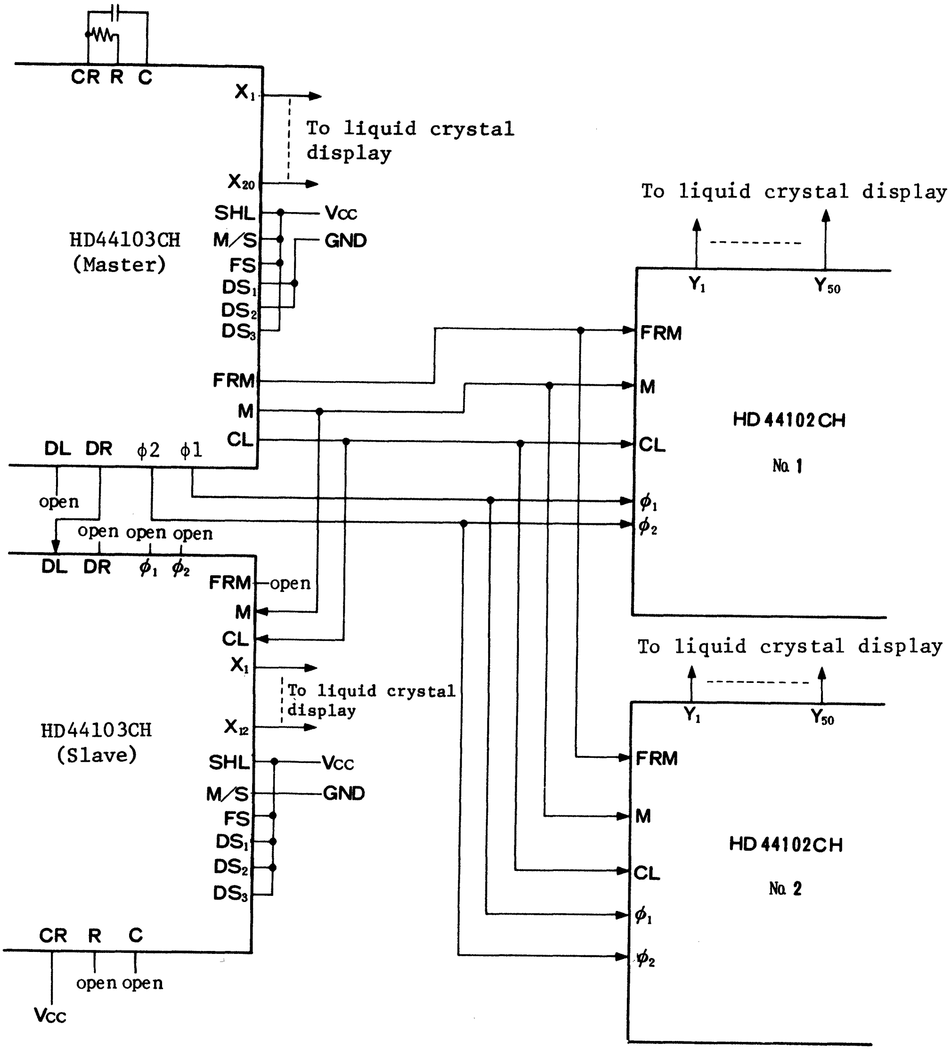
Goes to "1" when RST is in the reset state (Busy also goes to "1").
Goes to "0" when RST is in the operating state.

Goes to "1" in the display OFF state.
Goes to "0" on the display ON state.

Goes to "1" when address counter is in the UP mode.
Goes to "0" when address counter is in the DOWN mode.

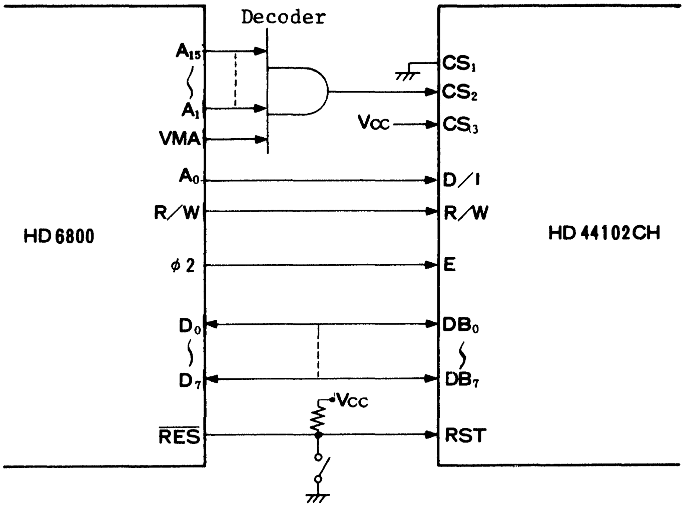
Goes to "1" while instructions (1) ∿ (5) are being executed.
During "1", none of instructions (1) ∿ (5) are accepted.

■CONNECTION BETWEEN LCD DRIVERS (EXAMPLE OF 1/32 DUTY)



■INTERFACE TO CPU

(1) Example of connection to HD6800



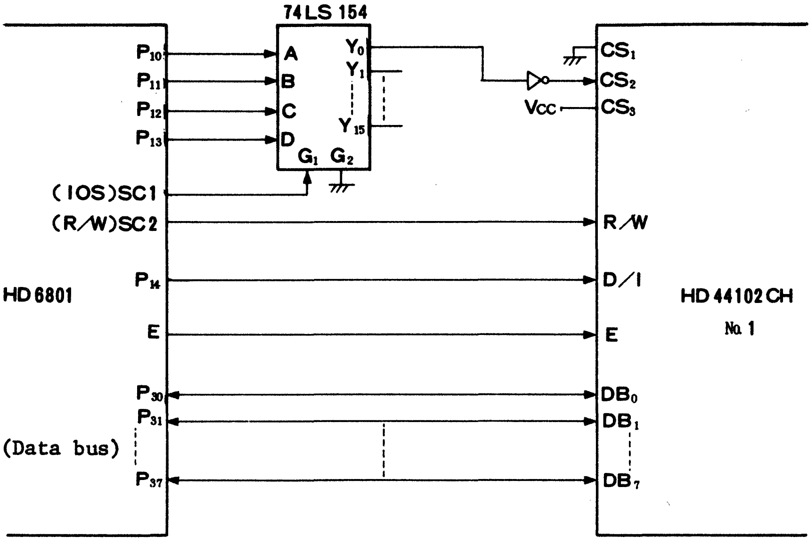
Example of Connection to HD6800 Series

In the decoder given in this example, the addresses of HD44102CH in the address space of HD6800 are:

Read/write of display data : $'FFFF'
Write of display instruction: $'FFFE'
Read of status : $'FFFE'

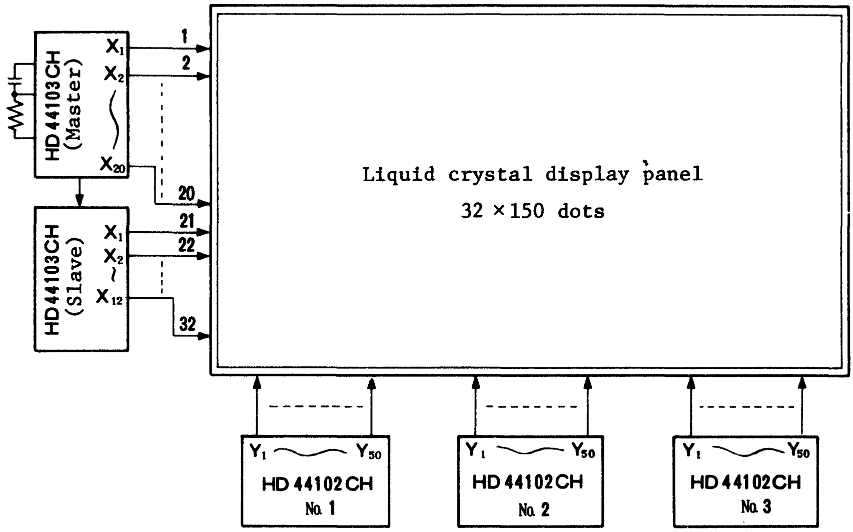
Thus, the HD44102CH can be controlled by reading/writing data at these addresses.

(2) Example of connection to HD6801

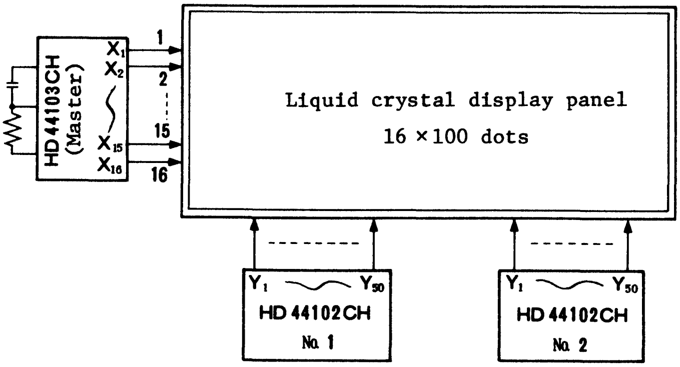


- The HD6801 is set to mode 5. P10 ∿P14 are used as output ports, and P30 ∿P37 are used as data buses.
- The 74LS154 is a 4-to-16 decoder that decodes 4 bits of P10 ∿P13 to select the chips.
- Therefore, the HD44102CH can be controlled by selecting the chips through P10 ∿P13 and specifying the D/I signal through P14 in advance, and later conducting memory Read or Write for external memory space ($0100 to $01FF) of HD6801. The IOS signal is output to SC1, and the R/W signal is output to SC2.
- For further details on HD6800 and HD6801, refer to each manual.

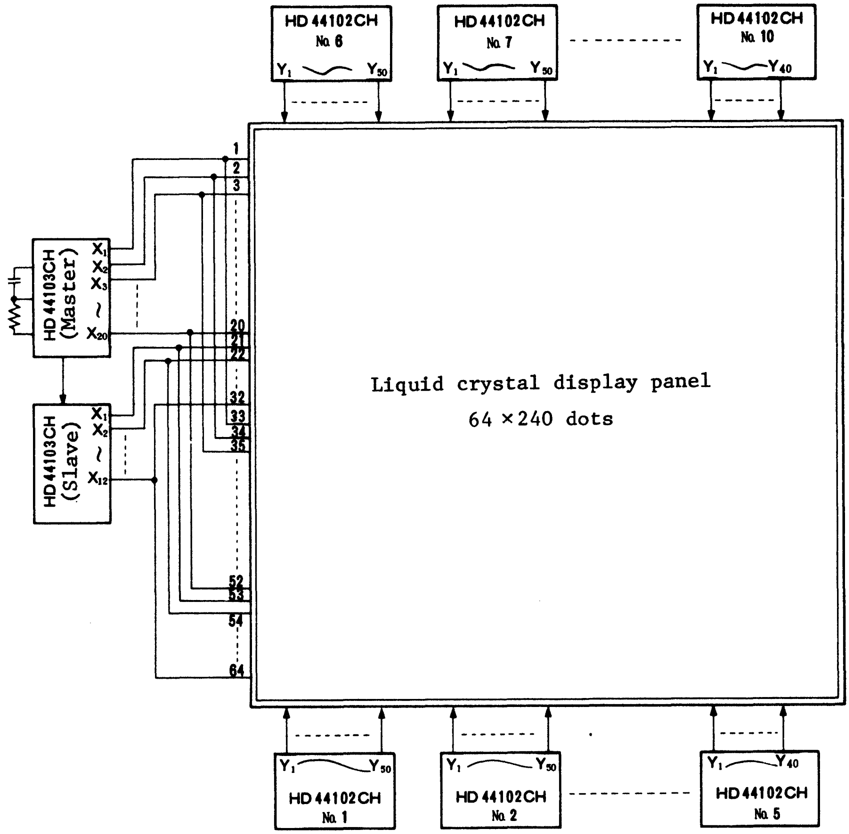
■CONNECTION TO LIQUID CRYSTAL DISPLAY



(a) Example of connection of 1/32 duty, 1-screen display



(b) Example of connection of 1/16 duty, 1-screen display



(c) Example of connection of 1/32 duty, 2-screen display

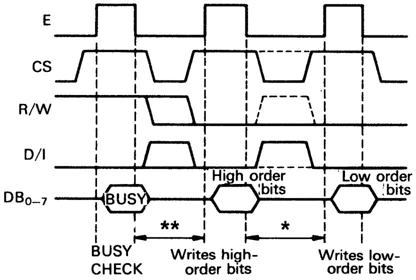
LIMITATIONS ON USING 4-BIT INTERFACE FUNCTION

The HD44102 usually transfers display control data and display data via 8-bit data bus. It also has the 4-bit interface function in which the HD44102 transfers 8-bit data by dividing it into the high-order 4 bits and the low-order 4-bits in order to reduce the number of wires to be connected. You should take an extra care in using the application with the 4-bit interface function since it has the following limitations.

LIMITATIONS

The HD44102 is designed to transfer the high-order 4-bits and the low-order 4-bits of data in that order after busy check. The LSI does not work normally if the signals are in the following state for the time period (indicated with (*) in the figure) from when the high-order 4 bits are written (or read) to when the low-order 4 bits are written (or read); R/W = high and D/I = low while the chip is being selected (CS1 = high and CS2 = CS3 = don't care, or CS1 = low and CS2 = CS3 = high).

EXAMPLE OF WRITING DISPLAY CONTROL INSTRUCTIONS



If the signals are in the limited state mentioned before for the time period indicated with (*) the LSI does not work normally. Please do not make the signals indicated with dotted lines simultaneously. As far as the time period indicated with (**), there is no problem.

The following explains how the malfunction is caused and gives the measures in application.

CAUSE

Busy check checks if the LSI is ready to accept the next instruction or display data, by reading the status register of the HD44102. And at the same time, it resets the internal counter counting the order of high-order data and low-order data. This function makes the LSI ready to accept only the high-order data after busy check. Strictly speaking, if R/W = high and D/I = low while the chip is being selected, the internal counter is reset and the LSI gets ready to accept high-order bits. Therefore, the LSI takes low-order data for high-order data if the state mentioned above exist in the interval between transferring high-order data and transferring low-order data.

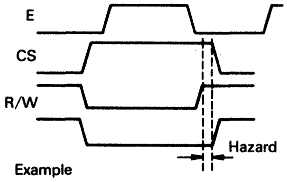
MEASURES IN APPLICATION

1) When HD44102 Controlled Via Port

When you control the HD44102 with the port of a single-chip microcomputer, you should take care of the software and observe the limitations strictly.

2) When HD44102 Controlled Via Bus

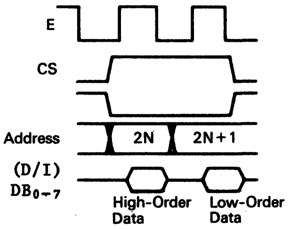
a) Malfunction Caused by Hazard



Writing High-Order Data

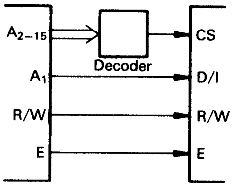
Hazard of input signals may also cause the phenomenon mentioned before. The phase shift at transition of the input signals may cause the malfunction and so the AC characteristics must be fully studied.

b) Using 2-Byte Instruction



Last 2 Machine Cycles of 2-Byte Instruction

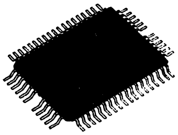
In the application with the HD6303, you can prevent malfunction by using 2-byte instructions such as STD and STX. This is because the high-order and low-order data are accessed in that order without a break in the last machine cycle of the instruction and R/W and D/I do not change in the meantime. However, you cannot use the least significant bit of the address signals as the D/I signal since the address for the second byte is added 1. And design the CS decoder so that the addresses for the HD44102 should be 2N and 2N+1, and that those addresses should be accessed when using 2-byte instructions. Fox example, in the figure shown following figure the address signal A_1 is used as D/I signal and A_2 - A_{15} are used for the CS decoder. Addresses 4N and 4N+1 are for instruction access and addresses 4N+2 and 4N+3 are for display data access.



HD44103CH
(Dot Matrix Liquid Crystal Graphic Display Common Driver)

DESCRIPTION

The HD44103CH is a common signal driver for dot matrix liquid crystal graphic display systems. It generates the timing signals required for display with its internal oscillator and supplies them to the column driver (HD44102CH) to control display, also automatically scanning the common signals of the liquid crystal according to the display duty. It can select 5 types of display duties ratio: 1/8, 1/12, 1/16, 1/24 and 1/32. 20 driver output lines are provided, and the impedance is low (500Ω max.) to enable a large screen to be driven.

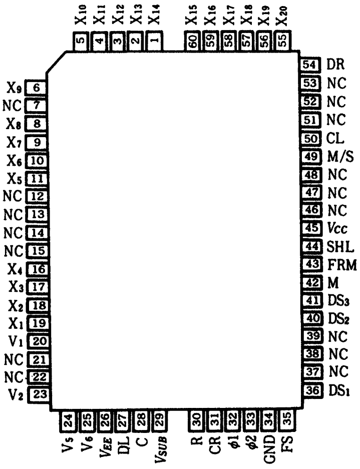


(FP-60)

■ FEATURES

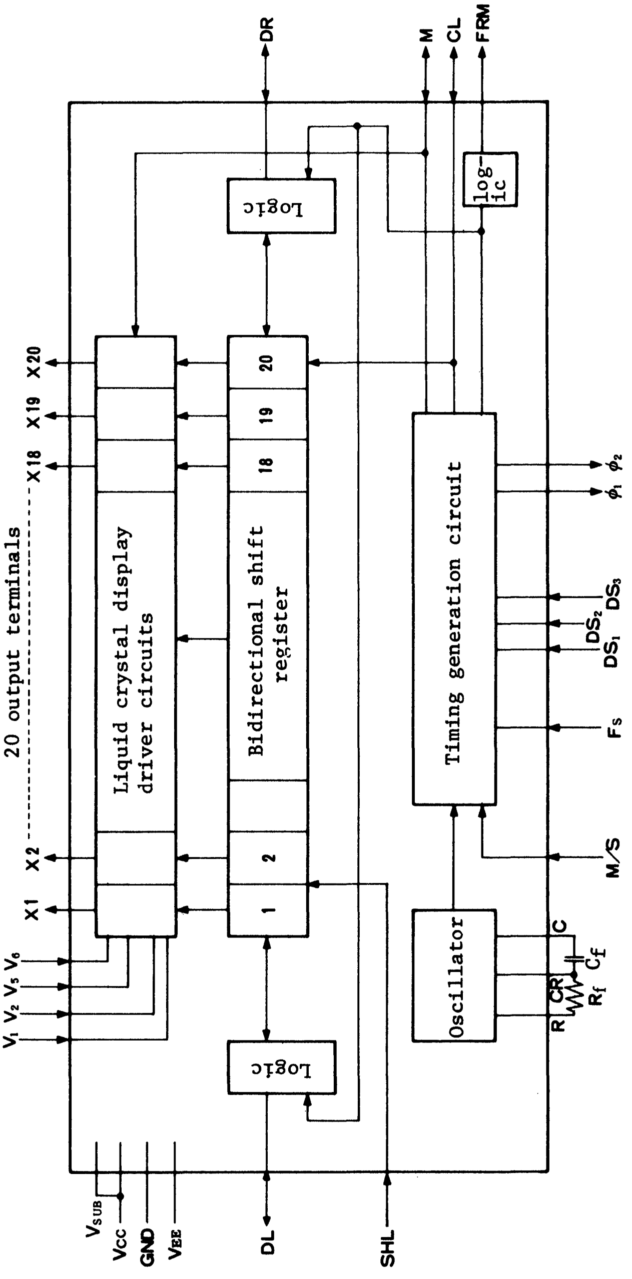
- Dot matrix liquid crystal graphic display common driver incorporating the timing generation circuit in it.
- Internal oscillator (Oscillation frequency can be selected by attaching an oscillation resistor and an oscillation capacity)
- Generates display timing signals.
- 20-bit bidirectional shift register for generating common signals
- 20 liquid crystal driver circuits with low output impedance
- Selectable display duty ratio: 1/8, 1/12, 1/16, 1/24, 1/32
- Low power dissipation
- Power supplies: V_{CC} ...5V±10%,
  V_{EE} ... 0 to -5.5V
- CMOS process
- 60-pin plastic flat package

■ PIN ARRANGEMENT



(TOP VIEW)

■BLOCK DIAGRAM



●TERMINAL ARRANGEMENT LIST

No.	Power supply, Clock	Input	Output	No.	Power supply, Clock	Input	Output
1			X 14	31	CR		
2			X 13	32			ϕ_1
3			X 12	33			ϕ_2
4			X 11	34	GND		
5			X 10	35		FS	
6			X 9	36		DS1	
7	N. C.			37	N. C.		
8			X 8	38	N. C.		
9			X 7	39	N. C.		
10			X 6	40		DS2	
11			X 5	41		DS3	
12	N. C.			42		M	M
13	N. C.			43			FRM
14	N. C.			44		SHL	
15	N. C.			45	V_{CC}		
16			X 4	46	N. C.		
17			X 3	47	N. C.		
18			X 2	48	N. C.		
19			X 1	49		M/S	
20	V_1			50		CL	CL
21	N. C.			51	N. C.		
22	N. C.			52	N. C.		
23	V_2			53	N. C.		
24	V_5			54		DR	DR
25	V_6			55			X 20
26	V_{EE}			56			X 19
27		DL	DL	57			X 18
28	C			58			X 17
29	V_{SUB}	Connect to V_{CC}.		59			X 16
30	R			60			X 15

(Note) N.C.: Unused terminal. Don't connect any wire to these terminals.
Connect V_{SUB} to V_{CC}.

●ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rated value	Unit	Note
Supply voltage (1)	V_{CC}	-0.3 ∿ +7.0	V	1
Supply voltage (2)	V_{EE}	V_{CC}-13.5 ∿ V_{CC}+0.3	V	14
Terminal voltage (1)	V_{T1}	-0.3 ∿ V_{CC}+0.3	V	1, 2
Terminal voltage (2)	V_{T2}	V_{EE}-0.3 ∿ V_{CC}+0.3	V	3
Operating temperature	T_{opr}	-20 ∿ +75	°C	
Storage temperature	T_{stg}	-55 ∿ +125	°C	

Note 1: Referred to GND=0.

Note 2: Applied to input terminals (except V1, V2, V5 and V6) and I/O common terminals.

Note 3: Applied to terminals V1, V2, V5 and V6.

Note 14: Connect a protection resistor of 220Ω±5% to V_{EE} power supply in series.

●ELECTRICAL CHARACTERISTICS

(V_{CC}=+5V±10%, GND=0V, V_{EE}=0 to -5.5V, Ta=-20 to +75°C) (Note 4)

Item	Symbol	Test condition	Min.	Typ	Max.	Unit	Note
Input "high" voltage	V_{IH}		0.7×V_{CC}	-	V_{CC}	V	5
Input "low" voltage	V_{IL}		0	-	0.3×V_{CC}	V	5
Output "high" voltage	V_{OH}	I_{OH}=-400μA	V_{CC}-0.4	-	-	V	6
Output "low" voltage	V_{OL}	I_{OL}=+400μA	-	-	0.4	V	6
Vi-Xj ON resistance	R_{ON}	V_{EE}=-5V±10%,Load current ±150μA	-	-	500	Ω	
Input leakage current (1)	I_{IL1}	V_{IN}=V_{CC}∿GND	-1	-	1	μA	7
Input leakage current (2)	I_{IL2}	V_{IN}=V_{CC}∿V_{EE}	-2	-	2	μA	8
Shift frequency	f_{SFT}	In slave mode	-	-	50	kHz	9
Oscillation frequency	f_{OSC}	R_f=68kΩ2% C_f=10pF±5%	300	430	560	kHz	10
External clock operating frequency	f_{cp}		50	-	560	kHz	
External clock duty	Duty		45	50	55	%	11
External clock rise time	t_{rcp}		-	-	50	ns	11
External clock fall time	t_{fcp}		-	-	50	ns	11

Item	Symbol	Test condition	Min.	Typ	Max.	Unit	Note
Dissipation power (master)	P_{w1}	CR oscillation= 430kHz	–	–	4.4	mW	12
Dissipation power (slave)	P_{w2}	Frame frequency =70Hz	–	–	1.1	mW	13

Note 4: Specified within this range unless otherwise noted.

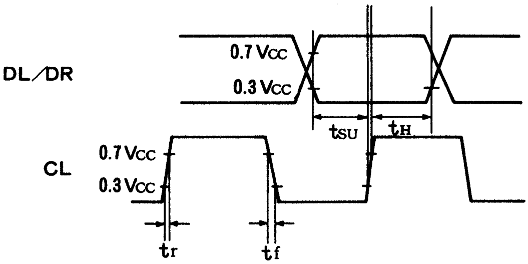
Note 5: Applied to CR, FS, DS1 to DS3, M, SHL, M/S, CL, DR and DL.

Note 6: Applied to DL, DR, M, FRM, CL, $\phi 1$ and $\phi 2$.

Note 7: Applied to input terminals CR, FS, DS1 to DS3, SHL and M/S, and I/O common terminals DL, DR, M and CL at high impedance.

Note 8: Applied to V1, V2, V5 and V6.

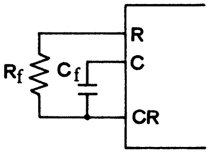
Note 9: Shift operation timing



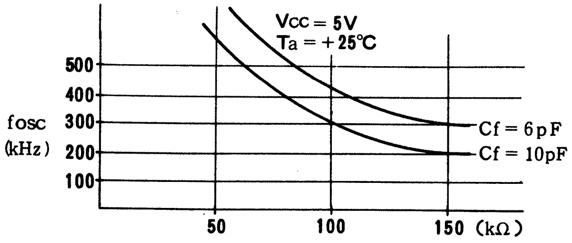
	min.	typ	max.	unit
t_{SU}	5	–	–	μs
t_H	5	–	–	μs
t_r	–	–	100	ns
t_f	–	–	100	ns

Note 10: Relationship between oscillation frequency and R_f/C_f

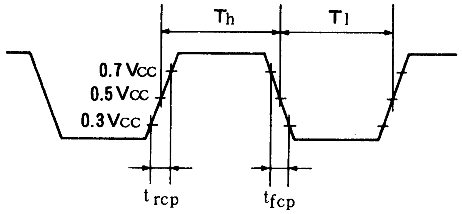
CR oscillator



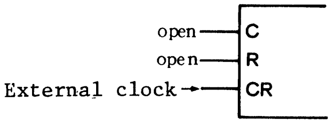
The values of Rf and Cf are typical values. The oscillation frequency varies with the mounting condition. Adjust oscillation frequency to a required value.



Note 11:



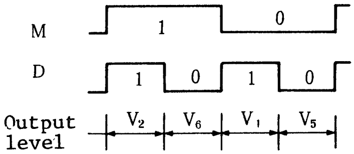
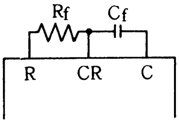
$$Duty = \frac{Th}{Th + Tl}$$



Note 12: Measured by V_{CC} terminal at output non-load of R_f=68kΩ±2% and C_f=10pF±5%, 1/32 duty in the master mode. Input terminals must be fixed at V_{CC} or GND while measuring.

Note 13: Measured by V_{CC} terminal at output non-load, 1/32 duty, frame frequency of 70Hz in the slave mode. Input terminals must be fixed at V_{CC} or GND while measuring.

- TERMINAL FUNCTIONS

Terminal name	Number of terminals	I/O	Function
X1∿X20	20	O	Liquid crystal display driver output. Relationship among output level, M and data (D) in shift register.  M 1 0 D 1 0 1 0 Output level V_2 V_6 V_1 V_5
CR, R, C	3		Oscillator  CR oscillator
M	1	I/O	Signal for converting liquid crystal display driver signal into AC Master: Output terminal Slave : Input terminal

<table>
<tr><th>Terminal name</th><th>Number of terminals</th><th>I/O</th><th>Function</th></tr>
<tr><td>CL</td><td>1</td><td>I/O</td><td>Shift register shift clock.
Master: Output terminal
Slave : Input terminal</td></tr>
<tr><td>FRM</td><td>1</td><td>O</td><td>Frame signal, Display synchronous signal</td></tr>
<tr><td>DS1∿DS3</td><td>3</td><td>I</td><td>Display duty ratio select.
<table>
<tr><th>Display duty ratio</th><th>1/24</th><th colspan="2">1/12</th><th>X</th><th>1/32</th><th colspan="2">1/16</th><th>1/8</th></tr>
<tr><td>DS1</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>DS2</td><td>L</td><td>L</td><td>H</td><td>H</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>DS3</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td></tr>
</table></td></tr>
<tr><td>FS</td><td>1</td><td>I</td><td>Frequency select.
The relationship between the frame frequency f_{FRM} and the oscillation frequency f_{OSC} is as follows:
FS="H": $f_{OSC} = 6144 \times f_{FPM}$ ··· (1)
FS="L": $f_{OSC} = 3072 \times f_{FRM}$ ··· (2)
Example 1) When FS="H", adjust Rf and Cf so that the oscillation frequency is approx. 430kHz if the frame frequency is 70Hz.
Example 2) When FS="L", adjust Rf and Cf so that the oscillation is approx. 215kHz, in order to obtain the same display waveforms as Example 1. When compared with Example 1, the power dissipation is reduced because of the operation at lower frequency. However, the operating clocks $\phi 1$ and $\phi 2$ supplied to the column driver have lower frequencies. Therefore, the access time of the column driver HD44102CH becomes longer.</td></tr>
<tr><td>DL, DR</td><td>2</td><td>I/O</td><td>Data I/O terminals of bidirectional shift register.</td></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>Shift direction select of bidirectional shift register.
<table>
<tr><th>SHL</th><th>Shift direction</th></tr>
<tr><td>H</td><td>DL → DR</td></tr>
<tr><td>L</td><td>DL ← DR</td></tr>
</table></td></tr>
</table>

Terminal name	Number of terminals	I/O	Function
M/S	1	I	Master/slave select. M/S="H": Master mode The oscillator and timing generation circuit operate to supply display timing signals to the display system. Each of I/O common terminals, DL, DR, M and CL is placed in the output state. M/S="L": Slave mode The timing generation circuit stops operating. The oscillator is not required. Connect terminal CR to V_{CC}. Open terminals C and R. One (determined by SHL) of DL and DR, and terminals M and CL are placed in the input state. Connect M, CL and one of DL and DR of the master to the respective terminals. Connect FD, DS1, DS2 and DS3 to V_{CC}. When display duty ratio is 1/8, 1/12 or 1/16, one HD44103CH is required. Use it in the master mode. When display duty ratio is 1/24 or 1/32, two HD44103CHs are required. Use the one in the master mode to drive common signals 1 to 20, and the other in the slave mode to drive common signals 21 to 24 (32).
$\phi 1$, $\phi 2$	2	O	Operating clock output terminals for HD44102CH. The frequencies of $\phi 1$ and $\phi 2$ become half of oscillation frequency.
V1, V2, V5, V6	4		Liquid crystal display driver level power supply V1 and V2: Selected level V5 and V6: Non-selected level
V_{CC} GND V_{EE}	3		Power supply. V_{CC}-GND: Power supply for internal logic V_{CC}-V_{EE}: Power supply for driver circuit logic

●BLOCK FUNCTIONS

Oscillator

The oscillator is a CR oscillator that attaches an oscillation resistor Rf and oscillation capacity Cf. The oscillation frequency varies with the values of Rf and Cf and the mounting conditions. Refer to ELECTRICAL CHARACTERISTICS (Note 10) to make proper adjustment.

Timing Generation Circuit

The timing generation circuit divides the signals from the oscillator and generates display timing signals (M, CL and FRM) and operating clock (ϕ1 and ϕ2) for HD44102CH according to the display duty ratio set by DS1 to DS3.
In the slave mode, this block stops operating. It is meaningless to set FS, DS1 to DS3. However, connect them to V_{CC} to prevent floating current.

Bidirectional Shift Register

This is a 20-bit bidirectional shift register. The shift direction is determined by the SHL. The data input from DL or DR performs a shift operation at the rise of shift clock CL.

Liquid Crystal Display Driver Circuit

Each of 20 driver circuits is a multiplex circuit composed of four CMOS switches. The combination of the data from the shift register with M signal allows one of the four liquid crystal display driver levels V1, V2, V5 and V6 to be transferred to the output terminals.

●APPLICATIONS

Refer to the applications of the HD44102CH.

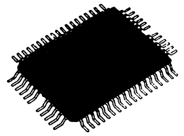
HD44105H (Dot Matrix Liquid Crystal Graphic Display Common Driver)

DESCRIPTION

The HD44105H is a common signal driver for LCD dot matrix graphic display systems. It generates the timing signals required for display with its internal oscillator and supplies them to the column driver (HD44102H) to control display, also automatically scanning the common signals of the liquid crystal according to the display duty.

It can select 7 types of display duty 1/8, 1/12, 1/16, 1/24, 1/32, 1/48 and 1/64.

It provides 32 driver output lines and the impedance is low (1kΩ max) enough to make a large screen driven.

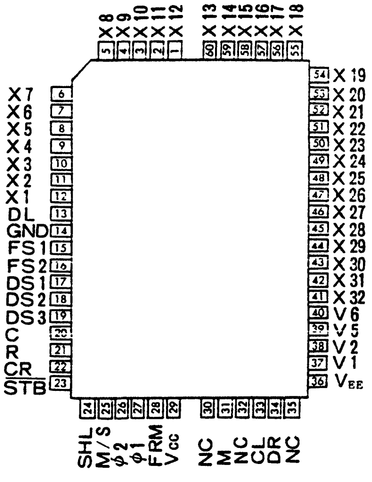


(FP-60)

■ FEATURES

- Dot matrix graphic display common driver including the timing generation circuit.
- Internal oscillator (Oscillation frequency is selectable by attaching an oscillation resistor and an oscillation capacity.)
- Generates display timing signals.
- 32-bit bidirectional shift register for generating common signals.
- 32 liquid crystal driver circuits with low impedance.
- Selectable display duty ratio : 1/8, 1/12, 1/16, 1/24, 1/32, 1/48, 1/64.
- Low power dissipation
- Power supplies : Vcc = +5V ± 10%
  VEE = 0 ∿ -5.5V
- CMOS process
- 60-pin flat plastic package

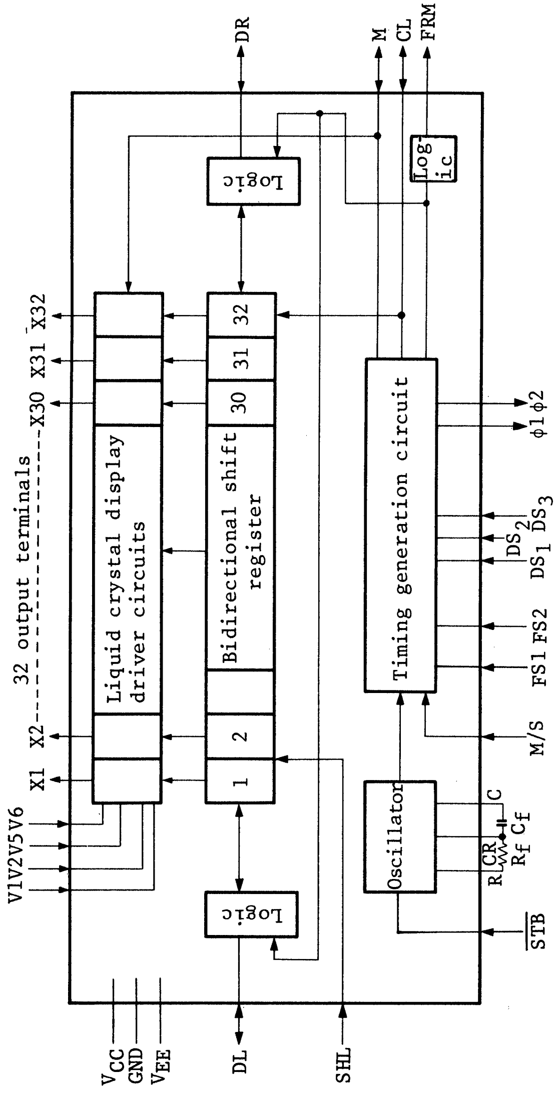
■ Pin Arrangement



(Top View)

Note) NCs show unused terminals. Don't connect any lines to them in using this LSI.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Ta = 25°C)

Item	Symbol	Ratings	Unit	Note
Supply voltage (1)	Vcc	-0.3 ∿ +7.0	V	1
Supply voltage (2)	VEE	Vcc-13.5 ∿ Vcc+0.3	V	
Terminal voltage (1)	VT1	-0.3 ∿ Vcc+0.3	V	1, 2
Terminal voltage (2)	VT2	VEE-0.3 ∿ Vcc+0.3	V	3
Operating temperature	Topr	-20 ∿ +75	°C	
Storage temperature	Tstg	-55 ∿ +125	°C	

(Note 1) Referred to GND = 0V.

(Note 2) Applied to input terminals (except for V1, V2, V5 and V6) and I/O common terminals.

(Note 3) Applied to terminals V1, V2, V5 and V6. Connect a protection resistor of 47Ω ± 10% to each terminal in series.

■ ELECTRICAL CHARACTERISTICS (Vcc=+5V±10%, GND=0V, VEE= 0 ∿ -5.5V, Ta= -20 ∿ +75°C) (Note 5)

Item	Symbol	Test Condition	min	typ	max	Unit	Note
Input "High" Voltage	V_{IH}		0.7×Vcc	-	Vcc	V	6
Input "Low" Voltage	V_{IL}		0	-	0.3×Vcc	V	6
Output "High" Voltage	V_{OH}	I_{OH}=-400μA	Vcc-0.4	-	-	V	7
Output "Low" Voltage	V_{OL}	I_{OL}=400μA	-	-	0.4	V	7
Vi-Xj ON Resistance	R_{ON}	V_{EE}=-5V±10%, Load Current ± 150μA	-	-	1000	Ω	
Input Leakage Current (1)	I_{IL1}	V_{IN}=Vcc ∿ GND	-1	-	1	μA	8
Input Leakage Current (2)	I_{IL2}	V_{IN}=Vcc ∿ V_{EE}	-5	-	5	μA	9
Shift Frequency	F_{SET}	in slave mode	-	-	50	kHz	10
Oscillation Frequency	f_{OSC}	Rf=68kΩ±2%, Cf=10pF±5%	300	430	560	kHz	11
External Clock Operating Frequency	f_{CP}		50	-	560	kHz	12
External Clock Duty	Duty		45	50	55	%	12
External Clock Rise Time	tr_{CP}		-	-	50	ns	12
External Clock Fall Time	tf_{CP}		-	-	50	ns	12
Dissipation Power (master)	P_{W1}	CR Oscillation, 430kHz	-	-	4.4	mW	13
Dissipation Power (Slave)	P_{W2}	Frame 70Hz	-	-	1.1	mW	14

(Note 5) Specified within this range unless otherwise noted.

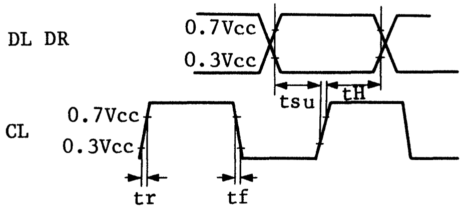
(Note 6) Applied to CR, FS1, FS2, DS1 to DS3, M, SHL, M/S, CL, DR, DL and $\overline{\text{STB}}$.

(Note 7) Applied to DL, DR, M, FRM, CL, $\phi 1$ and $\phi 2$.

(Note 8) Applied to input terminals CR, FS1, FS2, DS1 to DS3, SHL, M/S and $\overline{\text{STB}}$ and I/O common terminals DL, DR, M and CL at high impedance.

(Note 9) Applied to V1, V2, V5 and V6.

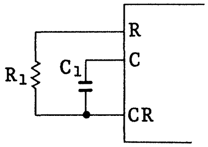
(Note 10) Shift operation timing.



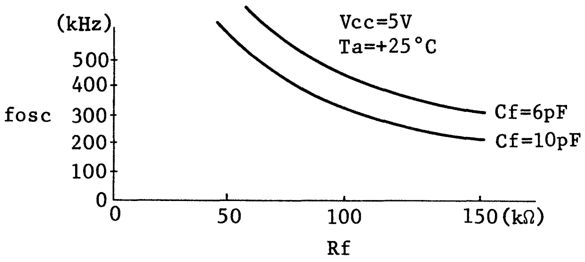
	min	typ	max	Unit
tsu	5	–	–	μs
t_H	5	–	–	μs
tr	–	–	100	ns
tf	–	–	100	ns

(Note 11) Relation between oscillation frequency and RF, Cf.

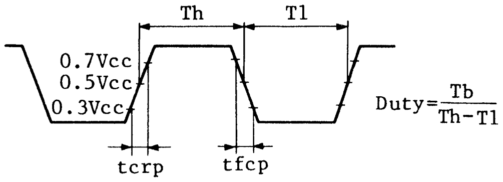
Connection

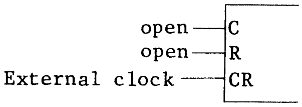


The values of Rf and Cf are typical values. The oscillation frequency varies with the mounting condition. Adjust oscillation frequency to a required value.



(Note 12)

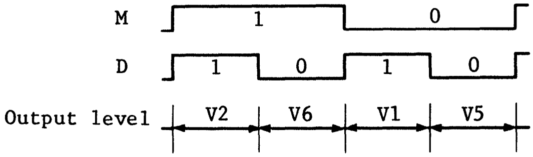
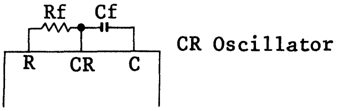




(Note 13) Measured by Vcc terminal at output non-load of Rf=68kΩ±2% and Cf=10pF±5%, and 1/32 duty in the master mode.
Input terminals are connected to Vcc or GND.

(Note 14) Measured by Vcc terminal at output non-load, 1/32 duty and frame frequency of 70Hz in the slave mode.
Input terminals are connected to Vcc or GND.

■ TERMINAL FUNCTION

<table>
<tr><th>Terminal Name</th><th>Number of terminals</th><th>I/O</th><th>Function</th></tr>
<tr><td>X1 ∿ X32</td><td>32</td><td>O</td><td>Liquid crystal display driver output.
Relation among output level, M and data(D) in shift register.
 </td></tr>
<tr><td>CR,R,C</td><td>3</td><td></td><td>Oscillator.
 </td></tr>
<tr><td>M</td><td>1</td><td>I/O</td><td>Signal for converting liquid crystal display driver signal into AC.
Master: Output terminal
Slave : Input terminal</td></tr>
<tr><td>CL</td><td>1</td><td>I/O</td><td>Shift register shift clock.
Master: Output terminal
Slave : Input terminal</td></tr>
<tr><td>FRM</td><td>1</td><td>O</td><td>Frame signal, Display synchronous signal</td></tr>
<tr><td>DS1∿DS3</td><td>3</td><td>I</td><td>Display duty ratio select.
<table>
<tr><td>Display duty ratio</td><td>1/8</td><td>1/16</td><td>1/32</td><td>1/64</td><td>-</td><td>1/12</td><td>1/24</td><td>1/48</td></tr>
<tr><td>DS1</td><td>L</td><td>L</td><td>H</td><td>H</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>DS2</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>DS3</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td></tr>
</table></td></tr>
<tr><td>FS1∿FS2</td><td>2</td><td>I</td><td>Selects frequency.
The relation between the frame frequency f_{FRM} and the oscillation frequency f_{OSC} is as follows.
<table>
<tr><td>FS1</td><td>FS2</td><td>f_{OSC}(kHz)</td><td>f_{FRM}(Hz)</td><td>f_M(Hz)</td><td>f_{CP}(kHz)</td></tr>
<tr><td>L</td><td>L</td><td>107.5</td><td>70</td><td>35</td><td>53.8</td></tr>
<tr><td>H</td><td>L</td><td>107.5</td><td>70</td><td>35</td><td>53.8</td></tr>
<tr><td>L</td><td>H</td><td>215.0</td><td>70</td><td>35</td><td>107.5</td></tr>
<tr><td>H</td><td>H</td><td>430.0</td><td>70</td><td>35</td><td>215.0</td></tr>
</table>
f_{OSC}: Oscillation frequency
f_{FRM}: Frame frequency
f_M : M signal frequency
f_{CP} : Frequencies of $\phi1$ and $\phi2$</td></tr>
</table>

<table>
<tr><th>Terminal Name</th><th>Number of terminals</th><th>I/O</th><th>Function</th></tr>
<tr><td>$\overline{STB}$</td><td>1</td><td>I</td><td>Input terminal for testing.
Connect this terminal to Vcc.</td></tr>
<tr><td>DL, DR</td><td>2</td><td>I/O</td><td>Data I/O terminals of bidirectional shift register.</td></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>Selects shift direction of bidirectional shift register.<table><tr><th>SHL</th><th>Shift direction</th></tr><tr><td>H</td><td>DL → DR</td></tr><tr><td>L</td><td>DL ← DR</td></tr></table></td></tr>
<tr><td>M/S</td><td>1</td><td>I</td><td>Selects Master/Slave.
M/S='H': Master mode
The oscillator and timing generation circuit operate to supply display timing signals to the display system. Each of I/O common terminals, DL, DR, M and CL is in the output state.
M/S='L': Slave mode
The timing generation circuit stops operating. The oscillator is not required. Connect terminal CR to Vcc. Open terminals C and R. One (determined by SHL) of DL and DR, and terminals M and CL are in the input state. Connect M, CL and one of DL and DR of the master to the respective terminals. Connect FS1, FS2, DS1, DS2, DS3, $\overline{STB}$ to Vcc.
When display duty ratio is 1/8, 1/12, 1/16, 1/24, 1/32, one HD44105H is required. Use it in the master mode.
When display duty ratio is 1/48, 1/64, two HD44105Hs are required. Use one in the master mode to drive common signals 1 to 32, and another in the slave mode to drive common signals 33 to 48(64).</td></tr>
<tr><td>ϕ1, ϕ2</td><td>2</td><td>O</td><td>Operating clock output terminals for HD44102CH. The frequencies of ϕ1 and ϕ2 are half of oscillation frequency.</td></tr>
<tr><td>V1, V2,
V5, V6</td><td>4</td><td></td><td>Liquid crystal display driver level power supply
V1 and V2 : Selected level
V5 and V6 : Non-selected level</td></tr>
<tr><td>V_{CC}, GND
V_{EE}</td><td>3</td><td></td><td>Power supply
V_{CC} - GND : Power supply for internal logic.
V_{CC} - V_{EE} : Power supply for driver circuit logic.</td></tr>
</table>

■ BLOCK FUNCTIONS

- Oscillator

A CR oscillator that attaches an oscillation resistor Rf and an oscillation capacity Cf. The oscillation frequency varies with the values of Rf and Cf and the mounting conditions. Refer to ELECTRICAL CHARACTERISTICS (Note 11) to make proper adjustment.

- Timing Generation Circuit

This circuit divides the signals from the oscillator and generates display timing signals (M, CL and FRM) and operating clock ($\phi 1$ and $\phi 2$) for HD44102CH according to the display duty ratio set by DS1 to DS3. In the slave mode, this block stops operating. It is meaningless to set FS1, FS2 and DS1 to DS3. However, connect them to Vcc to prevent floating current.

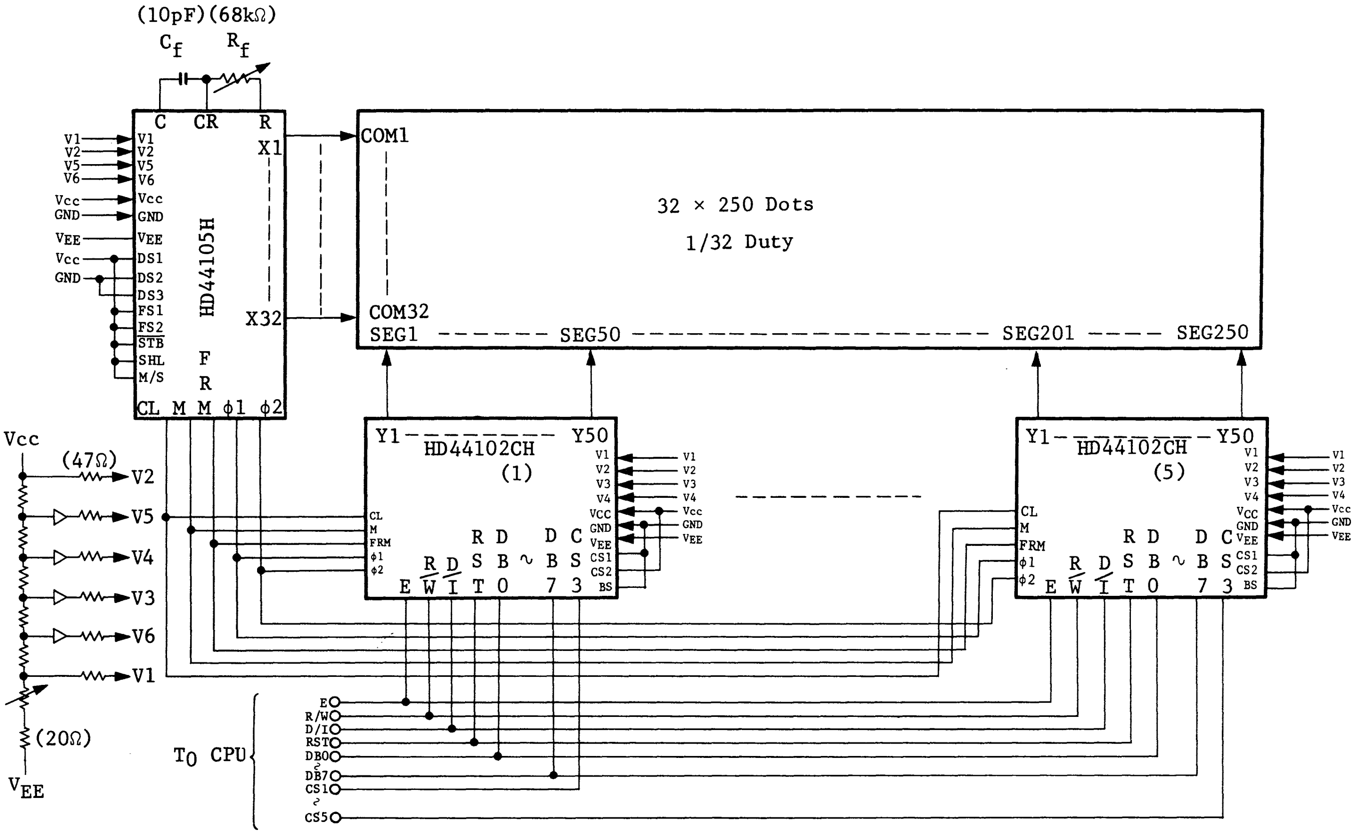
- Bidirectional Shift Register

A 32-bit bidirectional shift register. The shift direction is determined by the SHL. The data input from DL or DR performs a shift operation at the rise of shift clock CL.

- Liquid Crystal Display Driver Circuit

Each of 32 driver circuits is a multiplex circuit composed of four CMOS switches. The combination of the data from the shift register with M signal allows one of the four liquid crystal display driver levels V1, V2, V5 and V6 to be transferred to the output terminals.

■ Connection between HD44105H and HD44102CH

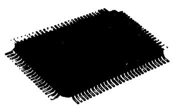


HD61100A
(LCD Driver with 80-Channel Output)

DESCRIPTION

The HD61100A is a driver LSI for liquid crystal display systems. It receives serial display data from a micro computer or a display control LSI, HD61830, etc., and generates liquid crystal driving signals.

It has liquid crystal driving outputs which corresponds to internal 80-bit flip flops. Both static drive and dynamic drive are possible according to the combination of transfer clock frequency and latch clock frequency.



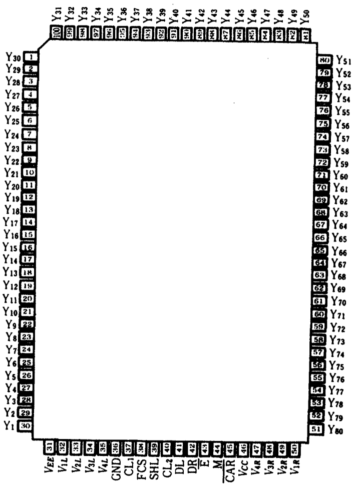
(FP-100)

■ FEATURES

- Liquid crystal display driver with serial/parallel conversion function.
- Internal liquid crystal display driver
  ...... 80 drivers
- Display duty

  Any duty is selectable according to combination of transfer clock and latch clock.
- Data transfer rate .... 2.5 MHz max
- Power supply
  - Vcc - +5V±10% (Internal logic)
  - VEE - 0 ∿ -11.5V (Liquid crystal display driver circuit)
- Liquid crystal driving level....17.0V max.
- CMOS process
- 100-pin flat plastic package (FP-100)

■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply voltage (1)	V_{CC}	-0.3 to +7.0	V	2
Supply voltage (2)	V_{EE}	Vcc-19.0 to Vcc+0.3	V	
Terminal voltage (1)	V_{T1}	-0.3 to Vcc +0.3	V	2, 3
Terminal voltage (2)	V_{T2}	VEE-0.3 to Vcc+0.3	V	4
Operating temperature	Topr	-20 to +75	°C	
Storage temperature	Tstg	-55 to +125	°C	

(Note 1) LSI's may be permanently destoryed if being used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the limits of electrical characteristics, because using beyond these conditions may cause malfunction and poor reliability.

(Note 2) All voltage values are referred to GND=0V.

(Note 3) Applies to input terminals, FCS, SHL, CL1, CL2, DL, DR, $\overline{E}$ and M.

(Note 4) Applies to V_{1L} V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L} and V_{4R}. Must maintain

$V_{CC} \geqq V_{1L} = V_{1R} \geqq V_{3L} = V_{3R} \geqq V_{4L} = V_{4R} \geqq V_{2L} = V_{2R} \geqq V_{EE}$.

Connect a protection resistor of 15Ω±10% to each terminals in series.

■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS

(Vcc=5V±10%, GND=0V, V_{EE}=0∿-11.5V, Ta=-20∿+75°C)

Item	Symbol	Test Condition	Min	Typ	Max	Unit	Note
Input "High" voltage	V_{IH}		0.7xV_{CC}	-	V_{CC}	V	1
Input "Low" voltage	V_{IL}		-	-	0.3×V_{CC}	V	1
Output "High" voltage	V_{OH}	I_{OH}=-400μA	V_{CC}-0.4	-	-	V	2
Output "Low" voltage	V_{OL}	I_{OL}=+400μA	-	-	0.4	V	2
Driver ON Resistance	R_{ON}	VEE=-10V, Load current= 100μA	-	-	7.5	kΩ	3
Input Leakage Current	I_{IL1}	V_{IN}=0 to V_{CC}	-1	-	+1	μA	1
Input Leakage Current	I_{IL2}	V_{IN}=V_{EE} to V_{CC}	-2	-	+2	μA	4
Dissipation Current(1)	I_{GND}		-	-	1.0	mA	5
Dissipation Current(2)	I_{EE}		-	-	0.1	mA	5

(Note 1) Applies to CL1, CL2, FCS, SHL, $\overline{E}$, M, DL and DR.

(Note 2) Applies to DL, DR and $\overline{CAR}$.

(Note 3) Applies to Y1 ∿ Y80.

(Note 4) Applies to V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L} and V_{4R}.

(Note 5) Specified when display data is transfered under following conditions.

CL2 frequency f_{CP2} = 2.5MHz (data transfer rate)
CL1 frequency f_{CP1} = 4.48kHz (data latch frequency)
M frequency f_M = 30Hz (frame frequency/2)

Specified when V_{IH}=V_{CC}, V_{IL}=GND and no load on outputs.

I_{GND} : currents between V_{CC} and GND.

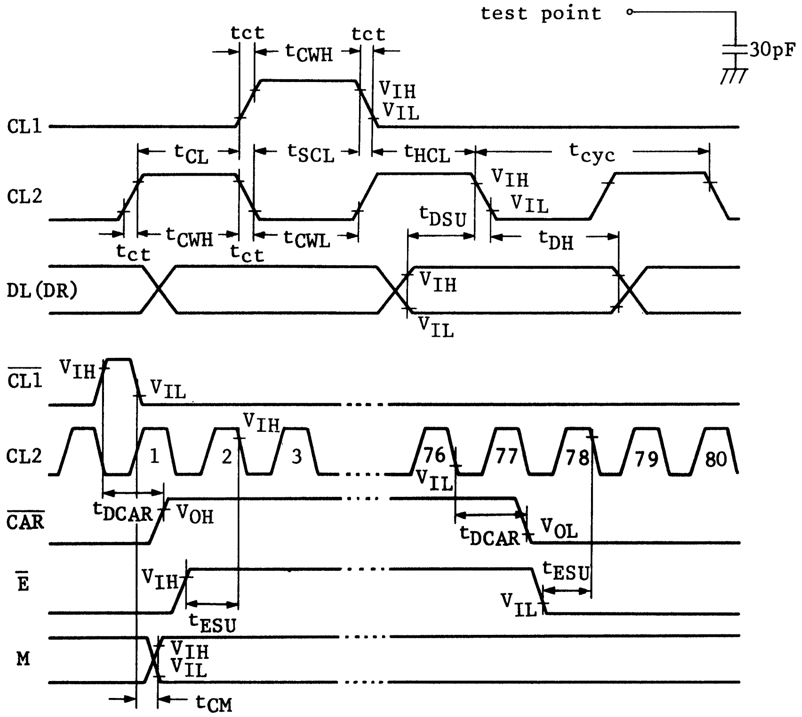
I_{EE} : currents between V_{CC} and V_{EE}.

- AC CHARACTERISTICS

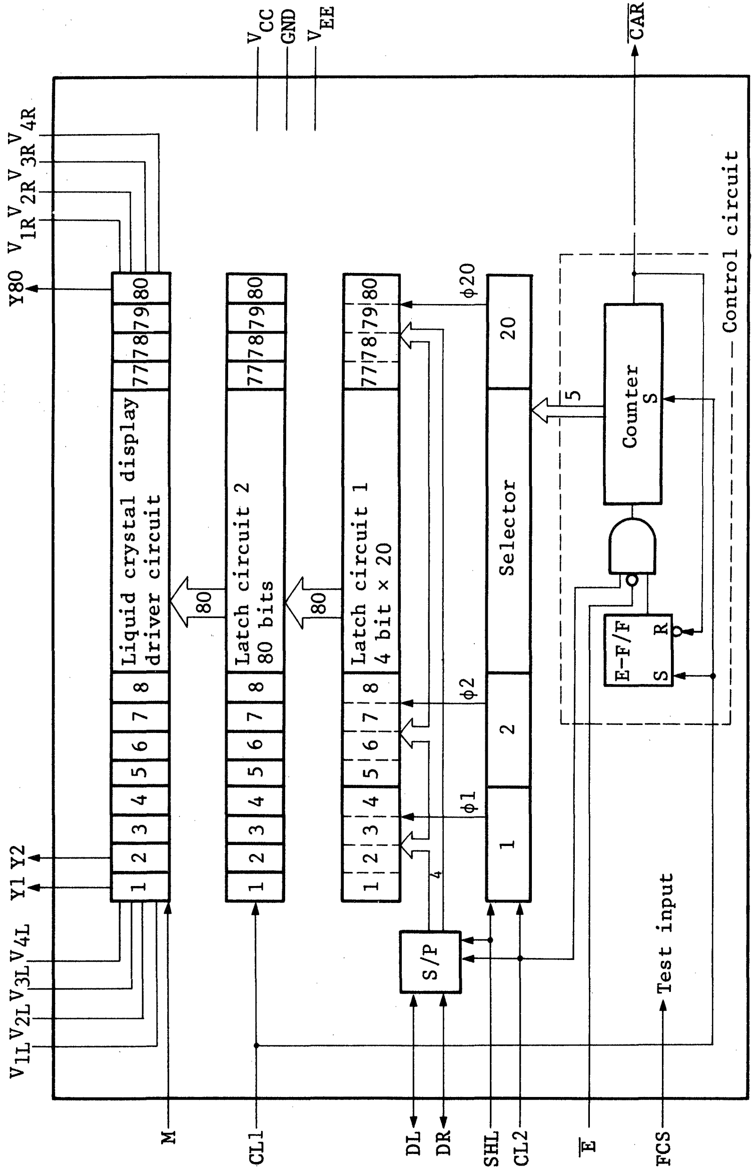
(Vcc=5V±10%, GND=0V, V_{EE}=0V∿-11.5V, Ta=-20∿+75°C)

Item	Symbol	Test Condition	Min	Typ	Max	Unit	Note
Clock cycle time	t_{CYC}		400	-	-	ns	
Clock high level width	t_{CWH}		150	-	-	ns	
Clock low level width	t_{CWL}		150	-	-	ns	
Clock setup time	t_{SCL}		100	-	-	ns	
Clock hold time	t_{HCL}		100	-	-	ns	
Clock rise/fall time	t_{Ct}		-	-	30	ns	
Clock phase different time	t_{CL}		100	-	-	ns	
Data setup time	t_{DSu}		80	-	-	ns	
Data hold time	t_{DH}		100	-	-	ns	
E setup time	t_{ESu}		200	-	-	ns	
Output delay time	t_{DCAR}		-	-	300	ns	1
M phase difference time	t_{CM}		-	-	300	ns	

(Note 1) The following load circuits are connected for specification:



■ BLOCK DIAGRAM



■ BLOCK FUNCTION

- Liquid Crystal Display Driver Circuit

The combination of the data from the latch circuit 2 and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3 and V4 to be output.

- 80-bit Latch Circuit 2

The data from latch circuit 1 is latched at the fall of CL1 and output to liquid crystal display driver circuit.

- S/P

Serial/Parallel conversion circuit which converts 1-bit data into 4-bit data. When SHL is "L" level, data from DL is converted into 4-bit data and transferred to the latch circuit 1. In this case, don't connect any lines to terminal DR which is in the output status.
When SHL is "H" level, input data from terminal DR without connecting any lines to terminal DL.

- 80-bit Latch Circuit 1

The 4-bit data is latched at ϕ1 ∿ ϕ20 and output to latch circuit 2. When SHL is "L" level, the data from DL are latched one in order of 1→2→3 ... →80 of each latch. When SHL is "H" level, they are latched in a reverse order (80→79→78 ... →1).

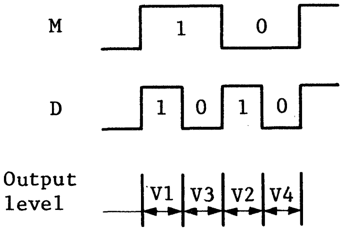
- Selector

The selector decodes output signals from the counter and generates latch clock ϕ1 to ϕ20. When the LSI is not active, ϕ1 ∿ ϕ20 are not generated, so the data at latch circuit 1 is stored even if input data (DL, DR) changes.

- Control Circuit

Controls operation : When E-F/F (enable F/F) indicates "1", S/P conversion is started by inputting "L" level to $\overline{\text{E}}$. After 80-bit data has been all converted, $\overline{\text{CAR}}$ output turns into "L" level and E-F/F is reset to "0", and consequently the conversion stops. E-F/F is RS flip-flop circuit which gives priority to SET over RESET and is set at "H" level of CL1.
Counter consists of 7 bits, and the output signals of upper 5 bits are transferred to the selector. $\overline{\text{CAR}}$ signal turns into "H" level at the rise of CL1 and the number of bit which can be S/P-converted increases by connecting $\overline{\text{CAR}}$ terminal with $\overline{\text{E}}$ terminal of the next HD61100A.

■ TERMINAL FUNCTIONS DESCRIPTION

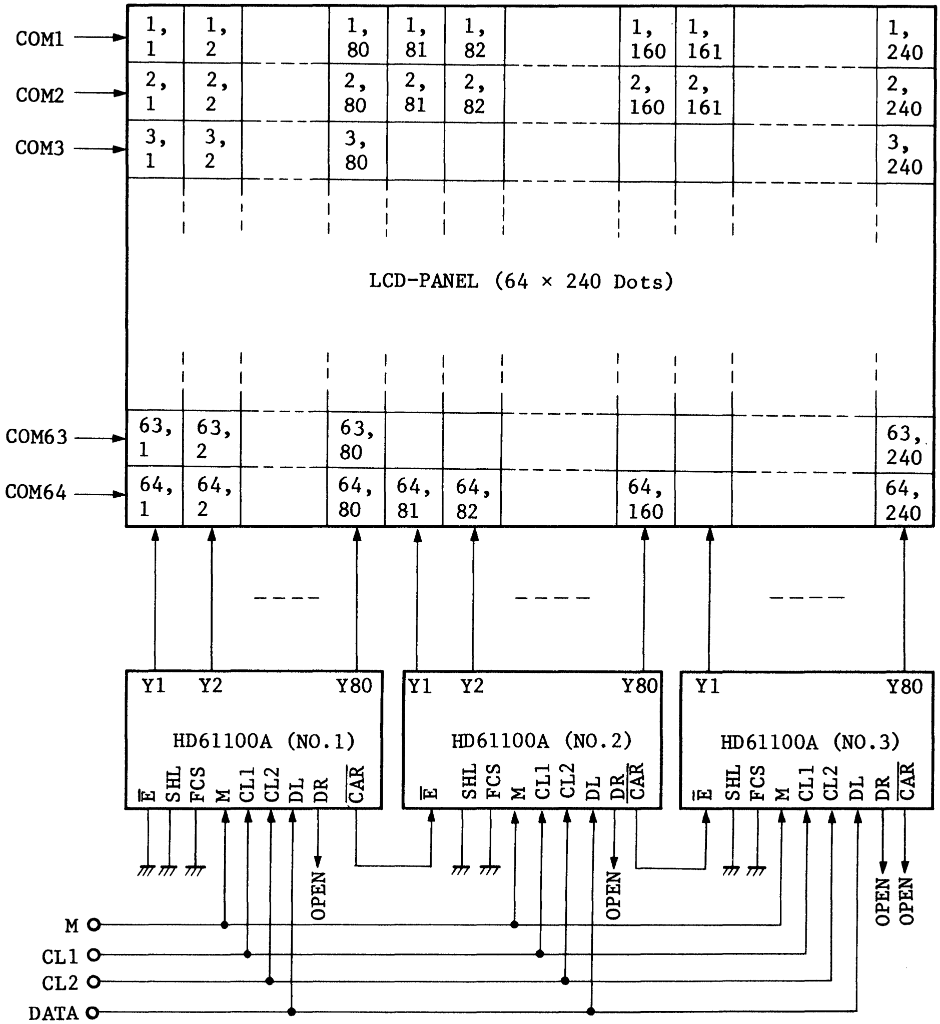
Terminal name	Number of terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 1		Power supply	V_{CC}-GND : Power supply for internal logic $V_{CC}-V_{EE}$: Power supply for LCD drive circuit
V_{1L}~V_{4L} V_{1R}~V_{4R}	8		Power supply	Power supply for liquid crystal drive V_{1L} (V_{1R}), V_{2L} (V_{2R})...selection level V_{3L} (V_{3R}), V_{4L} (V_{4R})...non-selection level Power supplies connected with V_{1L} and V_{1R} (V_{2L} & V_{2R}, V_{3L} & V_{3R}, V_{4L} & V_{4R}) should have the same voltages.
Y1~Y80	80	0	LCD	Liquid crystal driver outputs Selects one of the 4 levels, V1, V2, V3 and V4. Relation among output level, M and display data (D) is as follows. 
M	1	I	Controller	Switch signal to convert liquid crystal drive waveform into AC.
CL1	1	I	Controller	Latch clock of display data (fall edge trigger). Synchronizing with the fall of CL1, liquid crystal driver signals corresponding to the display data are output.
CL2	1	I	Controller	Shift clock of display data (D) Fall edge trigger

<table>
<tr><th>Terminal name</th><th>Number of terminals</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>DL, DR</td><td>2</td><td>I/O</td><td>Controller</td><td>Input of serial display data (D)
<table>
<tr><th>(D)</th><th>Liquid crystal driver output</th><th>Liquid crystal display</th></tr>
<tr><td>1 (H level)</td><td>selection level</td><td>ON</td></tr>
<tr><td>0 (L level)</td><td>non-selection level</td><td>OFF</td></tr>
</table>
I/O status of DL and DR terminals depends on SHL input level.
<table>
<tr><th>SHL</th><th>DL</th><th>DR</th></tr>
<tr><td>H level</td><td>O</td><td>I</td></tr>
<tr><td>L level</td><td>I</td><td>O</td></tr>
</table></td></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects a shift direction of serial data. When the serial data (D) is input in order of D1→· · ·→D80, the relations between the data (D) and output Y are as follows.
<table>
<tr><th>SHL</th><th>Y1</th><th>Y2</th><th>Y3</th><th>....</th><th>Y80</th></tr>
<tr><td>"L"</td><td>D1</td><td>D2</td><td>D3</td><td>....</td><td>D80</td></tr>
<tr><td>"H"</td><td>D80</td><td>D79</td><td>D78</td><td>....</td><td>D1</td></tr>
</table>
When SHL is "L", data is input from the terminal DL. Any lines should not be connected to the terminal DL, as it is in the state of output.
When SHL is "H", the relation between DL and DR reverses.</td></tr>
<tr><td>$\overline{E}$</td><td>1</td><td>I</td><td>GND or the terminal $\overline{CAR}$ of the HD61100A</td><td>Controls the S/P conversion.
The operation stops with "H" level, and the S/P conversion starts with "L" level.</td></tr>
</table>

Terminal name	Number of terminals	I/O	Connected to	Functions
$\overline{\text{CAR}}$	1	O	the input terminal $\overline{\text{E}}$ of the HD61100A	Used for cascade connection with the HD61100A to increase the number of bit which can be S/P converted.
FCS	1	I	GND	Input terminal for test. Connect to GND.

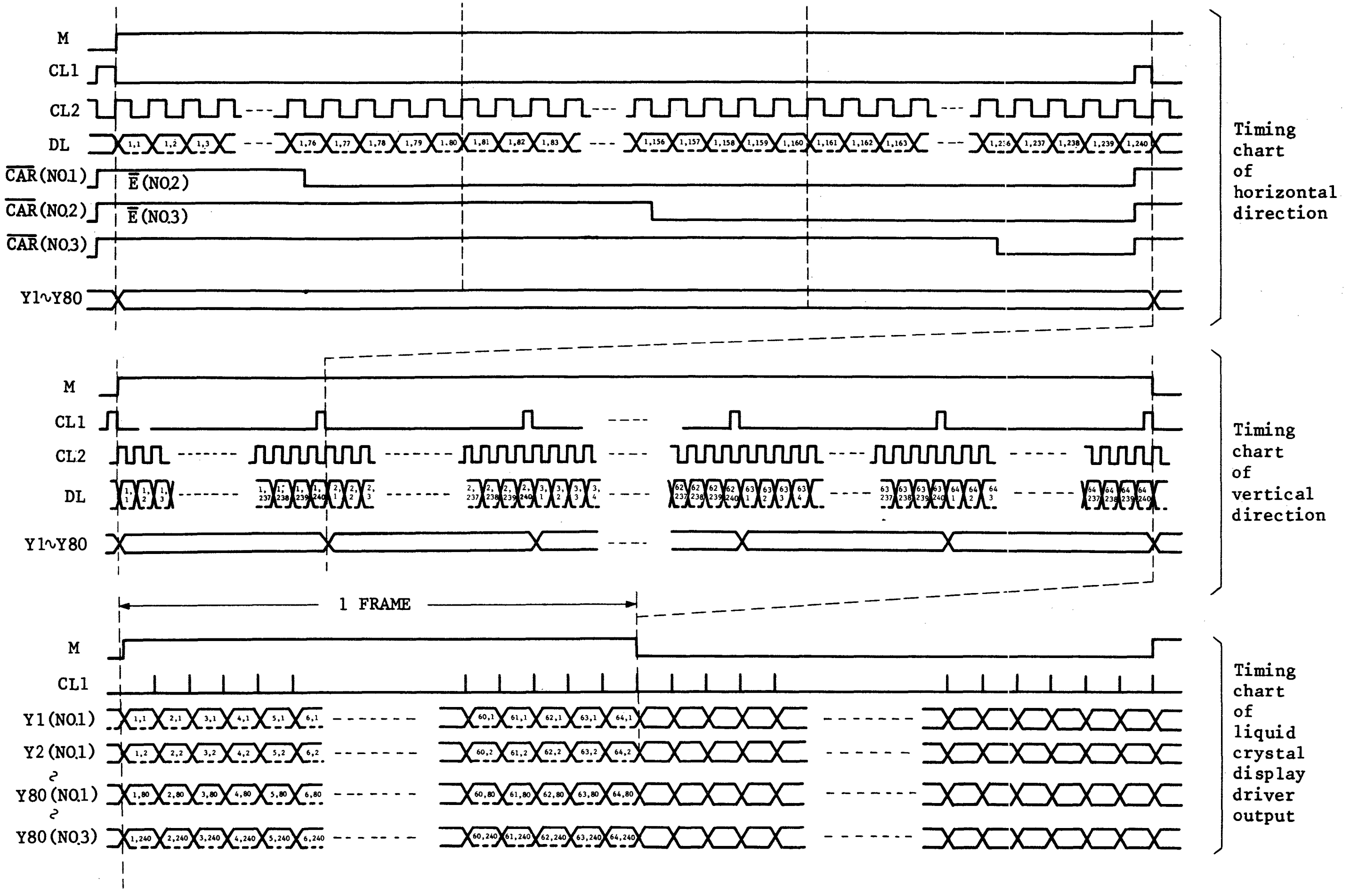
■ THE OPERATION OF THE HD61100A

The following is the LCD panel with 64 × 240 dots on which characters are displayed with 1/64 duty dynamic drive. Fig. 1 is an example of liquid crystal display and connection to HD61100A's. Fig. 2 shows a time chart of I/O signals of HD61100A.



Cascade three HD61100As. Input data to the terminal DL of NO.1, NO.2 and NO.3. Connect $\overline{E}$ of NO.1 to GND. Don't connect any lines to $\overline{CAR}$ of NO.3. Connect common signal terminals (COM1 ∿ COM64) to X1 ∿ X64 of common driver HD61103A. (m,n) of LCD panel is the address corresponding to each dot.

Fig. 1 LCD driver with 64 × 240 dots

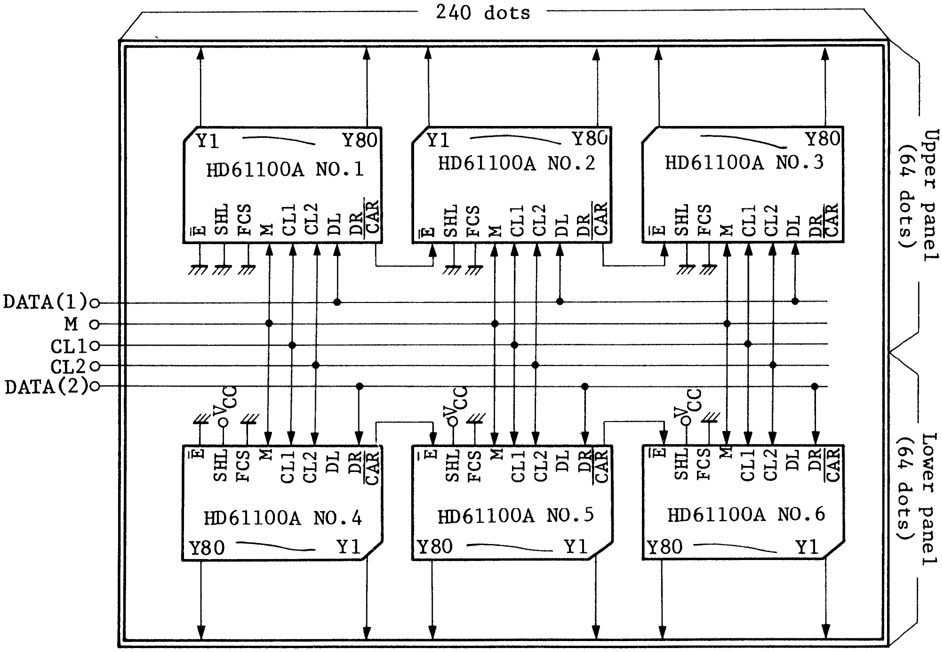


Timing chart in the example of connection of Fig.1. DL input (m,n) is the data which corresponds to each address (m,n) of LCD panel.

Fig. 2 HD61100A Timing Chart

■ EXAMPLE OF APPLICATION

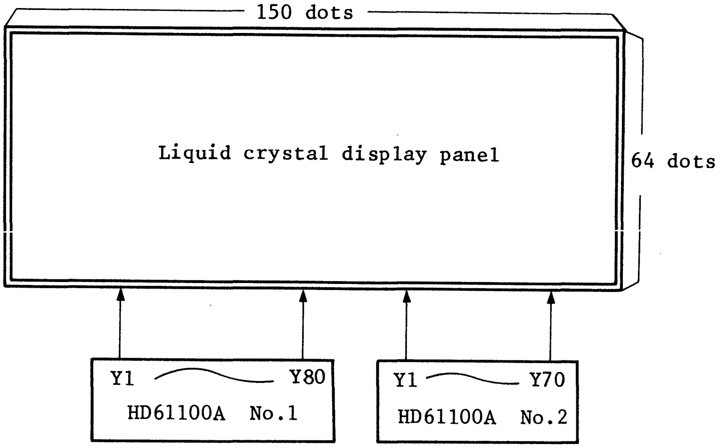
- An example of 128 × 240 dot liquid crystal display (1/64 duty)



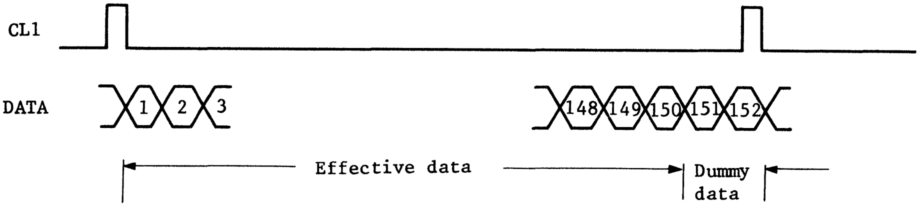
Liquid crystal panel is divided into upper and lower parts. These two parts are driven separately. HD61100As of No.1 ∿ No.3 drive upper half. Serial data, which are input from DATA(1) terminal, appear at $Y_1 \rightarrow Y_2 \rightarrow$ -- Y_{80} terminal of No.1, then at $Y_1 \rightarrow Y_2 \rightarrow$-- Y_{80} of No.2 and then at $Y_1 \rightarrow Y_2 \rightarrow$ -- Y_{80} of No.3 in order where they were input. (in the case of SHL=L). HD61100As of No.4 ∿ No.6 drive lower half. Serial data, which are input from DATA(2) terminal, appear at $Y_{80} \rightarrow T_{79} \rightarrow$ -- Y_1 of No.4, then at $Y_{80} \rightarrow Y_{79} \rightarrow$ -- Y_1 of No.5 and then $Y_{80} \rightarrow Y_{79} \rightarrow$ -- Y_1 of No.6 in order where they were input (in the case of SHL=H).

As shown in this example, PC board for display divided into upper and lower half can be easily designed by using SHL terminal effectively.

- Example of 64 × 150 dot liquid crystal display (1/64 duty, SHL=L)



4-bit parallel process is used in this LSI to lessen the power dissipation. Thus, the sum of the dots in lateral direction has to be multiple of 4. If not, as this example, consideration is needed to input signals.



As the sum of dots in lateral direction is 150, 2 more dummy data bits are transferred. (152=4 × 38).
Dummy data, which is output from Y71 and Y72 of NO.2, can be either "0" or "1" because these terminals do not connect with the liquid crystal display panel.

HD61102
(Dot Matrix Liquid Crystal Graphic Display Column Driver)

DESCRIPTION

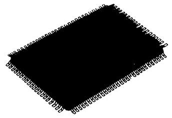
HD61102 is a column (segment) driver for dot matrix liquid crystal graphic display systems. It stores the display data transferred from a 8-bit micro-computer in the internal display RAM and generates dot matrix liquid crystal driving signals.

Each bit data of display RAM corresponds to ON/OFF of each dot of liquid crystal display to provide more flexible display.

As it is internally equipped with 64 output drivers for display, it is available for liquid crystal graphic display with many dots.

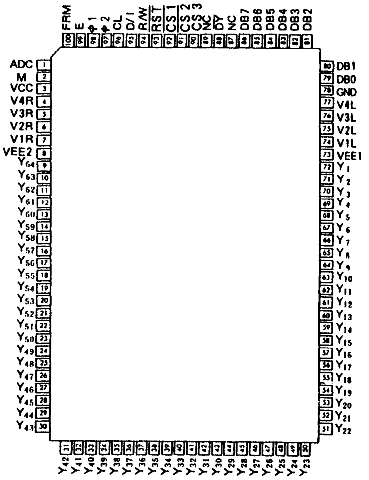
The HD61102, which is produced in the CMOS process, can accomplish a portable battery drive equipment by combining a CMOS micro-computer, utilizing the liquid crystal display's lower power dissipation.

Moreover it can facilitate dot matrix liquid crystal graphic display system configuration by combining the row (common) driver HD61103A.



(FP-100)

■ PIN ARRANGEMENT



(Top view)

■ FEATURES

- Dot matrix liquid crystal graphic display column driver incorporating display RAM.
- RAM data direct display by internal display RAM
  RAM bit data "1" .... ON
  RAM bit data "0" .... OFF
- Internal display RAM address counter
  preset, increment
- Display RAM capacity .... 512 bytes (4096 bits)
- 8-bit parallel interface
- Internal liquid crystal display driver circuit 64
- Display duty
  Combination of frame control signal and data latch synchronization signal make it possible to select out of static through an optional duty.
- Wide range of instruction function
  Display Data Read/Write, Display ON/OFF,
  Set address, Set Display Start line,
  Read Status
- Lower power dissipation ——during display 2mW max
- Power supply Vcc ——+5V ± 10%
  VEE —— 0V ∿ -10V
- Liquid crystal display driving level——15.5V max
- CMOS process
- 100 - pin flat plastic package (FP-100)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	-0.3 ∿ +7.0	V	2
	V_{EE}	V_{CC} -16.5 ∿ V_{CC} +0.3	V	3
Terminal voltage (1)	V_{T1}	V_{EE} -0.3 ∿ V_{CC} +0.3	V	4
Terminal voltage (2)	V_{T2}	-0.3 ∿ V_{CC} +0.3	V	2, 5
Operating temperature	Topr	-20 ∿ +75	°C	
Storage temperature	Tstg	-55 ∿ +125	°C	

(Note 1) LSI's may be destroyed for ever, if being used beyond the absolute maximum ratings.
In ordinary operation, it is desirable to use them observing the recommended operation conditions.
Using beyond these conditions may cause malfunction and poor reliability.

(Note 2) All voltage values are referred to GND=0V.

(Note 3) Apply the same supply voltage to V_{EE} 1 and V_{EE}2.

(Note 4) Applies to V1L, V2L, V3L, V4L, V1R, V2R, V3R and V4R.
Maintain
Vcc≧V1L=V1R≧V3L=V3R≧V4L=V4R≧V2L=V2R≧VEE

(Note 5) Applies to M, FRM, CL, $\overline{RST}$, ADC, ϕ1, ϕ2, $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I, ADC and DB0∿7.

■ ELECTRICAL CHARACTERISTICS
(GND=0V, VCC=4.5 ∿ 5.5V, VEE=0∿-10V, Ta=-20∿+75°C)

Item	Symbol	Test condition	Limit			Unit	Note
			min	typ	max		
Input "High" voltage	V_{IHC}		0.7×Vcc	-	Vcc	V	1
	V_{IHT}		2.0	-	Vcc	V	2
Input "Low" voltage	V_{ILC}		0	-	0.3×Vcc	V	1
	V_{ILT}		0	-	0.8	V	2
Output "High" voltage	V_{OH}	IOH=-205μA	2.4	-	-	V	3
Output "Low" voltage	V_{OL}	IOL=1.6mA	-	-	0.4	V	3
Input leakage current	I_{IL}	Vin=GND∿Vcc	-1.0	-	+1.0	μA	4
Three state (OFF) input current	I_{TSL}	Vin=GND∿Vcc	-5.0	-	+5.0	μA	5
Liquid crystal supply leakage current	I_{LSL}	Vin=VEE∿Vcc	-2.0	-	+2.0	μA	6
Driver ON resistance	R_{ON}	Vcc-VEE=15V $\pm I_{LOAD}$=0.1mA	-	-	7.5	KΩ	7
Dissipation current	Icc(1)	During display	-	-	100	μA	8
	Icc(2)	During access access cycle=1MHz	-	-	500	μA	8

(Note 1) Applies to M, FRM, CL, $\overline{RST}$, ADC, ADC, φ1 and φ2.

(Note 2) Applies to $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I and DB0 ∿ 7.

(Note 3) Applies to DB0 ∿ 7.

(Note 4) Applies to terminals except for DB0 ∿ 7.

(Note 5) Applies to DB0 ∿ 7 at high impedance.

(Note 6) Applies to V1L ∿ V4L and V1R ∿ V4R.

(Note 7) Applies to Y1 ∿ Y64.

(Note 8) Specified when liquid crystal display is in 1/64 duty.
Operation frequency f_{CLK}=250 kHz (φ1 and φ2 frequency)
Frame frequency f_M =70 Hz (FRM frequency)

Specified in the state of
Output terminal ----- not loaded
Input level --------- V_{IH}=Vcc(V)
V_{IL}=GND (V)

Measured at Vcc terminal

● INTERFACE AC CHARACTERISTICS

(1) MPU Interface

(GND=0V, Vcc=4.5 ∿ 5.5V, V_{EE}=0 ∿ -10V, Ta=-20 ∿ +75°C)

Item	Symbol	min	typ	max	Unit	Note
E cycle time	t_{CYC}	1000	-	-	ns	1, 2
E high level width	P_{WEH}	450	-	-	ns	1, 2
E low level width	P_{WEL}	450	-	-	ns	1, 2
E rise time	tr	-	-	25	ns	1, 2
E fall time	tf	-	-	25	ns	1, 2
Address setup time	t_{AS}	140	-	-	ns	1, 2
Address hold time	t_{AH}	10	-	-	ns	1, 2
Data setup time	t_{DSW}	200	-	-	ns	1
Data delay time	t_{DDR}	-	-	320	ns	2, 3
Data hold time (Write)	t_{DHW}	10	-	-	ns	1
Data hold time (Read)	t_{DHR}	20	-	-	ns	2

(Note 1)

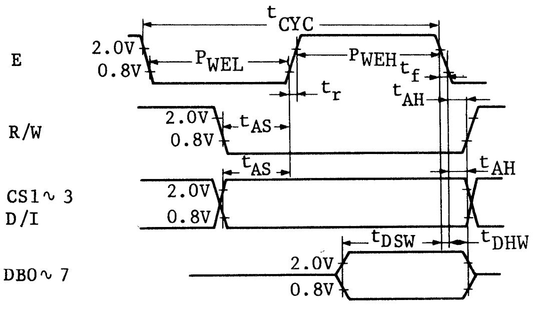


Fig. 1 CPU Write Timing

(Note 2)

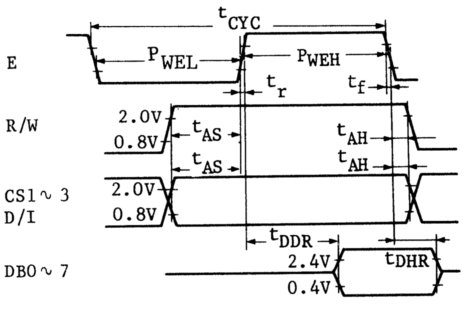
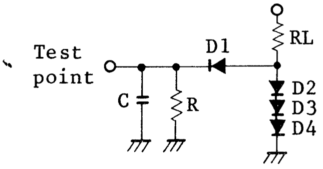


Fig. 2 CPU Read Timing

(Note 3) DB0 ∿ 7 : load circuit



RL=2.4KΩ

R =11KΩ

C =130pF (including jig capacity)

Diodes D1 to D4 are all 1S2074Ⓗ .

(2) Clock Timing

(GND=0V, Vcc=4.5 ∿ 5.5V, V_{EE}=0 ∿ -10V, Ta=20 ∿ +75°C)

Item	Symbol	Test condition	Limit			Unit
			min	typ	max	
ϕ1, ϕ2 cycle time	tcyc	Fig. 3	2.5	-	20	μs
ϕ1 "Low" level width	$t_{WL\phi1}$	Fig. 3	625	-	-	ns
ϕ2 "Low" level width	$t_{WL\phi2}$	Fig. 3	625	-	-	ns
ϕ1 "High" level width	$t_{WH\phi1}$	Fig. 3	1875	-	-	ns
ϕ2 "High" level width	$t_{WH\phi2}$	Fig. 3	1875	-	-	ns
ϕ1-ϕ2 phase difference	t_{D12}	Fig. 3	625	-	-	ns
ϕ2-ϕ1 phase difference	t_{D21}	Fig. 3	625	-	-	ns
ϕ1, ϕ2 rise time	tr	Fig. 3	-	-	150	ns
ϕ1, ϕ2 fall time	tf	Fig. 3	-	-	150	ns

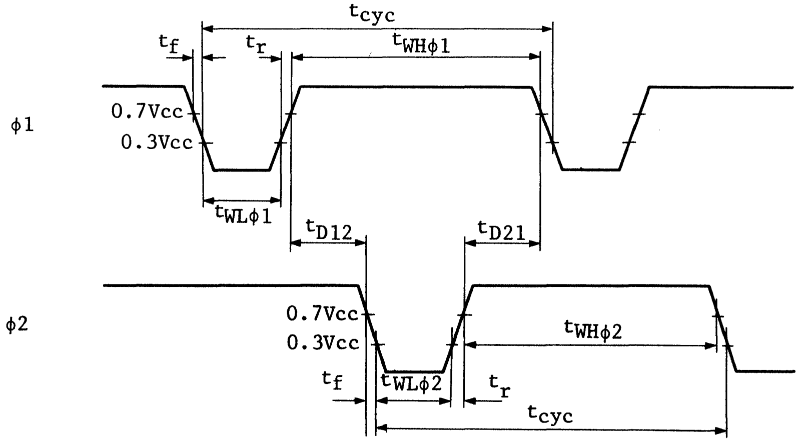


Fig. 3 External Clock Waveform

(3) Display Control Timing

(GND=0V, V_{CC}=4.5 ∿ 5.5V, V_{EE}=0 ∿ -10V, Ta=-20 ∿ +75°C)

Item	Symbol	Test condition	Limit			Unit
			min	typ	max	
FRM delay time	t_{DFRM}	Fig. 4	-2	-	+2	μs
M delay time	t_{DM}	Fig. 4	-2	-	+2	μs
CL "Low" level width	t_{WLCL}	Fig. 4	35	-	-	μs
CL "High" level width	t_{WHCL}	Fig. 4	35	-	-	μs

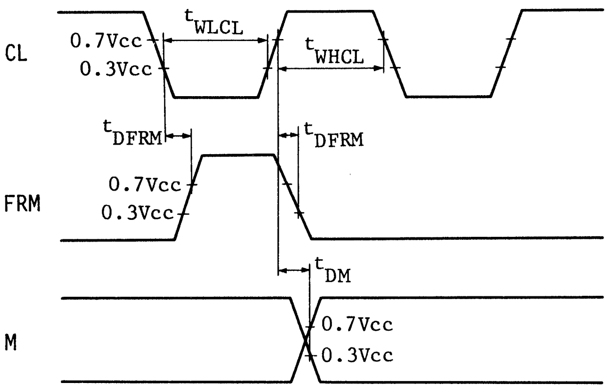
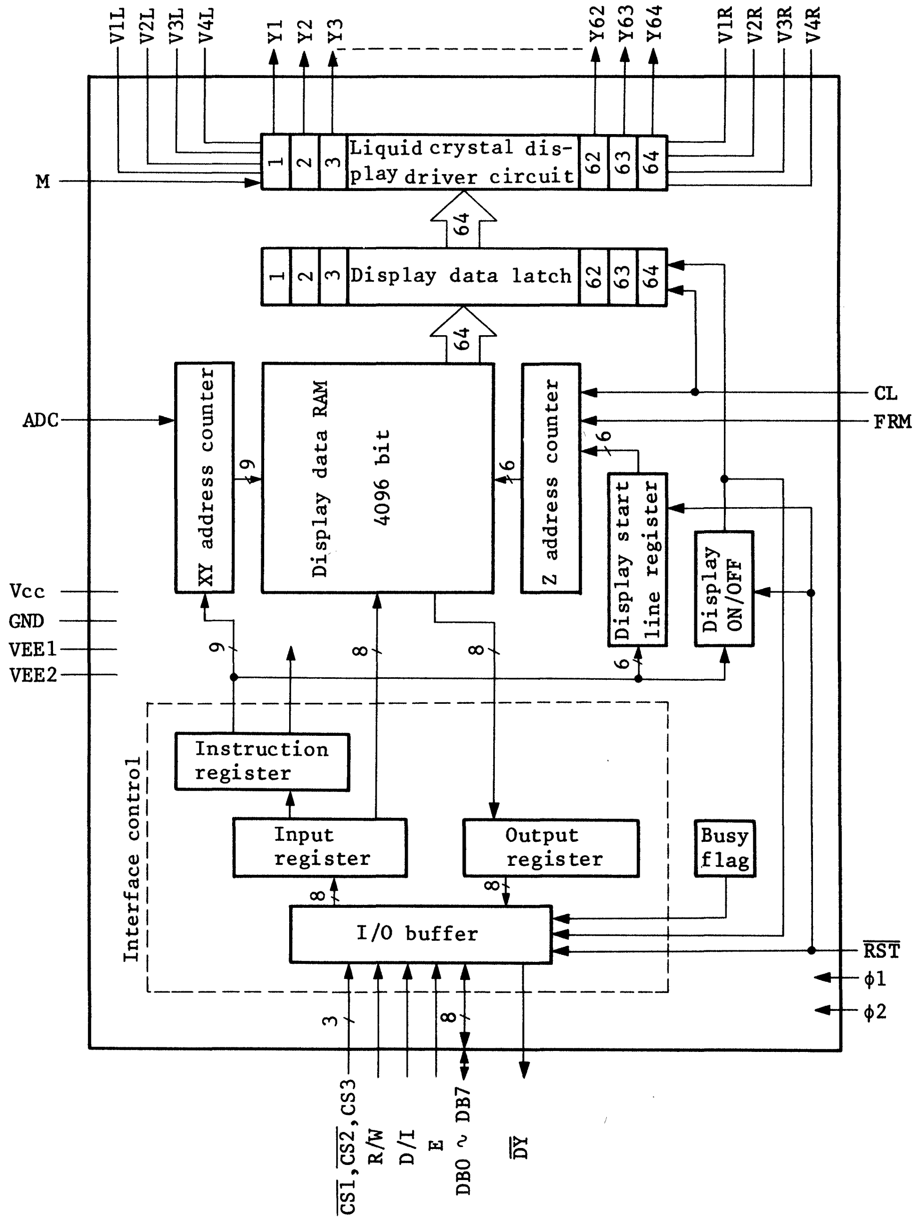


Fig. 4 Display Control Signal Waveform

■ BLOCK DIAGRAM



■ TERMINAL FUNCTIONS

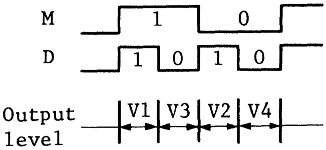
Terminal name	Number of terminals	I/O	Connected to	Functions
V_{CC} GND	2		Power supply	Power supply for internal logic. Recommended voltage is GND = 0V V_{CC} = +5V ± 10%
V_{EE} 1 V_{EE} 2	2		Power supply	Power supply for liquid crystal display drive circuit. Recommended power supply voltage is V_{CC} - 15 to GND. Connect the same power supply to V_{EE1} and V_{EE2}. V_{EE1} and V_{EE2} are not connected each other in the LSI.
V1L, V1R V2L, V2R V3L, V3R V4L, V4R	8		Power supply	Power supply for liquid crystal display drive. Apply the voltage specified depending on liquid crystals within the limit of V_{EE} through V_{CC}. V1L(V1R), V2L(V2R)---Selection level V3L(V3R),V4L(V4R)----Non-selection level Power supplies connected with V1L and V1R (V2L & V2R, V3L & V3R, V4L & V4R) should have the same voltages.
$\overline{CS1}$ $\overline{CS2}$ CS3	3	I	MPU	Chip selection. Data can be input or output when the terminals are in the next conditions. Terminal name: $\overline{CS1}$ 'L', $\overline{CS2}$ 'L', CS3 'H' (Condition)
E	1	I	MPU	Enable At write(R/W=L) : Data of DB0 to DB7 is latched at the fall of E. At read(R/W=H) : Data appears at DB0 to DB7 while E is in "High" level.

Terminal name	$\overline{CS1}$	$\overline{CS2}$	CS3
Condition	'L'	'L'	'H'

Terminal name	Number of terminals	I/O	Connected to	Functions
R/W	1	I	MPU	Read/Write R/W=H : Data appears at DB0 to DB7 and can be read by the CPU When E=H, $\overline{CS1}$, $\overline{CS2}$=L and CS3=H. R/W=L : DB0 to DB7 can accept at fall of E when $\overline{CS1}$, $\overline{CS2}$=L and CS3=H.
D/I	1	I	MPU	Data/Instruction D/I=H : Indicates that the data of DB0 to DB7 is display data. D/I=L : Indicates that the data of DB0 to DB7 is display control data.

ADC	1	I	V_{CC}/GND	Adress control signal determine the relation between Y address of display RAM and terminals from which the data is output.
				ADC=H : Y1-$0, Y64-$63
				ADC=L : Y64-$0, Y1-$63

DB0∿DB7	8	I/O	MPU	Data bus, three-state I/O common terminal
M	1	I	HD61103A	Switch signal to convert liquid crystal drive waveform into AC.
FRM	1	I	HD61103A	Display synchronous signal (frame signal) This signal presets the 6-bit display line counter and synchronizes a common signal with the frame timing when the FRM signal becomes high.
CL	1	I	HD61103A	Syncronous signal to latch display data. The CL signal indicates to count up the display output adress counter and latch the display data at rising.
Φ1,Φ2	1	I	HD61103A	2-phase clock signal for internal operation. The Φ1 and Φ2 clocks are used to perform the operations (I/O of display data and execution of instructions) other than display.

Terminal name	Number of terminals	I/O	Connected to	Functions
Y1∿Y64	64	O	Liquid criptal display	Liquid crystal display column (segment) drive output. These pins outputs light ON level when "1" is in the display RAM, and light OFF level with "0" in it. Relation among output level, M and display data (D) is as follows.  M 1 0 D 1 0 1 0 Output level V1 V3 V2 V4
$\overline{\text{RST}}$	1	I	CPU or external CR	The following registers can be initialized by setting the $\overline{\text{RST}}$ signal to "Low" level. (1) ON/OFF register 0 set (display OFF) (2) Display start line register 0 line set (displays from 0 line) After releasing reset, this condition can be changed only by the instruction.
$\overline{\text{DY}}$	1	O	Open	Output terminal for test. Usually, don't connect any lines to this terminal.
NC	2		Open	Unused terminals. Don't connect any lines to these terminals.

(Note) "1" corresponds to "High level" in positive logic.

■ FUNCTION OF EACH BLOCK

● Interface Control

(1) I/O buffer

Data is transferred through 8 data buses (DB0 ∿ DB7).

DB7 .... MSB (Most Significant Bit)
DB0 .... LSB (Least Significant Bit)

Data can neither be input nor output unless $\overline{\mathrm{CS1}}$ to CS3 are in the active mode. Therefore, when $\overline{\mathrm{CS1}}$ to CS3 are not in active mode it is useless to switch the signals of input terminals except $\overline{\mathrm{RST}}$ and ADC, namely, the internal state is maintained and no instruction excute. Besides, pay attention to $\overline{\mathrm{RST}}$ and ADC which operate irrespectively by $\overline{\mathrm{CS1}}$ to CS3.

(2) Register

Both input register and output register are provided to interface to MPU of which the speed is different from that of internal operation. The selection of these registers depend on the combination of R/W and D/I signals.

Table 1. Register Selection

D/I	R/W	Operation
1	1	Reads data out of output register as internal operation (display data RAM → output register)
1	0	Writes data into input register as internal operation (input register → display data RAM)
0	1	Busy check. Read of status data.
0	0	Instruction

① Input register

Input register is used to store data temporarily before writing it into display data RAM.
The data from MPU is written into input register, then into display data RAM automatically by internal operation.

When $\overline{\text{CS1}}$ to CS3 are in the active mode and D/I and R/W select the input register as shown in Table 1, data is latched at the fall of E signal.

② Output register

Output register is used to store data temporarily which is read from display data RAM. To read out the data from output register, $\overline{\text{CS1}}$ to CS3 should be in the active mode and both D/I and R/W should be 1. With READ instruction, data stored in the output register is output while E is "H" level. Then, at the fall of E, the display data at the indicated address is latched into the output register and the address is increased by 1. The contents in the output register is rewritten with READ instruction, while is held with address set instruction, etc.

Therefore, the data of the specified address can not be output with READ instruction soon after the address is set, but can be output at the second read of data. That is to say, one dummy read is necessary. Fig. 5 shows the CPU read timing.

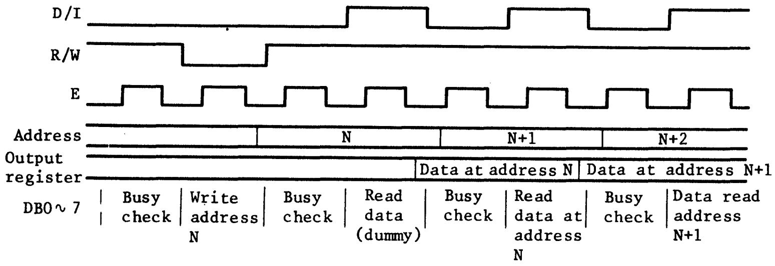
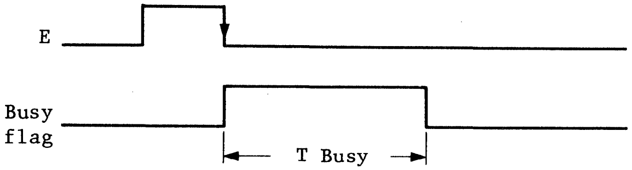


Fig. 5 CPU Read Timing

- Busy Flag

"1" of busy flag indicates that HD61102 is on the move and any instructions except Status Read instruction can not be accepted. The value of the busy flag is read out on DB7 by the Status Read instruction. Make sure that the busy flag is reset ("0") before the issue of instruction.



$1/f_{CLK} \leqq T\ Busy \leqq 3/f_{CLK}$

f_{CLK} is $\phi 1$, $\phi 2$ frequency

- Display ON/OFF Flip Flop

Display ON/OFF flip flop selects one of two states, ON state and OFF state of segments Y1 to Y64. In ON state, the display data corresponding to that in RAM is output to the segments. On the other hand, the display data at all segments disappear in OFF state independent of the data in RAM.
It is controlled by display ON/OFF instruction. '0' of $\overline{RST}$ signal sets the segments in OFF state. The status of the flip flop is output to DB5 by Status Read instruction. Display ON/OFF instruction does not influence data in RAM. To control display data latch by this flip flop, CL signal (display synchronous signal) should be input correctly.

- Display Start Line Register

The register specifies a line in RAM which corresponds to the top line of LCD panel, when displaying contents in display data RAM on the LCD panel.
It is used for scrolling of the screen.
6-bit display start line information is written into this register by display start line set instruction, with 'H' level of FRM signal instructing to start the display, the information in this register is transferred to Z address counter which controls the display address, and the Z address counter is preset.

- X, Y Address Counter

This is a 9-bit counter which designates addresses of internal display data RAM. X address counter of upper 3 bits and Y address counter of lower 6 bits should be set each address by respective instruction.

(1) X address counter

Ordinary register with no count functions. An address is set in by instructions.

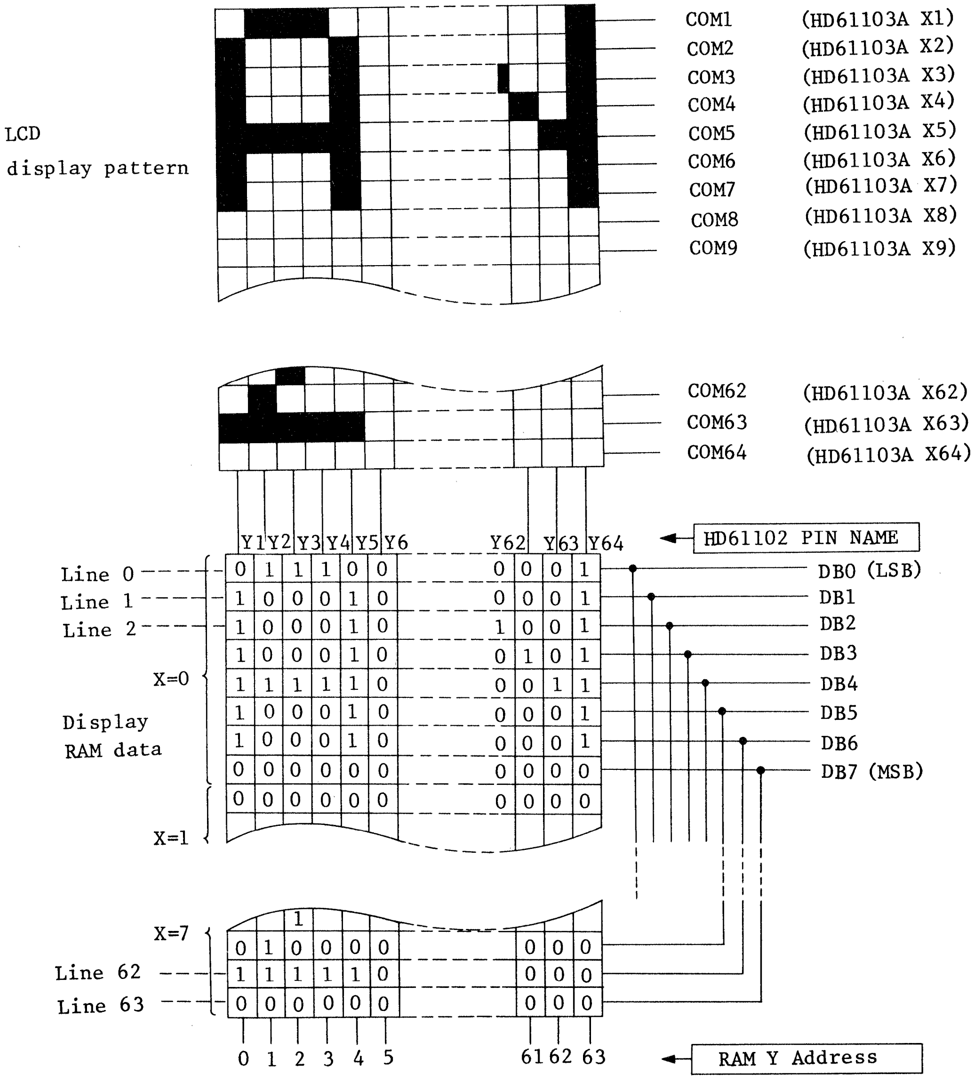
(2) Y address counter

An address is set in by instruction and it is increased by 1 automatically by R/W operations of display data. The Y address counter loops the values of 0 to 63 to count.

- Display Data RAM

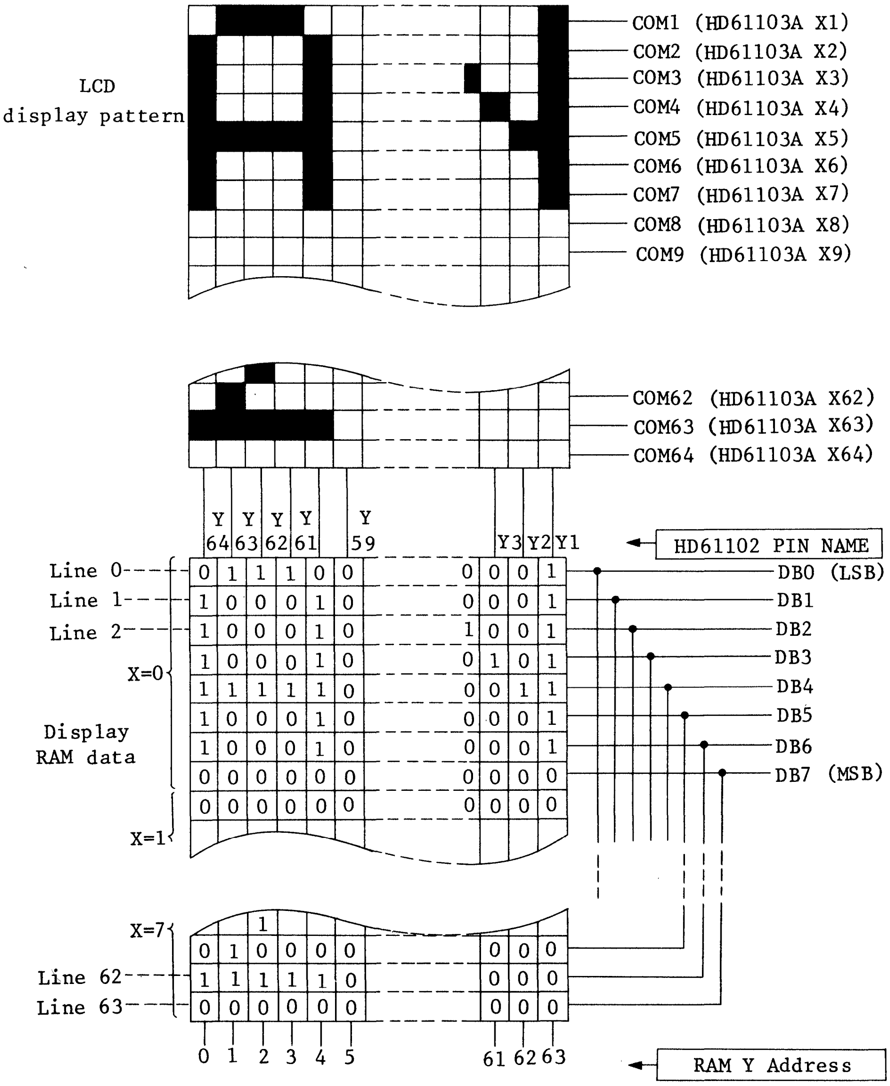
Dot data for display is stored in this RAM. 1-bit data of this RAM corresponds to light ON (data=1) and light OFF (data=0) of 1 dot in the display panel. The correspondence between Y addresses of RAM and segment PINs can be reversed by ADC signal.
As ADC signal controls Y address counter, a reverse of the signal during the operation causes malfunction and destruction of the contents of register and data of RAM. Therefore, never fail to connect ADC pin to V_{CC} or GND when using.

Fig. 6 shows the relations between Y address of RAM and segment pins in the cases of ADC=1 and ADC=0. (display start line=0, 1/64 duty).



(a) ADC="1" (Connected to Vcc)

Fig. 6 Relation between RAM Data and Display



(b) ADC="0" (Connected to GND)

Fig. 6 Relation Between RAM Data and Display

- Z Address Counter

The Z address counter generates addresses for outputting the display data synchronized with the common signal. This counter consists of 6-bit and counts up at the fall of CL signal. With "H" level of FRM, the contents of the display start line register is preset at the Z counter.

- Display data Latch

The display data latch stores the display data temporarily which is output from display data RAM to liquid crystal driving circuit.
Data is latched at the rise of CL signal. Display ON/OFF instruction controls the data in this latch and does not influence data in display data RAM.

- Liquid Crystal Display Driver Circuit

The combination of latched display data and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3 and V4 to be output.

- Reset

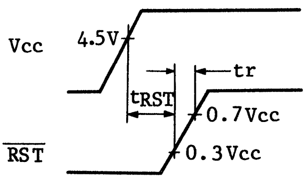
The system can be initialized by setting $\overline{\text{RST}}$ terminal at "Low" level when turning power ON.

1) Display-OFF
2) Set display start line register 0 line.

While $\overline{\text{RST}}$ is in Low level, any instruction except Status Read cannot be accepted. Therefore, Carry out other instructions after making sure that DB4=0 (clear RESET) and DB7=0 (Ready) by Status Read instruction.
The conditions of Power Supply at initial power up are as follows.

Item	Symbol	Min.	Typ	Max.	Unit
Reset time	t_{RST}	1.0	-	-	μs
Rise time	t_r	-	-	200	ns

Do not fail to set the system again because RESET during operation may destroy the data in all the register except ON/OFF register and in RAM.



■ DISPLAY CONTROL INSTRUCTIONS

• Outline

Table 2 shows the instructions. Read/Write (R/W) signal, Data/Instruction (D/I) signal and Data bus signal (DB0 to DB7) are also called instructions because the internal operation depends on the signals from MPU.
These explanations are detailed from the following page. Generally, there are following three kinds of instructions.

(1) Instruction to give addresses in the internal RAM
(2) Instruction to transfer data from/to the internal RAM
(3) Other instructions

In general use, the instruction (2) are used most frequently. But, since Y address of the internal RAM is increased by 1 automatically after writing (reading) data, the program can be lessened. During the execution of an instruction, the system cannot accept other instructions than Status Read instruction. Send instructions from MPU after making sure if the busy flag is "0", which is the proof an instruction is not being excuted.

Table 2. Instructions

Instructions	Code										Functions	
	R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1 Display ON/OFF	0	0	0	0	1	1	1	1	1	1/0	Controls the ON/OFF of display. RAM data and internal status are not affected. 1:ON, 0:OFF.	
2 Display start line	0	0	1	1	display start line (0∼63)						Specifies a RAM line displayed at the top of the screen.	
3 Set page (X address)	0	0	1	0	1	1	1	Page (0∼7)			Sets the page (X address) of RAM at the page (X address) register.	
4 Set Y address	0	0	0	1	Y address (0∼63)						Sets the Y address at the Y address counter	
5 Status Read	1	0	Busy	0	ON/OFF	RESET	0	0	0	0	Reads the status. RESET 1: reset 0:normal ON/OFF 1: display OFF 0:display ON Busy 1: on the internal operation 0: Ready	
6 Write display data	0	1	Write Data								Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM.	Has access to the address of the display RAM specified in advance. After the access, Y address is increased by 1.
7 Read display data	1	1	Read Data								Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.	

Note 1) Busy time varies with the frequency (f_{CLK}) of $\phi 1$, and $\phi 2$.

$(1/f_{CLK} \leqq T_{BUSY} \leqq 3/f_{CLK})$

- Detailed Explanation

(1) Display ON/OFF

	R/W	D/I	DB7							DB0
Code	0	0	0	0	1	1	1	1	1	D

← high-order-bit low-order-bit →

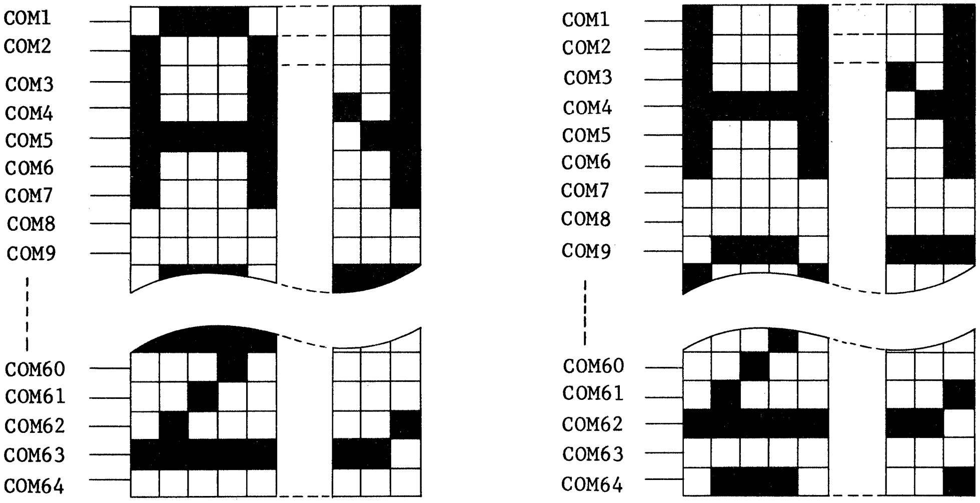
The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen with D=0, it remains in the display data RAM. Therefore, you can make it appear by changing D=0 into D=1.

(2) Display start line

	R/W	D/I	DB7							DB0
Code	0	0	1	1	A	A	A	A	A	A

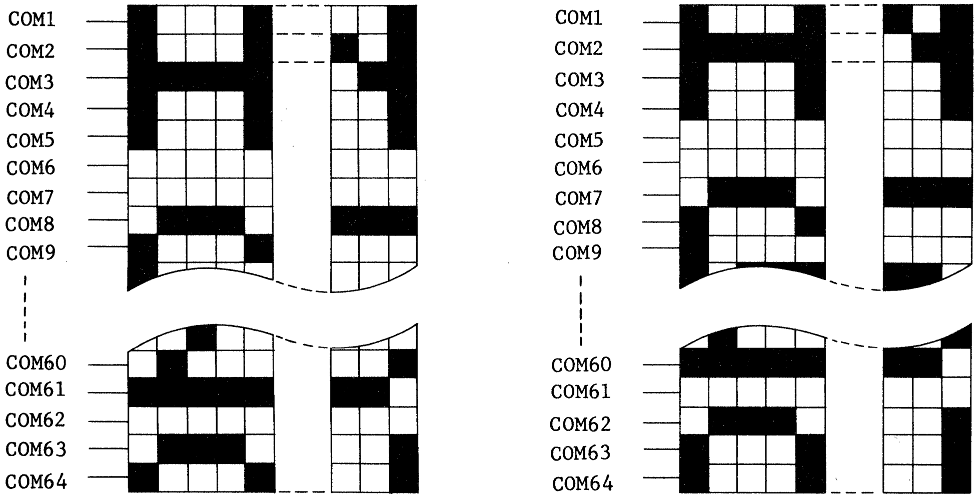
← high-order-bit low-order-bit →

Z address AAAAAA (binary) of the display data RAM is set at the display start line register and displayed at the top of the screen.
Fig. 7 are the examples of display (1/64 duty) when the start line=0 ∿ 3.
When the display duty is 1/64 or more (ex. 1/32, 1/24 etc.), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.



Start line=0

Start line=1



Start line=2

Start line=3

Fig. 7 Relation Between Start Line and Display

(3) Set page (X address)

	R/W	D/I	DB7							DB0
Code	0	0	1	0	1	1	1	A	A	A

← high-order-bit low-order-bit →

X address AAA (binary) of the display data RAM is set at the X address register. After that, writing or reading to or from MPU is executed in this specified page until the next page is set.

(4) Set Y address

	R/W	D/I	DB7							DB0
Code	0	0	0	1	A	A	A	A	A	A

← high-order-bit low-order-bit →

Y address AAAAAA (binary) of the display data RAM is set at the Y address counter. After that, Y address counter is increased by 1 every time the data is written or read to or from MPU.

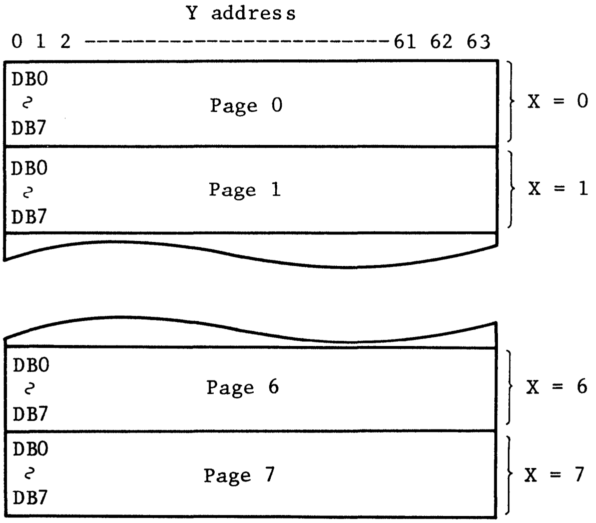


Fig. 8 Address Configuration of Display Data RAM

(5) Status Read

	R/W	D/I	DB7							DB0
Code	1	0	BUSY	0	ON/ OFF	RESET	0	0	0	0

← high-order-bit low-order-bit →

BUSY: When BUSY is 1, the LSI is in internal operation. No instructions are accepted while BUSY is 1, so you should make sure that BUSY is 0 before writing the next instruction.

ON/OFF: This bit shows the liquid crystal display conditions - ON condition or OFF condition.
When ON/OFF is 1, the display is in OFF condition.
When ON/OFF is 0, the display is in ON condition.

RESET: RESET=1 shows that the system is being initialized. In this condition, any instructions except Status Read instruction cannot be accepted.
RESET=0 shows that initializing has finished and the system is in the usual operation.

(6) Write Display Data

	R/W	D/I	DB7							DB0
Code	0	1	D	D	D	D	D	D	D	D

← high-order-bit low-order-bit →

Writes 8-bit data DDDDDDDD (binary) into the display data RAM. Then Y address is increased by 1 automatically.

(7) Read Display Data

	R/W	D/I	DB7							DB0
Code	1	1	D	D	D	D	D	D	D	D

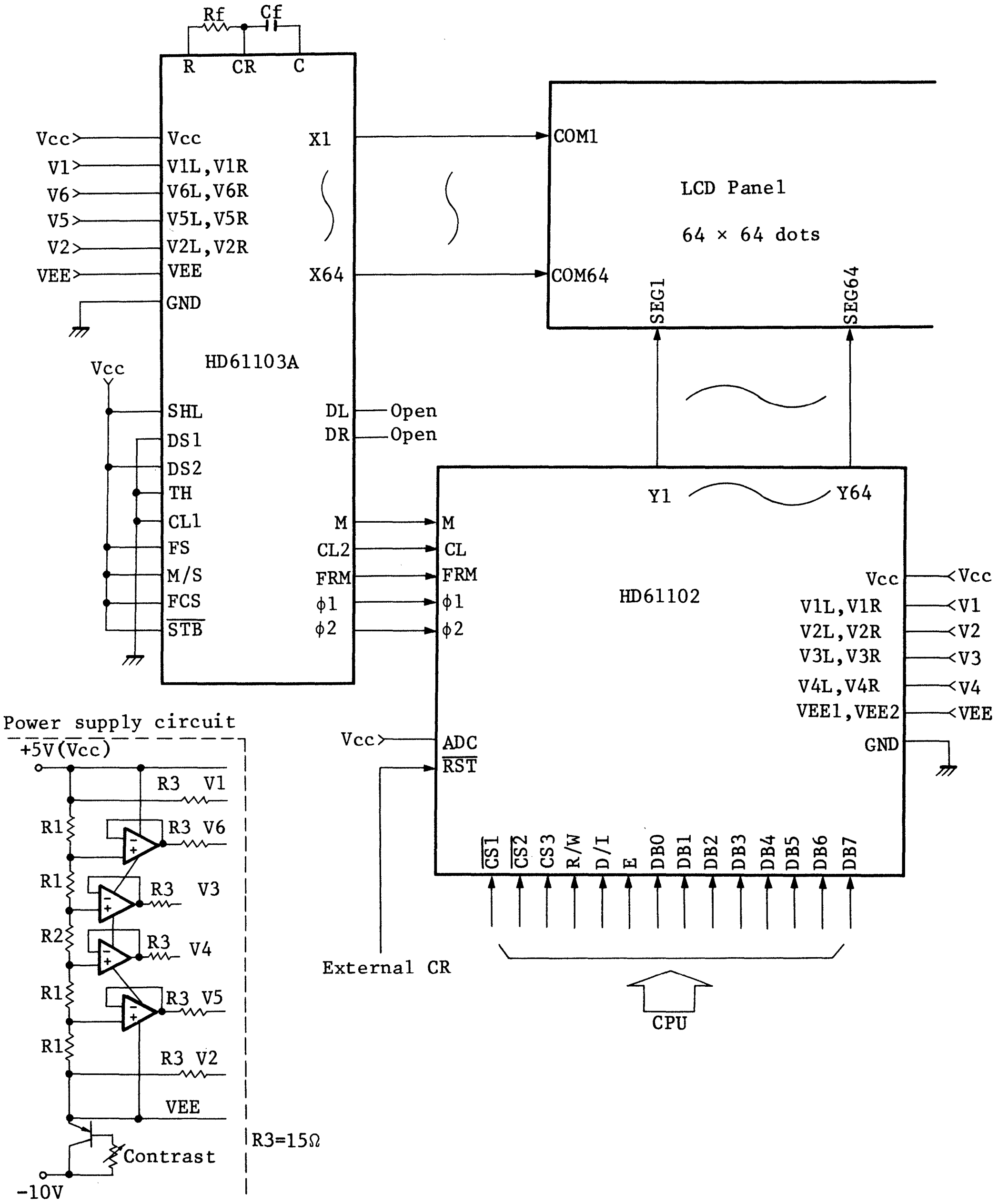
← high-order-bit low-order-bit →

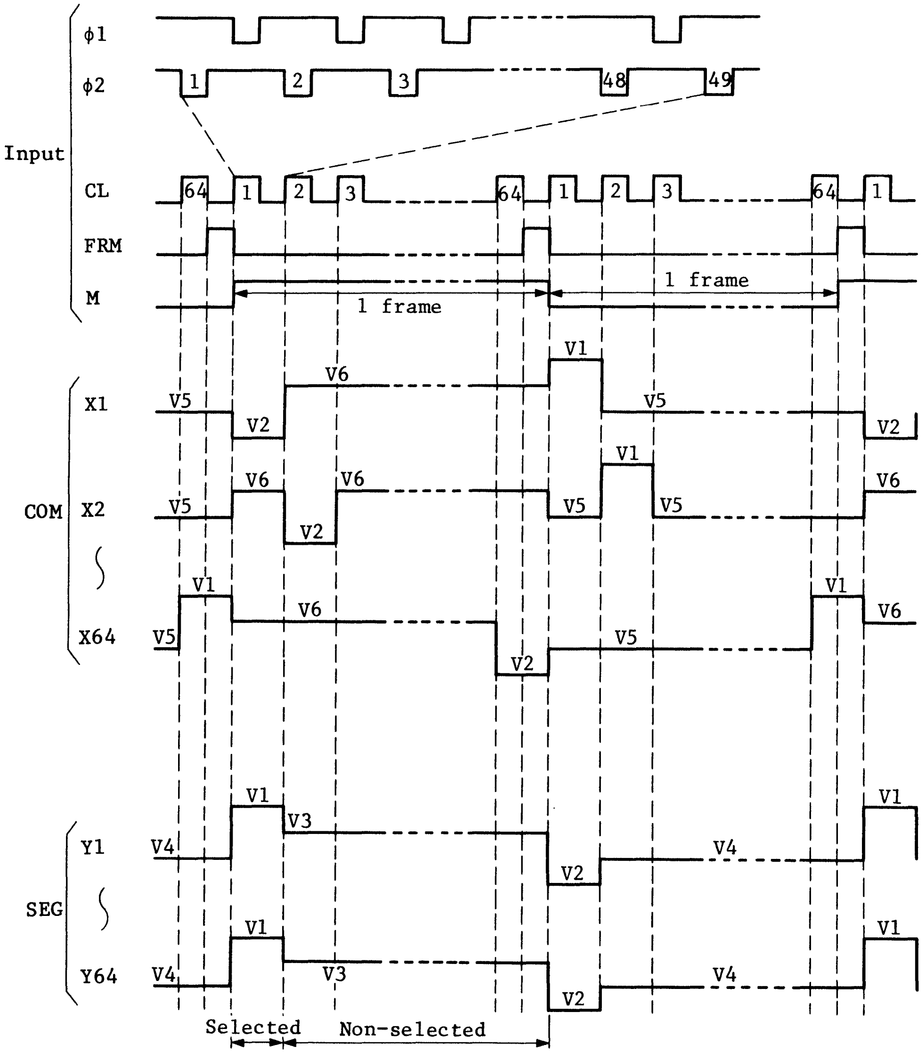
Read out 8-bit data DDDDDDDD (binary) from the display data RAM. Then Y address is increased by 1 automatically.

One dummy read is necessary soon after the address setting. For details, refer to the explanation of output register in "FUNCTION OF EACH BLOCK".

■ THE USAGE OF HD61102

- Interface with HD61103A (1/64 duty)



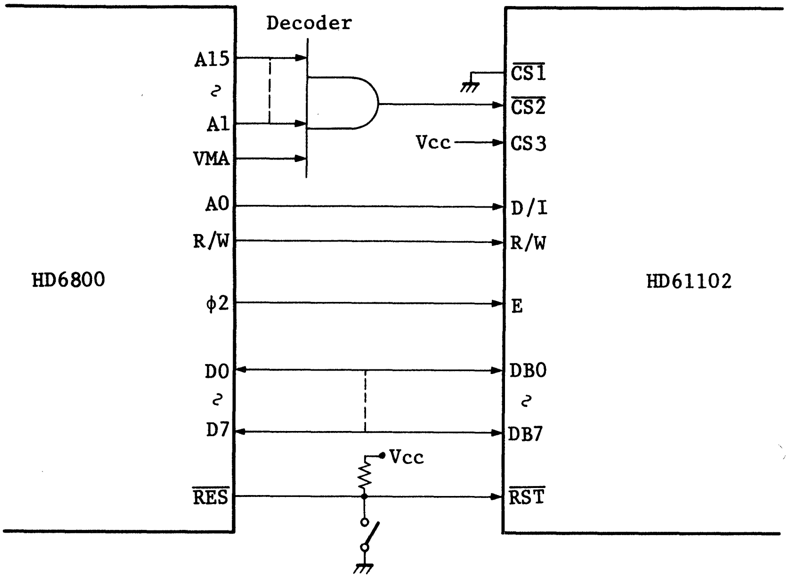


The wave forms of Y1 to Y64 outputs vary with the display data. In this example, the top line of the panel lights up and other dots do not.

Fig. 9 LCD Driver Timing Chart (1/64 duty)

- Interface with CPU

a) Example of connection with HD6800



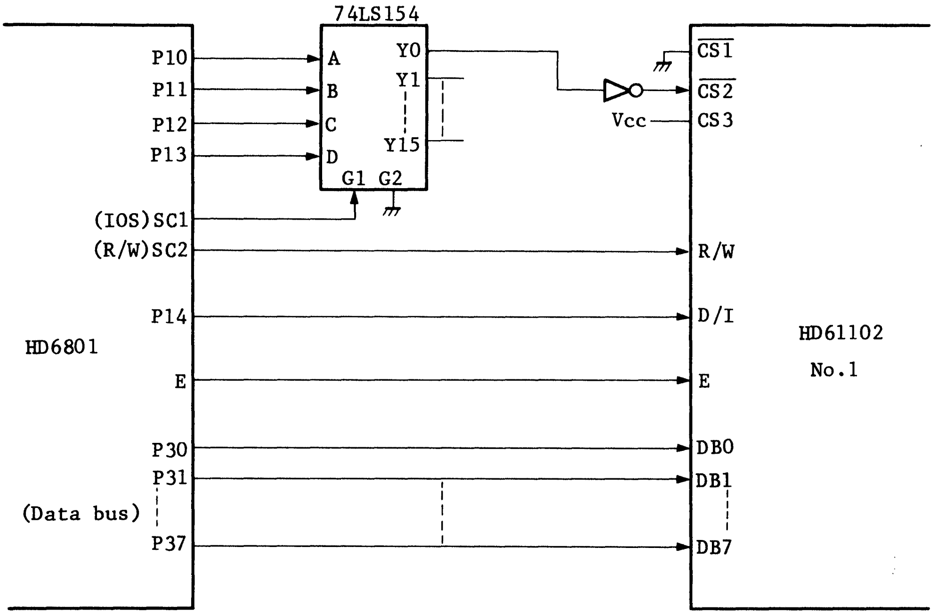
The example of connection with HD6800 series

In this decoder, addresses of HD61102 in the address area of HD6800 are:

Read/Write of the display data	$FFFF
Write of display instruction	$FFFE
Read out of status	$FFFE

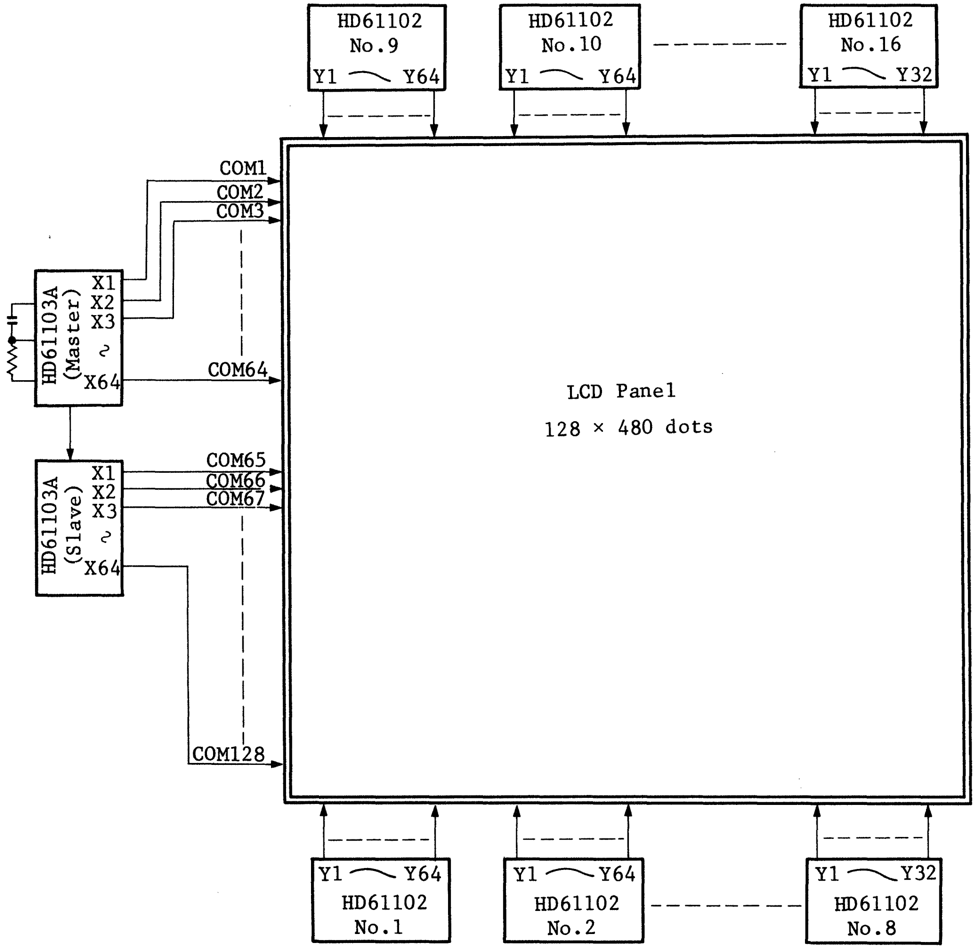
Therefore, you can control HD61102 by reading/writing the data at these addresses.

b) Example of connection with HD6801



- Set HD6801 in Mode 5.
  P10 to P14 are used as the output port and P30 to P37 as the data bus.
- 74LS154 is 4 to 16 decoder and genelate chip select signal to make specified HD61102 active after decoding 4 bits of P10 to P13.
- Therefore, after making the operation possible by P10 to P13 and specifying D/I signal by P14, read/write from/to the external memory area ($0100 to $01FE) to control HD61102.
  In this case, IOS signal is output from SC1 and R/W signal from SC2.
- For details of HD6800 and HD6801, refer to the each manual.

- Example of Application

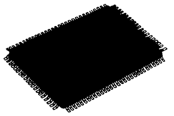


Note) In this example, two HD61103A's output the equivalent waveforms. So, stand-alone operation is possible. In this case, connect COM1 and COM65 to X1, COM2 and COM66 to X2, ..., and COM64 and COM128 to X64. However, for the large screen display, you had better drive in 2 rows as this example to guarantee the display quality.

HD61103A
(Dot Matrix Liquid Crystal Graphic Display Common Driver)

DESCRIPTION

The HD61103A is a common signal driver for dot matrix liquid crystal graphic display systems. It generates the timing signals (switch signal to convert LCD waveform to AC, frame synchronous signal) and supplies them to the column driver to control display. It provides 64 driver output lines and the impedance is low enough to drive a large screen.

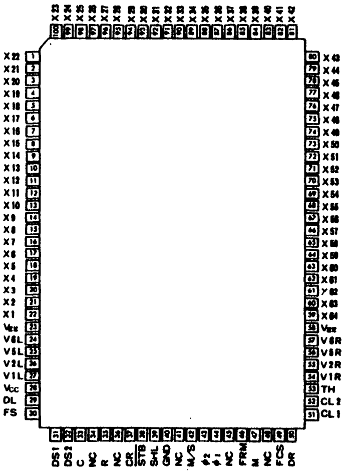


As the HD61103A is produced in a CMOS process, it is fit for use in portable battery drive equipments utilizing the liquid crystal display's low power consumption.
The user can easily construct a dot matrix liquid crystal graphic display system by combining the HD61103A and the column (segment) driver HD61102.

■ FEATURES

- Dot matrix liquid crystal graphic display common driver with low impedance.
- Low impedance —1.5kΩ max.
- Internal liquid crystal display driver circuit —— 64 circuits
- Internal dynamic display timing generator circuit
- Selectable display duty ratio factor 1/48, 1/64, 1/96, 1/128.
- Can be used as a column driver transferring data serially.
- Low power dissipation
  —— during display 5mW

■ PIN ARRANGEMENT


X23 X24 X25 X26 X27 X28 X29 X30 X31 X32 X33 X34 X35 X36 X37 X38 X39 X40 X41 X42
X22 X21 X20 X19 X18 X17 X16 X15 X14 X13 X12 X11 X10 X9 X8 X7 X6 X5 X4 X3 X2 X1
VEE V6L V5L V2L V1L VCC DL FS
X43 X44 X45 X46 X47 X48 X49 X50 X51 X52 X53 X54 X55 X56 X57 X58 X59 X60 X61 X62 X63 X64
VEE V6R V5R V2R V1R TH CL2 CL1
DS1 DS2 C NC R NC CR STB SHL GND NC M/S φ2 φ1 NC FRM M NC FCS DR

(Top View)

- Power supplies : V_{CC} — +5V ± 10%
  V_{EE} — 0 ∿ -11.5V
- LCD drive level — 17.0V max
- CMOS process
- 100-pin flat plastic package (FP-100)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Limit	Unit	Note
Power Supply Voltage (1)	V_{CC}	-0.3 ∿ +7.0	V	2
Power Supply Voltage (2)	V_{EE}	V_{CC}-19.0 ∿ V_{CC} +0.3	V	5
Terminal Voltage (1)	V_{T1}	-0.3 ∿ V_{CC} +0.3	V	2, 3
Terminal Voltage (2)	V_{T2}	V_{EE}-0.3 ∿ V_{CC} +0.3	V	4, 5
Operating Temperature	Topr	-20 ∿ +75	°C	
Storage Temperature	Tstg	-55 ∿ +125	°C	

Note 1) If LSI's are used beyond absolute maximum ratings, they may be permanently destroyed. We strongly recommend you to use the LSI within electrical characteristic limits for normal operation, because use beyond these conditions will cause malfunction and poor reliability.

Note 2) Based on GND=0V

Note 3) Applies to input terminals (except V1L, V1R, V2L, V2R, V5L, V5R, V6L and V6R) and I/O common terminals at high impedance.

Note 4) Applies to V1L, V1R, V2L, V2R, V5L, V5R, V6L and V6R.

Note 5) Apply the same value of voltages to V1L and V1R, V2L and V2R, V5L and V_{5R}, V6L and V6R, V_{EE}(23 pin) and V_{EE}(58 pin) respectively. Maintain $V_{CC} \geqq V1L=V1R \geqq V6L=V6R \geqq V5L=V5R$
$\geqq V2L=V2R \geqq V_{EE}$

■ ELECTRICAL CHARACTERISTICS

- DC Characteristics (V_{CC}=+5V ± 10%, GND=0V, V_{EE}=0 ∿ -11.5V
  Ta= -20 ∿ +75°C)

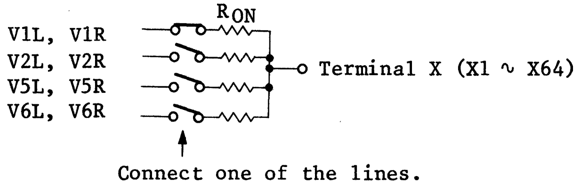
Test Item	Symbol	Test conditions	Specifications			Unit	Note
			Min	Typ	Max		
Input "High" voltage	V_{IH}		0.7×Vcc	-	V_{CC}	V	1
Input "Low" voltage	V_{IL}		GND	-	0.3×V_{CC}	V	1
Output "High" voltage	V_{OH}	I_{OH}=-0.4mA	V_{CC}-0.4	-	-	V	2
Output "Low" voltage	V_{OL}	I_{OL}=+0.4mA	-	-	+0.4	V	2
Vi-Xj ON resistance	R_{ON}	V_{CC}-V_{EE}=10V Load current ±150μA	-	-	1.5	KΩ	3
Input Leakage Current	I_{IL1}	Vin=0∿V_{CC}	-1.0	-	+1.0	μA	4
Input Leakage Current	I_{IL2}	Vin=V_{EE}∿V_{CC}	-2.0	-	+2.0	μA	5
Operating Frequency	f_{opr1}	In master mode External clock operation	50	-	600	kHz	6
Operating Frequency	fopr2	In slave mode Shift register	50	-	1500	kHz	7
Oscillation Frequency	fosc	Cf=20pF±5% Rf=47KΩ±2%	315	450	585	kHz	8,13
Dissipation Current (1)	I_{GG1}	In master mode 1/128 duty Cf=20pF Rf=47kΩ	-	-	1.0	mA	9,10
Dissipation Current (2)	I_{GG2}	In slave mode 1/128 duty	-	-	200	μA	9,11
Dissipation Current	I_{EE}	In master mode 1/128 duty	-	-	100	μA	9,12

Note 1) Applies to input terminals FS, DS1, DS2, CR, $\overline{\text{STB}}$, SHL, M/S, FCS, CL1 and TH and I/O common terminals DL, M, DR and CL2 in the input status.

Note 2) Applies to output terminals, ϕ1, ϕ2 and FRM and I/O common terminals DL, M, DR and CL2 in the output status.

Note 3) Resistance value between terminal X (one of X1 to X64) and terminal V (one of V1L, V1R, V2L, V2R, V5L, V5R, V6L and V6R) when load current is applied to each terminal X.

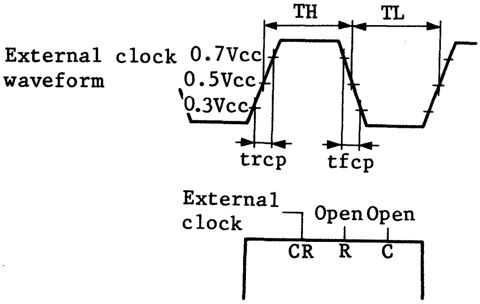
Equivalent circuit between terminal X and terminal V.



Note 4) Applies to input terminals FS, DS1, DS2, CR, $\overline{\text{STB}}$, SHL, M/S, FCS, CL1 and TH, I/O common terminals DL, M, DR and CL2 in the input status and NC terminals.

Note 5) Applies to V1L, V1R, V2L, V2R, V5L, V5R, V6L and V6R. Don't connect any lines to X1 to X64.

Note 6) External clock is as follows.

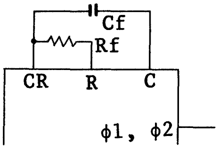


$$\text{Duty} = \frac{TH}{TH+TL} \times 100\%$$

	Min	Typ	Max	Unit
Duty	45	50	55	%
trcp	-	-	50	ns
tfcp	-	-	50	ns

Note 7) Applies to the shift register in the slave mode. For details, refer to AC Characteristics.

Note 8) Connect oscillation resistor (Rf) and oscillation capacitance (Cf) as shown in this figure. Oscillation frequency (f_{OSC}) is twice as much as the frequency ($f\phi$) at $\phi 1$ or $\phi 2$.



Cf=20pF
Rf=47kΩ fosc=2 × fϕ

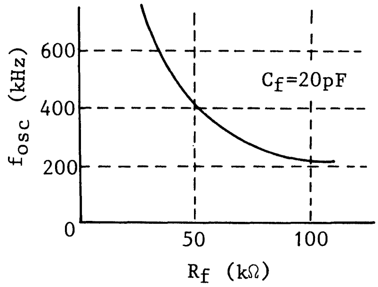
Note 9) No lines are connected to output terminals and current flowing through the input circuit is excluded. This value is specified at $V_{IH}=V_{CC}$ and $V_{IL}=GND$.

Note 10) This value is specified about current flowing through GND in the following conditions: Internal oscillation circuit is used. Each terminal of DS1, DS2, FS, SHL, M/S, $\overline{STB}$ and FCS is connected to V_{CC} and each of CL1 and TH to GND. Oscillator is set as described in Note 8.

Note 11) This value is specified about current flowing through GND under the following conditions: Each terminals of DS1, DS2, FS, SHL, $\overline{STB}$, FCS and CR is connected to V_{CC}, CL1, TH and M/S to GND and the terminals CL2, M and DL are respectively connected to terminals CL2, M and DL of the HD61103A under the condition described in Note 10.

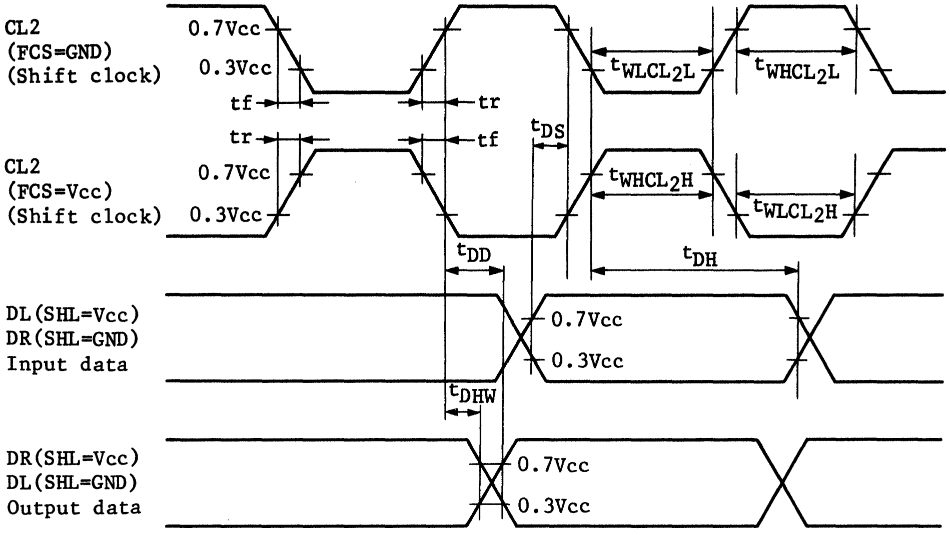
Note 12) This value is specified about current flowing through V_{EE} under the condition described in Note 10). Don't connect any lines to terminal V.

Note 13) This figure shows a typical relation among oscillation frequency, Rf and Cf. Oscillation frequency may vary with the mounting condition.



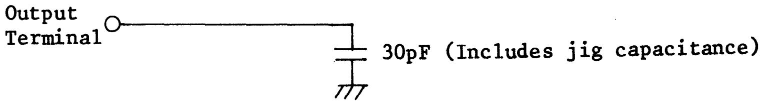
- AC Characteristics (V_{CC}=+5V±10% GND=0V, V_{EE}= 0 ∿ -11.5V Ta=-20 ∿ +75°C)

(1) In the slave mode (M/S=GND)



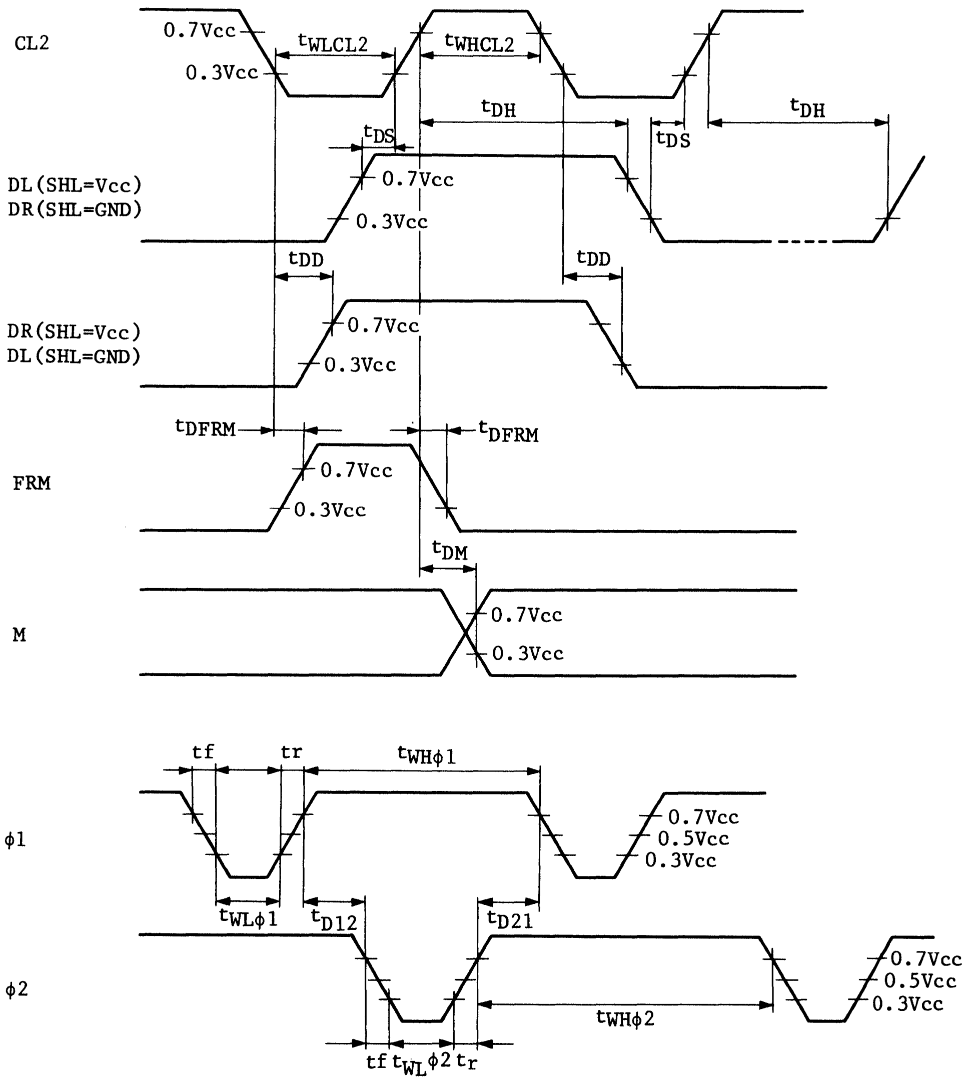
Item	Symbol	min.	typ.	max.	Unit	Note
CL2 "Low" level width (FCS=GND)	t_{WLCL2L}	450	-	-	ns	
CL2 "High" level width (FCS=GND)	t_{WHCL2L}	150	-	-	ns	
CL2 "Low" level width (FCS=V_{CC})	t_{WLCL2H}	150	-	-	ns	
CL2 "High" level width (FCS=V_{CC})	t_{WHCL2H}	450	-	-	ns	
Data setup time	t_{DS}	100	-	-	ns	
Data hold time	t_{DH}	100	-	-	ns	
Data delay time	t_{DD}	-	-	200	ns	1
Data hold time	t_{DHW}	10	-	-	ns	
CL2 rise time	tr	-	-	30	ns	
CL2 fall time	tf	-	-	30	ns	

Note 1) The following load circuit is connected for specification.



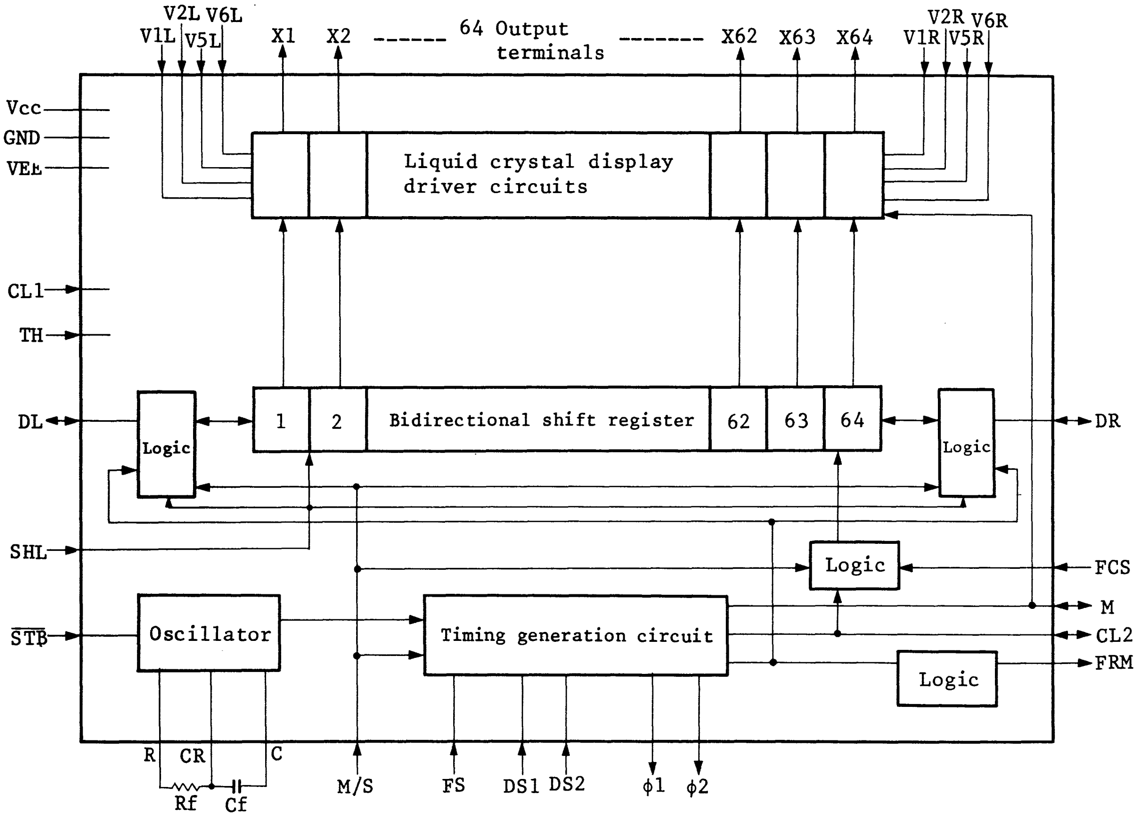
(2) In the master mode

(M/S=V_{CC}, FCS=V_{CC}, Cf=20pF, Rf=47KΩ)



Item	Symbol	min	typ	max	Unit	Note
Data setup time	t_{DS}	20	-	-	µs	
Data hold time	t_{DH}	40	-	-	µs	
Data delay time	t_{DD}	5	-	-	µs	
FRM delay time	t_{DFRM}	-2	-	+2	µs	
M delay time	t_{DM}	-2	-	+2	µs	
CL_2 "Low" level width	t_{WLCL2}	35	-	-	µs	
CL_2 "High" level width	t_{WHCL2}	35	-	-	µs	
$\phi 1$ "Low" level width	$t_{WL\phi 1}$	700	-	-	ns	
$\phi 2$ "Low" level width	$t_{WL\phi 2}$	700	-	-	ns	
$\phi 1$ "High" level width	$t_{WH\phi 1}$	2100	-	-	ns	
$\phi 2$ "High" level width	$t_{WH\phi 2}$	2100	-	-	ns	
$\phi 1$-$\phi 2$ phase difference	t_{D12}	700	-	-	ns	
$\phi 2$-$\phi 1$ phase difference	t_{D21}	700	-	-	ns	
$\phi 1$, $\phi 2$ rise time	tr	-	-	150	ns	
$\phi 1$, $\phi 2$ fall time	tf	-	-	150	ns	

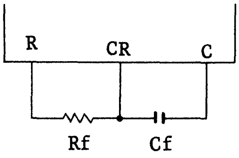
■ BLOCK DIAGRAM

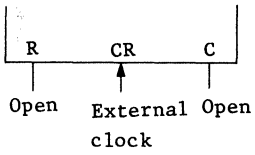


Block Functions

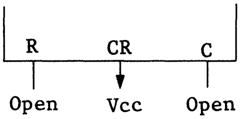
- Oscillator

The oscillator is a CR oscillator that generates display timing signals and operating clocks for the HD61102. It is required when the HD61103A is used with the HD61102. It attaches an oscillation resistor Rf and an oscillation capacity Cf as shown in the following figure and terminal $\overline{STB}$ is connected to "high" level. When using an external clock, input the clock into terminal CR and don't connect any lines to terminal R and C.





Oscillator is not required when the HD61103A is used with the HD61830. Then, connect terminal CR to "high" level and don't connect any lines to terminals R and C.



- Timing Generator Circuit

The timing generator circuit generates display timing and operating clock for the HD61102. This circuit is required when the HD61103A is used with the HD61102. Then connect terminal M/S to "high" level. (master mode).
It is not necessary when display timing signal is supplied from other circuits, for example, from HD61830. In this case connect the terminals FS, DS1 and DS2 to "high" level and M/S to "low" level. (Slave mode)

- Bidirectional Shift Register

This is a 64-bit bidirectional shift register. The data is shifted from DL to DR when SHL is at high level and from DR to DL when SHL is at low level. In this case, CL2 is used as shift clock. The lowest order bit of the bidirectional shift register, which is on the side of DL, corresponds to X1 and the highest order bit on the side of DR corresponds to X64.

- Liquid Crystal Display Driver Circuit

The combination of the data from the shift register with M signal allows one of the four liquid crystal display driver levels V1, V2, V5 and V6 to be transferred to the output terminals.

Data from the shift register	M	Output level
1	1	V2
0	1	V6
1	0	V1
0	0	V5

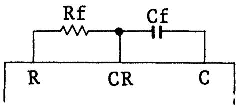
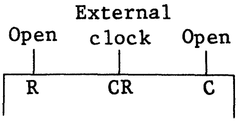
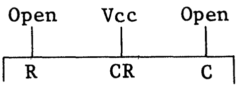
■ HD61103A TERMINAL FUNCTIONS

Terminal name	Number of terminals	I/O	Connected to	Function
VCC GND VEE	1 1 2		Power supply	V_{CC}-GND: Power supply for internal logic. V_{CC}-V_{EE}: Power supply for driver circuit logic.
V1L,V2L, V5L,V6L, V1R,V2R, V5R,V6R	8		Power supply	Liquid crystal display driver level power supply. V1L(V1R), V2L(V2R): Selected level V5L(V5R), V6L(V6R): Non-selected level voltages of the level power supplies connected to V1L and V1R should be the same. (This applies to the combination of V2L & V2R, V5L & V5R and V6L & V6R respectively)
M/S	1	I	V_{CC} or GND	Selects Master/Slave M/S=V_{CC}: In master mode When the HD61103A is used with the HD61102, timing generation circuit operates to supply display timing signals and operation clock to the HD61102. Each of I/O common terminals DL, DR, CL2 and M is in the output state. M/S=GND: In slave mode The timing operation circuit stops operating. The HD61103A is used in this mode when combined with the HD61830. Even if combined with the HD61102, this mode is used when display timing signals (M, data, CL2 etc.) are supplied by another HD61103A in the master mode. Terminals M and CL2 are in the input state. When SHL is V_{CC}, DL is in the input state and DR is in the output state. When SHL is GND, DL is in the output state and DR is in the input state.

- to be continued

<table>
<tr><th>Terminal name</th><th>Number of terminals</th><th>I/O</th><th>Connected to</th><th>Function</th></tr>
<tr><td>FCS</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects shift clock phase
FCS=V_{CC} Shift register operates at the rising edge of CL2. Select this condition when HD61103A is used with HD61102 or when MA of the HD61830 connects to CL2 in the combination with the HD61830.
FCS=GND Shift register operates at the fall of CL2. Select this condition when CL1 of HD61830 connects to CL2 in the combination with the HD61830.</td></tr>
<tr><td>FS</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects frequency
When the frame frequency is 70Hz, the oscillation frequency should be:
fosc=430kHz at FCS=V_{CC}
fosc=215kHz at FCS=GND
This terminal is active only in the master mode. Connect it to V_{CC} in the slave mode.</td></tr>
<tr><td>DS1,DS2</td><td>2</td><td>I</td><td>V_{CC} or GND</td><td>Selects display duty factor
<table>
<tr><th>Display Duty</th><th>1/48</th><th>1/64</th><th>1/96</th><th>1/128</th></tr>
<tr><td>DS1</td><td>GND</td><td>GND</td><td>V_{CC}</td><td>V_{CC}</td></tr>
<tr><td>DS2</td><td>GND</td><td>V_{CC}</td><td>GND</td><td>V_{CC}</td></tr>
</table>
This terminals are valid only in the master mode. Connect them to V_{CC} in the slave mode.</td></tr>
<tr><td>STB
TH
CL1</td><td>1
1
1</td><td>I</td><td>V_{CC} or GND</td><td>Input terminal for testing
Connect $\overline{STB}$ to V_{CC}.
Connect TH and CL1 to GND.</td></tr>
<tr><td>CR,R,C</td><td>3</td><td></td><td></td><td>Oscillator.
In the master mode, use these terminals as shown below.</td></tr>
</table>

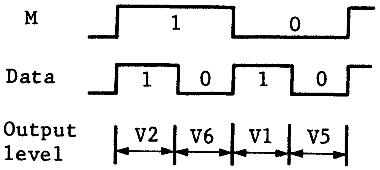
- to be continued

Terminal name	Number of terminals	I/O	Connected to	Function
CR,R,C	3			Usage of these terminal in the master mode Internal oscillation  External clock  In the slave mode, stop the oscillator as shown below. 
$\phi 1$, $\phi 2$	2	O	HD61102	Operating clock output terminals for the HD61102. Master mode: Connect these terminals to terminals $\phi 1$ and $\phi 2$ of the HD61102 respectively. Slave mode : Don't connect any lines to these terminals.
FRM	1	O	HD61102	Frame signal Master mode: Connect this terminal to terminals FRM of the HD61102. Slave mode : Don't connect any lines to this terminal.
M	1	I/O	MB of HD61830 or M of HD61102	Signal to convert LCD driver signal into AC. Master mode: Output terminal. Connect this terminal to terminal M of the HD61102. Slave mode : Input terminal. Connect this terminal to terminal MB of the HD61830.
CL2	1	I/O	CL1 or MA of HD61830 or CL of HD61102	Shift clock Master mode: Output terminal Connect this terminal to terminal CL of the HD61102.

- to be continued

<table>
<tr><th>Terminal name</th><th>Number of terminals</th><th>I/O</th><th>Connected to</th><th>Function</th></tr>
<tr><td>CL2</td><td>1</td><td>I/O</td><td>CL1 or MA of HD61830
or
CL of HD61102</td><td>Slave mode : Input terminal
Connect this terminal to terminal CL1 or MA of the HD61830.</td></tr>
<tr><td>DL, DR</td><td>2</td><td>I/O</td><td>Open or FLM of HD61830</td><td>Data I/O terminals of bidirectional shift register.
DL corresponds to X1's side and DR to X64's side.
Master mode : Output common scanning signal.
Don't connect any lines to these terminals normally.
Slave mode : Connect terminal FLM of the HD61830 to DL (when SHL=V_{CC}) or DR (when SHL=GND)
<table>
<tr><td>M/S</td><td colspan="2">V_{CC}</td><td colspan="2">GND</td></tr>
<tr><td>SHL</td><td>V_{CC}</td><td>GND</td><td>V_{CC}</td><td>GND</td></tr>
<tr><td>DL</td><td>Output</td><td>Output</td><td>Input</td><td>Output</td></tr>
<tr><td>DR</td><td>Output</td><td>Output</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>NC</td><td>5</td><td></td><td>Open</td><td>Not used.
Don't connect any lines to this terminal.</td></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects shift direction of bidirectional shift register.
<table>
<tr><td>SHL</td><td>Shift direction</td><td>Common scanning direction</td></tr>
<tr><td>V_{CC}</td><td>DL → DR</td><td>X1 → X64</td></tr>
<tr><td>GND</td><td>DL ← DR</td><td>X1 ← X64</td></tr>
</table></td></tr>
<tr><td>X1∿X64</td><td>64</td><td>0</td><td>Liquid crystal display</td><td>Liquid crystal display driver output.
Output one of the four liquid crystal display driver levels V1, V2, V5 and V6 with the combination of the data from the shift register and M signal.</td></tr>
</table>

- to be continued

Terminal name	Number of terminals	I/O	Connected to	Functions
X1∿X64	64	O	Liquid crystal display	 M 1 0 Data 1 0 1 0 Output level V2 V6 V1 V5 Data "1" — Selected level "0" — Non-selected level When SHL is V_{CC}, X1 corresponds to COM1 and X64 corresponds to COM64. When SHL is GND, X64 corresponds to COM1 and X1 corresponds to COM64.

■ EXAMPLE OF APPLICATION

HD61103A Connection List

H...V_{CC} } Fixed
L...GND }

"-" meanse "open".

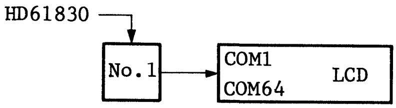
Rf...Oscillation resistor
Cf...Oscillation capacity

	M/S	TH	CL1	FCS	FS	DS1	DS2	$\overline{\text{STB}}$	CR	R	C	$\phi 1$	$\phi 2$	FRM	M	CL2	SHL	DL	DR	X1 ~ X64
A	L	L	L	L	H	H	H	H	H	-	-	-	-	-	from MB of HD61830	from CL1 of HD61830	H	from FLM of HD61830	-	COM1 ~COM64
																	L	-	from FLM of HD61830	COM64 ~COM1
B	L	L	L	H	H	H	H	H	H	-	-	-	-	-	from MB of HD61830	from MA of HD61830	H	from FLM of HD61830	to DL/DR of HD61103A No.2	COM1 ~COM64
																	L	to DL/DR of HD61103A No.2	from FLM of HD61830	COM64 ~COM1
C	L	L	L	H	H	H	H	H	H	-	-	-	-	-	from MB of HD61830	from MA of HD61830	H	from DL/DR of HD61103A No.1	-	COM65 ~COM128
																	L	-	from DL/DR of HD61103A No.1	COM128~COM65
D	H	L	L	H	H	L or L	L H	H	Rf Cf	Rf	Cf	to $\phi 1$ of HD61102	to $\phi 2$ of HD61102	to FRM of HD61102	to M of HD61102	to CL of HD61102	H	-	-	COM1 ~COM64
																	L	-	-	COM64 ~COM1
E	H	L	L	H	H	L or L	L H	H	Rf Cf	Rf	Cf	to $\phi 1$ of HD61102	to $\phi 2$ of HD61102	to FRM of HD61102	to M of HD61102 HD61103A	to CL of HD61102 to CL2 of HD61103A	H	-	to DL/DR of HD61103A No.2	COM1 ~COM64
																	L	to DL/DR of HD61103A No.2	-	COM64 ~COM1
F	L	L	L	H	H	H	H	H	H	-	-	-	-	-	from M of HD61103A No.1	from CL2 of HD61103A No.1	H	from DL/DR of HD61103A No.1	-	COM1 ~COM64
																	L	-	from DL/DR of HD61103A No.1	COM64 ~COM1

Outline of HD61103A System Configuration

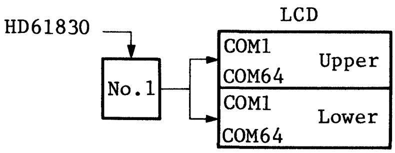
1) Use with HD61830

a) When display duty ratio of LCD is more than 1/64



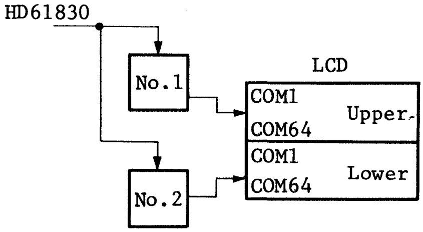
One HD61103A drives common signals.

Refer to Connection list 'A'



One HD61103A drives common signals for upper and lower panels.

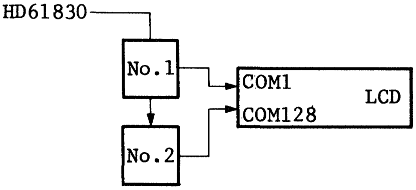
Refer to Connection list 'A'



Two HD61103A's drive upper and lower panel separately to ensure the quality of display. No.1 and No.2 operate in parallel.

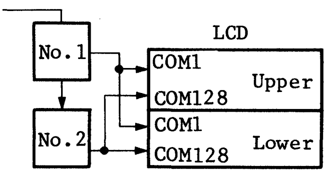
For both of No.1 and No.2, refer to Connection list 'A'

b) When display duty ratio of LCD is from 1/65 to 1/128



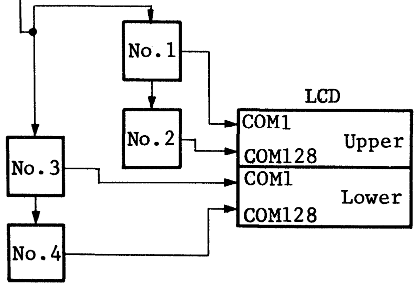
Two HD61103A's connected serially drive common signals.

Refer to Connection list 'B' for No.1.
Refer to Connection list 'C' for No.2.



Two HD61103A's connected serially drive upper and lower panels in parallel.

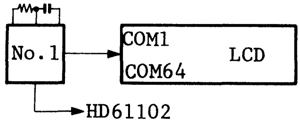
Refer to Connection list 'B' for No.1.
Refer to Connection list 'C' for No.2.



Two sets of HD61103A's connected serially drive upper and lower panels in parallel to ensure the quality of display.

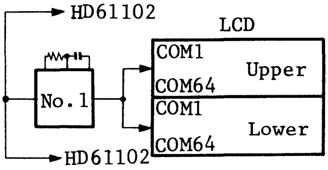
Refer to Connection list 'B' for No.1 and 3.
Refer to Connection list 'C' for No.2 and 4.

2) Use with HD61102 (1/64 duty)



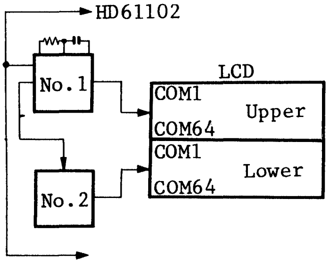
One HD61103A drives common signals and supplies timing signals to the HD61102's.

Refer to Connection list 'D"



One HD61103A drives upper and lower panels and supplies timing signals to the HD61102's.

Refer to Connection list 'D'



Two HD61103A's drive upper and lower panels in parallel to ensure the quality of display. No.1 supplies timing signals to No.2 and the HD61102's.

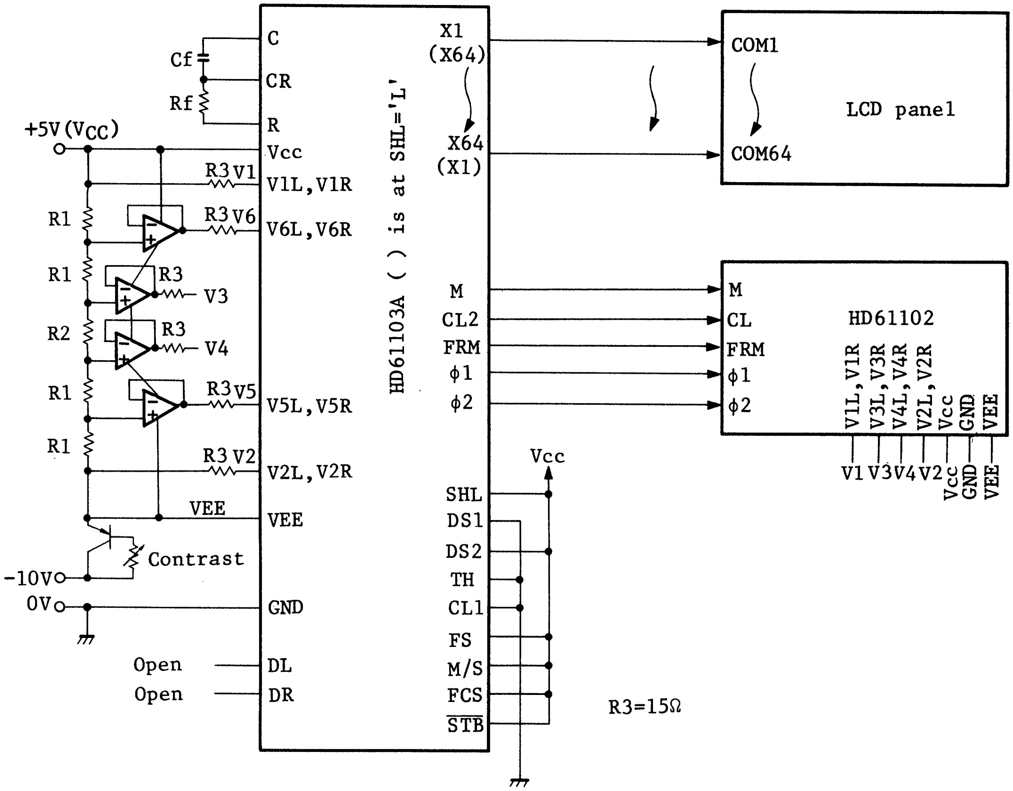
Refer to Connection list 'E' for No.1

Refer to Connection list 'F' for No.2

- Example of Connection 1)

° Use with HD61102 (RAM type segment driver)

a) 1/64 duty ratio (See Connection List "D")



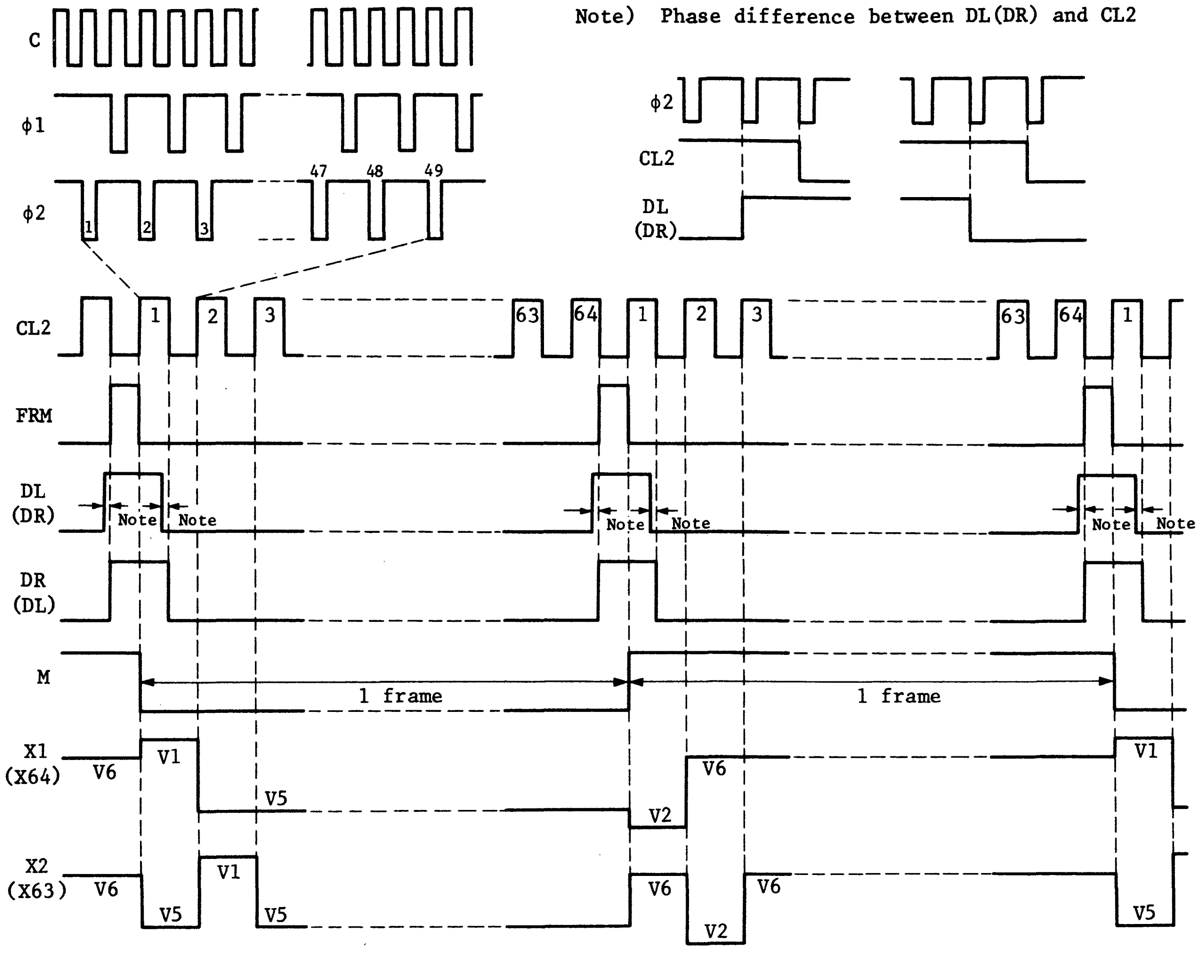
Note 1) The values of R1 and R2 vary with the LCD panel used.
When bias factor is 1/9, the values of R1 and R2 should satisfy

$$\frac{R1}{4R1 + R2} = \frac{1}{9}$$

For example,

R1=3kΩ, R2=15kΩ

Example of Waveform (RAM type, 1/64 duty)



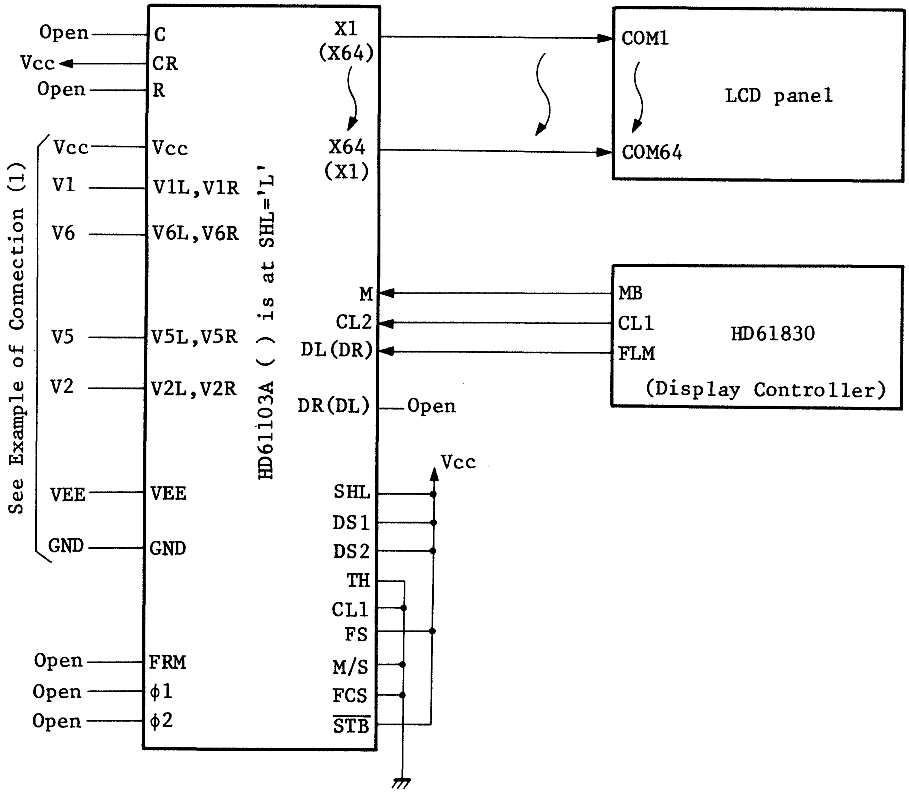
Note) Phase difference between DL(DR) and CL2

( ) ... at SHL='L'

Example of Connection 2)

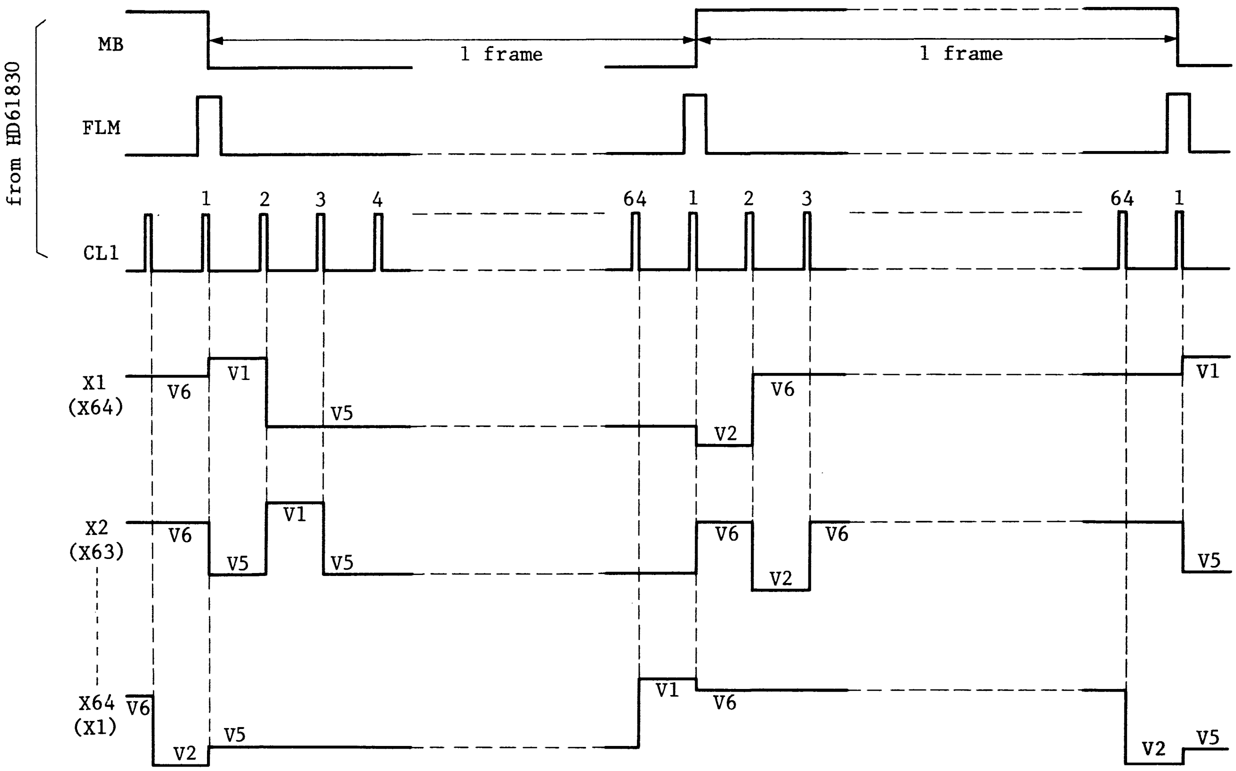
- Use with HD61830 (Display controller)

a) 1/64 duty ratio (See Connection List "A")



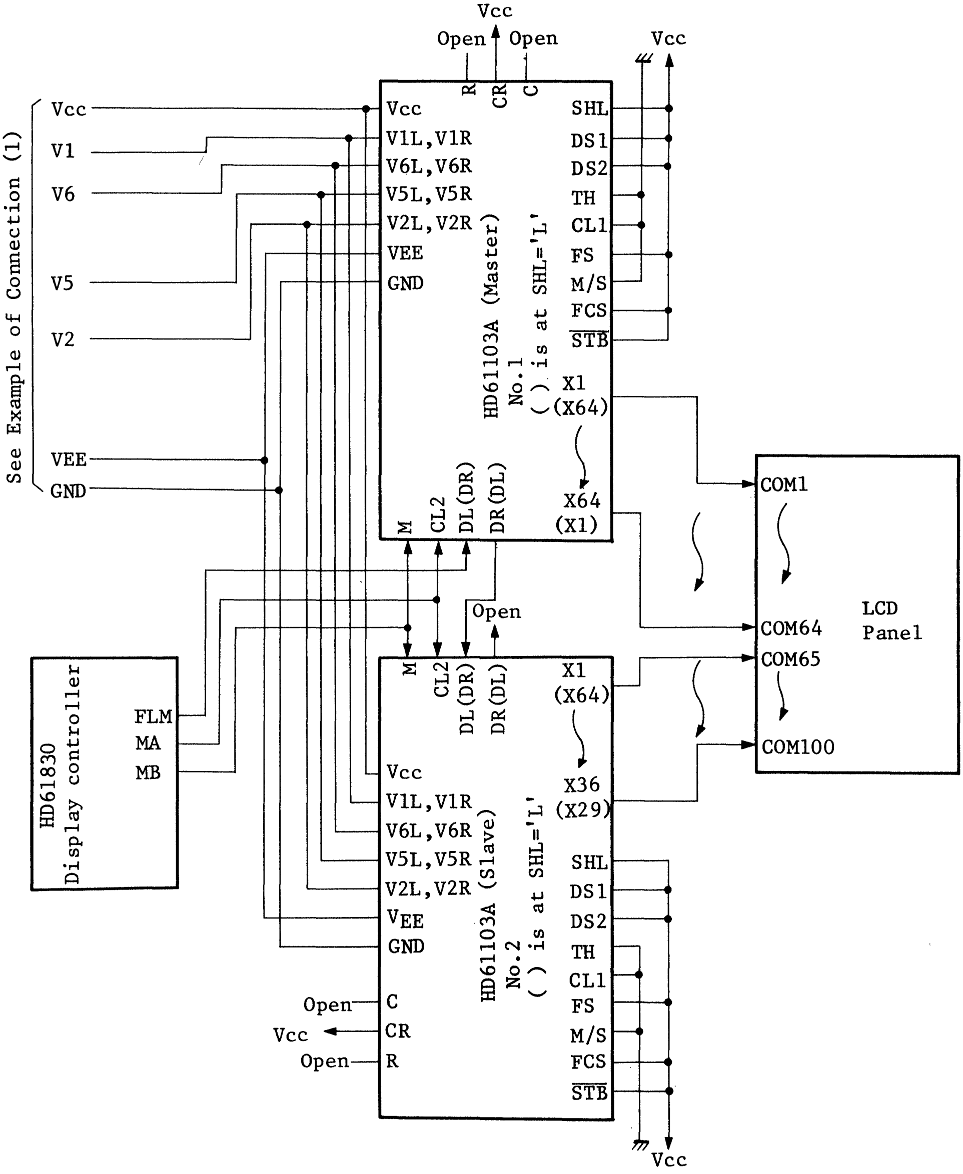
Example of Waveform

a) 1/64 duty ratio

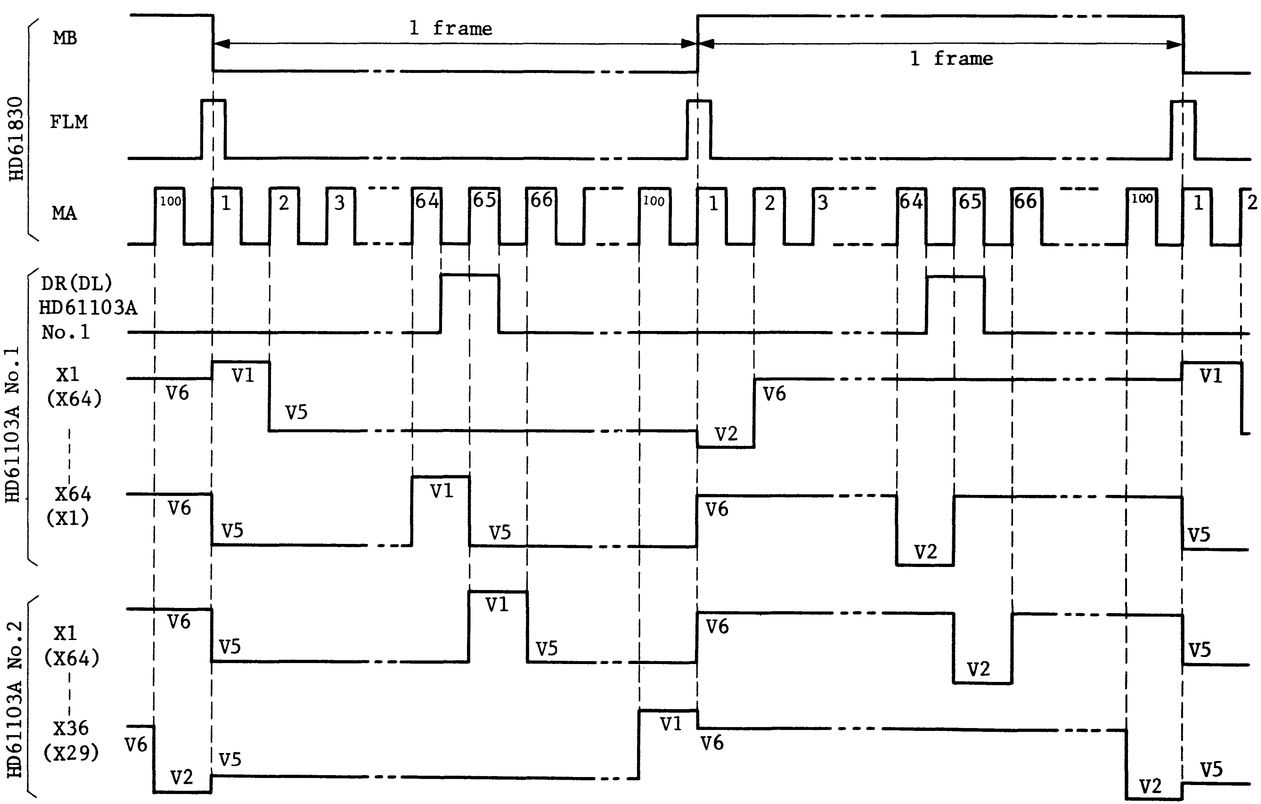


( ) ... at SHL='L'

b) 1/100 duty ratio (See Connection List 'B' 'C')



Example of Waveform b) 1/100 duty



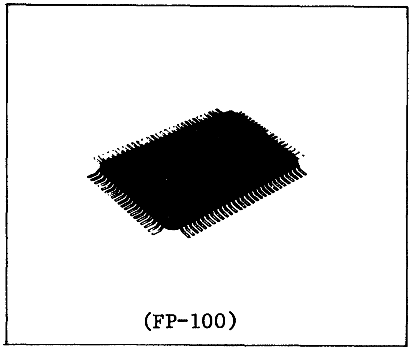
( ): Case of SHL=Low level.

HD61200

(LCD Driver with 80-Channel Output)

DESCRIPTION

The HD61200 is a colume driver LSI for a large-area dot matrix LCD. This employs 1/32 or more duty multiplexing method. It receives serial display data from a microcomputer or a display control LSI, HD61830, etc., and generates liquid crystal driving signals.

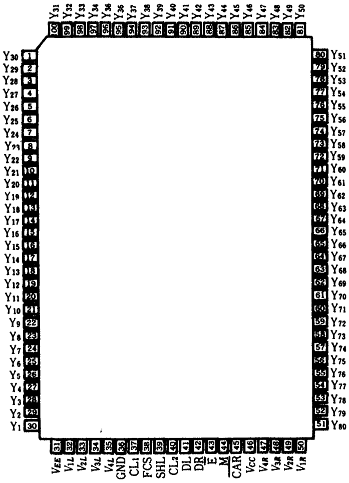


(FP-100)

FEATURES

- Liquid crystal display driver with serial/parallel conversion function.
- Internal liquid crystal display driver .... 80 drivers
- Drives liquid crystal panels with 1/32 - 1/128 duty multiplexing.
- Capable of interfacing to LCD controllers, HD61830 and HD61830B.
- Data transfer rate .... 2.5 MHz max
- Power supply
  Vcc - 5V±10% (Internal logic)
- Power supply voltage for liquid crystal display drive ... 8V ∿ 17V
- CMOS process
- 100-pin flat plastic package (FP-100)

PIN ARRANGEMENT



(Top View)

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply voltage (1)	V_{CC}	-0.3 to +7.0	V	2
Supply voltage (2)	V_{EE}	V_{cc}-19.0 to Vcc+0.3	V	
Terminal voltage (1)	V_{T1}	-0.3 to Vcc +0.3	V	2, 3
Terminal voltage (2)	V_{T2}	V_{EE}-0.3 to Vcc+0.3	V	4
Operating temperature	Topr	-20 to +75	°C	
Storage temperature	Tstg	-55 to +125	°C	

(Note 1) LSI's may be permanently destroyed if being used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the limits of electrical characteristics, because using beyond these conditions may cause malfunction and poor reliability.

(Note 2) All voltage values are referred to GND=0V.

(Note 3) Applies to input terminals, FCS, SHL, CL1, CL2, DL, DR, $\overline{E}$ and M.

(Note 4) Applies to V_{1L}, V_{1R} V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L} and V_{4R}. Must maintain

$V_{CC} \geqq V_{1L} = V_{1R} \geqq V_{3L} = V_{3R} \geqq V_{4L} = V_{4R} \geqq V_{2L} = V_{2R} \geqq V_{EE}$.

Connect a protection resistor of 47Ω±10% to each terminals in series.

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS

(Vcc=5V±10%, GND=0V, Vcc-VEE=8V∿17V Ta=-20∿75°C)

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
Input "High" voltage	V_{IH}		$0.7 \times V_{CC}$	-	V_{CC}	V	1
Input "Low" voltage	V_{IL}		0	-	$0.3 \times V_{CC}$	V	1
Output "High" voltage	V_{OH}	I_{OH}=-400μA	V_{CC}-0.4	-	-	V	2
Output "Low" voltage	V_{OL}	I_{OL}=400μA	-	-	0.4	V	2
Driver ON Resistance	R_{ON}	Load current= 100μA	-	-	7.5	kΩ	5
Input Leakage Current	I_{IL1}	V_{IN}=0 to V_{CC}	-1	-	1	μA	1
Input Leakage Current	I_{IL2}	V_{IN}=V_{EE} to VCC	-2	-	2	μA	3
Dissipation Current(1)	I_{GND}		-	-	1.0	mA	4
Dissipation Current(2)	I_{EE}		-	-	0.1	mA	4

(Note 1) Applies to CL1, CL2, SHL, $\overline{E}$, M, DL and DR.

(Note 2) Applies to $\overline{CAR}$.

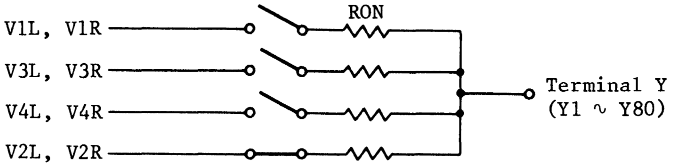
(Note 3) Applies to V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L} and V_{4R}.

(Note 4) Specified when display data is transfered under following conditions.

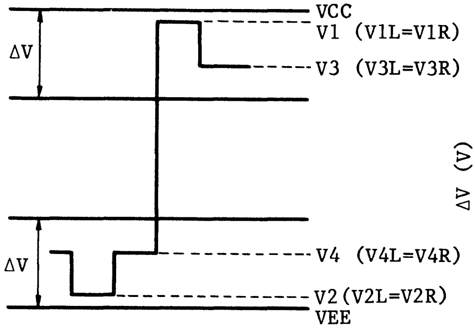
CL2 frequency f_{CP2} = 2.5MHz (data transfer rate)
CL1 frequency f_{CP1} = 4.48kHz (data latch frequency)
M frequency f_M = 35Hz (frame frequency/2)
Specified at V_{IH}=V_{CC} (V), V_{IL}=0V and no load on outputs.
I_{GND} : currents between V_{CC} and GND.
I_{EE} : currents between V_{CC} and V_{EE}.

(Note 5) Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V3L, V3R, V4L and V4R) when load current flows through one of the terminals Y1 to Y80. This value is specified under the following condition.

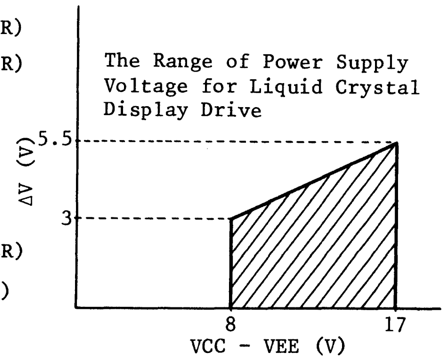
VCC - VEE = 17 V
V1L=V1R, V3L=V3R = VCC-2/7(VCC-VEE)
V2L=V2R, V4L=V4R = VEE+2/7(VCC-VEE)



Here is a description of the range of power supply voltage for liquid crystal display drive. Apply positive voltage to V1L=V1R and V3L=V3R and negative voltage to V2L=V2R and V4L=V4R within the ΔV range. This range allows stable impedance on driver output (RON). Notice the ΔV depends on power supply voltage VCC-VEE.



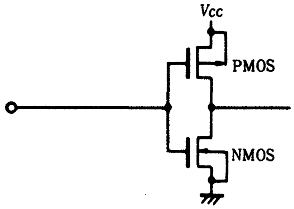
Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive



Correlation between Power Supply Voltage VCC-VEE and ΔV

TERMINAL CONFIGURATION

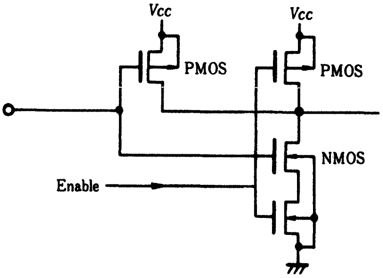
- Input Terminal

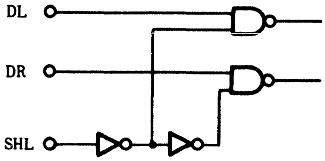


Applicable terminals :
CL1, CL2, SHL, $\overline{E}$, M

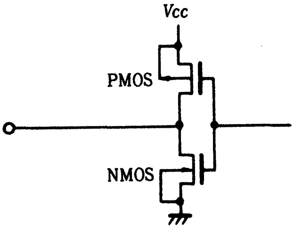
- Input Terminal (with Enable)

Applicable terminal: DL DR





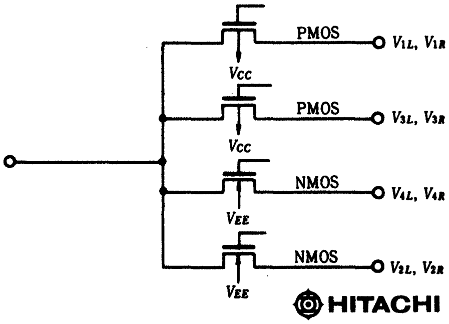
- Output Terminal



Applicable terminal : $\overline{CAR}$

- Output Terminal

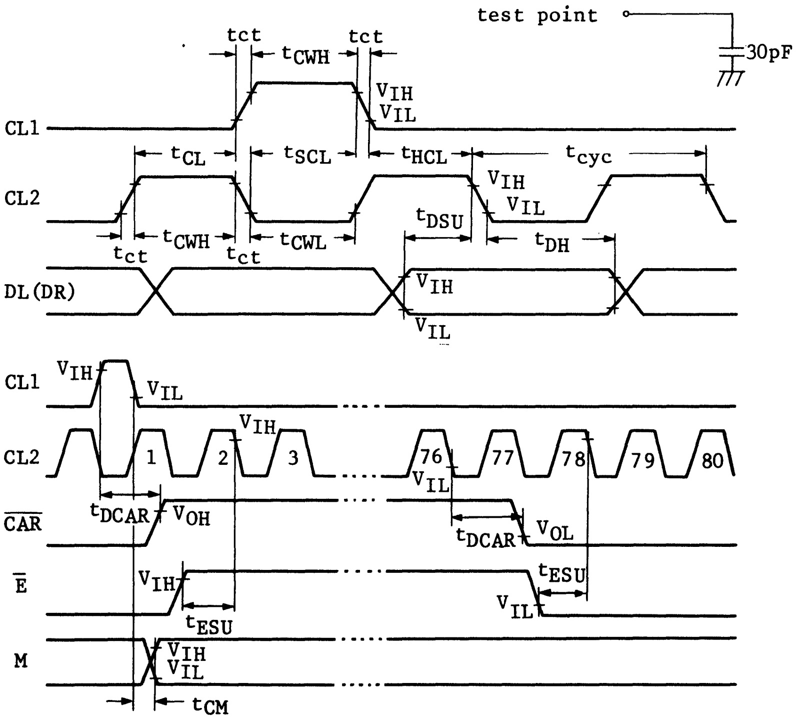
Applicable terminals:
Y1 ∿ Y80



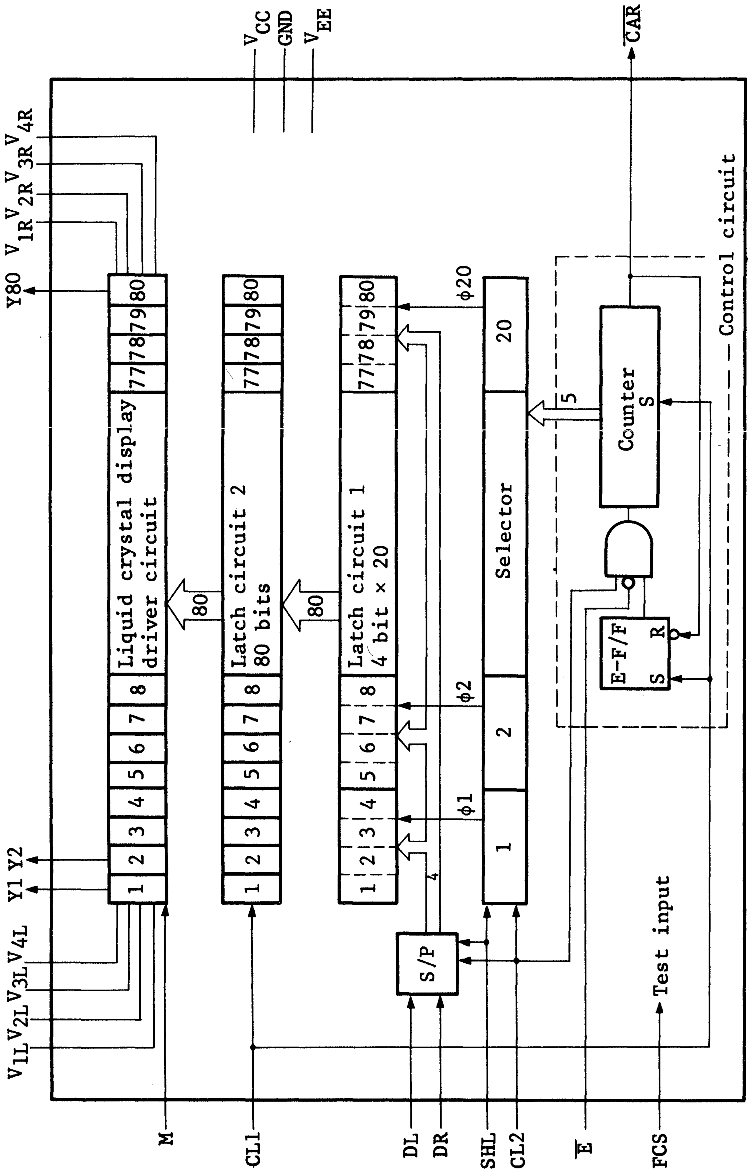
- AC CHARACTERISTICS
(Vcc=5V±10%, GND=0V, Ta=-20∿ +75°C)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit	Note
Clock cycle time	t_{CYC}		400	-	-	ns	
Clock high level width	t_{CWH}		150	-	-	ns	
Clock low level width	t_{CWL}		150	-	-	ns	
Clock setup time	t_{SCL}		100	-	-	ns	
Clock hold time	t_{HCL}		100	-	-	ns	
Clock rise/fall time	t_{Ct}		-	-	30	ns	
Clock phase different time	t_{CL}		100	-	-	ns	
Data setup time	t_{DSU}		80	-	-	ns	
Data hold time	t_{DH}		100	-	-	ns	
E setup time	t_{ESU}		200	-	-	ns	
Output delay time	t_{DCAR}		-	-	300	ns	1
M phase difference time	t_{CM}		-	-	300	ns	

(Note 1) The following load circuits are connected for specification:



■ BLOCK DIAGRAM



BLOCK FUNCTION

Liquid Crystal Display Driver Circuit

The combination of the data from the latch circuit 2 and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3 and V4 to be output.

80-bit Latch Circuit 2

The data from latch circuit 1 is latched at the fall of CL1 and output to liquid crystal display driver circuit.

S/P

Serial/Parallel conversion circuit which converts 1-bit data into 4-bit data. When SHL is "L" level, data from DL is converted into 4-bit data and transferred to the latch circuit 1. In this case, don't connect any lines to terminal DR.

When SHL is "H" level, input data from terminal DR without connecting any lines to terminal DL.

80-bit Latch Circuit 1

The 4-bit data is latched at $\phi 1 \sim \phi 20$ and output to latch circuit 2. When SHL is "L" level, the data from DL are latched one in order of 1→2→3 ... →80 of each latch. When SHL is "H" level, they are latched in a reverse order (80→79→78 ... →1).

Selector

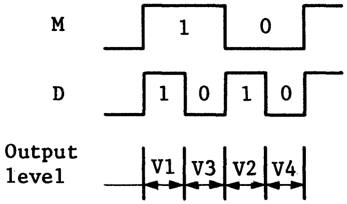
The selector decodes output signals from the counter and generates latch clock $\phi 1$ to $\phi 20$. When the LSI is not active, $\phi 1 \sim \phi 20$ are not generated, so the data at latch circuit 1 is stored even if input data (DL, DR) changes.

Control Circuit

Controls operation : When E-F/F (enable F/F) indicates "1", S/P conversion is started by inputting "L" level to $\overline{E}$. After 80-bit data has been all converted, $\overline{CAR}$ output turns into "L" level and E-F/F is reset to "0", and consequently the conversion stops. E-F/F is RS flip-flop circuit which gives priority to SET over RESET and is set at "H" level of CL1.

Counter consists of 7 bits, and the output signals of upper 5 bits are transferred to the selector. $\overline{CAR}$ signal turns into "H" level at the rise of CL1 and the number of bit which can be S/P-converted increases by connecting $\overline{CAR}$ terminal with $\overline{E}$ terminal of the next HD61200.

TERMINAL FUNCTIONS DESCRIPTION

Terminal name	Number of terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 1		Power supply	V_{CC}-GND : Power supply for internal logic V_{CC}-V_{EE} : Power supply for LCD drive circuit
$V_{1L} \sim V_{4L}$ $V_{1R} \sim V_{4R}$	8		Power supply	Power supply for liquid crystal drive V_{1L} (V_{1R}), V_{2L} (V_{2R})...selection level V_{3L} (V_{3R}), V_{4L} (V_{4R})...non-selection level Power supplies connected with V_{1L} and V_{1R}(V_{2L} & V_{2R}, V_{3L} & V_{3R}, V_{4L} & V_{4R}) should have the same voltages.
$Y1 \sim Y80$	80	O	LCD	Liquid crystal driver outputs Selects one of the 4 levels, V1, V2, V3 and V4. Relation among output level, M and display data (D) is as follows.  M 1 0 D 1 0 1 0 Output level V1 V3 V2 V4
M	1	I	Controller	Switch signal to convert liquid crystal drive waveform into AC.
CL1	1	I	Controller	Synchronous Signal (a counter is reset at "High" level) Latch clock of display data (fall edge trigger). Synchronizing with the fall of CL1, liquid crystal driver signals corresponding to the display data are output.
CL2	1	I	Controller	Shift clock of display data (D) Fall edge trigger

<table>
<tr><th>Terminal name</th><th>Number of terminals</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>DL, DR</td><td>2</td><td>I</td><td>Controller</td><td>Input of serial display data (D)
<table>
<tr><th>(D)</th><th>Liquid crystal driver output</th><th>Liquid crystal display</th></tr>
<tr><td>1 (H level)</td><td>selection level</td><td>ON</td></tr>
<tr><td>0 (L level)</td><td>non-selection level</td><td>OFF</td></tr>
</table>
</td></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects a shift direction of serial data.
When the serial data (D) is input in order of D1→ ... →D80, the relations between the data (D) and output Y are as follows.
<table>
<tr><th>SHL</th><th>Y1</th><th>Y2</th><th>Y3</th><th>....</th><th>Y80</th></tr>
<tr><td>"L"</td><td>D1</td><td>D2</td><td>D3</td><td>....</td><td>D80</td></tr>
<tr><td>"H"</td><td>D80</td><td>D79</td><td>D78</td><td>....</td><td>D1</td></tr>
</table>
When SHL is "L", data is input from the terminal DL. Any lines should not be connected to the terminal DR.
When SHL is "H", the relation between DL and DR reverses.</td></tr>
<tr><td>$\overline{E}$</td><td>1</td><td>I</td><td>GND or the terminal $\overline{\text{CAR}}$ of the HD61200</td><td>Controls the S/P conversion.
The operation stops with "H" level, and the S/P conversion starts with "L" level.</td></tr>
</table>

Terminal name	Number of terminals	I/O	Connected to	Functions
$\overline{\text{CAR}}$	1	O	the input terminal $\overline{\text{E}}$ of the HD61200	Used for cascade connection with the HD61200 to increase the number of bit which can be S/P converted.
FCS	1	I	GND	Input terminal for test. Connect to GND.

■ THE OPERATION OF THE HD61200

The following is the LCD panel with 64 × 240 dots on which characters are displayed with 1/64 duty dynamic drive. Fig. 1 is an example of liquid crystal display and connection to HD61200 's. Fig. 2 shows a time chart of I/O signals of HD61200

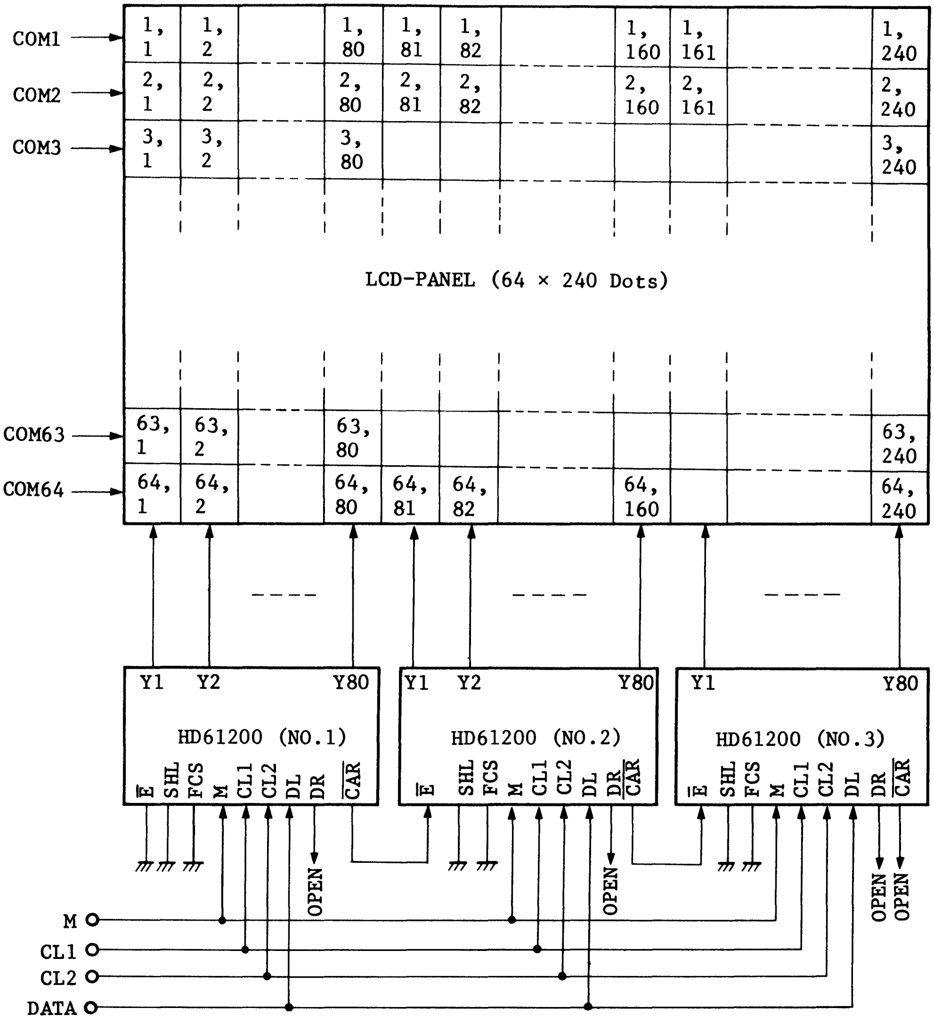
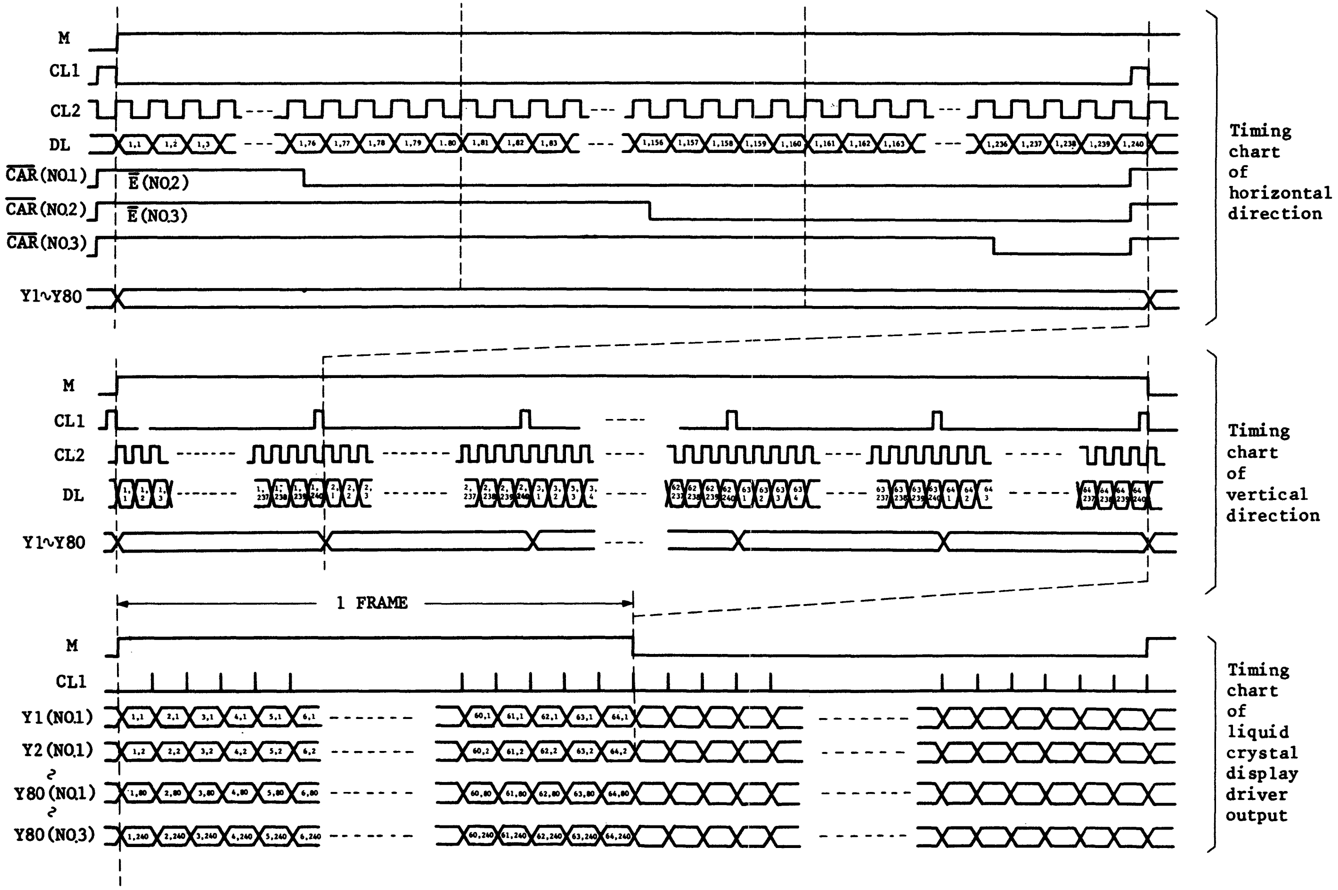


Fig. 1 LCD driver with 64 × 240 dots

Cascade three HD61200 s. Input data to the terminal DL of NO.1, NO.2 and NO.3. Connect $\overline{E}$ of NO.1 to GND. Don't connect any lines to $\overline{CAR}$ of NO.3. Connect common signal terminals (COM1 ∿ COM64) to X1 ∿ X64 of common driver HD61203. (m,n) of LCD panel is the address corresponding to each dot.

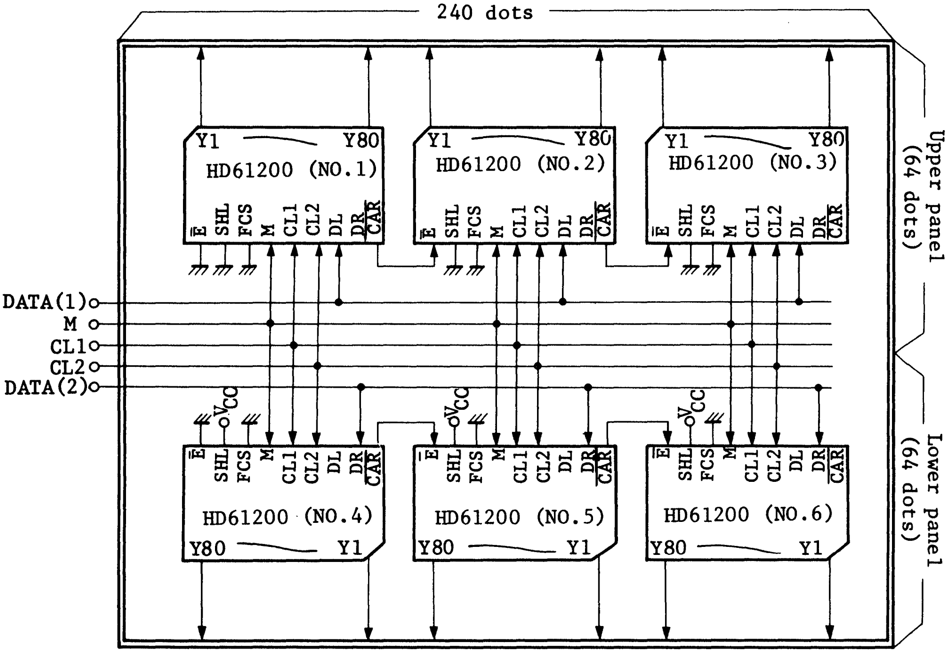

M
CL1
CL2
DL
CAR(NO.1)
CAR(NO.2)
CAR(NO.3)
E(NO.2)
E(NO.3)
Y1~Y80
Timing chart of horizontal direction
Timing chart of vertical direction
1 FRAME
Y1(NO.1)
Y2(NO.1)
Y80(NO.1)
Y80(NO.3)
Timing chart of liquid crystal display driver output

Timing chart in the example of connection of Fig.1. DL input (m,n) is the data which corresponds to each address (m,n) of LCD panel.

Fig. 2 HD61200 Timing Chart

■ EXAMPLE OF APPLICATION

- An example of 128 × 240 dot liquid crystal display (1/64 duty)



Liquid crystal panel is divided into upper and lower parts. These two parts are driven separately. HD61200s of No.1 ∿ No.3 drive upper half. Serial data, which are input from DATA (1) terminal, appear at $Y_1 \rightarrow Y_2 \rightarrow$ -- Y_{80} terminal of No.1, then at $Y_1 \rightarrow Y_2 \rightarrow$ -- Y_{80} of No.2 and then at $Y_1 \rightarrow Y_2 \rightarrow$ -- Y_{80} of No.3 in order where they were input. (in the case of SHL=L). HD61200s of No.4 ∿ No.6 drive lower half. Serial data, which are input from DATA (2) terminal, appear at $Y_{80} \rightarrow T_{79} \rightarrow$ -- Y_1 of No.4, then at $Y_{80} \rightarrow Y_{79} \rightarrow$ -- Y_1 of No.5 and then $Y_{80} \rightarrow Y_{79} \rightarrow$ -- Y_1 of No.6 in order where they were input (in the case of SHL=H).

As shown in this example, PC board for display divided into upper and lower half can be easily designed by using SHL terminal effectively.

HD61202
(Dot Matrix Liquid Crystal Graphic Display Column Driver)

DESCRIPTION

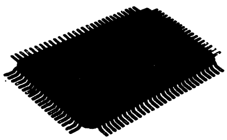
HD61202 is a column (segment) driver for dot matrix liquid crystal graphic display systems. It stores the display data transferred from a 8-bit microcomputer in the internal display RAM and generates dot matrix liquid crystal driving signals.

Each bit data of display RAM corresponds to ON/OFF of each dot of liquid crystal display to provide more flexible display.

As it is internally equipped with 64 output drivers for display, it is available for liquid crystal graphic display with many dots.

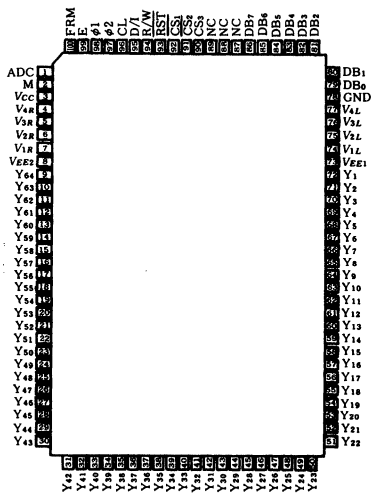
The HD61202 which is produced in the CMOS process, can accomplish a portable battery drive equipment by combining a CMOS micro-computer, utilizing the liquid crystal display's lower power dissipation.

Moreover it can facilitate dot matrix liquid crystal graphic display system configuration by combining the row (common) driver HD61203.



(FP-100)

PIN ARRANGEMENT



(Top View)

FEATURES

- Dot matrix liquid crystal graphic display column driver incorporating display RAM.
- RAM data direct display by internal display RAM
  - RAM bit data "1" .... ON
  - RAM bit data "0" .... OFF
- Internal display RAM address counter preset, increment
- Display RAM capacity .... 512 bytes (4096 bits)

- 8-bit parallel interface
- Internal liquid crystal display driver circuit 64
- Display duty

  Drives liquid crystal panels with 1/32 ∿ 1/64 duty multiplexing.
- Wide range of instruction function

  Display Data Read/Write, Display ON/OFF, Set address, Set Display Start line, Read Status
- Lower power dissipation.........during display 2mW max
- Power supply Vcc.........5V ± 10%
- Liquid crystal display driving voltage... 8V ∿ 17.0V
- CMOS process
- 100 - pin flat plastic package (FP-100)

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	-0.3 ∿ +7.0	V	2
	VEE1 VEE2	V_{CC} -19.0 ∿ V_{CC} +0.3	V	3
Terminal voltage (1)	V_{T1}	V_{EE} -0.3 ∿ V_{CC} +0.3	V	4
Terminal voltage (2)	V_{T2}	-0.3 ∿ V_{CC} +0.3	V	2, 5
Operating temperature	Topr	-20 ∿ +75	°C	
Storage temperature	Tstg	-55 ∿ +125	°C	

(Note 1) LSI's may be destroyed for ever, if being used beyond the absolute maximum ratings.
In ordinary operation, it is desirable to use them observing the recommended operation conditions.
Using beyond these conditions may cause malfunction and poor reliability.

(Note 2) All voltage values are referred to GND=0V.

(Note 3) Apply the same supply voltage to V_{EE} 1 and V_{EE2}.

(Note 4) Applies to V1L, V2L, V3L, V4L, V1R, V2R, V3R and V4R.
Maintain
Vcc≧V1L=V1R≧V3L=V3R≧V4L=V4R≧V2L=V2R≧VEE

(Note 5) Applies to M, FRM, CL, $\overline{\text{RST}}$, ADC, $\phi 1$, $\phi 2$, $\overline{\text{CS1}}$, $\overline{\text{CS2}}$, CS3, E, R/W, D/I, and DB0∿7.

■ ELECTRICAL CHARACTERISTICS

(GND=0V, VCC=4.5 ∿ 5.5V, Vcc-VEE=8∿17.0V, Ta=-20∿+75°C)

Item	Symbol	Test condition	Limit			Unit	Note
			Min.	Typ.	Max.		
Input "High" voltage	V_{IHC}		0.7×Vcc	-	Vcc	V	1
	V_{IHT}		2.0	-	Vcc	V	2
Input "Low" voltage	V_{ILC}		0	-	0.3×Vcc	V	1
	V_{ILT}		0	-	0.8	V	2
Output "High" voltage	V_{OH}	IOH=-205μA	2.4	-	-	V	3
Output "Low" voltage	V_{OL}	IOL=1.6mA	-	-	0.4	V	3
Input leakage current	I_{IL}	Vin=GND∿Vcc	-1.0	-	+1.0	μA	4
Three state (OFF) input current	I_{TSL}	Vin=GND∿Vcc	-5.0	-	+5.0	μA	5
Liquid crystal supply leakage current	I_{LSL}	Vin=VEE∿Vcc	-2.0	-	+2.0	μA	6
Driver ON resistance	R_{ON}	Vcc-VEE=15V $\pm I_{LOAD}$=0.1mA	-	-	7.5	kΩ	8
Dissipation current	Icc(1)	During display	-	-	100	μA	7
	Icc(2)	During access access cycle=1MHz	-	-	500	μA	7

(Note 1) Applies to M, FRM, CL, $\overline{\text{RST}}$, φ1 and φ2.

(Note 2) Applies to $\overline{\text{CS1}}$, $\overline{\text{CS2}}$, CS3, E, R/W, D/I and DB0 ∿ 7.

(Note 3) Applies to DB0 ∿ 7.

(Note 4) Applies to terminals except for DB0 ∿ 7.

(Note 5) Applies to DB0 ∿ 7 at high impedance.

(Note 6) Applies to V1L ∿ V4L and V1R ∿ V4R.

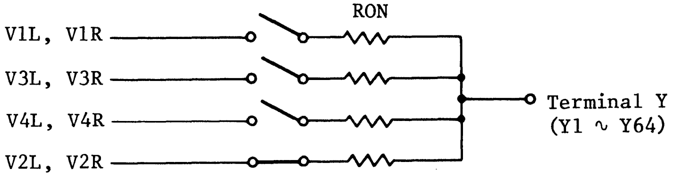
(Note 7) Specified when liquid crystal display is in 1/64 duty.
Operation frequency f_{CLK}=250 kHz (φ1 and φ2 frequency)
Frame frequency f_M = 70 Hz (FRM frequency)

Specified in the state of
Output terminal ----- not loaded
Input level --------- V_{IH}=Vcc(V)
V_{IL}=GND (V)

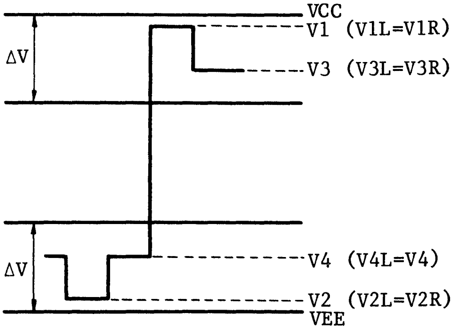
Measured at Vcc terminal

(Note 8) Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V3L, V3R, V4L and V4R) when load current flows through one of the terminals Y1 to Y64. This value is specified under the following condition.

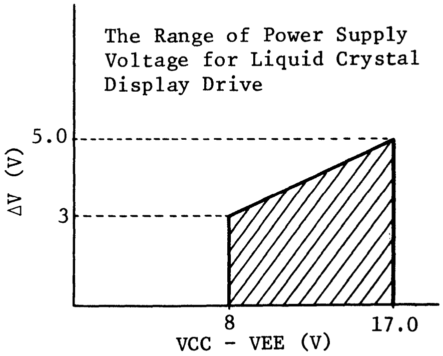
VCC - VEE = 15.5V
V1L=V1R, V3L=V3R = VCC-2/7 (VCC-VEE)
V2L=V2R, V4L=V4R = VEE+2/7 (VCC-VEE)



Here is a description of the range of power supply voltage for liquid crystal display drive. Apply positive voltage to V1L=V1R and V3L=V3R and negative voltage to V2L=V2R and V4L=V4R within the ΔV range. This range allows stable impedance on driver output (RON). Notice that ΔV depends on power supply voltage VCC-VEE.



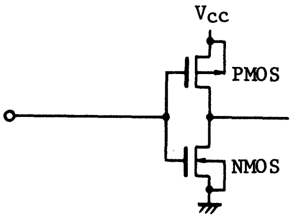
Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive



Correlation between Power Supply Voltage VCC-VEE and ΔV

Terminal Configuration

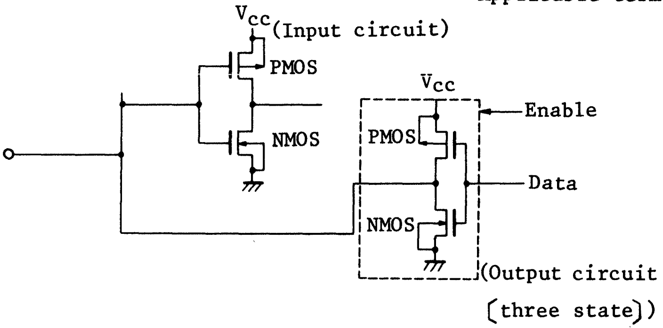
- Input Terminal



Applicable terminals :
M, FRM, CL, $\overline{\text{RST}}$, ϕ1, ϕ2, $\overline{\text{CS1}}$, $\overline{\text{CS2}}$, CS3,
E, R/W, D/I, ADC

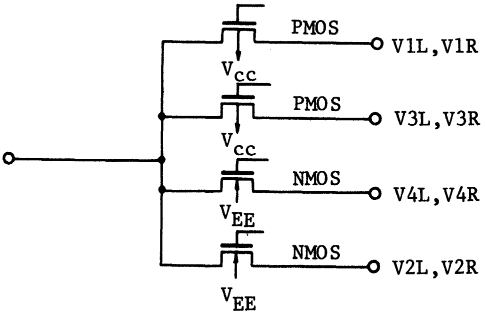
- Input/Output Terminal

Applicable terminals : DB0∿DB7



- Output Terminal

Applicable terminals:
Y1 ∿ Y64



● INTERFACE AC CHARACTERISTICS

(1) MPU Interface

(GND=0V, Vcc=4.5 ∿ 5.5V, Ta=-20∿+75°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
E cycle time	t_{CYC}	1000	-	-	ns	1, 2
E high level width	P_{WEH}	450	-	-	ns	1, 2
E low level width	P_{WEL}	450	-	-	ns	1, 2
E rise time	tr	-	-	25	ns	1, 2
E fall time	tf	-	-	25	ns	1, 2
Address setup time	t_{AS}	140	-	-	ns	1, 2
Address hold time	t_{AH}	10	-	-	ns	1, 2
Data setup time	t_{DSW}	200	-	-	ns	1
Data delay time	t_{DDR}	-	-	320	ns	2, 3
Data hold time (Write)	t_{DHW}	10	-	-	ns	1
Data hold time (Read)	t_{DHR}	20	-	-	ns	2

(Note 1)

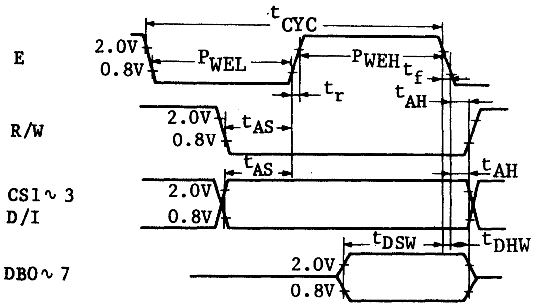


Fig. 1 CPU Write Timing

(Note 2)

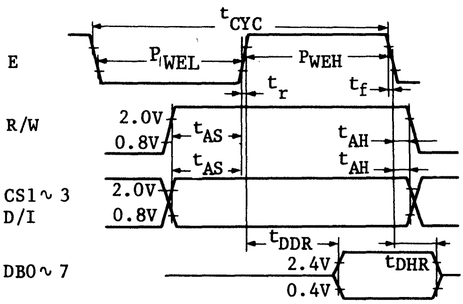
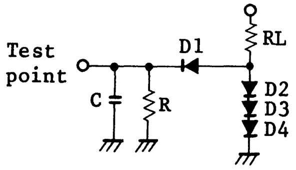


Fig. 2 CPU Read Timing

(Note 3) DB0 ∿ 7 : load circuit



RL=2.4KΩ

R =11KΩ

C =130pF (including jig capacity)

Diodes D1 to D4 are all 1S2074Ⓗ.

(2) Clock Timing

(GND=0V, Vcc=4.5 ∿ 5.5V, Ta=-20∿+75°C)

Item	Symbol	Test condition	Limit			Unit
			Min.	Typ.	Max.	
ϕ1, ϕ2 cycle time	tcyc	Fig. 3	2.5	-	20	μs
ϕ1 "Low" level width	$t_{WL\phi1}$	Fig. 3	625	-	-	ns
ϕ2 "Low" level width	$t_{WL\phi2}$	Fig. 3	625	-	-	ns
ϕ1 "High" level width	$t_{WH\phi1}$	Fig. 3	1875	-	-	ns
ϕ2 "High" level width	$t_{WH\phi2}$	Fig. 3	1875	-	-	ns
ϕ1-ϕ2 phase difference	t_{D12}	Fig. 3	625	-	-	ns
ϕ2-ϕ1 phase difference	t_{D21}	Fig. 3	625	-	-	ns
ϕ1, ϕ2 rise time	tr	Fig. 3	-	-	150	ns
ϕ1, ϕ2 fall time	tf	Fig. 3	-	-	150	ns

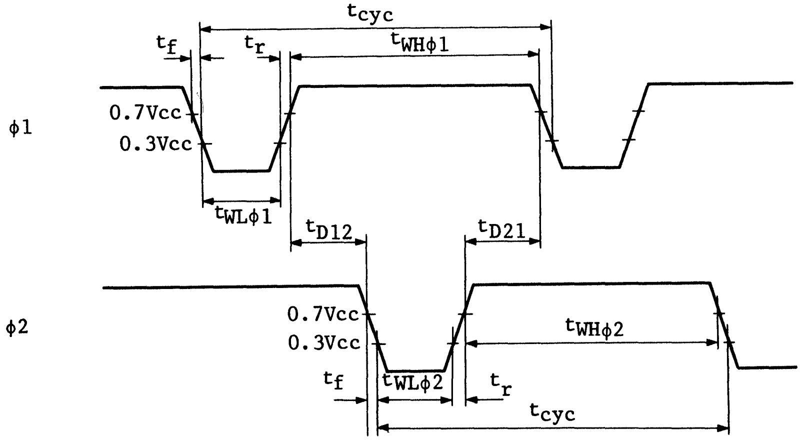


Fig. 3 External Clock Waveform

(3) Display Control Timing

(GND=0V, V_{CC}=4.5 ∿ 5.5V, Ta=-20∿+75°C)

Item	Symbol	Test condition	Limit			Unit
			Min.	Typ.	Max.	
FRM delay time	t_{DFRM}	Fig. 4	-2	-	+2	µs
M delay time	t_{DM}	Fig. 4	-2	-	+2	µs
CL "Low" level width	t_{WLCL}	Fig. 4	35	-	-	µs
CL "High" level width	t_{WHCL}	Fig. 4	35	-	-	µs

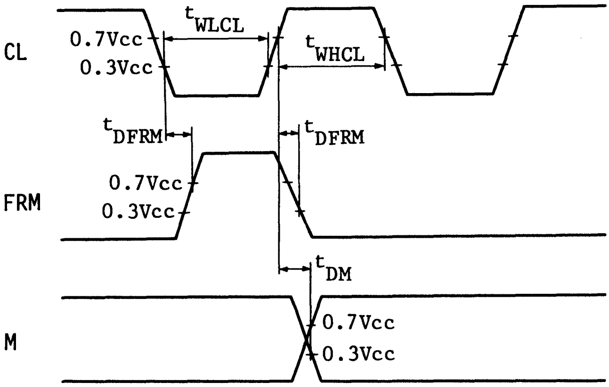
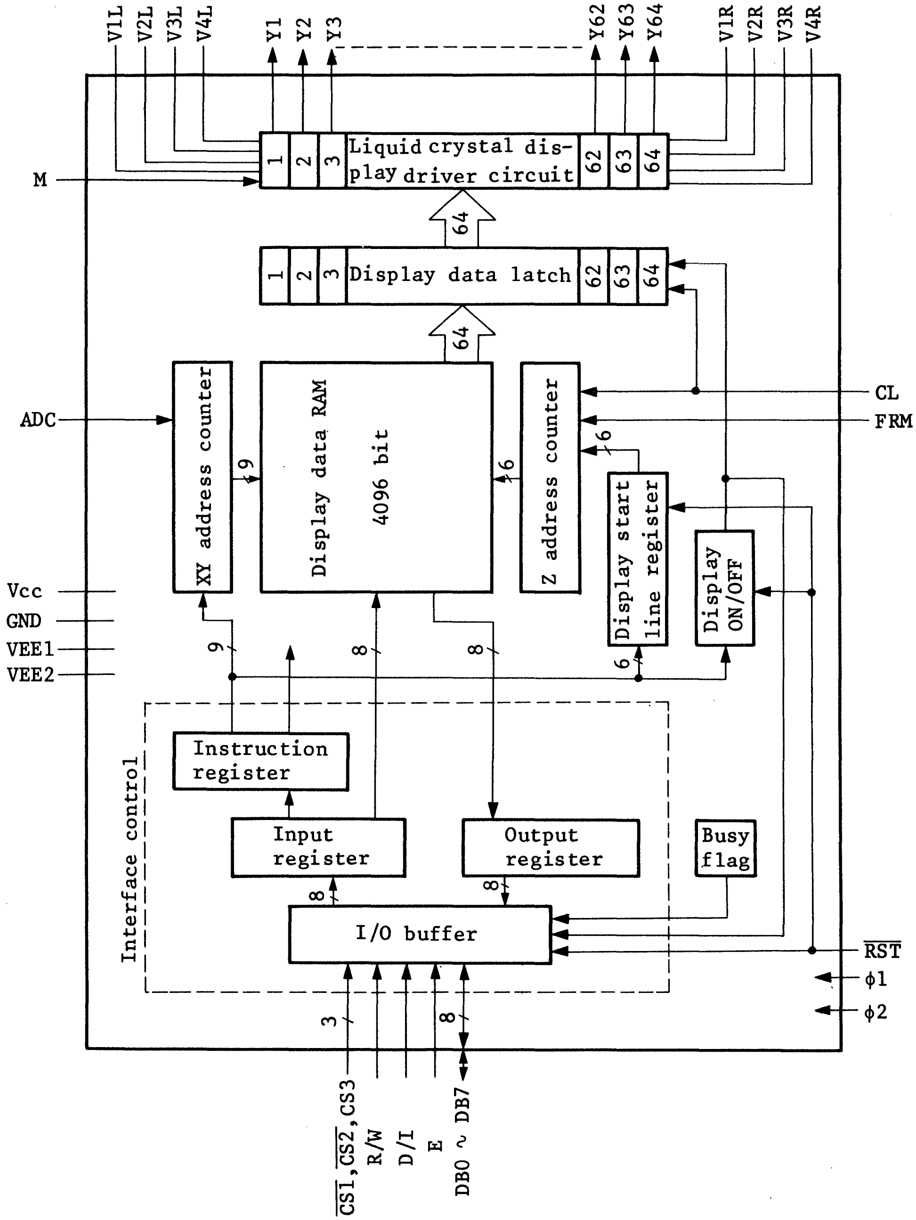


Fig. 4 Display Control Signal Waveform

■ BLOCK DIAGRAM



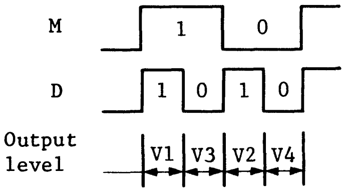
TERMINAL FUNCTIONS

<table>
<tr><th>Terminal name</th><th>Number of terminals</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>V_{CC}
GND</td><td>2</td><td></td><td>Power supply</td><td>Power supply for internal logic.
Recommended voltage is
GND = 0V
VCC = 5V ± 10%</td></tr>
<tr><td>V_{EE} 1
V_{EE} 2</td><td>2</td><td></td><td>Power supply</td><td>Power supply for liquid crystal display drive circuit.
Recommended power supply voltage is Vcc-VEE=8 ∿ 15.5V. Connect the same power supply to V_{EE1} and V_{EE2}.
V_{EE1} and V_{EE2} are not connected each other in the LSI.</td></tr>
<tr><td>V1L, V1R
V2L, V2R
V3L, V3R
V4L, V4R</td><td>8</td><td></td><td>Power supply</td><td>Power supply for liquid crystal display drive.
Apply the voltage specified depending on liquid crystals within the limit of V_{EE} through V_{CC}.
V1L(V1R), V2L(V2R)---Selection level
V3L(V3R), V4L(V4R)---Non-selection level
Power supplies connected with V1L and V1R (V2L & V2R, V3L & V3R, V4L & V4R) should have the same voltages.</td></tr>
<tr><td>$\overline{CS1}$
$\overline{CS2}$
CS3</td><td>3</td><td>I</td><td>MPU</td><td>Chip selection.
Data can be input or output when the terminals are in the next conditions.
<table>
<tr><td>Terminal name</td><td>$\overline{CS1}$</td><td>$\overline{CS2}$</td><td>$\overline{CS3}$</td></tr>
<tr><td>Condition</td><td>'L'</td><td>'L'</td><td>'H'</td></tr>
</table></td></tr>
<tr><td>E</td><td>1</td><td>I</td><td>MPU</td><td>Enable
At write(R/W=L) : Data of DB0 to DB7 is latched at the fall of E.
At read(R/W=H) : Data appears at DB0 to DB7 while E is in "High" level.</td></tr>
</table>

Terminal name	Number of terminals	I/O	Connected to	Functions
R/W	1	I	MPU	Read/Write R/W=H : Data appears at DB0 to DB7 and can be read by the CPU When E=H, $\overline{CS1}$, $\overline{CS2}$=L and CS3=H. R/W=L : DB0 to DB7 can accept at fall of E when $\overline{CS1}$, $\overline{CS2}$=L and CS3=H.
D/I	1	I	MPU	Data/Instruction D/I=H : Indicates that the data of DB0 to DB7 is display data. D/I=L : Indicates that the data of DB0 to DB7 is display control data.

ADC	1	I	V_{CC}/GND	Address control signal determine the relation between Y address of display RAM and terminals from which the data is output.
				ADC=H : Y1-$0, Y64-$63
				ADC=L : Y64-$0, Y1-$63

DB0∿DB7	8	I/O	MPU	Data bus, three-state I/O common terminal
M	1	I	HD61203	Switch signal to convert liquid crystal drive waveform into AC.
FRM	1	I	HD61203	Display synchronous signal (frame signal). This signal presets the 6-bit display line counter and synchronizes a common signal with the frame timing when the FRM signal becomes high.
CL	1	I	HD61203	Synchronous signal to latch display data. The CL signal indicates to count up the display output adress counter and latch the display data at rising.

Terminal name	Number of terminals	I/O	Connected to	Functions
φ1,φ2	2	I	HD61203	2-phase clock signal for internal operation. The φ1 and φ2 clocks are used to perform the operations (I/O of display data and execution of instructions) other than display.
Y1∿Y64	64	O	Liquid crystal display	Liquid crystal display column (segment) drive output. These pins outputs light ON level when "1" is in the display RAM, and light OFF level with "0" in it. Relation among output level, M and display data (D) is as follows.  M 1 0 D 1 0 1 0 Output level V1 V3 V2 V4
$\overline{\text{RST}}$	1	I	CPU or external CR	The following registers can be initialized by setting the $\overline{\text{RST}}$ signal to "Low" level. (1) ON/OFF register 0 set (display OFF) (2) Display start line register 0 line set (displays from 0 line) After releasing reset, this condition can be changed only by the instruction.
NC	3		Open	Unused terminals. Don't connect any lines to these terminals.

(Note) "1" corresponds to "High level" in positive logic.

■ FUNCTION OF EACH BLOCK

● Interface Control

(1) I/O buffer

Data is transferred through 8 data buses (DB0 ∿ DB7).

DB7 .... MSB (Most Significant Bit)
DB0 .... LSB (Least Significant Bit)

Data can neither be input nor output unless $\overline{CS1}$ to CS3 are in the active mode. Therefore, when $\overline{CS1}$ to CS3 are not in active mode it is useless to switch the signals of input terminals except $\overline{RST}$ and ADC, namely, the internal state is maintained and no instruction excute. Besides, pay attention to $\overline{RST}$ and ADC which operate irrespectively by $\overline{CS1}$ to CS3.

(2) Register

Both input register and output register are provided to interface to MPU of which the speed is different from that of internal operation. The selection of these registers depend on the combination of R/W and D/I signals.

Table 1. Register Selection

D/I	R/W	Operation
1	1	Reads data out of output register as internal operation (display data RAM → output register)
1	0	Writes data into input register as internal operation (input register → display data RAM)
0	1	Busy check. Read of status data.
0	0	Instruction

① Input register

Input register is used to store data temporarily before writing it into display data RAM.
The data from MPU is written into input register, then into display data RAM automatically by internal operation.
When $\overline{CS1}$ to CS3 are in the active mode and D/I and R/W select the input register as shown in Table 1, data is latched at the fall of E signal.

② Output register

Output register is used to store data temporarily which is read from display data RAM. To read out the data from output register, $\overline{\text{CS1}}$ to CS3 should be in the active mode and both D/I and R/W should be 1. With READ instruction, data stored in the output register is output while E is "H" level. Then, at the fall of E, the display data at the indicated address is latched into the output register and the address is increased by 1.
The contents in the output register is rewritten with READ instruction, while is held with address set instruction, etc.

Therefore, the data of the specified address can not be output with READ instruction soon after the address is set, but can be output at the second read of data. That is to say, one dummy read is necessary. Fig. 5 shows the CPU read timing.

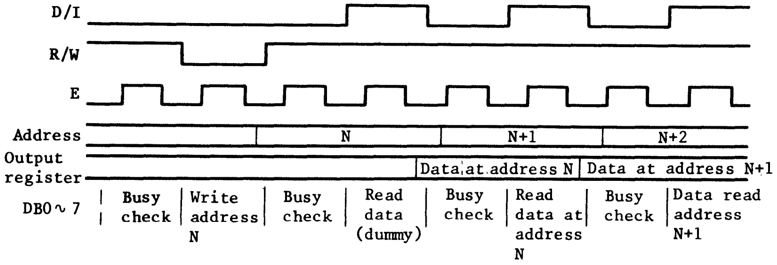
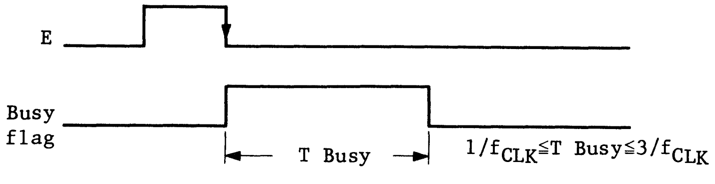


Fig. 5 CPU Read Timing

● Busy Flag

"1" of busy flag indicates that HD61202 is on the move and any instructions except Status Read instruction can not be accepted. The value of the busy flag is read out on DB7 by the Status Read instruction. Make sure that the busy flag is reset ("0") before the issue of instruction.



f_{CLK} is $\phi 1$, $\phi 2$ frequency

- Display ON/OFF Flip Flop

Display ON/OFF flip flop selects one of two states, ON state and OFF state of segments Y1 to Y64. In ON state, the display data corresponding to that in RAM is output to the segments. On the other hand, the display data at all segments disappear in OFF state independent of the data in RAM. It is controlled by display ON/OFF instruction '0' of $\overline{RST}$ signal sets the segments in OFF state. The status of the flip flop is output to DB5 by Status Read instruction. Display ON/OFF instruction does not influence data in RAM. To control display data latch by this flip flop, CL signal (display synchronous signal) should be input correctly.

- Display Start Line Register

The register specifies a line in RAM which corresponds to the top line of LCD panel, when displaying contents in display data RAM on the LCD panel. It is used for scrolling of the screen.

6-bit display start line information is written into this register by display start line set instruction, with 'H' level of FRM signal instructing to start the display, the information in this register is transferred to Z address counter which controls the display address, and the Z address counter is preset.

- X, Y Address Counter

This is a 9-bit counter which designates addresses of internal display data RAM. X address counter of upper 3 bits and Y address counter of lower 6 bits should be set each address by respective instruction.

(1) X address counter

Ordinary register with no count functions. An address is set in by instructions.

(2) Y address counter

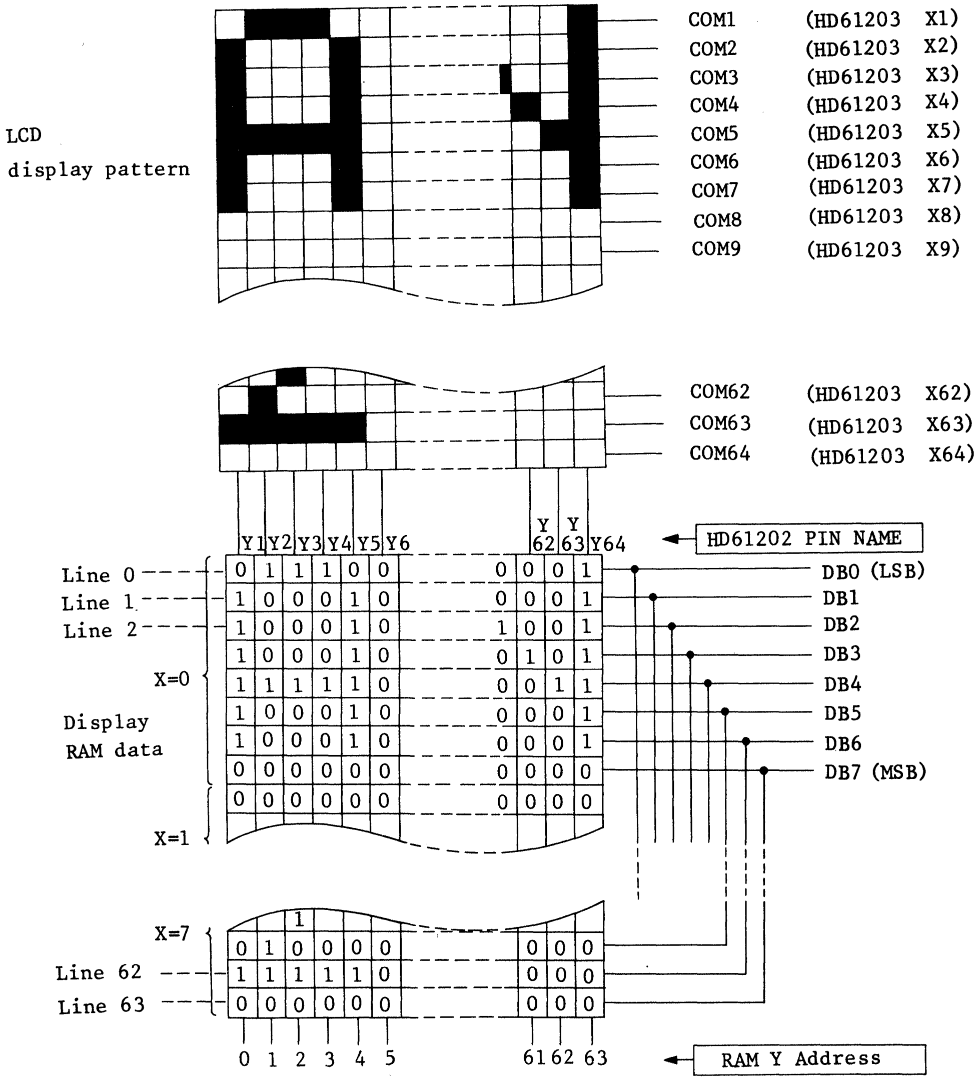
An address is set in by instruction and it is increased by 1 automatically by R/W operations of display data. The Y address counter loops the values of 0 to 63 to count.

- Display Data RAM

Dot data for display is stored in this RAM. 1-bit data of this RAM corresponds to light ON (data=1) and light OFF (data=0) of 1 dot in the display panel. The correspondence between Y addresses of RAM and segment PINs can be reversed by ADC signal.

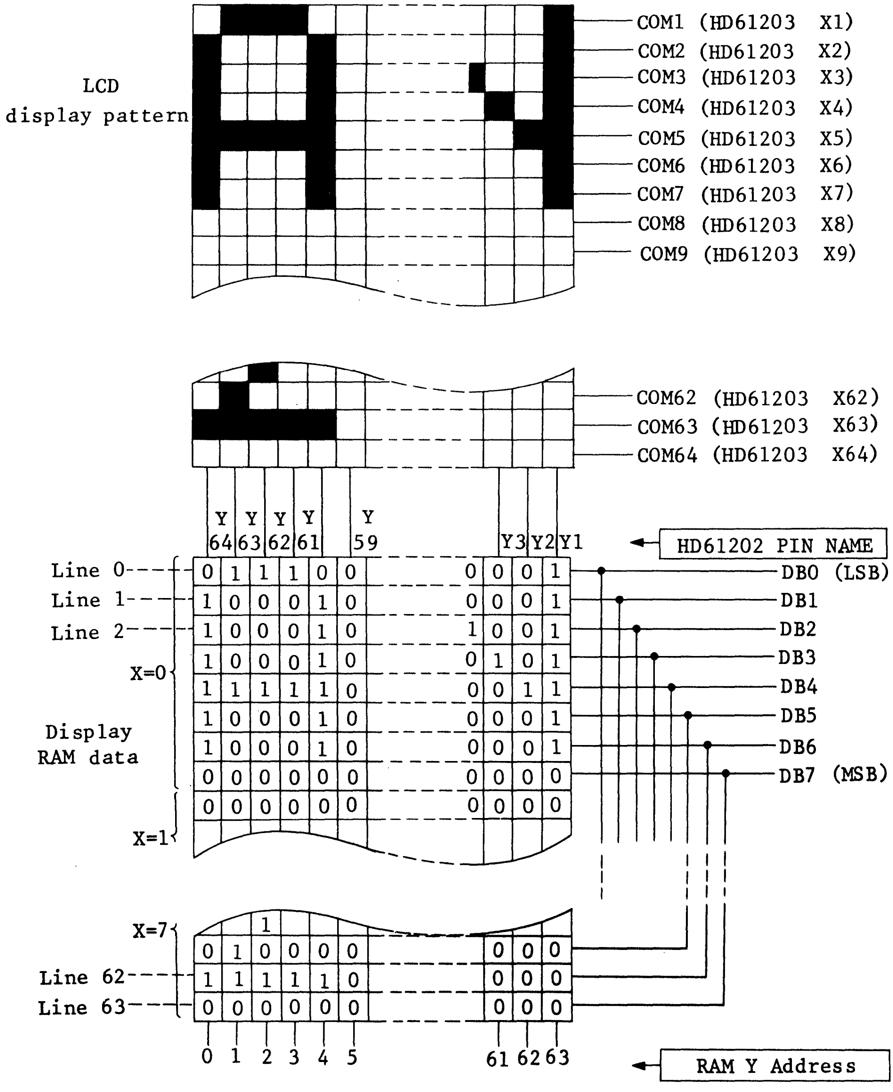
As ADC signal controls Y address counter, a reverse of the signal during the operation causes malfunction and destruction of the contents of register and data of RAM. Therefore, never fail to connect ADC pin to V_{CC} or GND when using.

Fig. 6 shows the relations between Y address of RAM and segment pins in the cases of ADC=1 and ADC=0. (display start line=0, 1/64 duty).



(a) ADC="1" (Connected to Vcc)

Fig. 6 Relation between RAM Data and Display



(b) ADC="0" (Connected to GND)

Fig. 6 Relation Between RAM Data and Display

Z Address Counter

The Z address counter generates addresses for outputting the display data synchronized with the common signal. This counter consists of 6-bit and counts up at the fall of CL signal. With "H" level of FRM, the contents of the display start line register is preset at the Z counter.

Display data Latch

The display data latch stores the display data temporarily which is output from display data RAM to liquid crystal driving circuit.
Data is latched at the rise of CL signal. Display ON/OFF instruction controls the data in this latch and does not influence data in display data RAM.

Liquid Crystal Display Driver Circuit

The combination of latched display data and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3 and V4 to be output.

Reset

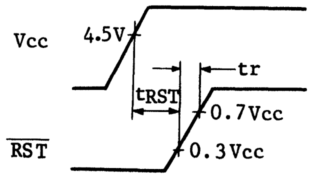
The system can be initialized by setting $\overline{\text{RST}}$ terminal at "Low" level when turning power ON.

1) Display-OFF
2) Set display start line register 0 line.

While $\overline{\text{RST}}$ is in Low level, any instruction except Status Read cannot be accepted. Therefore, Carry out other instructions after making sure that DB4=0 (clear RESET) and DB7=0 (Ready) by Status Read instruction.
The conditions of Power Supply at initial power up are as follows.

Item	Symbol	Min.	Typ.	Max.	Unit
Reset time	t_{RST}	1.0	-	_	μs
Rise time	t_r	-	-	200	ns

Do not fail to set the system again because RESET during operation may destroy the data in all the register except ON/OFF register and in RAM.



Display Control Instructions

Outline

Table 2 shows the instructions. Read/Write (R/W) signal, Data/Instruction (D/I) signal and Data bus signal (DB0 to DB7) are also called instructions because the internal operation depends on the signals from MPU.
These explanations are detailed from the following page. Generally, there are following three kinds of instructions.

(1) Instruction to give addresses in the internal RAM
(2) Instruction to transfer data from/to the internal RAM
(3) Other instructions

In general use, the instruction (2) are used most frequently. But, since Y address of the internal RAM is increased by 1 automatically after writing (reading) data, the program can be lessened. During the execution of an instruction, the system cannot accept other instructions than Status Read instruction. Send instructions from MPU after making sure if the busy flag is "0", which is the proof an instruction is not being excuted.

Table 2. Instructions

Instructions	Code										Functions	
	R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1 Display ON/OFF	0	0	0	0	1	1	1	1	1	1/0	Controls the ON/OFF of display. RAM data and internal status are not affected. 1:ON, 0:OFF.	
2 Display start line	0	0	1	1	display start line (0~63)						Specifies a RAM line displayed at the top of the screen.	
3 Set page (X address)	0	0	1	0	1	1	1	Page (0~7)			Sets the page (X address) of RAM at the page (X address) register.	
4 Set Address	0	0	0	1	Y address (0~63)						Sets the Y address at the Y address counter	
5 Status Read	1	0	Busy	0	ON/OFF	RESET	0	0	0	0	Reads the status. RESET 1: reset 0:normal ON/OFF 1: display OFF 0:display ON Busy 1: on the internal operation 0: Ready	
6 Write deisplay data	0	1	Write Data								Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM.	Has access to the address of the display RAM specified in advance. After the access, Y address is increased by 1.
7 Read display data	1	1	Read Data								Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.	

Note 1) Busy time varies with the frequency (f_{CLK}) of $\phi 1$, and $\phi 2$.

$(1/f_{CLK} \leqq T_{BUSY} \leqq 3/f_{CLK})$

- Detailed Explanation

(1) Display ON/OFF

	R/W	D/I	DB7							DB0
Code	0	0	0	0	1	1	1	1	1	D

← high-order-bit low-order-bit →

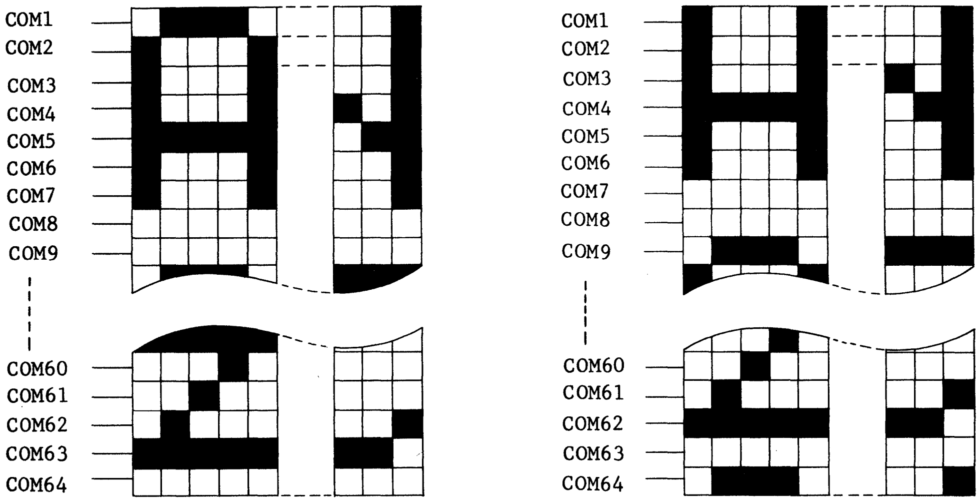
The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen width D=0, it remains in the display data RAM. Therefore, you can make it appear by changing D=0 into D=1.

(2) Display start line

	R/W	D/I	DB7							DB0
Code	0	0	1	1	A	A	A	A	A	A

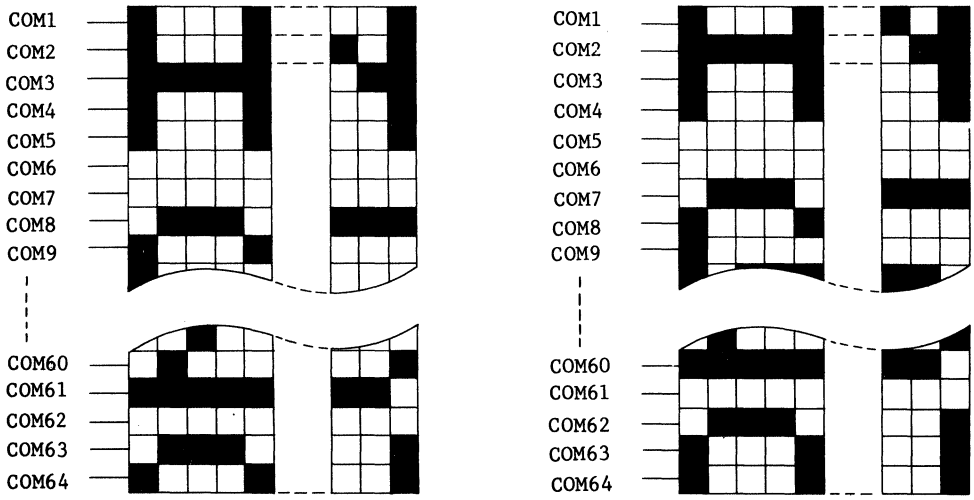
← high-order-bit low-order-bit →

Z address AAAAAA (binary) of the display data RAM is set at the display start line register and displayed at the top of the screen. Fig. 7 are the examples of display (1/64 duty) when the start line=0 ∿ 3. When the display duty is 1/64 or more (ex. 1/32, 1/24 etc.), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.



Start line=0

Start line=1



Start line=2

Start line=3

Fig. 7 Relation Between Start Line and Display

(3) Set page (X address)

	R/W	D/I	DB7							DB0
Code	0	0	1	0	1	1	1	A	A	A

← high-order-bit low-order-bit →

X address AAA (binary) of the display data RAM is set at the X address register. After that, writing or reading to or from MPU is executed in this specified page until the next page is set.

(4) Set Y address

	R/W	D/I	DB7							DB0
Code	0	0	0	1	A	A	A	A	A	A

← high-order-bit low-order-bit →

Y address AAAAAA (binary) of the display data RAM is set at the Y address counter. After that, Y address counter is increased by 1 every time the data is written or read to or from MPU.

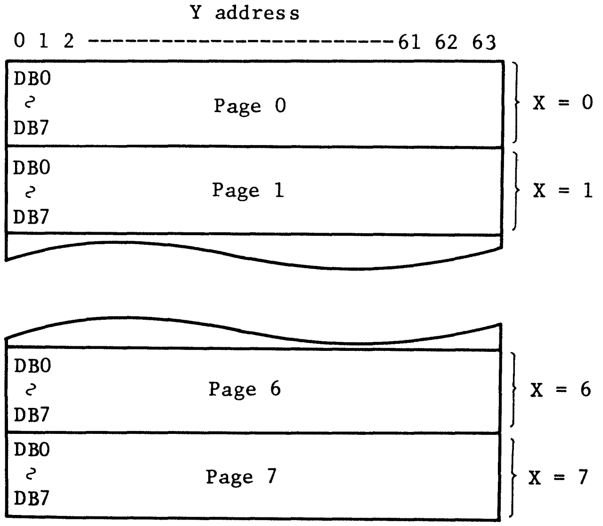


Fig. 8 Address Configuration of Display Data RAM

(5) Status Read

	R/W	D/I	DB7							DB0
Code	1	0	BUSY	0	ON/ OFF	RESET	0	0	0	0

← high-order-bit low-order-bit →

BUSY: When BUSY is 1, the LSI is in internal operation. No instructions are accepted while BUSY is 1, so you should make sure that BUSY is 0 before writing the next instruction.

ON/OFF: This bit shows the liquid crystal display conditions - ON condition or OFF condition.
When ON/OFF is 1, the display is in OFF condition.
When ON/OFF is 0, the display is in ON condition.

RESET: RESET=1 shows that the system is being initialized. In this condition, any instructions except Status Read instruction cannot be accepted.
RESET=0 shows that initializing has finished and the system is in the usual operation.

(6) Write Display Data

	R/W	D/I	DB7							DB0
Code	0	1	D	D	D	D	D	D	D	D

← high-order-bit low-order-bit →

Writes 8-bit data DDDDDDDD (binary) into the display data RAM. Then Y address is increased by 1 automatically.

(7) Read Display Data

	R/W	D/I	DB7							DB0
Code	1	1	D	D	D	D	D	D	D	D

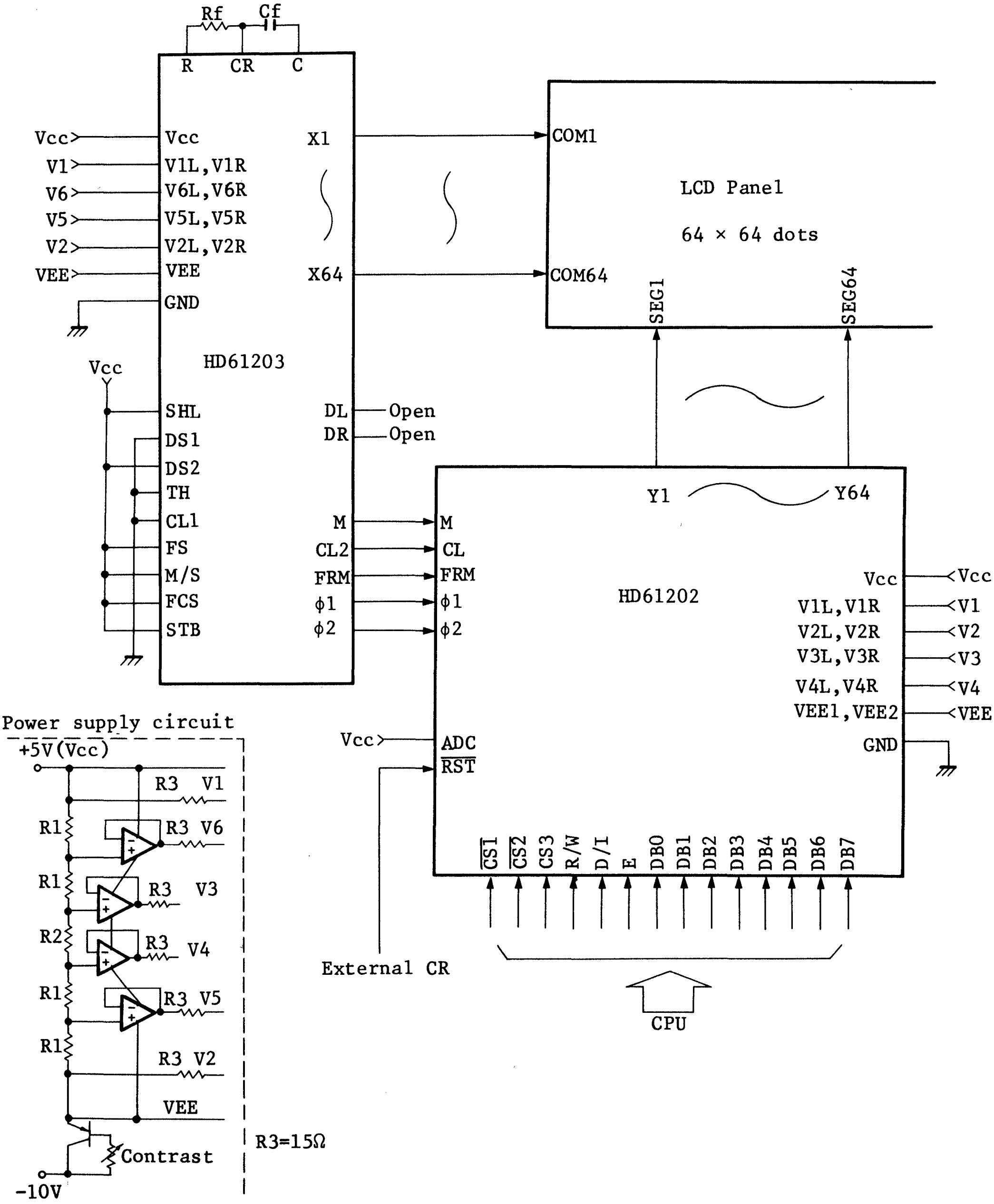
← high-order-bit low-order-bit →

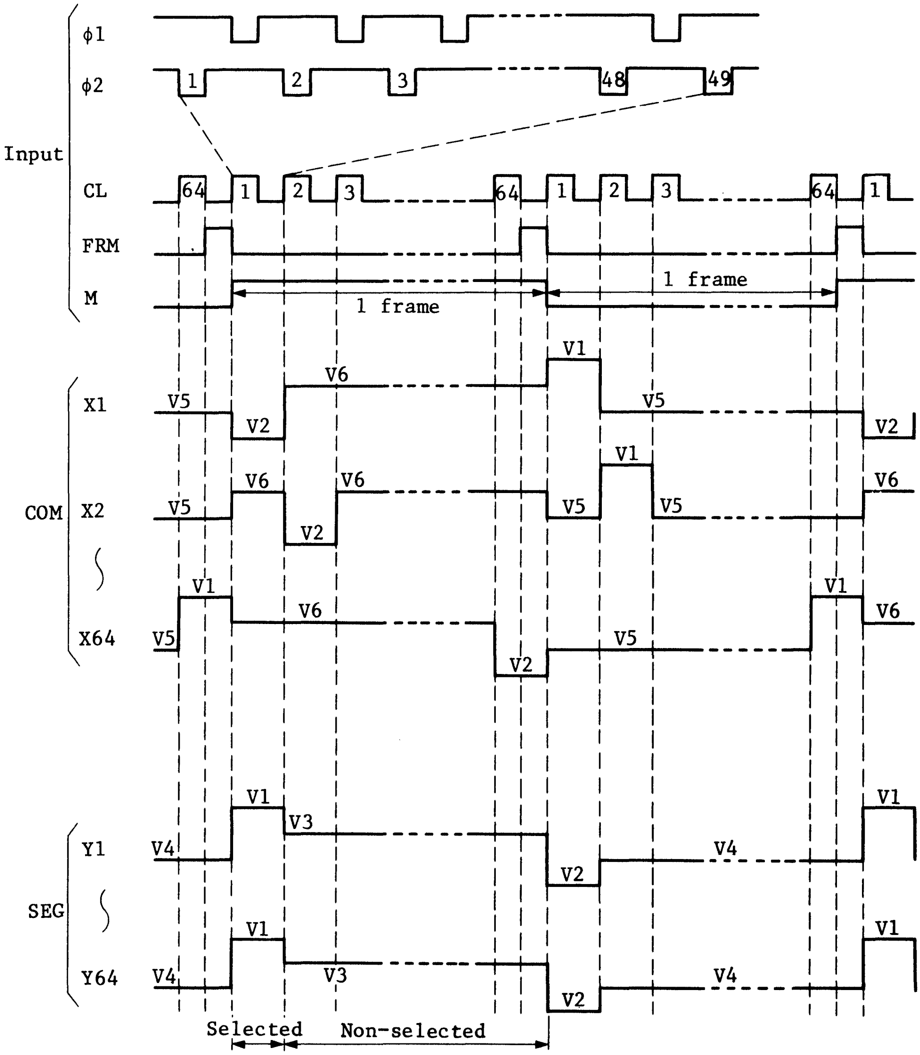
Read out 8-bit data DDDDDDDD (binary) from the display data RAM. Then Y address is increased by 1 automatically.

One dummy read is necessary soon after the address setting. For details, refer to the explanation of output register in "FUNCTION OF EACH BLOCK".

The Usage of HD61202

- Interface with HD61203 (1/64 duty)



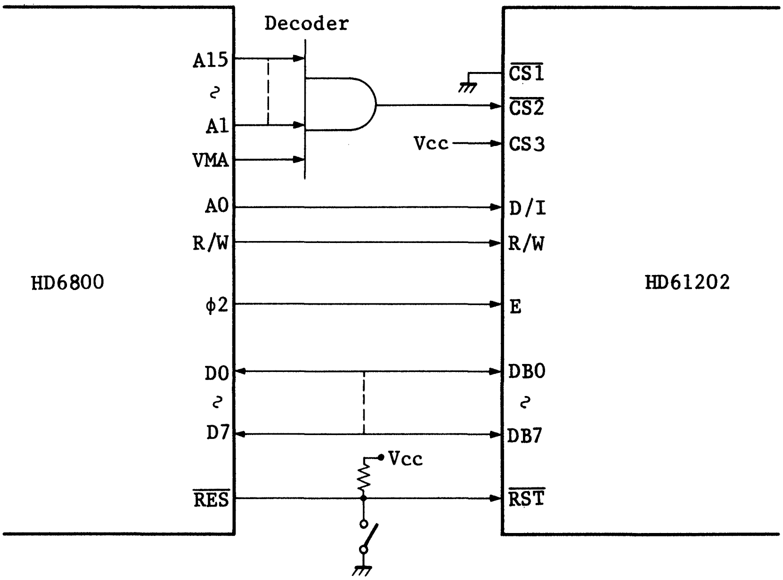


The wave forms of Y1 to Y64 outputs vary with the display data. In this example, the top line of the panel lights up and other dots do not.

Fig. 9 LCD Driver Timing Chart (1/64 duty)

Interface with CPU

a) Example of connection with HD6800



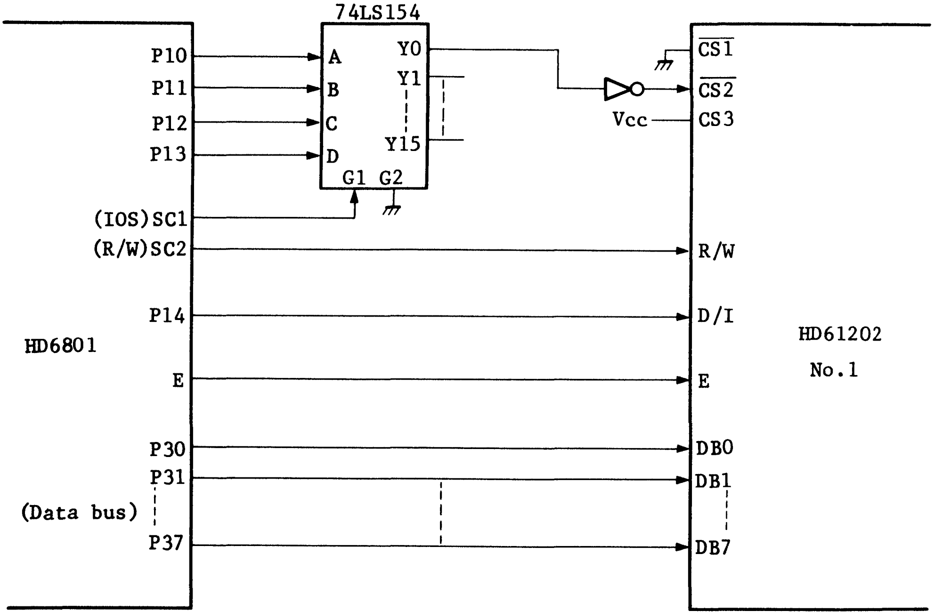
The example of connection with HD6800 series

In this decoder, addresses of HD61202 in the address area of HD6800 are:

Read/Write of the display data	$FFFF
Write of display instruction	$FFFE
Read out of status	$FFFE

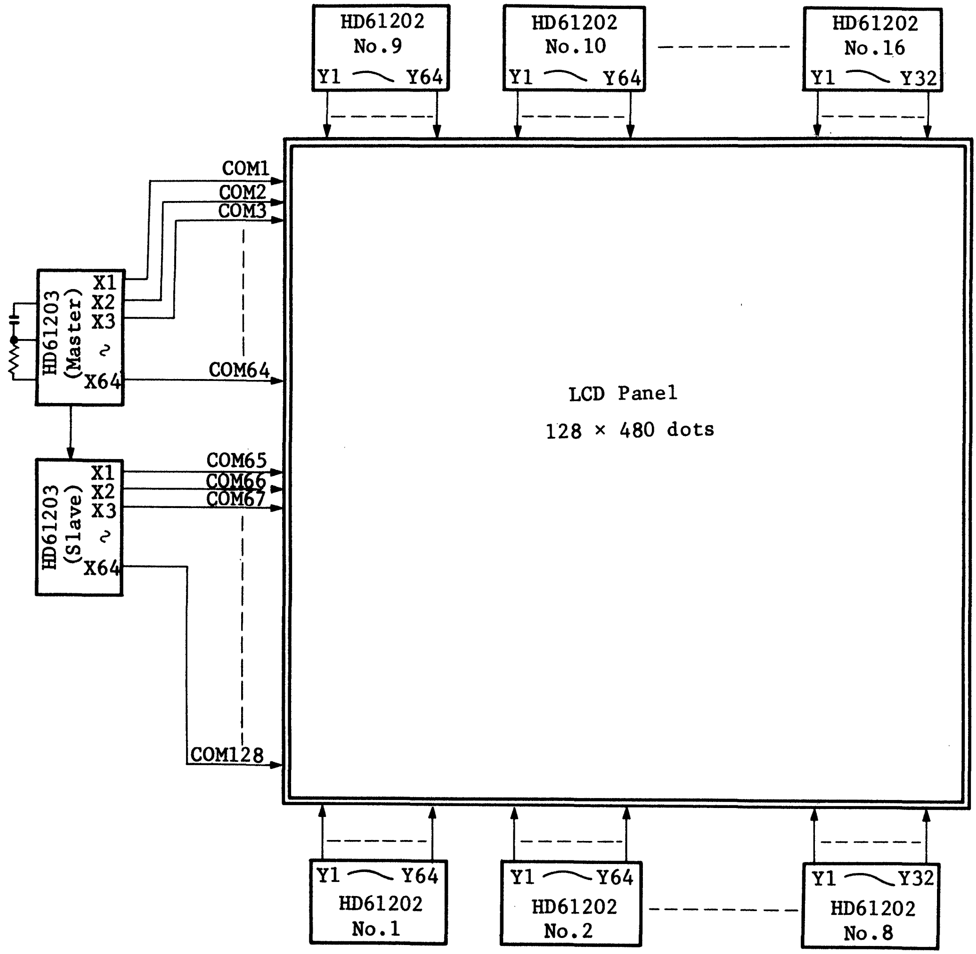
Therefore, you can control HD61202 by reading/writing the data at these addresses.

b) Example of connection with HD6801



- Set HD6801 in Mode 5. P10 to P14 are used as the output port and P30 to P37 as the data bus.
- 74LS154 is 4 to 16 decoder and generate chip select signal to make specified HD61202 active after decoding 4 bits of P10 to P13.
- Therefore, after making the operation possible by P10 to P13 and specifying D/I signal by P14, read/write from/to. the external memory area ($0100 to $01FE) to control HD61202. In this case, IOS signal is output from SC1 and R/W signal from SC2.
- For details of HD6800 and HD6801, refer to the each manual.

- Example of Application



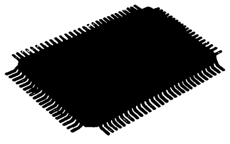
Note) In this example, two HD61203 's output the equivalent waveforms. So, stand-alone operation is possible. In this case, connect COM1 and COM65 to X1, COM2 and COM66 to X2, ..., and COM64 and COM128 to X64. However, for the large screen display, you had better drive in 2 rows as this example to guarantee the display quality.

HD61203
(Dot Matrix Liquid Crystal Graphic Display Common Driver)

DESCRIPTION

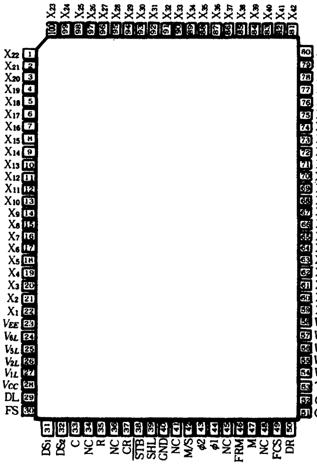
The HD61203 is a common signal driver for dot matrix liquid crystal graphic display systems. It generates the timing signals (switch signal to convert LCD waveform to AC, frame synchronous signal) and supplies them to the column driver to control display. It provides 64 driver output lines and the impedance is low enough to drive a large screen.

As the HD61203 is produced in a CMOS process, it is fit for use in portable battery drive equipments utilizing the liquid crystal display's low power consumption. The user can easily construct a dot matrix liquid crystal graphic display system by combining the HD61203 and the column (segment) driver HD61202.



(FP-100)

PIN ARRANGEMENT



(Top View)

FEATURES

- Dot matrix liquid crystal graphic display common driver with low impedance.
- Low impedance -- 1.5kΩ max.
- Internal liquid crystal display driver circuit -- 64 circuits
- Internal dynamic display timing generator circuit
- Display duty
  When used with the column driver HD61202
    1/48, 1/64, 1/96, 1/128
  When used with the column driver HD61200
    Selectable out of 1/32 to 1/128

- Low power dissipation
  - during display 5mW
- Power supplies : V_{CC} 5V ± 10%
- Power supply voltage for liquid crystal display drive .... 8V ∿ 17V
- CMOS process
- 100-pin flat plastic package (FP-100)

Absolute Maximum Ratings

Item	Symbol	Limit	Unit	Note
Power Supply Voltage (1)	V_{CC}	-0.3 ∿ +7.0	V	2
Power Supply Voltage (2)	V_{EE}	V_{CC}-19.0 ∿ V_{CC} +0.3	V	5
Terminal Voltage (1)	V_{T1}	-0.3 ∿ V_{CC} +0.3	V	2, 3
Terminal Voltage (2)	V_{T2}	V_{EE}-0.3 ∿ V_{CC} +0.3	V	4, 5
Operating Temperature	Topr	-20 ∿ +75	°C	
Storage Temperature	Tstg	-55 ∿ +125	°C	

Note 1) If LSI's are used beyond absolute maximum ratings, they may be permanently destroyed. We strongly recommend you to use the LSI within electrical characteristic limits for normal operation, because use beyond these conditions will cause malfunction and poor reliability.

Note 2) Based on GND=0V

Note 3) Applies to input terminals (except V1L, V1R, V2L, V2R, V5L, V5R, V6L and V6R) and I/O terminals at high impedance.

Note 4) Applies to V1L, V1R, V2L, V2R, V5L, V5R, V6L and V6R.

Note 5) Apply the same value of voltages to V1L and V1R, V2L and V2R, V5L and V_{5R}, V6L and V6R, V_{EE} (23 pin) and V_{EE} (58 pin) respectively.
Maintain $V_{CC} \geqq V1L=V1R \geqq V6L=V6R \geqq V5L=V5R \geqq V2L=V2R \geqq V_{EE}$

ELECTRICAL CHARACTERISTICS

- DC Characteristics (V_{CC}=5V ± 10%, GND=0V, VCC-VEE=8.0∿17.0V
  Ta= -20 ∿ +75°C)

Test Item	Symbol	Test conditions	Specifications			Unit	Note
			Min	Typ.	Max		
Input "High" voltage	V_{IH}		0.7×Vcc	-	V_{CC}	V	1
Input "Low" voltage	V_{IL}		GND	-	0.3×Vcc	V	1
Output "High" voltage	V_{OH}	I_{OH}=-0.4mA	V_{CC}-0.4	-	-	V	2
Output "Low" voltage	V_{OL}	I_{OL}=0.4mA	-	-	0.4	V	2
Vi-Xj ON resistance	R_{ON}	V_{CC}-V_{EE}=17V Load current ±150μA	-	-	1.5	kΩ	13
Input Leakage Current	I_{IL1}	Vin=0∿V_{CC}	-1.0	-	1.0	μA	3
Input Leakage Current	I_{IL2}	Vin=V_{EE}∿VCC	-2.0	-	2.0	μA	4
Operating Frequency	f_{opr1}	In master mode External clock operation	50	-	600	kHz	5
Operating Frequency	f_{opr2}	In slave mode Shift register	0.5	-	1500	kHz	6
Oscillation Frequency	fosc	Cf=20pF±5% Rf=47KΩ±2%	315	450	585	kHz	7,12
Dissipation Current (1)	I_{GG1}	In master mode 1/128 duty Cf=20pF Rf=47kΩ	-	-	1.0	mA	8,9
Dissipation Current (2)	I_{GG2}	In slave mode 1/128 duty	-	-	200	μA	8,10
Dissipation Current	I_{EE}	In master mode 1/128 duty	-	-	100	μA	8,11

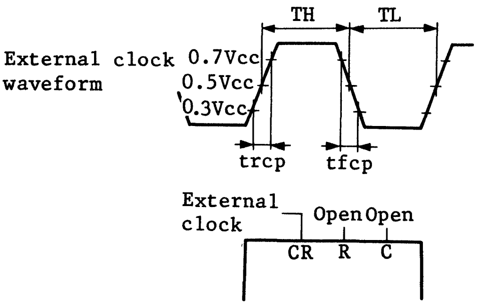
Note 1) Applies to input terminals FS, DS1, DS2, CR, SHL, M/S and FCS and I/O terminals DL, M, DR and CL2 in the input status.

Note 2) Applies to output terminals, ϕ1, ϕ2 and FRM and I/O common terminals DL, M, DR and CL2 in the output status.

Note 3) Applies to input terminals FS, DS1, DS2, CR, $\overline{STB}$, SHL, M/S, FCS, CL1 and TH, I/O terminals DL, M, DR and CL2 in the input status and NC terminals.

Note 4) Applies to V1L, V1R, V2L, V2R, V5L, V5R, V6L and V6R. Don't connect any lines to X1 to X64.

Note 5) External clock is as follows.

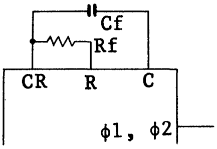


$$\text{Duty} = \frac{TH}{TH+TL} \times 100\%$$

	Min	Typ	Max	Unit
Duty	45	50	55	%
trcp	-	-	50	ns
tfcp	-	-	50	ns

Note 6) Applies to the shift register in the slave mode. For details, refer to AC Characteristics.

Note 7) Connect oscillation resistor (Rf) and oscillation capacitance (Cf) as shown in this figure. Oscillation frequency (f_{OSC}) is twice as much as the frequency ($f\phi$) at $\phi 1$ or $\phi 2$.



Cf=20pF
Rf=47kΩ

$fosc = 2 \times f\phi$

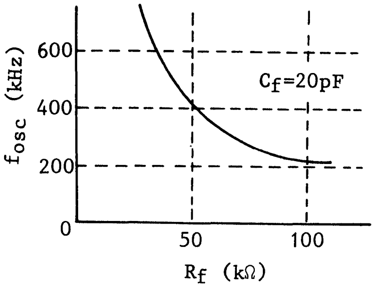
Note 8) No lines are connected to output terminals and current flowing through the input circuit is excluded. This value is specified at $V_{IH}=V_{CC}$ and V_{IL}=GND.

Note 9) This value is specified about current flowing through GND in the following conditions: Internal oscillation circuit is used. Each terminal of DS1, DS2, FS, SHL, M/S, $\overline{\text{STB}}$ and FCS is connected to V_{CC} and each of CL1 and TH to GND. Oscillator is set as described in Note 7.

Note 10) This value is specified about current flowing through GND under the following conditions: Each terminals of DS1, DS2, FS, SHL, $\overline{\text{STB}}$, FCS and CR is connected to V_{CC}, CL1, TH and M/S to GND and the terminals CL2, M and DL are respectively connected to terminals CL2, M and DL of the HD61203 under the condition described in Note 9.

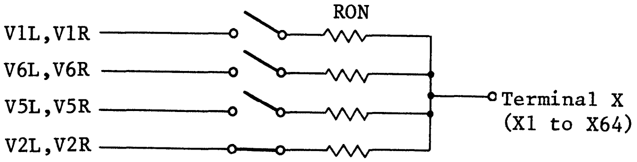
Note 11) This value is specified about current flowing through V_{EE} under the condition described in Note 9. Don't connect any lines to terminal V.

Note 12) This figure shows a typical relation among oscillation frequency, Rf and Cf. Oscillation frequency may vary with the mounting condition.

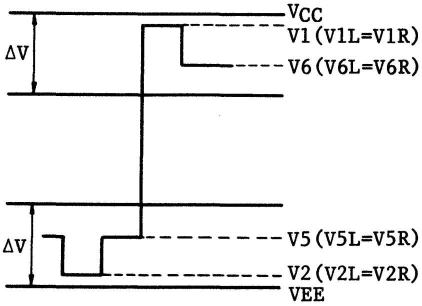


Note 13) Resistance between terminal X and terminal V (one of V1L, V1R, V2L, V2R, V5L, V5R, V6L and V6R) when load current flows through one of the terminals X1 to X64. This value is specified under the following condition.

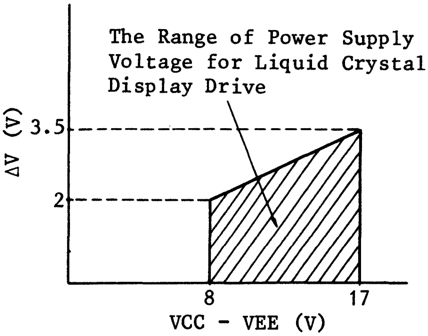
VCC - VEE = 17V
V1L=V1R, V6L=V6R = VCC-1/7(VCC-VEE)
V2L=V2R, V5L=V5R = VEE+1/7(VCC-VEE)



Here is a description of the range of power supply voltage for liquid crystal display drive. Apply positive voltage to V1L=V1R and V6L=V6R and negative voltage to V2L=V2R and V5L=V5R within the ΔV range. This range allows stable impedance on driver output (RON). Notice that ΔV depends on power supply voltage VCC-VEE.



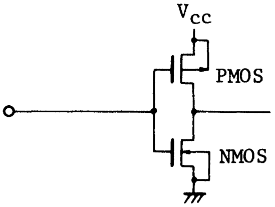
Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive



Correlation between Power Supply Voltage VCC-VEE and ΔV

Terminal Configuration

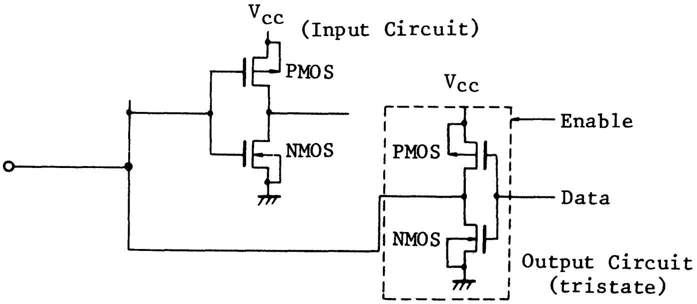
- Input Terminal



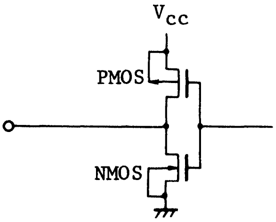
Applicable terminals :
CR, M/S, SHL, FCS, DS1, DS2, FS

- I/O Terminal

Applicable terminal : DL, DR, CL2, M

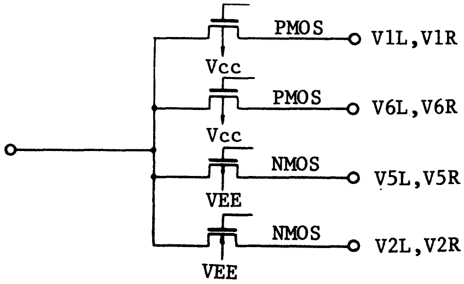


- Output Terminal



Applicable terminal : $\phi 1$, $\phi 2$, FRM

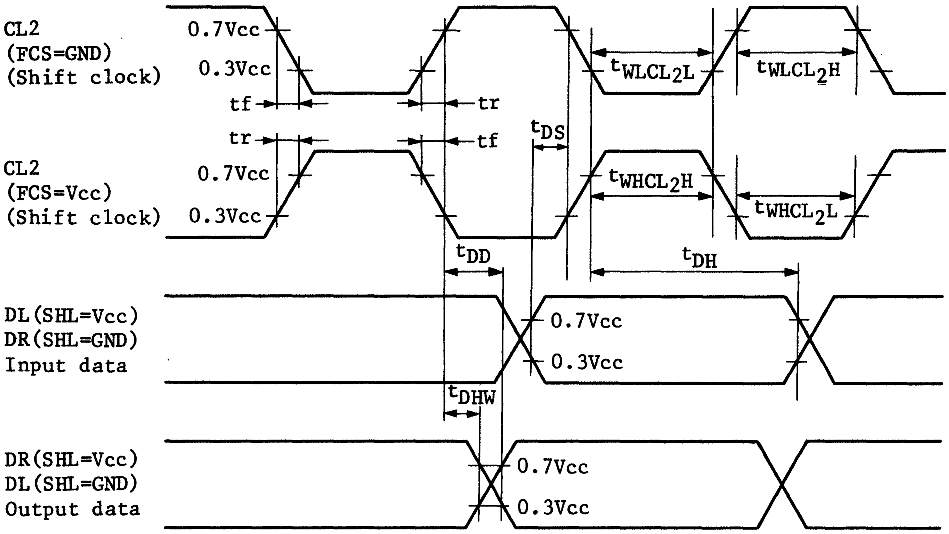
- Output Terminal



Applicable terminals:
X1 to X64

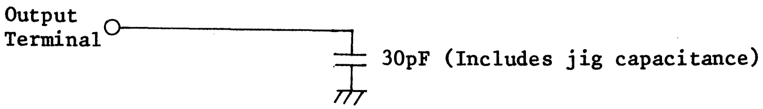
- AC Characteristics (V_{CC}=5V±10% GND=0V, Ta=-20∼+75°C)

(1) In the slave mode (M/S=GND)



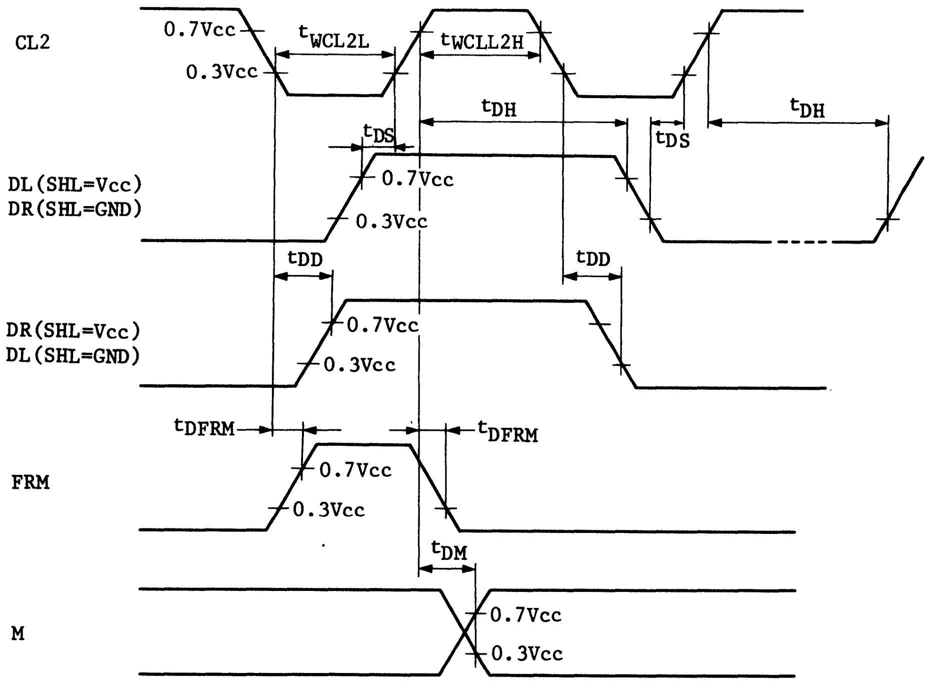
Item	Symbol	Min.	Typ.	Max	Unit	Note
CL2 "Low" level width (FCS=GND)	t_{WLCL2L}	450	-	-	ns	
CL2 "High" level width (FCS=GND)	t_{WLCL2H}	150	-	-	ns	
CL2 "Low" level width (FCS=V_{CC})	t_{WHCL2L}	150	-	-	ns	
CL2 "High" level width (FCS=V_{CC})	t_{WHCL2H}	450	-	-	ns	
Data setup time	t_{DS}	100	-	-	ns	
Data hold time	t_{DH}	100	-	-	ns	
Data delay time	t_{DD}	-	-	200	ns	1
Output data hold time	t_{DHW}	10	-	-	ns	
CL2 rise time	tr	-	-	30	ns	
CL2 fall time	t_f	-	-	30	ns	

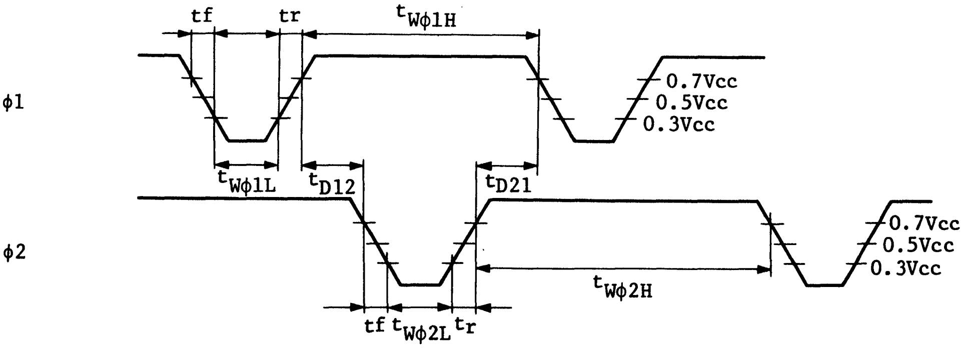
Note 1) The following load circuit is connected for specification.



(2) In the master mode

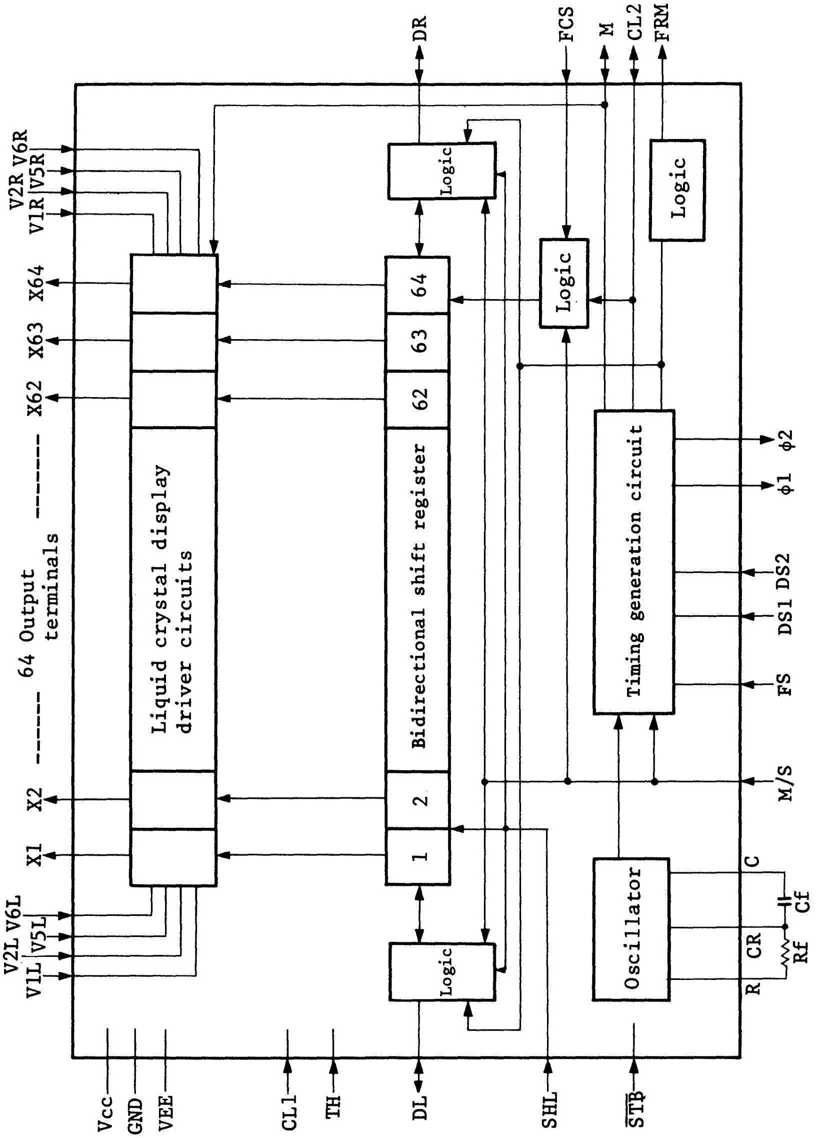
(M/S=V_{CC}, FCS=V_{CC}, Cf=20pF, Rf=47KΩ)





Item	Symbol	Min.	Typ.	Max.	Unit
Data setup time	t_{DS}	20	-	-	μs
Data hold time	t_{DH}	40	-	-	μs
Data delay time	t_{DD}	5	-	-	μs
FRM delay time	t_{DFRM}	-2	-	2	μs
M delay time	t_{DM}	-2	-	2	μs
CL_2 "Low" level width	t_{WCL2L}	35	-	-	μs
CL_2 "High" level width	t_{WCL2H}	35	-	-	μs
$\phi1$ "Low" level width	$t_{W\phi1L}$	700	-	-	ns
$\phi2$ "Low" level width	$t_{W\phi2L}$	700	-	-	ns
$\phi1$ "High" level width	$t_{W\phi1H}$	2100	-	-	ns
$\phi2$ "High" level width	$t_{W\phi2H}$	2100	-	-	ns
$\phi1$-$\phi2$ phase difference	t_{D12}	700	-	-	ns
$\phi2$-$\phi1$ phase difference	t_{D21}	700	-	-	ns
$\phi1$, $\phi2$ rise time	tr	-	-	150	ns
$\phi1$, $\phi2$ fall time	tf	-	-	150	ns

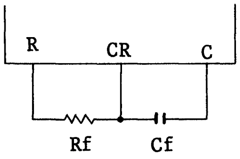
■ Block Diagram

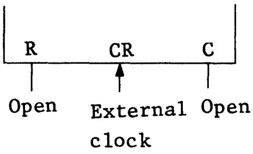


Block Functions

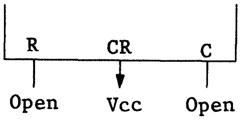
- Oscillator

The oscillator is a CR oscillator that generates display timing signals and operating clocks for the HD61202. It is required when the HD61203 is used with the HD61202. It attaches an oscillation resistor Rf and an oscillation capacity Cf as shown in the following figure and terminal $\overline{\mathrm{STB}}$ is connected to "high" level. When using an external clock, input the clock into terminal CR and don't connect any lines to terminal R and C.





Oscillator is not required when the HD61203 is used with the HD61830. Then, connect terminal CR to "high" level and don't connect any lines to terminals R and C.



- Timing Generator Circuit

The timing generator circuit generates display timing and operating clock for the HD61202. This circuit is required when the HD61203 is used with the HD61202. Then connect terminal M/S to "high" level. (master mode). It is not necessary when display timing signal is supplied from other circuits, for example, from HD61830. In this case connect the terminals FS, DS1 and DS2 to "high" level and M/S to "low" level. (Slave mode)

- Bidirectional Shift Register

This is a 64-bit bidirectional shift register. The data is shifted from DL to DR when SHL is at high level and from DR to DL when SHL is at low level. In this case, CL2 is used as shift clock. The lowest order bit of the bidirectional shift register, which is on the side of DL, corresponds to X1 and the highest order bit on the side of DR corresponds to X64.

- Liquid Crystal Display Driver Circuit

The combination of the data from the shift register with M signal allows one of the four liquid crystal display driver levels V1, V2, V5 and V6 to be transferred to the output terminals.

Data from the shift register	M	Output level
1	1	V2
0	1	V6
1	0	V1
0	0	V5

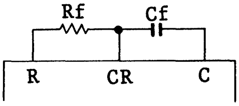
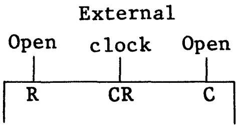
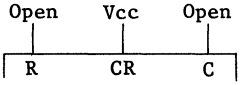
HD61203 Terminal Functions

Terminal name	Number of terminals	I/O	Connected to	Function
VCC GND VEE	1 1 2		Power supply	V_{CC}-GND: Power supply for internal logic. V_{CC}-V_{EE}: Power supply for driver circuit logic.
V1L,V2L, V5L,V6L V1R,V2R V5R,V6R	8		Power supply	Liquid crystal display driver level power supply. V1L(V1R), V2L(V2R): Selected level V5L(V5R), V6L(V6R): Non-selected level voltages of the level power supplies connected to V1L and V1R should be the same. (This applies to the combination of V2L & V2R, V5L & V5R and V6L & V6R respectively)
M/S	1	I	V_{CC} or GND	Selects Master/Slave M/S=V_{CC}: In master mode When the HD61203 is used with the HD61202, timing generation circuit operates to supply display timing signals and operation clock to the HD61202. Each of I/O common terminals DL, DR, CL2 and M is in the output state. M/S=GND: In slave mode The timing operation circuit stops operating. The HD61203 is used in this mode when combined with the HD61830. Even if combined with the HD61202, this mode is used when display timing signals (M, data, CL2 etc.) are supplied by another HD61203 in the master mode. Terminals M and CL2 are in the input state.

(to be continued)

<table>
<tr><th>Terminal name</th><th>Number of terminals</th><th>I/O</th><th>Connected to</th><th>Function</th></tr>
<tr><td>M/S</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>When SHL is V_{CC}, DL is in the input state and DR is in the output state.
When SHL is GND, DL is in the output state and DR is in the input state.</td></tr>
<tr><td>FCS</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects shift clock phase
FCS=V_{CC} Shift register operates at the rising edge of CL2. Select this condition when HD61203 is used with HD61202 or when MA of the HD61830 connects to CL2 in the combination with the HD61830.
FCS=GND Shift register operates at the fall of CL2. Select this condition when CL1 of HD61830 connects to CL2 in the combination with the HD61830.</td></tr>
<tr><td>FS</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects frequency
When the frame frequency is 70Hz, the oscillation frequency should be:
fosc=430kHz at FCS=V_{CC}
fosc=215kHz at FCS=GND
This terminal is active only in the master mode. Connect it to V_{CC} in the slave mode.</td></tr>
<tr><td>DS1,DS2</td><td>2</td><td>I</td><td>V_{CC} or GND</td><td>Selects display duty factor
<table>
<tr><th>Display Duty</th><th>1/48</th><th>1/64</th><th>1/96</th><th>1/128</th></tr>
<tr><td>DS1</td><td>GND</td><td>GND</td><td>V_{CC}</td><td>V_{CC}</td></tr>
<tr><td>DS2</td><td>GND</td><td>V_{CC}</td><td>GND</td><td>V_{CC}</td></tr>
</table>
This terminals are valid only in the master mode. Connect them to V_{CC} in the slave mode.</td></tr>
</table>

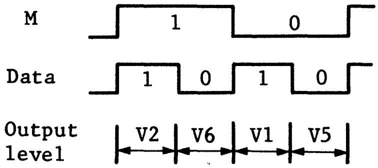
(to be continued)

Terminal name	Number of terminals	I/O	Connected to	Function
$\overline{\text{STB}}$ TH CL1	1 1 1	I	V_{CC} or GND	Input terminal for testing Connect $\overline{\text{STB}}$ to V_{CC}. Connect TH and CL1 to GND.
CR,R,C	3			Oscillator. In the master mode, use these terminals as shown below. Usage of these terminal in the master mode Internal oscillation External clock   In the slave mode, stop the oscillator as shown below. 
ϕ1, ϕ2	2	O	HD61202	Operating clock output terminals for the HD61202. Master mode: Connect these terminals to terminals ϕ1 and ϕ2 of the HD61202 respectively. Slave mode : Don't connect any lines to these terminals.
FRM	1	O	HD61202	Frame signal Master mode: Connect this terminal to terminals FRM of the HD61202. Slave mode : Don't connect any lines to this terminal.

(to be continued)

<table>
<tr><th>Terminal name</th><th>Number of terminals</th><th>I/O</th><th>Connected to</th><th>Function</th></tr>
<tr><td>M</td><td>1</td><td>I/O</td><td>MB of HD61830 or M of HD61202</td><td>Signal to convert LCD driver signal into AC.
Master mode: Output terminal. Connect this terminal to terminal M of the HD61202.
Slave mode : Input terminal. Connect this terminal to terminal MB of the HD61830.</td></tr>
<tr><td>CL2</td><td>1</td><td>I/O</td><td>CL1 or MA of HD61830 or CL of HD61202</td><td>Shift clock
Master mode: Output terminal Connect this terminal to terminal CL of the HD61202.
Slave mode : Input terminal Connect this terminal to terminal CL1 or MA of the HD61830.</td></tr>
<tr><td>DL, DR</td><td>2</td><td>I/O</td><td>Open or FLM of HD61830</td><td>Data I/O terminals of bidirectional shift register.
DL corresponds to X1's side and DR to X64's side.
Master mode: Output common scanning signal. Don't connect any lines to these terminals normally.
Slave mode : Connect terminal FLM of the HD61830 to DL (when SHL=V_{CC}) or DR (when SHL=GND)
<table>
<tr><td>M/S</td><td colspan="2">V_{CC}</td><td colspan="2">GND</td></tr>
<tr><td>SHL</td><td>V_{CC}</td><td>GND</td><td>V_{CC}</td><td>GND</td></tr>
<tr><td>DL</td><td>Output</td><td>Output</td><td>Input</td><td>Output</td></tr>
<tr><td>DR</td><td>Output</td><td>Output</td><td>Output</td><td>Input</td></tr>
</table>
</td></tr>
</table>

(to be continued)

<table>
<tr><th>Terminal name</th><th>Number of terminals</th><th>I/O</th><th>Connected to</th><th>Function</th></tr>
<tr><td>NC</td><td>5</td><td></td><td>Open</td><td>Not used.
Don't connect any lines to this terminal.</td></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects shift direction of bidirectional shift register.
<table>
<tr><th>SHL</th><th>Shift direction</th><th>Common scanning direction</th></tr>
<tr><td>V_{CC}</td><td>DL → DR</td><td>X1 → X64</td></tr>
<tr><td>GND</td><td>DL ← DR</td><td>X1 ← X64</td></tr>
</table></td></tr>
<tr><td>X1∿X64</td><td>64</td><td>O</td><td>Liquid crystal display</td><td>Liquid crystal display driver output.
Output one of the four liquid crystal display driver levels V1, V2, V5 and V6 with the combination of the data from the shift register and M signal.

Data "1" — Selected level
"0" — Non-selected level
When SHL is V_{CC}, X1 corresponds to COM1 and X64 corresponds to COM64.
When SHL is GND, X64 corresponds to COM1 and X1 corresponds to COM64.</td></tr>
</table>

HD61203 Connection List

H...V_{CC} } Fixed
L...GND }

"-" means "open".

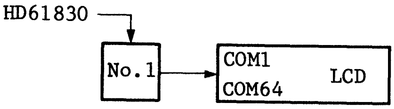
Rf...Oscillation resistor
Cf...Oscillation capacity

	M/S	TH	CL1	FCS	FS	DS1	DS2	$\overline{\text{STB}}$	CR	R	C	$\phi1$	$\phi2$	FRM	M	CL2	SHL	DL	DR	X1 ∿ X64
A	L	L	L	L	H	H	H	H	H	-	-	-	-	-	from MB of HD61830	from CL1 of HD61830	H	from FLM of HD61830	-	COM1 ∿COM64
																	L	-	from FLM of HD61830	COM64 ∿COM1
B	L	L	L	H	H	H	H	H	H	-	-	-	-	-	from MB of HD61830	from MA of HD61830	H	from FLM of HD61830	to DL/DR of HD61203 No.2	COM1 ∿COM64
																	L	to DL/DR of HD61203 No.2	from FLM of HD61830	COM64 ∿COM1
C	L	L	L	H	H	H	H	H	H	-	-	-	-	-	from MB of HD61830	from MA of HD61830	H	from DL/DR of HD61203 No.1	-	COM65 ∿COM128
																	L	-	from DL/DR of HD61203 No.1	COM128∿COM65
D	H	L	L	H	H	L or L	L H	H	Rf Cf	Rf	Cf	to $\phi1$ of HD61202	to $\phi2$ of HD61202	to FRM of HD61202	to M of HD61202	to CL of HD61202	H	-	-	COM1 ∿COM64
																	L	-	-	COM64 ∿COM1
E	H	L	L	H	H	L or L	L H	H	Rf Cf	Rf	Cf	to $\phi1$ of HD61202	to $\phi2$ of HD61202	to FRM of HD61202	to M of HD61202 HD61203	to CL of HD61202 to CL2 of HD61203	H	-	to DL/DR of HD61203 No.2	COM1 ∿COM64
																	L	to DL/DR of HD61203 No.2	-	COM64 ∿COM1
F	L	L	L	H	H	H	H	H	H	-	-	-	-	-	from M of HD61203 No.1	from CL2 of HD61203 No.1	H	from DL/DR of HD61203 No.1	-	COM1 ∿COM64
																	L	-	from DL/DR of HD61203 No.1	COM64 ∿COM1

Outline of HD61203 System Configuration

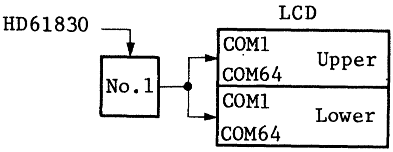
1) Use with HD61830

a) When display duty ratio of LCD is 1/64



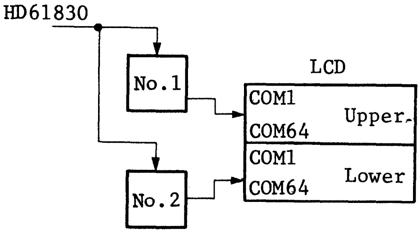
One HD61203 drives common signals.

Refer to Connection list 'A'



One HD61203 drives common signals for upper and lower panels.

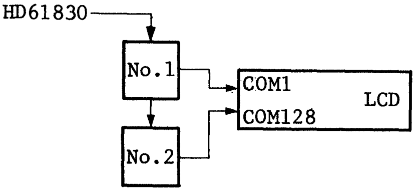
Refer to Connection list 'A'



Two HD61203's drive upper and lower panel separately to ensure the quality of display. No.1 and No.2 operate in parallel.

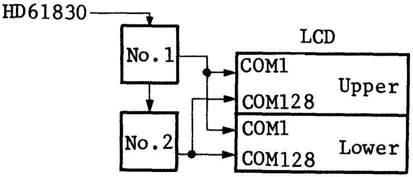
For both of No.1 and No.2, refer to Connection list 'A'

b) When display duty ratio of LCD is from 1/65 to 1/128



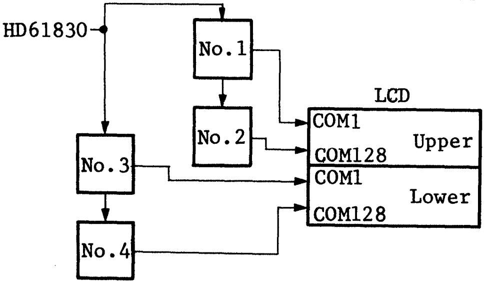
Two HD61203's connected serially drive common signals.

Refer to Connection list 'B' for No.1.
Refer to Connection list 'C' for No.2.



Two HD61203 's connected serially drive upper and lower panels in parallel.

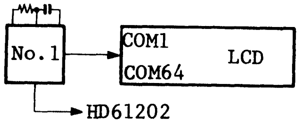
Refer to Connection list 'B' for No.1.
Refer to Connection list 'C' for No.2.



Two sets of HD61203 's connected serially drive upper and lower panels in parallel to ensure the quality of display.

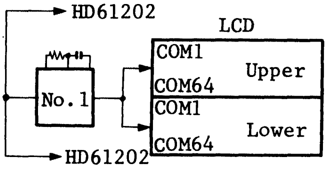
Refer to Connection list 'B' for No.1 and 3.
Refer to Connection list 'C' for No.2 and 4.

2) Use with HD61202 (1/64 duty)



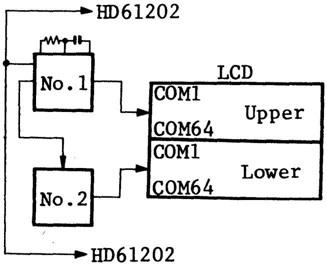
One HD61203 drives common signals and supplies timing signals to the HD61202's.

Refer to Connection list 'D'



One HD61203 drives upper and lower panels and supplies timing signals to the HD61202's.

Refer to Connection list 'D'



Two HD61203 's drive upper and lower panels in parallel to ensure the quality of display. No.1 supplies timing signals to No.2 and the HD61202's.

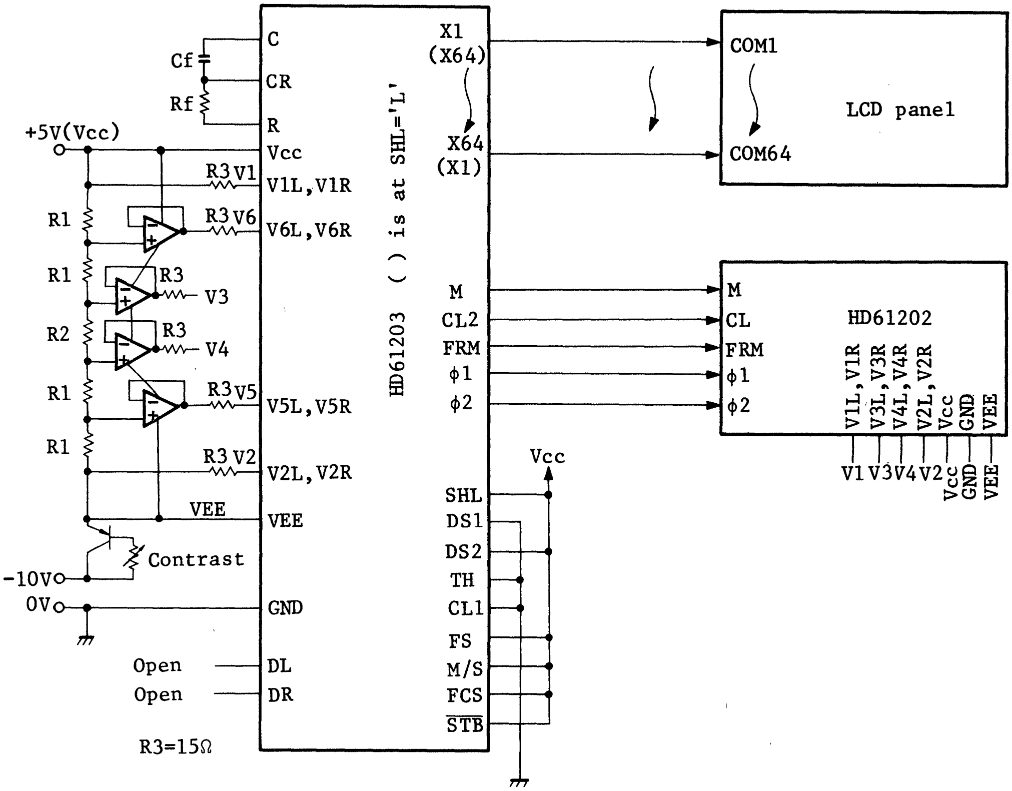
Refer to Connection list 'E' for No.1

Refer to Connection list 'F' for No.2

- Example of Connection 1)

(1) Use with HD61202 (RAM type segment driver)

a) 1/64 duty ratio (See Connection List "D")



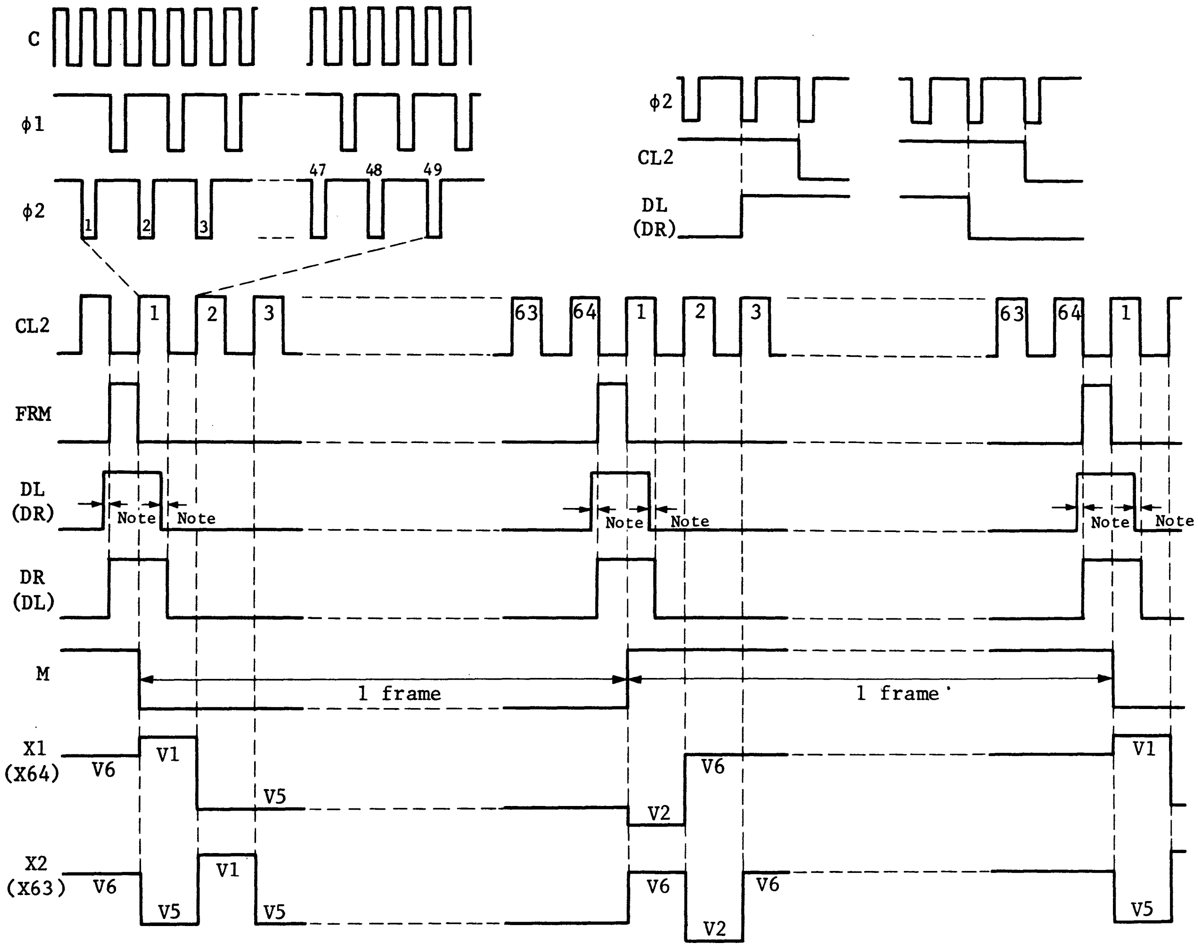
Note 1) The values of R1 and R2 vary with the LCD panel used. When bias factor is 1/9, the values of R1 and R2 should satisfy

$$\frac{R1}{4R1 + R2} = \frac{1}{9}$$

For example,

R1=3kΩ, R2=15kΩ

Example of Waveform (RAM type, 1/64 duty)



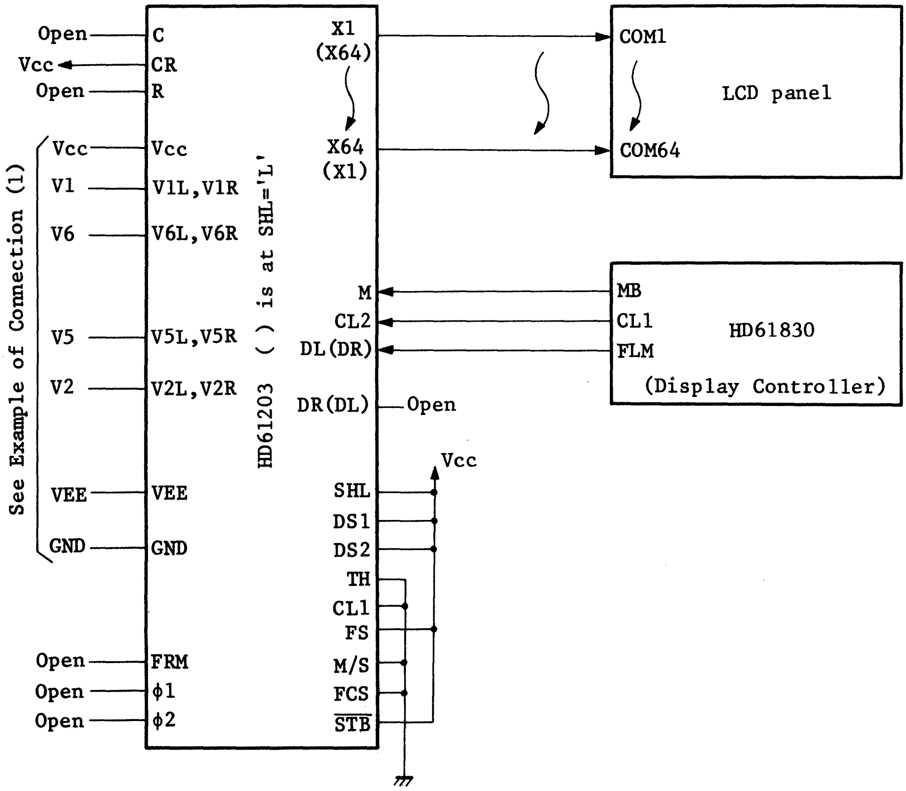
( ) ... at SHL='L'

Note) Phase difference between DL(DR) and CL2

Example of Connection 2)

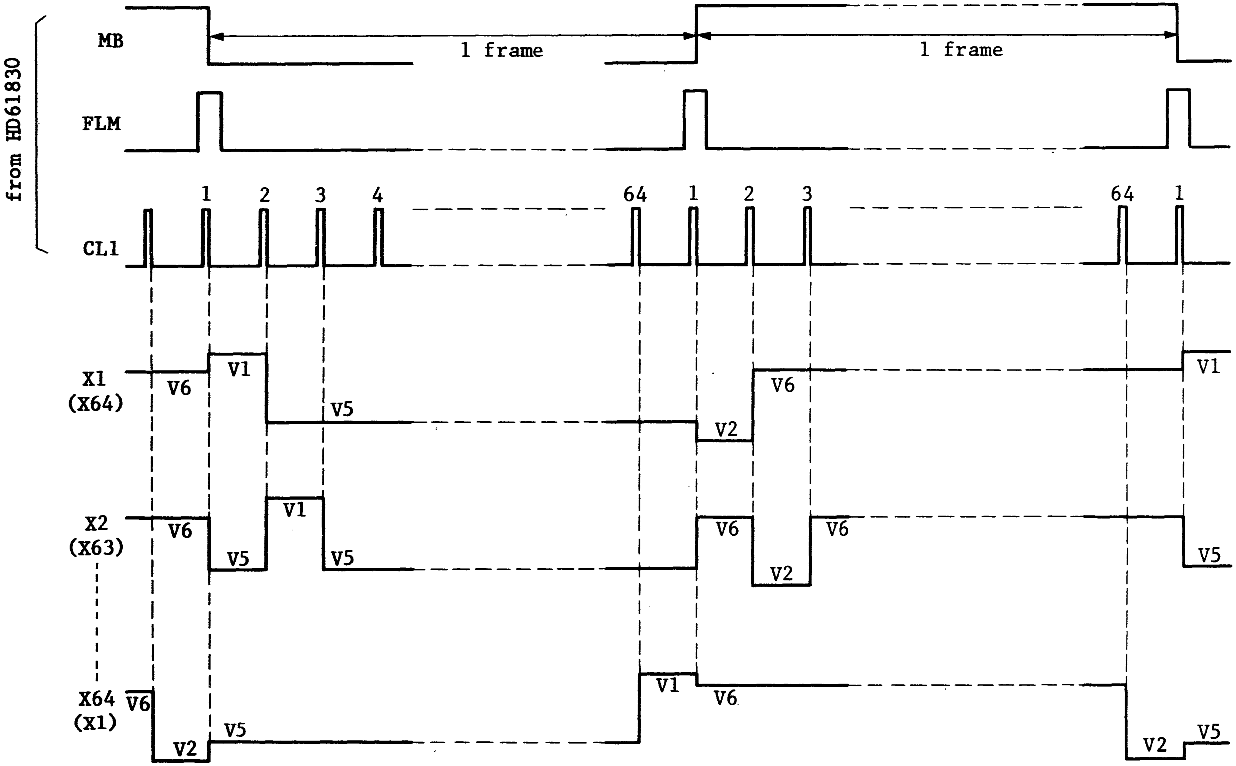
(2) Use with HD61830 (Display controller)

a) 1/64 duty ratio (See Connection List "A")



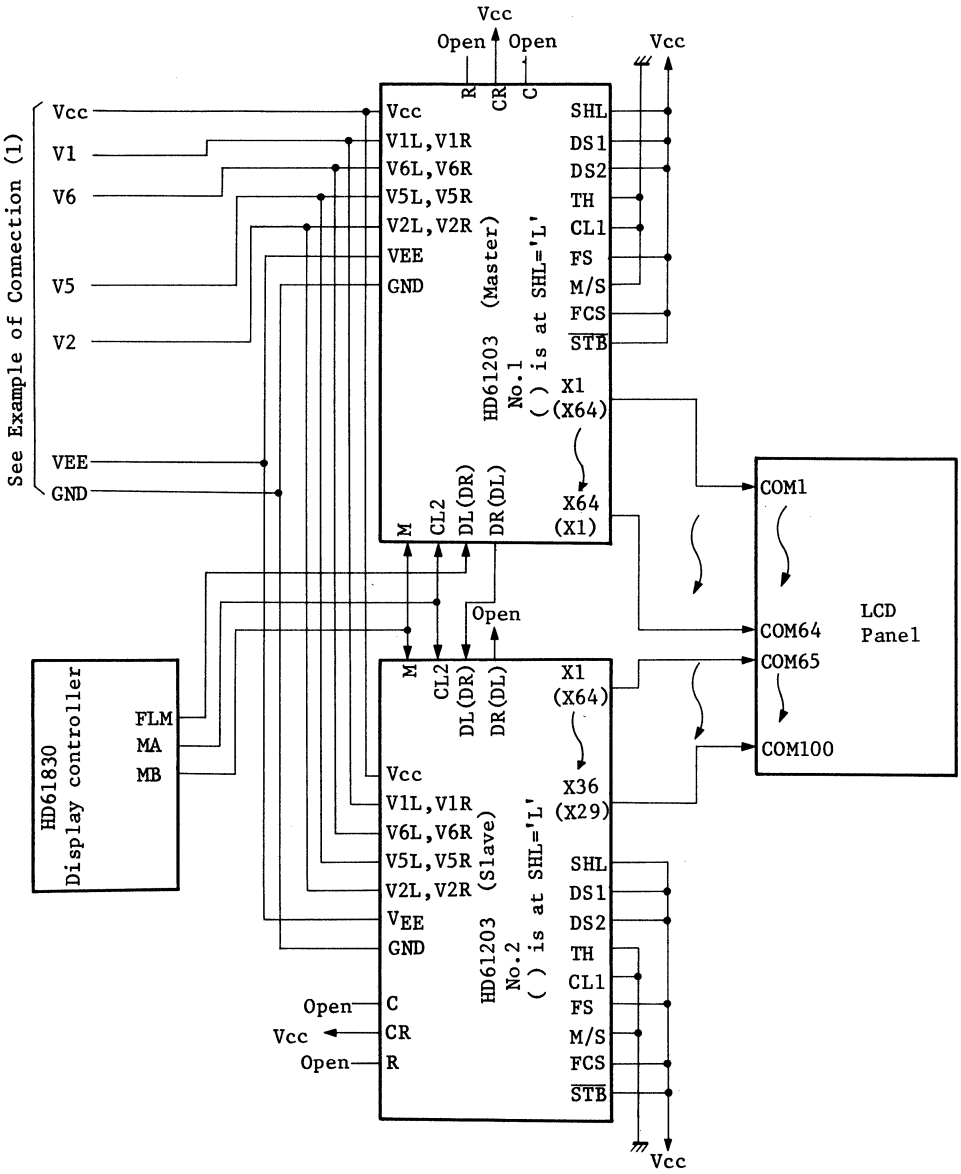
Example of Waveform

a) 1/64 duty ratio

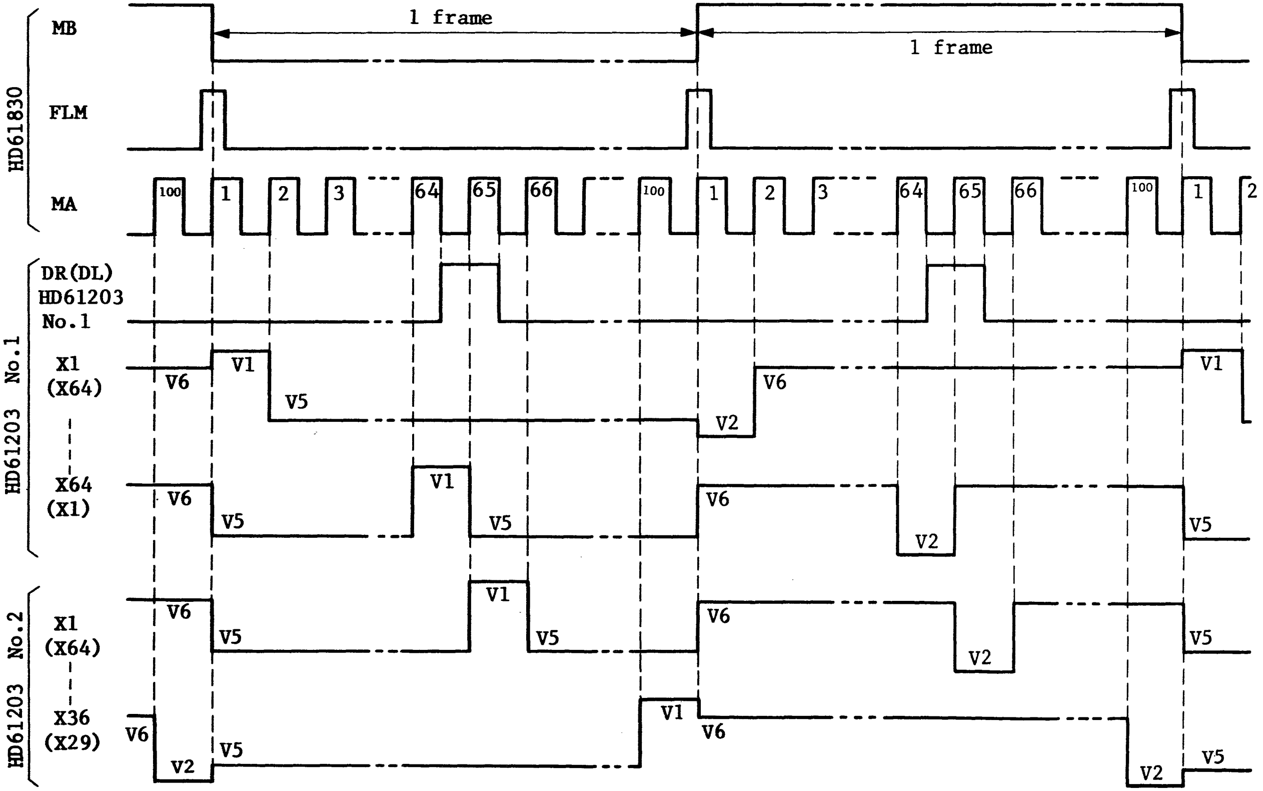


( ) ... at SHL='L'

b). 1/100 duty ratio (See Connection List 'B' 'C')



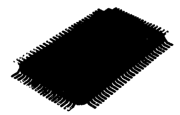
Example of Waveform b) 1/100 duty



HD61104, HD61104A
(Dot Matrix Liquid Crystal Graphic Display Column Driver)

DESCRIPTION

HD61104, HD61104A is a column (segment) driver for large-area dot matrix liquid crystal graphic display systems.



(FP-100)

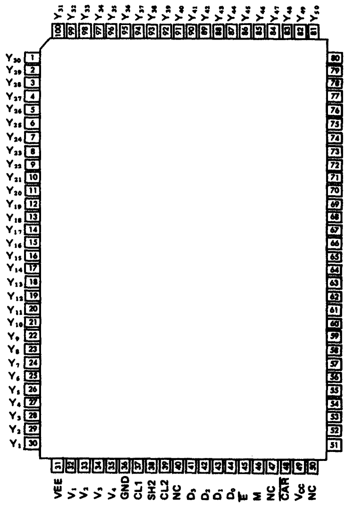
■ FEATURES

- Display duty 1/64 ∿ 1/200
- Internal liquid crystal display driver 80 drivers
- 4-bit bus, bi-directional shift data transfer
- Cascade connection with enable format
- Data transfer rate 3.5 MHz
- Power supply for logic circuit 5V ± 10%
- Power supply for LCD drive circuits:
  - 10 to 26V (HD61104)
  - 10 to 28V (HD61104A)
- Stand-by function
- CMOS process
- 100-pin flat plastic package

■ ORDERING INFORMATION

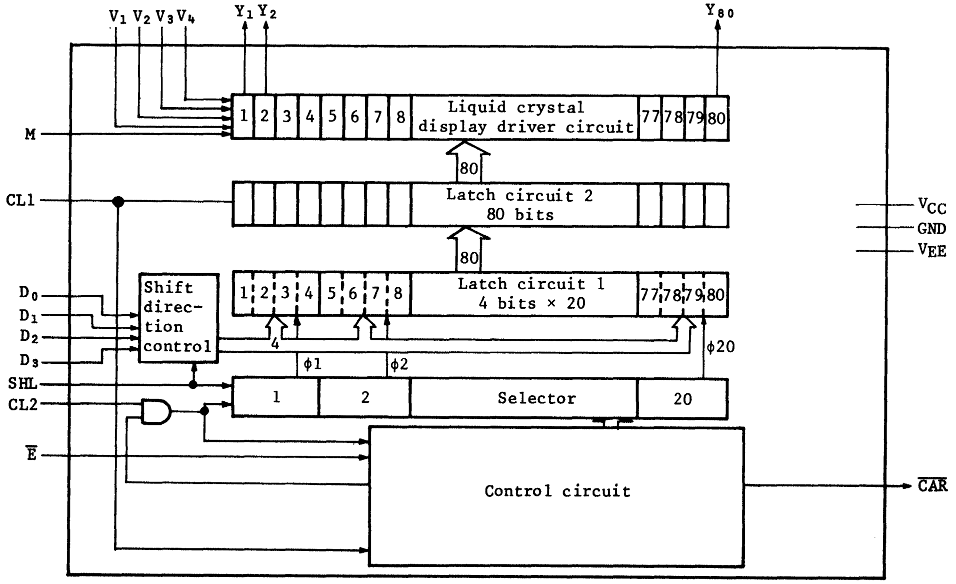
Type No.	LCD driving Level (V)	Package
HD61104	+10 to +26	100 pin plastic QFP (FP-100)
HD61104A	+10 to +28 V	

■ Pin Arrangement



(Top View)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Value	Unit	Note
Supply voltage (1)		V_{CC}	-0.3 to +7.0	V	2
Supply voltage (2)	HD61104	V_{EE}	V_{CC} - 28.0 to V_{CC} + 0.3	V	
	HD61104A	V_{EE}	V_{CC} - 28.5 to V_{CC} + 0.3		
Terminal voltage (1)		V_{T1}	-0.3 to V_{CC} + 0.3	V	2, 3
Terminal voltage (2)		V_{T2}	V_{EE} - 0.3 to V_{CC} + 0.3	V	4
Operating temperature		Topr	-20 to +75	°C	
Storage temperature		Tstg	-55 to +125	°C	

(Note 1) LSI's may be permanently destroyed if being used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the limits of electrical characteristics, because using beyond these conditions may cause malfunction and poor reliability.

(Note 2) All voltage values are referred to GND = 0V.

(Note 3) Applies to input terminals, SHL, CL1, CL2, D0 - D3, $\overline{E}$ and M.

(Note 4) Applies to V1, V2, V3 and V4. Must maintain

$$V_{CC} \geq V1 \geq V3 \geq V4 \geq V2 \geq V_{EE}$$

Connect a protection resistor of 15Ω ± 10% to each terminals in series.

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, GND = 0V, $V_{CC} - V_{EE}$ = 10 to 26V (HD61104), $V_{CC} - V_{EE}$ = 10 to 28 (HD61104A), Ta = -20 to +75°C)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit	Note
Input "High" voltage	V_{IH}		0.7×V_{CC}		V_{CC}	V	1
Input "Low" voltage	V_{IL}		0		0.3×V_{CC}	V	1
Output "High" Voltage	V_{OH}	I_{OH}=-400μA	V_{CC}-0.4			V	2
Output "Low" voltage	V_{OL}	I_{OL}=400μA			0.4	V	2
Driver ON Resistance	R_{ON}	V_{EE}=-10V, Load current= 100μA			7.5	kΩ	5
Input Leakage Current	I_{IL1}	V_{IN}=0 to V_{CC}	-1		1	μA	1
Input Leakage Current	I_{IL2}	V_{IN}=V_{EE} to V_{CC}	-25		25	μA	3
Dissipation Current (1)	I_{GND}				2.0	mA	4
Dissipation Current (2)	I_{EE}	HD61104			0.2	mA	4
		HD61104A			0.4		
Dissipation Current (3)	I_{ST}				100	μA	4 5

(Note 1) Applies to CL1, CL2, SHL, $\overline{E}$, M, and D0 - D3.

(Note 2) Applies to $\overline{CAR}$.

(Note 3) Applies to V1, V2, V3 and V4.

(Note 4) Specified when display data is transferred under following conditions.

CL2 frequency fcp2 = 2.5 MHz (data transfer rate)
CL1 frequency fcp1 = 14.0 kHz (data latch frequency)
M frequency f_M = 35 Hz (frame frequency / 2)
Display duty ratio 1/200

Specified when V_{IH} = V_{CC}, V_{IL} = GND and no load on outputs.

I_{GND}: currents between V_{CC} and GND
IEE : currents between V_{CC} and V_{EE}

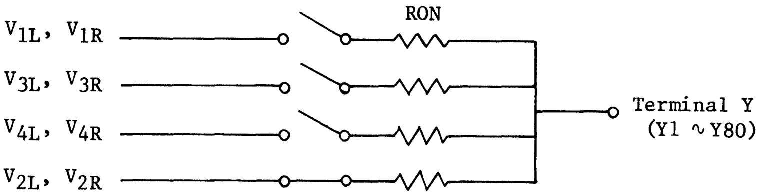
(Note 5) Currents between V_{CC} and GND at stand-by ($\overline{E}$ input = "H").

(Note 6) Resistance between terminal Y (one of Y1 to Y80) and terminal V (one of V1, V2, V3, and V4) when load current flows through one of the terminals Y1 to Y80. This value is specified under the following condition.

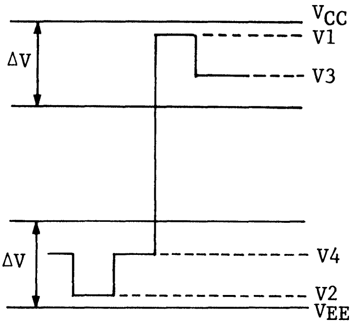
$V_{CC} - V_{EE} = 26V$

$V1, V3 = V_{CC} - 2/10\ (V_{CC} - V_{EE})$

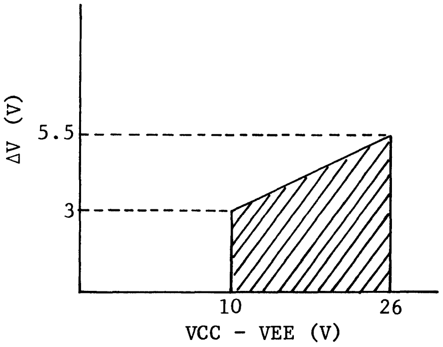
$V2, V4 = V_{EE} + 2/10\ (V_{CC} - V_{EE})$



Here is a description of the range of power supply voltage for liquid crystal display drive. Apply positive voltage to V1, and V3, and negative voltage to V2 and V4, within the ΔV range respectively. This range allows stable impedance on driver output (R_{ON}). Notice that ΔV depends on power supply voltage $V_{CC} - V_{EE}$.



Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive

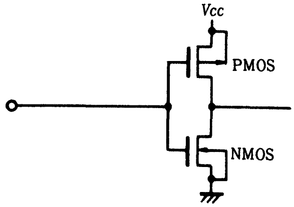


Correlation between Power Supply Voltage V_{CC}-V_{EE} and ΔV

Terminal Configuration

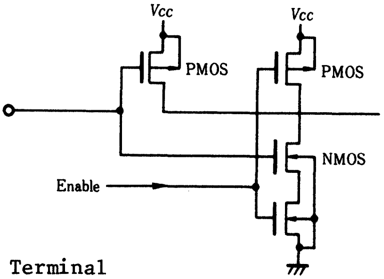
- Input Terminal

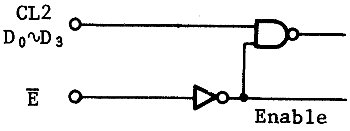
  Applicable Terminals: CL1, SHL, $\overline{E}$, M



- Input Terminal (controlled by Enable signal)

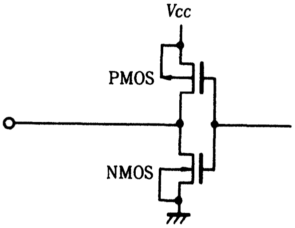
  Applicable Terminals: CL2, D0 ∿ D3





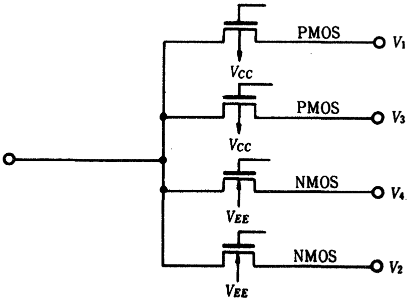
- Output Terminal

  Applicable Terminal: $\overline{\text{CAR}}$



- Output Terminal

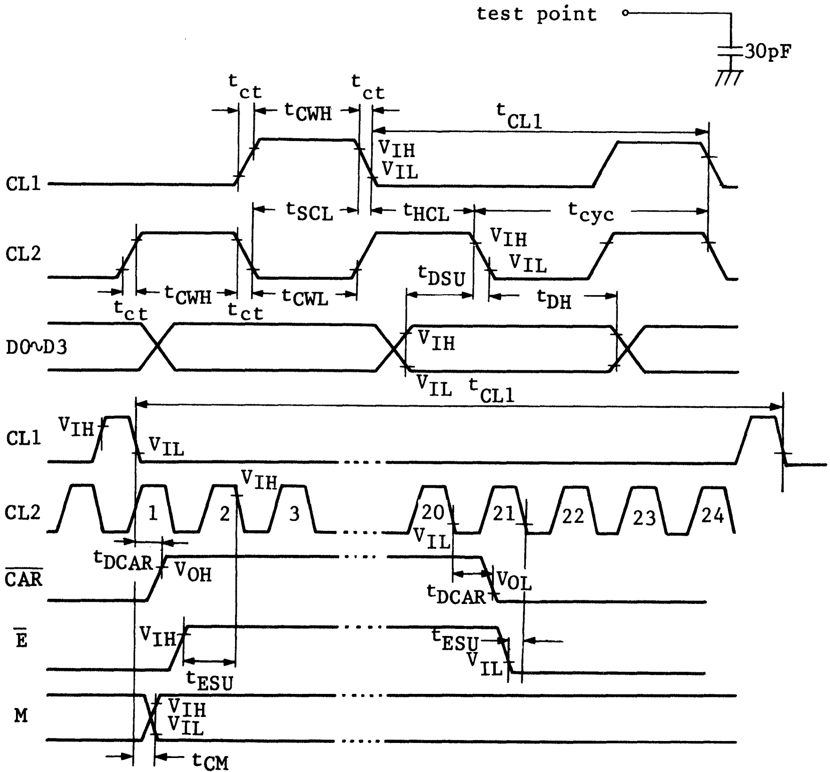
  Applicable Terminals: Y1 ∿ Y80

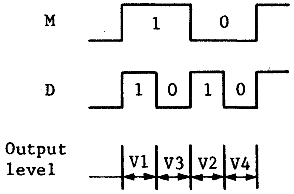


- AC CHARACTERISTICS
  (V_{CC} = 5V ± 10%, GND = 0V, Ta = -20 to +75°C)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit	Note
Clock cycle time	tCYC		285			ns	
Clock high level width	tCWH		110			ns	
Clock low level width	tCWL		110			ns	
Clock setup time	tSCL		80			ns	
Clock hold time	tHCL		80			ns	
Clock rise/fall time	tCT				30	ns	
Data setup time	tDSU		80			ns	
Data hold time	tDH		80			ns	
E setup time	tESU		75			ns	
Output delay time	tDCAR				180	ns	1
M phase difference time	tCM				300	ns	
CL1 cycle time	tCL1		tCYC × 10			ns	

Note 1) The following load circuits are connected for specification:



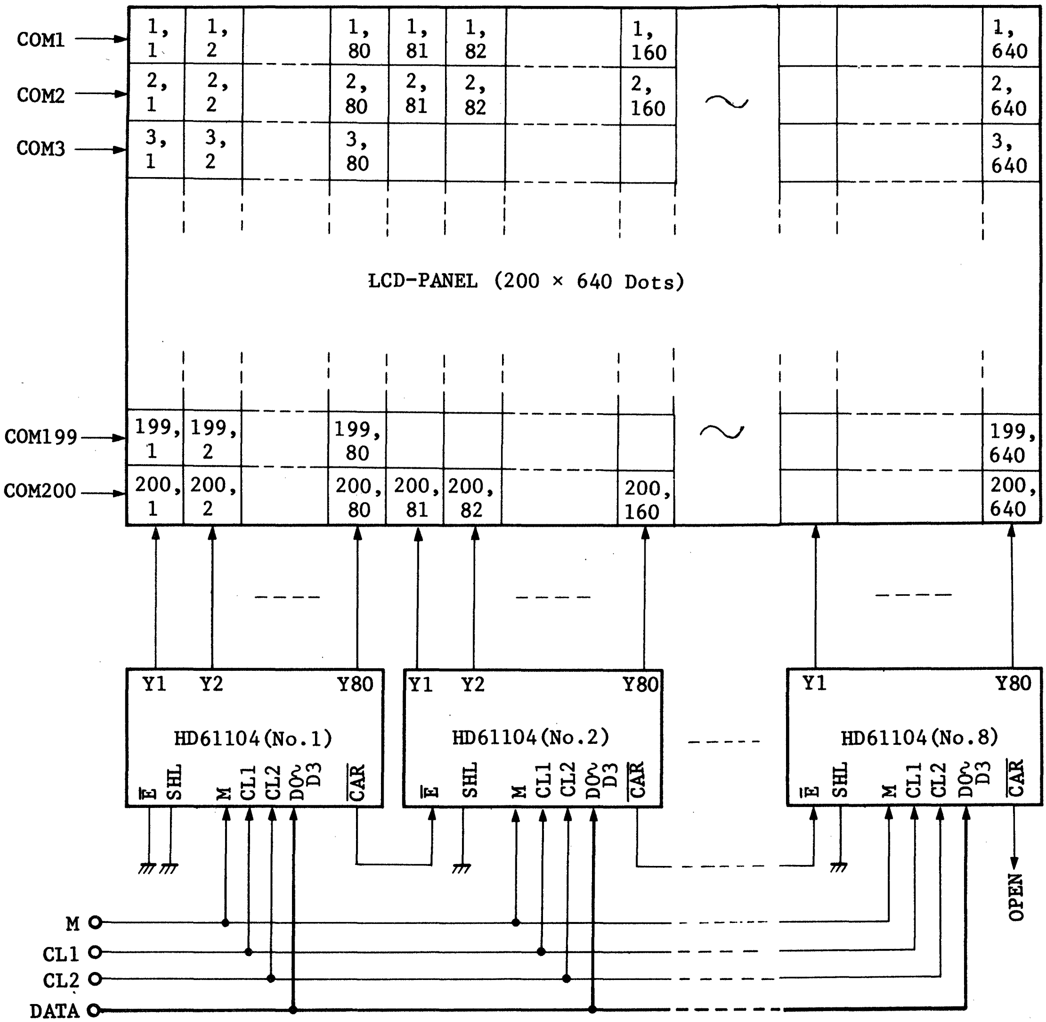
Terminal name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 1		Power supply	V_{CC} - GND: Power supply for internal logic V_{CC} - V_{EE}: Power supply for LCD drive circuit
V1 V2 V3 V4	4		Power supply	Power supply for liquid crystal drive V1, V2 --- selection level V3, V4 --- non-selection level
Y1~Y80	80	O	LCD	Liquid crystal driver outputs Selects one of the 4 levels, V1, V2, V3, and V4. Relation among output level, M, and display data (D) is as follows.  M 1 0 D 1 0 1 0 Output level V1 V3 V2 V4
M	1	I	Controller	Switch signal to convert liquid crystal drive waveform into AC.
CL1	1	I	Controller	Latch clock of display data (fall edge trigger) Synchronizing with the fall of CL1, liquid crystal driver signals corresponding to the display data are output.
CL2	1	I	Controller	Shift clock of display data (D) Fall edge trigger

-to be continued

<table>
<tr><th>Terminal name</th><th>Number of Terminals</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>D0~D3</td><td>4</td><td>I</td><td>Controller</td><td>Input of 4-bit display data (D)
<table>
<tr><th>(D)</th><th>Liquid Crystal driver output</th><th>Liquid crystal display</th></tr>
<tr><td>1
("H" level)</td><td>Selection level</td><td>ON</td></tr>
<tr><td>0
("L" level)</td><td>Non-selection level</td><td>OFF</td></tr>
</table>
Truth table Positive logic
<table>
<tr><th>SHL</th><th>Input data and latch circuit 1</th></tr>
<tr><td rowspan="4">0</td><td>D3 → 1 → 5 → 9 --- → 73 → 77</td></tr>
<tr><td>D2 → 2 → 6 → 10 --- → 74 → 78</td></tr>
<tr><td>D1 → 3 → 7 → 11 --- → 75 → 79</td></tr>
<tr><td>D0 → 4 → 8 → 12 --- → 76 → 80</td></tr>
<tr><td rowspan="4">1</td><td>D3 → 80 → 76 → 72 --- → 8 → 4</td></tr>
<tr><td>D2 → 79 → 75 → 71 --- → 7 → 3</td></tr>
<tr><td>D1 → 78 → 74 → 70 --- → 6 → 2</td></tr>
<tr><td>D0 → 77 → 73 → 69 --- → 5 → 1</td></tr>
</table>
ex.) When SHL="0", the data which is input to D3 is latched to each bit of the latch circuit 1 in order of 1 → 5 → 9 --- → 77.</td></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects a shift direction of display data.</td></tr>
<tr><td>$\overline{E}$</td><td>1</td><td>I</td><td>GND or the terminal $\overline{CAR}$ of the HD61104</td><td>Enable input
The operation stops with "H" level, and enables at "L" level.</td></tr>
<tr><td>$\overline{CAR}$</td><td>1</td><td>0</td><td>the input terminal $\overline{E}$ of the HD61104</td><td>Enable output
Used for cascade connection.</td></tr>
<tr><td>NC</td><td>3</td><td></td><td></td><td>Unused. No wire is to be connected.</td></tr>
</table>

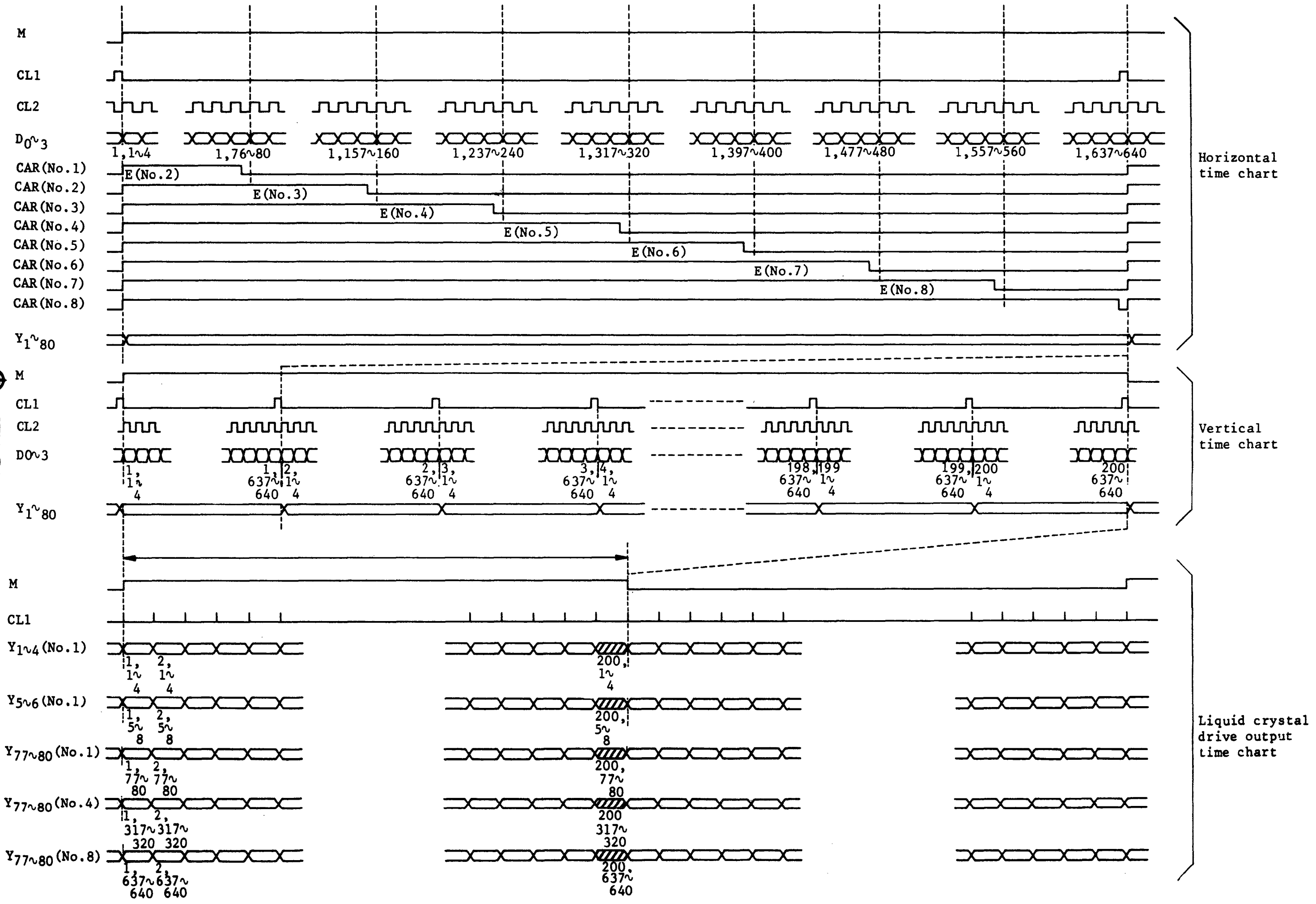
■TYPICAL APPLICATION

The following is the LCD panel with 200 × 640 dots on which characters are displayed with 1/200 duty dynamic drive.



Cascade eight HD61104's. Input data to the terminal D0∿D3 of No.1∿No.8. Connect $\overline{E}$ of No.1 to GND. No lines to be connected to $\overline{CAR}$ of No.8 Connect common signal terminals (COM1∿COM200) to the common driver HD61105. (m,n) of LCD panel is the address corresponding to each dot.

Example of Waveform



HD66106F
(LCD Driver for High Voltage)

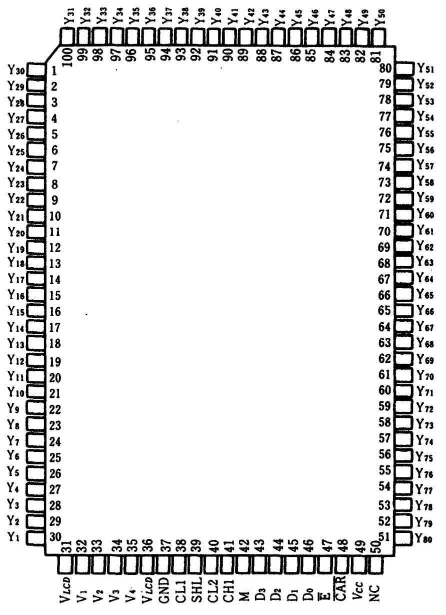
Description

The HD66106F LCD driver has a high duty ratio and many outputs for driving a large capacity dot matrix LCD panel.
It includes 80 LCD drive circuits and can drive up to 1/480 duty. For example, only 14 drivers are enough to drive an LCD panel of 640 × 480 dots. It also easily interfaces with various LCD controllers because of its internal automatic chip enable signal generator.
Using this LSI sharply lowers the cost of an LCD system.

Features

- Column and row driver
- 80 LCD drive circuits
- Multiplexing duty ratio: 1/100 to 1/480
- 4-bit parallel data transfer
- Internal automatic chip enable signal generator
- Internal standby function
- Recommended LCD controller LSI's: HD63645 and HD64645 (LCTC)
- Power supply: +5 V ± 10% for the internal logic, and 14.0 V to 37.0 V for LCD drive circuits
- Operation frequency: 6.0 MHz (max.)
- CMOS process
- 100-pin flat plastic package (FP-100)

Pin Arrangement



(Top view)

Pin Description

Power supply

V_{CC}, GND: V_{CC} supplies power to the internal logic circuit. GND is the logic and drive ground.

V_{LCD}: V_{LCD} supplies power to the LCD drive circuit.

V_1, V_2, V_3, and V_4: V_1-V_4 supply power for driving LCD (figure 1).

Control signals

CL1: The LSI latches data at the negative edge of CL1 when the LSI is used as a column driver. Fix to GND when the LSI is used as a row driver.

CL2: The LSI latches display data at the negative edge of CL2 when the LSI is used as a column driver, and shifts line select data at the negative edge when it is used as a row driver.

M: M changes LCD drive outputs to AC.

D_0-D_3: D_0-D_3 input display data for the column driver (table 2).

Table 1. Pin Function

Symbol	Pin No.	Pin Name	I/O
V_{CC}	49	V_{CC}	I
GND	37	Ground	I
V_{LCD}	31, 36	V_{LCD}	I
V_1	32	LCD voltage 1	I
V_2	33	V_2 LCD voltage 2	I
V_3	34	V_3 LCD voltage 3	I
V_4	35	V_4 LCD voltage 4	I
CL1	38	Clock 1	I
CL2	40	Clock 2	I
M	42	M	I
D_0-D_3	46-43	Data 0 to data 3	I
SHL	39	Shift left	I
$\overline{E}$	47	Enable	I
$\overline{CAR}$	48	Carry	O
CH1	41	Channel 1	I
Y_1-Y_{80}	30-1, 100-51	Drive outputs 1-80	O
NC	50	No connection	—

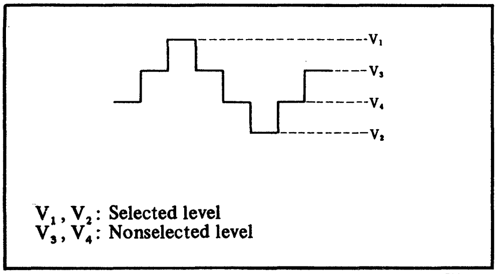


Figure 1. Power Supply for Driving LCD

Table 2. Relation between Display Data and LCD State

Display Data	LCD Outputs	LCD
1 (= high level)	Selected level	On
0 (= low level)	Nonselected level	Off

SHL: SHL controls the shift direction of display data and line select data (figure 2, table 3).

$\overline{E}$: $\overline{E}$ inputs the enable signal when the LSI is used as a column driver (CH1 = V_{CC}). The LSI is disabled when $\overline{E}$ is high and enabled when low. $\overline{E}$ inputs scan data when the LSI is used as a row driver (CH1 = GND). When HD66106Fs are connected in cascade, E connects with $\overline{CAR}$ of the preceding LSI.

$\overline{CAR}$: $\overline{CAR}$ outputs the enable signal when the LSI is used as a column driver (CH1 = V_{CC}). $\overline{CAR}$ outputs scan data when the LSI is used as a row driver (CH1 = GND). When HD66106Fs are connected in cascade, $\overline{CAR}$ connects with $\overline{E}$ of the next LSI.

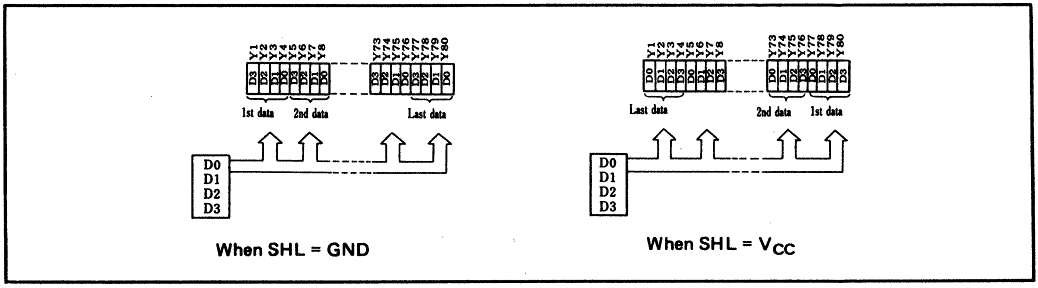
CH1: CH1 selects the driver function. The chip drives columns when CH1 = V_{CC}, and rows when CH1 = GND.

Y_1-Y_{80}: Each Y outputs one of the four voltage levels—V_1, V_2, V_3, or V_4—according to the combination of M and display data (figure 3).

NC: NC is not used. Do not connect any wire.

Table 3. Relation between SHL and Scan Direction of Selected Line (When LSI is Used as a Row Driver)

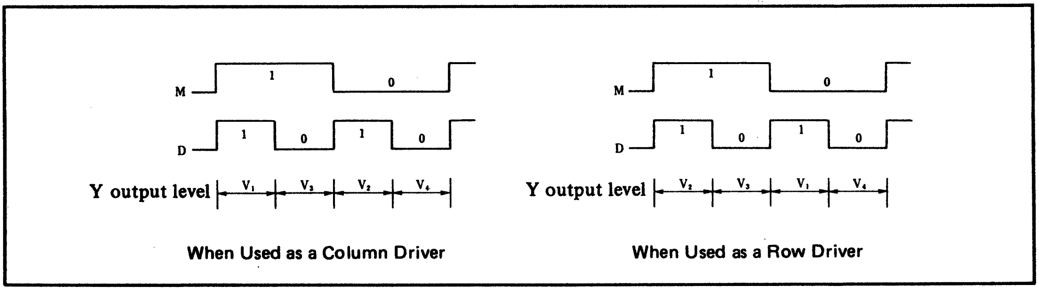
SHL	Shift Direction of Shift Register	Scan Direction of Selected Line
V_{CC}	$\overline{E}$ → 1 → 2 → 3 ---------------→ 80	Y_1 → Y_2 → Y_3 --------------------→ Y_{80}
GND	$\overline{E}$ → 80 → 79 → 78 ---------------→ 1	Y_{80} → Y_{79} → Y_{78} --------------------→ Y_1



When SHL = GND

When SHL = V_{CC}

Figure 2. Relation between SHL and Data Output (When LSI is Used as a Column Driver)



When Used as a Column Driver

When Used as a Row Driver

Figure 3. Selection of LCD Drive Output Level

Internal Block Diagram

LCD Drive Circuits

The HD66106F begins latching data when $\overline{E}$ goes low, which enables the data latching operation. It latches 4 bits of data simultaneously at the fall of CL2 and stops automatically (= standby state) when it has latched 80 bits.

Latch Circuit 2

When the LSI is used as a column driver, latch circuit 2 functions as an 80-bit latch circuit. It latches the data sent from latch circuit 1 at the fall of CL1 and transfers its outputs to the LCD drive circuits.

When the LSI is used as a row driver, this circuit functions as an 80-bit bidirectional shift register. The data sent from the $\overline{E}$ pin shifts at the fall of CL2. When SHL = V_{CC}, the data shifts from bit 1 to bit 80 in order of entry. When SHL = GND, the data shifts from bit 80 to bit 1.

Latch Circuit 1

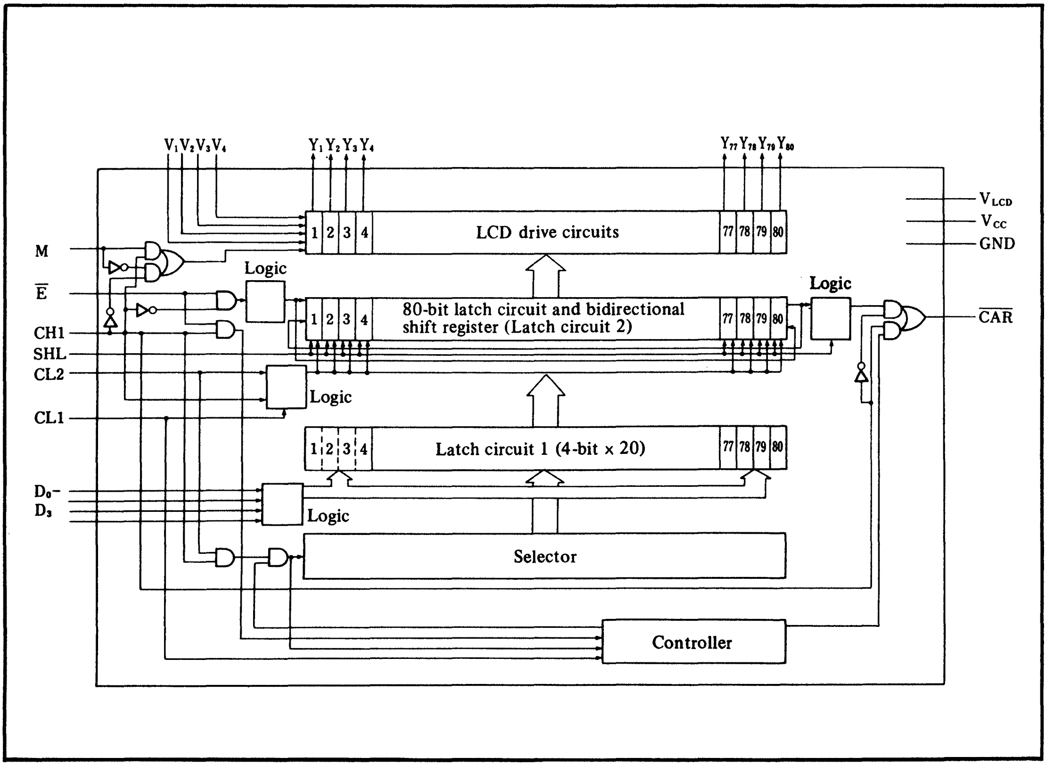
Latch circuit 1 is composed of twenty 4-bit parallel data latches. It latches the display data D_0-D_3 at the fall of CL2 when the LSI is used as a column driver. The signals sent from the selector determine which 4-bit latch should latch the data.

Selector

The selector is composed of a 5-bit up and down counter and a decoder. When the LSI is used as a column driver, it generates the latch signal to be sent to latch circuit 1, incrementing the counter at the negative edge of CL2.

Controller

The controller operates when the LSI is used as a column driver. It stops data latching when twenty pulses of CL2 have been input (= power-down function) and automatically generates the chip enable signal announcing the start of data latching into the next LSI.



Functional Description

When Used as a Column Driver

The HD66106F begins latching data when $\overline{E}$ goes low, which enables the data latching operation. It latches 4 bits of data simultaneously at the fall of CL2 and stops automatically (= standby state) when it has latched 80 bits.

Data outputs change at the fall of CL1. Latched data d_1 is transferred to the output pin Y_1 and d_{80} to Y_{80} when SHL = GND. Conversely, d_{80} is transferred to Y_1 and d_1 to Y_{80} when SHL = V_{CC}. The output level is selected out of V_1-V_4 according to the combination of display data and the alternating signal M (figure 4).

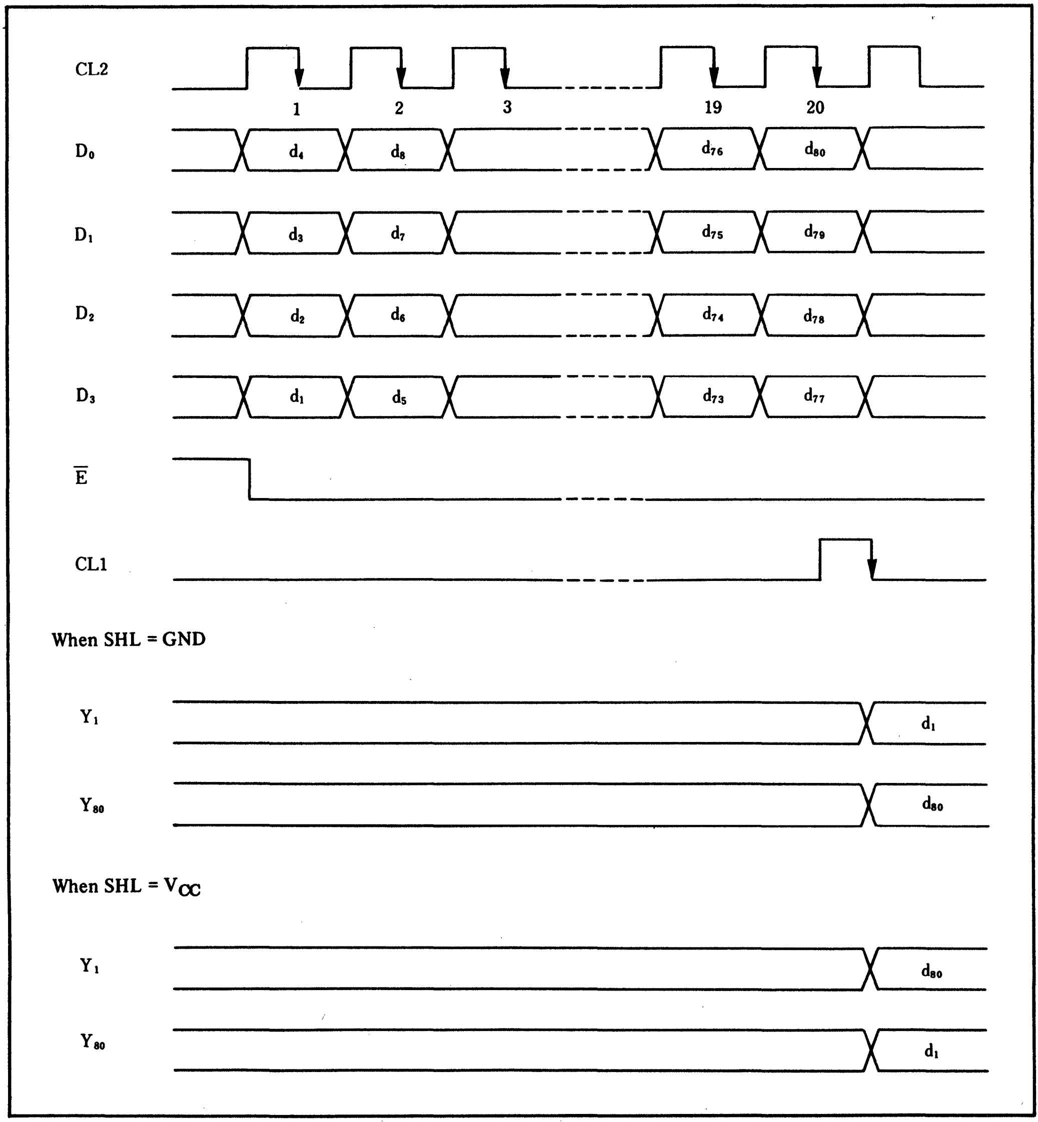


Figure 4. Column Driver Timing Chart

When Used as a Row Driver

The HD66106F shifts the line scan data sent from the pin $\overline{E}$ in order at the fall of CL2. When SHL = V_{CC}, data is shifted from Y_1 to Y_{80} and Y_{80} to Y_1 when SHL = GND.
In both cases, the data delayed for 80 bits by the shift register is output from the $\overline{CAR}$ pin to become the line scan data for the next LSI.

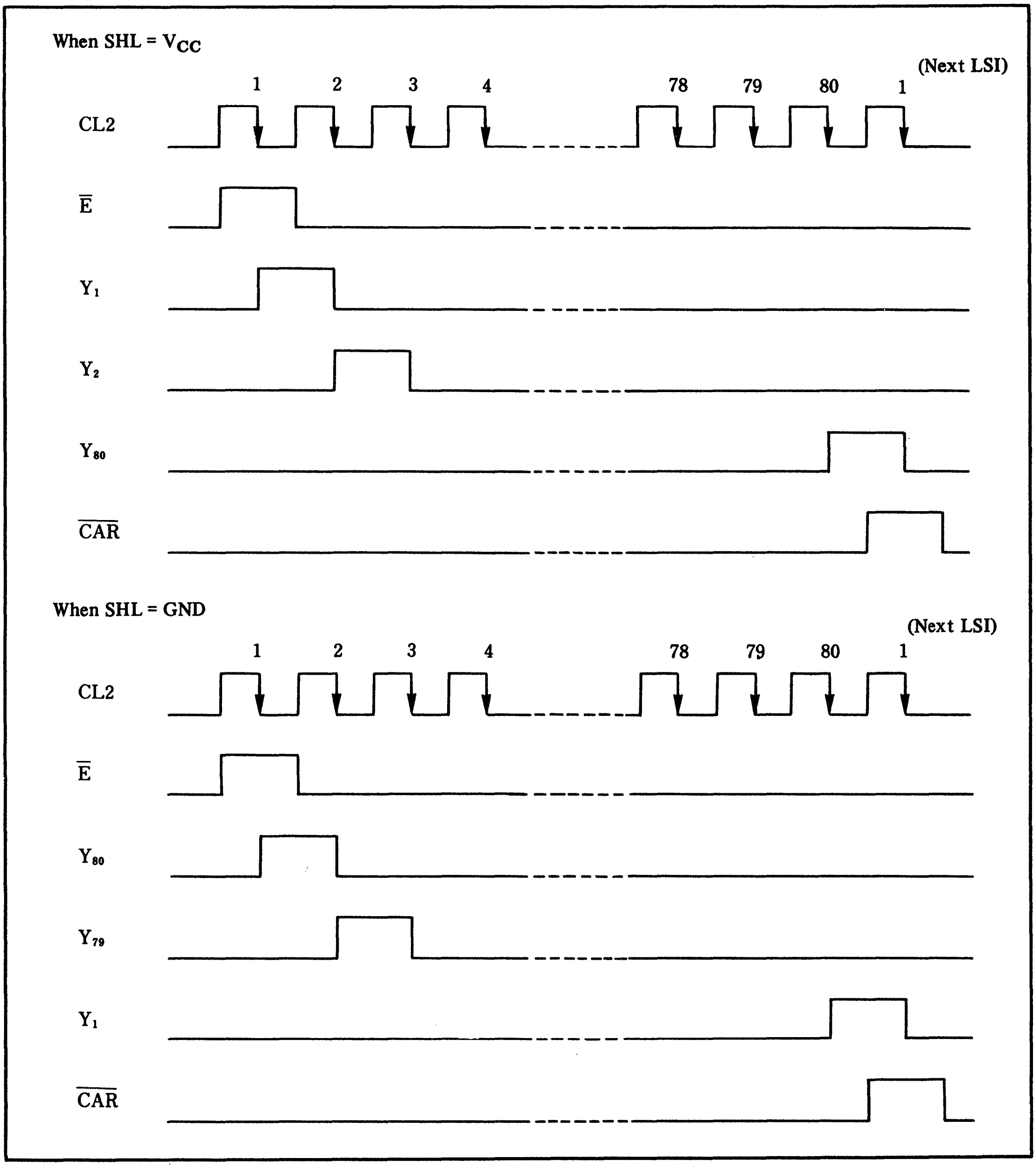


Figure 5. Row Driver Timing Chart

LCD Power Supply

This section explains the range of power supply voltage for driving LCD. V_1 and V_3 voltages should be near V_{LCD}, and V_2 and V_4 should be near GND (figure 6). Each voltage must be within ΔV. ΔV determines the range within which R_{ON}, impedance of driver's output, is stable. Note that ΔV depends on power supply voltage V_{LCD}-GND (figure 7).

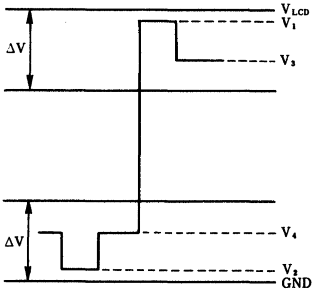


Figure 6. Driver's Output Waveform and Each Level of Voltage

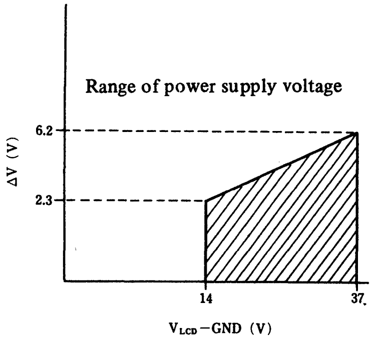
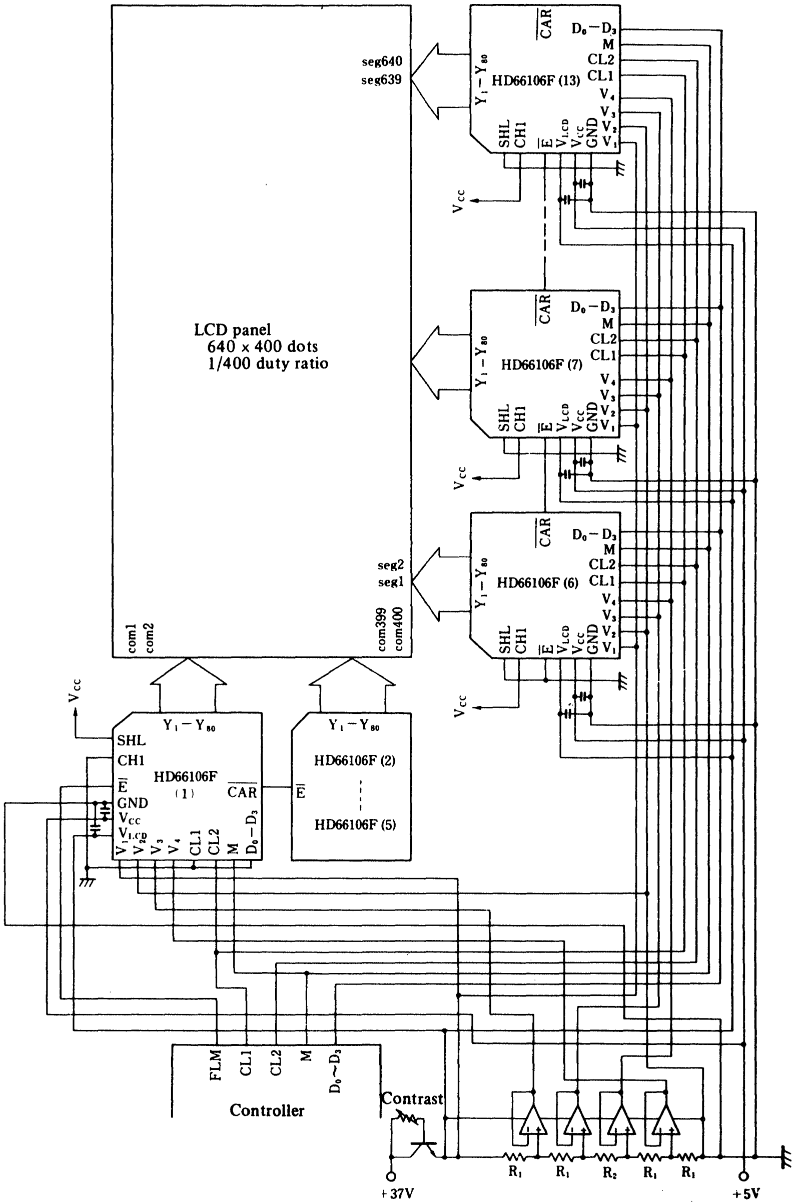


Figure 7. Power Supply Voltage V_{LCD}-GND and ΔV

Application Example

Application Diagram

Figure 8 shows an example of an LCD panel of 640 x 400 dots driven by HD66106Fs.



Notes: 1. R_1 and R_2 depend on the LCD panel in use. When using an LCD panel with 1/20 bias, $R_1/(4R_1 + R_2)$ should be 1/20. For example, R_1 -3 kΩ and R_2 -48 kΩ.

2. Use bypass capacitors to stabilize power supply when designing a board. It is desirable to use two capacitors with some 0.1 μF per LSI, putting one between V_{LCD} and GND, and the other between V_{CC} and GND.

Figure 8. Application Example

Timing waveform example

Figures 9 and 10 show the timing waveforms of the application example shown in figure 8.

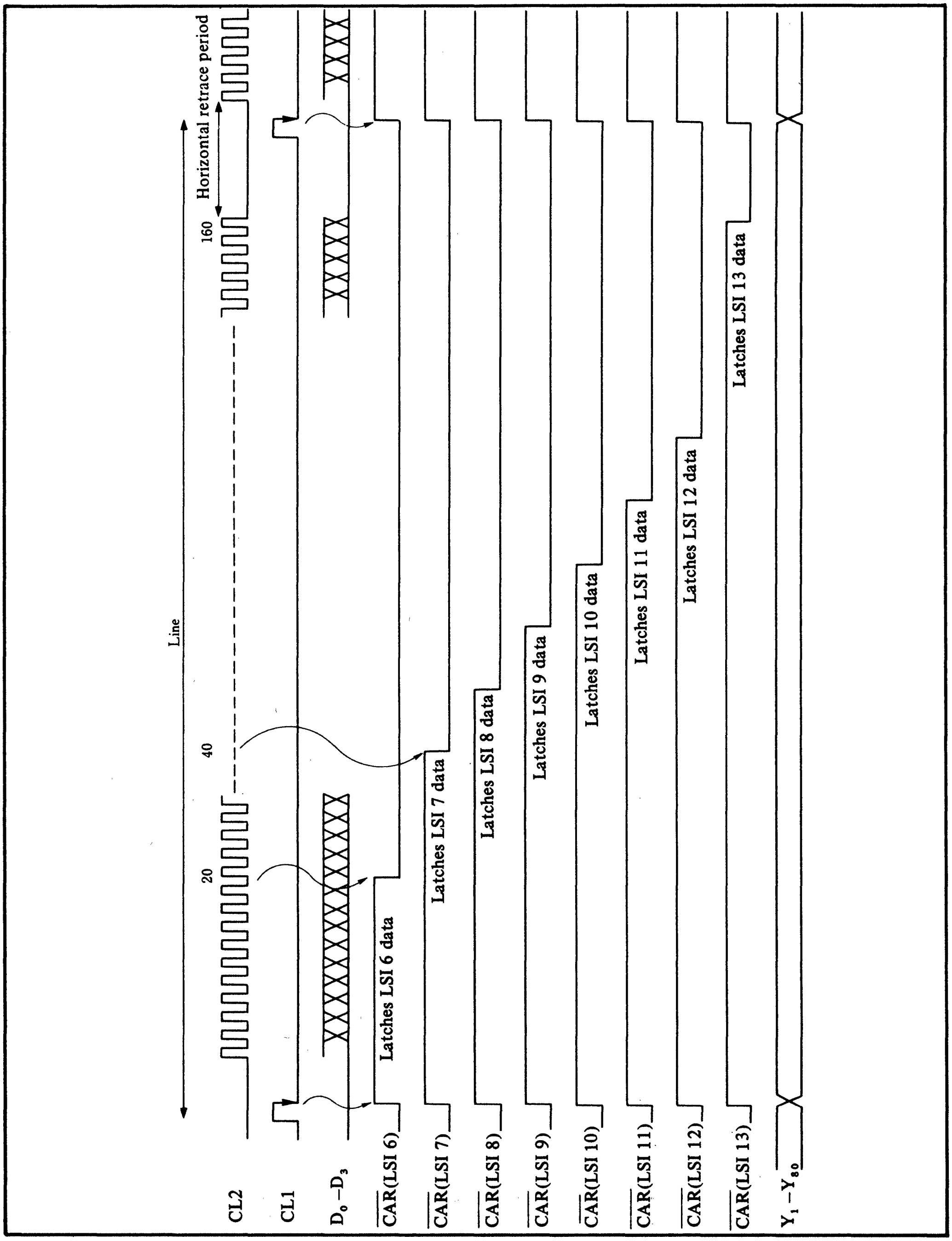


Figure 9. Timing Waveform for Column Drivers (LSI 6-LSI 13)

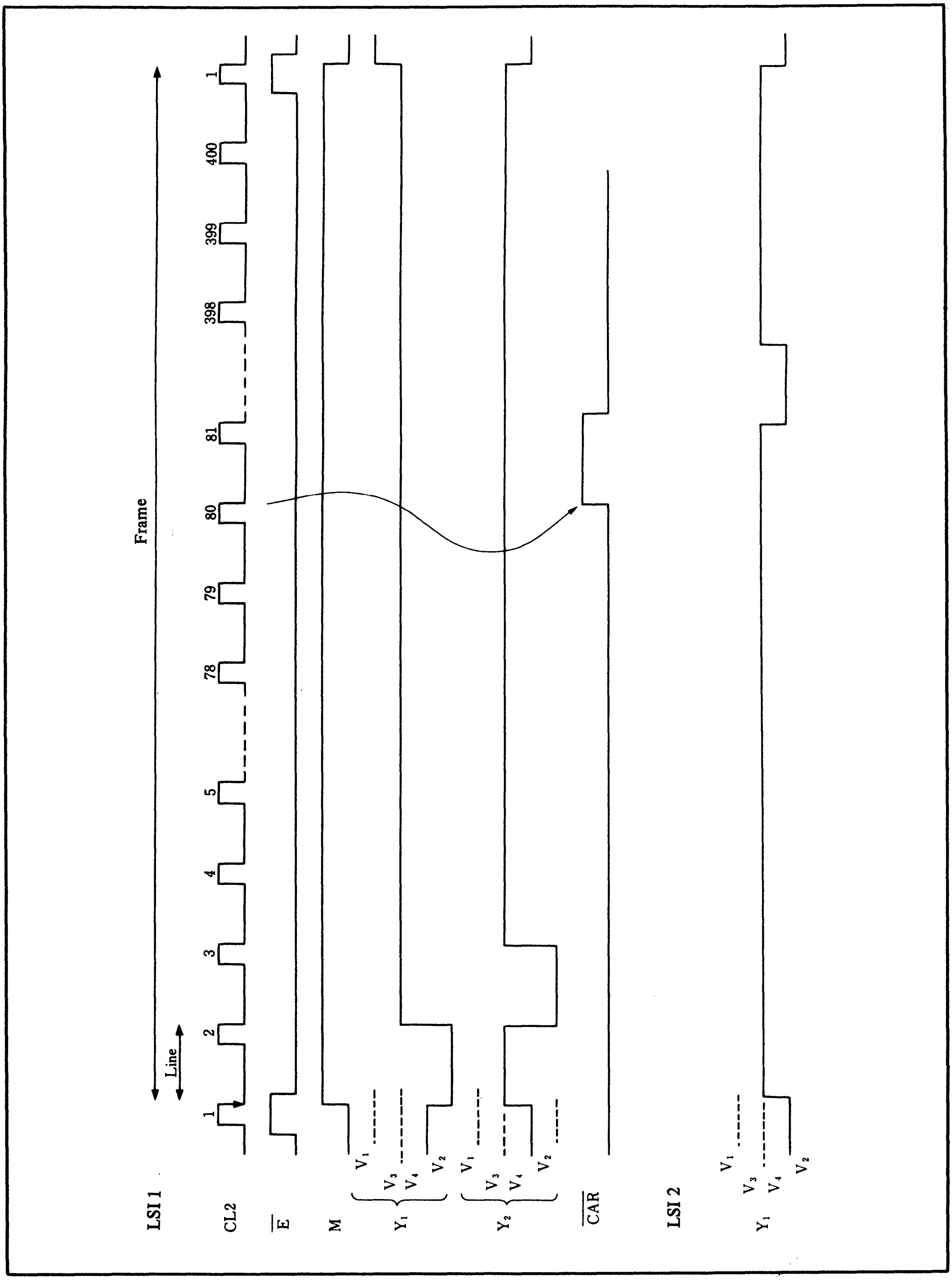


Figure 10. Timing Waveform for Row Drivers (LSI 1-LSI 5)

Absolute Maximum Ratings

Item		Symbol	Rating	Unit	Notes
Supply Voltage	Logic circuits	V_{CC}	–0.3 to +7.0	V	1
	LCD drive circuits	V_{LCD}	–0.3 to +38	V	1
Input voltage (Logic)		V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage (LCD drive)		V_{T2}	–0.3 to V_{LCD} + 0.3	V	1, 3
Operation temperature		T_{opr}	–20 to +75	°C	
Storage temperature		T_{stg}	–55 to +125	°C	

Notes:
1. Reference point is GND (= 0 V).
2. Applies to the input pins for logic circuits.
3. Applies to the input pins for LCD drive circuits.
4. Using an LSI beyond its maximum rating may result in its permanent destruction. LSIs should usually be used under electrical characteristics for normal operations. Exceeding any of these limits may adversely affect reliability.

Electrical Characteristics

DC Characteristics (V_{CC} = 5 V ± 10 %, V_{LCD} = 14 V to 37 V, Ta = –20°C to 75°C unless otherwise noted)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	CL1, CL2, M, SHL, D_0–D_3, $\overline{E}$, CH1	0.8xVcc	–	Vcc	V		
Input low voltage	V_{IL}		0	–	0.2xV_{CC}	V		
Output high voltage	V_{OH}	$\overline{CAR}$	V_{CC}–0.4	–	–	V	I_{OH}=–0.4 mA	
Output low voltage	V_{OL}		–	–	0.4	V	I_{OL}=0.4 mA	
Vi-Yj on resistance	R_{ON}	Y_1–Y_{80}, V_1–V_4	–	–	3.0	kΩ	I_{ON}=100 μA	4
Input leakage current (1)	I_{IL1}	CL1, CL2, M, SHL, D_0–D_3, $\overline{E}$, CH1	–5.0	–	5.0	μA	V_{IN}=V_{CC} to GND	
Input leakage current (2)	I_{IL2}	V_1–V_4	–50.0	–	50.0	μA	V_{IN}=V_{LCD} to GND	
Current consumption (1)	I_{CC1}		–	–	3.0	mA	f_{CL2}=6 MHz,	
(2)	I_{LCD1}		–	–	0.5	mA	f_{CL1}=28 kHz	1
(3)	I_{ST}		–	–	0.2	mA	At the standby state f_{CL2}=6 MHz, f_{CL1}=28 kHz	2
(4)	I_{CC2}		–	–	0.2	mA	f_{CL1}=28 kHz,	1
(5)	I_{LCD2}		–	–	0.1	mA	f_m=35 Hz	3

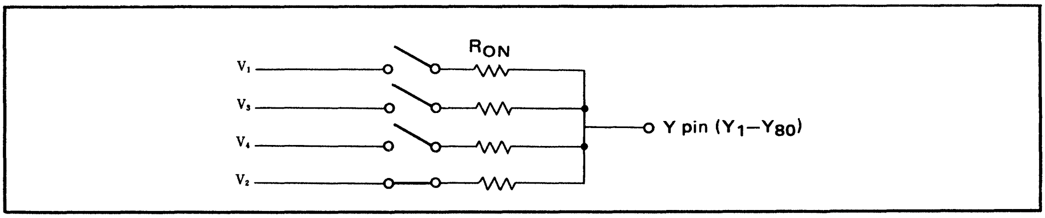
Notes:

1. Input and output current is excluded. When the input is at the intermediate level in CMOS, excessive current flows from the power supply through the input circuit. V_{IH} and V_{IL} must be fixed at V_{CC} and GND respectively to avoid it.
2. Applies when the LSI is used as a column driver.
3. Applies when the LSI is used as a row driver.
4. Indicates the resistance between Y pin and V pin (one of V_1, V_2, V_3, and V_4) when it supplies load current to one of Y_1–Y_{80} pins.

   Conditions: V_{LCD}–GND=37 V

   V_1, V_3=V_{LCD}–2/20 (V_{LCD}–GND)

   V_2, V_4=GND+2/20 (V_{LCD}–GND)



AC Characteristics (V_{CC} = 5 V ± 10 %, V_{LCD} = 14 V to 37 V, Ta = –20°C to +75°C unless otherwise noted)

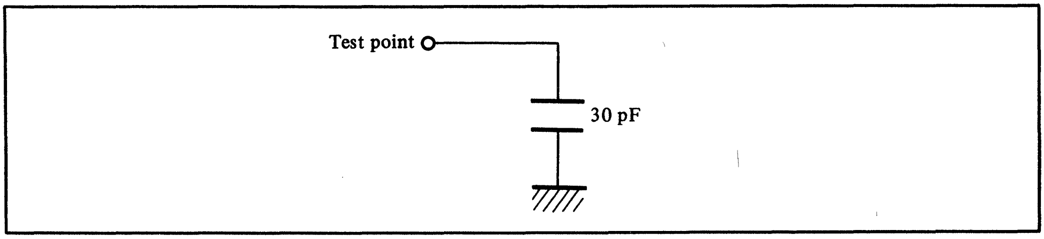
Column Driver

Item	Symbol	Pin	Min	Typ	Max	Unit	Notes
Clock cycle time	t_{cyc}	CL2	166	–	–	ns	
Clock high level width	t_{CWH}	CL2	50	–	–	ns	
Clock low level width	t_{CWL}	CL2	50	–	–	ns	
Clock setup time	t_{SCL}	CL2	200	–	–	ns	
Clock hold time	t_{HCL}	CL2	200	–	–	ns	
Clock rise/fall time	t_{ct}	CL1, CL2	–	–	30	ns	
Data setup time	t_{DSU}	D_0–D_3	30	–	–	ns	
Data hold time	t_{DH}	D_0–D_3	30	–	–	ns	
$\overline{E}$ setup time	t_{ESU}	$\overline{E}$	50	–	–	ns	
Output delay time	t_{DCAR}	$\overline{CAR}$	–	–	80	ns	1
M phase difference	t_{CM}	M, CL1	–	–	300	ns	

Row Driver

Item	Symbol	Pin	Min	Typ	Max	Unit	Notes
Clock low level width	t_{WL1}	CL2	5	–	–	µs	
Clock high level width	t_{WH1}	CL2	125	–	–	ns	
Data setup time	t_{DS}	$\overline{E}$	100	–	–	ns	
Data hold time	t_{DH}	$\overline{E}$	30	–	–	ns	
Data output delay time	t_{DD}	$\overline{CAR}$	–	–	3	µs	1
Data output hold time	t_{DHW}	$\overline{CAR}$	30	–	–	ns	1
Clock rise/fall time	t_{ct}	CL2	–	–	30	ns	

Note: 1. Values when the following load circuit is connected:



Column Driver

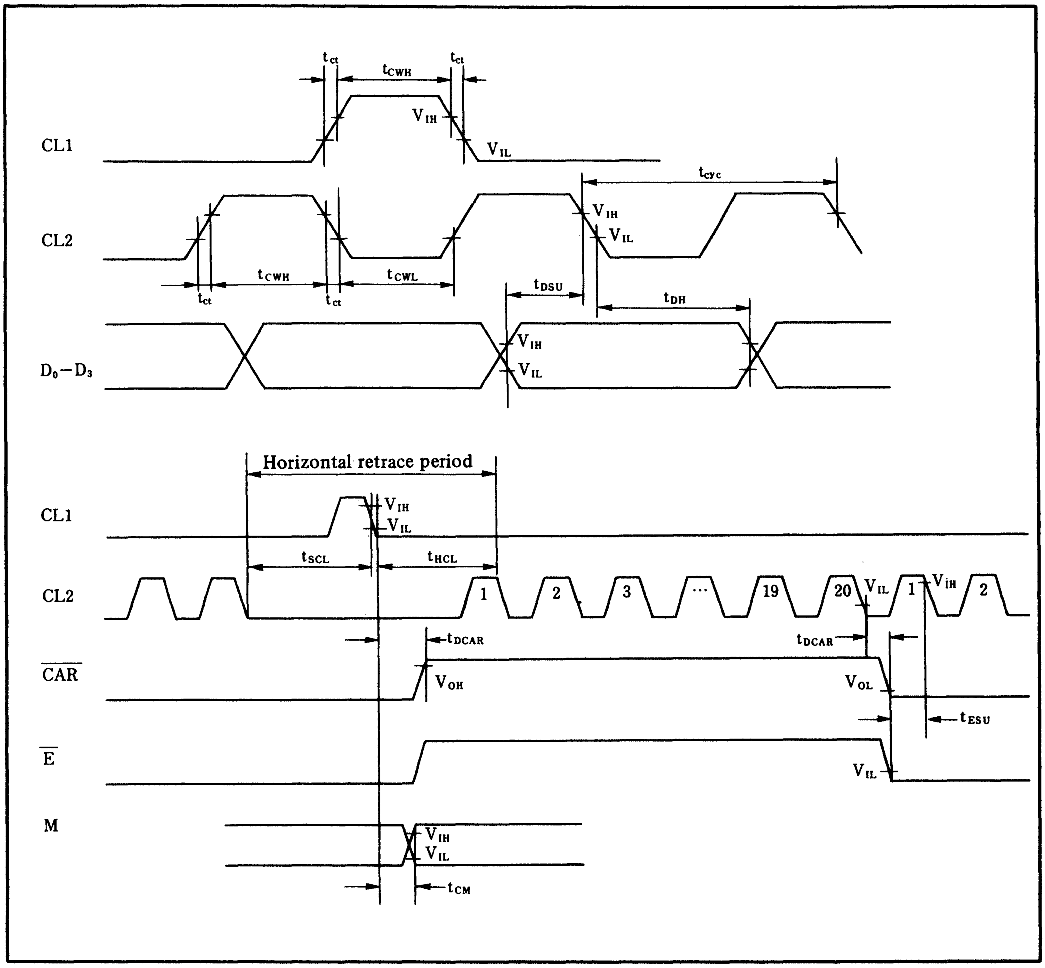


Figure 11. Controller Interface of Column Driver

Row Driver

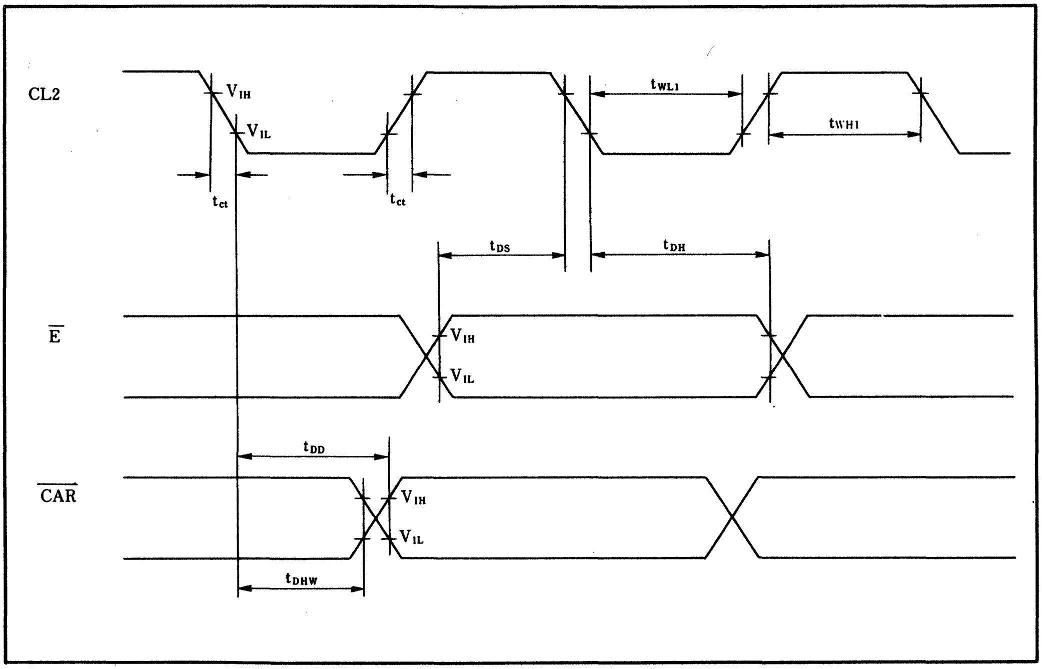


Figure 12. Controller Interface of Row Driver

HD66107T

(LCD Driver for High Voltage)

Description

The HD66107T is a multi-output, high duty ratio LCD driver used for large capacity dot matrix LCD panels. It consists of 160 LCD drive circuits with a display duty ratio up to 1/480: the seven HD66107Ts can drive a 640 × 480 dots LCD panel. Moreover, the LCD driver enables interfaces with various LCD controllers due to a built-in automatic generator of chip enable signals. Use of the HD66107T can help reduce the cost of an LCD-panel configuration, since it reduces the number of LCD drivers, compared with use of the HD61104 and HD61105.

Features

- Column and row driver
- 160 LCD drive circuits
- Multiplexing duty ratio :1/100 to 1/480
- 4-bit and 8-bit parallel data transfer
- Internal automatic chip enable signal generatator
- Internal standby mode
- Recommended LCD controller LSIs:
  HD63645, HD64645, and HD64646 (LCTC), HD66840 (LVIC)
- Power supply voltage
  internal logic : +5 V ± 10%
  LCD drive circuit : 14.0 to 37.0 V
- Operation frequency: 8.0 MHz (max.)
- CMOS Process
- 192-pin TAB (Tape Automated Bonding) package

Pin Description

Power Supply

V_{CC}, GND: V_{CC} supplies power to the internal logic circuits. GND is the logic and drive ground.

V_{LCD},: V_{LCD} supplies power to the LCD drive circuit.

Table 1. Pin Function

Symbol	Pin No.	Pin name	Input/output
V_{CC}	167	V_{CC}	
GND	161, 186, 187	Ground	
V_{LCD}	166, 192	V_{LCD}	
V1L, R	191, 165	V1L, R	
V2L, R	188, 162	V2L, R	
V3L, R	190, 164	V3L, R	
V4L, R	189, 163	V4L, R	
CL1	183	Clock 1	Input
CL2	184	Clock 2	Input
M	182	M	Input
D_0-D_7	174-181	DATA0-DATA7	Input
SHL	172	Shift left	Input
CH2	171	Channel 2	Input
BS	173	Bus Select	Input
TEST	185	TEST	Input
Y1-Y160	1-160	Y1-Y160	Output
SHL	172	Shift left	Input
$\overline{E}$	169	Enable	Input
$\overline{CAR}$	168	Carry	Onput
CH1	170	Channel 1	Input

V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L}, V_{4R}: V_1 to V_4 supply power for driving an LCD (figure 1).

Control Signal

CL1: The LSI latches data at the negative edge of CL1 when the LSI is used as a column driver. Fix to GND when the LSI is used as a row driver.

CL2: The LSI latches display data at the negative edge of CL2 when the LSI is used as a column driver, and shifts line select data at the negative edge when it is used as a row driver.

M: M changes LCD drive outputs to AC.

D_0-D_7: D_0-D_7 input display data for the column driver (table 2).

SHL: SHL controls the shift direction of display data and line select data (figure 2, table 3).

$\overline{E}$: $\overline{E}$ inputs the enable signal when the LSI is used as a column driver (CH1 = V_{CC}).
The LSI is disabled when $\overline{E}$ is high and enabled when low. $\overline{E}$ inputs scan data when the LSI is used as a row driver (CH1 = GND). When HD66107Ts are connected in cascade, $\overline{E}$ connects with $\overline{CAR}$ of the preceding LSI.

$\overline{CAR}$: outputs the enable signal when the LSI is used as a column driver (CH1 = V_{CC}).

Table 2. Relation between Display data and LCD state

Display Data	LCD Output	LCD
1 (=high level)	V1L, R/V2L, R	On
0 (=low level)	Nonselected level	Off

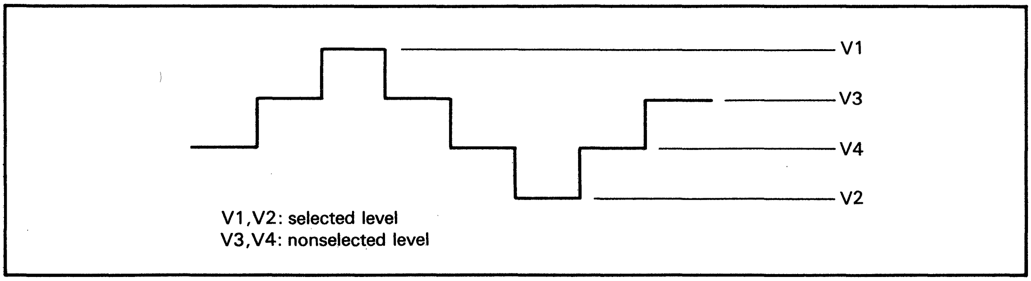


Figure 1. Power Supply for Driving an LCD

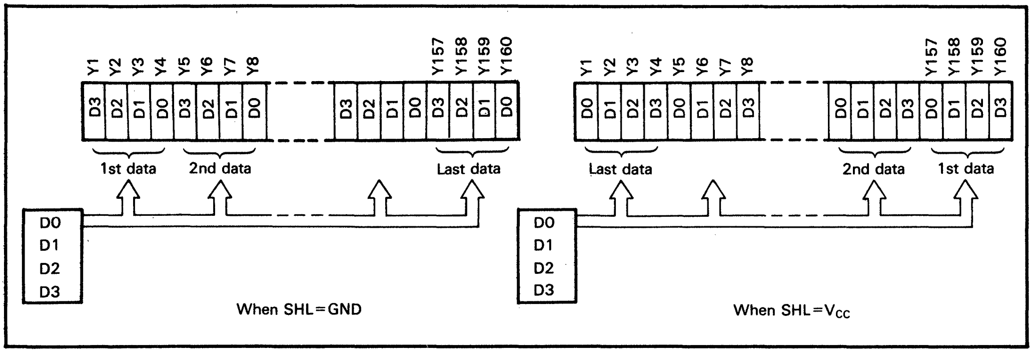


Figure 2. Relation between SHL and Data Output

$\overline{\mathrm{CAR}}$ outputs acan data when the LSI is used as a row driver (CH1 = GND). When HD66107Ts. are connected in cascade, $\overline{\mathrm{CAR}}$ connects with $\overline{\mathrm{E}}$ of the next LSI.

CH1: CH1 selects the driver function. The chip devices are columns when CH1 = V_{CC}, and commons when CH1 = GND.

CH2: CH2 selects the number of output data bits.

BS: BS selects the number of input data bits. When BS = V_{CC}, the chip latches 8-bits data. When BS = GND, the chip latches 4-bits data via D_0 to D_3. Fix D_4 through D_7 to GND.

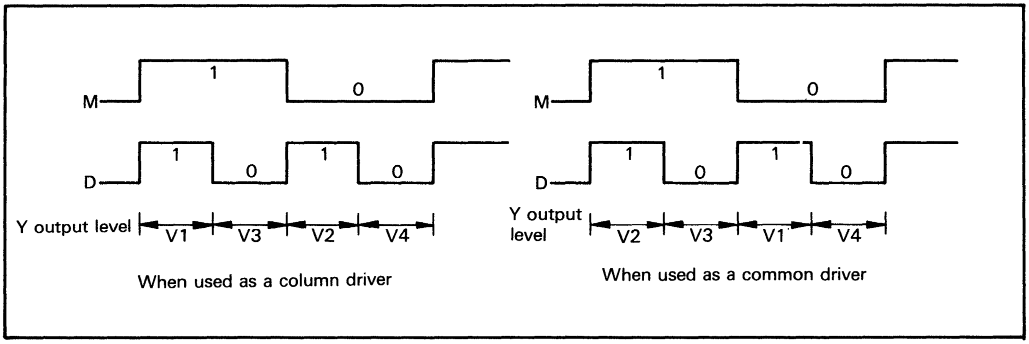
TEST: Used for testing; fixed to GND, Other wise.

LCD drive interface

Y1-Y160: Each Y outputs one of the four voltage levels-V1, V2, V3, V4-according to the combination of M and display data (figure 3).

Table 3. Relation between SHL and Scan Direction of Selected Line (When LSI is Used as Common Driver)

SHL	Shift Direction of Shift Register	Scan Direction of Selected Line
V_{CC}	E→ 1→ 2→ 3→ 4--------→160	Y1→ Y2→ Y3→ Y4--------→Y160
GND	E→ 160→ 79→ 78→ 77--------→1	Y160→ Y79→ Y77→ Y76--------→160

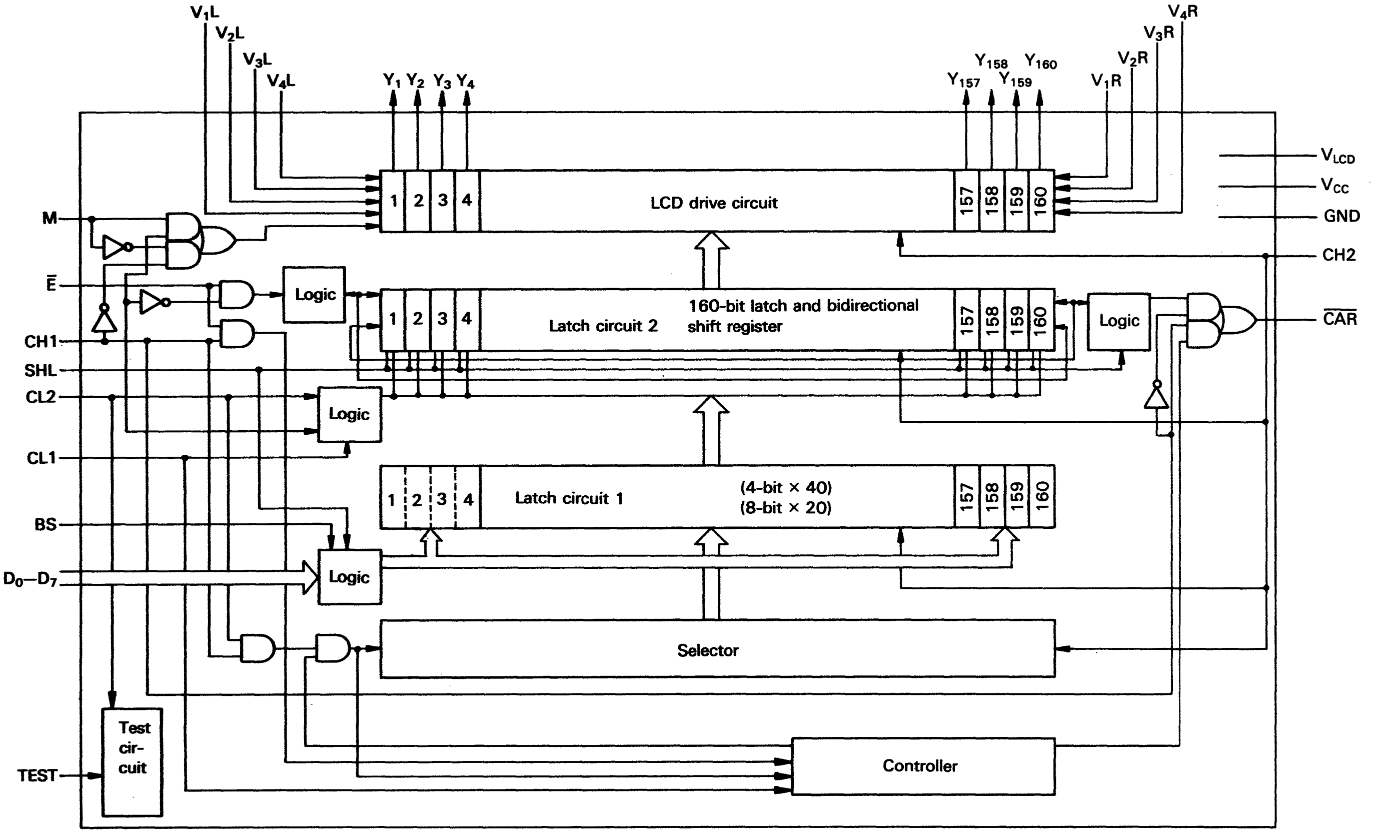


When used as a column driver

When used as a common driver

Figure 3. Selection of LCD Driver Output Level

Block Diagram



Function

LCD drive circuits

The LCD drive circuits generate four levels of voltages-V_1, V_2, V_3, and V_4-for driving an LCD. They select and transfer one of the four levels to the output circuit according to the combination of M and the data in the latch circuit 2.

Latch circuit 2

This circuit is used as a 160-bit latch circuit during column driving. Latch circuit 2 latches data input from latch circuit 1 at the falling edge of CL1 and outputs latched data to the drive circuits.

In the case of row driving latch circuit 2 is used as a 160-bit bidirectional shift register. Data input from $\overline{E}$ is shifted at the falling edge of CL2. When $SHL = V_{CC}$, data is shifted in input order from bit 1 to bit 160 of the shift register. When SHL = GND, data is shifted from bit 160 to bit 1 of the reister. Moreover, this latch circuit can be used as an 80-bit shift register. In this case, Y41 through Y120 are enabled, while the other bits remain unchanged.

Latch circuit 1

This circuit consists of twenty 8-bit parallel data latch circuits. It latches data D_0 through D_7 at the falling edge of CL2 during column driving. The selector signals specify which 8-bit circuit latches data. Moreover, this circuit can be used as forty 4-bit parallel data latch circuits by switching BS, in which case the circuit latches data D_0 through D_3. Moreover, this latch circuit can be used as an 80-bit shift register. In this case Y41 through Y120 are enabled, while the other bits remain unchanged.

Selector

The selector consists of a 6-bit up and down counter and a decoder. During column driving it generates a latch signal for latch circuit 1, incrementing the counter at the falling edge of CL2.

Controller

This controller is enabled during column driving. It provides a power-down function which detects completion of data latch and stops LSI operations.
Moreover, the controller automatically generates a chip enable signal ($\overline{CAR}$) which starts next-stage data latching.

Test circuit

This circuit divides the external clock and generates test signals.

Fundamental Operations

Column driving (1)

CH2 = GND (160-bit data output mode)
BS = Vcc (8-bit data latch mode)

The HD66107T starts data latch when $\overline{E}$ is at low level. In this case 8-bit parallel data is latched at the falling edge of CL2. When 160-bit data latch is completed, the HD66107T automatically stops and enters standby mode and $\overline{CAR}$ is goes to low level. If $\overline{CAR}$ is connected with $\overline{E}$ of the next-stage LSI, this next-stage LSI is activated when $\overline{CAR}$ of the previous LSI goes low.

Data is output at the falling edge of CL1. When SHL = GND, data dl is output to pin Y1 and dl60 to Y160. On the other hand, when SHL = Vcc, data d160 is output to pin Y1 and d1 to Y160. The output level is selected from among V1- V4 according to the combination of display data and alternating signal M.

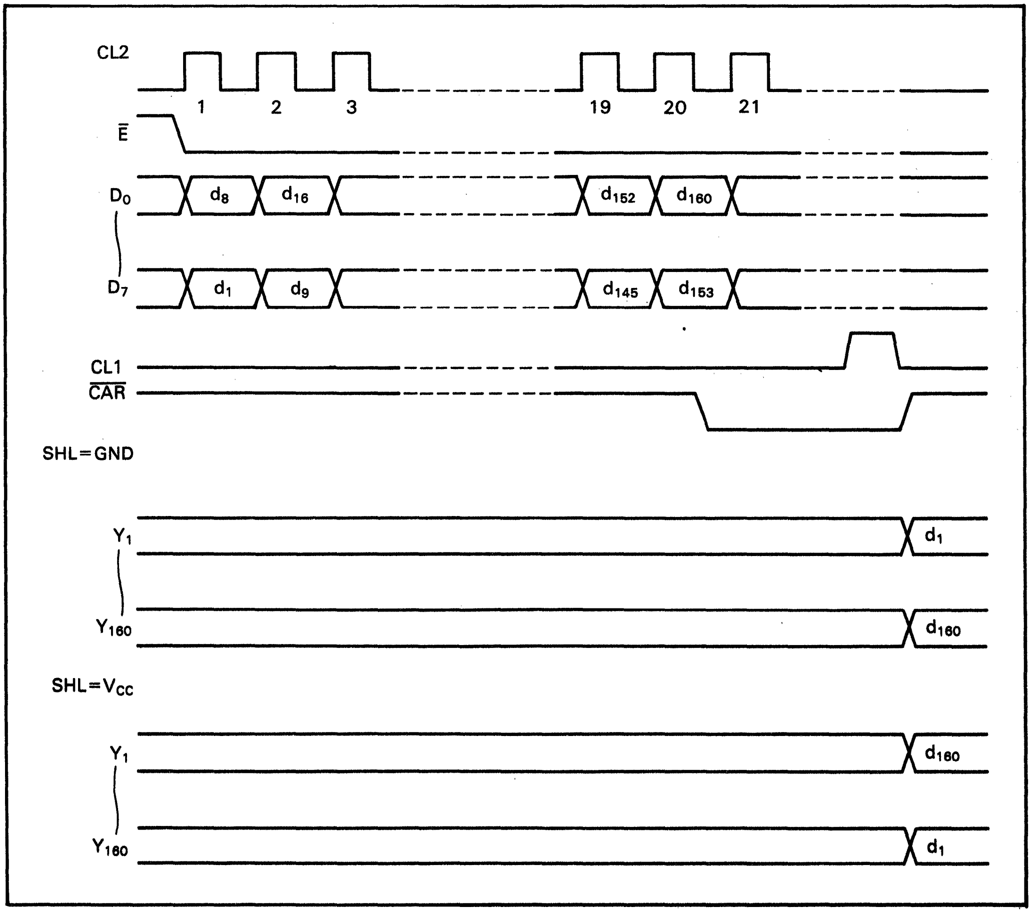


Figure 4. Column Driver Timing Chart (1)

Column driving (2)

CH2 = GND (160-bit data output mode)
BS = GND (4-bit data latch mode)

4-bit display data (D_0-D_3) is latched at the falling edge of CL2. Other operations are performed in the same way as described in "Column driving (1)".

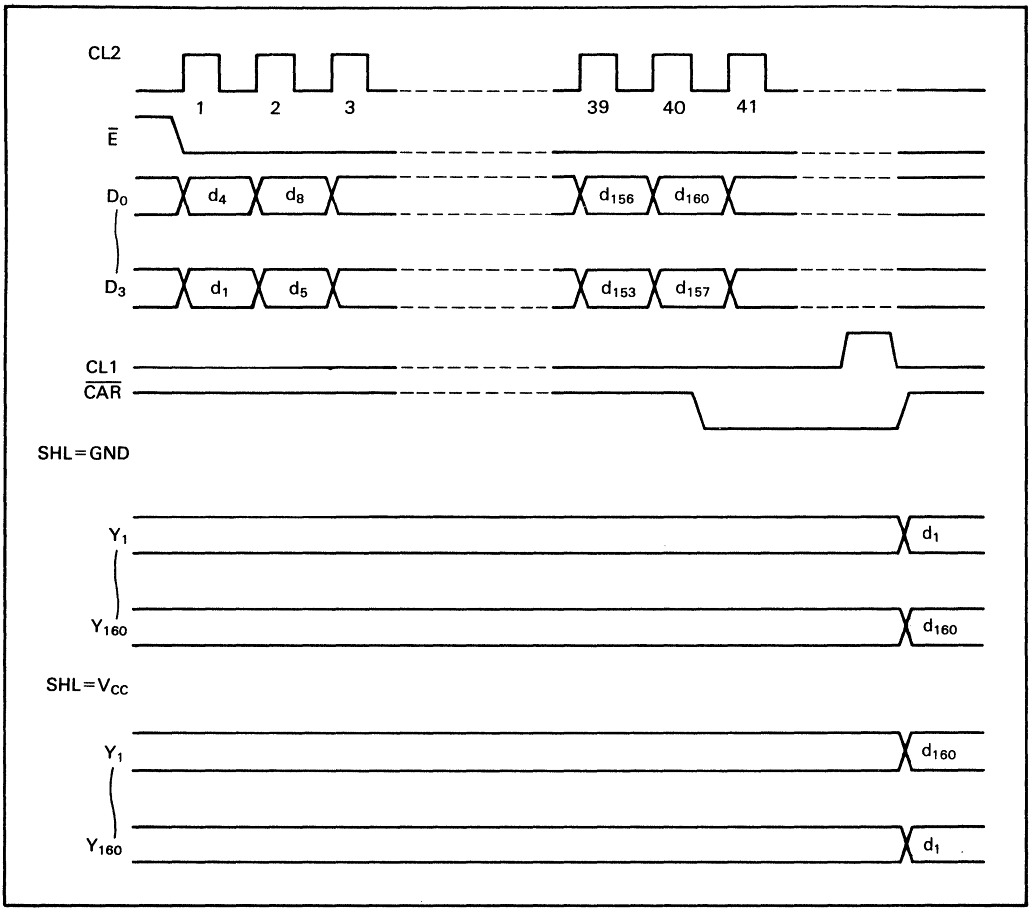


Figure 5. Column Driver Timing Chart (2)

Column driving (3)

CH2 = V_{CC} (80-bit data output mode)
BS = V_{CC} (8-bit data latch mode)

When CH2 is high (V_{cc}), the HD66107T can be used as an 80-bit column driver. In this case, Y41 through Y120 are enabled, the states of Y1 through Y40 and Y121 through Y160 remain unchanged.

When SHL = GND, data d1 is output to pin Y41 and d80 is output to Y120.
Conversely, when SHL = V_{cc}, data d80 is output to Y41 and d1 is output to Y120.

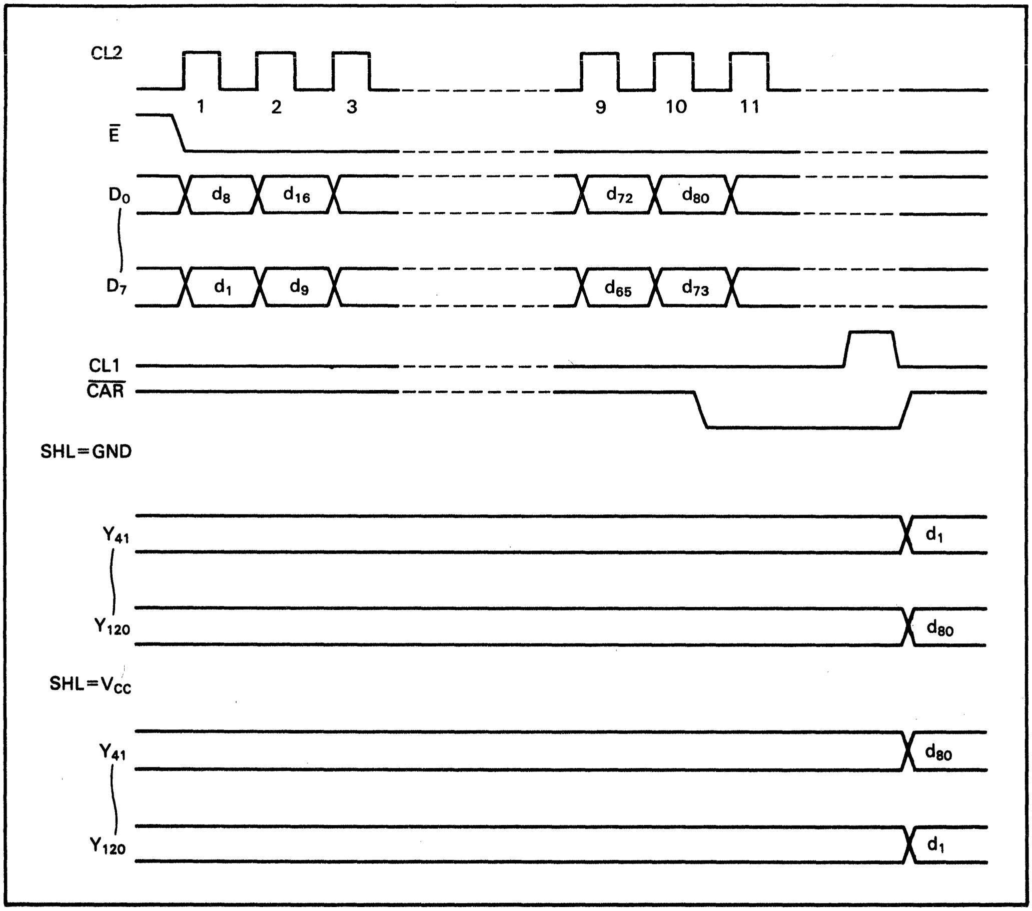


Figure 6. Column Driver Timing Chart (3)

Column driving (4)

CH2 = V_{cc} (80-bit data output mode)
BS = GND (4-bit data latch mode)

When CH2=V_{cc} and BS=GND, 4-bit parallel data is latched, while 80-bit data is output. The output of latched data is performed in described at "Column driving (3)".

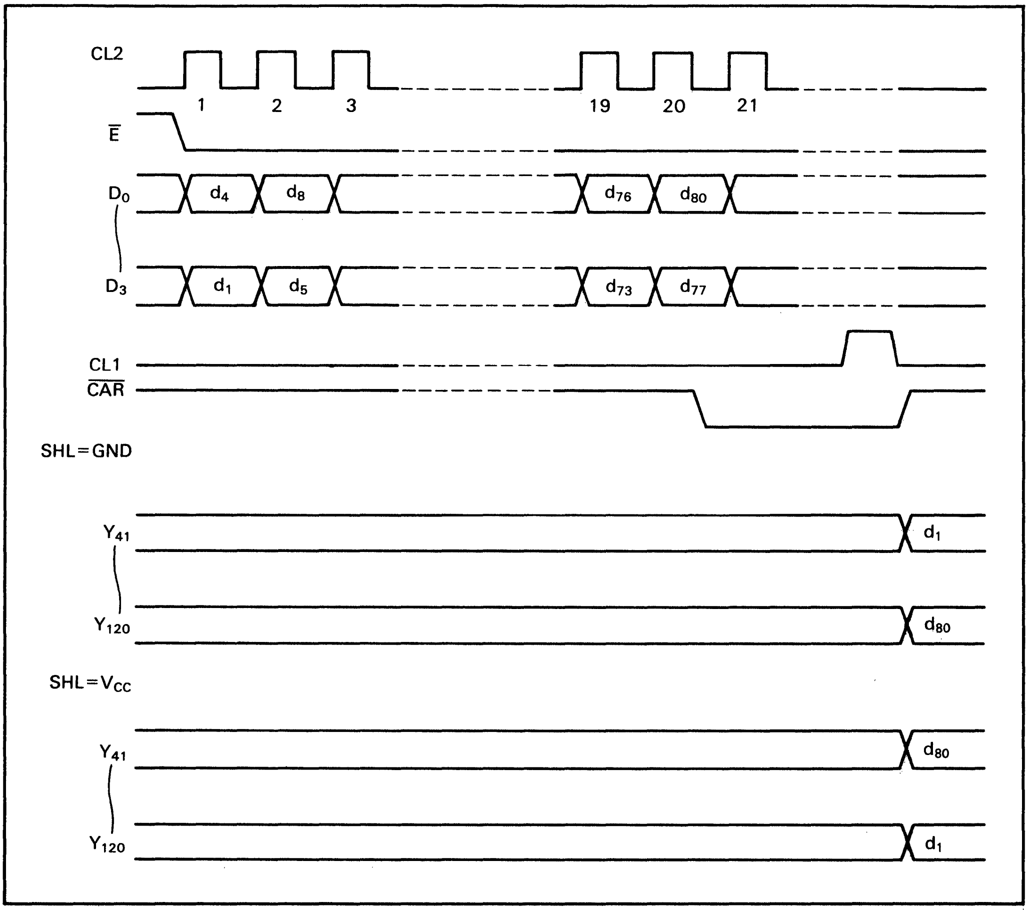


Figure 7. Column Driver Timing Chart (4)

Common driving (1)

CH2 = GND (160-bit data output mode)

The HD66107T shifts line scan data input through $\overline{E}$ at the falling edge of CL2.

When SHL=V_{CC}, 160-bit data is shifted from Y1 to Y160, whereas when SHL=GND, data is shifted from Y160 to Y1. In both cases the HD66107T outputs the data delayed for 160 bits by the shift register through $\overline{CAR}$, becoming line scan data for the next IC driver.

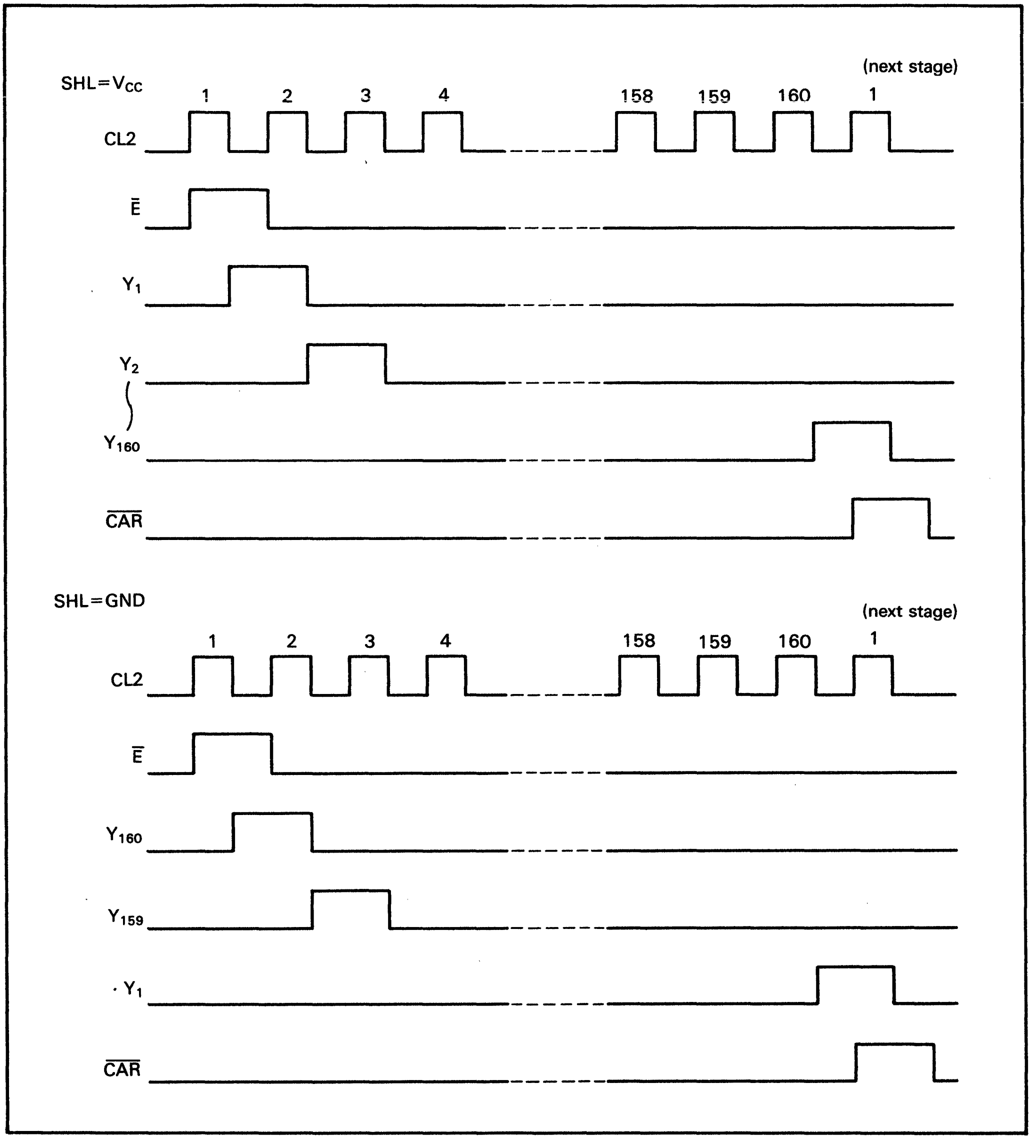


Figure 8. Common Driver Timing Chart (1)

Common driving (2)

CH2 = V_{CC} (80-bit data output mode)

When CH2 is high, the HD66107T can be used as an 80-bit row driver. In this case, Y41 to Y120 are enabled, while the other bits remain unchanged.

Line scan data input through $\overline{E}$ is shifted at the falling edge of CL2. When SHL = Vcc, data is shifted from Y41 to Y120. Conversely, when SHL = GND, data is shifted from Y120 to Y41. In both cases the HD66107T outputs the data delayed for 80 bits by the shift register through $\overline{CAR}$, becoming line scan data for the next LSI.

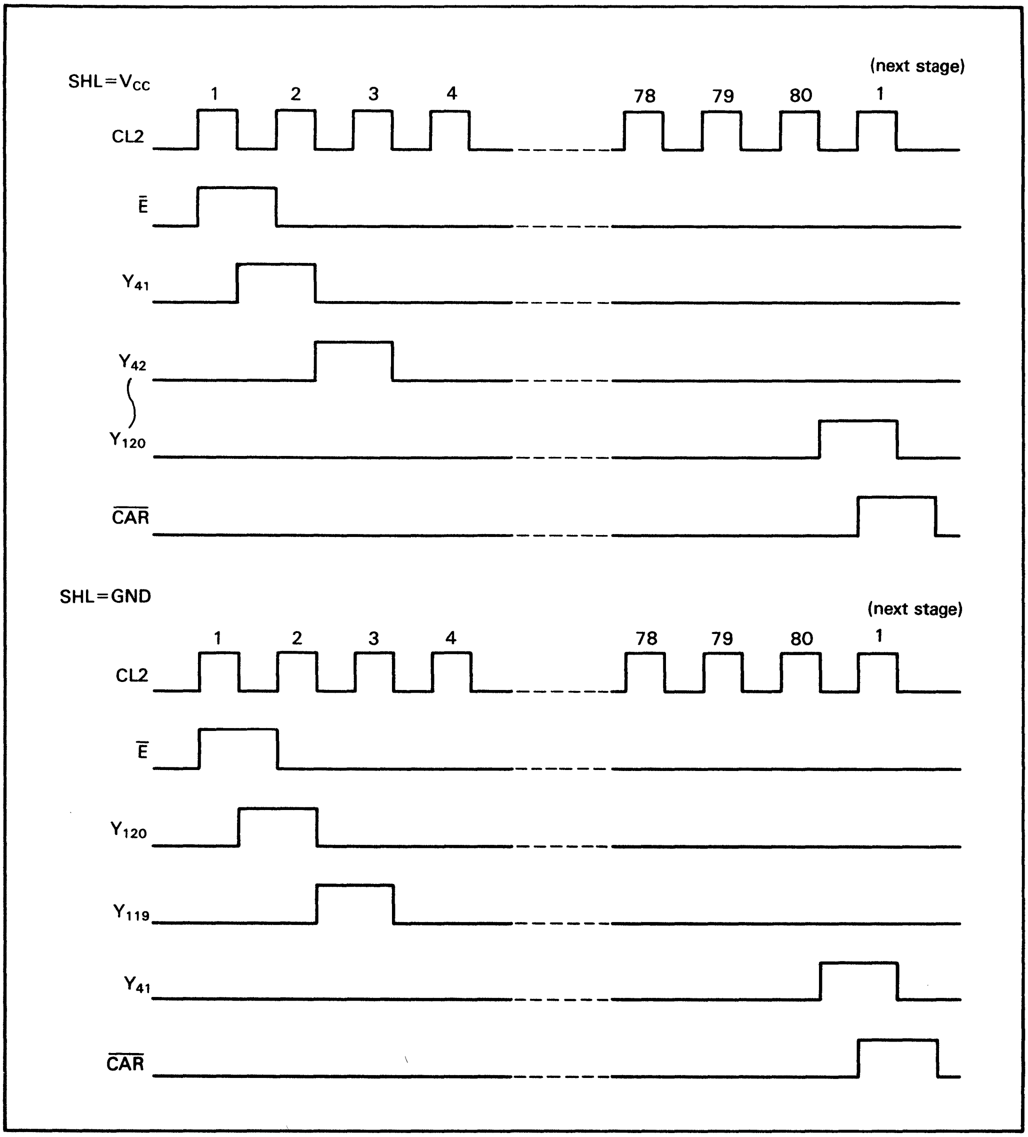


Figure 9. Common Driver Timing Chart (2)

LCD Power Supply

This section explains the range of power supply voltage for driving LCD. V_1 and V_3 voltages should be near V_{LDC}, and V_2 and V_4 should be near GND (figure 10). Each voltage must be within ΔV. ΔV determines the range within which R_{ON}, impedance of driver's output, is stable. Note that ΔV depends on power supply voltage V_{LCD}-GND (figure 11).

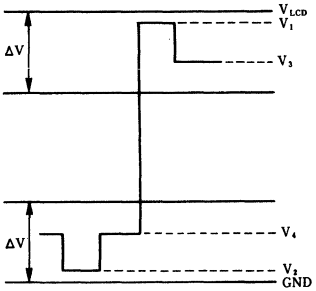


Figure 10. Driver's Output Waveform and Each Level of Voltage

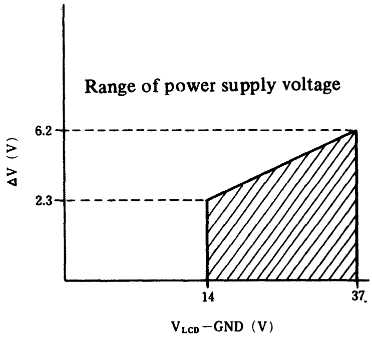
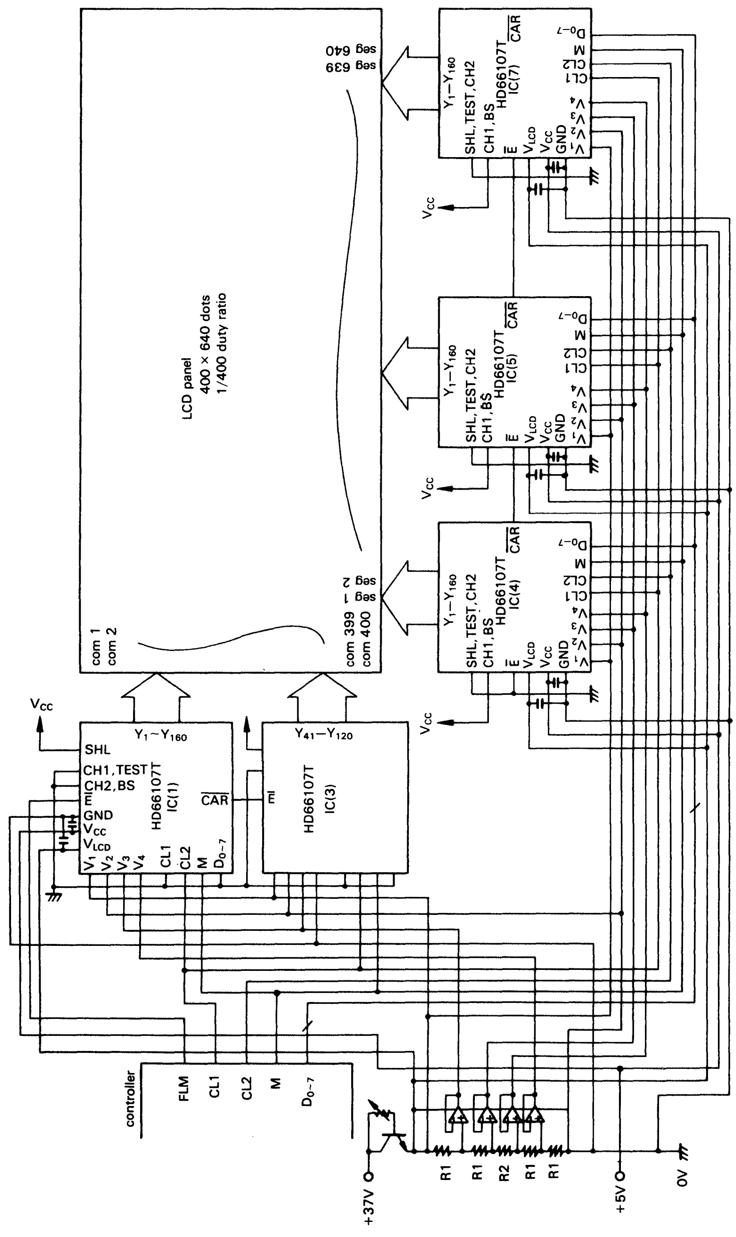


Figure 11. Power Supply Voltage V_{LCD}-GND and ΔV

Application

The following example shows a system configuration for driving a 640×400-dot LCD panel using the HD66107T.



Note 1: R1 and R2 are specified depending on the type of LCD panel. When using an LCD panel with 1/20 bias, R1/(4R1+R2) must be 1/20, i.e., R1 = 3 kΩ and R2 = 48 kΩ.

Note 2: When designihg a board, place capacitors close to each LSI in order to stabilize power supply. It is recommended to use two 0.1 μF capacitors per LSI; one is connected between V_{CC} and GND, and the other between V_{LCD} and GND.

Figure 12. Application Example

Example of Waveform

In column driving

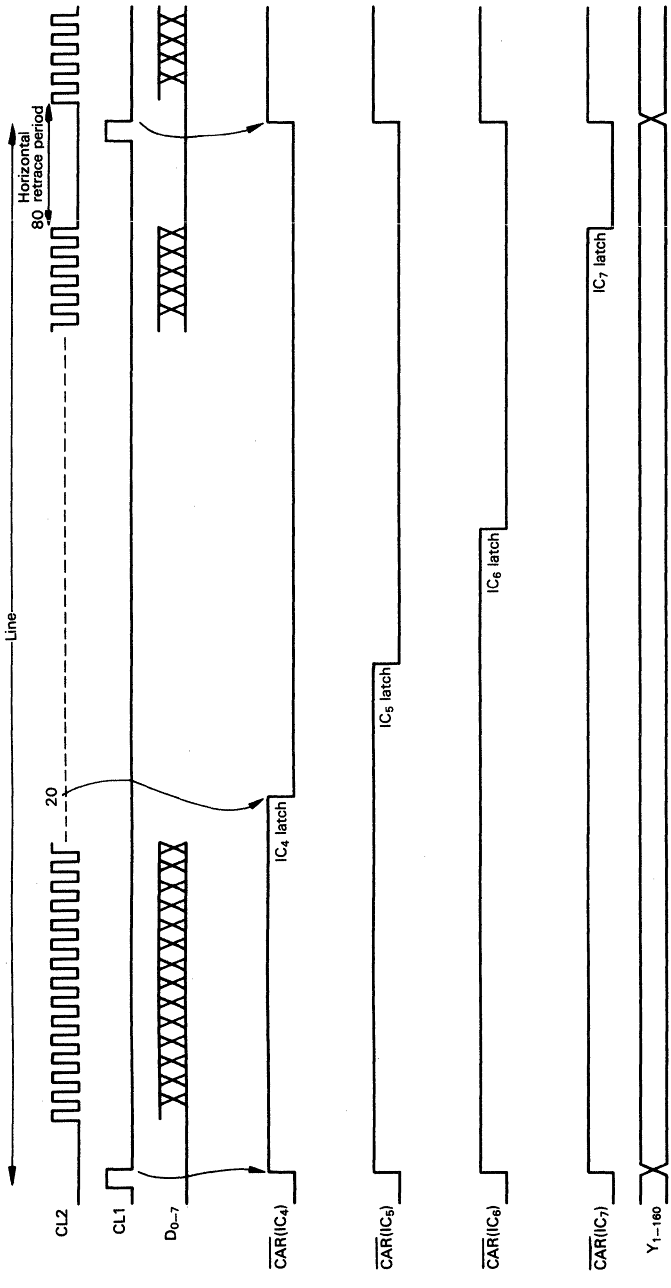
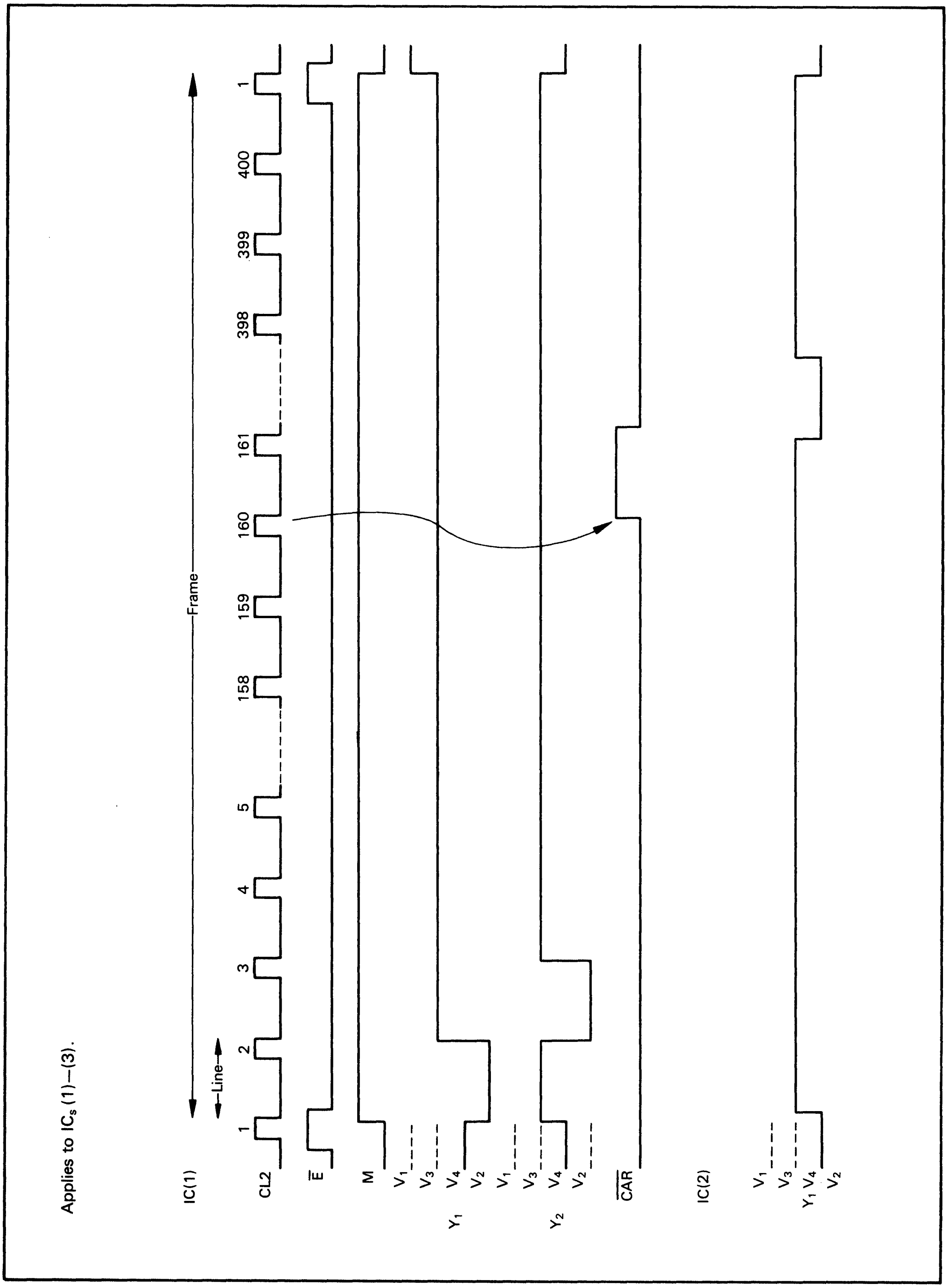


Figure 13. Column Driver Timing Chart (1)

In common driving



Applies to IC_s (1)–(3).

Figure 14. Common Driver Timing Chart

Absolute Maximum Rating

Item		Symbol	Rating	Unit	Note
Power supply voltage	Logic circuit	V_{CC}	−0.3− +7.0	V	1
	LCD drive circuit	V_{LCD}	−0.5− +38	V	1
Input voltage (1)		V_{T1}	−0.3−V_{CC}+0.3	V	1, 2
Input voltage (2)		V_{T2}	−0.3−V_{LCD}+0.3	V	1, 3
Operation temperature		T_{opr}	−20− +75	°C	
Storage temperature		T_{stg}	−55− +125	°C	

Note 1. Reference point is GND (= 0V.)
2. Applies to input pins for logic circuit.
3. Applies to input pins for LCD drive circuits.
4. If the LSI is used beyond absolute maximum ratings, it may be permanently damaged. It should always be used within the above electrical characteristics to prevent malfunction or degradation of the LSI's reliability.

Electrical Characteristics

DC Characteristics (V_{CC}=5V±10%, V_{LCD}=14 to 37V, Ta=−20 to 75°C)

Item	Symbol	Pins	Min.	Max.	Unit	Condition	Note
Input high voltage	V_{IH}	CL1, CL2, M SHL, BS, CH2, TEST, D_0-D_7, $\overline{E}$, CH1	0.8×V_{CC}	V_{CC}	V		
Input low voltage	V_{IL}		0	0.2×V_{CC}	V		
Output high voltage	V_{OH}	$\overline{CAR}$	V_{CC}−0.4	–	V	I_{OH}=−0.4mA	
Output low voltage	V_{OL}		–	0.4	V	I_{OL}=0.4mA	
Vi−Yj ON resistance	R_{ON}	Y1−Y160, V1−V4	–	3.0	kΩ	I_{ON}=150μA	
Input leak current (1)	I_{IL1}	CL1, CL2, M SHL, BS, CH2, TEST, D_0−D_7, $\overline{E}$, CH1	−5.0	5.0	μA	V_{IN}=V_{CC}−GND	
Input leak current (2)	I_{IL2}	V1−V4	−100	100	μA	V_{IN}=V_{LCD}−GND	
Power dissipation (1)	I_{CC1}		–	5.0	mA	f_{CL2}=8MHz	1
Power dissipation (2)	I_{LCD1}		–	2.0	mA	f_{CL1}=28kHz	2
Power dissipation (3)	I_{ST}		–	0.5	mA	In standy mode: f_{CL2}=8MHz, f_{CL1}=28kHz	 1 2
Power dissipation (4)	I_{CC2}		–	1.0	mA	f_{fcL1}=28kHz	1
Power dissipation (5)	I_{LCD2}		–	0.5	mA	fm=35Hz	3

Note 1. Input and output current is excluded. when an input is at the intermediate level is CMOS, the excessive current flows from the power supply though the input circuit. To avoid it, V_{IH} and V_{IL} must be fixed to V_{CC} and GND respectively.

2. Applies to column driving.
3. Applies to row driving.

AC Characteristics (Vcc=5V±10%, V_{LCD}=14 to 37V, Ta=−20 to 75°C)

In column driving

Item	Symbol	Pin name	Min.	Max.	Unit	Note
Clock cycle time	t_{cyc}	CL2	125	–	ns	
Clock high-level width	t_{CWH}	CL2	30	–	ns	
Clock low-level width	t_{CWL}	CL2	30	–	ns	
Clock setup time	t_{SCL}	CL2	200	–	ns	
Clock hold time	t_{HCL}	CL2	200	–	ns	
Clock rising/falling time	tct	CL1, CL2	–	30	ns	
Data setup time	t_{DSU}	D_0-D_7	30	–	ns	
Data hold time	t_{DH}	D_0-D_7	30	–	ns	
$\overline{E}$ setup time	t_{ESU}	$\overline{E}$	25	–	ns	
Output delay time	t_{DCAR}	$\overline{CAR}$	–	70	ns	1
M phase difference	t_{CM}	M, CL1	–	300	ns	

Note 1. Specified when connecting the load circuit shown to the right.

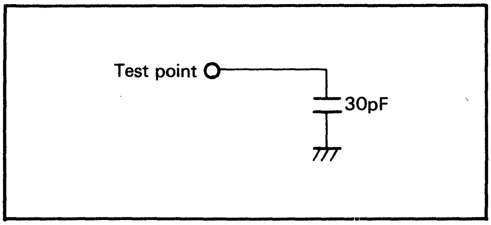


Figure 15. Test Circuit

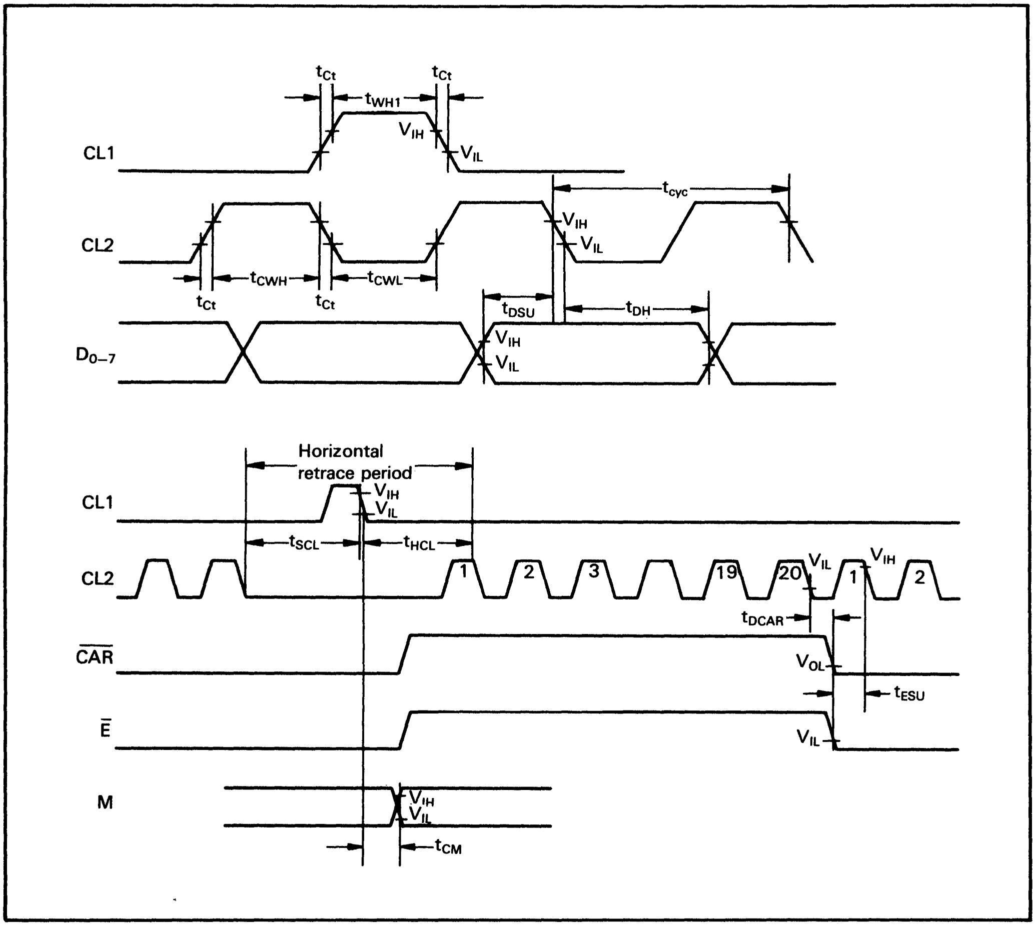


Figure 16. Controller Interface of column Driver

In common driving

Item	Symbol	Pin name	Min.	Max.	Unit	Note
Clock low-level width	t_{WL1}	CL2	5	–	μs	
Clock high-level width	t_{WH1}	CL2	60	–	ns	
Data setup time	t_{DS}	$\bar{E}$	100	–	ns	
Data hold time	t_{DH}	$\bar{E}$	30	–	ns	
Data output delay time	t_{DD}	$\overline{CAR}$	–	3	μs	1
Data output hold time	t_{DHW}	$\overline{CAR}$	30	–	ns	1
Clock rising/falling time	t_{Ct}	CL2	–	30	ns	

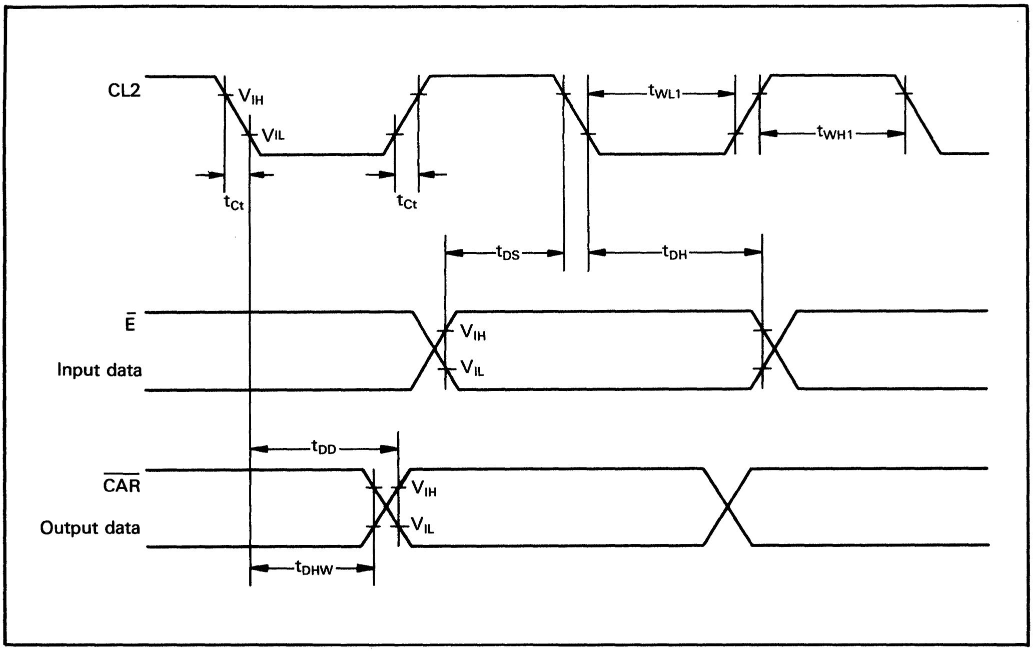


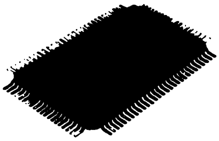
Figure 17. Controller Interface of common Driver

HD61105, HD61105A
(Dot Matrix Liquid Crystal Graphic Display Common Driver)

DESCRIPTION

The HD61105, HD61105A is a common signal driver for dot matrix liquid crystal graphic display systems. It provides 80 driver output lines and the impedance is low enough to drive a large screen.

As the HD61105, HD61105A is produced in a CMOS process, it fits for use in portable battery drive equipments utilizing the liquid crystal display's low power consumption.

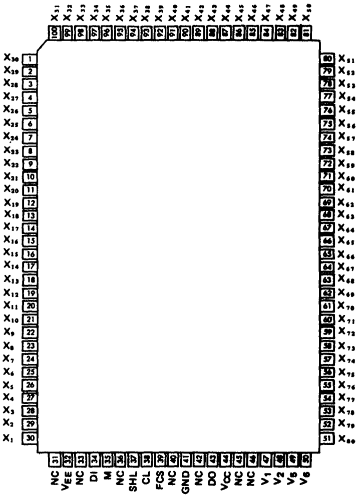


FP-100

■ FEATURES

- Dot matrix liquid crystal graphic display common driver with low impedance.
- Internal liquid crystal display driver circuit – 80 circuits
- Display duty ratio factor 1/64 ∿ 1/200
- Internal 80-bit shift register
- Power supply for logic circuit 5 ± 10%
- Power supply for LCD drive circuits;
  - 10 to 26V (HD61105)
  - 10 to 28V (HD61105A)
- CMOS process
- 100-pin plastic QFP (FP-100)

■ PIN ARRANGEMENT

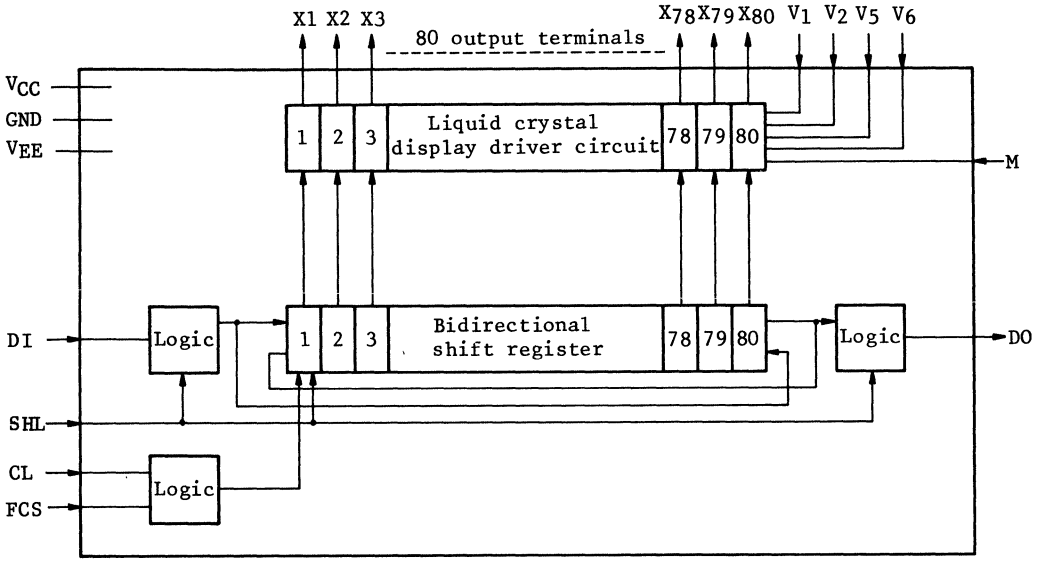


(Top View)

■ ORDERING INFORMATION

Type No.	LCD driving Level (V)	Package
HD61105	10 to 26	100 pin plastic QFP (FP-100)
HD61105A	10 to 28	

BLOCK DIAGRAM


X1 X2 X3
80 output terminals
X78 X79 X80 V1 V2 V5 V6
VCC
GND
VEE
1 2 3 Liquid crystal display driver circuit 78 79 80
M
DI
Logic
1 2 3 Bidirectional shift register 78 79 80
Logic
DO
SHL
CL
FCS
Logic

ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Value	Unit	Note
Supply voltage (1)		V_{CC}	-0.3 to +7.0	V	2
Supply voltage(2)	HD61105	V_{EE}	V_{CC} - 28.0 to V_{CC} + 0.3	V	5
	HD61105A		V_{CC} - 28.5 to V_{CC} + 0.3		
Terminal voltage (1)		V_{T1}	-0.3 to V_{CC} + 0.3	V	2, 3
Terminal voltage (2)		V_{T2}	V_{EE} - 0.3 to V_{CC} + 0.3	V	4, 5
Operating temperature		Topr	-20 to +75	°C	
Storage temperature		Tstg	-55 to +125	°C	

(Note 1) LSI's may be permanently destroyed if being used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the limits of electrical characteristics, because using beyond these conditions may cause malfunction and poor reliability.

(Note 2) All voltage values are referred to GND = 0V.

(Note 3) Applies to input terminals except V1, V2, V5 and V6.

(Note 4) Applies to V1, V2, V5 and V6.

(Note 5) $V_{CC} \geqq V1 \geqq V6 \geqq V5 \geqq V2 \geqq V_{EE}$ must be maintained.

ELECTRICAL CHARACTERISTICS

- DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, GND = 0V, V_{CC} - V_{EE} = 10 to 26V (HD61105), V_{CC} - V_{EE} = 10 to 28V (HD61105A), Ta = -20 to +75°C)

Test Item	Symbol	Test Condition	Specifications			Unit	Note
			Min.	Typ.	Max.		
Input "High" voltage	V_{IH}		0.7×V_{CC}	-	V_{CC}	V	1
Input "Low" voltage	V_{IL}		GND		0.3×V_{CC}	V	1
Output "High" voltage	V_{OH}	I_{OH}=-0.4mA	V_{CC}-0.4	-	-	V	2
Output "Low" voltage	V_{OL}	I_{OL}=0.4mA	-	-	0.4	V	2
Vi-Xj ON Resistance	R_{ON}	V_{CC}-V_{EE}=10V Load current ± 150μA	-	-	2.0	kΩ	5
Input Leakage Current	I_{IL1}	V_{IN}=0 to V_{CC}	-1.0		1.0	μA	3
Input Leakage Current	I_{IL2}	V_{IN}=V_{EE} to V_{CC}	-25		25	μA	4
Clock Frequency	fCL	Transfer clock CL	-	-	100	kHz	
Dissipation Current (1)	I_{GG1}	at 1/200 duty operation	-	-	200	μA	6
Dissipation Current (2)	I_{EE}	at 1/200 duty operation	-	-	100	μA	7

(Note 1) Applies to input terminals FCS, SHL, DI, M, and CL.

(Note 2) Applies to output terminal of DO.

(Note 3) Applies to the terminals NC, and the input terminals FCS, SHL, DI, M, and CL.

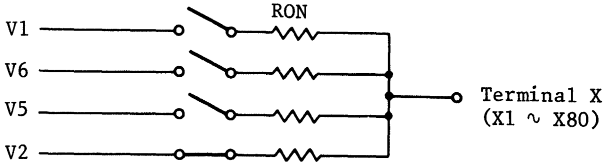
(Note 4) Applies to V1, V2, V5, and V6. No wire is to be connected to X1∿X80.

(Note 5) Resistance value between terminal X (one of X1 to X80) and terminal V (one of V1, V2, V5, and V6) when load current is applied to one of terminals X1 to X80. This value is specified under the following condition.

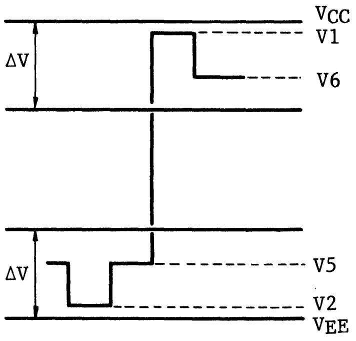
$V_{CC} - V_{EE} = 26V$

$V1, V6 = V_{CC} - 1/10\ (V_{CC} - V_{EE})$

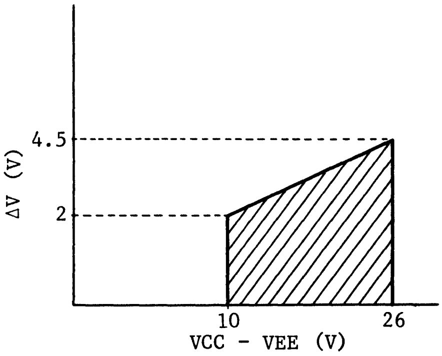
$V2, V5 = V_{EE} + 1/10\ (V_{CC} - V_{EE})$



Here is a description of the range of power supply voltage for liquid crystal display drive. Apply positive voltage to V1, and V6, and negative voltage to V2 and V5, within the ΔV range respectively. This range allows stable impedance on driver output (R_{ON}). Notice that ΔV depends on power supply voltage $V_{CC} - V_{EE}$.



Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive



Correlation between Power Supply Voltage $V_{CC}-V_{EE}$ and ΔV

(Note 6) The currents flowing through the GND terminal.

Specified when display data is transferred under following conditions.

CL frequency f_{CL} = 14 kHz (data transfer rate)

M frequency fM = 35 Hz (frame frequency / 2)

Display duty ratio 1/200

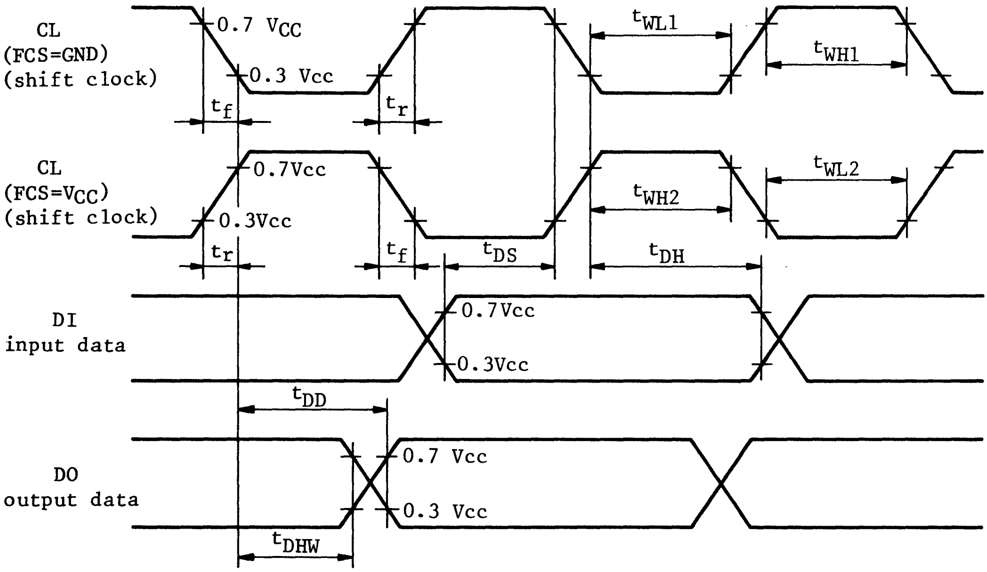
$V_{IH} = V_{CC}$, V_{IL} = GND

No load on outputs

(Note 7) The currents flowing through the V_{EE} terminal in the conditions of (Note 6). No line is to be connected to the V terminal.

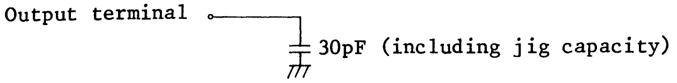
● AC CHARACTERISTICS

(V_{CC} = 5V ± 10%, GND = 0V, Ta = -20 to +75°C)



Item	Symbol	Min.	Typ.	Max.	Unit	Note
Clock low level width (FCS = GND)	tWL1	5.0			µs	
Clock high level width (FCS = GND)	tWH1	125			ns	
Clock low level width (FCS = Vcc)	tWL2	125			ns	
Clock high level width (FCS = Vcc)	tWH2	5.0			µs	
Data setup time	tDS	100			ns	
Data hold time	tDH	100			ns	
Output delay time	tDD			3.0	µs	1
Output hold time	tDHW	100			ns	
Clock rise time	tr			30	ns	
Clock fall time	tf			30	ns	

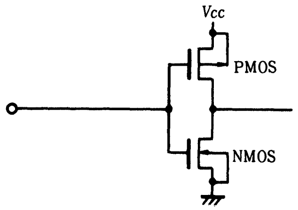
Note 1) The following load circuits are connected for specification:



TERMINAL CONFIGURATION

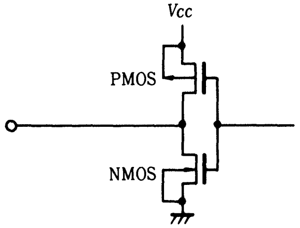
- Input Terminal

Applicable Terminals: DI, CL, SHL, FCS, M



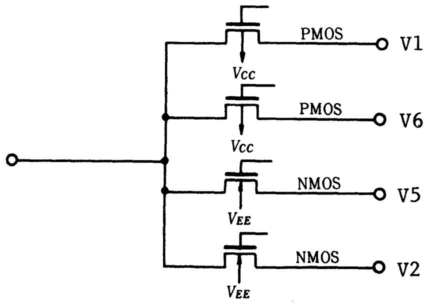
- Output Terminal

Applicable Terminal: DO

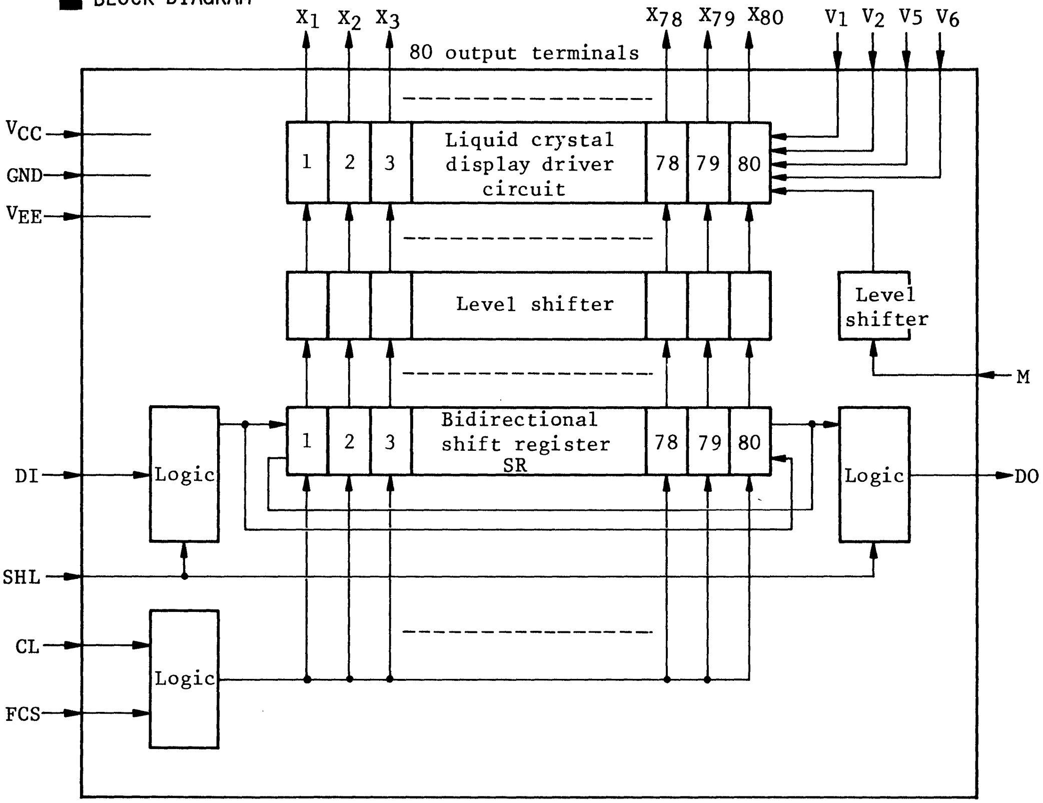


- Output Terminal

Applicable Terminals: X1 ∿ X80



BLOCK DIAGRAM



BLOCK FUNCTIONS

- Bidirectional Shift Register

This is a 80-bit bidirectional register. The data from the DI terminal is shifted by the shift clock CL. The output terminal DO outputs the last shifted data. In case of serial cascade connection, the terminal DO functions as the data input to the next LSI. The terminal SHL selects the data shift direction, and the terminal FCS selects the shift clock phase.

Truth Table

(Positive Logic)

SHL	Data Shift Direction
1	DI→SR1→SR2→SR3 ------- SR79→SR80→DO
0	DI→SR80→SR79→SR78 -------- SR2→SR1→DO

FCS	Shift Clock Phase
0	Shifted at the falling edge of CL.
1	Shifted at the rising edged of CL.

- Liquid Crystal Display Driver Circuit

The combination of the data from the shift register with M signal allows one of the four liquid crystal display driver levels V1, V2, V5, and V6 to be transferred to the output terminals.

Truth Table

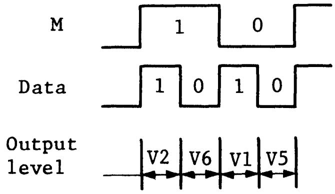
(Positive Logic)

Data from the shift register	M	Output level
0	0	V5
1	0	V1
0	1	V6
1	1	V2

- HD61105 TERMINAL FUNCTIONS

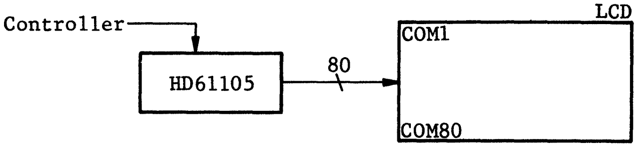
Terminal name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 1		Power supply	V_{CC} - GND: Power supply for internal logic V_{CC} - V_{EE}: Power supply for LCD drive circuit
V1 V2 V5 V6	4		Liquid crystal drive level power supply	Power supply for liquid crystal drive V1, V2 --- selection level V5, V6 --- non-selection level
FCS	1	I	V_{CC} or GND	Selects shift clock phase. FCS = V_{CC} Shift register operates at the rising edge of CL. FCS = GND Shift register operates at the fall of CL.
M	1	I	Controller	Signal to convert LCD driver signal into AC.

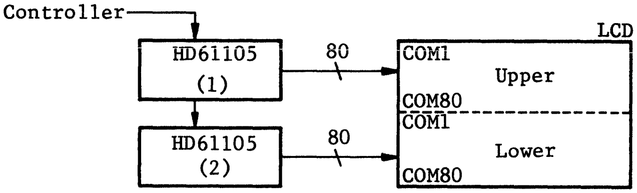
- to be continued

<table>
<tr><th>Terminal name</th><th>Number of Terminals</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>CL</td><td>1</td><td>I</td><td>Controller</td><td>Shift clock
FCS = V_{CC} Shift register operates at the rise of CL.
FCS = GND Shift register operates at the fall of CL.</td></tr>
<tr><td>DI</td><td>1</td><td>I</td><td>Controller or the terminal DO of HD61105</td><td>Shift register data input
In case of cascade connection, the terminal DI is connected to the terminal DO of the preceding LSI.</td></tr>
<tr><td>DO</td><td>1</td><td>O</td><td>Open or the terminal DI of HD61105</td><td>Shift register data output
In case of cascade connection, the terminal DO is connected to the terminal DI of the next LSI.</td></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects shift direction of bidirectional shift register.
<table>
<tr><th>SHL</th><th>Shift direction</th><th>Common scanning direction</th></tr>
<tr><td>VCC</td><td>DI→SR1→SR2→SR80</td><td>X1→X80</td></tr>
<tr><td>GND</td><td>DI→SR80→SR79→SR1</td><td>X80→X1</td></tr>
</table></td></tr>
<tr><td>X1 ∿ X80</td><td>80</td><td>O</td><td>Liquid crystal display</td><td>Liquid crystal display driver output
Outputs one of the four liquid crystal display driver levels V1, V2, V5 and V6 with the combination of the data from the shift register and M signal.

Data "1" --- Selection level
"0" --- Non-selection level
When SHL is VCC, X1 corresponds to COM1 and X80 corresponds to COM80.
When SHL is GND, X80 corresponds to COM1 and X1 corresponds to COM80.</td></tr>
<tr><td>NC</td><td>7</td><td></td><td>Open</td><td>Unused.
No line is to be connected.</td></tr>
</table>

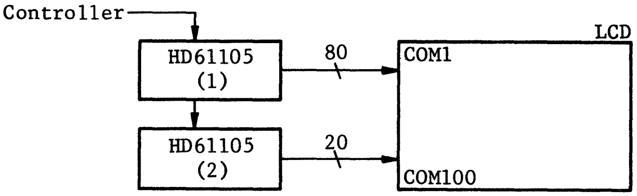
● OUTLINE OF HD61105 SYSTEM CONFIGURATION

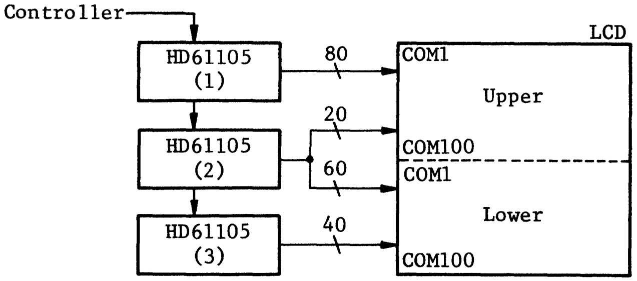
1) When display duty ratio of LCD is 1/80



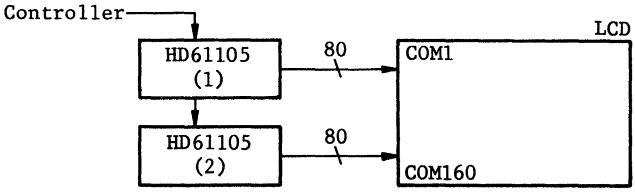


2) When display duty ratio of LCD is 1/100

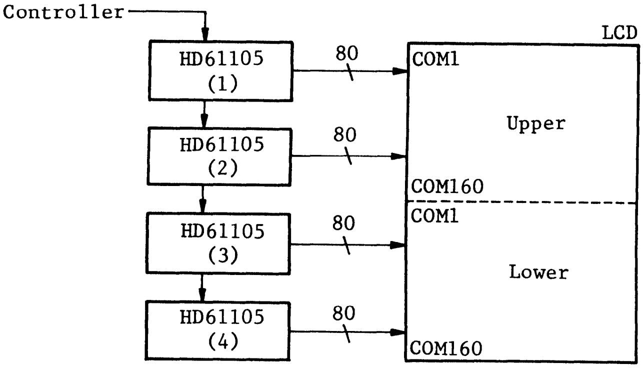




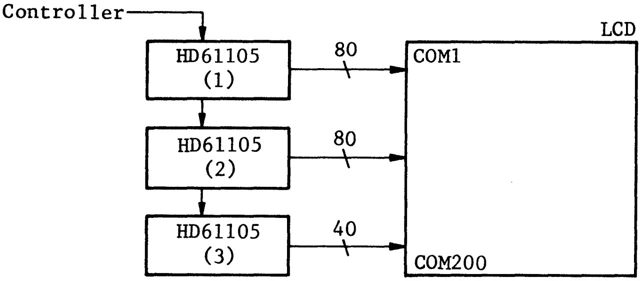
3) When display duty ratio of LCD is 1/160

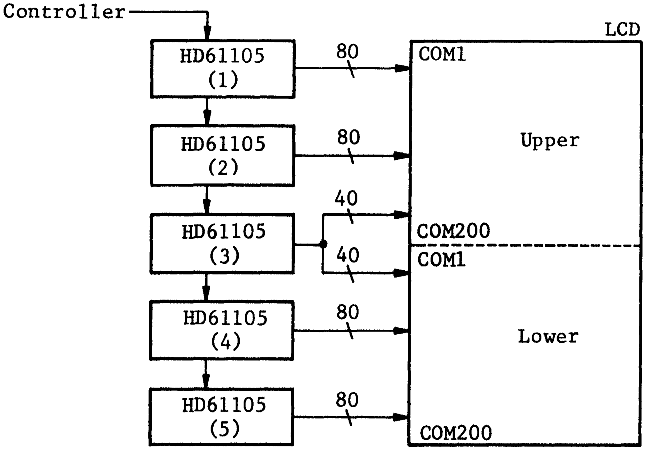


4) When display duty ratio of LCD is 1/160



5) When display duty ratio of LCD is 1/200

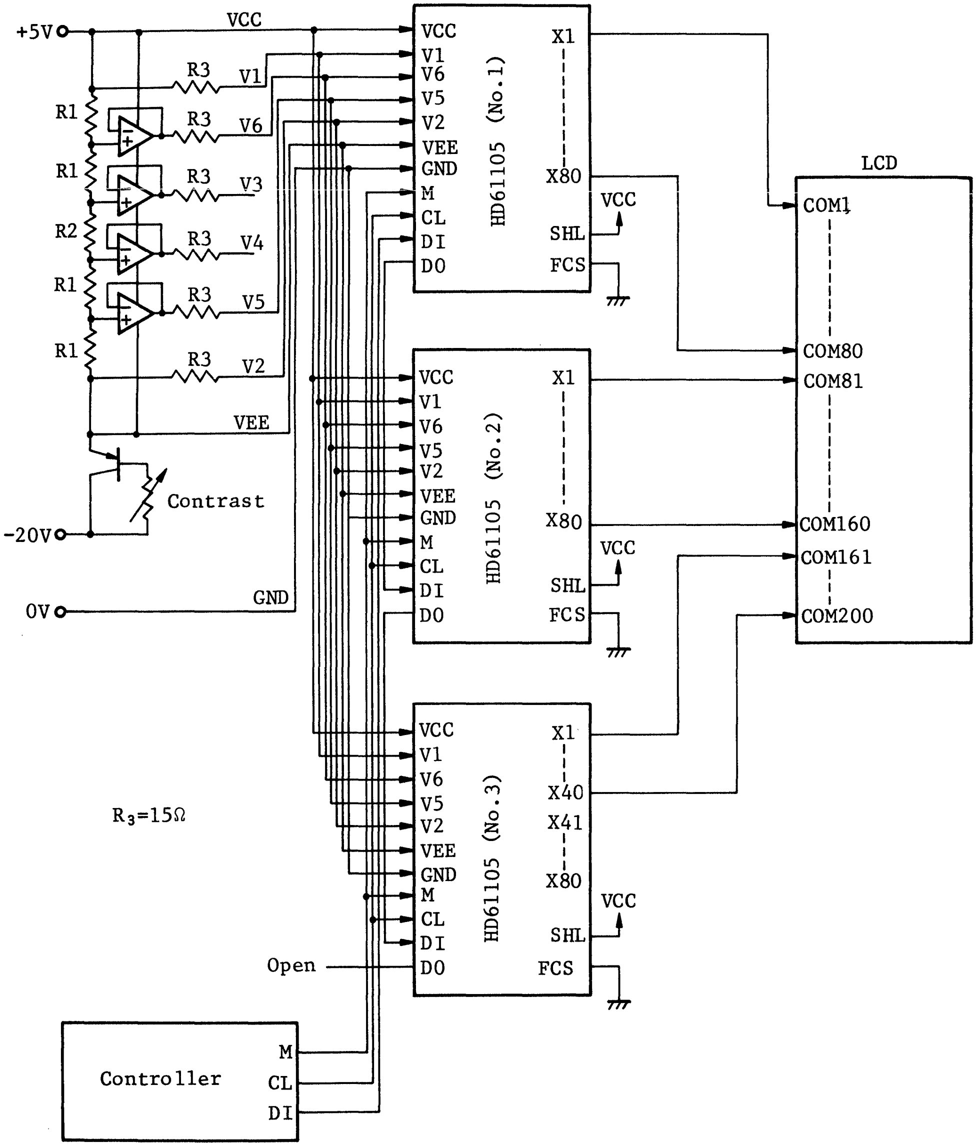




- EXAMPLE OF CONNECTION

1) 1/200 duty ratio

a) Example of connection (SHL = V_{CC}, FCS = GND)

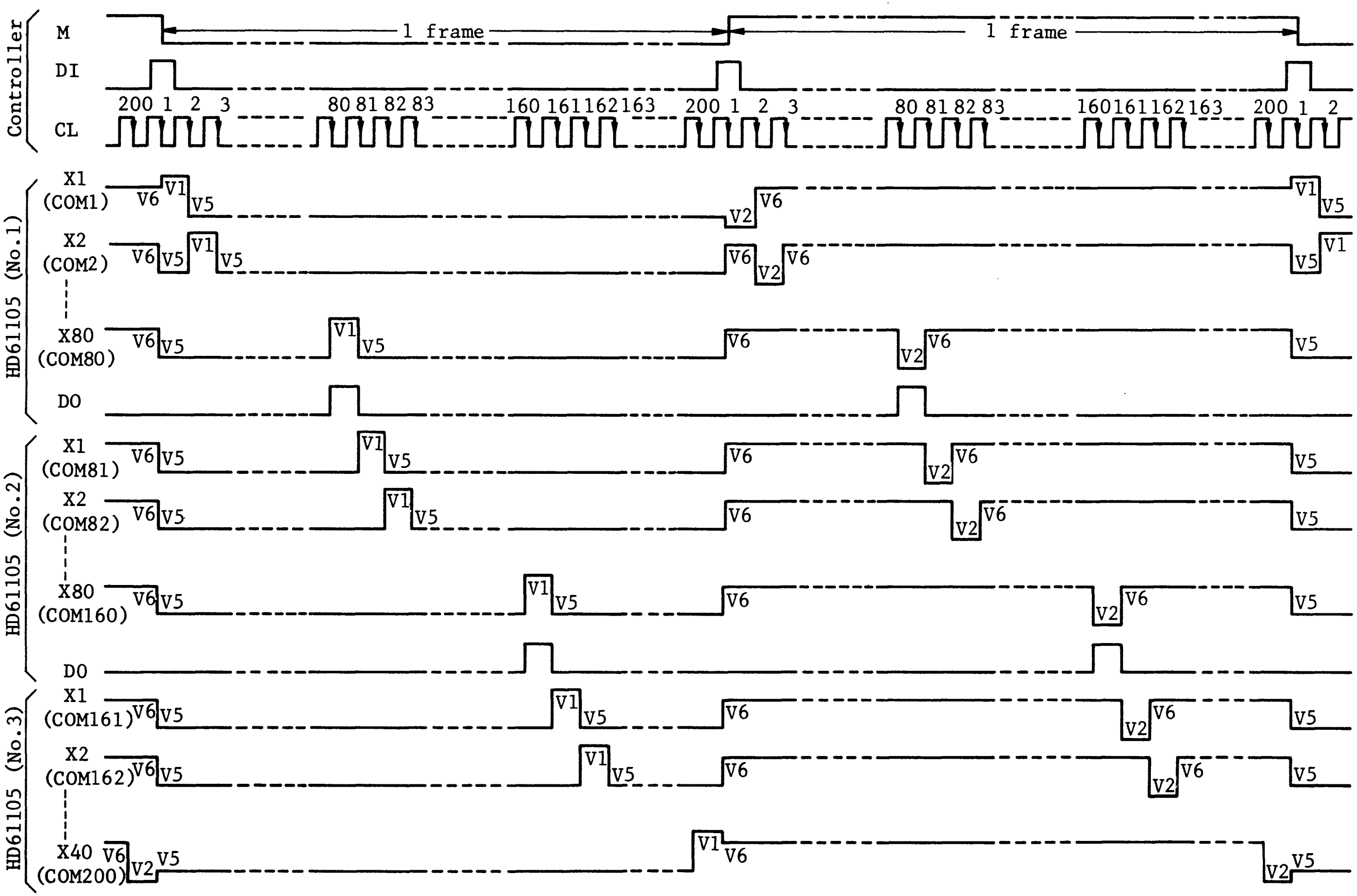


Note 1) The values of R1 and R2 vary with the LCD panel used.
When bias factor is 1/15, the values of R1 and R2 should satisfy

$$\frac{R1}{4R1 + R2} = \frac{1}{15}$$

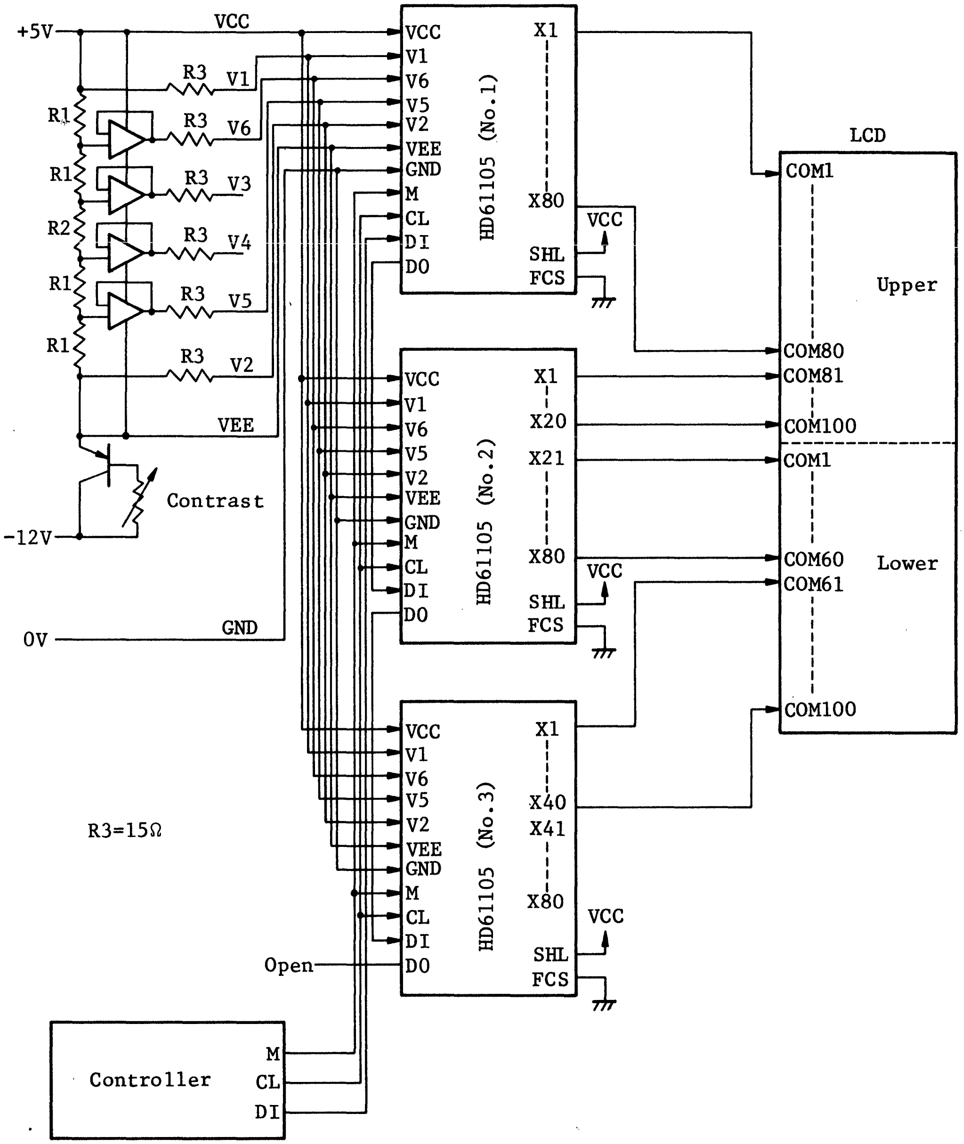
For example, R1 = 3k, R2 = 33kΩ

b) Example of Waveform



2) 1/100 duty ratio

a) Example of connection 1 (SHL = V_{CC}, FCS = GND)



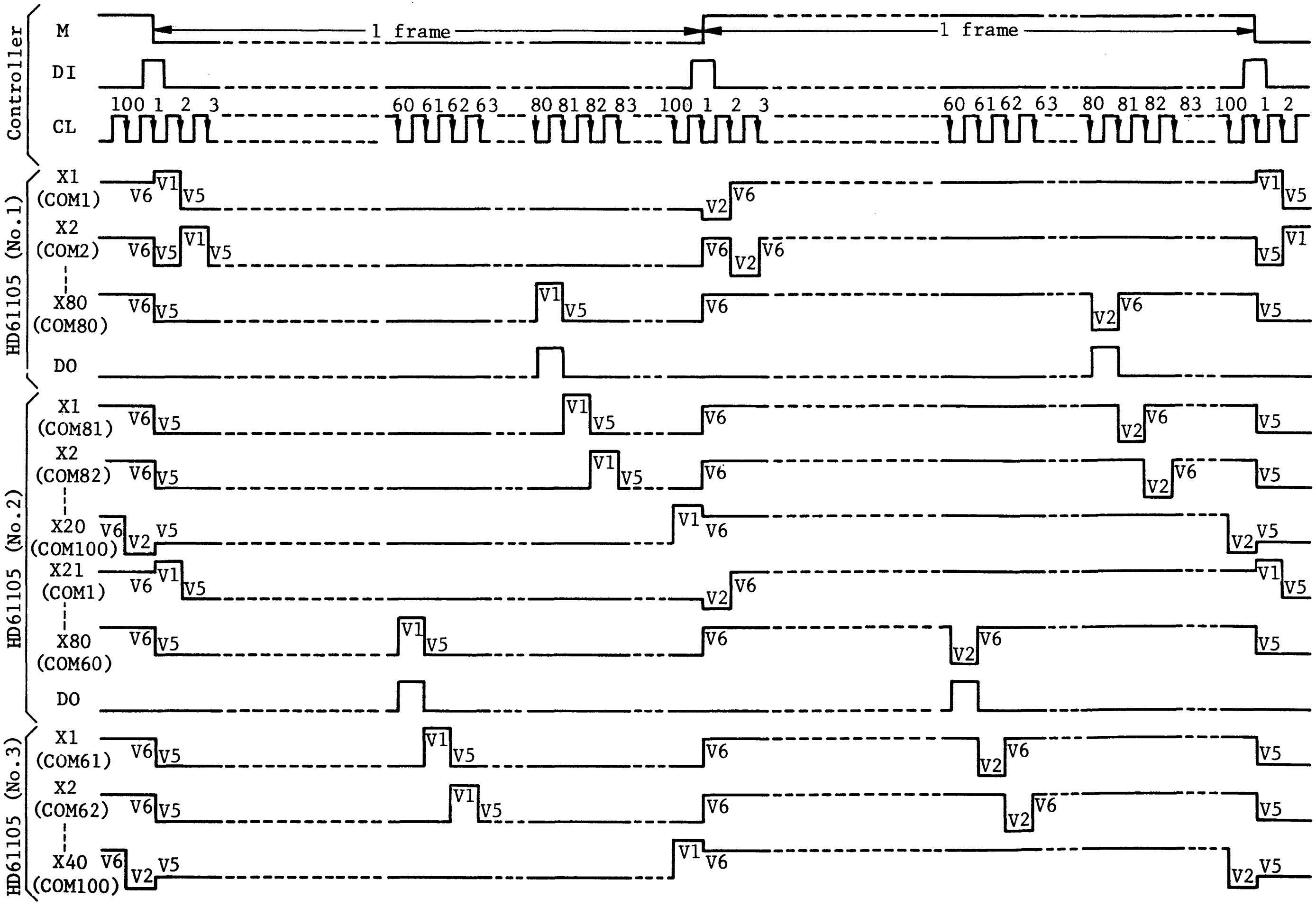
Note 1) The values of R1 and R2 vary with the LCD panel used.

When bias factor is 1/11, the values of R1 and R2 should satisfy

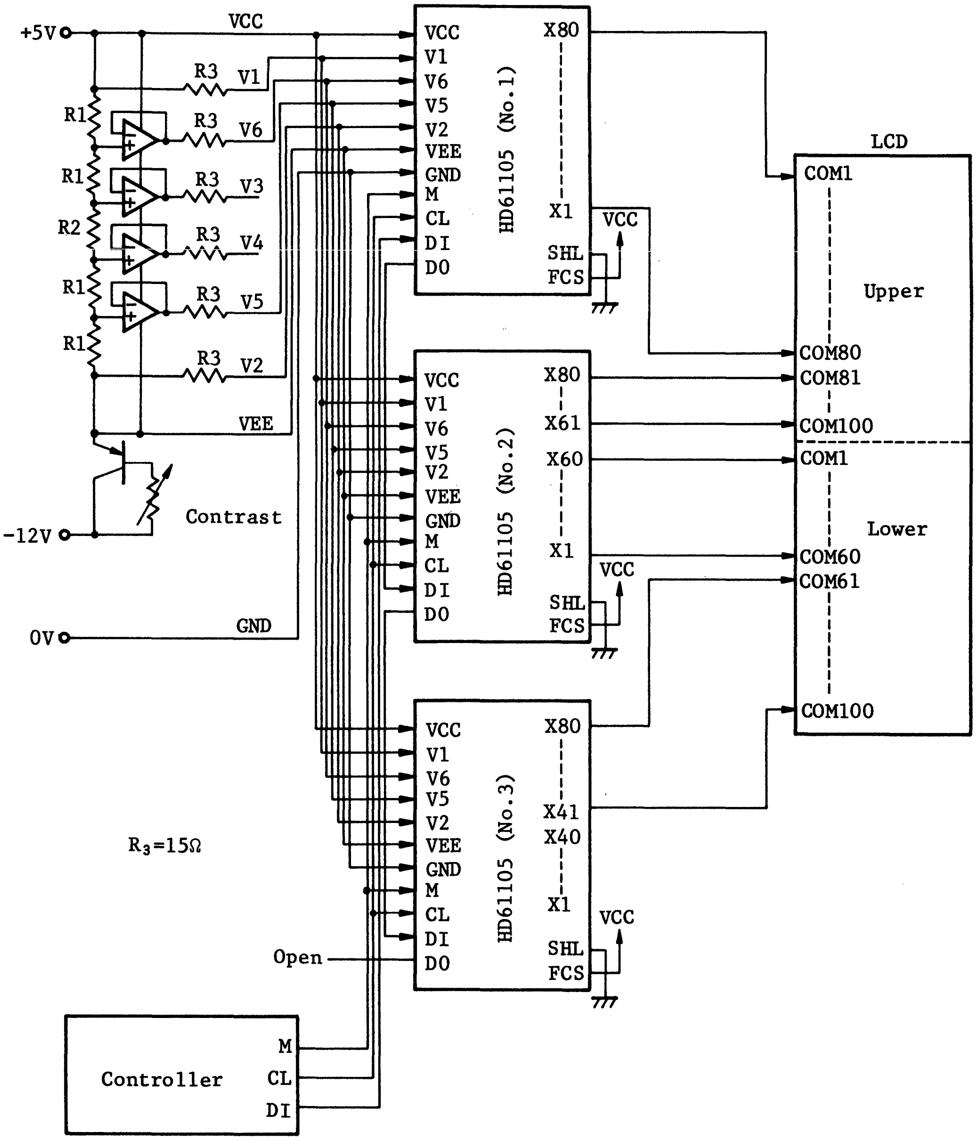
$$\frac{R1}{4R1 + R2} = \frac{1}{11}$$

For example, R1 = 3kΩ, R2 = 21kΩ

b) Example of Waveform



c) Example of connection 2 (SHL = GND, FCS = V_{CC})



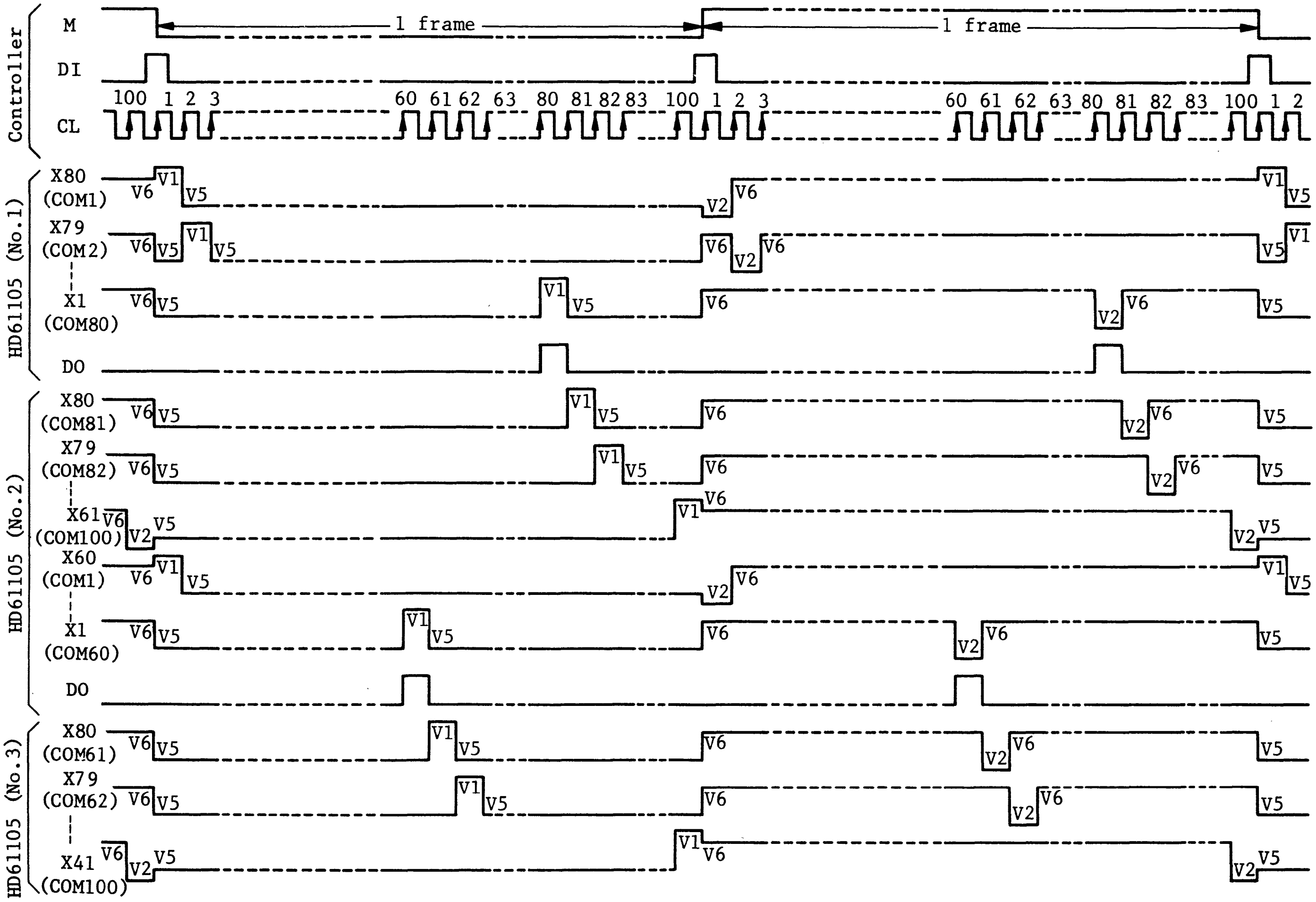
Note 1) The values of R1 and R2 vary with the LCD panel used.

When bias factor is 1/11, the values of R1 and R2 should satisfy

$$\frac{R1}{4R1 + R2} = \frac{1}{11}$$

For example, R1 = 3kΩ, R2 = 21kΩ

d) Example of Waveform



HD61830

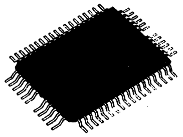
(Dot Matrix Liquid Crystal Graphic Display Controller)

DESCRIPTION

The HD61830 is a dot matrix liquid crystal graphic display controller LSI that stores the display data sent from an 8-bit microcomputer in the external RAM to generate dot matrix liquid crystal driving signals.

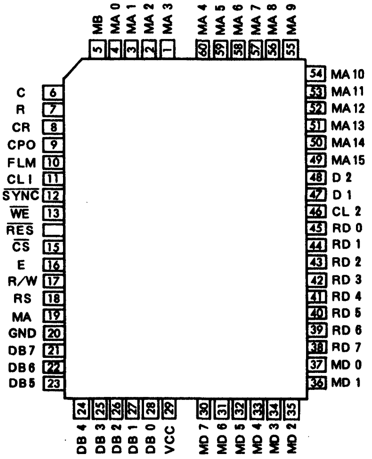
It is possible to select the graphic mode in which the 1-bit data of the external RAM corresponds to the ON/OFF state of 1 dot on liquid crystal display and the character mode in which characters are displayed by storing character codes in the external RAM and developing them into the dot patterns with the internal character generator ROM. Both modes can be provided for various applications.

The HD61830 is produced in the CMOS process. Thus, the combination with a CMOS microcomputer can accomplish a liquid crystal display device with lower power dissipation.



(FP—60)

■ PIN ARRANGEMENT

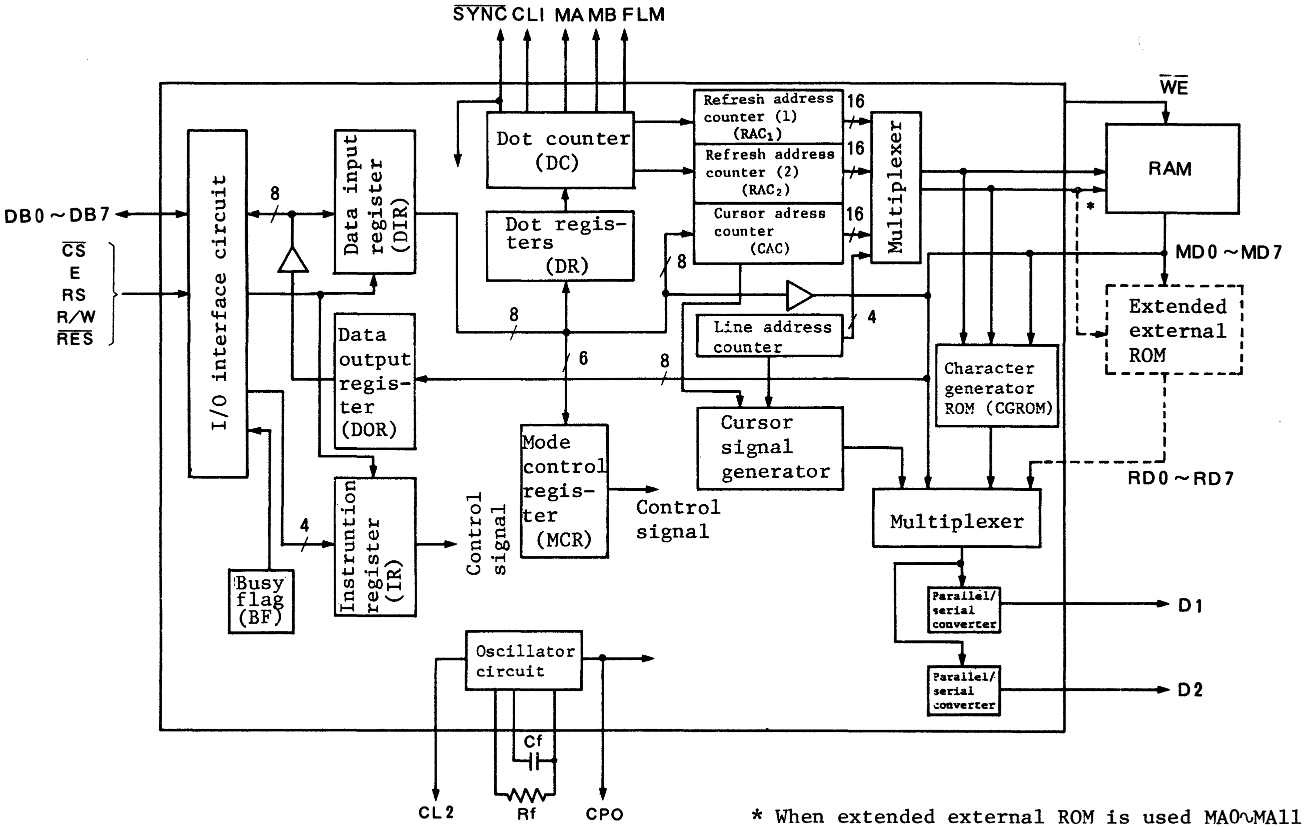


(Top View)

■ FEATURES

- Dot matrix liquid crystal graphic display controller
- Display control capacity
  - Graphic mode .... 512K dots (2^{16} bytes)
  - Character mode ..... 4096 characters (2^{12} characters)
- Internal character generator ROM ..... 7360 bits
  - 160 types of 5×7 dot character fonts
  - 32 types of 5×11 dot character fonts
  - Total 192 types
  - (Can be extended to 256 types (4K bytes max.) by external ROM)
- Interfaceable to 8-bit MPU
- Display duty (Can be selected by a program)
  - Static to 1/128 duty selectable
- Various instruction functions
  - Scroll, Cursor ON/OFF/blink, Character blink, Bit manipulation
- Display method ..... Selectable A or B types
- Internal oscillator (with external resistor and capacitor)
- Low power dissipation
- Power supply: Single +5V
- CMOS process
- 60-pin flat plastic package

■BLOCK DIAGRAM



* When extended external ROM is used MA0∿MA11 are applied to RAM, MA12∿MA15 are applied to extended external ROM.

■BLOCK FUNCTIONS

●Registers

The HD61830 has the five types of registers: instruction register (IR), data input register (DIR), data output register (DOR), dot registers (DR) and mode control register (MCR).

The IR is a 4-bit register which stores the instruction codes for specifying MCR, DR, a start address register, a cursor address register and so on. The lower order 4 bits DB0 to DB3 of data buses are written in it.

The DIR is an 8-bit register used to temporarily store the data written into the external RAM, DR, MCR and so on.

The DOR is an 8-bit register used to temporarily store the data read from the external RAM. Cursor address information is written into the cursor address counter (CAC) through the DIR. When the memory read instruction is set in the IR (latched at the falling edge of E signal), the data of external RAM is read to DOR by an internal operation. The data is transferred to the MPU by reading the DOR with the next instruction (the contents of DOR are output to the data bus when E is at "High" level).

The DR are registers used to store the dot informations such as character pitches and the number of vertical dots and so on. The information sent from the MPU is written into the DR via the DIR.

The MCR is a 6-bit register used to store the data which specifies states of display such as display ON/OFF and cursor ON/OFF/blink. The information sent from the MPU is written in it via the DIR.

● Busy Flag (BF)

With "1", the busy flag indicates the HD61830 is performing an internal operation. The next instruction cannot be accepted. As shown in Control Instruction(14),the busy flag is output on DB7 under the conditions of RS=1, R/W=1 and E=1. Make sure the busy flag is "0" before writing the next instruction.

● Dot Counters (DC)

The dot counters are counters that generate liquid crystal display timing according to the contents of DR.

● Refresh Address Counters (RAC1/RAC2)

The refresh address counters are counters used to control the addresses of external RAM, character generator ROM (CGROM) and extened external ROM having the two types: RAC1 and RAC2. The RAC1 is used for upper half of screen and the RAC2 for lower half. In the graphic mode, 16-bit data is output and used as the address signal of external RAM. In the character mode, the high order 4 bits (MA12∿MA15) are ignored. The 4 bits of line address counter are output instead of it and used as the address of extended ROM.

● Character Generator ROM

The character generator ROM has 7360 bits in total and stores 192 types of character data. A character code (8 bits) from the external RAM and a line code (4 bits) from the line address counter are applied to its address signals, and it outputs 5-bit dot data.

The character font is 5×7 (160 types) or 5×11 (32 types). The use of extended ROM allows 8×16 (256 types max.) to be used.

● Cursor Address Counter

The cursor address counter is a 16-bit counter that can be preset by the instruction. It is used to hold an address when the data of external RAM is read or written (when display dot data or a character code is read or written). The value of cursor address counter is automatically increased by 1 after the display data is read or written and after the Set/Clear Bit instruction is executed.

● Cursor Signal Generator

The cursor can be displayed by the instruction in the character mode. The cursor is automatically generated on the display specified by the cursor address and cursor position.

● Parallel/Serial Conversion

The parallel data sent from the external RAM, character generator ROM or extended ROM is converted into serial data by two parallel/serial conversion circuits and transferred to the liquid crystal driver circuits for upper screen and lower screen simultaneously.

■TERMINAL FUNCTIONS

Name	Function
DB0∿7	Data bus ... Three-state I/O common terminal Data is transferred to MPU through DB0 to DB7.
$\overline{\text{CS}}$	Chip select ... Selected state with $\overline{\text{CS}}$=0.
R/W	Read/Write ... R/W=1 ... MPU ← HD61830 R/W=0 ... MPU → HD61830
RS	Register select ... RS=1 ... Instruction register RS=0 ... Data register
E	Enable ... Data is written at the fall of E. Data can be read while E is 1.
CR, R, C	CR oscillator
$\overline{\text{RES}}$	Reset ... Reset=0 results in display OFF, slave mode and Hp=6.
MA0∿15	External RAM address output In character mode, the line code for external CG is output through MA12 to MA15 ("0": Character 1st line, "F": Character 16th line).
MD0∿7	Display data bus ... Three-state I/O common terminal.
RD0∿7	ROM data input ... Dot data from external character generator is input.
$\overline{\text{WE}}$	Write enable ... Write signal for external RAM.
CL2	Display data shift clock for LCD drivers.
CL1	Display data latch signal for LCD drivers.
FLM	Frame signal for display synchronization.
MA	Signal for converting liquid crystal driving signal into AC, A type
MB	Signal for converting liquid crystal driving signal into AC, B type
D1, D2	Display data serial output D1 ... For upper half of screen D2 ... For lower half of screen
CPO	Clock signal for HD61830 in slave mode.
$\overline{\text{SYNC}}$	Synchronous signal for parallel operation. Three-state I/O common terminal (with pull-up MOS). Master ... Synchronous signal is output. Slave ... Synchronous signal is input.

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	-0.3 ∿ +7.0	V	1, 2
Terminal voltage	V_T	-0.3 ∿ V_{CC}+0.3	V	1, 2
Operating temperature	T_{opr}	-20 ∿ +75	°C	
Storage temperature	T_{stg}	-55 ∿ +125	°C	

Note 1: All voltage is referred to GND=0V.

Note 2: If LSI's are used beyond absolute maximum ratings, they may be permanently destroyed. We strongly recommend you to use the LSI's within electrical characteristic limits for normal operation, because use beyond these conditions will cause malfunction and poor reliability.

■ELECTRICAL CHARACTERISTICS

(V_{CC}=5V±5%, GND=0V, Ta=-20∿+75°C)

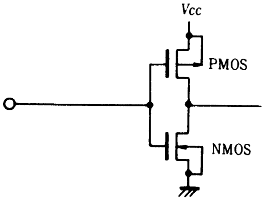
Item	Symbol	Test condition	Min.	Typ	Max.	Unit	Note
Input "High" voltage (TTL)	V_{IH}		2.2	-	V_{CC}	V	1
Input "Low" voltage (TTL)	V_{IL}		0	-	0.8	V	2
Input "High" voltage	V_{IHR}		3.0	-	V_{CC}	V	3
Input "High" voltage (CMOS)	V_{IHC}		0.7V_{CC}	-	V_{CC}	V	4
Input "Low" voltage (CMOS)	V_{ILC}		0	-	0.3V_{CC}	V	4
Output "High" voltage (TTL)	V_{OH}	$-I_{OH}$=0.6mA	2.4	-	V_{CC}	V	5
Output "Low" voltage (TTL)	V_{OL}	I_{OL}=1.6mA	0	-	0.4	V	5
Output "High" voltage(CMOS)	V_{OHC}	$-I_{OH}$=0.6mA	V_{CC}-0.4	-	V_{CC}	V	6
Output "Low" voltage (CMOS)	V_{OLC}	I_{OL}=0.6mA	0	-	0.4	V	6
Input leakage current	I_{IN}	V_{IN}=0∿V_{CC}	-5	-	5	µA	7
Three-state leakage current	I_{TSL}	V_{OUT}=0∿V_{CC}	-10	-	10	µA	8
Power dissipation (1)	P_{w1}	CR oscillation fosc=500kHz	-	10	15	mW	9
Power dissipation (2)	P_{w2}	External clock fcp=1MHz	-	20	30	mW	9
Internal clock operation							
Clock oscillation frequency	fosc	Cf=15pF±5% Rf=39kΩ±2%	400	500	600	kHz	10

Item	Symbol	Test condition	Min.	Typ	Max.	Unit	Note
External clock operation							
External clock operating frequency	f_{cp}		100	500	1100	kHz	11
External clock duty	Duty		47.5	50	52.5	%	11
External clock rise time	t_{rcp}		-	-	0.05	μs	11
External clock fall time	t_{fcp}		-	-	0.05	μs	11
Pull-up current	I_{PL}	V_{IN}=GND	2	10	20	μA	12

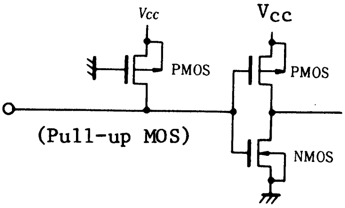
Note: The I/O terminals are of the following configuration:

- Shape of Input Terminal

Applicable terminal: $\overline{CS}$, E, RS, R/W, $\overline{RES}$, CR (Without pull-up MOS)

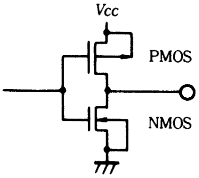


Applicable terminal: RD0~RD7 (With pull-up MOS)



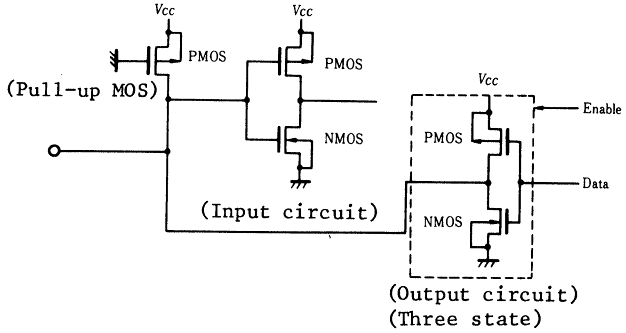
- Shape of Output Terminal

Applicable terminal: CL1, CL2, MA, MB, FLM, CPO, D1, D2, $\overline{WE}$, $\overline{OE}$, $\overline{CE}$, MA0~MA15



- Shape of I/O Common Terminal

Applicable terminal: DB0∿DB7, $\overline{\text{SYNC}}$, MD0∿MD7



Note 1: Applied to input terminals and I/O common terminals, except terminals $\overline{\text{SYNC}}$, CR and $\overline{\text{RES}}$.

Note 2: Applied to input terminals and I/O common terminals, except terminals $\overline{\text{SYNC}}$ and CR.

Note 3: Applied to terminal $\overline{\text{RES}}$.

Note 4: Applied to terminals $\overline{\text{SYNC}}$ and CR.

Note 5: Applied to terminals DB0∿DB7, $\overline{\text{WE}}$, MA0∿MA15,and MD0∿MD7.

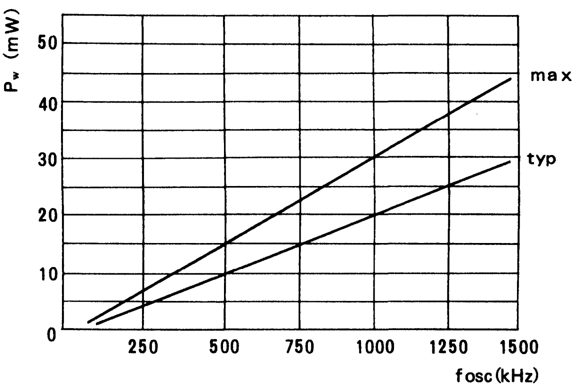
Note 6: Applied to terminals $\overline{\text{SYNC}}$, CPO, FLM, CL1, CL2, D1, D2, MA and MB.

Note 7: Applied to input terminals.

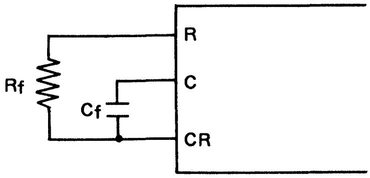
Note 8: Applied to I/O common terminals. However, the current which flows into the output drive MOS is excluded.

Note 9: The current which flows into the input and output circuits is excluded. When the input of CMOS is in the intermediate level, current flows through the input circuit, resulting in the increase of power supply current. To avoid this, input must be fixed at high or low.

The relationship between the operating frequency and the power dissipation is given below.



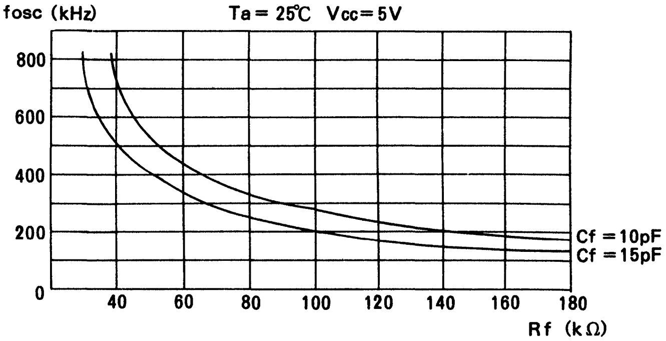
Note 10: Applied to the operation of internal oscillator when oscillation resistor Rf and oscillation capacity Cf are used.



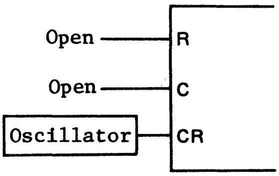
$C_f = 15pF \pm 5\%$
$R_f = 39k\Omega \pm 2\%$

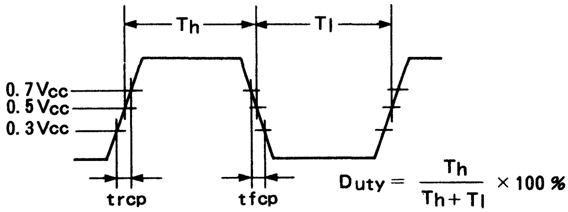
(when fosc = 500kHz typ)

The relationship among oscillation frequency, Rf and Cf is given below.



Note 11: Applied to external clock operation.

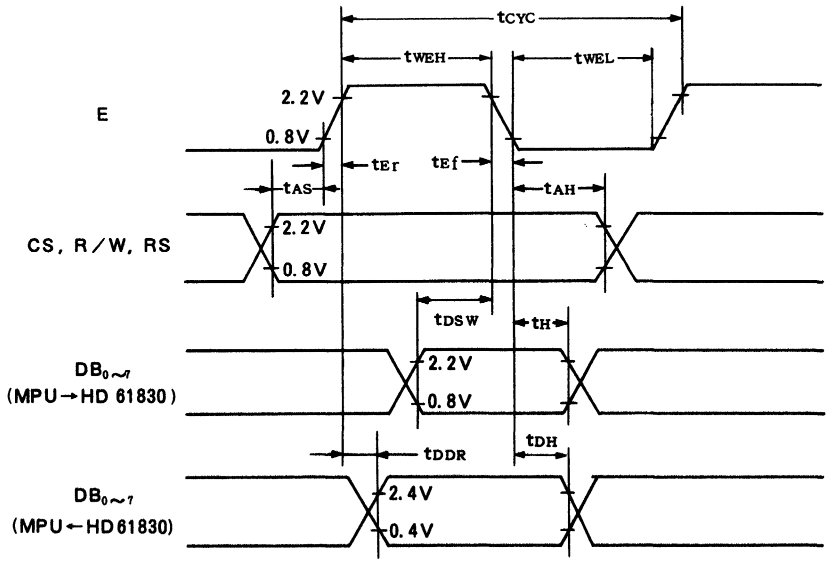




Note 12: Applied to $\overline{\text{SYNC}}$, DB0∿DB7, and RD0∿RD7.

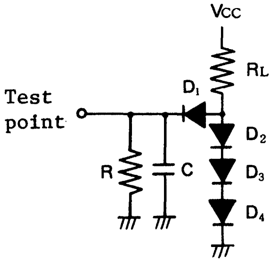
■TIMING CHARACTERISTICS

●Bus Read/Write Operation (Interface to MPU)



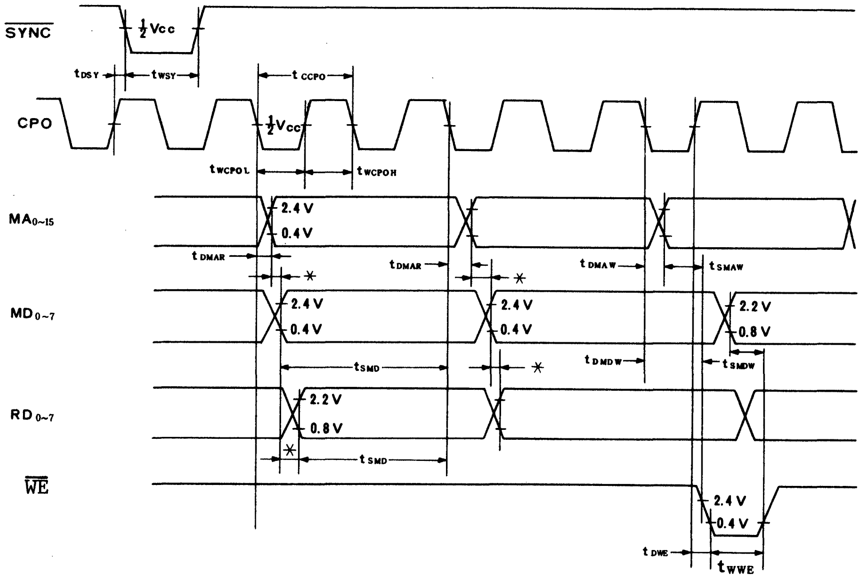
Item		Symbol	Min.	Typ	Max.	Unit	
Enable cycle time		t_{CYC}	1.0	-	-	μs	
Enable pulse width	"High" level	t_{WEH}	0.45	-	-	μs	
	"Low" level	t_{WEL}	0.45	-	-	μs	
Enable rise time		t_{Er}	-	-	25	ns	
Enable fall time		t_{Ef}	-	-	25	ns	
Setup time		t_{AS}	140	-	-	ns	
Data setup time		t_{DSW}	225	-	-	ns	
Data delay time		t_{DDR}	-	-	225	ns	Note
Data hold time		t_{H}	10	-	-	ns	
Address hold time		t_{AH}	10	-	-	ns	
Data hold time		t_{DH}	20	-	-	ns	

Note: The following load circuit is connected for specification:



R_L = 2.4 kΩ
R = 11 kΩ
C = 130 pF
Diodes D1 to D4: 1S2074 Ⓗ

●Interface to External RAM and ROM

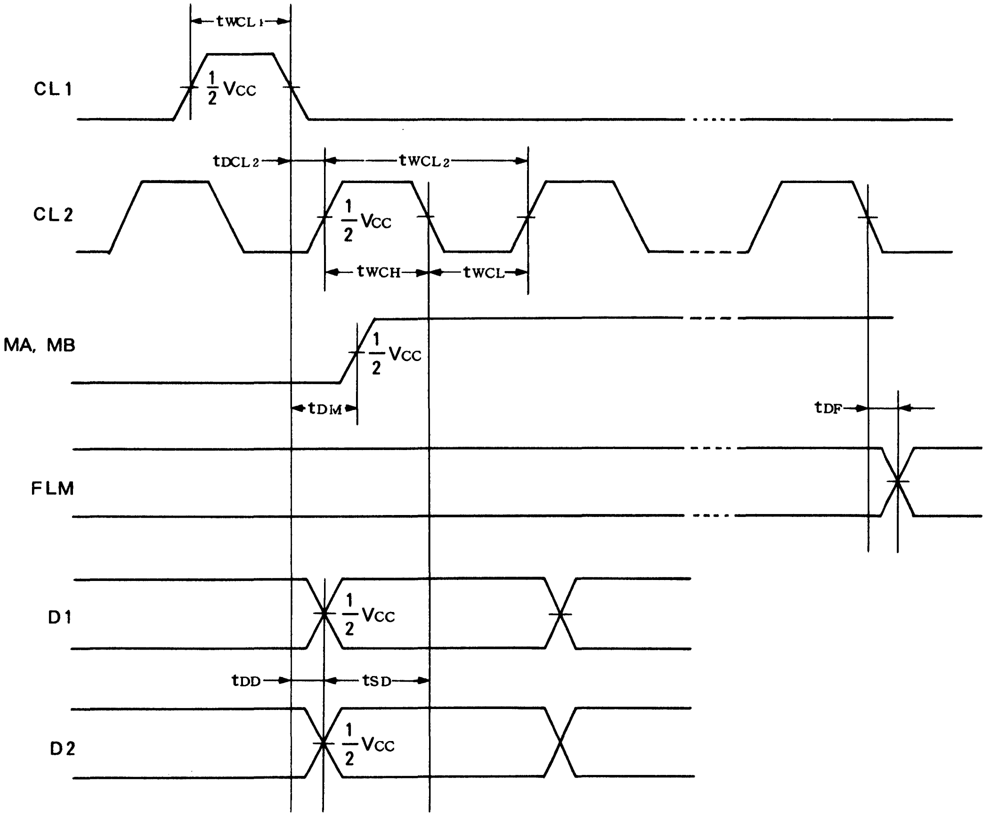


Item		Symbol	Min.	Typ	Max.	Unit
$\overline{\text{SYNC}}$ delay time		t_{DSY}	-	-	200	ns
$\overline{\text{SYNC}}$ pulse width	"High" level	t_{WSY}	900	-	-	ns
CPO cycle time		t_{CCPO}	900	-	-	ns
CPO pulse width	"High" level	t_{WCPOH}	450	-	-	ns
	"Low" level	t_{WCPOL}	450	-	-	ns
MA0 to MA15 refresh delay time		t_{DMAR}	-	-	200	ns
MA0 to MA15 write address delay time		t_{DMAW}	-	-	200	ns
MD0 to MD7 write data delay time		t_{DMDW}	-	-	200	ns
MD0 to MD7, RD0 to RD7 setup time		t_{SMD}	900	-	-	ns
Memory address setup time		t_{SMAW}	250	-	-	ns
Memory data setup time		t_{SMDW}	250	-	-	ns
$\overline{\text{WE}}$ delay time		t_{DWE}	-	-	200	ns
$\overline{\text{WE}}$ pulse width ("Low" level)		t_{WWE}	450	-	-	ns

Note 1: No load is applied to all the output terminals.

Note 2: "*" indicates the delay time of RAM and ROM.

- Data Transfer to Driver LSI



Item		Symbol	Min.	Typ	Max.	Unit
Clock pulse width ("High" level)		t_{WCL1}	450	-	-	ns
Clock delay time		t_{DCL2}	-	-	200	ns
Clock cycle time		t_{WCL2}	900	-	-	ns
Clock pulse width	"High" level	t_{WCH}	450	-	-	ns
	"Low" level	t_{WCL}	450	-	-	ns
MA, MB delay time		t_{DM}	-	-	300	ns
FLM delay time		t_{DF}	-	-	300	ns
Data delay time		t_{DD}	-	-	200	ns
Data setup time		t_{SD}	250	-	-	ns

Note: No load is applied to all the output terminals (MA, MB, FLM, D1 and D2).

● Display Control Instructions

Display is controlled by writing data into the instruction register and 13 data registers. The RS signal distinguishes the instruction register from the data registers. 8-bit data is written into the instruction register with RS=1, and the code of data register is specified. After that, the 8-bit data is written in the data register and the specified instruction is executed with RS=0.

During the execution of the instruction, no new instruction cân be accepted. Since the busy flag is set during this, read the busy flag and make sure it is 0 before writing the next instruction.

(1) Mode control

Code $"00" (hexadecimal) written into the instruction register specifies the mode control register.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	0
Mode control reg.	0	0	0	0	Mode data					

DB5	DB4	DB3	DB2	DB1	DB0	Cursor/blink	CG	Graphic/character display
1/0	1/0	0	0	0	0	Cursor OFF	Internal CG	Character display (Character mode)
		0	1			Cursor ON		
		1	0			Cursor OFF, character blink		
		1	1			Cursor blink		
		0	0		1	Cursor OFF	External CG	
		0	1			Cursor ON		
		1	0			Cursor OFF, character blink		
		1	1			Cursor blink		
		0	0	1	0			Graphic mode
Display ON/OFF	Master/ slave	Blink	Cursor	Graphic/ character mode	Ext./ Int.CG			

Master/slave:
1: Master mode
0: Slave mode

Display ON/OFF:
1: Display ON
0: Display OFF

(2) Set character pitch

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	1
Character pitch reg.	0	0	$(V_P - 1)$ binary				0	$(H_P - 1)$ binary		

Vp indicates the number of vertical dots per character. The space between the vertically-displayed characters is considered for determination. This value is meaningful only during character display (in the character mode) and becomes invalid in the graphic mode.

The Hp indicates the number of horizontal dots per character in display, including the space between horizontally-displayed characters. In the graphic mode, the Hp indicates the number of bits of 1-byte display data to be displayed.

There are three Hp values.

Hp	DB2	DB1	DB0	
6	1	0	1	Horizontal character pitch 6
7	1	1	0	" 7
8	1	1	1	" 8

(3) Set number of characters

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	0
Number-of-characters reg.	0	0	0	$(H_N - 1)$ binary						

H_N indicates the number of horizontal characters in the character mode or the number of horizontal bytes in the graphic mode. If the total sum of horizontal dots on the screen is taken as n,

$$n = Hp \times H_N$$

H_N can be set with an even number of 2 to 128 (decimal).

(4) Set number of time division (inverse of display duty ratio)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	1
Number-of-time shares reg.	0	0	0	(Nx - 1) binary						

Nx indicates the number of time division in multiplex display.

1/Nx is a display duty ratio.

A value of 1 to 128 (decimal) can be set to Nx.

(5) Set cursor position

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	1	0	0
Cursor position reg.	0	0	0	0	0	0	(Cp - 1) binary			

Cp indicates the position in a character where the cursor is displayed in the character mode. For example, in 5×7 dot font, the cursor is displayed under a character by specifying Cp=8 (decimal). The cursor horizontal length is equal to the horizontal character pitch Hp. A value of 1 to 16 (decimal) can be set to Cp. If a smaller value than the number of vertical character pitches Vp is set ($Cp \leqq Vp$), and a character is overlapped with the cursor, the cursor has higher priority of display (at cursor display ON). If Cp is greater than Vp, no cursor is displayed. The cursor horizontal length is equal to Hp.

(6) Set display start low order address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	0
Display start address reg. (low order byte)	0	0	(Start low order address) binary							

(7) Set display start high order address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	1
Display start address reg. (high order byte)	0	0	(Start high order address) binary							

These instructions cause display start addresses to be written in the display start address registers. The display start address indicates a RAM address at which the data displayed at the top left end on the screen is stored. In the graphic mode, the start address is composed of high/low order 16 bits. In the character display, it is composed of the lower 4 bits of high order address ($DB_3 \sim DB_0$) and 8 bits of low order address. The upper 4 bits of high order address are ignored.

(8) Set cursor address (low order) (RAM write low order address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	0
Cursor address counter (low order byte)	0	0	(Cursor low order address) binary							

(9) Set cursor address (high order) (RAM write high order address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	1
Cursor address counter (high order byte)	0	0	(Cursor high order address) binary							

These instructions cause cursor addresses to be written in the cursor address counters. The cursor address indicates an address for sending or receiving display data and character codes to or from the RAM. Namely, data at address specified by the cursor address are read/written. In the character mode, the cursor is displayed at the digit specified by the cursor address.

A cursor address consists of the low-order address (8 bits) and the high-order address (8 bits). Satisfy the following requirements. When setting the cursor address.

1.	When you want to rewrite (set) both the low order address and the high order address.	Set the low order address and then set the high order address.
2.	When you want to rewrite only the low order address.	Don't fail to set the high order address again after setting the low order address.

3.	When you want to rewrite only the high order address.	Set the high order address. You don't have to set the low order address again.

The cursor address counter is a 16 bit up-counter with SET and RESET functions. When the bit N changes from 1 to 0, the bit N+1 is added by 1. When setting the low order address, the LSB (bit 1) of the high order address is added by 1 if the MSB (bit 8) of the low order address changes from 1 to 0. Therefore, set both the low order address and the high order address as shown in above table.

(10) Write display data

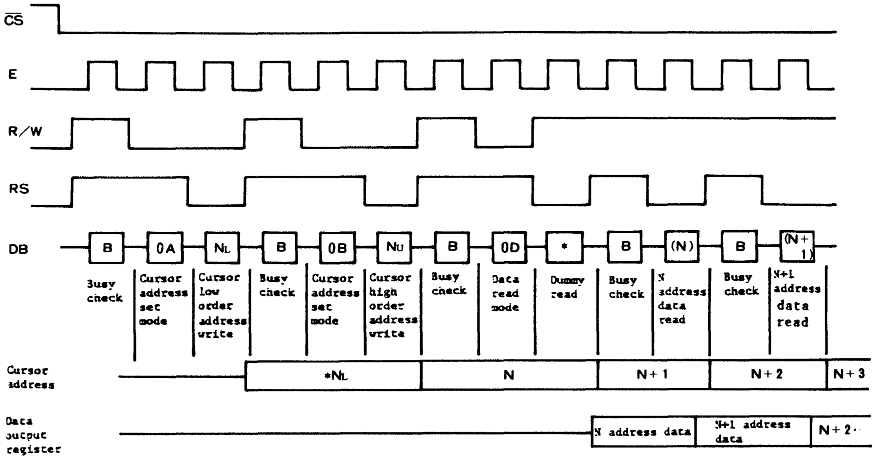
Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	0
RAM	0	0	MSB (pattern data, character code) LSB							

After the code $'0C' is written into the instruction register with RS=1, 8 bit data with RS=0 should be written into the data register. This data is transferred to the RAM specified by the cursor address as display data or character code. The cursor address is increased by 1 after this operation.

(11) Read display data

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	1
RAM	1	0	MSB (pattern data, character code) LSB							

Data can be read from the RAM with RS=0 after writing code $'0D' into the instruction register. The read procedure is as follows:



This instruction outputs the contents of data output register on Data Bus (DB0 to DB7) and then transfers RAM data specified by a cursor address to the data output register, also increasing the cursor address by 1. After setting the cursor address, correct data is not output at the first read but at the second time. Thus, make one dummy read when reading data after setting the cursor address.

(12) Clear bit

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	0
Bit clear reg.	0	0	0	0	0	0	0	(N_B - 1) binary		

(13) Set bit

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	1
Bit set reg.	0	0	0	0	0	0	0	(N_B - 1) binary		

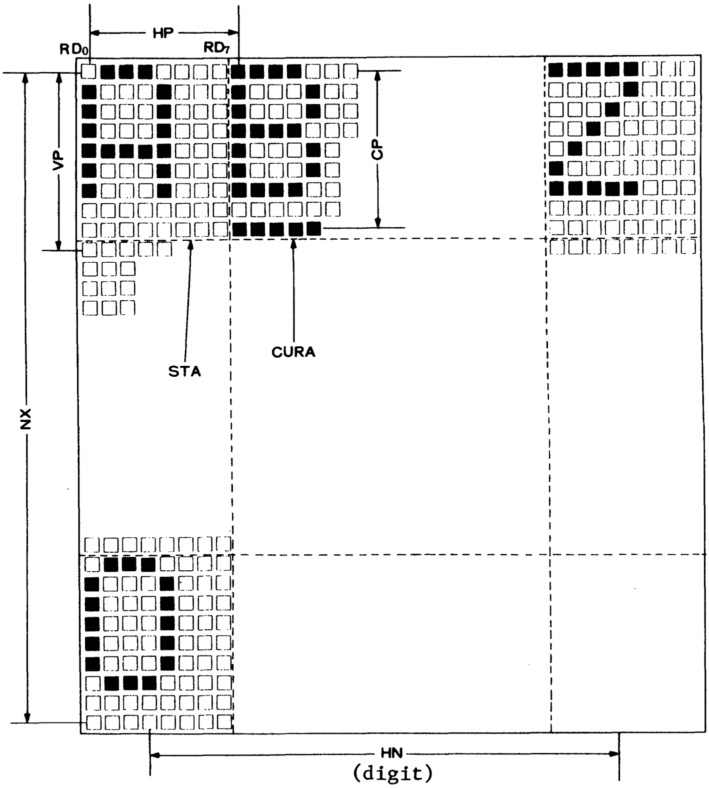
The Clear/Set Bit instruction sets 1 bit in a byte of display data RAM to 0 or 1, respectively. The position of the bit in a byte is specified by N_B and RAM address is specified by cursor address. After the execution of the instruction, the cursor address is automatically increased by 1. N_B is a value of 1 to 8. N_B=1 and N_B=8 indicates LSB and MSB, respectively.

(14) Read busy flag

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Busy flag	1	1	1/0							

When the read mode is set with RS=1, the busy flag is output to DB7. The busy flag is set to 1 during the execution of any of instructions (1) to (13). After the execution, it is set to 0. The next instruction can be accepted. No instruction can be accepted when busy flag=1. Before executing an instruction or writing data, perform a busy flag check to make sure the busy flag is 0. When data is written in the register (RS=1), no busy flag changes. Thus, no busy flag check is required just after the write operation into the instruction register with RS=1.

The busy flag can be read without specifying any instruction register.

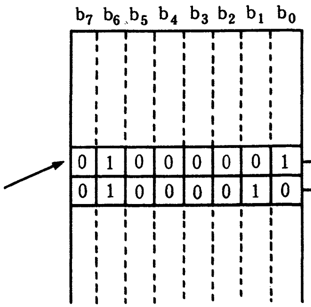
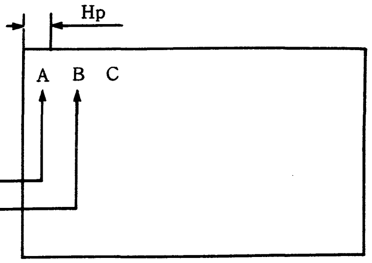
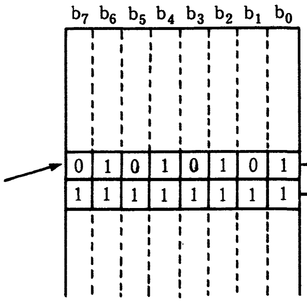
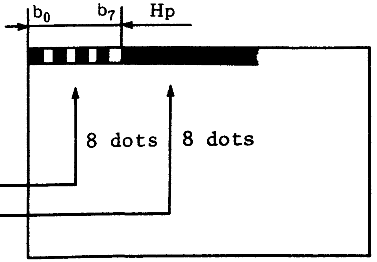


Symbol	Name	Meaning	Value
H_p	Horizontal character pitch	Lateral character pitch	6 to 8 dots
H_N	Number of horizontal characters	Number of lateral characters per line (number of digits) in the character mode or number of bytes per line in the graphic mode.	2 to 128 digits (an even number)
V_p	Vertical character pitch	Longitudinal character pitch	1 to 16 dots
C_p	Cursor position	Line number on which the cursor can be displayed	1 to 16 lines
N_x	Number of time division	Inverse of display duty ratio	1 to 128 lines

Note: If the number of vertical dots on screen is taken as m, and the number of horizontal dots as n,

$1/m = 1/Nx$ = display duty ratio
$n = Hp \times H_N$, m/Vp = Number of display lines
$C_p \leqq V_p$

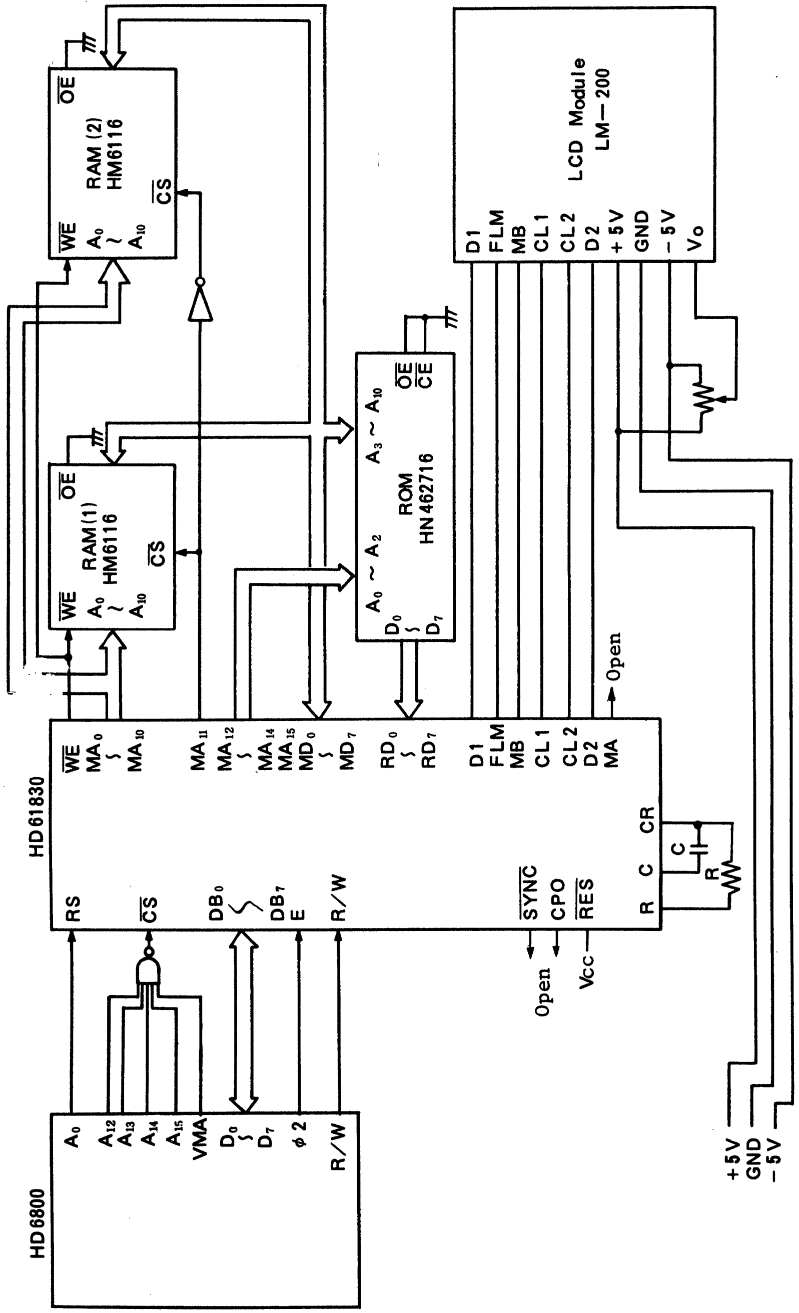
- Display Mode

Display mode	Display data from MPU	RAM	Liquid crystal display panel
Character dispaly	Character code (8 bits)	Start address  b7 b6 b5 b4 b3 b2 b1 b0 0 1 0 0 0 0 0 1 0 1 0 0 0 0 1 0	 Hp: 6, 7 or 8 dots
Graphic	Display pattern (8 bits)	Start address  b7 b6 b5 b4 b3 b2 b1 b0 0 1 0 1 0 1 0 1 1 1 1 1 1 1 1 1	 Hp: 8 dots

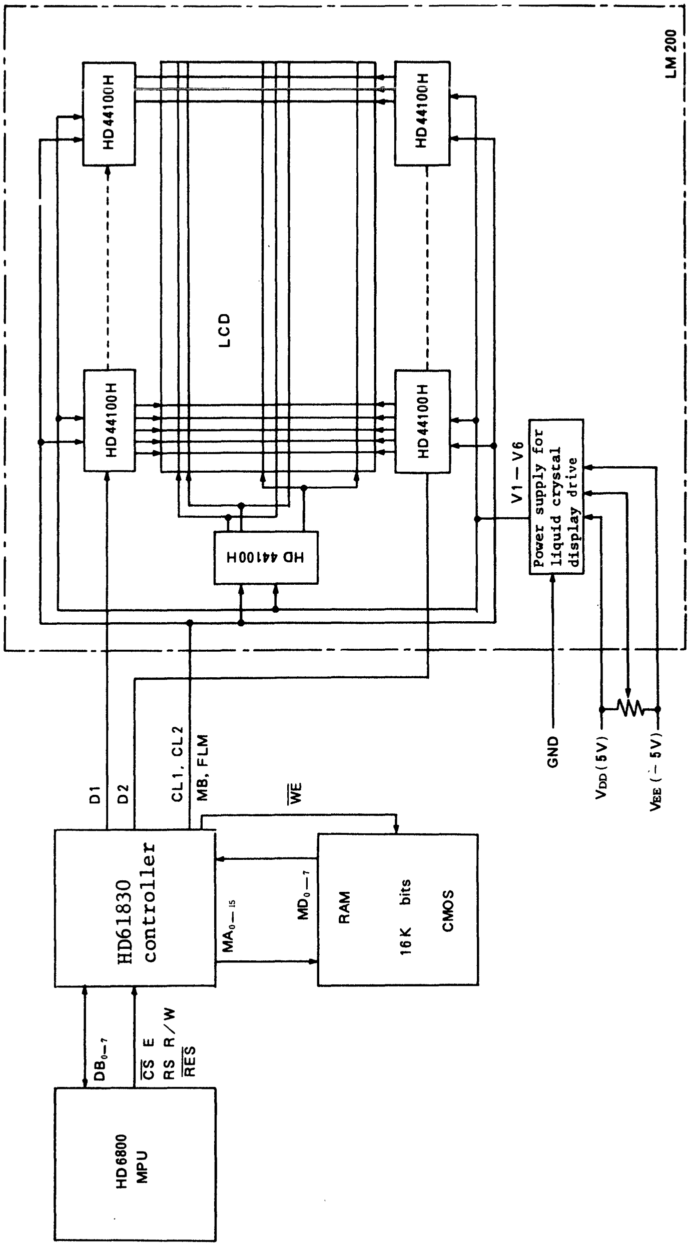
● Internal Character Generator Patterns and Character Codes

Higher 4bit / Lower 4bit	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000		0	@	P	`	p		ー	タ	ミ	α	p
xxxx0001	!	1	A	Q	a	q	。	ア	チ	ム	ä	q
xxxx0010	"	2	B	R	b	r	「	イ	ツ	メ	β	θ
xxxx0011	#	3	C	S	c	s	」	ウ	テ	モ	ε	∞
xxxx0100	$	4	D	T	d	t	、	エ	ト	ヤ	μ	Ω
xxxx0101	%	5	E	U	e	u	・	オ	ナ	ユ	σ	ü
xxxx0110	&	6	F	V	f	v	ヲ	カ	ニ	ヨ	ρ	Σ
xxxx0111	'	7	G	W	g	w	ァ	キ	ヌ	ラ	g	π
xxxx1000	(	8	H	X	h	x	ィ	ク	ネ	リ	√	x̄
xxxx1001	)	9	I	Y	i	y	ゥ	ケ	ノ	ル	⁻¹	y
xxxx1010	*	:	J	Z	j	z	ェ	コ	ハ	レ	j	千
xxxx1011	+	;	K	[	k	{	ォ	サ	ヒ	ロ	ˣ	万
xxxx1100	,	<	L	¥	l	|	ャ	シ	フ	ワ	¢	円
xxxx1101	-	=	M	]	m	}	ュ	ス	ヘ	ン	£	÷
xxxx1110	.	>	N	^	n	→	ョ	セ	ホ	゛	ñ	
xxxx1111	/	?	O	_	o	←	ッ	ソ	マ	゜	ö	█

■APPLICATION (CHARACTER MODE, EXTERNAL CG, CHARACTER FONT 8×8)

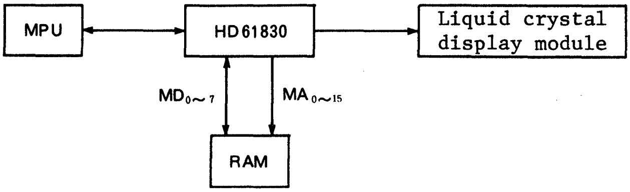


■APPLICATION (GRAPHIC MODE)

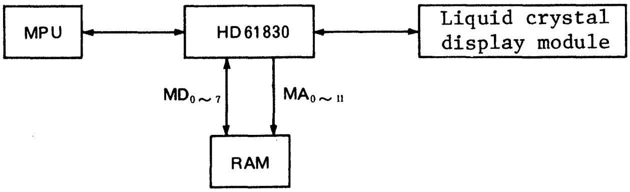


■EXAMPLE OF CONFIGURATION

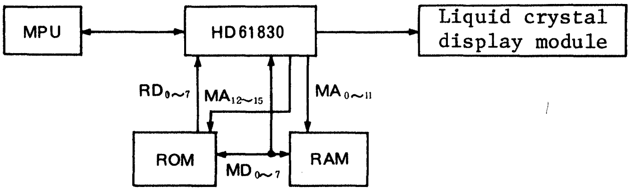
●Graphic Mode



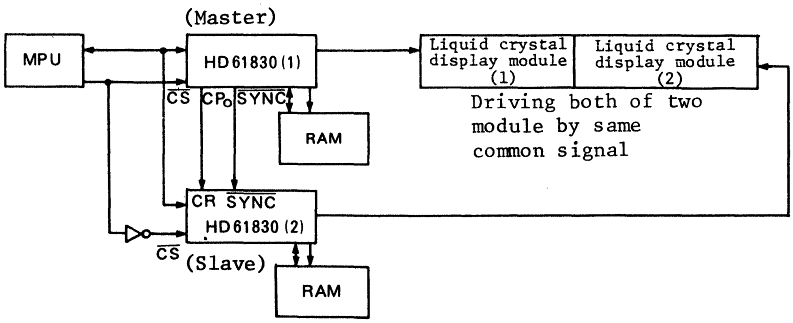
●Character Mode (1) (Internal Character Generator)



●Character Mode (2) (External Character Generator)

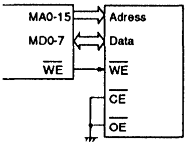
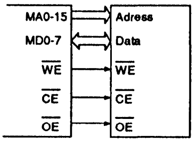
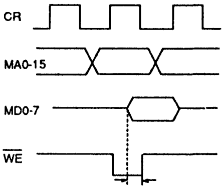
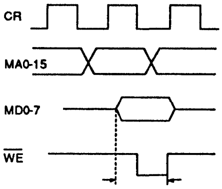
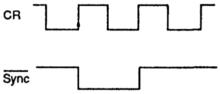
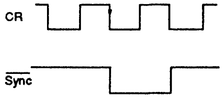


●Parallel Operation



Comparison Chart
The Difference Between HD61830 and HD61830B

The following is the difference between HD61830 and HD61830B

<table>
<tr><th>No.</th><th>Difference</th><th>HD61830</th><th>HD61830B</th></tr>
<tr><td>1</td><td>Display capacity
@ a chip</td><td>64 × 480 dot max. at one chip
fcp 1.1 MHz max.</td><td>200 × 320 dot max. at one chip
fcp 2.4 MHz max.</td></tr>
<tr><td>2</td><td>Oscillator</td><td>Internal clock or external clock</td><td>External clock only</td></tr>
<tr><td>3</td><td>Signal</td><td>HD61830
Display RAM
<table>
<tr><th>Pin No.</th><th>Signal</th></tr>
<tr><td>6</td><td>C</td></tr>
<tr><td>7</td><td>R</td></tr>
<tr><td>8</td><td>CPO</td></tr>
</table>

</td><td>HD61830B
Display RAM
<table>
<tr><th>Pin No.</th><th>Signal</th></tr>
<tr><td>6</td><td>$\overline{CE}$</td></tr>
<tr><td>7</td><td>$\overline{OE}$</td></tr>
<tr><td>8</td><td>NC</td></tr>
</table>

</td></tr>
<tr><td>4</td><td>Memory data setup timing</td><td>
</td><td>
</td></tr>
<tr><td>5</td><td>Timing of $\overline{SYNC}$</td><td>
</td><td>
</td></tr>
<tr><td>6</td><td>Reset ($\overline{RES}$) function</td><td>Up on reset ($\overline{RES}$ is Low)
1. Display OFF mode
2. HP-6 (Horizontal character pich6)
3. Internal Busy Flag is reset
4. Slavemode</td><td>Up on reset ($\overline{RES}$ is Low)
1. Display OFF mode
2. HP-6 (Horizontal character pich6)
3. Internal Busy Flag is reset
4. Slavemode
5. Timing clock for internal CGROM is inhibited while $\overline{RES}$ is low.</td></tr>
</table>

HD61830B
(Dot Matrix Liquid Crystal Graphic Display Controller)

Description

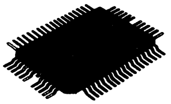
The HD61830B is a dot matrix liquid crystal graphic display controller LSI that stores the display data sent from an 8-bit microcomputer in the external RAM to generate dot matrix liquid crystal driving signals.

It is possible to select the graphic mode in which the 1-bit data of the external RAM corresponds to the ON/OFF state of 1 dot on liquid crystal display and the character mode in which characters are displayed by storing character cods in the external RAM and developing them into the dot patterns with the internal character generator ROM. Both modes can be provided for various applications.

The HD61830B is produced in the CMOS process. Thus, the combination with a CMOS microcomputer can accomplish a liquid crystal display device with lower power dissipation.

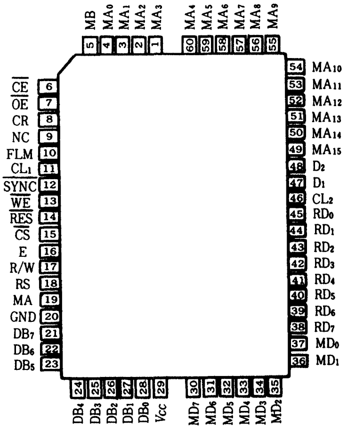
Features

- Dot matrix liquid crystal graphic display controller
- Display control capacity
  - —Graphic mode . . . . 512K dots (2^{16} bytes)
  - —Character mode . . . . 4096 characters (2^{12} characters)
- Internal character generator ROM . . . . . . 7360 bits
  - —160 types of 5 × 7 dot character fonts
  - —32 types of 5 × 11 dot character fonts
  - —Total 192 types
    (Can be extended to 256 types (4K bytes max.) by external ROM)
- Interfaceable to 8-bit MPU
- Display duty (Can be selected by a program)
  - —Static to 1/128 duty selectable
- Various instruction functions
  - —Scroll, Cursor ON/OFF/blink, Character blink, Bit manipulation
- Display method . . . . Selectable A or B types
- Operating frequency 2.4MHz
- Power supply: Single +5V
- CMOS process
- 60-pin flat plastic package



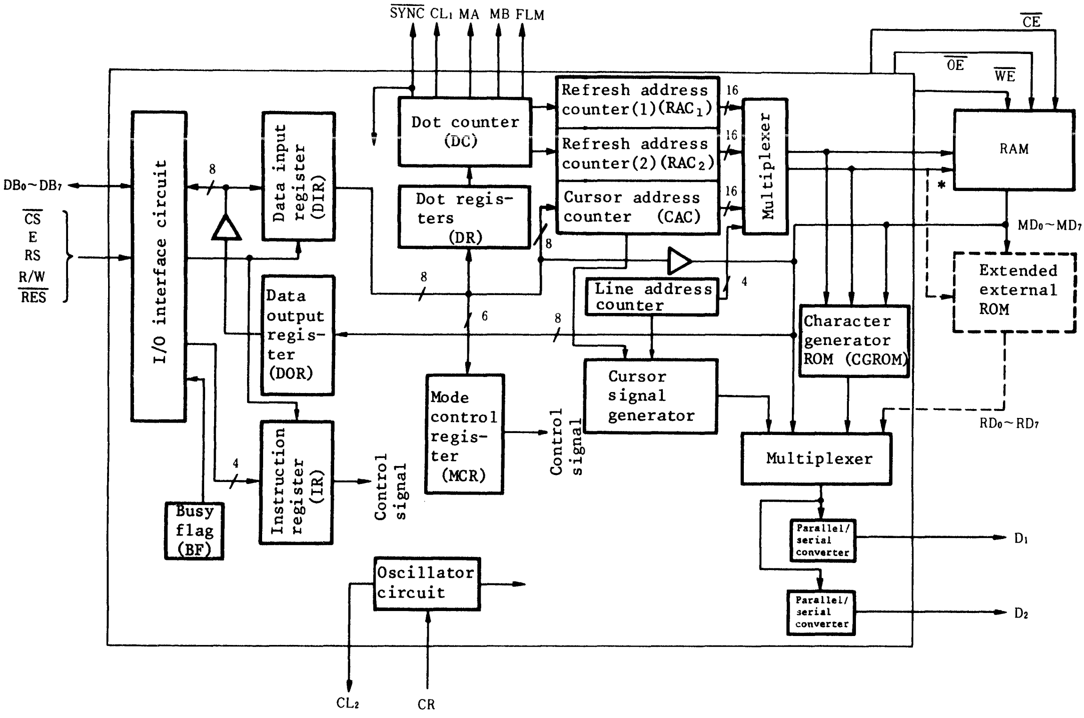
(FP-60)

PIN ARRANGEMENT



(Top View)

BLOCK DIAGRAM



* When extended external ROM is used MA0 ∿ MA11 are applied to RAM, MA12 ∿ MA15 are applied to extended external ROM.

BLOCK FUNCTIONS

Registers

The HD61830B has the five types of registers: instruction register (IR), data input register (DIR), data output register (DOR), dot registers (DR) and mode control register (MCR).

The IR is a 4-bit register which stores the instruction codes for specifying MCR, DR, a start address register, a cursor address register and so on. The lower order 4 bits DB0 to DB3 of data buses are written in it.

The DIR is an 8-bit register used to temporarily store the data written into the external RAM, DR, MCR and so on.

The DOR is an 8-bit register used to temporarily store the data read from the external RAM. Cursor address information is written into the cursor address counter (CAC) through the DIR. When the memory read instruction is set in the IR (latched at the falling edge of E signal), the data of external RAM is read to DOR by an internal operation. The data is transferred to the MPU by reading the DOR with the next instruction (the contents of DOR are output to the data bus when E is at "High" level).

The DR are registers used to store the dot informations such as character pitches and the number of vertical dots and so on. The information sent from the MPU is written into the DR via the DIR.

The MCR is a 6-bit register used to store the data which specifies states of display such as display ON/OFF and cursor ON/OFF/blink etc. The information sent from the MPU is written in it via the DIR.

Busy Flag (BF)

With "1", the busy flag indicates the HD61830B is performing an internal operation. The next instruction cannot be accepted. As shown in Control Instruction (14), the busy flag is output on DB7 under the conditions of RS=1, R/W=1 and E=1. Make sure the busy flag is "0" before writing the next instruction.

Dot Counters (DC)

The dot counters are counters that generate liquid crystal display timing according to the contents of DR.

- Refresh Address Counters (RAC1/RAC2)

The refresh address counters are counters used to control the addresses of external RAM, character generator ROM (CGROM) and extened external ROM having the two types: RAC1 and RAC2. The RAC1 is used for upper half of screen and the RAC2 for lower half. In the graphic mode, 16-bit data is output and used as the address signal of external RAM. In the character mode, the high order 4 bits (MA12 ∿ MA15) are ignored. The 4 bits of line address counter are output instead of it and used as the address of extended ROM.

- Character Generator ROM

The character generator ROM has 7360 bits in total and stores 192 types of character data. A character code (8 bits) from the external RAM and a line code (4 bits) from the line address counter are applied to its address signals, and it outputs 5-bit dot data.

The character font is 5×7 (160 types) or 5×11 (32 types). The use of extended ROM allows 8×16 (256 types max.) to be used.

- Cursor Address Counter

The cursor address counter is a 16-bit counter that can be preset by the instruction. It is used to hold an address when the data of external RAM is read or written (when display dot data or a character code is read or written). The value of cursor address counter is automatically increased by 1 after the display data is read or written and after the Set/Clear Bit instruction is executed.

- Cursor Signal Generator

The cursor can be displayed by the instruction in the character mode. The cursor is automatically generated on the display specified by the cursor address and cursor position.

- Parallel/Serial Conversion

The parallel data sent from the external RAM, character generator ROM or extended ROM is converted into serial data by two parallel/serial conversion circuits and transferred to the liquid crystal driver circuits for upper screen and lower screen simultaneously.

TERMINAL FUNCTIONS

Name	Function
DB0∿7	Data bus ... Three-state I/O common terminal Data is transferred to MPU through DB0 to DB7.
$\overline{\text{CS}}$	Chip select ... Selected state with $\overline{\text{CS}}$=0.
R/W	Read/Write ... R/W=1 ... MPU ← HD61830B R/W=0 ... MPU → HD61830B
RS	Register select ... RS=1 ... Instruction register RS=0 ... Data register
E	Enable ... Data is written at the fall of E. Data can be read while E is 1.
CR	External clock input.
$\overline{\text{RES}}$	Reset ... $\overline{\text{RES}}$=0 results in display OFF, slave mode and Hp=6.
MA0∿15	External RAM address output In character mode, the line code for external CG is output through MA12 to MA15 ("0": Character 1st line, "F": Character 16th line).
MD0∿7	Display data bus ... Three-state I/O common terminal.
RD0∿7	ROM data input ... Dot data from external character generator is input.
$\overline{\text{WE}}$	Write enable ... Write signal for external RAM.
CL2	Display data shift clock for LCD drivers.
CL1	Display data latch signal for LCD drivers.
FLM	Frame signal for display synchronization.
MA	Signal for converting liquid crystal driving signal into AC, A type.
MB	Signal for converting liquid crystal driving signal into AC, B type.
D1, D2	Display data serial output D1 ... For upper half of screen D2 ... For lower half of screen
$\overline{\text{SYNC}}$	Synchronous signal for parallel operation. Three-state I/O common terminal (with pull-up MOS). Master ... Synchronous signal is output. Slave .... Synchronous signal is input.

-to be continued

Name	Function
$\overline{CE}$	Chip enable $\overline{CE}$=0 ... Chip enable make external RAM in active.
$\overline{OE}$	Output enable $\overline{OE}$=1 ... Output enable informs external RAM that HD61830B requires data bus.
NC	Unused terminal. Don't connect any wires to this terminal.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	-0.3 ∿ +7.0	V	1,2
Terminal voltage	V_T	-0.3 ∿ V_{CC}+0.3	V	1,2
Operating temperature	Topr	-20 ∿ +75	°C	
Storage temperature	T_{stg}	-55 ∿ +125	°C	

Note 1: All voltage is referred to GND=0V.

Note 2: If LSI's are used beyond absolute maximum ratings, they may be permanently destroyed. We strongly recommend you to use the LSI's within electrical characteristic limits for normal operation, because use beyond these conditions will cause malfunction and poor reliability.

■ ELECTRICAL CHARACTERISTICS

(V_{CC}=5V±10%, GND=0V, Ta=-20∿+75°C)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit	Note
Input "High" voltage (TTL)	V_{IH}		2.2	-	V_{CC}	V	1
Input "Low" voltage (TTL)	V_{IL}		0	-	0.8	V	2
Input "High" voltage	V_{IHR}		3.0	-	V_{CC}	V	3
Input "High" voltage (CMOS)	V_{IHC}		$0.7V_{CC}$	-	V_{CC}	V	4
Input "Low" voltage (CMOS)	V_{ILC}		0	-	$0.3V_{CC}$	V	4
Output "High" voltage (TTL)	V_{OH}	$-I_{OH}$=0.6mA	2.4	-	V_{CC}	V	5
Output "Low" voltage (TTL)	V_{OL}	I_{OL}=1.6mA	0	-	0.4	V	5
Output "High" voltage (CMOS)	V_{OHC}	$-I_{OH}$=0.6mA	V_{CC}-0.4	-	V_{CC}	V	6
Output "Low" voltage (CMOS)	V_{OLC}	I_{OL}=0.6mA	0	-	0.4	V	6
Input leakage current	I_{IN}	V_{IN}=0∿V_{CC}	-5	-	5	μA	7
Three-state leakage current	I_{TSL}	V_{OUT}=0∿V_{CC}	-10	-	10	μA	8
Pull-up current	I_{PL}	Vin=GND	2	10	20	μA	9
Power dissipation	P_W	External clock fcp=2.4MHz	-	-	50	mW	10

Note 1: Applied to input terminals and I/O common terminals, except terminals $\overline{SYNC}$, CR and $\overline{RES}$.

Note 2: Applied to input terminals and I/O common terminals, except terminals $\overline{SYNC}$ and CR.

Note 3: Applied to terminal $\overline{RES}$.

Note 4: Applied to terminals $\overline{SYNC}$ and CR.

Note 5: Applied to terminals DB0∿DB7, $\overline{WE}$, MA0∿MA15, $\overline{OE}$, $\overline{CE}$, and MD0∿MD7.

Note 6: Applied to terminals $\overline{SYNC}$, FLM, CL1, CL2, D1, D2, MA and MB.

Note 7: Applied to input terminals.

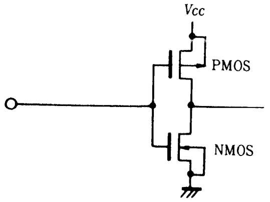
Note 8: Applied to I/O common terminals. However, the current which flows into the output drive MOS is excluded.

Note 9: Applied to $\overline{SYNC}$, DB0∿DB7, and RD0∿RD7.

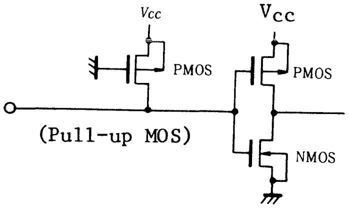
Note 10: The current which flows into the input and output circuits is excluded. When the input of CMOS is in the intermediate level, current flows through the input circuit, resulting in the increase of power supply current. To avoid this, input must be fixed at high or low.

- Shape of Input Terminal

Applicable terminal: $\overline{\text{CS}}$, E, RS, R/W, $\overline{\text{RES}}$, CR (Without pull-up MOS)

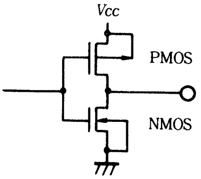


Applicable terminal: RD0∿RD7 (With pull-up MOS)



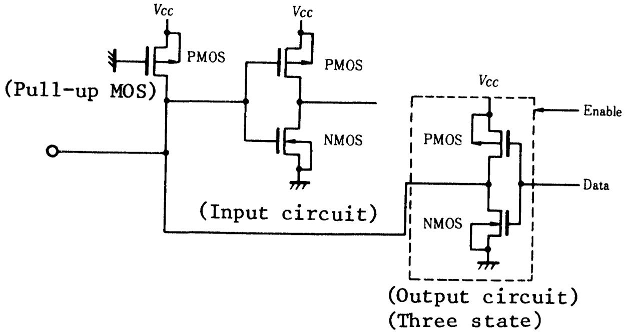
- Shape of Output Terminal

Applicable terminal: CL1, CL2, MA, MB, FLM, D1, D2, $\overline{\text{WE}}$, $\overline{\text{OE}}$, $\overline{\text{CE}}$, MA0∿MA15



- Shape of I/O Common Terminal

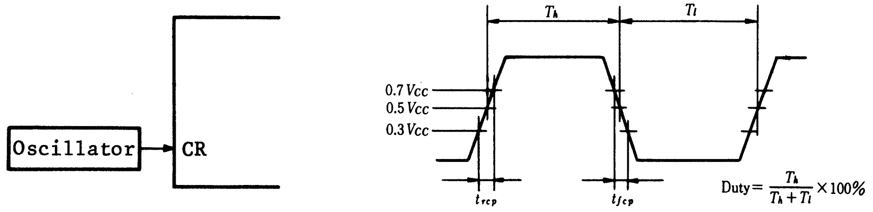
Applicable terminal: DB0∿DB7, $\overline{\text{SYNC}}$, MD0∿MD7 (MD0∿MD7 have no pull-up MOS)



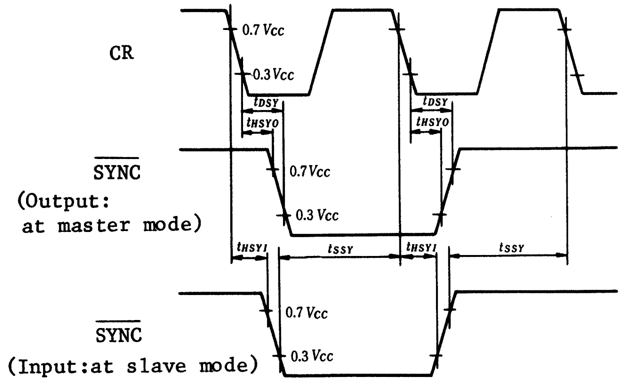
- Clock Operation

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit	Note
External clock operating frequency	f_{cp}		100	-	2400	kHz	1
External clock duty	Duty		47.5	50	52.5	%	1
External clock rise time	t_{rcp}		-	-	25.0	ns	1
External clock fall time	t_{fcp}		-	-	25.0	ns	1
$\overline{\text{SYNC}}$ output hold time	t_{HSYO}		30	-	-	ns	2, 3
$\overline{\text{SYNC}}$ output delay time	t_{DSY}		-	-	210	ns	2, 3
$\overline{\text{SYNC}}$ input hold time	t_{HSYI}		10	-	-	ns	2
$\overline{\text{SYNC}}$ input set-up time	t_{SSY}		-	-	180	ns	2

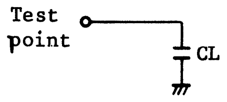
Note 1: Applied to external clock input terminal.



Note 2: Applied to $\overline{\text{SYNC}}$ terminal.

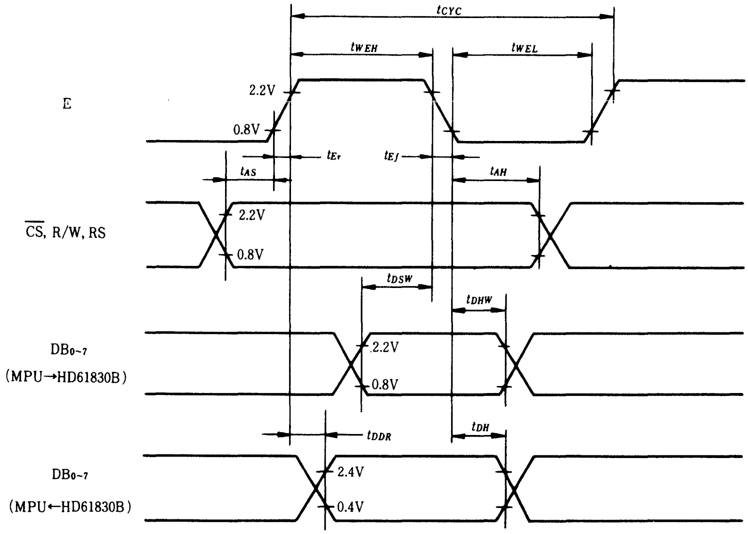


Note 3: Testing load circuit.



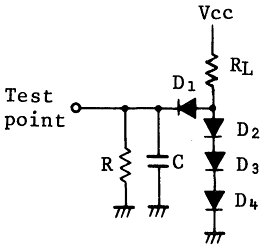
C_L=30pF
(C_L includes jig capacitance)

- Bus Read/Write Operation (Interface to MPU)



Item		Symbol	Min.	Typ.	Max.	Unit
Enable cycle time		t_{CYC}	1.0	-	-	μs
Enable pulse width	"High" level	t_{WEH}	0.45	-	-	μs
	"Low" level	t_{WEL}	0.45	-	-	μs
Enable rise time		t_{Er}	-	-	25	ns
Enable fall time		t_{Ef}	-	-	25	ns
Setup time		t_{AS}	140	-	-	ns
Data setup time		t_{DSW}	225	-	-	ns
Data delay time		t_{DDR}	-	-	225	ns(Note)
Data hold time		t_{DHW}	10	-	-	ns
Address hold time		t_{AH}	10	-	-	ns
Data hold time		t_{DH}	20	-	-	ns

Note: The following load circuit is connected for specification:



R_L = 2.4kΩ

R = 11kΩ

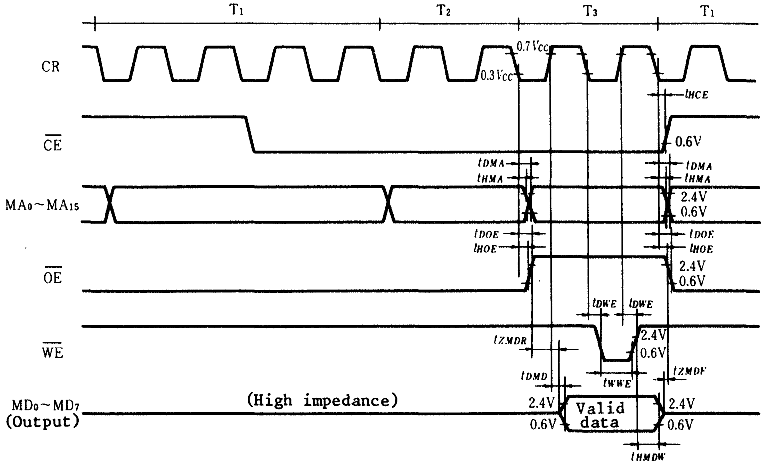
C = 130 pF (C includes jig capacitance)

Diodes D1 to D4: 1S2074 Ⓗ

- Interface to External RAM and ROM

Item	Symbol	Test condition	Min.	Typ.	Max.	unit	Note
MA0∿MA15 delay time	t_{DMA}		-	-	300	ns	1, 2, 3
MA0∿MA15 hold time	t_{HMA}		40	-	-	ns	1, 2, 3
$\overline{CE}$ delay time	t_{DCE}		-	-	300	ns	1, 2, 3
$\overline{CE}$ hold time	t_{HCE}		40	-	-	ns	1, 2, 3
$\overline{OE}$ delay time	t_{DOE}		-	-	300	ns	1, 3
$\overline{OE}$ hold time	t_{HOE}		40	-	-	ns	1, 3
MD output delay time	t_{DMD}		-	-	150	ns	1, 3
MD output hold time	t_{HMDW}		10	-	-	ns	1, 3
$\overline{WE}$ delay time	t_{DWE}		-	-	150	ns	1, 3
$\overline{WE}$ clock pules width	t_{WWE}		150	-	-	ns	1, 3
MD output high impedance time (1)	t_{ZMDF}		10	-	-	ns	1, 3
MD output high impedance time (2)	t_{ZMDR}		50	-	-	ns	1, 3
RD data set-up time	t_{SRD}		50	-	-	ns	2
RD data hold time	t_{HRD}		40	-	-	ns	2
MD data set-up time	t_{SMD}		50	-	-	ns	2
MD data hold time	t_{HMD}		40	-	-	ns	2

Note 1: RAM write timing

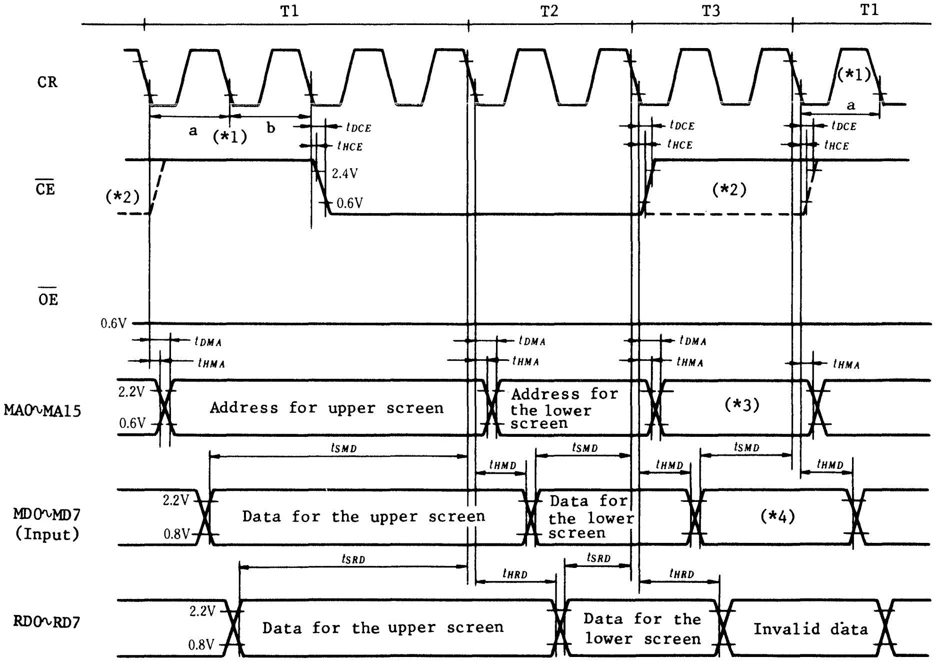


T1: Memory data refresh timing for upper screen

T2: Memory data refresh timing for lower screen

T3: Memory read/write timing

Note 2: ROM/RAM read timing



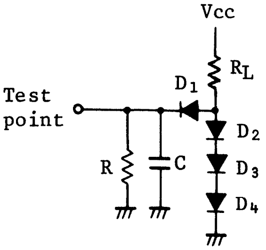
(*1) This figure shows the timing in the case of Hp=8.
In the case of Hp=7, time shown by "b" becomes zero., and in the case of Hp=6, time shown by "a" and "b" becomes zero. Therefore, the number of clock pulse during T1 become 4, 3 or 2 in the case of Hp=8, Hp=7 or Hp=6 respectively.

(*2) The waveform in the case of instruction with memory read is shown with a dash line. In other case, the waveform shown with a solid line is generated.

(*3) When the instruction with RAM read/write is excuted, the value of cursor address is output. In other case, invalid data is output.

(*4) When the instruction with RAM read is excuted, HD61830B latch the data at this timing. In other case, this data is invalid.

Note 3: Test load circuit



R_L=2.4kΩ

R =11kΩ

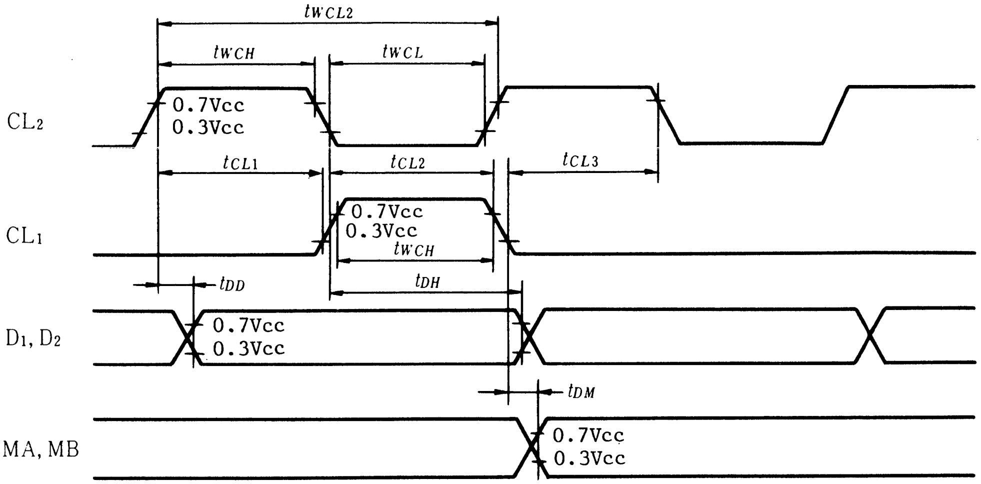
C =50 pF (C includes jig capacitance)

Diodes D1 to D4: 1S2074Ⓗ

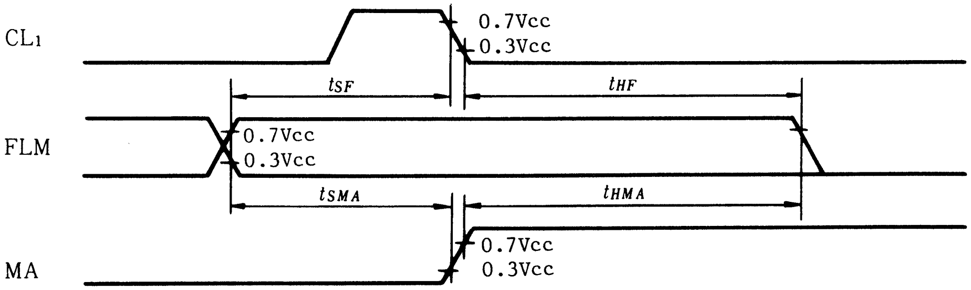
- Data Transfer to Driver LSI

Items	Symbol	Test condition	Min.	Typ.	Max	Unit	Note
Clock cycle time	t_{WCL2}		416	-	-	ns	1, 3
Clock pulse width (High level)	t_{WCH}		150	-	-	ns	1, 3
Clock pulse width (Low level)	t_{WCL}		150	-	-	ns	1, 3
Data delay time	t_{DD}		-	-	50	ns	1, 3
Data hold time	t_{DH}		100	-	-	ns	1, 3
Clock phase difference (1)	t_{CL1}		100	-	-	ns	1, 3
Clock phase difference (2)	t_{CL2}		100	-	-	ns	1, 3
Clock phase difference (3)	t_{CL3}		100	-	-	ns	1, 3
MA, MB delay time	t_{DM}		-200	-	200	ns	1, 3
FLM set-up time	t_{SF}		400	-	-	ns	2, 3
FLM hold time	t_{HF}		1000	-	-	ns	2, 3
MA set-up time	t_{SMA}		400	-	-	ns	2, 3
MA hold time	t_{HMA}		1000	-	-	ns	2, 3

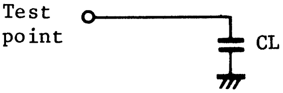
Note 1:



Note 2:



Note 3: Test load circuit



CL=100pF (CL includes jig capacitance)

- Display Control Instructions

Display is controlled by writing data into the instruction register and 13 data registers. The RS signal distinguishes the instruction register from the data registers. 8-bit data is written into the instruction register with RS=1, and the code of data register is specified. After that, the 8-bit data is written in the data register and the specified instruction is executed with RS=0.

During the execution of the instruction, no new instruction can be accepted. Since the busy flag is set during this, read the busy flag and make sure it is 0 before writing the next instruction.

(1) Mode control

Code $"00" (hexadecimal) written into the instruction register specifies the mode control register.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	0
Mode control reg.	0	0	0	0	Mode data					

DB5	DB4	DB3	DB2	DB1	DB0	Cursor/blink	CG	Graphic/character display
1/0	1/0	0	0	0	0	Cursor OFF	Internal CG	Character display (Character mode)
		0	1			Cursor ON		
		1	0			Cursor OFF, character blink		
		1	1			Cursor blink		
		0	0		1	Cursor OFF	External CG	
		0	1			Cursor ON		
		1	0			Cursor OFF, character blink		
		1	1			Cursor blink		
		0	0	1	0			Graphic mode
Display ON/OFF	Master/slave	Blink	Cursor	Graphic/character mode	Ext./Int.CG			

Master/slave:
1: Master mode
0: Slave mode

Display ON/OFF:
1: Display ON
0: Display OFF

(2) Set character pitch

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	1
Character pitch reg.	0	0	(V_p-1) binary				0	(H_p-1) binary		

Vp indicates the number of vertical dots per character. The space between the vertically-displayed characters is considered for determination. This value is meaningful only during character display (in the character mode) and becomes invalid in the graphic mode.

The Hp indicates the number of horizontal dots per character in display, including the space between horizontally-displayed characters. In the graphic mode, the Hp indicates the number of bits of 1-byte display data to be displayed.

There are three Hp values.

Hp	DB2	DB1	DB0	
6	1	0	1	Horizontal character pitch 6
7	1	1	0	Horizontal character pitch 7
8	1	1	1	Horizontal character pitch 8

(3) Set number of characters

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	0
Number-of-characters reg.	0	0	0	$(H_N - 1)$ binary						

H_N indicates the number of horizontal characters in the character mode or the number of horizontal bytes in the graphic mode. If the total sum of horizontal dots on the screen is taken as n,

$$n = Hp \times H_N$$

H_N can be set with an even number of 2 to 128 (decimal).

(4) Set number of time division (inverse of display duty ratio)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	1
Number-of-time shares reg.	0	0	0	(Nx - 1) binary						

Nx indicates the number of time division in multiplex display.

1/Nx is a display duty ratio.

A value of 1 to 128 (decimal) can be set to Nx.

(5) Set cursor position

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	1	0	0
Cursor position reg.	0	0	0	0	0	0	(Cp - 1) binary			

Cp indicates the position in a character where the cursor is displayed in the character mode. For example, in 5×7 dot font, the cursor is displayed under a character by specifying Cp=8 (decimal). The cursor horizontal length is equal to the horizontal character pitch Hp. A value of 1 to 16 (decimal) can be set to Cp. If a smaller value than the number of vertical character pitches Vp is set (Cp≦Vp), and a character is overlapped with the cursor, the cursor has higher priority of display (at cursor display ON). If Cp is greater than Vp, no cursor is displayed. The cursor horizontal length is equal to Hp.

(6) Set display start low order address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	0
Display start address reg. (low order byte)	0	0	(Start low order address) binary							

(7) Set display start high order address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	1
Display start address reg. (high order byte)	0	0	(Start high order address) binary							

These instructions cause display start addresses to be written in the display start address registers. The display start address indicates a RAM address at which the data displayed at the top left end on the screen is stored. In the graphic mode, the start address is composed of high/low order 16 bits. In the character display, it is composed of the lower 4 bits of high order address ($DB_3 \sim DB_0$) and 8 bits of low order address. The upper 4 bits of high order address are ignored.

(8) Set cursor address (low order) (RAM write low order address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	0
Cursor address counter (low order byte)	0	0	(Cursor low order address) binary							

(9) Set cursor address (high order) (RAM write high order address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	1
Cursor address counter (high order byte)	0	0	(Cursor high order address) binary							

These instructions cause cursor addresses to be written in the cursor address counters. The cursor address indicates an address for sending or receiving display data and character codes to or from the RAM. Namely, data at address specified by the cursor address are read/written. In the character mode, the cursor is displayed at the digit specified by the cursor address.

A cursor address consists of the low-order address (8 bits) and the high-order address (8 bits). Satisfy the following requirements. When setting the cursor address.

1.	When you want to rewrite (set) both the low order address and the high order address.	Set the low order address and then set the high order address.
2.	When you want to rewrite only the low order address.	Don't fail to set the high order address again after setting the low order address.
3.	When you want to rewrite only the high order address.	Set the high order address. You don't have to set the low order address again.

The cursor address counter is a 16 bit up-counter with SET and RESET functions. When the bit N changes from 1 to 0, the bit N+1 is added by 1. When setting the low order address, the LSB (bit 1) of the high order address is added by 1 if the MSB (bit 8) of the low order address changes from 1 to 0. Therefore, set both the low order address and the high order address as shown in above table.

(10) Write display data

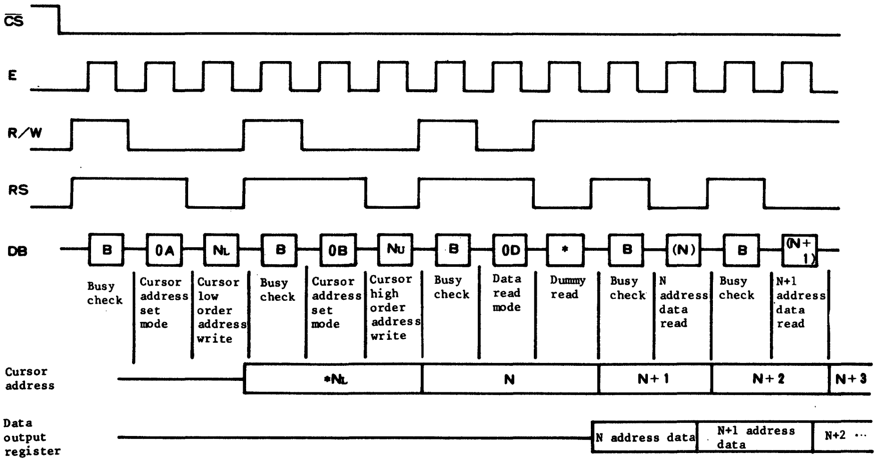
Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	0
RAM	0	0	MSB (pattern data, character code) LSB							

After the code $'0C' is written into the instruction register with RS=1, 8 bit data with RS=0 should be written into the data register. This data is transferred to the RAM specified by the cursor address as display data or character code. The cursor address is increased by 1 after this operation.

(11) Read display data

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	1
RAM	1	0	MSB (pattern data, character code) LSB							

Data can be read from the RAM with RS=0 after writing code $'0D" into the instruction register. The read procedure is as follows:



This instruction outputs the contents of data output register on Data Bus (DB0 to DB7) and then transfers RAM data specified by a cursor address to the data output register, also increasing the cursor address by 1. After setting the cursor address, correct data is not output at the first read but at the second time. Thus, make one dummy read when reading data after setting the cursor address.

(12) Clear bit

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	0
Bit clear reg.	0	0	0	0	0	0	0	(N_B-1)binary		

(13) Set bit

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	1
Bit set reg.	0	0	0	0	0	0	0	(N_B-1) binary		

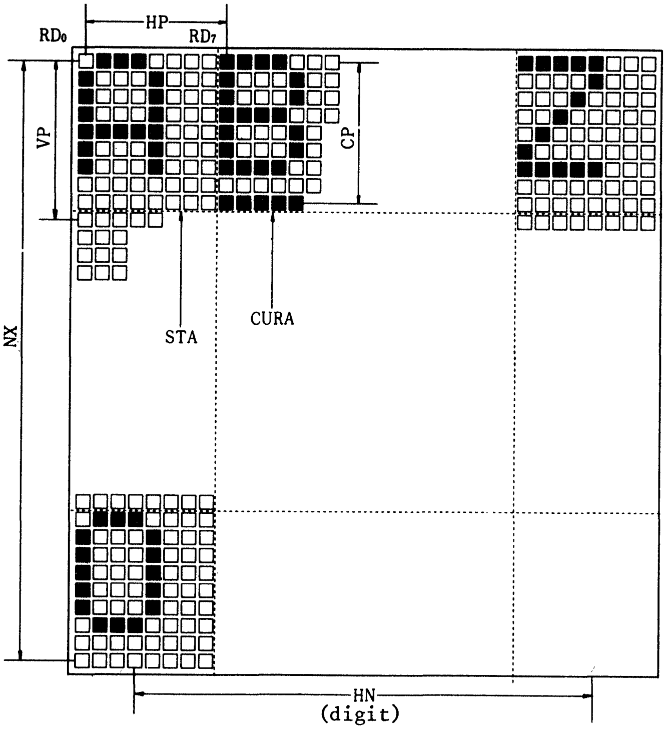
The Clear/Set Bit instruction sets 1 bit in a byte of display data RAM to 0 or 1, respectively. The position of the bit in a byte is specified by N_B and RAM address is specified by cursor address. After the execution of the instruction, the cursor address is automatically increased by 1. N_B is a value of 1 to 8. $N_B=1$ and $N_B=8$ indicates LSB and MSB, respectively.

(14) Read busy flag

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Busy flag	1	1	1/0	*						

When the read mode is set with RS=1, the busy flag is output to DB7. The busy flag is set to 1 during the execution of any of instructions (1) to (13). After the execution, it is set to 0. The next instruction can be accepted. No instruction can be accepted when busy flag=1. Before executing an instruction or writing data, perform a busy flag check to make sure the busy flag is 0. When data is written in the register (RS=1), busy flag doesn't change. Thus, no busy flag check is required just after the write operation into the instruction register with RS=1.

The busy flag can be read without specifying any instruction register.



Symbol	Name	Meaning	Value
Hp	Horizontal character Pitch	Lateral character pitch	6 to 8 dots
H_N	Number of horizontal characters	Number of lateral characters per line (number of digits) in the character mode or number of bytes per line in the graphic mode.	2 to 128 digits (an even number)
Vp	Vertical character pitch	Longitudinal character pitch	1 to 16 dots
Cp	Cursor position	Line number on which the cursor can be displayed	1 to 16 lines
Nx	Number of time division	Inverse of display duty ratio	1 to 128 lines

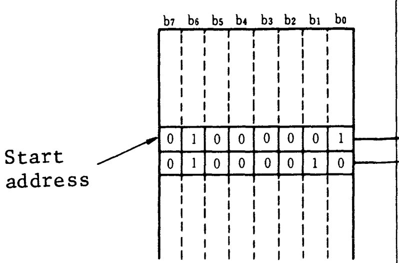
Note: if the number of vertical dots on screen is taken as m, and the number of horizontal dots as n,

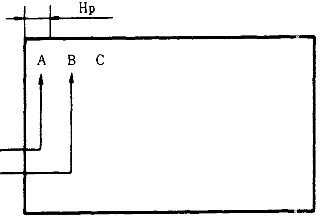
$1/m = 1/Nx$ = display duty ratio

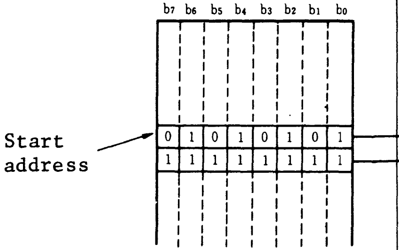
$n = Hp \times H_N$, m/Vp = Number of display lines

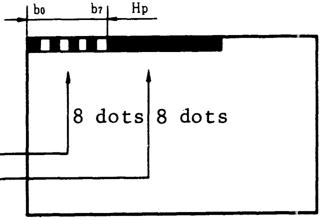
$Cp \leqq Vp$

● Display Mode

<table>
<tr><th>Display mode</th><th>Display data from MPU</th><th>RAM</th><th>Liquid crystal display panel</th></tr>
<tr><td>Character display</td><td>Character code (8 bits)</td><td>


</td><td>


Hp: 6, 7 or 8 dots
</td></tr>
<tr><td>Graphic</td><td>Display pattern (8 bits)</td><td>


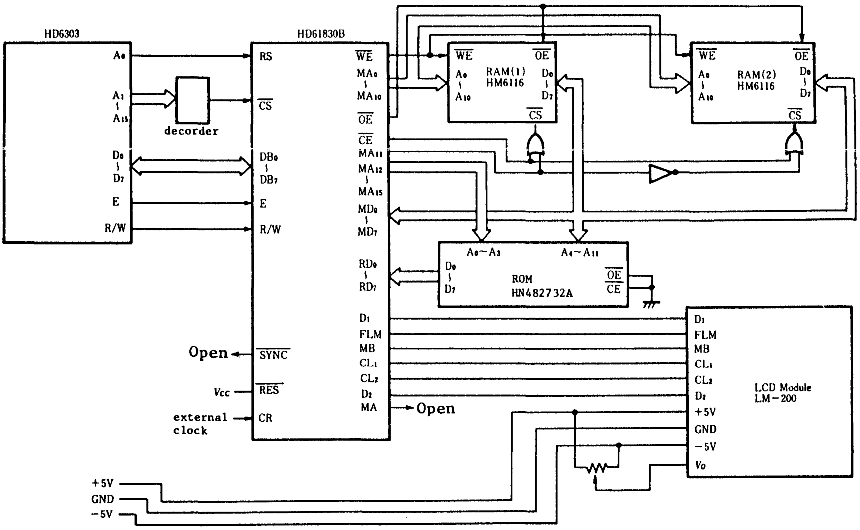
</td><td>


Hp: 8 dots
</td></tr>
</table>

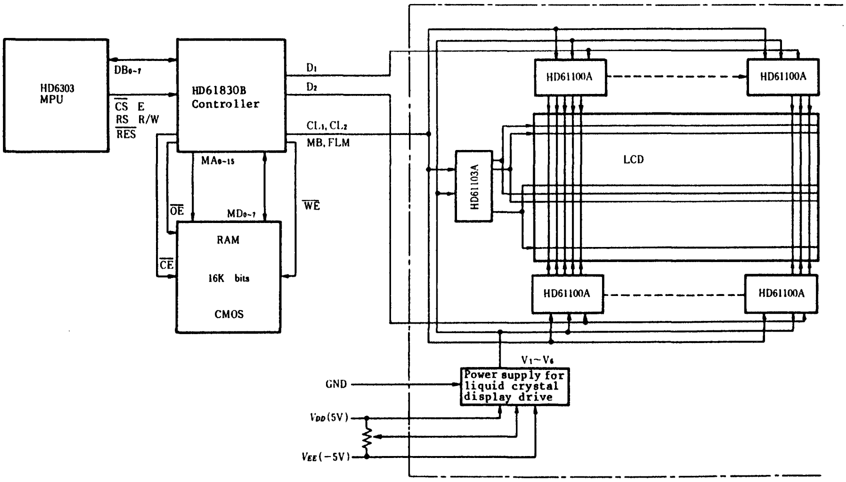
- Internal Character Generator Patterns and Character Codes

Lower 4 bit \ Higher 4 bit	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000		0	@	P	`	p		ｰ	ﾀ	ﾐ	α	p
xxxx0001	!	1	A	Q	a	q	｡	ｱ	ﾁ	ﾑ	ä	q
xxxx0010	"	2	B	R	b	r	｢	ｲ	ﾂ	ﾒ	β	θ
xxxx0011	#	3	C	S	c	s	｣	ｳ	ﾃ	ﾓ	ε	∞
xxxx0100	$	4	D	T	d	t	､	ｴ	ﾄ	ﾔ	μ	Ω
xxxx0101	%	5	E	U	e	u	･	ｵ	ﾅ	ﾕ	σ	ü
xxxx0110	&	6	F	V	f	v	ｦ	ｶ	ﾆ	ﾖ	ρ	Σ
xxxx0111	'	7	G	W	g	w	ｧ	ｷ	ﾇ	ﾗ	g	π
xxxx1000	(	8	H	X	h	x	ｨ	ｸ	ﾈ	ﾘ	√	x̄
xxxx1001	)	9	I	Y	i	y	ｩ	ｹ	ﾉ	ﾙ	⁻¹	y
xxxx1010	*	:	J	Z	j	z	ｪ	ｺ	ﾊ	ﾚ	j	千
xxxx1011	+	;	K	[	k	{	ｫ	ｻ	ﾋ	ﾛ	ˣ	万
xxxx1100	,	<	L	¥	l	|	ｬ	ｼ	ﾌ	ﾜ	¢	円
xxxx1101	-	=	M	]	m	}	ｭ	ｽ	ﾍ	ﾝ	£	÷
xxxx1110	.	>	N	^	n	→	ｮ	ｾ	ﾎ	ﾞ	ñ	
xxxx1111	/	?	O	_	o	←	ｯ	ｿ	ﾏ	ﾟ	ö	█

APPLICATION (CHARACTER MODE, EXTERNAL CG, CHARACTER FONT 8X8)

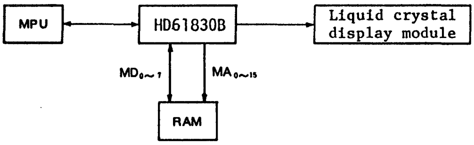


APPLICATION (GRAPHIC MODE)

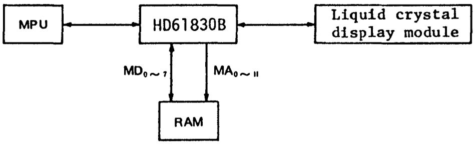


EXAMPLE OF CONFIGURATION

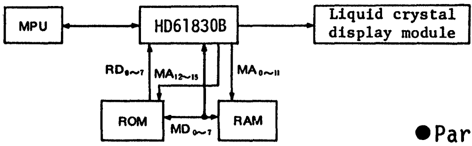
●Graphic Mode



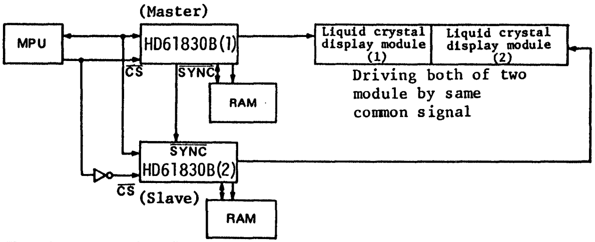
●Character Mode (1) (Internal Character Generator)



●Character Mode (2) (External Character Generator)



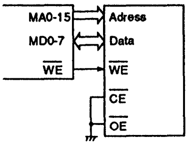
●Parallel Operation

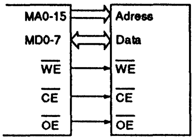

(Master)
MPU
HD61830B(1)
Liquid crystal display module (1)
Liquid crystal display module (2)
CS
SYNC
RAM
SYNC
HD61830B(2)
CS
(Slave)
RAM

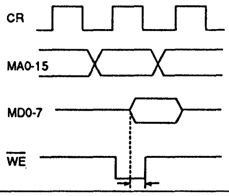
Driving both of two module by same common signal

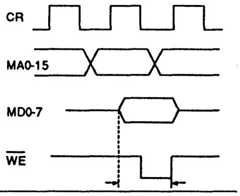
Comparison Chart
The Difference Between HD61830 and HD61830B

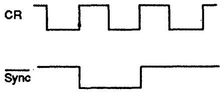
The following is the difference between HD61830 and HD61830B

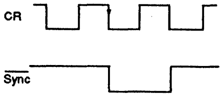
<table>
<tr><th>No.</th><th>Difference</th><th>HD61830</th><th>HD61830B</th></tr>
<tr><td>1</td><td>Display capacity @ a chip</td><td>64 × 480 dot max. at one chip
fcp 1.1 MHz max.</td><td>200 × 320 dot max. at one chip
fcp 2.4 MHz max.</td></tr>
<tr><td>2</td><td>Oscillator</td><td>Internal clock or external clock</td><td>External clock only</td></tr>
<tr><td>3</td><td>Signal</td><td>
<table>
<tr><th>Pin No.</th><th>Signal</th></tr>
<tr><td>6</td><td>C</td></tr>
<tr><td>7</td><td>R</td></tr>
<tr><td>8</td><td>CPO</td></tr>
</table>
HD61830
Display RAM


</td><td>
<table>
<tr><th>Pin No.</th><th>Signal</th></tr>
<tr><td>6</td><td>$\overline{CE}$</td></tr>
<tr><td>7</td><td>$\overline{OE}$</td></tr>
<tr><td>8</td><td>NC</td></tr>
</table>
HD61830B
Display RAM


</td></tr>
<tr><td>4</td><td>Memory data setup timing</td><td>


</td><td>


</td></tr>
<tr><td>5</td><td>Timing of $\overline{\text{SYNC}}$</td><td>


</td><td>


</td></tr>
<tr><td>6</td><td>Reset ($\overline{\text{RES}}$) function</td><td>Up on reset ($\overline{\text{RES}}$ is Low)
1. Display OFF mode
2. HP-6 (Horizontal character pich6)
3. Internal Busy Flag is reset
4. Slavemode</td><td>Up on reset ($\overline{\text{RES}}$ is Low)
1. Display OFF mode
2. HP-6 (Horizontal character pich6)
3. Internal Busy Flag is reset
4. Slavemode
5. Timing clock for internal CGROM is inhibited while $\overline{\text{RES}}$ is low.</td></tr>
</table>

HD63645/HD64645

LCD Timing Controller (LCTC)

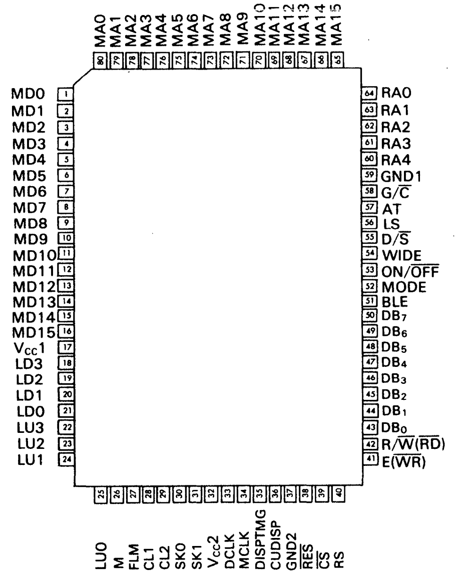
Description

The HD63645/HD64645 LCTC is a control LSI for large size dot matrix liquid crystal displays. The LCTC is software compatible with the HD6845 CRTC, since its programming method of internal registers and memory addresses is based on the CRTC. A display system can be easily converted from a CRT to an LCD.

The LCTC offers a variety of functions and performance features such as vertical and horizontal scrolling, and various types of character attribute functions such as reverse video, blinking, nondisplay (white or black), and an OR function for simple superimposition of character and graphic displays. The LCTC also provides DRAM refresh address output.

A compact LCD system with a large screen can be configured by connecting the LCTC with the HD61104 (column driver) and the HD61105 (common driver) by utilizing 4-bit × 2 data outputs. Power dissipation has been lowered by adopting the CMOS process.

Pin Arrangement



( ) is for HD64645

Features

- Software compatible with the HD6845 CRTC
- Programmable screen size :
  - —Up to 1024 dots (height)
  - —Up to 4096 dots (width)
- High-speed data transfer :
  - —Up to 20 Mbits/sec in character mode
  - —Up to 40 Mbits/sec in graphic mode
- Selectable single or dual screen configuration
- Programmable multiplexing duty ratio: static to 1/512 duty cycle
- Programmable character font :
  - —1-32 dots (height)
  - —8 dots (width)
- Versatile character attributes: reverse video, blinking, nondisplay (white), nondisplay (black)
- OR function: superimposing characters and graphics display
- Cursor with programmable height, blink rate, display position, and on/off switch
- Vertical smooth scrolling and horizontal scrolling by the character
- Versatile display modes programmable by mode register or external pins: display on/off, graphic or character, normal or wide, attributes, and blink enable
- Refresh address output for dynamic RAM
- 4- or 8-bit parallel data transfer between LCTC and LCD driver
- Recommended LCD driver: HD61104 (column) and HD61105 (common), HD66106
- CPU interface: 68 family (HD63645), 80 family (HD64645)
- CMOS process
- Single +5 V ±10%
- 80-pin plastic QFP (FP-80)

Ordering Information

Type No.	Bus Timing	Bus Interface	Package
HD63645	2 MHz	68 System	80-pin Plastic QFP (FP-80)
HD64645	4 MHz	80 System	80-pin Plastic QFP (FP-80)
HD64646	4MHz	80 System	80-pin Plastic QFP (FP-80A)

Note: See HD64646 data sheet is this data book.

Pin Description

Symbol	Pin Number	Name	I/O
$V_{CC}1$, $V_{CC}2$	17, 32	V_{CC}	—
GND1, GND2	37, 59	Ground	—
LU0-LU3	22-25	LCD Up Panel Data 0-3	O
LD0-LD3	18-21	LCD Down Panel Data 0-3	O
CL1	28	Clock One	O
CL2	29	Clock Two	O
FLM	27	First Line Marker	O
M	26	M	O
MA0-MA15	65-80	Memory Address 0-15	O
RA0-RA4	60-64	Raster Address 0-4	O
MD0-MD7	1-8	Memory Data 0-7	I
MD8-MD15	9-16	Memory Data 8-15	I
DB_0-DB_7	43-50	Data Bus 0-7	I/O
$\overline{CS}$	39	Chip Select	I
E	41	Enable (HD63645 Only)	I
R/$\overline{W}$	42	Read/Write (HD63645 Only)	I
$\overline{WR}$	41	Write (HD64645 Only)	I
$\overline{RD}$	42	Read (HD64645 Only)	I
RS	40	Register Select	I
$\overline{RES}$	38	Reset	I
DCLK	33	D Clock	I
MCLK	34	M Clock	O
DISPTMG	35	Display Timing	O
CUDISP	36	Cursor Display	O
SK0	30	Skew 0	I
SK1	31	Skew 1	I
ON/$\overline{OFF}$	53	On/Off	I
BLE	51	Blink Enable	I
AT	57	Attribute	I
G/$\overline{C}$	58	Graphic/Character	I
WIDE	54	Wide	I
LS	56	Large Screen	I
D/$\overline{S}$	55	Dual/Single	I
MODE	52	Mode	I

Pin Functions

Power Supply (Vcc1, 2, GND)

Power Supply Pin (+5 V): Connect $V_{CC}1$ and $V_{CC}2$ with +5 V power supply circuit.

Ground Pin (0 V): Connect GND1 and GND2 with 0 V.

LCD Interface

LCD Up Panel Data (LU0-LU3), LCD Down Panel Data (LD0-LD3): LU0-LU3 and LD0-LD3 output LCD data as shown in table 1.

Clock One (CL1): CL1 supplies timing clocks for display data latch.

Clock Two (CL2): CL2 supplies timing clock for display data shift.

First Line Marker (FLM): FLM supplies first line marker.

M (M): M converts liquid crystal drive output to AC.

Memory Interface

Memory Address (MA0-MA15): MA0-MA15 supply the display memory address.

Raster Address (RA0-RA4): RA0-RA4 supply the raster address.

Memory Data (MD0-MD7): MD0-MD7 receive the character dot data and bit-mapped data.

Memory Data (MD8-MD15): MD8-MD15 receive attribute code data and bit-mapped data.

MPU Interface

Data Bus (DB0-DB7): DB0-DB7 send/receive data as a three-state I/O common bus.

Chip Select ($\overline{\text{CS}}$): $\overline{\text{CS}}$ selects a chip. Low level enables MPU read/write of the LCTC internal registers.

Enable (E): E receives an enable clock. (HD63645F only).

Read/Write (R/$\overline{\text{W}}$): R/$\overline{\text{W}}$ enables MPU read of the LCTC internal registers when R/$\overline{\text{W}}$ is high, and MPU write when low. (HD63634F only).

Write ($\overline{\text{WR}}$): $\overline{\text{WR}}$ receives MPU write signal. (HD64645F Only)

Read ($\overline{\text{RD}}$): $\overline{\text{RD}}$ receives MPU read signal. (HD64645F Only)

Register Select (RS): RS selects registers. (Refer to table 5.)

Reset ($\overline{\text{RES}}$): $\overline{\text{RES}}$ performs external reset of the LCTC. Low level of $\overline{\text{RES}}$ stops and zero-clears the LCTC internal counter. No register contents are affected.

Timing Signal

D Clock (DCLK): DCLK inputs the system clock.

M Clock (MCLK): MCLK indicates memory cycle ; DCLK is divided by four.

Display Timing (DISPTMG): DISPTMG high indicates that the LCTC is reading display data.

Cursor Display (CUDISP): CUDISP supplies cursor display timing ; connect with MD12 in character mode.

Skew 0 (SK0)/Skew 1 (SK1): SK0 and SK1 control skew timing. Refer to table 2.

Mode Select

The mode select pins ON/$\overline{\text{OFF}}$, BLE, AT, G/$\overline{\text{C}}$,

Table 1. LCD Up Panel Data and LCD Down Panel Data

	Single Screen		
Pin name	**4-Bit Data**	**8-Bit Data**	**Dual Screen**
LU0-LU3	Data output	Data output	Data output for upper screen
LD0-LD3	Disconnected	Data output	Data output for lower screen

and WIDE are ORed with the mode register (R22) to determine the mode.

On/Off (ON/$\overline{\text{OFF}}$): ON/$\overline{\text{OFF}}$ switches display on and off. (High = display on).

Blink Enable (BLE): BLE high level enables attribute code "blinking" (MD13) and provides normal/blank blinking of specified characters for 32 frames each.

Attribute (AT): AT controls character attribute functions.

Graphic/Character (G/$\overline{\text{C}}$): G/$\overline{\text{C}}$ switches between graphic and character display mode (graphic display when high).

Wide (WIDE): WIDE switches between normal and wide display mode (high = wide display, low = normal display).

Large Screen (LS): LS controls a large screen. LS high provides a data transfer rate of 40 Mbits/s for a graphic display. Also used to specify 8-bit LCD interface mode. For more details, refer to page 26.

Dual/Single (D/$\overline{\text{S}}$): D/$\overline{\text{S}}$ switches between single and dual screen display (dual screen display when high).

Mode (MODE): MODE controls easy mode. MODE high sets duty ratio, maximum number of rasters, cursor start/end rasters, etc. (Refer to table 9.)

Table 2. Skew Signals

SK0	SK1	Skew Function
0	0	No skew
1	0	1-character time skew
0	1	2-character time skew
1	1	Inhibited combination

Function Overview

LCD and CRT Display Systems

Figure 1 shows a system using both LCD and CRT displays.

Main Features of HD63645F/HD64645F

Main features of the LCTC are:

- High-resolution liquid crystal display screen control (up to 720 × 512 dots)
- Software compatible with HD6845 (CRTC)
- Built-in character attribute control circuit

Table 3 shows how the LCTC can be used.

Table 3. Functions, Application, and Configuration

Classification	Item	Description
Functions	Screen Format	Programmable horizontal scanning cycle by the character clock period Programmable multiplexing duty ratio from static up to 1/512 Programmable number of displayed characters per character row Programmable number of rasters per character row (number of vertical dots within a character row + space between character rows)
	Cursor Control	Programmable cursor display position, corresponding to RAM address Programmable cursor height by setting display start/end rasters Programmable blink rate, 1/32 or 1/64 frame rate
	Memory Rewriting	Time for rewriting memory set either by specifying number of horizontal total characters or by cycle steal utilizing MCLK
	Memory Addressing	16-bit memory address output, up to 64 kbytes x 2 memory accessible DRAM refresh address output
	Paging and Scrolling	Paging by updating start address Horizontal scrolling by the character, by setting horizontal virtual screen width Vertical smooth scrolling by updating display start raster
	Character Attributes	Reverse video, blinking, nondisplay (white or black) character attributes
Application	CRTC Compatible	Facilitates system replacement of CRT display with LCD.
	OR Function	Enables superimposing display of character screen and graphic screen
Configuration	LCTC Configuration	Single 5 V power supply I/O TTL compatible except $\overline{\text{RES}}$, MODE, SK0, SK1 Bus connectable with HMCS 6800 family (HD63645) Bus connectable with 80 family (HD64645) CMOS process Internal logic fully static 80-pin flat plastic package

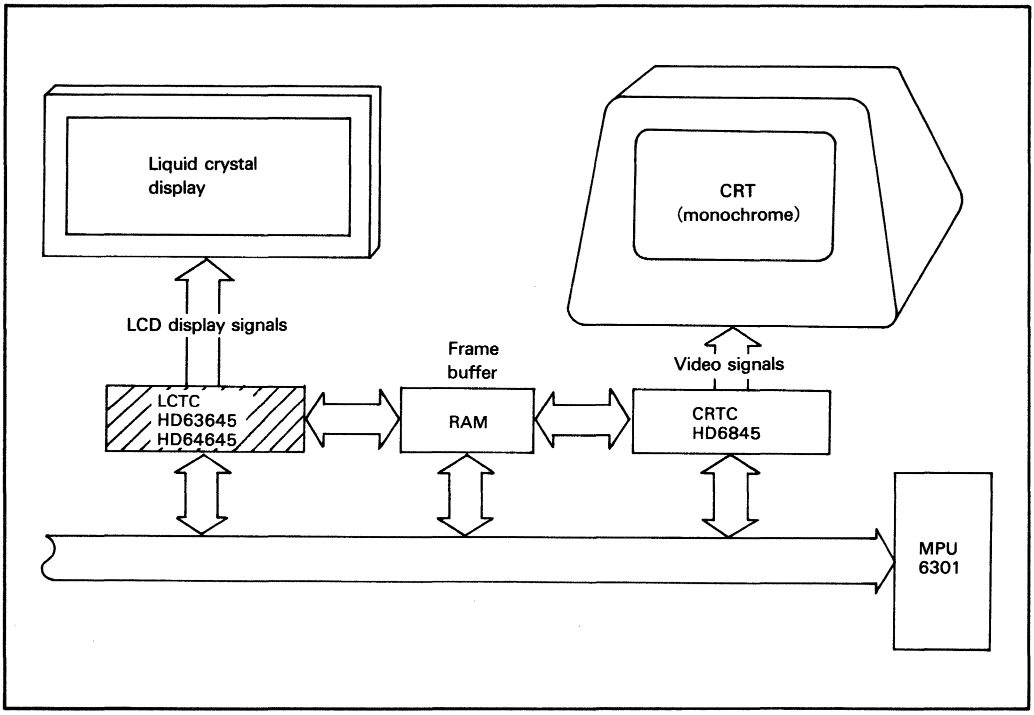
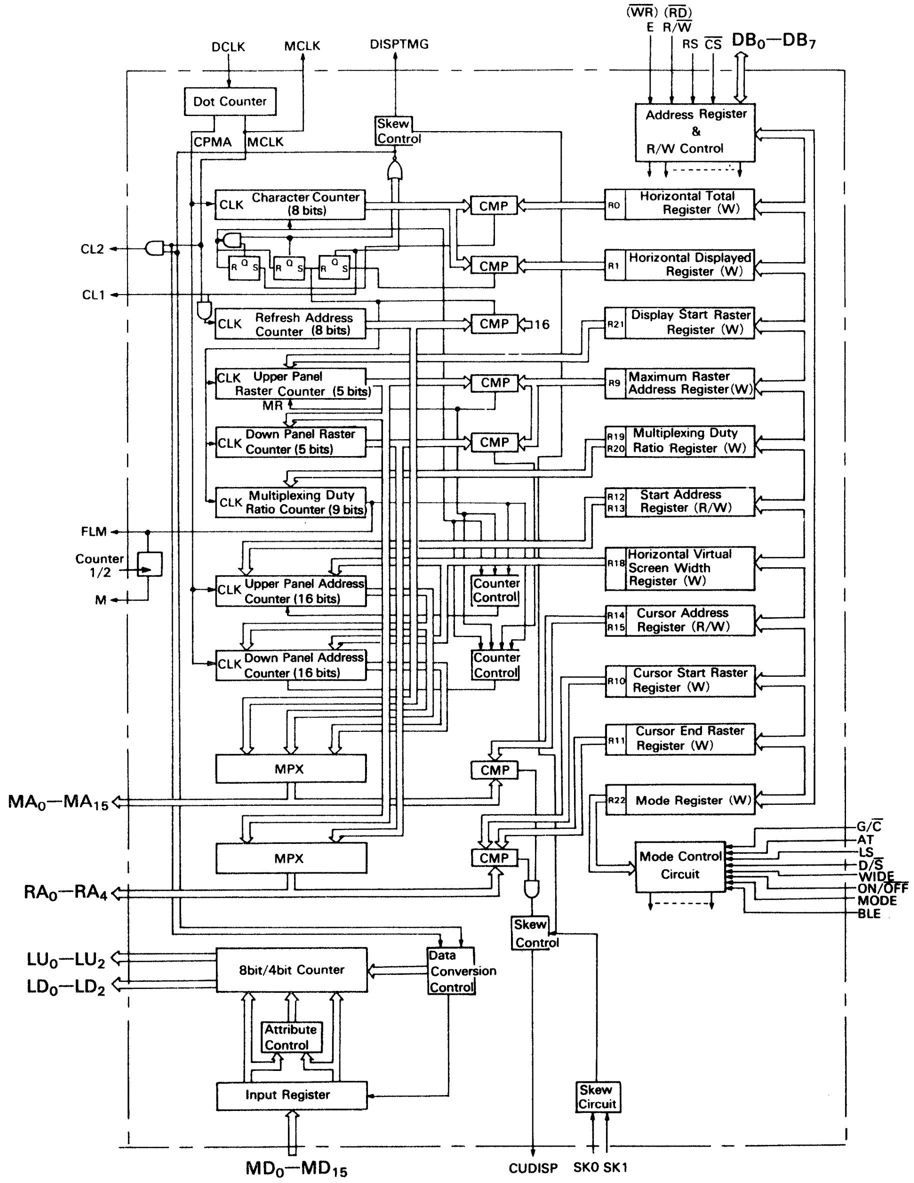


Figure 1. LCD and CRT Displays

Internal Block Diagram

Figure 2 is a block diagram of the LCTC.


(WR) (RD)
E R/W
RS CS
DB0—DB7
DCLK
MCLK
DISPTMG
Dot Counter
CPMA
MCLK
Skew Control
Address Register & R/W Control
CLK Character Counter (8 bits)
CMP
R0 Horizontal Total Register (W)
CL2
R Q S
CMP
R1 Horizontal Displayed Register (W)
CL1
CLK Refresh Address Counter (8 bits)
CMP 16
R21 Display Start Raster Register (W)
CLK Upper Panel Raster Counter (5 bits)
MR
CMP
R9 Maximum Raster Address Register (W)
CLK Down Panel Raster Counter (5 bits)
CMP
R19 R20 Multiplexing Duty Ratio Register (W)
CLK Multiplexing Duty Ratio Counter (9 bits)
R12 R13 Start Address Register (R/W)
FLM
Counter 1/2
M
R18 Horizontal Virtual Screen Width Register (W)
CLK Upper Panel Address Counter (16 bits)
Counter Control
R14 R15 Cursor Address Register (R/W)
CLK Down Panel Address Counter (16 bits)
Counter Control
R10 Cursor Start Raster Register (W)
R11 Cursor End Raster Register (W)
MPX
CMP
MA0—MA15
R22 Mode Register (W)
MPX
CMP
RA0—RA4
Mode Control Circuit
G/C
AT
LS
D/S
WIDE
ON/OFF
MODE
BLE
Skew Control
LU0—LU2
LD0—LD2
8bit/4bit Counter
Data Conversion Control
Attribute Control
Input Register
Skew Circuit
MD0—MD15
CUDISP
SK0 SK1

( ) is for HD64645 (80 types bus interface)

Figure 2. LCTC Block Diagram

System Block Configuration Examples

Figure 3 is a block diagram of a character/graphic display system. Figure 5 shows two examples using LCD drivers.

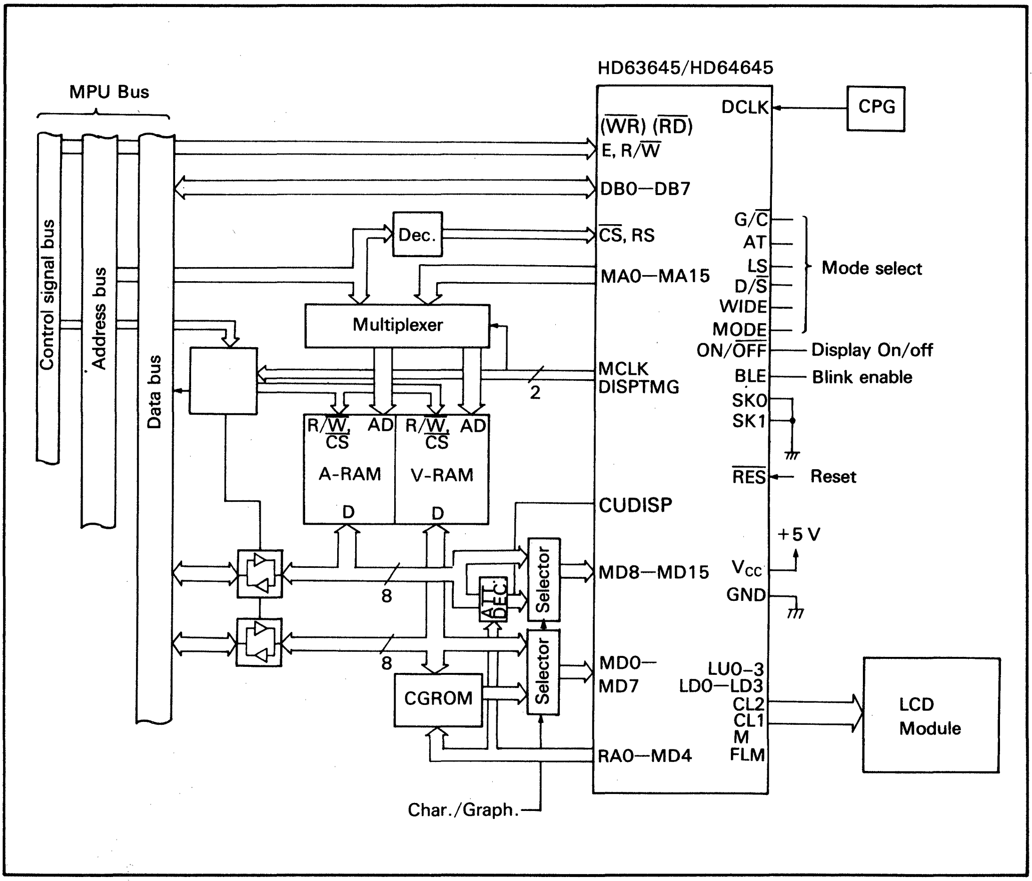
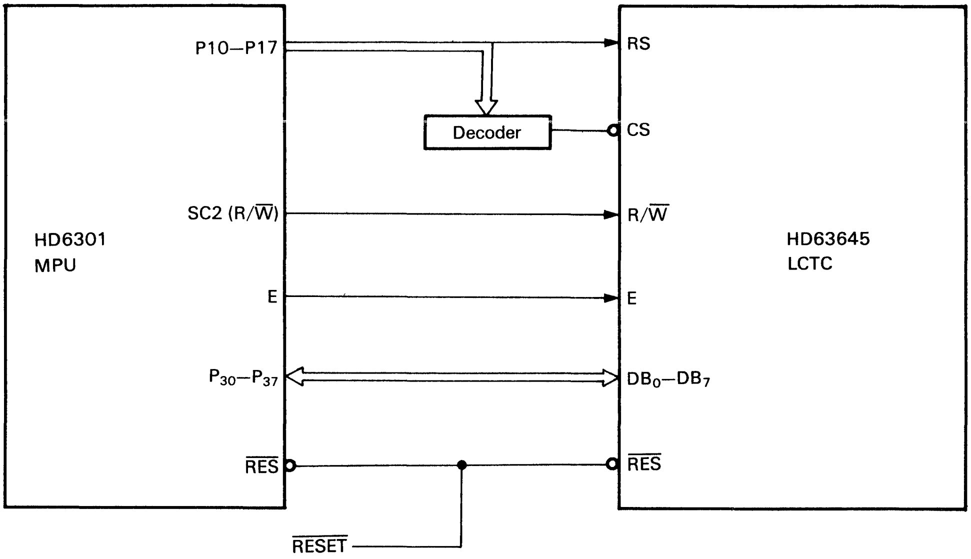


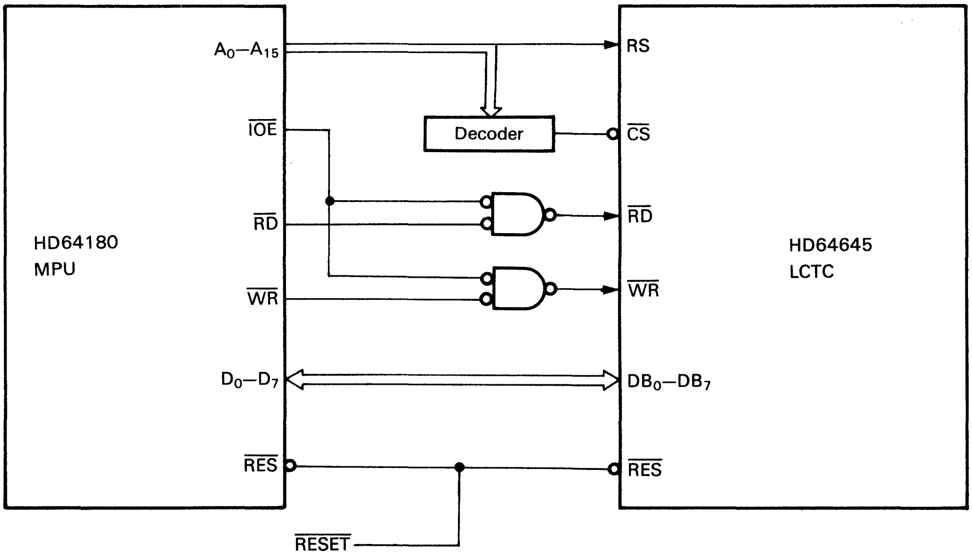
Figure 3. Character/Graphic Display System Example

Interface to MPU



Note: HD6301 is set in mode 5. P10—P17 are used as output ports, and P30—P37 as data buses. SC2 outputs R/$\overline{\text{W}}$ here.

(1) Interface between HD6301 and HD63645



Note: Concerning 80 family MPU's, I/O space is separate from memory space in software. Thus the LCTC, a part of I/O, needs the ANDed signals of the interface signals and $\overline{\text{IOE}}$. So $\overline{\text{IOE}}$ and $\overline{\text{RD}}$, and $\overline{\text{IOE}}$ and $\overline{\text{WR}}$ should be ORed to satisfy t_{AS}, the timing of $\overline{\text{CS}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$.

(2) Interface between HD64180 and HD64645

Figure 4. Interface to MPU

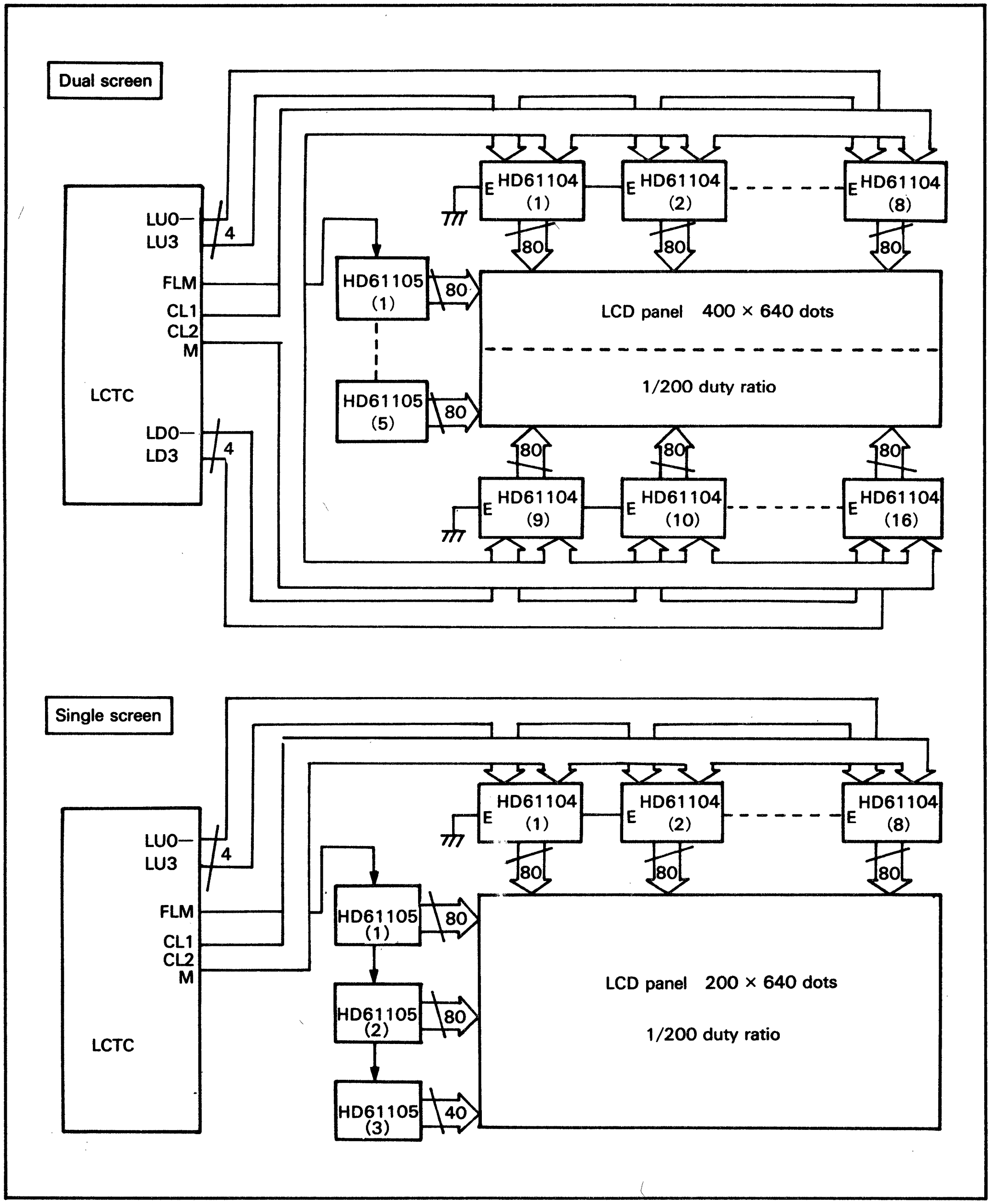


Figure 5. LCD Driver Examples

Registers

Table 5 shows the register mapping. Table 5 describes the in function. Table 6 shows the differences between CRTC and LCTC registers.

Table 4. Registers Mapping

		Address Register	Reg.					Data Bit							
$\overline{CS}$	RS	4 3 2 1 0	No.	Register Name	Program Unit	Symbol	R/W	7	6	5	4	3	2	1	0
1	–	– – – – –		Invalid	–	–	–	▨	▨	▨	▨	▨	▨	▨	▨
0	0	– – – – –	AR	Address Register	–	–	W	▨	▨	▨					
0	1	0 0 0 0 0	R0	Horizontal Total Characters	Character[3]	Nht	W								
0	1	0 0 0 0 1	R1	Horizontal Displayed Characters	Character	Nhd	W								
0	1	0 1 0 0 1	R9	Maximum Raster Address	Raster	Nr	W	▨	▨	▨					
0	1	0 1 0 1 0	R10	Cursor Start Raster	Raster[4]	Ncs	W	▨	B	P					
0	1	0 1 0 1 1	R11	Cursor End Raster	Raster	Nce	W	▨	▨	▨					
0	1	0 1 1 0 0	R12	Start Address (H)	Memory Address	–	R/W								
0	1	0 1 1 0 1	R13	Start Address (L)	Memory Address	–	R/W								
0	1	0 1 1 1 0	R14	Cursor Address (H)	Memory Address	–	R/W								
0	1	0 1 1 1 1	R15	Cursor Address (L)	Memory Address	–	R/W								
0	1	1 0 0 1 0	R18	Horizontal Virtual Screen Width	Character	Nir	W								
0	1	1 0 0 1 1	R19	Multiplexing Duty Ratio (H)	Raster[3]	Ndh	W	▨	▨	▨	▨	▨	▨	▨	
0	1	1 0 1 0 0	R20	Multiplexing Duty Ratio (L)	Raster[3]	Ndl	W								
0	1	1 0 1 0 1	R21	Display Start Raster	Raster	Nsr	W	▨	▨	▨					
0	1	1 0 1 1 0	R22	Mode Register	—Note[5]	–	W	▨	▨	▨	ON/OFF	G/C	WIDE	BLE	AT

Notes :
1. ▨ : Invalid data bits
2. R/W indicates whether write access or read access is enabled to/from each register.
   W : Only write accessible
   R/W : Both read and write accessible
3. The "value to be specified less 1" should be programmed in these registers (R0, R1) and R20).
4. Data bits 5 and 6 of cursor start register control the cursor status as shown below. (For more details, refer to page 27).

B	P	Cursor Blink Mode
0	0	Cursor on ; without blinking
0	1	Cursor off
1	0	Blinking once every 32 frames
1	1	Blinking once every 64 frames

5. The OR of mode pin status and mode register data determines the mode.
6. Registers R2-R8, R16, and R17 are not assigned for the LCTC. Programming to these registers, will be ignored.

Table 5. Internal Register Description

Reg. No.	Register Name	Size(Bits)	Description
AR	Address Register	5	Specifies the internal control registers (R0, R1, R9-R15, R18-R22) address to be accessed
R0	Horizontal Total Characters	8	Specifies the horizontal scanning period
R1	Horizontal Displayed Characters	8	Specifies the number of displayed characters per character row
R9	Maximum Raster Address	5	Specifies the number of rasters per character row, including the space between character rows
R10	Cursor Start Raster	5+2	Specifies the cursor start raster address and its blink mode
R11	Cursor End Raster	5	Specifies the cursor end raster address
R12	Start Address (H)	16	Specify the display start address
R13	Start Address (L)		
R14	Cursor Address (H)	16	Specify the cursor display address
R15	Cursor Address (L)		
R18	Horizontal Virtual Screen Width	8	Specifies the length of one row in memory space for horizontal scrolling
R19	Multiplexing Duty Ratio (H)	9	Specify the number of rasters for one screen
R20	Multiplexing Duty Ratio (L)		
R21	Display Start Raster	5	Specifies the display start raster within a character row for smooth scrolling
R22	Mode Register	5	Controls the display mode

*For more details of registers, refer to "Internal Registers".

Table 6. Internal Register Comparison between LCTC and CRTC

Reg. No.	LCTC HD63645/HD64645	Comparison	CRTC HD6845
AR	Address Register	Equivalent to CRTC	Address Register
R0	Horizontal Total Characters		Horizontal Total Characters
R1	Horizontal Displayed Characters		Horizontal Displayed Characters
R2		Particular to CRTC ; unnecessary for LCTC	Horizontal Sync Position
R3			Sync Width
R4			Vertical Total Characters
R5			Vertical Total Adjust
R6			Vertical Displayed Characters
R7			Vertical Sync Position
R8			Interlace and Skew
R9	Maximum Raster Address	Equivalent to CRTC	Maximum Raster Address
R10	Cursor Start Raster		Cursor Start Raster
R11	Cursor End Raster		Cursor End Raster
R12	Start Address (H)		Start Address (H)
R13	Start Address (L)		Start Address (L)
R14	Cursor Address (H)		Cursor (H)
R15	Cursor Address (L)		Cursor (L)
R16		Particular to CRTC ; unnecessary for LCTC	Light Pen (H)
R17			Light Pen (L)
R18	Horizontal Virtual Screen Width	Additional registers for LCTC	
R19	Multiplexing Duty Ratio (H)		
R20	Multiplexing Duty Ratio (L)		
R21	Display Start Raster		
R22	Mode Register		

Functional Description

Programmable Screen Format

Figure 6 illustrates the relation between LCD display screen and registers. Figure 7 shows a timing chart of signals output from the LCTC in mode 5 as an example.

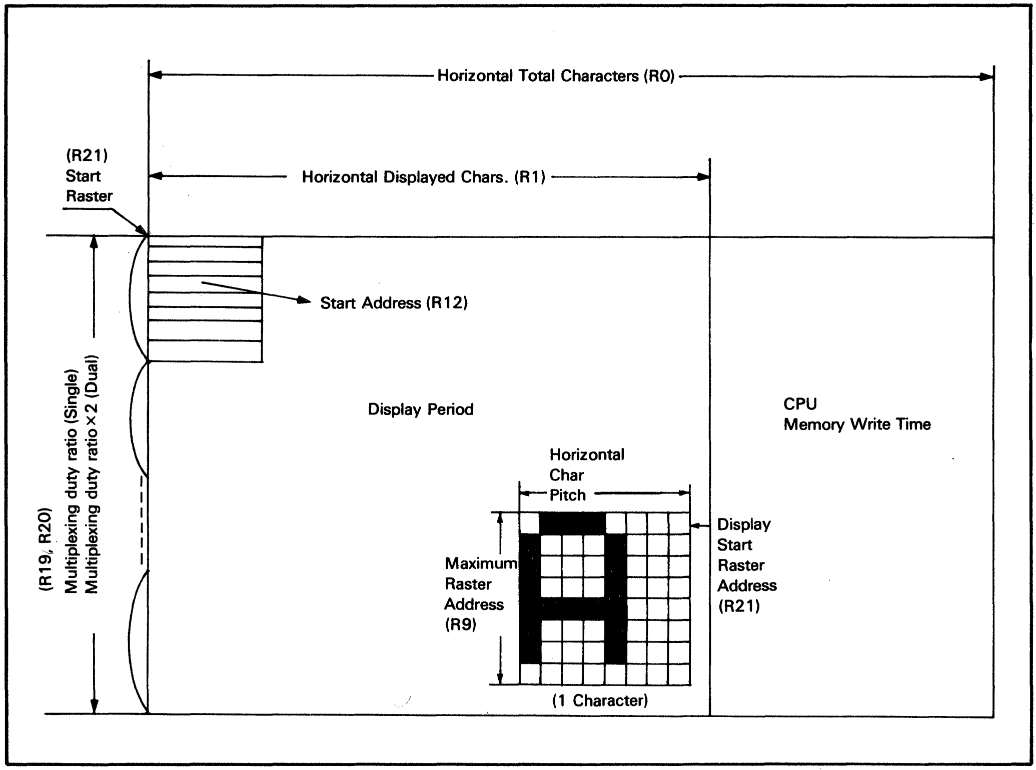


Figure 6. Relation between Display Screen and Registers

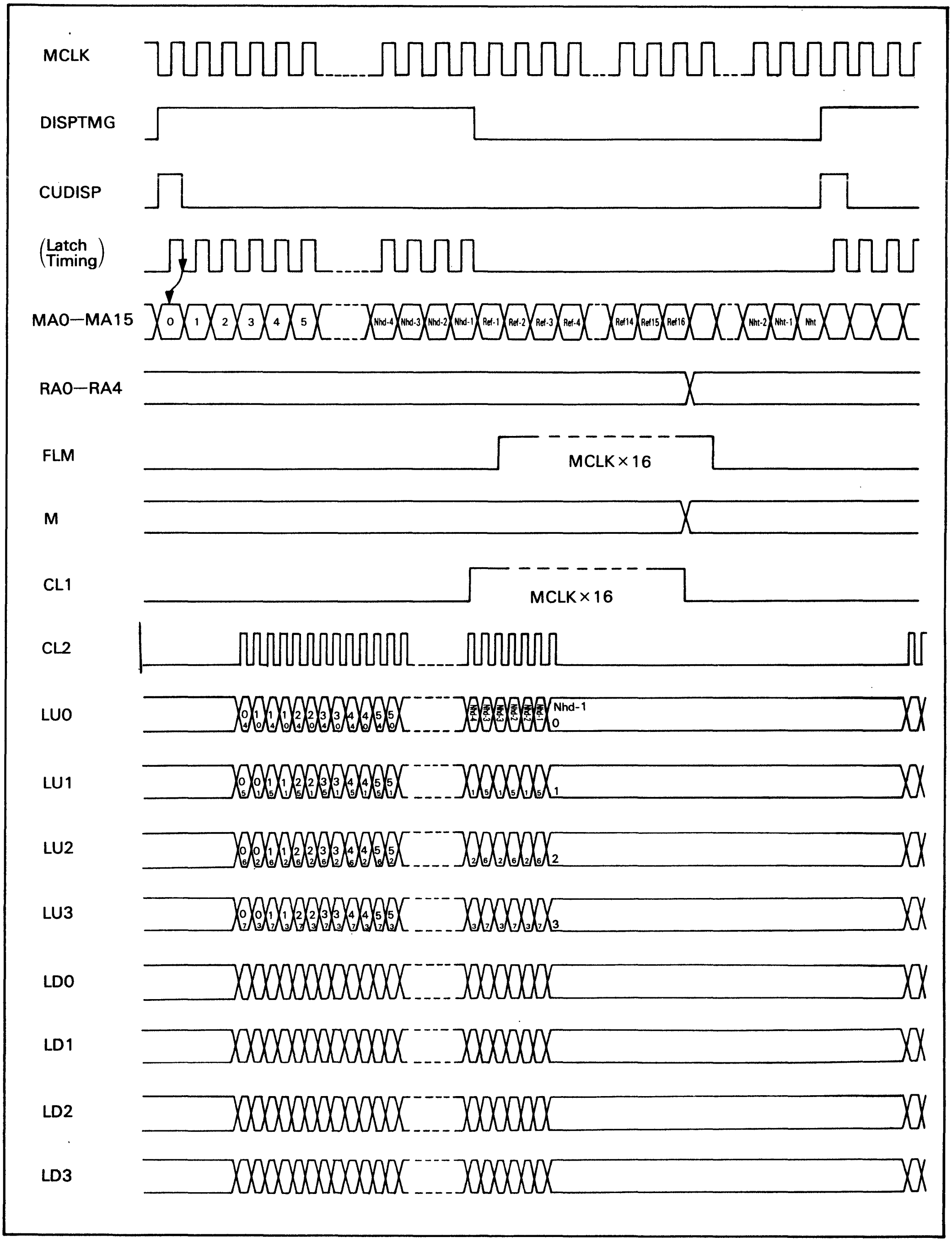


Figure 7. LCTC Timing Chart (In Mode 5: Single Screen, 4-Bit Transfer, Normal Character Display)

Cursor Control

The following cursor functions (figure 8) can be controlled by programming specific registers.

- Cursor display position
- Cursor height
- Cursor blink mode

A cursor can be displayed only in character mode. Also, CUDISP pin must be connected to MD12 pin to display a cursor.

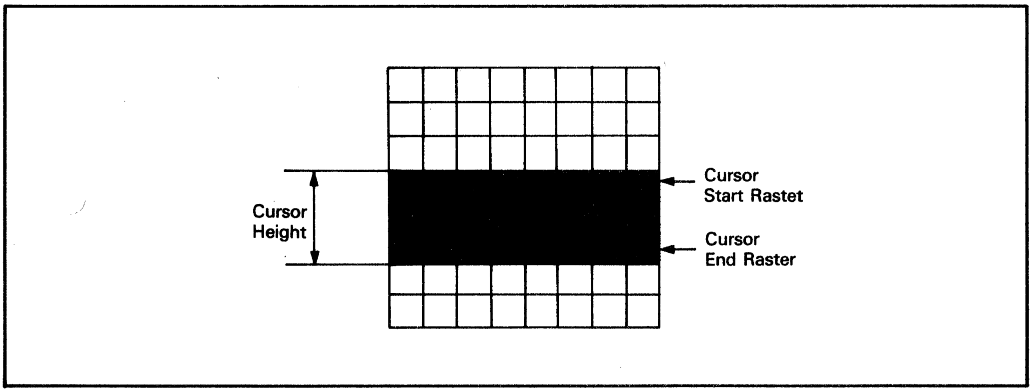


Figure 8. Cursor Display

Character Mode and Graphic Mode

The LCTC supports two types of display modes; character mode and graphic mode. Graphic mode 2 is provided to utilize software for system using the CRTC (HD6845).

The display mode is controlled by an OR between the mode select pins (D/$\overline{S}$, G/$\overline{C}$, LS, WIDE, AT) and mode register (R22).

Character Mode: Character mode displays characters by using CG-ROM. The display data supplied from memory is accessed in 8-bit units. A variety of character attribute functions are provided, such as reverse video, blinking, nondisplay (white or black), etc., by storing the attribute data in attribute RAM (A-RAM).

Figure 9 illustrates the relation between character display screen and memory contents.

Graphic Mode 1: Graphic Mode 1 directly displays data stored in a graphic memory buffer. The display data supplied from memory is accessed in 16-bit units. Character attribute functions or wide mode are not provided. Figure 10 illustrates the relation between graphic display screen and memory contents.

Graphic Mode 2: Graphic mode 2 utilizes software for the system using the CRTC (HD6845). The display data supplied from memory is accessed in 16-bit units. Character attribute functions or wide mode are not provided. The same memory addresses are output repeatedly a number of times specified by maximum raster register (R9). The raster address is output in the same way as character mode.

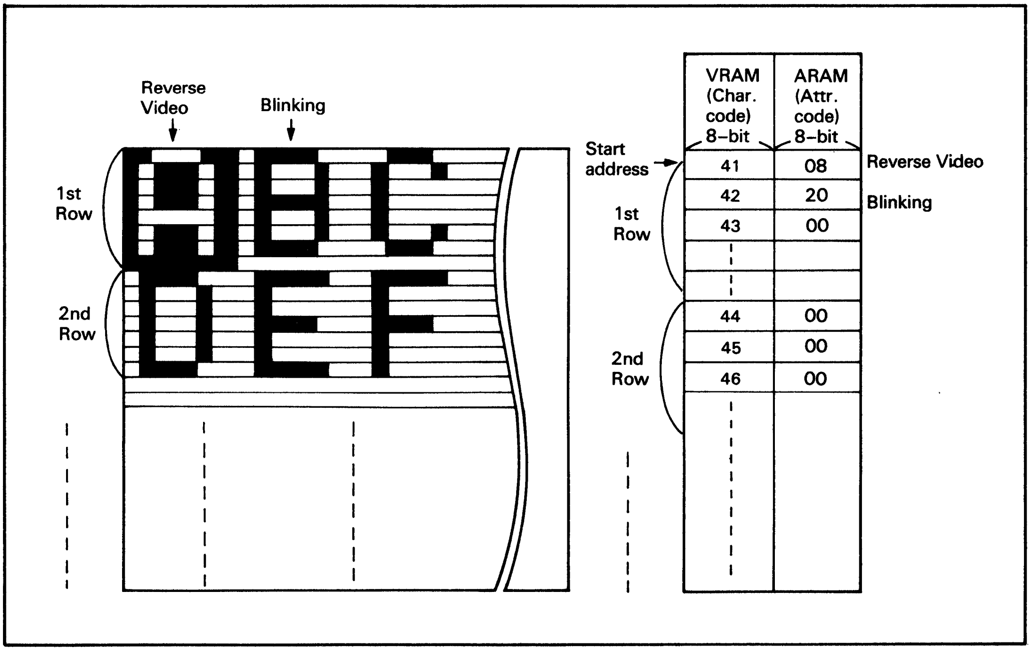


Figure 9. Relation between Character Screen and Memory Contents

Horizontal Virtual Screen Width

Horizontal virtual screen width can be specified by the character in addition to the number of horizontal displayed characters (figure 11).

The display screen can be scrolled in any direction by the character, by setting the horizontal virtual screen width and updating the start address. This function is enabled by programming the horizontal virtual screen width register (R18).

Figure 12 shows an example.

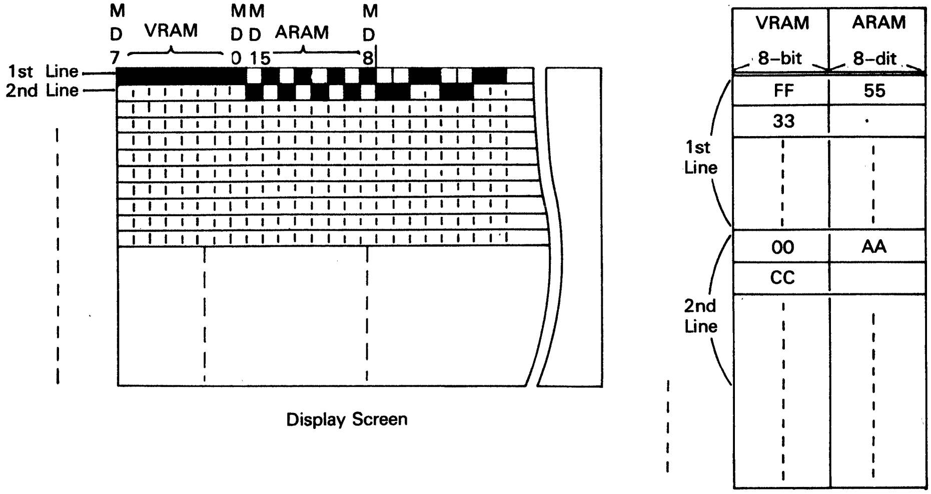


Figure 10. Relation between Graphic Screen and Memory Contents

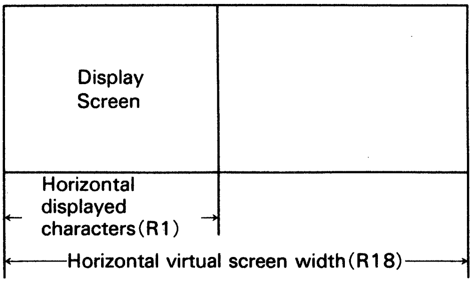

Display Screen
Horizontal displayed characters (R1)
Horizontal virtual screen width (R18)

Figure 11. Horizontal Virtual Screen Width

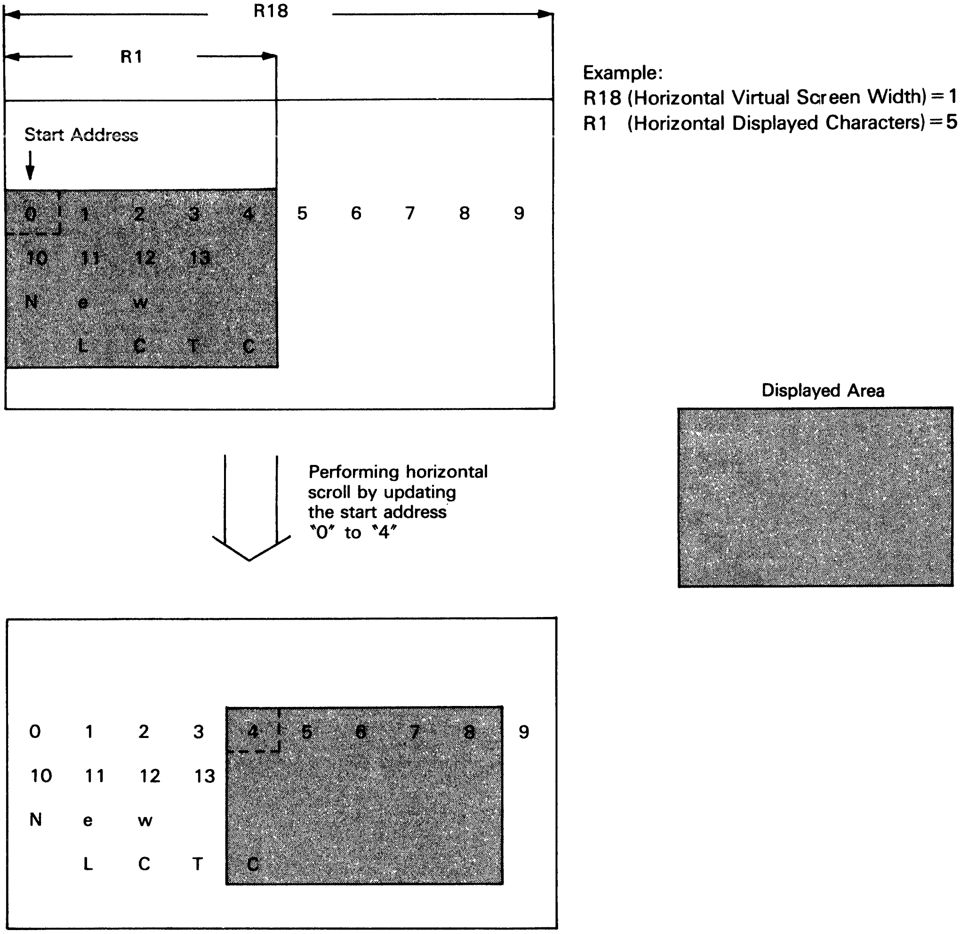

R18
R1
Start Address
0 1 2 3 4 5 6 7 8 9
10 11 12 13
N e w
L C T C
Example:
R18 (Horizontal Virtual Screen Width) = 10
R1 (Horizontal Displayed Characters) = 5
Displayed Area
Performing horizontal scroll by updating the start address "0" to "4"
0 1 2 3 4 5 6 7 8 9
10 11 12 13
N e w
L C T C

Figure 12. Example of Horizontal Scroll by Setting Horizontal Virtual Screen Width

Smooth Scroll

Vertical smooth scrolling (figure 13) is performed by updating the display start raster, as specified by the start raster register (R21). This function is offered only in character mode.

Wide Display

The character to be displayed can be doubled in width, by supplying the same data twice (figure 14). This function is offered only in character mode, and controlled either by bit 2 of the mode register (R22) or by the WIDE pin.

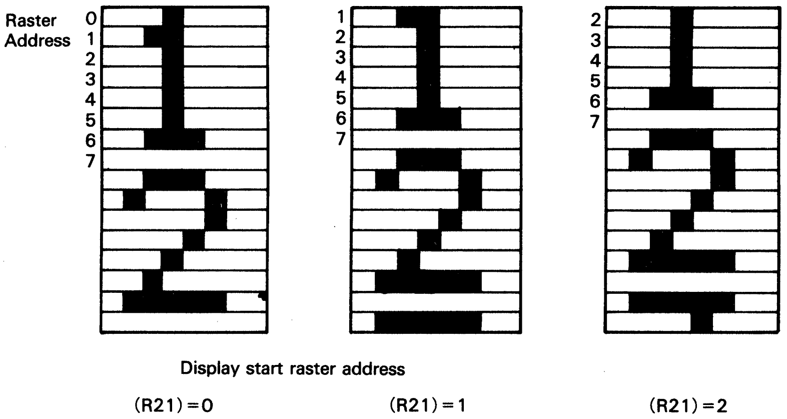


Figure 13. Example of Smooth Scroll by Setting Display Start Raster Address

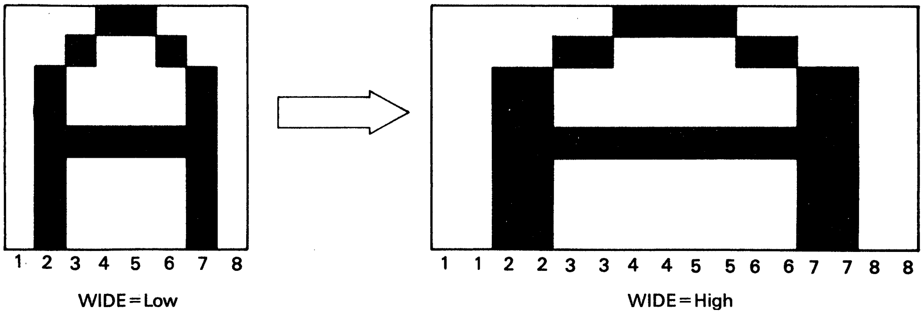


Figure 14. Example of Wide Display

Attribute Functions

A variety of character attribute functions such as reverse video, blinking, nondisplay (white) or nondisplay (black) can be implemented by storing the attribute data in A-RAM (attribute RAM). Figure 15 shows a display example using each attribute function.

The attribute functions are offered only in character mode, and controlled either by bit 0 of the mode register (R22) or the AT pin. As shown in figure 15, a character attribute can be specified by placing the character code on MD0-MD7, and the attribute code on MD11-MD15. MD8-MD10 are invalid.

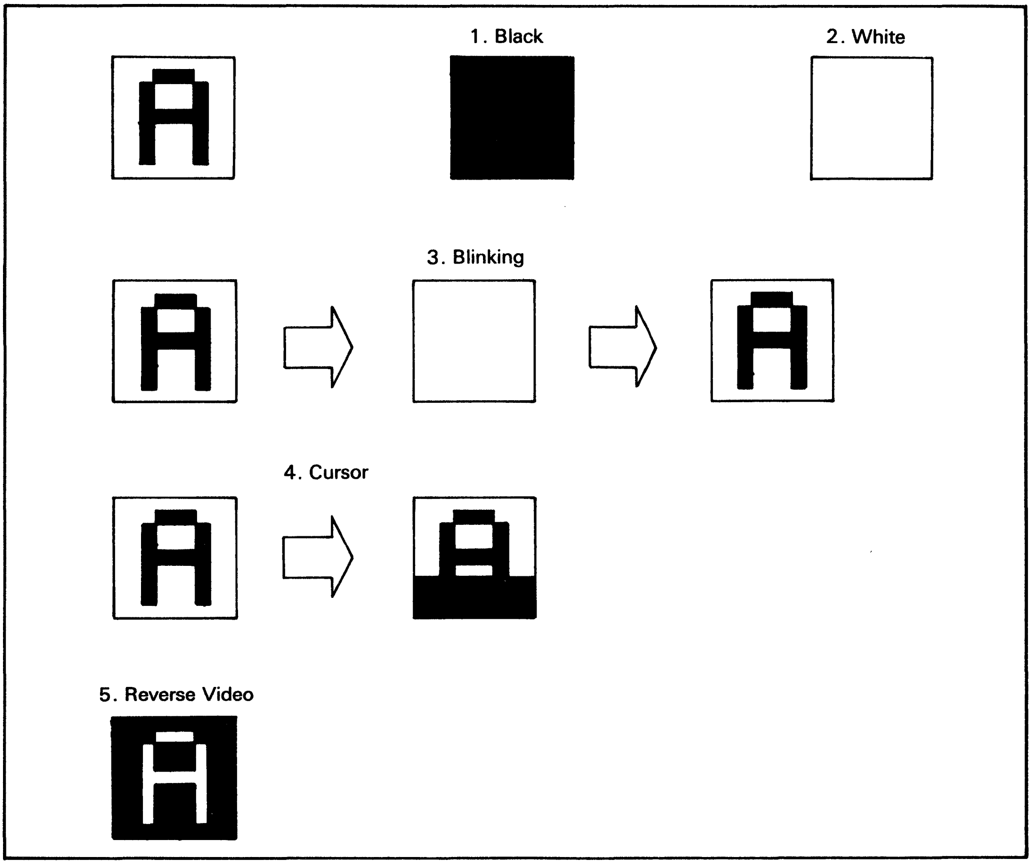


Figure 15. Display Example Using Attribute Functions

MD Input	15	14	13	12	11	10-8	7-0
Function	Non-display (black)	Non-display (white)	Blinking	Cursor	Reverse video	* * *	Character Code

* : Invalid

Figure 16. Attribute Code

OR Function—Superimposing Characters and Graphics

The OR function (figure 17) generates the OR of the data entered into MD0-MD7 (e.g. character data) and the data into MD8-MD15 (e.g. graphic data) in the LCTC and transfers this data as 1 byte.

This function is offered only in character mode, and controlled by bit 0 of the mode register (R22) or by the AT pin. Any attribute functions are disabled when using the OR function.

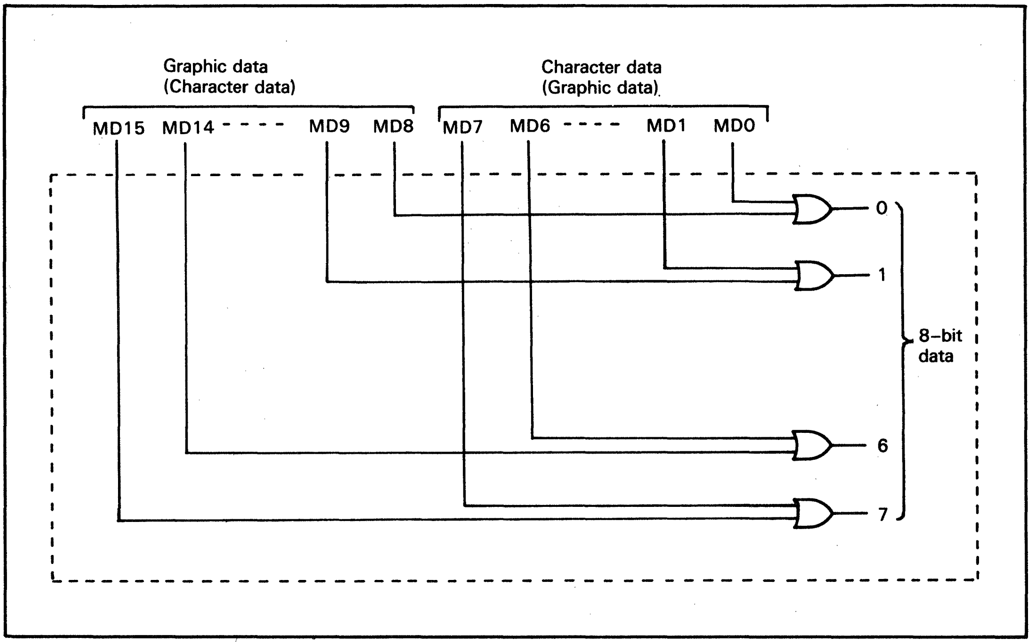


Figure 17. OR Function

DRAM Refresh Address Output Function

The LCTC outputs the address for DRAM refresh while CL1 is high, as shown in figure 18. The 16 refresh addresses per scanned line are output 16 times, from \$00-\$FF.

Skew Function

The LCTC can specify the skew (delay) for CUDISP, DISPTMG, CL2 outputs and MD inputs.

If buffer memory and character generator ROM cannot be accessed within one horizontal character display period, the access is retarded to the next cycle by inserting a latch to memory address output and buffer memory output. The skew function retards the CUDISP, DISPTMG, CL2 outputs, and MD inputs in the LCTC to match phase with the display data signal.

By utilizing this function, a low-speed memory can be used as a buffer RAM or a character generator ROM.

This function is controlled by pins SK0 and SK1 as shown in table 7.

Table 7. Skew Function

SK0	SK1	Skew Function
0	0	No skew
1	0	1 character time skew
0	1	2 character time skew
1	1	Inhibited combination

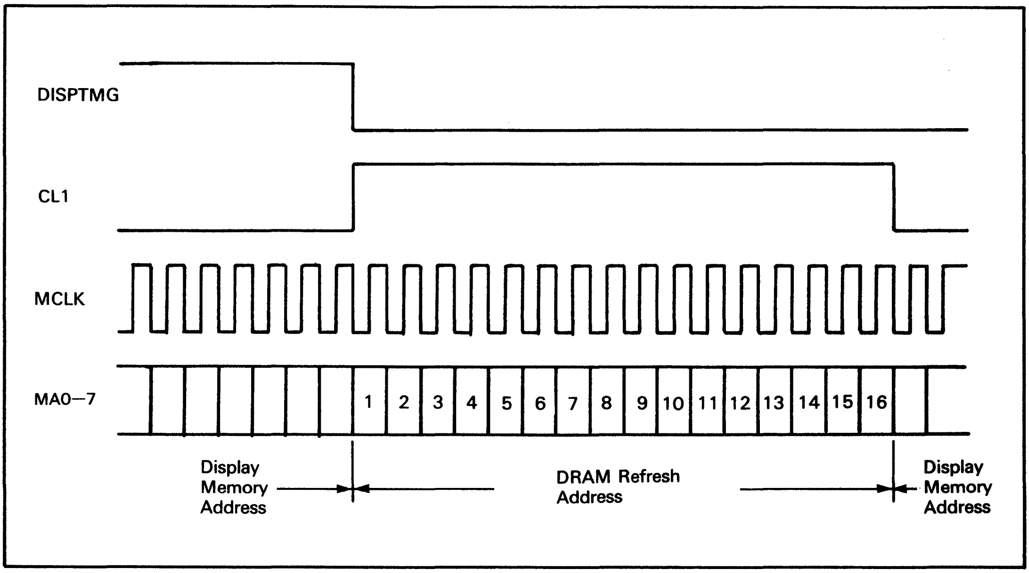


Figure 18. DRAM Refresh Address Output

Easy Mode

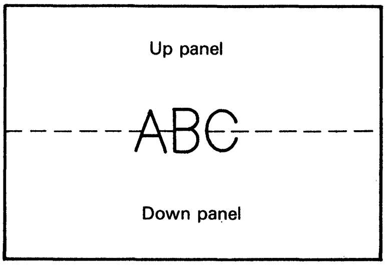
This mode utilizes software for systems using the CRTC (HD6845). By setting MODE pin to high, the display mode and screen format are fixed as shown in table 8. With this mode, software for a CRT screen can be utilized in a system using the LCTC, without changing the BIOS.

Automatic Correction of Down Panel Paster Address

When the LCTC mode is set for character display and dual screen, memory addresses (MA) and raster addresses (RA) are output in such a way as to keep continuity of display spreading over the two panels. Therefore users can use the LCTC without considering the multiplexing duty ratio (the number of vertical dots of a screen) or the character font. (See figure 19.)

Table 8. Fixed Values in Easy Mode

Reg. No.	Register Name	Fixed Value (decimal)
R9	Maximum raster address	7
R10	Cursor start raster	6
R11	Cursor end raster	7
R18	Horizontal virtual screen width	Same value as (R1)
R19	Multiplexing duty ratio (H)	99 (in dual screen mode)
R20	Multiplexing duty ratio (L)	199 (in single screen mode)
R21	Display start raster	0
R22	Mode register	0



Characters keep continuity in spite of the break of a screen.

Figure 19. Example of the Display in the Character Mode

System Configuration and Mode Setting

LCD System Configuration

The screen configuration, single or dual, must be specified when using the LCD system (figure 20).

Using the single screen configuration, you can construct an LCD system with lower cost than a dual screen system, since the required number of column driversis smaller and the manufacturing process for mounting them is simpler. However, there are some limitations, such as duty ratio, breakdown voltage of a driver, and display quality of the liquid crystal, in single screen configuration. Thus, a dual screen configuration may be more suitable to an application.

The LCTC also offers an 8-bit LCD data transfer function to support an LCD screen with a smaller interval of signal input terminals. For a general size LCD screen, such as 640 × 200 single, or 640 × 400 dual, the usual 4-bit LCD data transfer is satisfactory.

Hardware Configuration and Mode Setting

The LCTC supports the following hardware configurations:

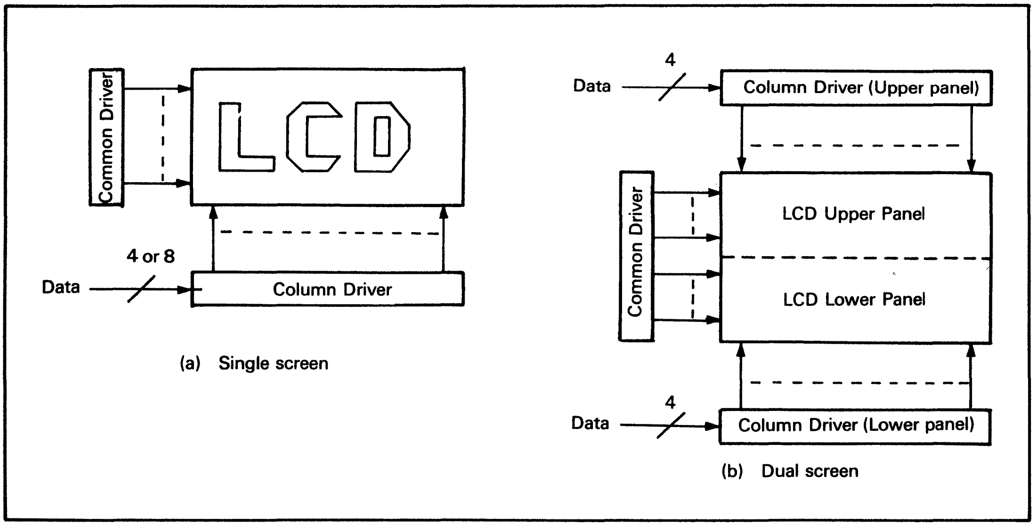
- Single or dual screen configuration
- 4-or 8-bit LCD data transfer

and the following screen format:

- Character, graphic 1, or graphic 2 display
- Normal or wide display (only in character mode)
- OR or attribute display (only in character mode)

Also, the LCTC supports up to 40 Mbits/s of large screeen mode (mode 13) for large screen display. This mode is provided only in graphic 1 mode.

Table 9 shows the mode selection method according to hardware configuration and screen format. Table 10 shows how they are specified.



(a) Single screen

(b) Dual screen

Figure 20. Hardware Configuration According to Screen Format

Table 9. Mode Selection

Hardware Configuration			Screen Format				
LCD Data Transfer	**Screen Configu-ration**	**Screen Size**	**Character/ Graphic**	**Normal/ Wide**	**Attribute/ OR**	**Maximum data transfer speed (MBPS)**	**Mode No.**
4-bit	Single	Normal	Character	Normal	AT OR	20	5
				Wide	AT OR	10	6
			Graphic 1			20	7
			Graphic 2			20	8
	Dual	Normal	Character	Normal	AT OR	20	1
				Wide	AT OR	10	2
			Graphic 1			20	3
			Graphic 2			20	4
		Large	Graphic 1			40	13
8-bit	Single	Normal	Character	Normal	AT OR	20	9
				Wide	AT OR	10	10
			Graphic 1			20	11
			Graphic 2			20	12

Note : Maximum data transfer speed indicates amount of the data read out of a memory. Thus, the data transfer speed sent to the LCD driver in wide function is 20 Mbps.

Mode List

Table 10. Mode List

No.	Mode Name	Pin Name D/$\overline{S}$	G/$\overline{C}$	LS	WIDE	AT	Screen Confg.	Graphic/ Character	Data Transfer	Wide Display	Attribute
1	Dual-screen character	1	0	0	0	0	Dual screen	Character	4-bit × 2	Normal	OR
		1	0	0	0	1					AT
2	Dual-screen wide character	1	0	0	1	0				Wide	OR
		1	0	0	1	1					AT
3	Dual-screen graphic 1	1	1	0	0	1		Graphic		—	—
4	Dual-screen graphic 2	1	1	0	0	0					
5	Single-screen character	0	0	0	0	0	Single screen	Character	4-bit	Normal	OR
		0	0	0	0	1					AT
6	Single-screen wide character	0	0	0	1	0				Wide	OR
		0	0	0	1	1					AT
7	Single-screen graphic 1	0	1	0	0	1		Graphic		—	—
8	Single-screen graphic 2	0	1	0	0	0					
9	8-bit character	0	0	1	0	0		Character	8-bit	Normal	OR
		0	0	1	0	1					AT
10	8-bit wide character	0	0	1	1	0				Wide	OR
		0	0	1	1	1					AT
11	8-bit graphic 1	0	1	1	0	1		Graphic		—	—
12	8-bit graphic 2	0	1	1	0	0					
13	Large screen	1	1	1	0	1	Dual screen		4-bit × 2		

The LCTC display mode is determined by pins D/$\overline{S}$ (pin 55), G/$\overline{C}$ (pin 58), LS (pin 56), WIDE (pin 54), and AT (pin 57). As for G/C, WIDE, and AT, the OR is taken between data bits 0, 2, and 3 of the mode register (R22). The display mode can be controlled by either one of the external pins or the data bits of R22.

Note : The above 5 pins have 32 status combinations (high and low). Any combinations other than the above are inhibited, because they may cause malfunctions. If you set an inhibited combination, set the right combination again.

Internal Registers

The HD63645/HD64645 has one address register and fourteen data registers. In order to select one out of fourteen data registers, the address of the data register to be selected must be written into the address register. The MPU can transfer data to/from the data register corresponding to the written address.

To be software compatible with the CRTC (HD6845), registers R2-R8, R16, and R17, which are not necessary for an LCD are defined as invalid for the LCTC.

Address Register (AR)

AR register (figure 21) specifies one out of 14 data registers. Address data is written into the address register when RS is low. If no register corresponding to a specified address exists, the address data is invalid.

Horizontal Total Characters Register (R0)

R0 register (figure 22) specifies a horizontal scanning period. The total number of horizontal characters less 1 must be programmed into this 8-bit register in character units. The "Nht" indicates the horizontal scanning period including the period when the CPU occupies memory (total number of horizontal characters minus the number of horizontal displayed characters). Its unit is, then, converted from time into the number of characters. This value is to be specified according to the specification of the LCD system to be used.

Horizontal Displayed Characters Register (R1)

R1 register (figure 23) specifies the number of characters displayed per row. The horizontal character pitches are 8 bits for normal character display and 16 dots for wide character display and graphic display.

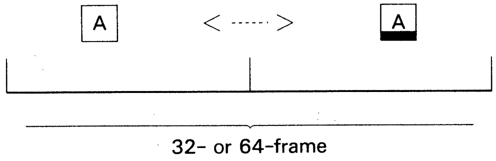
The "Nhd" must be less than the total number of horizontal characters.

Maximum Raster Address Register (R9)

R9 register (figure 24) specifies the number of rasters per row in characters mode, consisting of 5 bits. The programmable range is 0 (1 raster/row) to 31 (32 rasters/row).

Cursor Start Raster Register (R10)

R10 register (figure 25) specifies the cursor start raster address and its blink mode. Refer to table 11.



Cursor End Raster Register (R11)

R11 register (figure 26) specifies the cursor end raster address.

Start Address Register (H/L)(R12/R13)

R12/R13 register (figure 27) specifies a buffer memory read start address. Updating this register facilitates paging and scrolling. R14/R15 register can be read and written to/from

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0	—	
—	—	—	Register address						W

Figure 21. Address Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Nht (Total characters − 1)								Character	W

Figure 22. Horizontal Total Characters Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Nhd (Displayed characters)								Character	W

Figure 23. Horizontal Displayed Characters Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	Nr					Raster	W

Figure 24. Maximum Raster Address Register

the MPU.

Cursor Address Register (H/L)(R14/R15)
R14/R15 register (figure 28) specifies a cursor display address. Cusor display requires setting R10 and R11, and CUDISP should be connected with MD12 (in character mode). This register can be read from and written to the MPU.

Horizontal Virtual Screen Width Register (R18)
R18 register (figure 29) specifies the memory width to determine the start address of the next row. By using this register, memory width can be specified larger than the number of horizontal displayed characters. Updating the display start address facilitates scrolling in any direction within a memory space.

The start address of the next row is that of the previous row plus Nir. If a larger memory width than display width is unnecessary, Nir should be set equal to the number of horizontal displayed characters.

Multiplexing Duty Ratio Register (H/L) (R19/R20)
R19/R20 register (figure 30) specifies the number of vertical dots of the display screen. The programmed value differs according to the LCD screen configuration.

In single screen configuration:
(Programmed value) = (Number of vertical dots) − 1.

In dual screen configuration:

$$\text{(Programmed value)} = \frac{\text{(Number of vertical dots)}}{2} - 1.$$

Display Start Raster Register (R21)
R21 register (figure 31) specifies the start raster of the character row displayed on the top of the screen. The programmed value should be equal or less than the maximum raster address. Updating this register allows smooth scrolling in character mode.

Mode register (R22)
The OR of the data bits of R22 (figure 32) register and the external terminals of the same name determines a particular mode. (figure 33)

Table 11 Cursor Blink Mode

B	P	Cursor blink mode
0	0	Cursor on ; without blinking
0	1	Cursor off
1	0	Blinking once every 32 frames
1	1	Blinking once every 64 frames

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	B	P	Ncs (Raster address)					Raster	W

Figure 25. Cursor Start Raster Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	Nce (Raster address)					Raster	W

Figure 26. Cursor End Raster Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0	Memory address	R/W
Memory address (H) (R12)									
Memory address (L) (R13)									

Figure 27. Start Address Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0	Memory address	R/W
Memory address (H) (R14)									
Memory address (L) (R15)									

Figure 28. Cursor Address Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Nir (No. of chars. of virtual width)								Character	W

Figure 29. Horizontal Virtual Screen Width Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	—	—	—	— (R19)	Ndh*	Raster	W
Ndl (Number of rasters − 1) (R20)									

* : Number of rasters

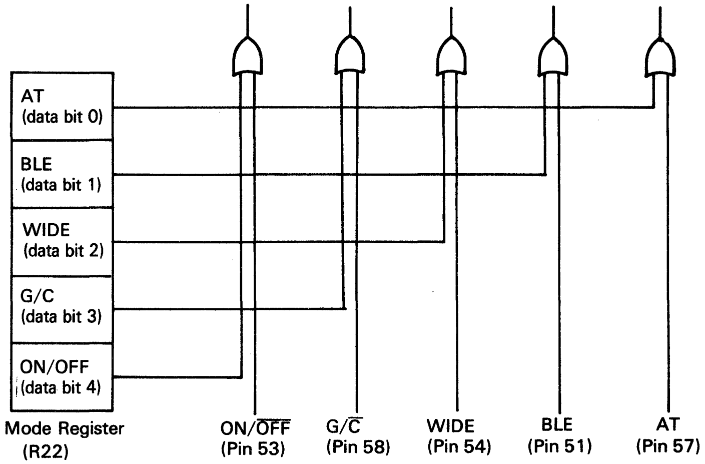
Figure 30. Multiplexing Duty Ratio Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
—	—	—	Raster address					Raster	W

Figure 31. Display Start Raster Register

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0	—	W
—	—	—	ON/OFF	G/C	WIDE	BLE	AT		

Figure 32. Mode Register



Notes: 1. AT (valid only when G/$\overline{\text{C}}$ is low (character mode))
AT = High: Attribute functions enabled, OR function disabled.
AT = Low: OR function enabled, attribute functions disabled.

2. BLE (valid only when G/$\overline{\text{C}}$ is low (character mode))
BLE = High: Blinking enable on the character specified by attribute RAM
BLE = Low: No blinking

3. WIDE (valid only when G/$\overline{\text{C}}$ is low (character mode))
WIDE = High: Wide display enabled
WIDE = Low: Normal display

4. G/$\overline{\text{C}}$
G/C = High: Graphic 1 display (when AT = Low) or Graphic 2 display (when AT = High)
G/C = Low: Character display

5. ON/$\overline{\text{OFF}}$
ON/$\overline{\text{OFF}}$ = High: Display on state
ON/$\overline{\text{OFF}}$ = Low: Display off state

Figure 33. Correspondence between Mode Register and External Pins

Restrictions on Programming Internal Registers

Note when programming that the values you can write into the internal registers is restricted as shown in Table 12.

Table 12. Restrictions on Writing Values into the Internal Registers

Function	Restrictions	Register
Display Format	$1 < Nhd < Nht + 1 \leqq 256$	R0, R1
	$Nhd + \frac{16}{m} *1 \leqq Nht + 1$	
	(No. of vertical dots) x (no. of horizontal dots) x (frame frequency; f_{FRM}) ≦ (data transfer speed; V)	R1, R19, R20
	$\begin{Bmatrix} 1 \\ 2 \end{Bmatrix} *2 \times (Nd + 1) \times Nhd \times \begin{Bmatrix} 8 \\ 16 \end{Bmatrix} *3\ f_{FRM} \leqq V$	
	$Nhd \leqq Nir$	R1, R18
	$0 \leqq Nd \leqq 511$	R19, R20
Cursor Control	$0 \leqq Ncs \leqq Nce$	R10, R11
	$Nce \leqq Nr$	R10, R9
Smooth Scroll	$Nsr \leqq Nr$	R21, R9
Memory Width Set	$0 \leqq Nir \leqq 255$	R18

*1 m varies according to the modes. See the following table.

Mode No.	m
5,9	1
1,6,7,8,10,11,12,13	2
2,3,4	4

*2 Set 1 when an LCD screen is a single screen, and set 2 when dual. Modes are classified as shown in the following table.

Mode No.	Value
5,6,7,8,9,10,11,12	1
1,2,3,4,13	2

*3 Set 8 when a character is constructed with 8 dots, and set 16 when with 16 dots. Modes are classified as shown in the following table.

Mode No.	Value
1,5,9	8
2,3,4,6,7,8,10,11,12,13	16

Reset

$\overline{\text{RES}}$ pin determines the internal state of LSI counters and the like. This pin does not affect register contents nor does it basically control output terminals.

"Reset" is defined as follows (Figure 34) :

- ○ At reset: the time when $\overline{\text{RES}}$ goes low
- ○ During reset: the period while $\overline{\text{RES}}$ remains low
- ○ After reset: the period on and after the $\overline{\text{RES}}$ transition from low to high

$\overline{\text{RES}}$ pin should be pulled high by users during operation.

Reset State of Pins

$\overline{\text{RES}}$ pin does not basically control output pins, and operates regardless of other input pins.

(1) Preserves states before reset :
LU0-LU3, LD0-LD3, FLM, CL1, RA0-RA4

(2) Fixed at high level :
MLCK

(3) Preserves states before reset or fixed at low level according to the timing when the reset signal is input :
DISPTMG, CUDISP, MA0-MA15

(4) Fixed at high or low according to mode :
CL2

(5) Unaffected :
DB_0-DB_7

Reset State of Registers

$\overline{\text{RES}}$ pin does not affect register contents. Therefore, registers can be read or written even during a reset state ; their contents will be preserved regardless of reset until they are rewritten to.

Notes for HD63645/HD64645

(1) The HD63645/HD64645 are CMOS LSIs, and it should be noted that input pins must not be left disconnected, etc.

(2) At power-on, the state of internal registers becomes undefined. The LSI operation is undefined until all internal registers have been programmed.

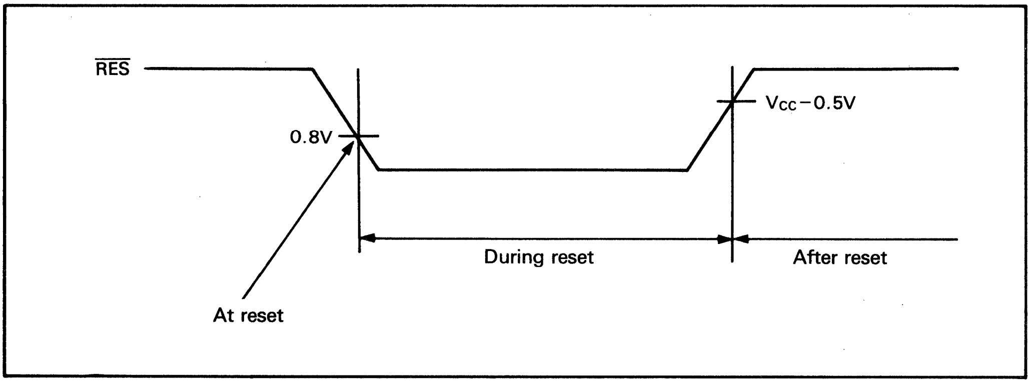


Figure 34. Reset Definition

Absolute Maximum Ratings

Item	Symbol	Value	Note
Supply voltage	V_{CC}	−0.3 to +7.0 V	2
Terminal voltage	V_{in}	−0.3 to V_{CC} +0.3 V	2
Operating temperature	T_{opr}	−20°C to +75°C	
Storage temperature	T_{stg}	−55°C to +125°C	

Notes : 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 5.0 V ±10%, GND = 0 V, Ta = −20°C to +75°C). If these conditions are exceeded, it could affect reliability of LSI.

2. Width respect to GROUND (GND = 0 V)

Electrical Characteristics

DC characteristics (V_{CC} = 5.0 V ±10%, GND = 0 V, T_a = −20°C to +75°C, unless otherwise noted.)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high voltage	$\overline{\text{RES}}$, MODE, SK0, SK1	V_{IH}	V_{CC}−0.5		V_{CC}+0.3	V	
	DCLK, ON/$\overline{\text{OFF}}$		2.2		V_{CC}+0.3	V	
	All others		2.0		V_{CC}+0.3	V	
Input low voltage	All others	V_{IL}	−0.3		0.8	V	
Output high voltage	TTL Interface[1]	V_{OH}	2.4			V	I_{OH} = −400 μA
	CMOS Interface[1]		V_{CC}−0.8			V	I_{OH} = −400 μA
Output low voltage	TTL Interface	V_{OL}			0.4	V	I_{OL} = 1.6mA
	CMOS Interface				0.8	V	I_{OL} = 400 μA
Input leakage current	All inputs except DB_0-DB_7	I_{IL}	−2.5		+2.5	μA	
Three state (off-state) leakage current	DB_0-DB_7	I_{TSL}	−10		+10	μA	
Current dissipation[2]		I_{CC}			10	mA	

Notes: 1. TTL Interface ; MA0-MA15, RA0-RA4, DISPTMG, CUDISP, DB0-DB7, MCLK
C-MOS Interface ; LU0-LU3, LD0-LD3, CL1, CL2, M, FLM

2. Input/output current is excluded. When input is at the intermediate level with CMOS, excessive current flows through the input circuit to power supply. Input level must be fixed at high or low to avoid this condition.

3. If the capacity loads of LU0-LU3 and LD0-LD3 exceed the rating, noise over 0.8 V may be produced on CUDISP, DISPTMG, MCLK, FLM and M. In case the loads of LU0-LU3 and LD0-LD3 are larger than the ratings, supply signals to the LCD module through buffers.

AC Characteristics

CPU Interface (HD63645 —— 68 family)

Item	Symbol	Min	Typ	Max	Unit	Figure
Enable cycle time	t_{CYCE}	500			ns	35
Enable pulse width (high)	P_{WEH}	220			ns	
Enable pulse width (low)	P_{WEL}	220			ns	
Enable rise time	t_{Er}			25	ns	
Enable fall time	t_{Ef}			25	ns	
$\overline{CS}$, RS, R/$\overline{W}$ setup time	t_{AS}	70			ns	
$\overline{CS}$, RS, R/$\overline{W}$ hold time	t_{AH}	10			ns	
DB$_0$-DB$_7$ setup time	t_{DS}	60			ns	
DB$_0$-DB$_7$ hold time	t_{DHW}	10			ns	
DB$_0$-DB$_7$ output delay time	t_{DDR}			150	ns	
DB$_0$-DB$_7$ output hold time	t_{DHR}	20			ns	

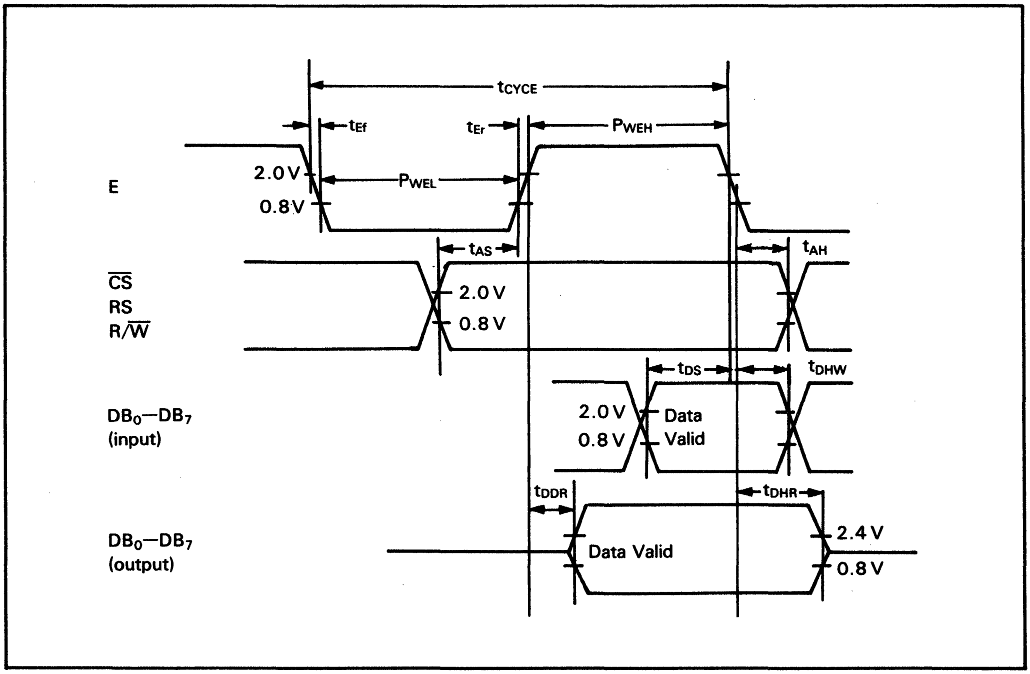


Figure 35. CPU Interface (HD63645)

CPU Interface (HD64645 —— 80 family)

Item	Symbol	Min	Typ	Max	Unit	Figure
$\overline{RD}$ high level width	t_{WRDH}	190			ns	36
$\overline{RD}$ low level width	t_{WRDL}	190			ns	
$\overline{WR}$ high level width	t_{WWRH}	190			ns	
$\overline{WR}$ low level width	t_{WWRL}	190			ns	
$\overline{CS}$, RS setup time	t_{AS}	0			ns	
$\overline{CS}$, RS hold time	t_{AH}	0			ns	
DB_0-DB_7 setup time	t_{DSW}	100			ns	
DB_0-DB_7 hold time	t_{DHW}	0			ns	
DB_0-DB_7 output delay time	t_{DDR}			150	ns	
DB_0-DB_7 output hold time	t_{DHR}	20			ns	

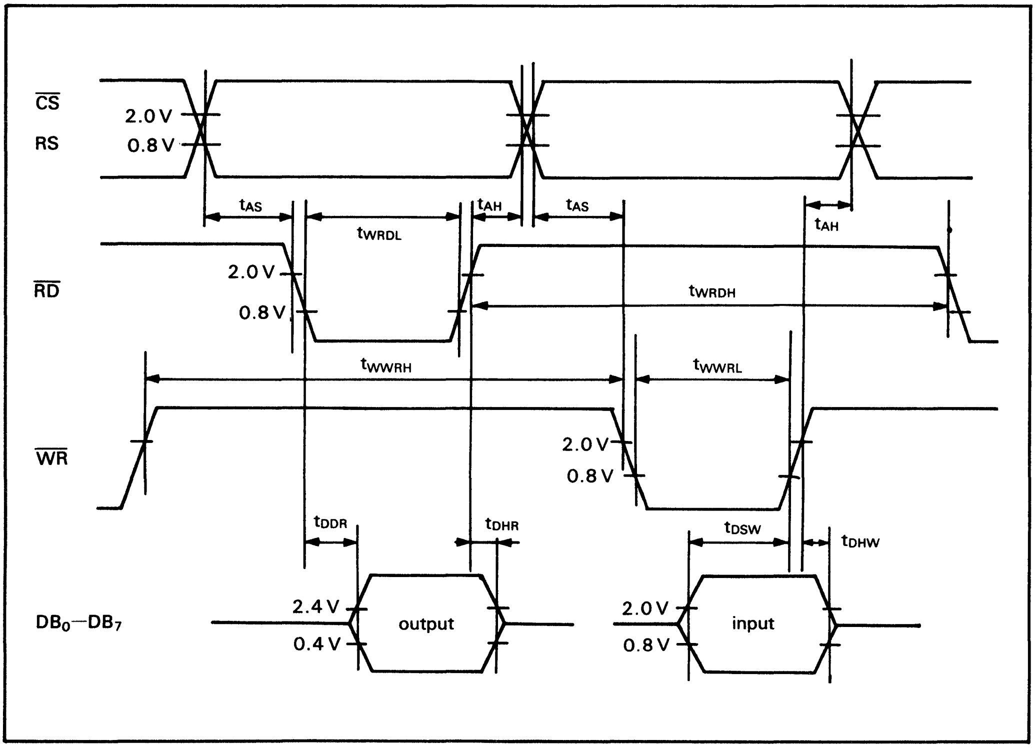


Figure 36. CPU Interface (HD64645)

AC Characteristics (Cont)

Memory Interface

Item	Symbol	Min	Typ	Max	Unit	Figure
DCLK cycle time	t_{CYCD}	100			ns	37
DCLK high level width	t_{WDH}	30			ns	
DCLK low level width	t_{WDL}	30			ns	
DCLK rise time	t_{Dr}			20	ns	
DCLK fall time	t_{Df}			20	ns	
MCLK delay time	t_{DMD}			70	ns	
MCLK rise time	t_{Mr}			30	ns	
MCLK fall time	t_{Mf}			30	ns	
MA0-MA15 delay time	t_{MAD}			150	ns	
MA0-MA15 hold time	t_{MAH}	10			ns	
RA0-RA4 delay time	t_{RAD}			150	ns	
RA0-RA4 hold time	t_{RAH}	10			ns	
DISPTMG delay time	t_{DTD}			150	ns	
DISPTMG hold time	t_{DTH}	10			ns	
CUDISP delay time	t_{CDD}			150	ns	
CUDISP hold time	t_{CDH}	10			ns	
CL1 delay time	t_{CL1D}			150	ns	
CL1 hold time	t_{CL1H}	10			ns	
CL1 rise time	t_{CL1r}			50	ns	
CL1 fall time	t_{CL1f}			50	ns	
MD0-MD15 setup time	t_{MDS}	30			ns	
MD0-MD15 hold time	t_{MDH}	15			ns	

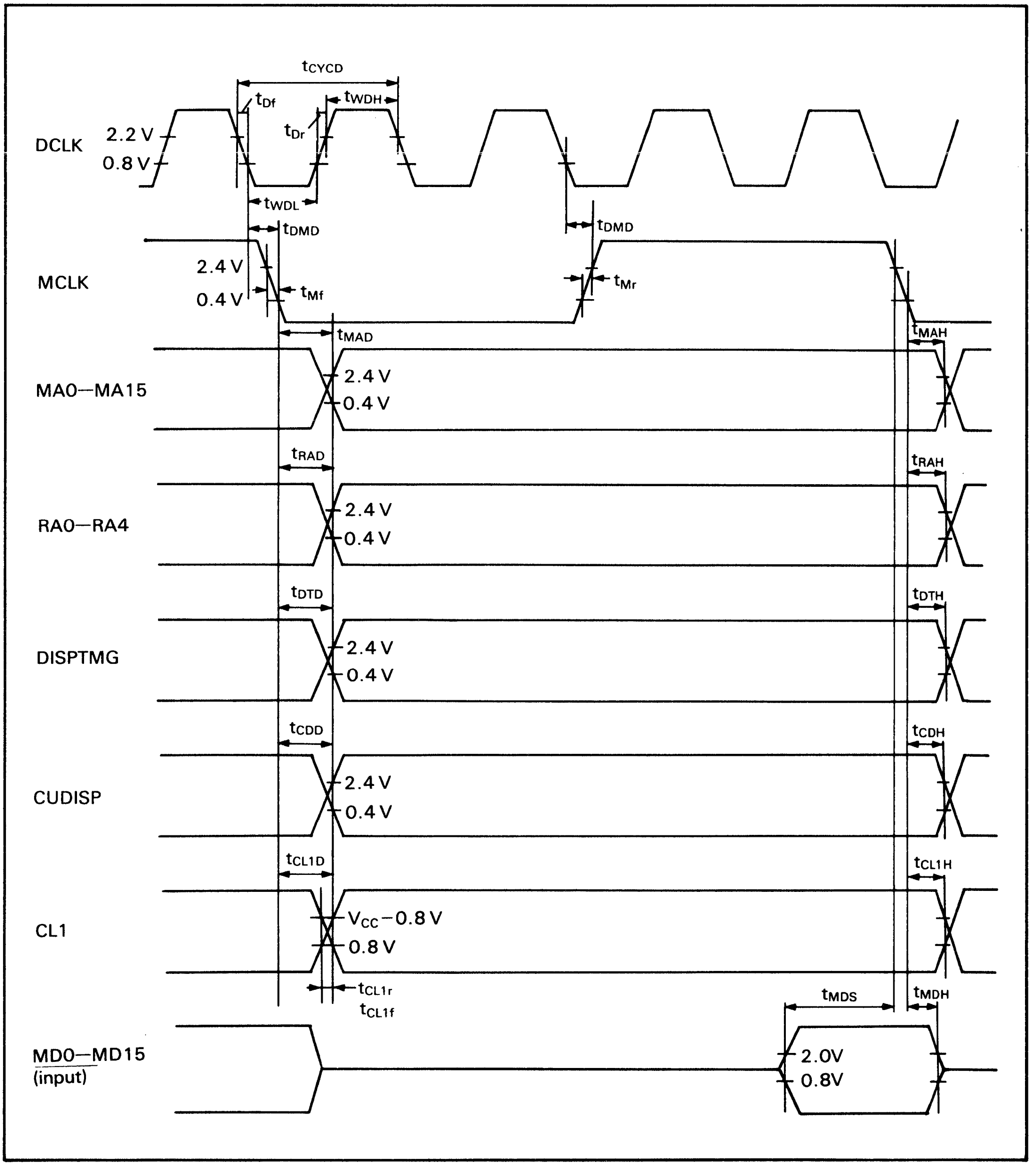


Figure 37. Memory Interface

AC Characteristics (Cont)

LCD Interface

Item	Symbol	Min	Typ	Max	Unit	Figure
Display data setup time	t_{LDS}	50			ns	38
Display data hold time	t_{LDH}	100			ns	
CL2 high level width	t_{WCL2H}	100			ns	
CL2 low level width	t_{WCL2L}	100			ns	
FLM setup time	t_{FS}	500			ns	
FLM hold time	t_{FH}	300			ns	
CL1 rise time	t_{CL1r}			50	ns	
CL1 fall time	t_{CL1f}			50	ns	
CL2 rise time	t_{CL2r}			50	ns	
CL2 fall time	t_{CL2f}			50	ns	

Note : At fCL2 = 3 MHz

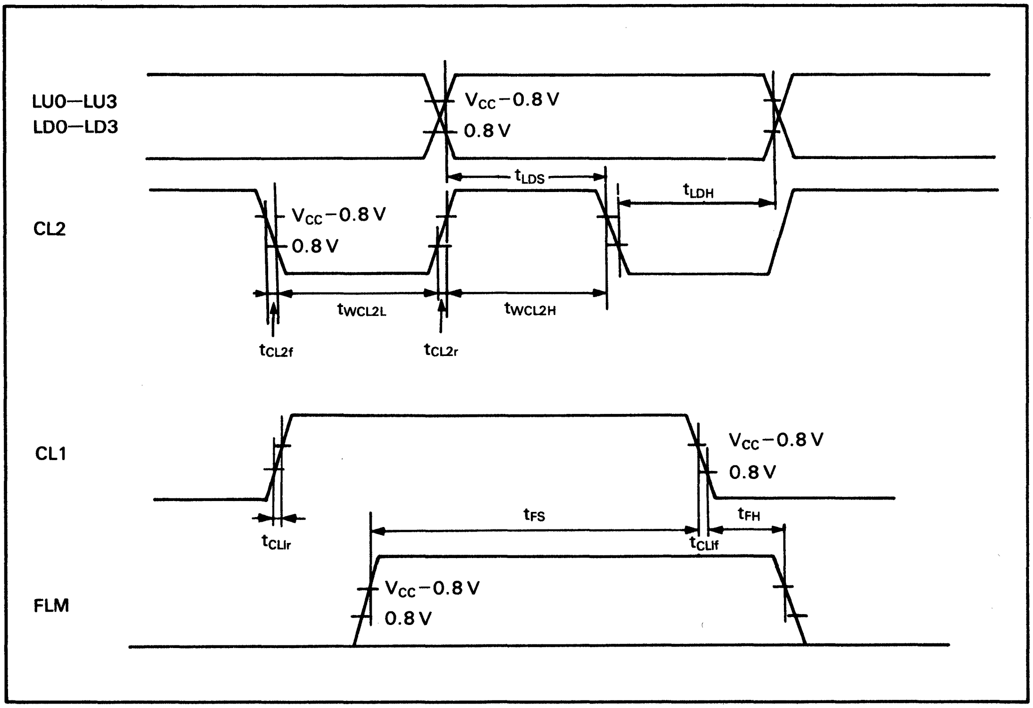
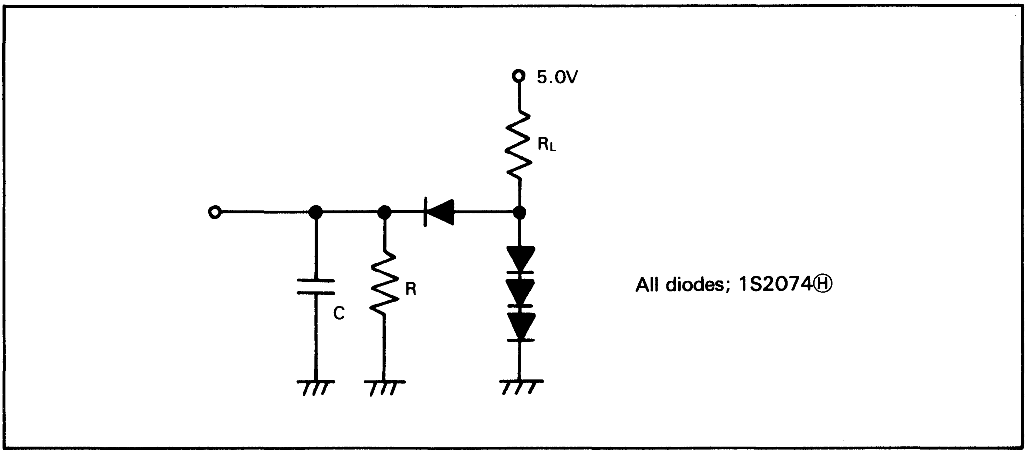


Figure 38. LCD Interface

AC Characteristics

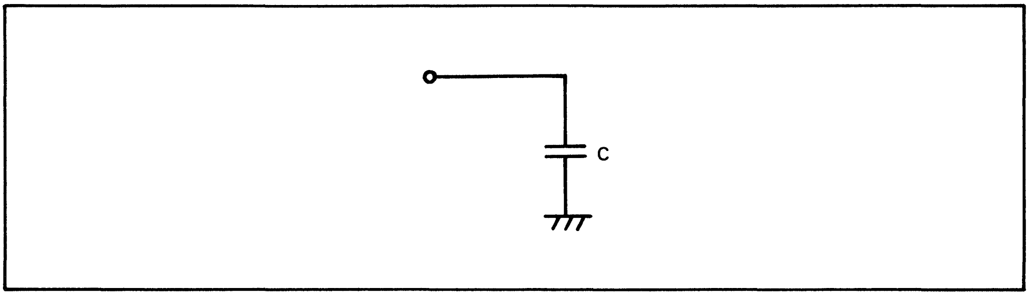
TTL Load

Terminal	**R_L**	**R**	**C**	**Remarks**
DB_0-DB_7	2.4 kΩ	11 kΩ	130 pF	tr, tf : Not specified
MA0-MA15, RA0-RA4, DISPTMG, CUDISP	2.4 kΩ	11kΩ	40 pF	
MCLK	2.4 kΩ	11 kΩ	30 pF	tr, tf : Specified



Capacity Load

Terminal	**C**	**Remarks**
CL2	150 pF	tr, tf : Specified
CL1	200 pF	
LU0-LU3, LD0-LD3, M	150 pF	tr, tf : Not specified
FLM	50 pF	



HD64646

LCD Timing Controller (LCTC)

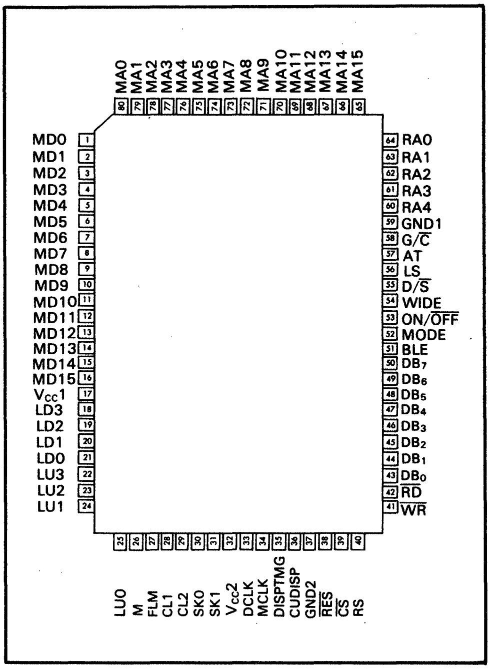
Description

The HD64646 LCTC is a modified version of the HD64645 LCTC with differente LCD interface timing.
The HD64646 is a control LSI for large size dot matrix liquid crystal displays. The LCTC is software compatible with the HD6845 CRTC, since its programming method of internal registers and memory addresses is based on the CRTC. A display system can be easily converted from a CRT to an LCD.

The LCTC offers a variety of functions and performance features such as vertical and horizontal scrolling, and various types of character attribute functions such as reverse video, blinking, nondisplay (white or black), and an OR function for simple superimposition of character and graphic displays. The LCTC also provides DRAM refresh address output.

A compact LCD system with a large screen can be configured by connecting the LCTC with the HD61104 (column driver) and the HD61105 (common driver) by utilizing 4-bit × 2 data outputs. Power dissipation has been lowered by adopting the CMOS process.

Pin Arrangement



Features

- Software compatible with the HD6845 CRTC
- Programmable screen size:
  —Up to 1024 dots (height)
  —Up to 4096 dots (width)
- High-speed data transfer:
  —Up to 20 Mbits/sec in character mode
  —Up to 40 Mbits/sec in graphic mode
- Selectable single or dual screen configuration
- Programmable multiplexing duty ratio: static to 1/512 duty cycle
- Programmable character font:
  —1-32 dots (height)
  —8 dots (width)
- Versatile character attributes: reverse video, blinking, nondisplay (white), nondisplay (black)
- OR function: superimposing characters and graphics display
- Cursor with programmable height, blink rate, display position, and on/off switch
- Vertical smooth scrolling and horizontal scrolling by the character
- Versatile display modes programmable by mode register or external pins: display on/off, graphic or character, normal or wide, attributes, and blink enable
- Refresh address output for dynamic RAM
- 4- or 8-bit parallel data transfer between LCTC and LCD driver
- Recommended LCD driver: HD61104 (column) and HD61105 (common), HD66106 (column/common)
- CPU interface:
  80 family
- CMOS process
- Single +5 V ±10%
- 80-pin plastic QFP (FP-80A)

Ordering Information

Type No.	Bus Timing	Bus Interface	Package
HD63645	2 MHz	68 System	FP-80
HD64645	4 MHz	80 System	FP-80
HD64646	4 MHz	80 System	FP-80B

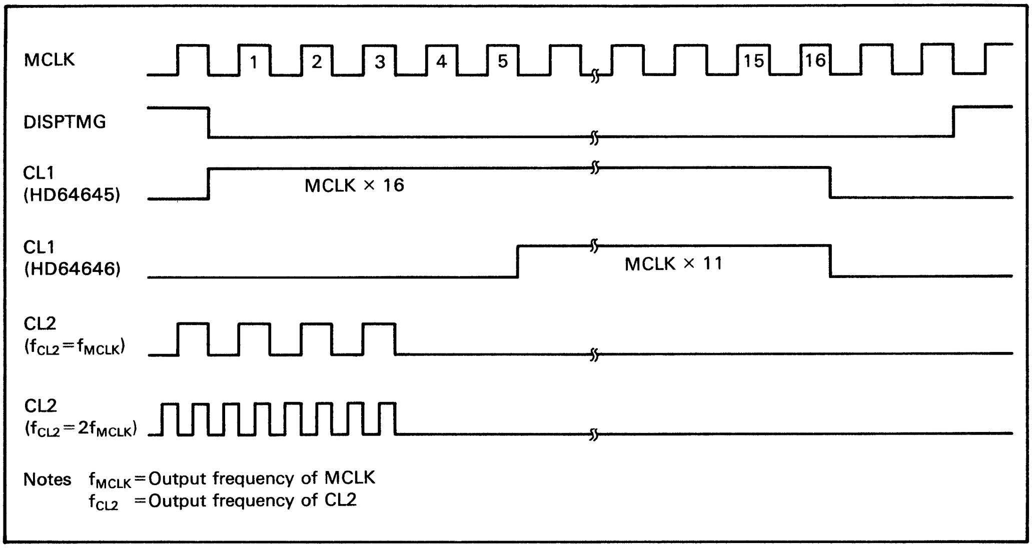
Differences Between HD64645 and HD64646

Fig.1 and Fig.2 show the relation between display data transfer period, when display data shift clock CL2 changes, and display data latch clock CL1. Fig.1 shows the case without skew function and fig.2 shows the case with skew function.

In Fig.1 "High" period between CL2 and CL1 of HD64645 overlap.

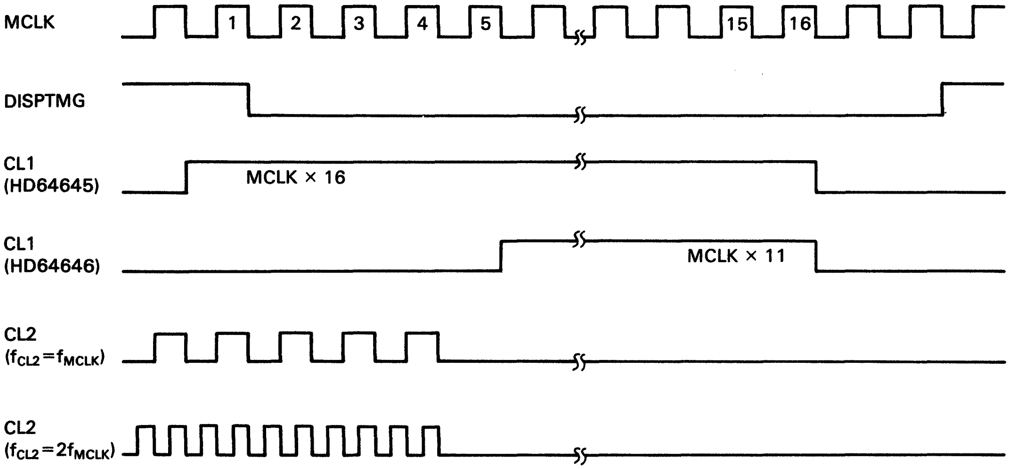
HD64646 has no overlap like HD64645, and except for overlap parts HD64646 is the same as HD64645 functionally.

Besides, in case of skew function, phase relation between CL1 and CL2 changes. As Fig.2 shows, data transfer period and CL1 "High" period of HD64646 never overlap in case of skew function.

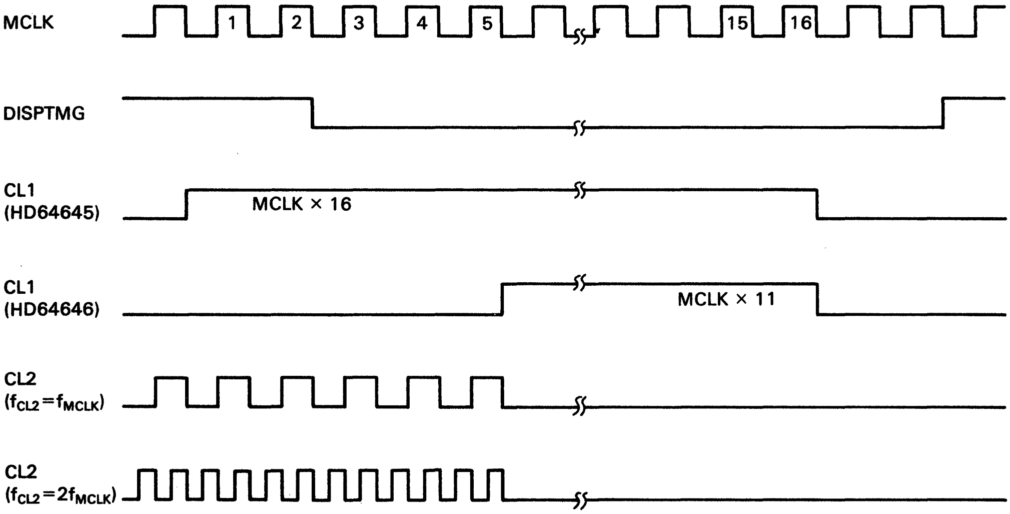


Notes f_{MCLK}=Output frequency of MCLK
f_{CL2} =Output frequency of CL2

Figure 1. Differences between HD64645 and HD64646 (no skew)



(a) 1 character skew



(b) 2 character skew

Figure 2. Differences between HD64645 and HD64646 (skew)

Absolute Maximum Ratings

Item	Symbol	Value	Note
Supply voltage	V_{CC}	−0.3 to +7.0 V	2
Terminal voltage	V_{in}	−0.3 to V_{CC} +0.3 V	2
Operating temperature	T_{opr}	−20°C to +75°C	
Storage temperature	T_{stg}	−55°C to +125°C	

Notes : 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 5.0 V ±10%, GND = 0 V, Ta = −20°C to +75°C). If these conditions are exceeded, it could affect reliability of LSI.

2. With respect to GROUND (GND = 0 V)

Electrical Characteristics

DC characteristics (V_{CC} = 5.0 V ±10%, GND = 0 V, T_a = −20°C to +75°C, unless otherwise noted.)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high voltage	$\overline{\text{RES}}$, MODE, SK0, SK1	V_{IH}	$V_{CC}-0.5$		$V_{CC}+0.3$	V	
	DCLK, ON/$\overline{\text{OFF}}$		2.2		$V_{CC}+0.3$	V	
	All others		2.0		$V_{CC}+0.3$	V	
Input low voltage	All others	V_{IL}	−0.3		0.8	V	
Output high voltage	TTL Interface[1]	V_{OH}	2.4			V	$I_{OH}=-400\mu A$
	CMOS Interface[1]		$V_{CC}-0.8$			V	$I_{OH}=-400\mu A$
Output low voltage	TTL Interface	V_{OL}			0.4	V	$I_{OL}=1.6mA$
	CMOS Interface				0.8	V	$I_{OL}=400\mu A$
Input leakage current	All inputs except DB_0-DB_7	I_{IL}	−2.5		+2.5	μA	
Three state (off-state) leakage current	DB_0-DB_7	I_{TSL}	−10		+10	μA	
Current dissipation[2]		I_{CC}			10	mA	

Notes : 1. TTL Interface ; MA0-MA15, RA0-RA4, DISPTMG, CUDISP, DB0-DB7, MCLK
C-MOS Interface ; LU0-LU3, LD0-LD3, CL1, CL2, M, FLM

2. Input/output current is excluded. When input is at the intermediate level with CMOS, excessive current flows through the input circuit to power supply. Input level must be fixed at high or low to avoid this condition.

3. If the capacity loads of LU0-LU3 and LD0-LD3 exceed the rating, noise over 0.8 V may be produced on CUDISP, DISPTMG, MCLK, FLM and M. In case the loads of LU0-LU3 and LD0-LD3 are larger than the ratings, supply signals to the LCD module through buffers.

AC Characteristics

CPU Interface

Item	Symbol	Min	Typ	Max	Unit	Figure
$\overline{\text{RD}}$ high level width	t_{WRDH}	190			ns	3
$\overline{\text{RD}}$ low level width	t_{WRDL}	190			ns	
$\overline{\text{WR}}$ high level width	t_{WWRH}	190			ns	
$\overline{\text{WR}}$ low level width	t_{WWRL}	190			ns	
$\overline{\text{CS}}$, RS setup time	t_{AS}	0			ns	
$\overline{\text{CS}}$, RS hold time	t_{AH}	0			ns	
DB_0-DB_7 setup time	t_{DSW}	100			ns	
DB_0-DB_7 hold time	t_{DHW}	0			ns	
DB_0-DB_7 output delay time	t_{DDR}			150	ns	
DB_0-DB_7 output hold time	t_{DHR}	20			ns	

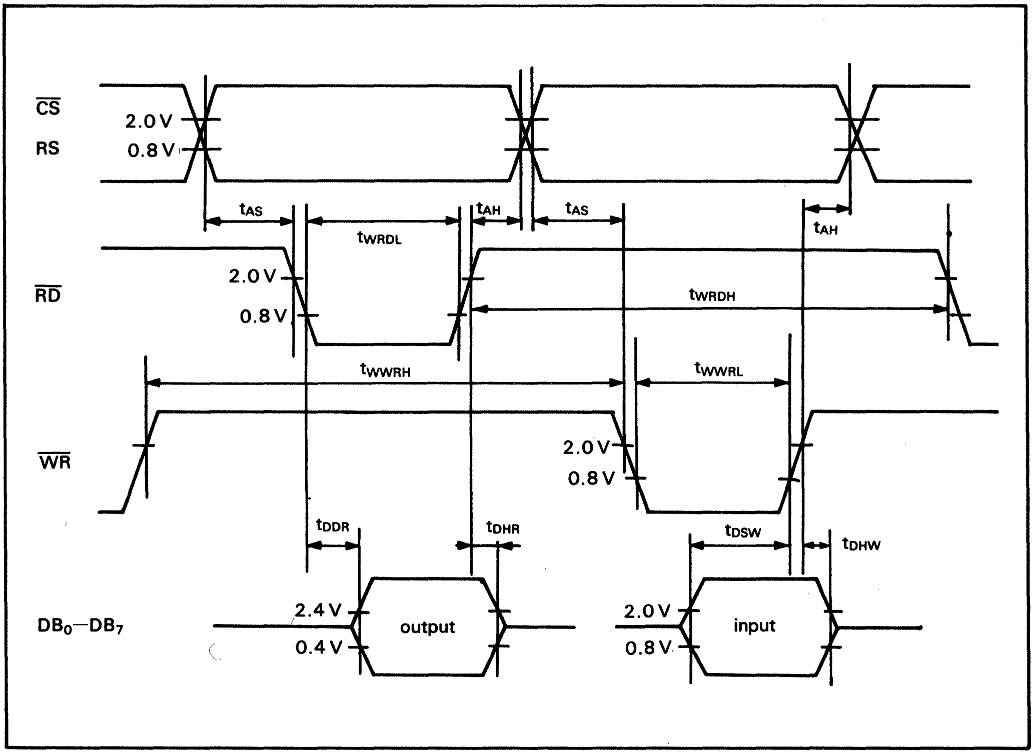


Figure 3. CPU Interface

AC Characteristics (Cont)

Memory Interface

Item	Symbol	Min	Typ	Max	Unit	Figure
DCLK cycle time	t_{CYCD}	100			ns	4
DCLK high level width	t_{WDH}	30			ns	
DCLK low level width	t_{WDL}	30			ns	
DCLK rise time	t_{Dr}			20	ns	
DCLK fall time	t_{Df}			20	ns	
MCLK delay time	t_{DMD}			60	ns	
MCLK rise time	t_{Mr}			30	ns	
MCLK fall time	t_{Mf}			30	ns	
MA0-MA15 delay time	t_{MAD}			150	ns	
MA0-MA15 hold time	t_{MAH}	10			ns	
RA0-RA4 delay time	t_{RAD}			150	ns	
RA0-RA4 hold time	t_{RAH}	10			ns	
DISPTMG delay time	t_{DTD}			150	ns	
DISPTMG hold time	t_{DTH}	10			ns	
CUDISP delay time	t_{CDD}			150	ns	
CUDISP hold time	t_{CDH}	10			ns	
CL1 delay time	t_{CL1D}			150	ns	
CL1 hold time	t_{CL1H}	10			ns	
CL1 rise time	t_{CL1r}			50	ns	
CL1 fall time	t_{CL1f}			50	ns	
MD0-MD15 setup time	t_{MDS}	30			ns	
MD0-MD15 hold time	t_{MDH}	15			ns	

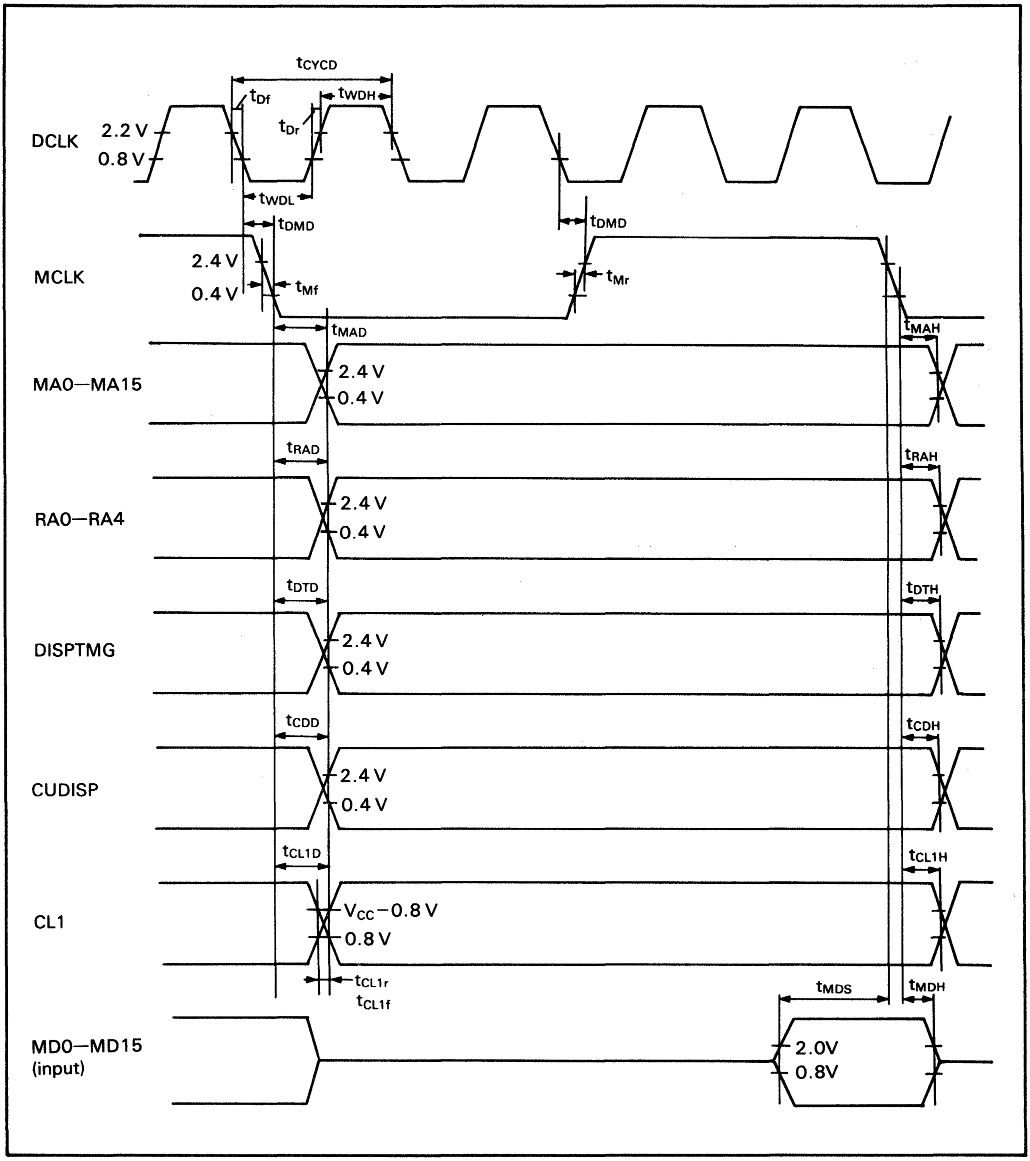


Figure 4. Memory Interface

AC Characteristics (Cont)

LCD Interface 1 (at f_{CL2}=3MHz)

Item	Symbol	Min	Typ	Max	Unit	Figure
FLM stetup time	t_{FS}	500	–	–	ns	5
FLM hold time	t_{FH}	300	–	–	ns	
M delay time	t_{DM}	–	–	200	ns	
CL1 high level width	t_{CL1H}	300	–	–	ns	
Clock setup time	t_{SCL}	500	–	–	ns	
Clock hold time	t_{HCL}	100	–	–	ns	
Phase difference 1	t_{PD1}	100	–	–	ns	
Phase difference 2	t_{PD2}	500	–	–	ns	
CL2 high level width	t_{CL2H}	100	–	–	ns	
CL2 low level width	t_{CL2L}	100	–	–	ns	
CL2 rise time	t_{CL2r}	–	–	50	ns	
CL2 fall time	t_{CL2f}	–	–	50	ns	
Display data setup time	t_{LDS}	80	–	–	ns	
Display data hold time	t_{LDH}	100	–	–	ns	
Display data delay time	t_{LDD}	–	–	30	ns	

LCD Interface 2 (at f_{CL2}=5MHz)

Item	Symbol	Min	Typ	Max	Unit	Figure
FLM setup time	t_{FS}	500	–	–	ns	5
FLM hold time	t_{FH}	200	–	–	ns	
M delay time	t_{DM}	–	–	200	ns	
CL1 high level width	t_{CL1H}	300	–	–	ns	
Clock setup time	t_{SCL}	500	–	–	ns	
Clock hold time	t_{HCL}	100	–	–	ns	
Phase difference 1	t_{PD1}	70	–	–	ns	
Phase difference 2	t_{PD2}	500	–	–	ns	
CL2 high level width	t_{CL2H}	50	–	–	ns	
CL2 low level width	t_{CL2L}	50	–	–	ns	
CL2 rise time	t_{CL2r}	–	–	50	ns	
CL2 fall time	t_{CL2f}	–	–	50	ns	
Display data setup time	t_{LDS}	30	–	–	ns	
Display data hold time	t_{LDH}	30	–	–	ns	
Display data delay time	t_{LDD}	–	–	30	ns	

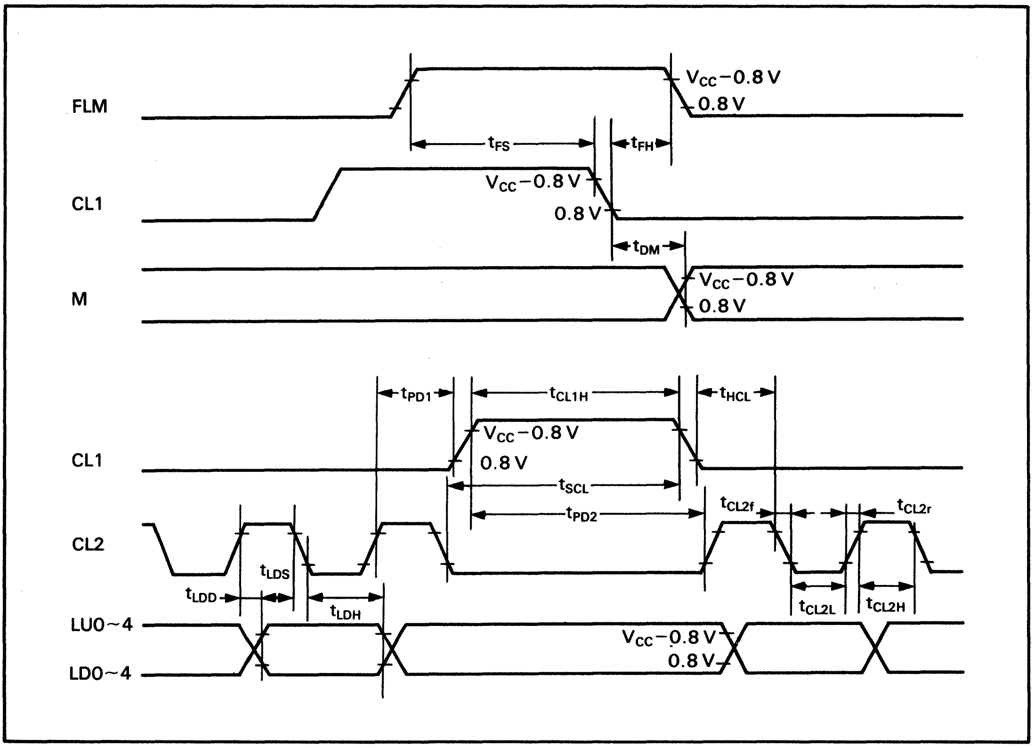
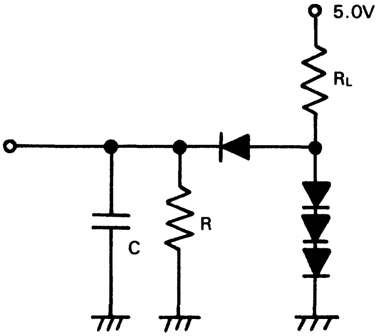


Figure 5. LCD Interface

AC Characteristics

TTL Load

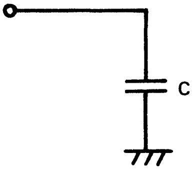
Terminal	R_L	R	C	Remarks
DB_0-DB_7	2.4 kΩ	11 kΩ	130 pF	tr, tf : Not specified
MA0-MA15, RA0-RA4, DISPTMG, CUDISP	2.4 kΩ	11 kΩ	40 pF	
MCLK	2.4 kΩ	11 kΩ	30 pF	tr, tf : Specified



All diodes; 1S2074Ⓗ

Capacity Load

Terminal	C	Remarks
CL2	150 pF	tr, tf : Specified
CL1	200 pF	
LU0-LU3, LD0-LD3, M	150 pF	tr, tf : Not specified
FLM	50 pF	



HD66840

LCD Video Interface Controller (LVIC)

Description

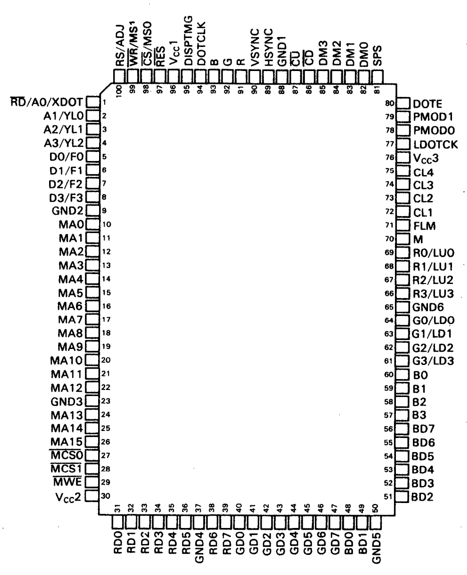
The HD66840 LVIC interface controller converts the standard video signals R, G, B for CRT display into LCD data. It enables a CRT display system to be replaced by an LCD system without any changes. It also enables the software originally intended for CRT display to control the LCD.

Since the LVIC can control TFT-type LCDs in addition to the current TN-type LCD, it can support color display as well as monochrome display. It can program screen size and can control a large-panel LCD of 720 dots × 512 dots (max).

Features

- Converts video R, G, B signals for CRT display into LCD data:
  —Monochrome display data
  —8-level gray scale display data
  —8-color display data
- Can select LVIC control method:
  —Pin programming method
  —Internal register programming method (either with MPU or ROM)
- Can program screen size:
  —200, 350, 400, 480, 512, or 540 dots (lines) in height and 640, or 720 dots (80, or 90 characters) in width by pin programming method
  —4-1024 dots (lines) in height and 32-4048 dots (4-506 characters) in width by internal register programming method
- Can regenerate the display timing signal from HSYNC and VSYNC
- Internal PLL circuit can generate the dot clock (external charge pump, low pass filter (LPF), and voltage-controlled oscillator (VCO) required)
- Can control both TN-type LCD and TFT-type LCD
- Maximum operating frequency: 25, 30 MHz (dot clock for CRT display)
- LCD driver interface: 4-, 8-, or 12-bit (4 bits each for R, G, B) parallel data transfer
- Recommended LCD drivers: HD61104, HD61105, and HD66106
- CMOS 1.3 μm process
- Single power supply: +5 V ± 10 %
- 100-pin plastic QFP (FP-100A)

Pin Arrangement



Pin Description

Table 1 describes the pins.

Table 1. Pin Description

Symbol	Pin Number	Pin Name	I/O
$V_{CC}1$-$V_{CC}3$	96, 30, 76	$V_{CC}1$, V_{CC} 2, V_{CC} 3	—
GND1-GND6	88, 9, 23, 37, 50, 65	Ground 1-6	—
R, G, B[1]	91, 92, 93	Red, green, blue serial data	I
HSYNC	89	Horizontal synchronization	I
VSYNC	90	Vertical synchronization	I
DISPTMG[2]	95	Display timing	I
DOTCLK	94	Dot clock	I
R0-R3[3]	69-66	LCD red data 0-3	O
LU0-LU3[4]	69-66	LCD up panel data 0-3	O
G0-G3[3,5]	64-61	LCD green data 0-3	O
LD0-LD3[4,5]	64-61	LCD down panel data 0-3	O
B0-B3[3,6]	60-57	LCD blue data 0-3	O
CL1	72	LCD data line clock	O
CL2	73	LCD data shift clock	O
CL3[7]	74	Y-driver shift clock 1	O
CL4[7]	75	Y-driver shift clock 2	O
FLM	71	First line marker	O
M	70	LCD driving signal alternation	O
LDOTCK	77	LCD dot clock	I
$\overline{\text{MCS0}}$, $\overline{\text{MCS1}}$[8]	27, 28	Memory chip select 0, 1	O
$\overline{\text{MWE}}$[9]	29	Memory write enable	O
MA0-MA15[9]	10-22, 24-26	Memory address 0-15	O
RD0-RD7[9]	31-36, 38-39	Memory red data 0-7	I/O
GD0-GD7[9,10]	40-47	Memory green data 0-7	I/O
BD0-BD7[9,10]	48, 49 51-56	Memory blue data 0-7	I/O

Ordering Information

Type No.	Dot clock (MHz)	Package
HD66840F25	25MHz	100-pin Plastic QFP (FP-100A)
HD66840F30	30MHz	

Table 1. Pin Description (cont)

Symbol	Pin Number	Pin Name	I/O
PMOD0, PMOD1	78, 79	Program mode 0, 1	I
DOTE	80	Dot clock edge change	I
SPS	81	Synchronization polarity select	I
DM0-DM3	82-85	Display mode 0-3	I
$\overline{CS}$ (MPU programming)[11]	98	Chip select	I
MS0 (pin programming)[11]	98	Memory select 0	I
$\overline{WR}$ (MPU programming)[11,12]	99	Write	I
MS1 (pin programming)[11]	99	Memory select 1	I
$\overline{RD}$ (MPU programming)[12]	1	Read	I
A0 (ROM programming)	1	Address 0	O
XDOT (pin programming)	1	X-dot	I
RS (MPU programming)[11]	100	Register select	I
ADJ (pin programming)[11]	100	Adjust	I
D0-D3 (MPU programming)	5-8	Data 0-3	I/O
D0-D3 (ROM programming)	5-8	Data 0-3	I
F0-F3 (pin programming)	5-8	Fine adjust 0-3	I
A1-A3 (ROM programming)[13]	2-4	Address 1-3	O
YL0-YL2 (pin programming)[13]	2-4	Y-line 0-2	I
$\overline{RES}$[14]	97	Reset	I
$\overline{CD}$	86	Charge down	O
$\overline{CU}$	87	Charge up	O

Notes:
1. When CRT display data is monochrome, G and B pins should be fixed low.
2. Fix high or low when regenerating the display timing signal internally.
3. For 8-color display modes.
4. For monochrome and 8-level gray scale display modes.
5. Leave disconnected in 4-bit/single screen data transfer modes.
6. Leave disconnected in monochrome and 8-level gray scale display modes.
7. Leave disconnected when controlling TN-type LCD.
8. Leave disconnected when using no buffer memories.
9. Leave disconnected when using no buffer memories.
10. In monochrome display modes, the LVIC writes the OR of R, G, B signals into R-plane RAMs. Thus, no RAMs are required for G and B planes in these modes.
    Pull up these pins 20-kΩ resistance. If G and B plane RAMs are connected in monochrome display modes, the LVIC writes G and B signals into each RAM. However, it does not affect the display or the contents of R-plane RAM whether G- and B-plane RAMs are connected or not.
11. Fix high or low when controlling the LVIC by ROM programming method.
12. $\overline{WR}$ and $\overline{RD}$ must not be low at the same time.
13. Fix high or low when controlling the LVIC by MPU programming method.
14. Make sure to input $\overline{RES}$ signal after power-on.

Power Supply

$V_{CC}1$-$V_{CC}3$: Connect $V_{CC}1$-$V_{CC}3$ with +5 V.

GND1-GND6: Ground GND1-GND6.

CRT Display Interface

R, G, B: Input CRT display R, G, B signals on R, G and B respectively.

HSYNC: Input the CRT horizontal synchronization on HSYNC.

VSYNC: Input the CRT vertical synchronization on VSYNC.

DISPTMG: Input the display timing signal, which announces the horizontal or vertical display period, on DISPTMG.

DOTCLK: Input the dot clock for CRT display on DOTCLK.

LCD Interface

R0-R3: R0-R3 output R data for the LCD.

LU0-LU3: LU0-LU3 output LCD up panel data.

G0-G3: G0-G3 output G data for LCD.

LD0-LD3: LD0-LD3 output LCD down panel data.

B0-B3: B0-B3 output B data for LCD.

CL1: CL1 outputs the line select clock for LCD data.

CL2: CL2 outputs the shift clock for LCD data.

CL3: CL3 outputs the line select and shift clock when a Y-driver is set on one side of an LCD screen (see "LCD System Configuration").

CL4: CL4 outputs the line select and shift clock when Y-drivers are set on both sides of an LCD screen (see "LCD System Configuration").

FLM: FLM outputs the first line marker for a Y-driver.

M: The M output signal converts the LCD drive signal to AC.

LDOTCK: LDOTCK outputs the LCD dot clock.

Buffer Memory Interface

$\overline{\text{MCS0}}$, $\overline{\text{MCS1}}$: $\overline{\text{MCS0}}$ and $\overline{\text{MCS1}}$ output the buffer memory chip select signal.

$\overline{\text{MWE}}$: $\overline{\text{MWE}}$ outputs the write enable signal of buffer memories.

MA0-MA15: MA0-MA15 output buffer memory addresses.

RD0-RD7: RD0-RD7 transfer data between R data buffer memory and the LVIC.

GD0-GD7: GD0-GD7 transfer data between G data buffer memory and the LVIC.

BD0-BD7: BD0-BD7 transfer data between B data buffer memory and the LVIC.

Mode Setting

PMOD0, PMOD1: The PMOD0-PMOD1 input signals select a programming method (table 6).

DOTE: The DOTE input signal switches the timing of the data latch. The LVIC latches R, G, B signal at the falling edge of DOTCLK when DOTE is high, and at the rising edge when low.

SPS: The SPS input signal selects the polarity of VSYNC. (The polarity of HSYNC is fixed.) VSYNC is high active when SPS is high, and low active when low.

DM0-DM3: The DM0-DM3 input signals select a display mode (table 8).

MS0-MS1: The MS0-MS1 input signals select the kind of buffer memories (table 2).

XDOT: The XDOT input signal specifies the number of horizontal displayed characters. The number is 90 when XDOT is high, and 80 when low.

YL0-YL2: The YL0-YL2 input signals specify the number of vertical displayed lines (table 3).

ADJ: The ADJ input signal determines whether F0-F3 pins adjust the number of vertical displayed lines or the display timing signal. F0-F3 pins adjust the display timing signal when ADJ is high, and adjust the number of vertical displayed lines when low.

F0-F3: F0-F3 input data for adjusting the number of vertical displayed lines (table 4), or the display timing signal (see "Fine

Adjustment of Display Timing Signal").

MPU Interface

$\overline{CS}$: The MPU selects the LVIC when $\overline{CS}$ is low.

$\overline{WR}$: The MPU inputs the $\overline{WR}$ write signal to write data into internal registers of the LVIC. The MPU can write data when $\overline{WR}$ is low and cannot write data when high.

$\overline{RD}$: The MPU inputs the $\overline{RD}$ read signal to read data from internal registers of the LVIC. The MPU can read data when $\overline{RD}$ is low and cannot read data when high.

RS: The MPU inputs the RS signal together with $\overline{CS}$ to select internal registers. The MPU selects data registers (R0-R15) when RS is high and $\overline{CS}$ is low, and selects the address register (AR) when RS is low and $\overline{CS}$ is low.

D0-D3: D0-D3 transfer internal register data between the MPU and LVIC.

$\overline{RES}$: $\overline{RES}$ inputs the external reset signal.

ROM Interface

A0-A3: A0-A3 output address 0 to address 3 to an external ROM.

D0-D3: D0-D3 input data from an external ROM to internal registers.

PLL Circuit Interface

$\overline{CD}$: $\overline{CD}$ outputs the charge down signal to an external charge pump.

$\overline{CU}$: $\overline{CU}$ outputs the charge up signal to an external charge pump.

Table 2. Memory Type and MS1, MS0 Pins

MS1	MS0	Memory Type
0	0	No memory
0	1	8-kbyte memory
1	0	32-kbyte memory
1	1	64-kbyte memory

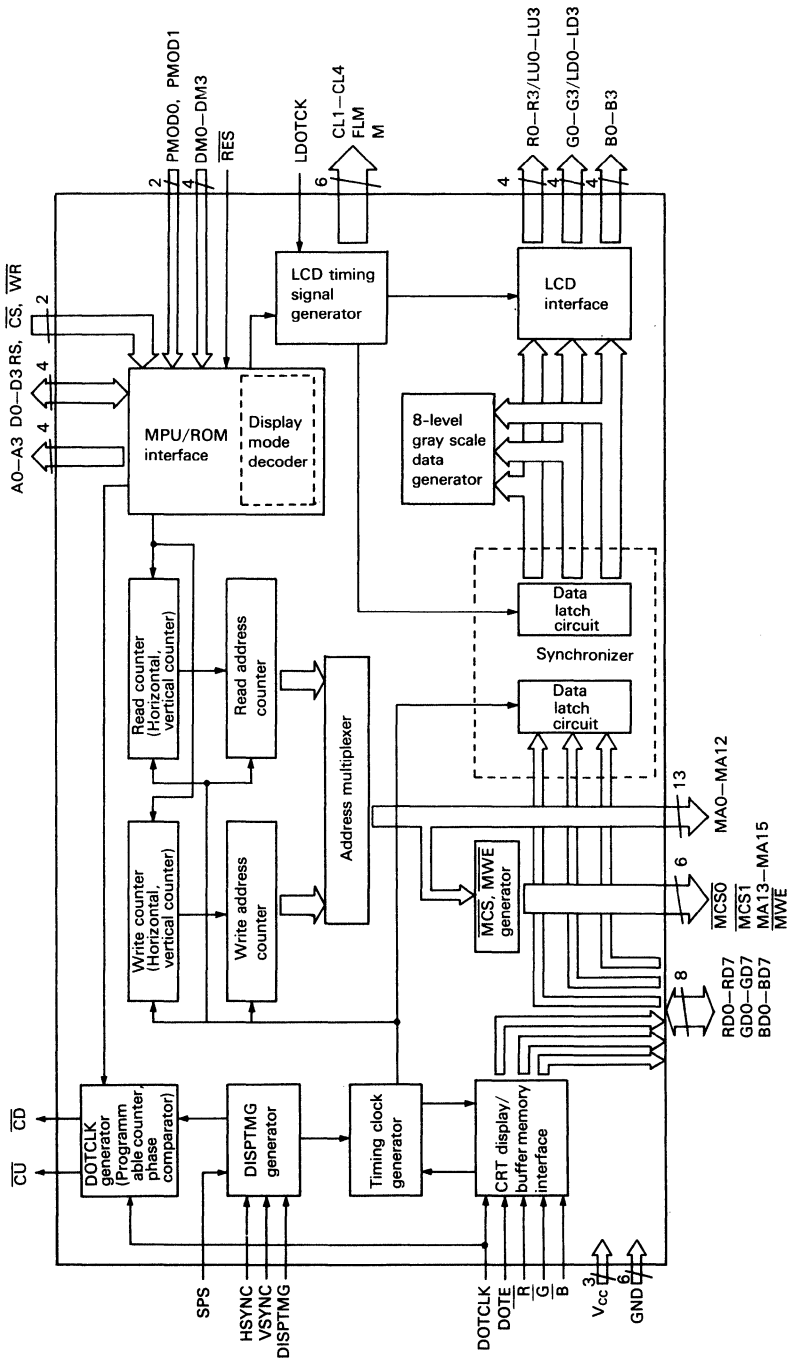
Table 3. Number of Vertical Displayed Lines and YL0-YL2 Pins

YL2	YL1	YL0	Number of Vertical Displayed Lines
0	0	0	200
0	0	1	350
0	1	0	400
0	1	1	480
1	0	0	512
1	0	1	540
1	1	0	Prohibited
1	1	1	

Table 4. Fine Adjustment of Vertical Displayed Lines

F3	F2	F1	F0	Number of Lines Adjusted
0	0	0	0	± 0
0	0	0	1	+ 1
0	0	1	0	+ 2
⋮	⋮	⋮	⋮	⋮
1	1	1	0	+ 14
1	1	1	1	+ 15

Internal Block Diagram



Registers

Table 5 lists the internal registers and figure 1 illustrates the bit assignment to the registers.

Table 5. Register List

		Address Register				Reg.		Program	Read/
$\overline{\text{CS}}$	**RS**	**3**	**2**	**1**	**0**	**No.**	**Register Name**	**Unit**	**Write**
1	—	—	—	—	—	—	Invalid	—	—
0	0	—	—	—	—	AR	Address register[1]	—	W
0	1	0	0	0	0	R0	Control register 1	—	R/W
0	1	0	0	0	1	R1	Control register 2	—	R/W
0	1	0	0	1	0	R2	Vertical displayed lines register (middle-order)[2]	Line	R/W
0	1	0	0	1	1	R3	Vertical displayed lines register (low-order)[2]	Line	R/W
0	1	0	1	0	0	R4	Vertical displayed lines register (high-order)[2]	Line	R/W
							CL3 period register (high-order)[3]	Char	R/W
0	1	0	1	0	1	R5	CL3 period register (low-order)[3]	Char	R/W
0	1	0	1	1	0	R6	Horizontal displayed characters register (high-order)[4]	Char	R/W
0	1	0	1	1	1	R7	Horizontal displayed characters register (low-order)	Char	R/W
0	1	1	0	0	0	R8	CL3 pulse width register	Char	R/W
0	1	1	0	0	1	R9	Fine adjust register[5]	Dot	R/W
0	1	1	0	1	0	R10	PLL frequency-dividing ratio register (high-order)[6]	—	R/W
0	1	1	0	1	1	R11	PLL frequency-dividing ratio register (low-order)[6]	—	R/W
0	1	1	1	0	0	R12	Vertical backporch register (high-order)[2,7]	Line	R/W
0	1	1	1	0	1	R13	Vertical backporch register (low-order)[2,7]	Line	R/W
0	1	1	1	1	0	R14	Horizontal backporch register (high-order)[2,7]	Dot	R/W
0	1	1	1	1	1	R15	Horizontal backporch register (low-order)[2,7]	Dot	R/W

Notes:
1. If you attempt to read data from the register with RS = 0, the bus is driven to high-impedance state and the output data is indefinite.
2. (The specified value − 1) should be written into these registers.
3. Valid only in 8-color display modes with horizontal stripes.
4. The most significant bit is invalid in dual screen configuration modes.
5. Valid only when the display timing signal is supplied externally.
6. Valid only when generating the dot clock.
7. Valid only when generating the display timing signal internally

Register No.	Data Bit				
	3	2	1	0	
—	▨	▨	▨	▨	
AR	Address register				
R0	▨	▨	DSP	DCK	← Control register 1
R1	MC	DON	MS1	MS0	← Control register 2
R2	Vertical displayed				
R3	lines register				
R4					
R5	CL3 period register				
R6	Horizontal displayed				
R7	characters registor				
R8	CL3 pulse width register				
R9	Fine adjust register				
R10	PLL frequency-				
R11	dividing ratio register				
R12	Vertical Backporch				
R13	register				
R14	Horizontal Backporch				
R15	register				

Note: ▨ indicates invalid bits. Attempting to read data from these register bits returns indefinite output data.

Figure 1. Register Bit Assignment

System Configuration

Figure 2 is the block diagram of a system in which the LVIC is used outside of a personal computer.

The LVIC converts the R, G, B serial data sent from the personal computer into parallel data and writes them into the buffer memories once. It reads out the data in turn and outputs them to LCD drivers to drive an LCD. Here the latch clock of the serial data, namely the dot clock (DOTCLK) is generated by a PLL circuit, using HSYNC as a basic clock. The frequency of the dot clock is specified by the PLL frequency-dividing ratio register (R10, R11).

The user may also configure a system without VCO and LPF if supplying the dot clock externally and may configure a system without the MPU if the LVIC is controlled by the pin programming method.

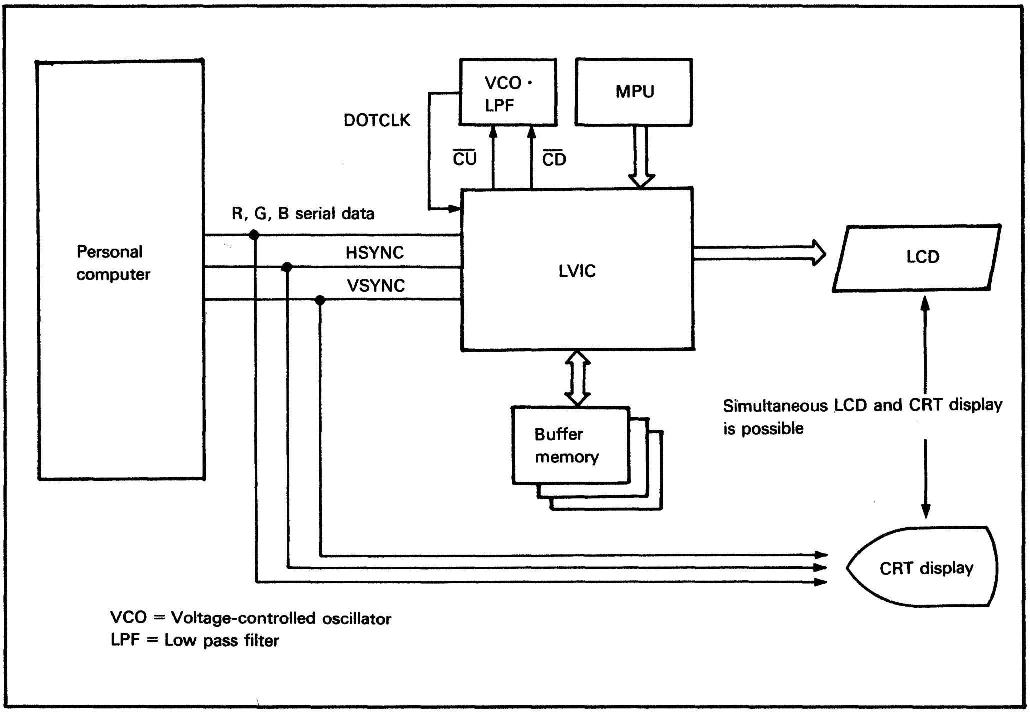


Figure 2. System Block Diagram (MPU Programming Method, Regenerates DOTCLK)

Functional Description

Programming Method

The user may select one of two methods to control the LVIC functions: by pin programming method or by internal registers (internal register programming method). The internal register programming method can be divided into the MPU programming method and the ROM programming method. The MPU writes data into internal registers in the MPU programming method and ROM writes the data in the ROM programming method. Table 6 lists the relation between programming method and pins.

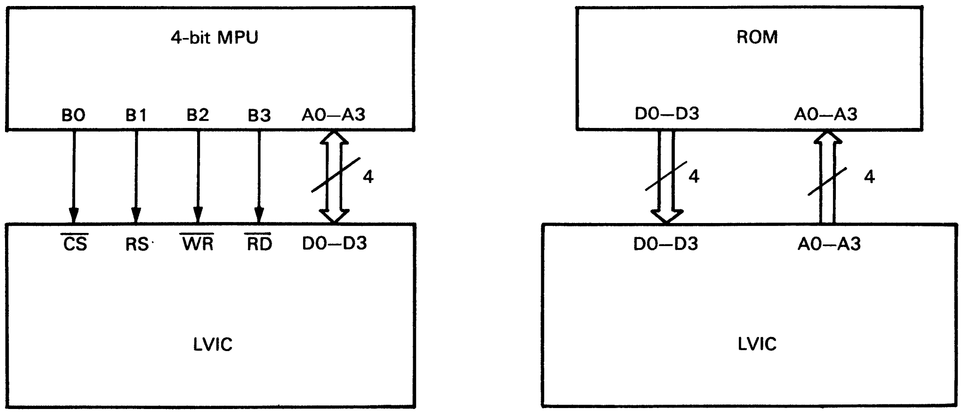
Pin Programming Method: LVIC mode setting pins control functions in the pin programming method.

Internal Register Programming Method: In the internal register programming method, an MPU or ROM writes data into internal registers to control functions. Figure 3 illustrates the connections of MPU or ROM and the LVIC. Figure 3 (1) is an example of using a 4-bit microprocessor, but since the LVIC's MPU bus is compatible with the 4-MHz 80-family controller bus, it can also be connected directly with the bus of host MPU.

Table 6. Programming Method Selection

Pins			
PMOD1	**PMOD0**	**Programming Method**	
0	0	Pin programming	
0	1	Internal register	With MPU
1	0	Programming	With ROM
1	1	Prohibited (Note)	

Note: This combination is for a test mode and disables display.



(1) Connection of MPU and LVIC

(2) Connection of ROM and LVIC

Figure 3. Connection of MPU or ROM and LVIC

Screen Size

Screen size can be programmed either by pins or internal registers.

In the pin programming method, the user may select either 640 dots or 720 dots (80 characters or 90 characters) as the number of horizontal displayed characters with the XDOT pin, and 200, 350, 400, 480, 512, or 540 lines as the number of vertical displayed lines with YL2-YL0 pins. The number of vertical displayed lines can be adjusted with ADJ and F3-F0 pins within +0 to +15 lines.

In the internal register programming method, the user may select any even number from 32 dots to 4048 dots (= 4 characters up to 506 characters) with the horizontal displayed characters register (R6, R7), and any even number from 4 lines up to 1028 lines with the vertical displayed lines register (R2, R3 and the high-order two bits of R4). However, odd number of lines can also be selected when screen configuration is single and a Y-driver (scan driver) is set on one side of an LCD screen.

Figure 4 illustrates the relation between an LCD screen and pins and internal registers controlling screen size.

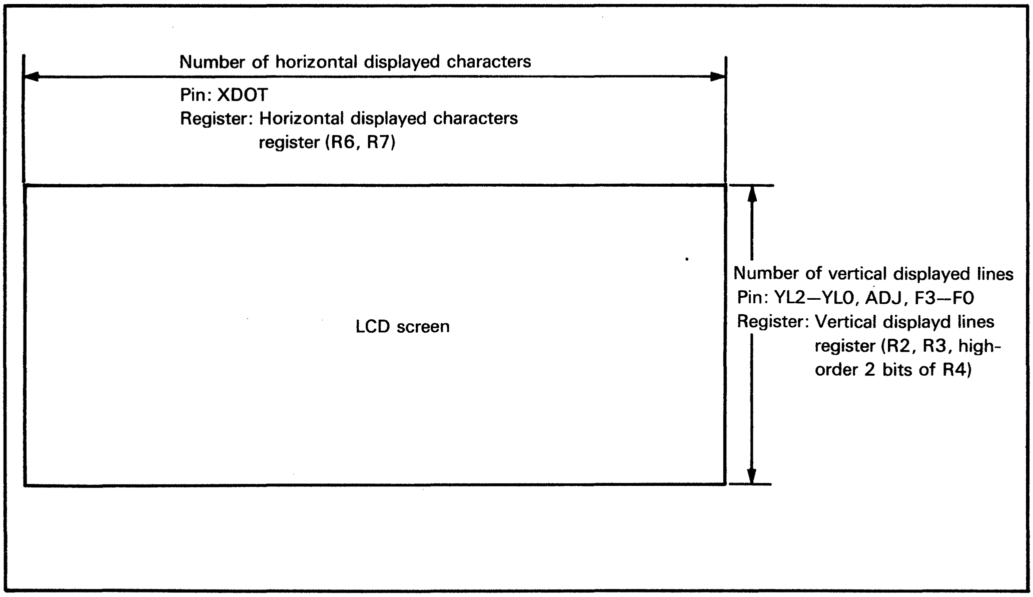

Number of horizontal displayed characters
Pin: XDOT
Register: Horizontal displayed characters register (R6, R7)
LCD screen
Number of vertical displayed lines
Pin: YL2—YL0, ADJ, F3—F0
Register: Vertical displayd lines register (R2, R3, high-order 2 bits of R4)

Figure 4. Relation between LCD Screen and Pins and Internal Registers

Memory Selection

The user may select 8-, 32-, or 64-kbyte SRAMs as buffer memory for the LVIC. Since the LVIC has a chip selector for these memories, no external decoder is required. The user selects the memory with pins MS1 and MS0 or with data bits MS1 and MS0 of the control register 2 (R1). Table 7 lists the kinds of memories and pin address assignments.

Memory capacity required depends on screen size and can be obtained with the following expression:

Memory capacity (bytes) = Nhd × Nvd

Nhd: number of horizontal displayed characters

Nvd: number of vertical displayed lines

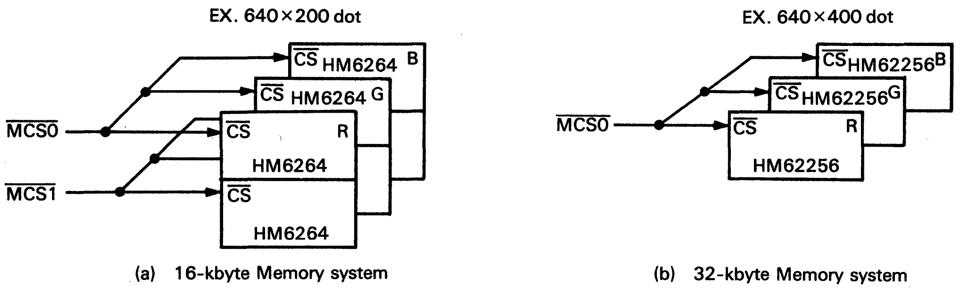
For example, the screen of 640 × 200 dots requires 16-kbyte memory capacity since 80 characters × 200 lines is 16 kbytes. (8 dots compose a character.)
Therefore, each plane needs two HM6264s, which has 8-kbyte memory capacity, in 8-level gray scale display modes. Conncet $\overline{\text{MCS0}}$ with one of the memories of each plane and $\overline{\text{MCS1}}$ with the other (figure 5 (a)).

When the screen size is 640 × 400 dots, 32-kbyte memory capacity is required (figure 5 (b)).
Therefore, each plane needs a HM62256, which has 32-kbyte memory capacity.
Connect $\overline{\text{MCS0}}$ with $\overline{\text{CS}}$ of the memories here.

Table 7. Memories and Pin Address Assignment

Pins or Bits					
MS1	**MS0**	**Memory**	**Address Output Pins**	**Chip Select Pins**	**Address Assignment**
0	0	No memory[1]	—	—	—
0	1	8-kbyte	MA0-MA12	$\overline{\text{MCS0}}$	\$0000-\$1FFF
				$\overline{\text{MCS1}}$	\$2000-\$3FFF
				MA13	\$4000-\$5FFF
				MA14	\$6000-\$7FFF
				MA15	\$8000-\$9FFF
1	0	32-kbyte	MA0-MA14	$\overline{\text{MCS0}}$	\$00000-\$07FFF
				$\overline{\text{MCS1}}$	\$08000-\$0FFFF
				MA15	\$10000-\$17FFF
1	1	64-kbyte	MA0-MA15	$\overline{\text{MCS0}}$	\$00000-\$0FFFF
				$\overline{\text{MCS1}}$	\$10000-\$1FFFF

Note: 1. There are some limitations when the user uses no memory. Refer to "User Precautions."



(a) 16-kbyte Memory system (b) 32-kbyte Memory system

Figure 5. Relation between Display Screen Memories

Display Modes

The LVIC supports 16 display modes, depending on the state of the DM3-DM0 pins. The display mode consists of display color, type of LCD data output, how to set LCD drivers around an LCD screen, how to arrange color data (= type of stripes), and how to output M signal (= type of alternating signal). Table 8 lists display modes.

Table 8. Modes List

Mode	**Pins**				**Display**	**LCD Data Output**		**LCD Driver Setting**			
No.	**DM3**	**DM2**	**DM1**	**DM0**	**Color**	**Data Transfer**	**Screen Config.**	**X-Driver[2]**	**Y-Driver[3]**	**Stripe[4]**	**Alternating**
1	0	0	0	0	Monochrome	4-bit	Dual	One side	One side	—	Per frame
2	0	0	0	1			Single				
3[1]	0	0	1	0					Both sides		
4	0	0	1	1		8-bit			One side		
5[1]	0	1	0	0					Both sides		
6	0	1	0	1	8-level gray scale	4-bit	Dual		One side		
7	0	1	1	0			Single				
8	0	1	1	1		8-bit					
9[1]	1	0	0	0	8-clolor	12-bit (4 bits for R,G,B each)				Vertical	Per line
10[1]	1	0	0	1					Both sides		
11[1]	1	0	1	0				Both sides	One side		
12[1]	1	0	1	1					Both sides		
13[1]	1	1	0	0				One side	One side	Horizontal	
14[1]	1	1	0	1					Both sides		
15[1]	1	1	1	0				Both sides	One side		
16[1]	1	1	1	1					Both sides		

Notes: 1. For TFT-type LCD.
2. Data output driver
3. Scan driver
4. Refer to "Display Color, 8-Color Display."

Display Color

The LVIC converts R, G, B, the color data for CRT display, into the monochrome, 8-level gray scale, or 8-color display data.

Monochrome Display (Mode 1 to Mode 5): In monochrome modes 1-5, the LVIC displays two colors, namely black (= display on) and white (= display off). As shown in table 9, the OR of CRT display R, G, B data determines the display color.

8-Level Gray Scale Display (Mode 6 to Mode 8): In 8-level gray scale modes 6-8, the LVIC thins out data on certain lines to display an 8-level gray scale according to CRT display color (luminosity). Table 10 shows the relation between CRT display color (luminosity) and LCD color (contrast).

8-Color Display (Mode 9 to Mode 16): In 8-color modes 9-16, the LVIC displays 8 colors with red (R), green (G), and blue (B) filters on liquid crystal cells. The eight colors are the same as those provided by CRT display. As illustrated in figure 5, 8-color display has of two stripe modes: horizontal stripe mode and vertical stripe mode. In the former mode, the LVIC arranges R, G, B data horizontally, with horizontal filters. In the latter mode, the LVIC arranges R, G, B data vertically, with vertical filters. Three cells express a dot in both modes.

Table 9. Monochrome Display

CRT Display Data				LCD		
R	G	B	CRT Display Color	On/Off	Color	
1	1	1	White	On	Black	■
1	1	0	Yellow	On	Black	■
0	1	1	Cyan	On	Black	■
0	1	0	Green	On	Black	■
1	0	1	Magenta	On	Black	■
1	0	0	Red	On	Black	■
0	0	1	Blue	On	Black	■
0	0	0	Black	Off	White	□

Table 10. 8-Level Gray Scale Display

CRT Display Data			CRT		LCD		
R	G	B	Color	Luminosity	Color	Contrast	
1	1	1	White	High	Black	Strong	■
1	1	0	Yellow				■
0	1	1	Cyan	↕	↕	↕	■
0	1	0	Green				■
1	0	1	Magenta				▓
1	0	0	Red				▒
0	0	1	Blue				░
0	0	0	Black	Low	White	Weak	□

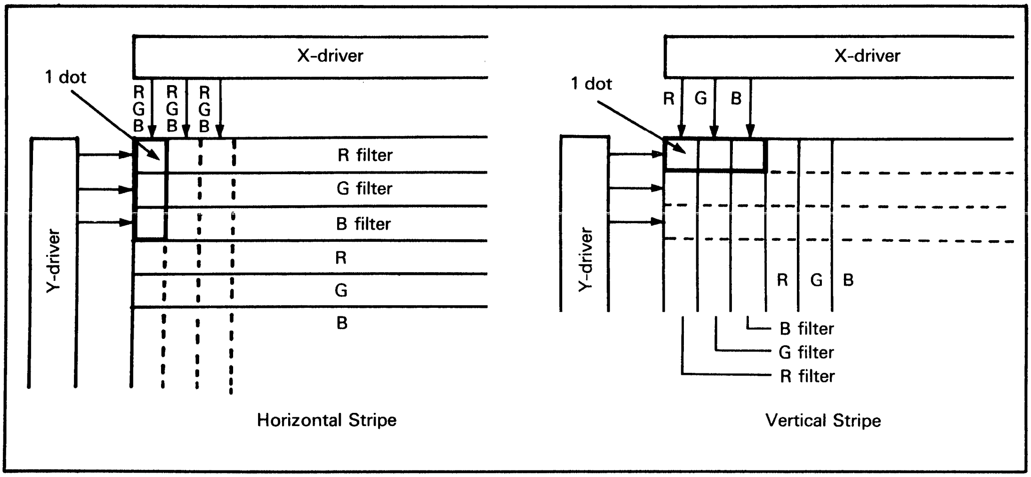


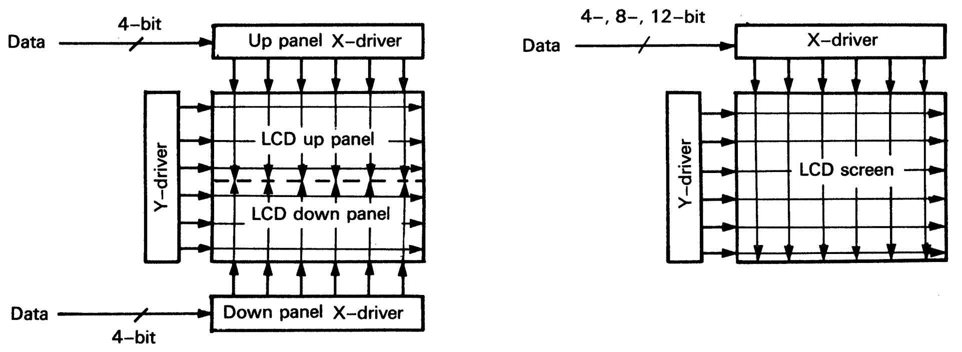
Figure 6. Stripe Modes in 8-Color Display

LCD System Configuration

The LVIC supports the following system configurations for LCD:

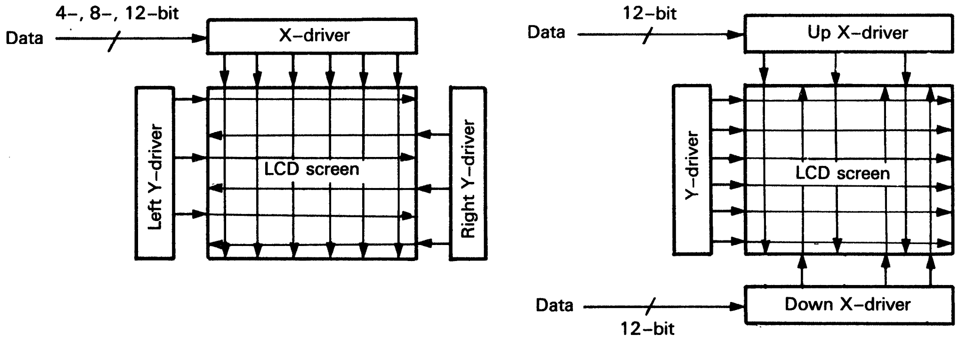
- Types of LCD data output:
  - —Data transfer: 4-bit, 8-bit, or 12-bits (4 bits for R, G, B each)
  - —Screen configuration: Single or dual
- How to set LCD drivers around LCD screen:
  - —X-driver: On one side or on both sides
  - —Y-driver: On one side or on both sides

Figure 7 illustrates these system configurations by mode.



System Configuration for Mode 1 and Mode 6 (4-Bit Data Transfer, Dual Screen, X-Driver and Y-Driver on One Side Each) (Note)

System Configuration for Modes 2, 4, 7, 8, 9, and 13 (4-, 8-, or 12-Bit Data Transfer, Single Screen, X-Driver and Y-Driver on One Side Each)



System Configuration for Modes 3, 5, 10, and 14 (4-, 8-, or 12-Bit Data Transfer, Single Screen, X-Driver on One Side and Y-Driver on Both Sides)

System Configuration for Mode 11 and Mode 15 (12-Bit Data Transfer, Single Screen, X-Driver on Both Sides and Y-Driver on One Side)

Note: Although there are two X-drivers, the X-driver is considered to be set on one side, not on both sides, because the LCD up panel and down panel are each regarded as one screen.

Figure 7. System Configurations by Mode

Calculation of LDOTCK

LDOTCK frequency f_L is calculated from the following expression:

$f_L = (Nhd + 6) \times 8 \times Nvd \times f_F$

Nhd : number of horizontal characters displayed on LCD

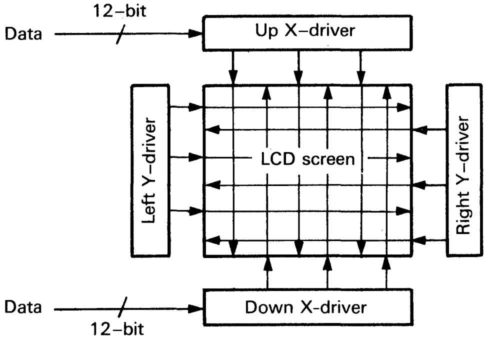
Nvd : number of virtical displayed lines on LCD

f_F : FLM frequency

Here f_L must hold the following relation, where f_D is frequency of dot clock for CRT display (= DOTCLK).

$f_L < f_D \times 15/16$ or

$f_L = f_D$ (The LDOTCK phase must be inverse of the DOTCLK phase in this case)



System Configuration for Mode 12 and Mode 16 (12-Bit Data Transfer, Single Screen, X-Driver and Y-Driver on Both Sides Each)

Notes: 1. X-drivers on both sides: Data output wires run from up and down X-drivers alternately, which widens the interval between wires to twice that in case of an X-driver an one side (figure 8).

2. Y-drivers on both sides: Line select signal output wires run from right and left Y-drivers alternately, which widens the interval between wires to twice that in case of Y-driver on one side (figure 9).

Figure 7. System Configurations by Mode (cont)

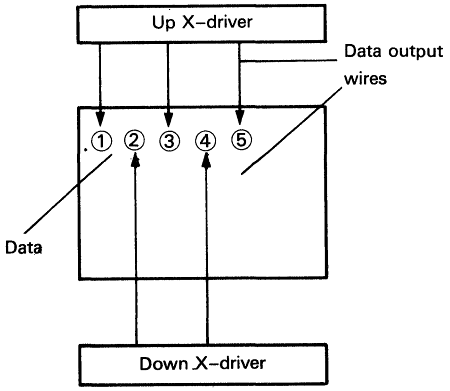


Figure 8. X-Drivers on Both Sides

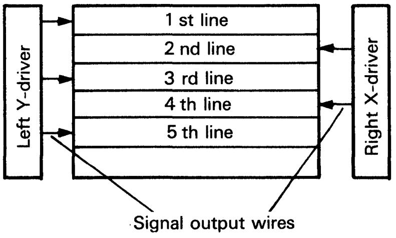


Figure 9. Y-Drivers on Both Sides

Display Timing Signal Generation

CRT display data is classified into display period data and retrace period data. Only display period data is necessary for LCD. Therefore, the LVIC needs a signal announcing whether the CRT display data transferred is for the display period or not. This signal is the display timing signal.

The LVIC can generate the display timing signal from HSYNC and VSYNC. Figure 10 illustrates the relation between HSYNC, VSYNC, the display timing signal (DISPTMG), and display data. Y lines and X dots in the figure are specified by the vertical backporch register (R12, R13) and the horizontal backporch register (R14, R15) respectively.

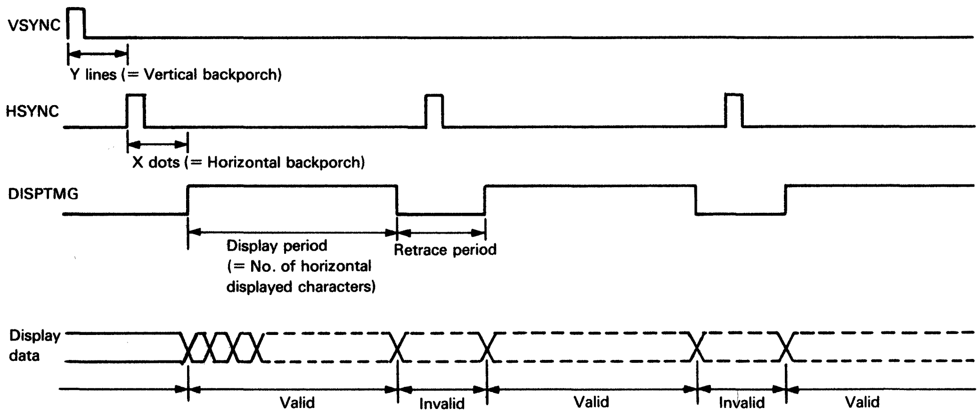


Figure 10. Relation between HSYNC, VSYNC, DISPTMG, and Display Data

Dot Clock Generation

The dot clock, which is a data latch clock, is not a standard video signal and does not appear from the CRT display plug. Thus it is necessary to generate the dot clock. The LVIC has a programmable counter and a phase comparator which are parts of a PLL circuit, and can generate the dot clock from HSYNC if a charge pump, a low pass filter (LPF), and a voltage-controlled oscillator (VCO) are externally attached.

Figure 11 is a block diagram of a PLL circuit. A PLL (phase-locked loop) circuit is a feedback controller regenerating a clock whose frequency and phase are the same as those of a basic clock. The basic clock is HSYNC here.

At power-on,VCO outputs to the programmable counter a signal whose frequency depends on the voltage at the time. The counter divides the frequency of the signal according to the value in the PLL frequency-dividing ratio register (R10, R11) and outputs it to the phase comparator. This is the frequency-divided clock.

The comparator compares the edges of the clock and HSYNC and outputs $\overline{\text{CU}}$ or $\overline{\text{CD}}$ signal to the charge pump and LPF according to the result. The comparator outputs $\overline{\text{CU}}$ when the frequency of the clock is lower than that of HSYNC or when the phase of the clock is behind that of HSYNC, while it outputs $\overline{\text{CD}}$ in the contrary case. The charge pump and LPF apply voltage to the VCO according to $\overline{\text{CU}}$ or $\overline{\text{CD}}$ signal.

This operation is repeated until the phase and the frequency of the frequency-divided clock coincide with those of HSYNC, making it a stable dot clock.

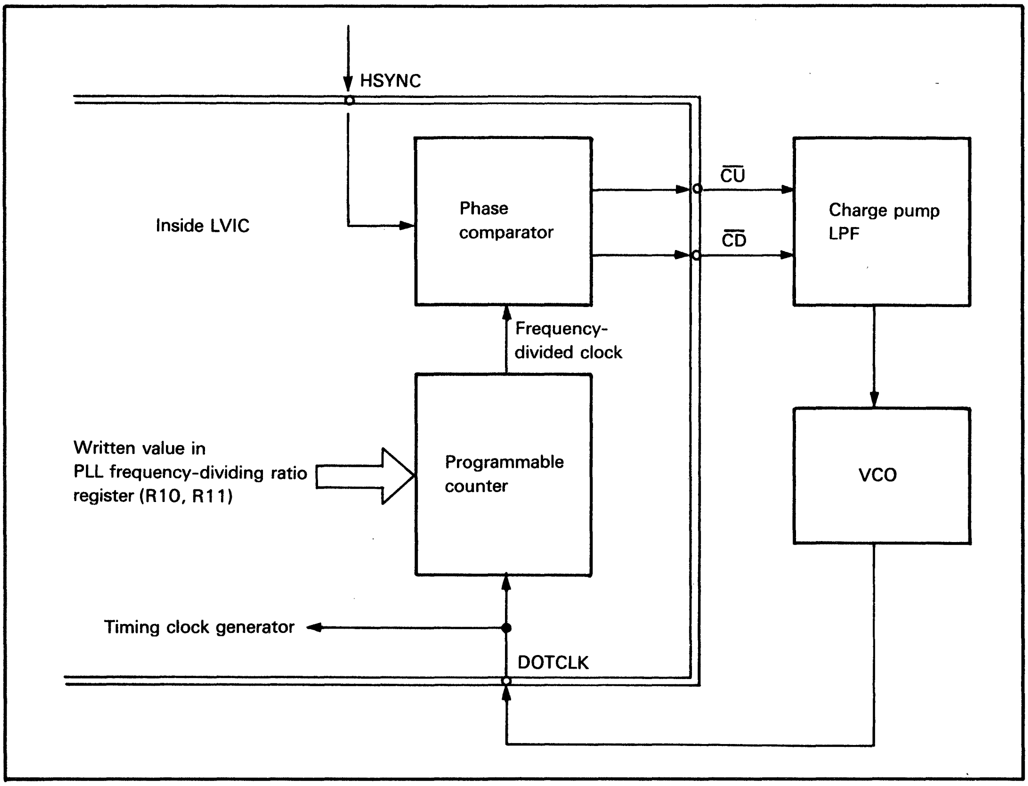


Figure 11. PLL Circuit Block Diagram

Doubled-in-Height Display

Doubled-in-height display doubles characters and pictures in height as illustrated in figure 12.

In TN-type LCD modes (= modes 1, 2, 4, 6, 7, and 8), CL3 frequency is twice as high as CL1 frequency (figure 13). As a result, using CL3 instead of CL1 as a shift clock (figure 14) enables two lines to be selected while an X-driver (data output driver) is outputting the same data, realizing doubled-in height display. However, the following procedures are necessary in this display since multiplexing duty ratio becomes twice as great as the value specified as the number of vertical displayed lines.

1. Halve the frequency of the LCD dot clock (= LDOTCK)
2. Halve the number of vertical displayed lines

This function is provided only for TN-type LCD.

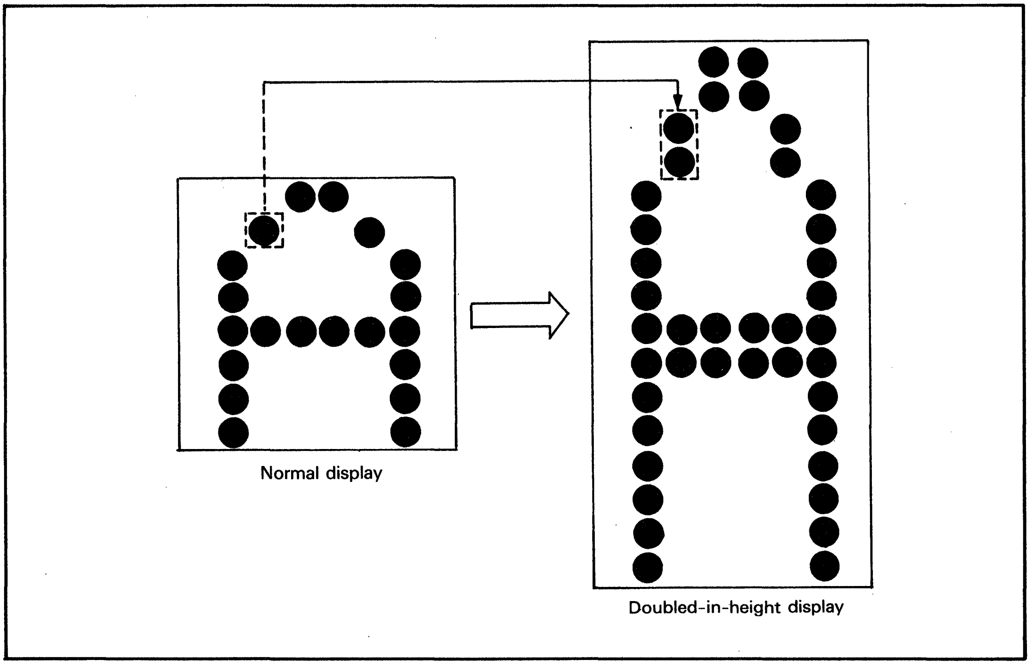


Figure 12. Doubled-in-Height Display Example

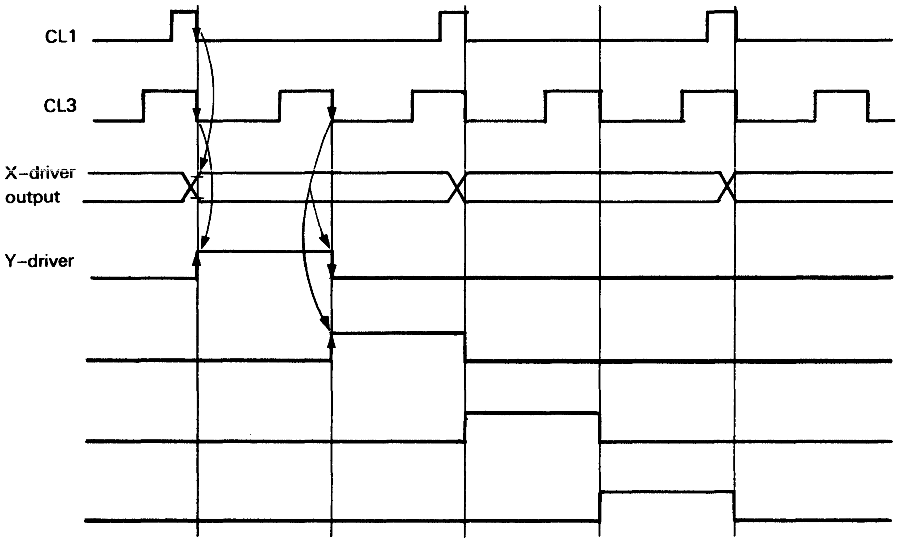


Figure 13. Relation between CL1 and CL3 in Modes 1, 2, 4, 6, 7, and 8

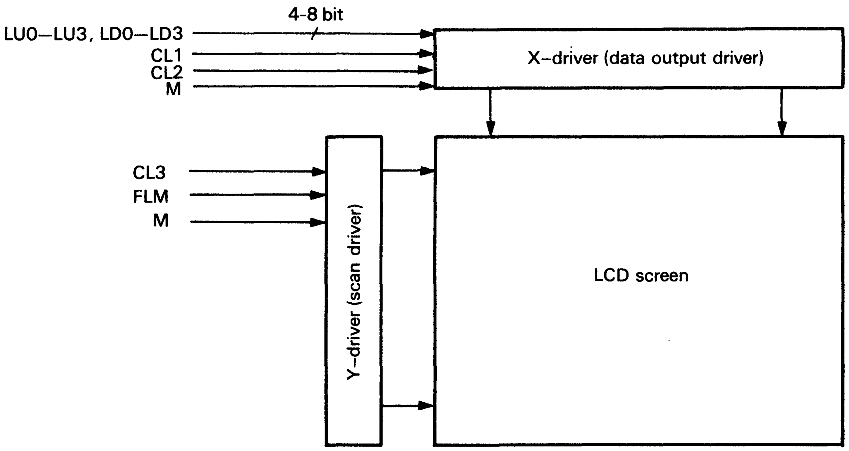


Figure 14. Connection for Doubled-in-Height Display

Display Timing Signal Fine Adjusment

When the display timing signal is supplied externally, a phase shift might appear between CRT data and the display timing signal. This is because each signal has its own peculiar lag. The LVIC can adjust the display timing signal with the F0-F3 pins or the fine adjust register (R9) to correct this phase shift.

Table 11 shows the relation between F3-F0 pins, data bit 3 to data bit 0 of the fine adjust register, and fine adjustment. Concerning the polarity of the number of dots adjusted, − indicates advancing the phase of the display timing signal and + indicates delaying it. F3 pin or data bit 3 of R9 selects the polarity. The adjustment reference point is the display start position.

Figure 15 shows examples of adjusting the display timing signal. Since the signal is two dots ahead of the display start position in case (1), (F3, F2, F1, F0) or (data bits 3, 2, 1, 0 of R9) should be set to (1, 0, 1, 0) to delay the signal for two dots. Since the signal is two dots behind the display start position in case (2), they should be set to (0, 0, 1, 0) to advance the signal for two dots. When there is no need to adjust the signal, settings of either (0, 0, 0, 0) or (1, 0, 0, 0) will do.

Table 11. Pins, Data Bits of R9, and Fine Adjustment

Pin:	**F3**	**F2**	**F1**	**F0**	**Number of Dots**
R9 Bit:	**3**	**2**	**1**	**0**	**Adjusted**
	0	0	0	0	0
		0	0	1	− 1
		⋮	⋮	⋮	⋮
		1	1	0	− 6
		1	1	1	− 7
	1	0	0	0	0
		0	0	1	+ 1
		⋮	⋮	⋮	⋮
		1	1	0	+ 6
		1	1	1	+ 7

Note: When adjusting the display timing signal with pins, set ADJ pin to 1.

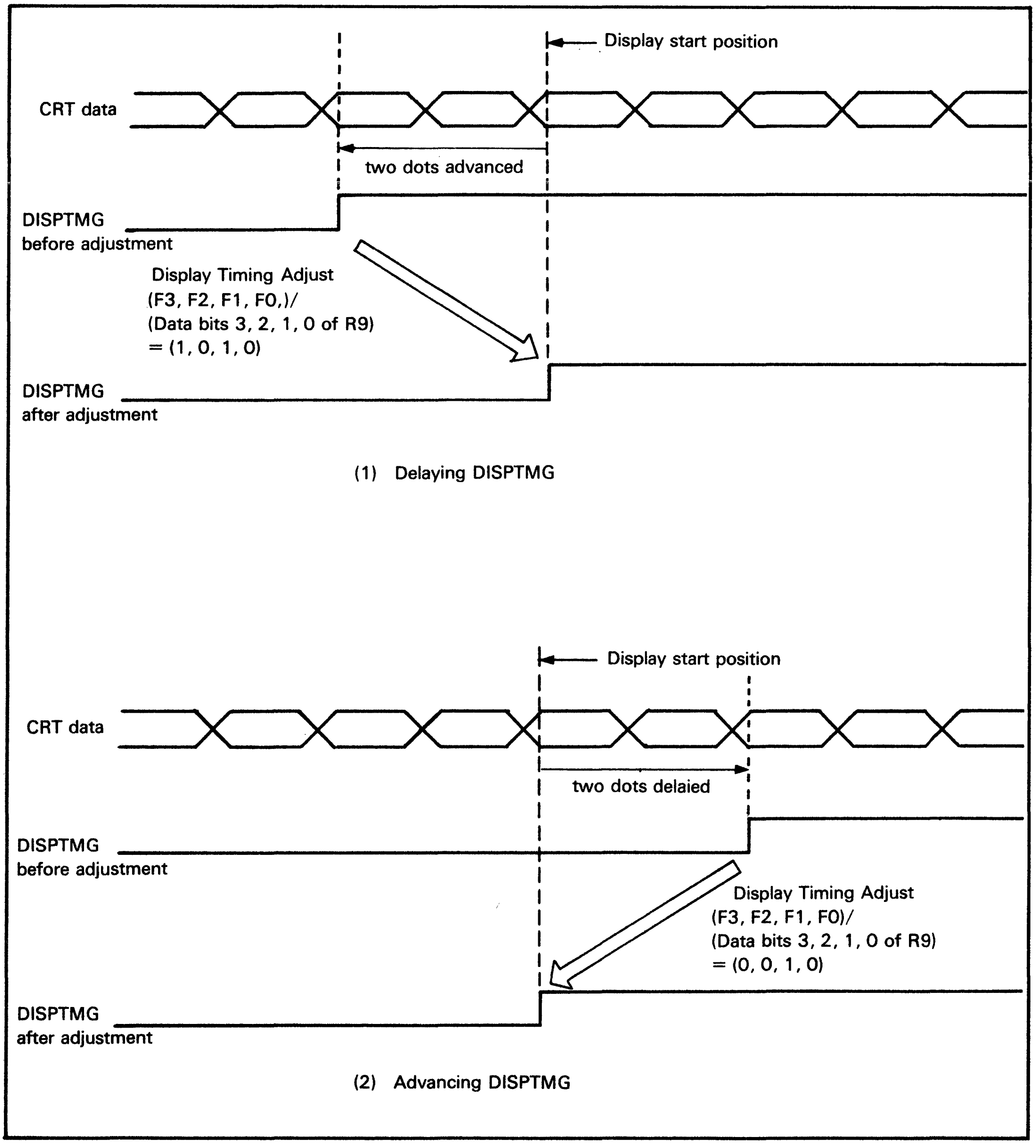


Figure 15. Adjustment of Display Timing Signal

Internal Registers

The LVIC has an address register (AR) and sixteen data registers (R0-R15). In order to specify one of the sixteen data registers, write its register address into the address register. The MPU transfers data to the data register corresponding to the written address.

All the registers are valid only when the LVIC is controlled by the internal register programming method and are invalid (don't care) when by the pin programming method.

Address Register (AR)

The address register (figure 16) is composed of four bits and specifies one data register out of sixteen. This register is selected by the MPU when RS pin is low and specifies any data register with the register address written by the MPU.

Control Register 1 (R0)

Control register 1 (figure 17) is composed of four bits, including two invalid bits. Each of two valid bits has its own function. Reading from and writing into invalid bits are passible. However, these operation does not affect the LSI function.

- DSP Bit
  —DSP = 1: LVIC generates the display timing signal
  —DSP = 0: LVIC does not generate the display timing signal
  (If DCK = 1, the display timing signal is generated in spite that DSP = 0)
- DCK Bit
  —DCK = 1: LVIC generates the dot clock
  —DCK = 0: LVIC does not generate the dot clock

	AR			
Data Bit	3	2	1	0
Value	Register address			

Figure 16. Address Register

	R0			
Data Bit	3	2	1	0
Function	▨	▨	DSP	DCK

Figure 17. Control Register 1

Control Register 2 (R0)

Control register 2 (figure 18) is composed of four bits and has three functions.

- MC Bit
  - —MC = 1: M signal alternates per line
  - —MC = 0: M signal alternates per frame
- DON Bit
  - —DON = 1: Display on
  - —DON = 0: Display off
- MS1 and MS0 Bits
  - —Select the memory type (table 12)

Vertical Displayed Lines Register (R2, R3, High-Order 2 Bits of R4), CL3 Period Register (Low-order 2 Bits of R4, R5)

The vertical displayed lines register (figure 19) is composed of ten bits (R2 + R3 + high-order two bits of R4) and specifies the number of vertical displayed lines. This register can specify both even and odd numbers in modes for a Y-driver on one side and single screen configuration, but even numbers only in the other modes. The value to be written into this register is (Nvd − 1), where Nvd = number of vertical displayed lines.

The CL3 period register is composed of six bits (low-order two bits of R4 + R5) and specifies the period of CL3 in 8-color display modes with horizontal stripes. Thus this register is invalid in the other modes. CL3 is a clock for the LVIC to output R, G, B data separately to LCD drivers. The value to be written into this register is (Nhd + 6) × 1/3 − 1, where Nhd = number of horizontal displayed characters. When (Nhd + 6) is not divisible by 3, the quotient should be rounded up or rounded down.

Table 12. Memory Type and MS1, MS0

MS1	MS0	Memory Type
0	0	No memory
0	1	8-kbyte
1	0	32-kbyte
1	1	64-kbyte

	R1			
Data Bit	3	2	1	0
Function	MC	DON	MS1	MS0

Figure 18. Control Register 2

<table>
<tr><td></td><td colspan="2">R4</td><td colspan="4">R2</td><td colspan="4">R3</td><td colspan="2">R4</td><td colspan="4">R5</td></tr>
<tr><td>Data Bit</td><td>3</td><td>2</td><td>3</td><td>2</td><td>1</td><td>0</td><td>3</td><td>2</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Value</td><td colspan="10">Nvd − 1 (Unit: Lines)</td><td colspan="6">(Nhd + 6) × 1/3 −1
(Unit: Characters)</td></tr>
<tr><td></td><td colspan="10">Vertical Displayed Lines Register</td><td colspan="6">CL3 Period Register</td></tr>
</table>

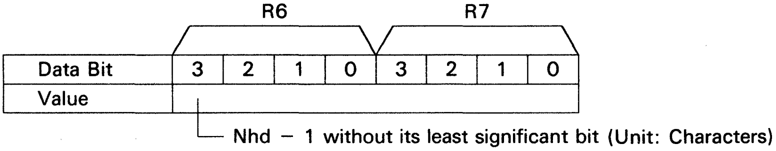
Figure 19. Vertical Displayed Lines Register and CL3 Period Register

Horizontal Displayed Characters Register (R6, R7)

The horizontal displayed characters register (figure 20) is composed of eight bits (R6 + R7) and specifies the number of horizontal displayed characters. This register can specify even numbers only. The most significant bit of R6 is invalid in the modes for dual screen configuration. When writing into this register, shift (Nhd − 1) in the low-order direction for one bit to cut off the least significant bit. Figure 20 shows how to write a value into the register when Nhd = 90.

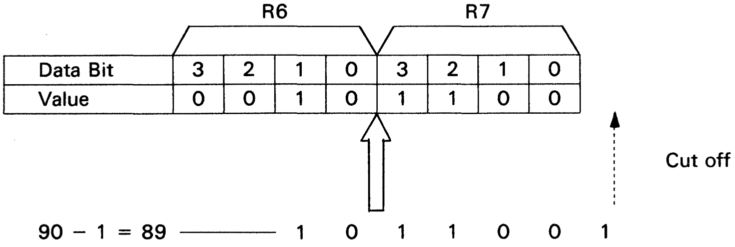
CL3 Pulse Width Register (R8)

The CL3 period register (figure 22) is composed of four bits and specifies the high-level pulse width of CL3. When controlling TFT-type LCDs, each gate of the LCD has to hold data from the time a Y-driver outputs the line select and shift signal to the time an X-driver the outputs next display data. Data must be held while CL3 is high. However, even when the LVIC is not controlling TFT-type LCDs, CL3 appears with the high-level pulse width specified by this register.


R6
R7
Nhd − 1 without its least significant bit (Unit: Characters)

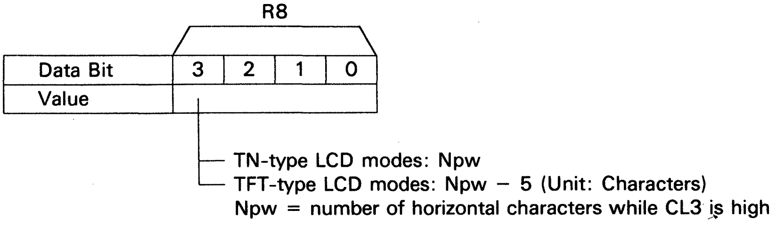
	R6				R7			
Data Bit	3	2	1	0	3	2	1	0
Value								

Figure 20. Horizontal Displayed Characters Register



	R6				R7			
Data Bit	3	2	1	0	3	2	1	0
Value	0	0	1	0	1	1	0	0

Figure 21. How to Write The Number of Horizontal Displayed Characters


R8
TN-type LCD modes: Npw
TFT-type LCD modes: Npw − 5 (Unit: Characters)
Npw = number of horizontal characters while CL3 is high

	R8			
Data Bit	3	2	1	0
Value				

Figure 22. CL3 Pulse Width Register

Fine Adjust Register (R9)

The fine adjust register (figure 23) is composed of four bits and adjusts the externally supplied display timing signal to synchronize its phase with that of LCD data. The value to be written into this register is determined by the interval between the positive edge of the display timing signal and the display start position. For more details, refer to "Display Timing Signal Fine Adjustment." This register is invalid when the display timing signal is generated internally.

PLL Frequency-Dividing Ratio Register (R10, R11)

The PLL frequency-dividing ratio register (figure 24) is composed of eight bits (R10 + R11) and specifies the PLL frequency-dividing ratio for generating a dot clock by a PLL circuit. The value to be written into this register is determined by the ratio of the frequency of HSYNC to that of the dot clock which the user wants. This register is invalid when the dot clock is supplied externally and is valid only when the LVIC is controlled by the internal register programming method and the DCK bit of control register 1 (R0) is 1. The written value in this register (N_{PLL}) is obtained with the following expression:

$N_{PLL} = Ncht \times 8 - 731$

Ncht: total number of characters for CRT

Ncht can be obtained as follows from the specifications of a CRT monitor:

Ncht = 1/8 × (DOTCLK frequency)/(HSYNC frequency)

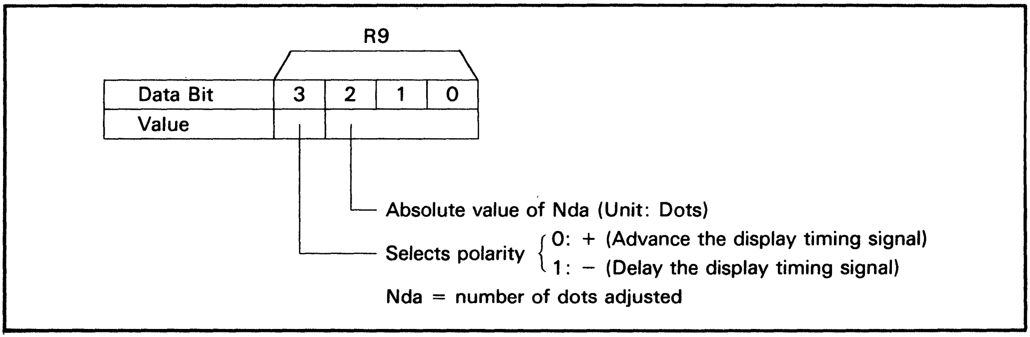
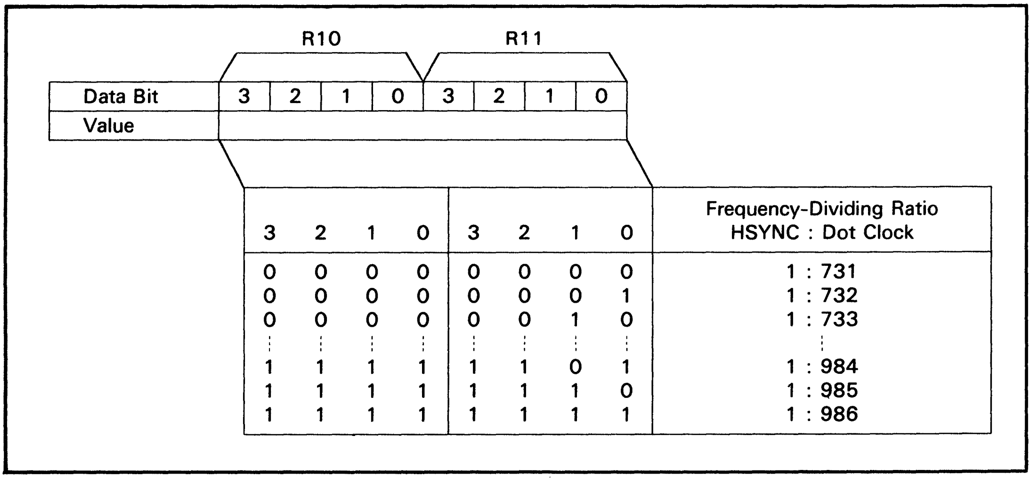

R9
Data Bit
3
2
1
0
Value
Absolute value of Nda (Unit: Dots)
Selects polarity
0: + (Advance the display timing signal)
1: − (Delay the display timing signal)
Nda = number of dots adjusted

Figure 23. Fine Adjust Register



3	2	1	0	3	2	1	0	Frequency-Dividing Ratio HSYNC : Dot Clock
0	0	0	0	0	0	0	0	1 : 731
0	0	0	0	0	0	0	1	1 : 732
0	0	0	0	0	0	1	0	1 : 733
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	0	1	1 : 984
1	1	1	1	1	1	1	0	1 : 985
1	1	1	1	1	1	1	1	1 : 986

Figure 24. PLL Frequency-Dividing Ratio Register

Vertical Backporch Register (R12, R13)

The vertical backporch register (figure 25) is composed of eight bits (R12 + R13) and specifies the vertical backporch. The vertical backporch is the number of lines between the positive edge of VSYNC and that of the display timing signal (DISPTMG). For more details, refer to "Display Timing Signal Generation." This register is invalid when the display timing signal is supplied externally and is valid only is a system which controls the LVIC by the internal register programming method and where the DSP bit of control register 1 (R0) is 1. (If the DCK bit of control register 1 (R0) is 1, DISPTMG will always be regenerated and the register is enabled even when DSP = 0.)

Horizontal Backporch Register (R14, R15)

The horizontal backporch register (figure 26) is composed of eight bits (R14 + R15) and specifies the horizontal backporch. The horizontal backporch is the number of characters between the posive edge of HSYNC and that of the display timing signal (DISPTMG). For more details, refer to "Display Timing Signal Generation". This register is invalid when the display timing signal is supplied externally and is valid only in a system which controls the LVIC by the internal register programming method and where the DSP bit of control register 1 (R0) is 1. (If the DCK bit of control register 1 (R0) is 1, DISPTMG will always be generated and this register is enabled even when DSP = 0.)

	R12				R13			
Data Bit	3	2	1	0	3	2	1	0
Value								

Ncvbp − 1 (Unit: Lines)
Ncvbp = number of lines between the positive edge of VSYNC and that of DISPTMG

Figure 25. Vertical Backporch Register

	R14				R15			
Data Bit	3	2	1	0	3	2	1	0
Value								

Nchbp × 8 − 1 (Unit: Dots)
Nchbp = number of characters between the positive edge of HSYNC and that of DISPTMG

Figure 26. Horizontal Backporch Register

Reset

$\overline{\mathrm{RES}}$ pin resets and starts the LVIC. Make sure to hold the reset signal low for at least 1 μs after power-on.

Reset is defined as shown in figure 27.

State of Pins During Reset

$\overline{\mathrm{RES}}$ basically does not control output pins and operates regardless of the other input pins. Output pins can be classified into the following five groups depending on their reset state.

1. Keeps state before reset: CL2
2. Driven to high-impedance state (fixed low when using no memory): RD0-RD7, GD0-GD7, BD0-BD7
3. Fixed high: $\overline{\mathrm{MWE}}$, CL4, M, $\overline{\mathrm{CD}}$, $\overline{\mathrm{MCS1}}$
4. Fixed low: MA0-MA12, R0-R3, G0-G3, B0-B3, $\overline{\mathrm{CS}}$, CL1, CL3, FLM, A0-A3, $\overline{\mathrm{CU}}$
5. Fixed high or low depending on the memory in use (table 13): MA13-MA15, $\overline{\mathrm{MCS0}}$

State of Registers During Reset

$\overline{\mathrm{RES}}$ pin does not affect register contents. Therefore, registers can be both read and written by the MPU even during reset. Registers keep the contents they had before reset until they are rewritten.

Memory Clear Function

After reset, the LVIC writes 0 in the memory area specified by MSEL0 and MSEL1 (table 7) regardless of R, G, B data.

Table 13. Memory Type and State of Pins During Reset

Kind of Memories	MA13	MA14	MA15	$\overline{\mathrm{MCS0}}$
No memory	Low	Low	High	High
8-kbyte memory	High	High	High	Low
32-kbyte memory	Low	Low	High	Low
64-kbyte memory	Low	Low	Low	Low

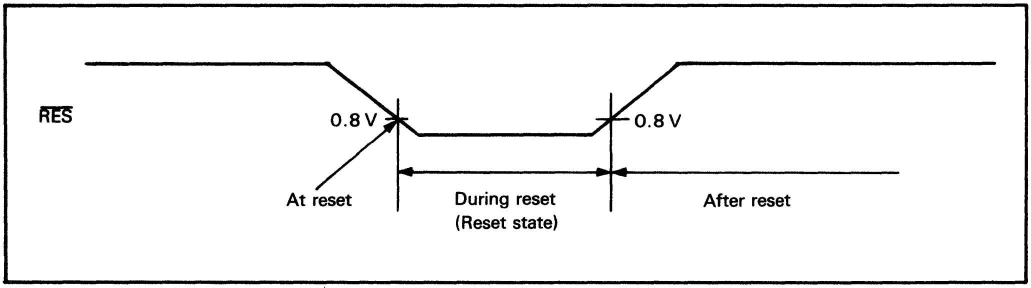


Figure 27. Reset Definition

User Precautions

1. There are following limitations when the user uses no memory. (MSEL0 = 0, MSEL1 = 1)
    - The display modes for dual screen configuration (= mode 1 and mode 6) are disabled.
    - The LVIC cannot support the LCD systems with Y-drivers on both sides. Even if the user selects the mode for the system with Y-drivers on both sides (= mode 3, 5, 10, 12, 14, or 16), the operation of the LVIC is exactly the same as that in the mode for the system with Y-driver on one side (= mode 2, 4, 9, 11, 13, or 15).
      And leave CL4 terminal disconnected in this usage.
2. The LVIC might operate irregularly until the internal registers have been written after reset in the system which controls the LVIC by internal register programming method.
3. Memory clear function might not work normally at power-on or after reset if MSEL0 and MSEL1 are not properly set to the value corresponding to the memories in use.
4. Since the LVIC is a CMOS LSI, input pins must not be left disconnected. Refer to table 1 concerning how to deal with each pin.

Programming

The values written in internal registers have the limit listed in table 14. The symbols in the table are difined as shown in table 15 and figure 27.

Table 14. Limit on Values Written in Registers

Function	Limit	Notes	Applicable Registers
Screen Configuration	$4 \leqq Nvd \leqq (Ncvbp + Ncvsp) - 1 \leqq 1024$	1,8	R2, R3, R4, R6, R7
	$4 \leqq Nhd \leqq (Nchbp \times 1/n + Nchsp) - 1 \leqq 506$		
	$(Nhd + 6) \times n \times Nvd \times f_F \leqq f_D \leqq 30$ MHz	2,8	R2, R3, R4, R6, R7
CL3 Control	$1 \leqq Npw \leqq (Nhd + 6) \times 1/2 - 1$	3	R4, R5, R6, R7, R8
	$1 \leqq Npw \leqq Nhd$	4	
	$1 \leqq Npw \leqq Npc - 1$	5	
DISPTMG Regeneration	$1 \leqq Nchbp \leqq 256$	6	R12, R13, R14, R15
	$1 \leqq Ncvbp \leqq 256$	6	
Without Buffer Memory	$4 \leqq Nhd \leqq Nchsp - 4$	7	R2, R3, R4, R6, R7
	$4 \leqq Nvd \leqq Ncvsp - 4$	7	

Notes:
1. $Nhd \leqq 256$ in dual screen configuration (= mode 1 and mode 6).
2. f_F: FLM frequency, f_D: frequency of CRT dot clock, f_L: frequency of LCD dot clock for LCD $f_L < f_D \times 15/16$, or $f_L = f_D$
3. In modes 1, 2, 4, 6, 7, and 8
4. In modes 3, 5, 9, 10, 11, and 12 (Npw = (value in R8) + 5)
5. In modes 13, 14, 15, and 16 (Npw = (value in R8) + 5)
6. Value in R14, R15 $\leqq (Nchsp \times n + Nchbp) - Nhd \times n - 2$
   Value in R12, R13 $\leqq (Ncvsp + Ncvbp) - Nvd - 2$
7. $Nht = Nchsp + Nchbp \times 1/n$, $Nd = Ncvbp + Ncvsp$
   ($Nht = Nhd + 6$, $Nd = Nvd$ when using buffer memory)
8. n: Horizontal character pitch (the number of horizontal dots in one character).

Table 15. Symbol Definition

Symbol	Definition
Nchd	Number of horizontal displayed characters on CRT display
Nchsp	Number of characters between the positive edge of DISPTMG and that of HSYNC (= Horizontal sync position)
Nchbp	Number of dots between the positive edge of HSYNC and that of DISPTMG (= horizontal backporch)
Ncvbp	Number of lines between the negative edge (positive edge when VSYNC is high in active state) of VSYNC and the first positive edge of DISPTMG (= vertical backporch)
Ncvsp	Number of lines between the first positive edge of DISPTMG and the next negative edge of VSYNC (= vertical sync position)
Ncvd	Number of vertical displayed lines on CRT display
Nhd	Number of horizontal displayed characters (on LCD)
Npc	Number of characters during CL3 period (= CL3 pulse cycle)
Npw	Number of characters while CL3 is high (= CL3 pulse width)
Nht	Total number of horizontal characters
Nvd	Number of vertical displayed lines (on LCD)

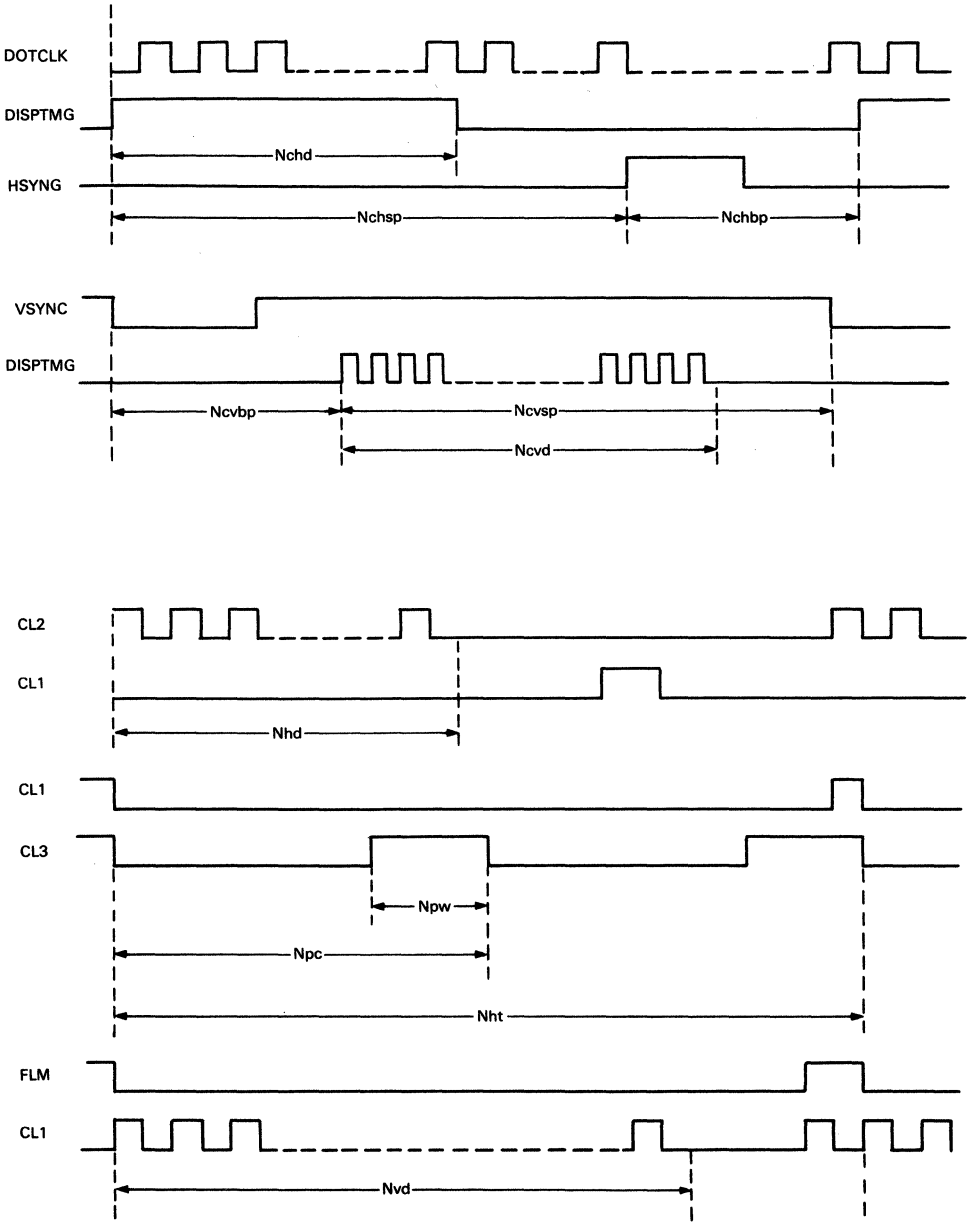


Figure 28. Symbol Definition

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	− 0.3 to + 7.0	V
Input voltage	V_{in}	− 0.3 to V_{CC} + 0.3	V
Operating temperature	T_{opr}	− 20 to + 75	°C
Storage temperature	T_{stg}	− 55 to + 125	°C

Notes: 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 5.0 V ± 10 %, GND = 0 V, Ta = −20°C to +75°C). If these conditions are exceeded, it could affect reliability of the LSI.

2. All voltages are referenced to GND = 0 V.

Electrical Characteristics

DC Characteristics 1 (V_{CC} = 5.0 V ± 10 %, GND = 0 V, Ta = − 20°C to + 75°C, unless otherwise noted)

Item		Symbol	Min	Max	Unit	Test Conditions
Input high voltage	$\overline{\text{RES}}$	V_{IH}	V_{CC} − 0.5	V_{CC} + 0.3	V	
	TTL interface[1]		2.0	V_{CC} + 0.3		
	TTL interface[4]		2.2	V_{CC} + 0.3		
	CMOS interface[1]		0.7 V_{CC}	V_{CC} + 0.3		
Input low voltage	TTL interface[1]	V_{IL}	−0.3	0.8	V	
	TTL interface[5]		−0.3	0.6		
	CMOS interface[1]		−0.3	0.3 V_{CC}		
Output high voltage	TTL interface[2]	V_{OH}	2.4	—	V	I_{OH} = −200 μA
	CMOS interface[2]		V_{CC} − 0.8	—		I_{OH} = −200 μA
Output low voltage	TTL interface[2]	V_{OL}	—	0.4	V	I_{OL} = 1.6 mA
	CMOS interface[2]		—	0.8		I_{OL} = 200 μA
Input leakage current	All inputs except I/O common pins[3]	I_{IL}	−2.5	2.5	μA	
Three state (off-state) leakage current	I/O common pins[3]	I_{TSL}	−10.0	10.0	μA	
Current consumption	—	I_{CC}	—	250	mA	f_{DOTCLK} = 30 MHz Output pins left disconnected

Notes: 1. TTL interface inputs: R, G, B, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, DISPTMG, RD0-RD7, GD0-GD7, BD0-BD7, D0-D3, A0/$\overline{\text{RD}}$/XDOT, $\overline{\text{RS}}$/ADJ, $\overline{\text{CS}}$/MS0
CMOS interface inputs: DM0-DM3, DOTE, PMOD0, PMOD1, A1/YL0-A2/YL2

2. TTL interface outputs: A0/$\overline{\text{RD}}$/XDOT, A1/YL0-A3/YL2, D0-D3, RD0-RD7, GD0-GD7, BD0-BD7, MA0-MA15, $\overline{\text{MCS0}}$, $\overline{\text{MCS1}}$, $\overline{\text{MWE}}$
CMOS interface outputs: $\overline{\text{CU}}$, $\overline{\text{CD}}$, R0/LU0-R3/LU3, G0/LD0-G3/LD3, B0-B3, M, FLM, CL1, CL2, CL3, CL4

3. I/O common pins: A0/$\overline{\text{RD}}$/XDOT, A1/YL0-A3/YL2, D0-D3, RD0-RD7, GD0-GD7, BD0-BD7
Inputs except I/O common pins: HSYNC, VSYNC, PMOD0, PMOD1, RS/ADJ, $\overline{\text{CS}}$/MS0, $\overline{\text{WR}}$/MS1, $\overline{\text{RES}}$, DOTE, DM0-DM3, LDOTCK, DOTCLK, R, G, B, DISPTMG

4. TTL interface: $\overline{\text{WR}}$/MS1, LDOTCK, DOTCLK

5. TTL interface: $\overline{\text{WR}}$/MS1

DC Characteristics 2 (V_{CC} = 5.0 V ± 5 %, GND = 0 V, Ta = − 20°C to + 75°C, unless otherwise noted)

Item		**Symbol**	**Min**	**Max**	**Unit**	**Test Conditions**
Input high voltage	$\overline{\text{RES}}$	V_{IH}	$V_{CC} - 0.5$	$V_{CC} + 0.3$	V	
	TTL interface[1]		2.0	$V_{CC} + 0.3$		
	CMOS interface[1]		0.7 V_{CC}	$V_{CC} + 0.3$		
Input low voltage	TTL interface[1]	V_{IL}	−0.3	0.8	V	
	CMOS interface[1]		−0.3	0.3 V_{CC}		
Output high voltage	TTL interface[2]	V_{OH}	2.4	—	V	I_{OH} = −200 μA
	CMOS interface[2]		$V_{CC} - 0.8$	—		I_{OH} = −200 μA
Output low voltage	TTL interface[2]	V_{OL}	—	0.4	V	I_{OL} = 1.6 mA
	CMOS interface[2]		—	0.8		I_{OL} = 200 μA
Input leakage current	All inputs except I/O common pins[3]	I_{IL}	−2.5	2.5	μA	
Three state (off-state) leakage current	I/O common pins[3]	I_{TSL}	−10.0	10.0	μA	
Current consumption	—	I_{CC}	—	250	mA	f_{DOTCLK} = 30 MHz Output pins left disconnected

Notes:
1. TTL interface inputs: R, G, B, HSYNC, VSYNC, DISPTMG, DOTCLK, LDOTCK, RD0-RD7, GD0-GD7, BD0-BD7, D0-D3, A0/$\overline{\text{RD}}$/XDOT, $\overline{\text{RS}}$/ADJ, $\overline{\text{CS}}$/MS0, $\overline{\text{WR}}$/MS1
   CMOS interface inputs: DM0-DM3, DOTE, PMOD0, PMOD1, A1/YL0-A2/YL2
2. TTL interface outputs: A0/$\overline{\text{RD}}$/XDOT, A1/YL0-A3/YL2, D0-D3, RD0-RD7, GD0-GD7, BD0-BD7, MA0-MA15, $\overline{\text{MCS0}}$, $\overline{\text{MCS1}}$, $\overline{\text{MWE}}$
   CMOS interface outputs: $\overline{\text{CU}}$, $\overline{\text{CD}}$, R0/LU0-R3/LU3, G0/LD0-G3/LD3, B0-B3, M, FLM, CL1, CL2, CL3, CL4
3. I/O common pins: A0/$\overline{\text{RD}}$/XDOT, A1/YL0-A3/YL2, D0-D3, RD0-RD7, GD0-GD7, BD0-BD7
   Inputs except I/O common pins: HSYNC, VSYNC, PMOD0, PMOD1, RS/ADJ, $\overline{\text{CS}}$/MS0, $\overline{\text{WR}}$/MS1, $\overline{\text{RES}}$, DOTE, DM0-DM3, LDOTCK, DOTCLK, R, G, B, DISPTMG

AC Characteristics (V_{CC} = 5.0 V ±10 %, GND = 0 V, Ta = −20 °C to +75 °C, unless otherwise noted)

Video Signal Interface (1) (HD66840F30: 30 MHz) (V_{CC} = 5.0 V ± 5 %)

Item	Symbol	Min	Max	Unit	Remark
DOTCLK cycle time	t_{CYCD}	33	1000	ns	
DOTCLK high-level pulse width	t_{WDH}	16.5	—	ns	
DOTCLK low-level pulse width	t_{WDL}	16.5	—	ns	
DOTCLK rise time	t_{Dr1}	—	5	ns	
DOTCLK fall time	t_{Df1}	—	5	ns	
R, G, B, setup time	t_{VDS}	10	—	ns	
R, G, B, hold time	t_{VDH}	10	—	ns	
DISPTMG setup time	t_{DTS}	10	—	ns	
DISPTMG hold time	t_{DTH}	10	—	ns	
HSYNC setup time	t_{HSS}	10	—	ns	
HSYNC hold time	t_{HSH}	10	—	ns	
Phase shift setup time	t_{PDS}	2 t_{CYCD}	—	ns	
Phase shift hold time	t_{PDH}	2 t_{CYCD}	—	ns	
Input signal rise time	t_{Dr2}	—	10	ns	Except DOTCLK
Input signal fall time	t_{Df2}	—	10	ns	Except DOTCLK

Video Signal Interface (2) (HD66840F25 : 25MHz)

Item	**Symbol**	**Min**	**Max**	**Unit**	**Remark**
DOTCLK cycle time	t_{CYCD}	40	1000	ns	
DOTCLK high-level pulse width	t_{WDH}	20	—	ns	
DOTCLK low-level pulse width	t_{WDL}	20	—	ns	
DOTCLK rise time	t_{Dr1}	—	5	ns	
DOTCLK fall time	t_{Df1}	—	5	ns	
R, G, B, setup time	t_{VDS}	10	—	ns	
R, G, B, hold time	t_{VDH}	10	—	ns	
DISPTMG setup time	t_{DTS}	10	—	ns	
DISPTMG hold time	t_{DTH}	10	—	ns	
HSYNC setup time	t_{HSS}	10	—	ns	
HSYNC hold time	t_{HSH}	10	—	ns	
Phase shift setup time	t_{PDS}	2 t_{CYCD}	—	ns	
Phase shift hold time	t_{PDH}	2 t_{CYCD}	—	ns	
Input signal rise time	t_{Dr2}	—	10	ns	Except DOTCLK
Input signal fall time	t_{Df2}	—	10	ns	Except DOTCLK

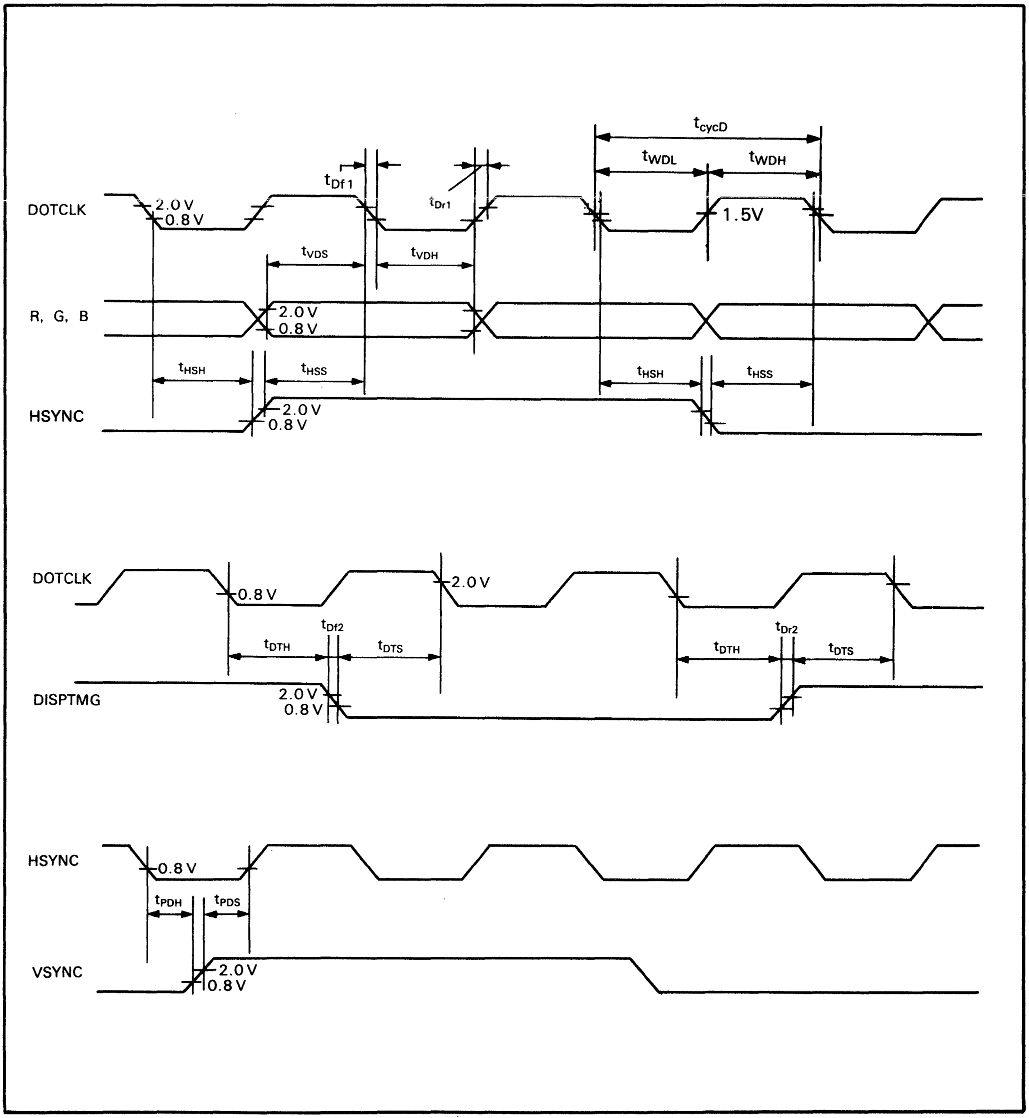


Figure 29. Video Signal Interface

Buffer Memory Interface

Item	Symbol	Min	Max	Unit
Read cycle time	t_{RC}	5 t_{CYCD} − 50	—	ns
RD0-RD7, GD0-GD7, BD0-BD7 data setup time	t_{SMD}	25	—	ns
RD0-RD7, GD0-GD7, BD0-BD7 data hold time	t_{HMD}	0	—	ns
Write cycle time	t_{WC}	6 t_{CYCD} − 50	—	ns
Address setup time	t_{AS}	t_{CYCD} − 30	—	ns
Address hold time	t_{WR}	t_{CYCD} − 30	—	ns
Chip select time	t_{CW}	4 t_{CYCD} − 40	—	ns
Write pulse width	t_{WP}	4 t_{CYCD} − 40	—	ns
RD0-RD7, GD0-GD7, BD0-BD7 output setup time	T_{SMDW}	2 t_{CYCD} − 25	—	ns
RD0-RD7, GD0-GD7, BD0-BD7 output hold time	t_{HMDW}	0	—	ns

Note: t_{CYCD} indicates DOTCLK cycle time (min 33 ns, max 1000 ns).

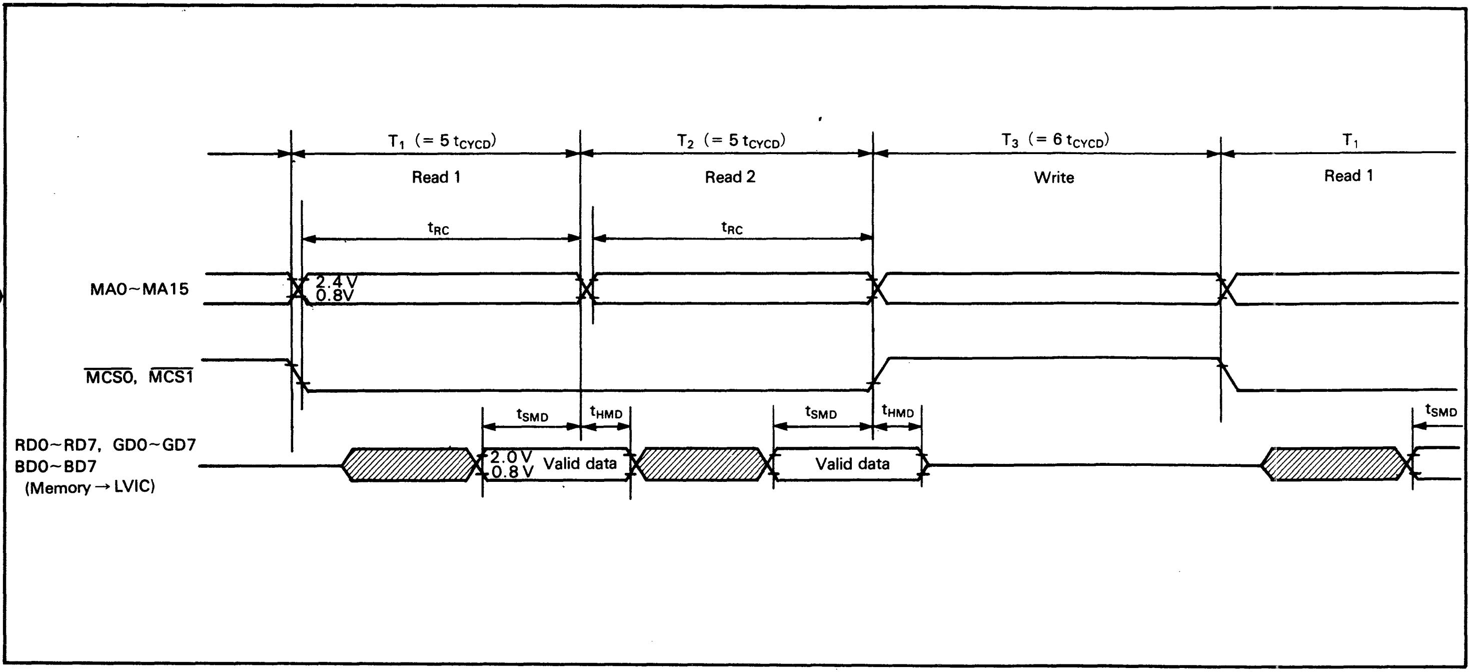


Figure 30. Buffer Memory Interface (RAM Read Timing)

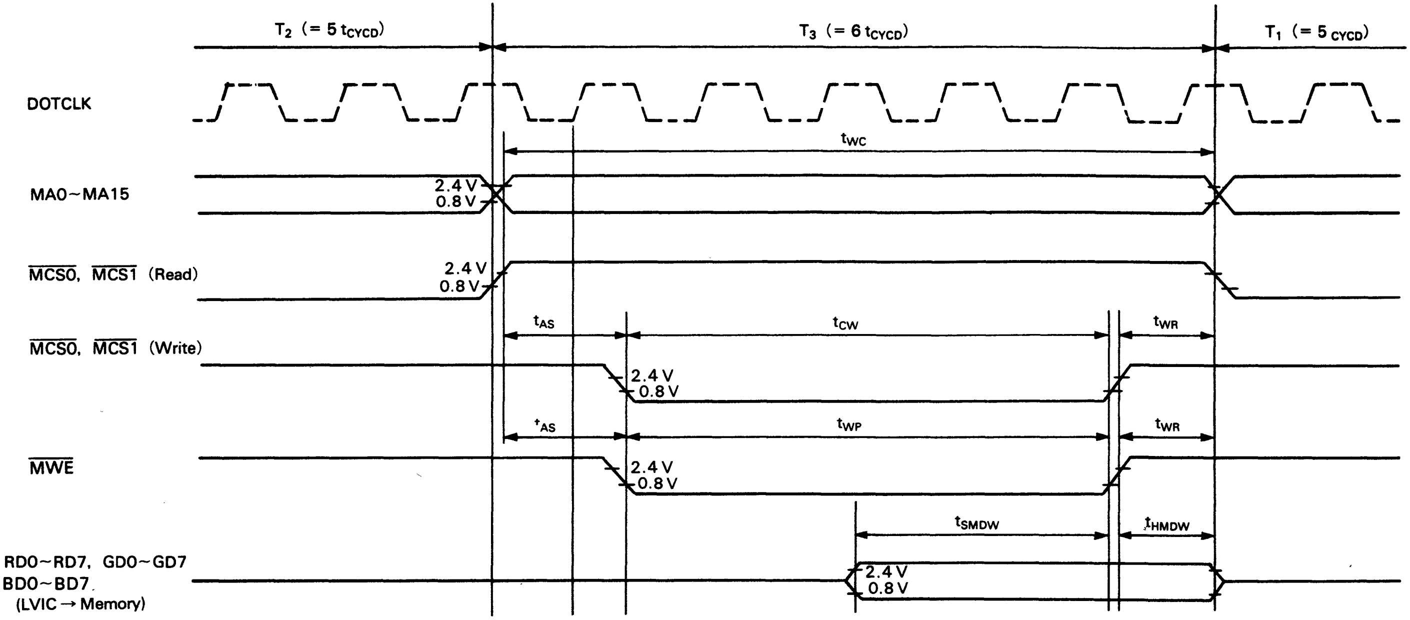


Figure 31. Buffer Memory Interface (RAM Write Timing)

LCD Driver Interface (TN-Type LCD Driver)

Item	Symbol	Min	Max	Unit
CL2 cycle time	t_{WCL2}	166	—	ns
CL2 high-level pulse width	t_{WCL2H}	50	—	ns
CL2 low-level pulse width	t_{WCL2L}	50	—	ns
CL2 rise time	t_{CL2r}	—	30	ns
CL2 fall time	t_{CL2f}	—	30	ns
CL1 high-level pulse width	t_{WCL1H}	200	—	ns
CL1 rise time	t_{CL1r}	—	30	ns
CL1 fall time	t_{CL1f}	—	30	ns
CL1 setup time	t_{SCL1}	500	—	ns
CL1 hold time	t_{HCL1}	200	—	ns
FLM hold time	t_{HF}	200	—	ns
M output delay time	t_{DM}	—	300	ns
Data delay time	t_{DD}	− 20	20	ns
LDOTCK cycle time	t_{WLDOT}	41	—	ns

Note: All the values are measureed at f_{CL2} = 6 MHz.

LCD Driver Interface (TFT-Type LCD Driver)

Item	Symbol	Min	Max	Unit	Remark
CL2 cycle time (X drivers on one side)	t_{TCL2S}	133		ns	Figure 34,35
CL2 high-level width (X drivers on one side)	t_{TCL2HS}	30		ns	
CL2 low-level width (X drivers on one side)	t_{TCL2LS}	30		ns	
CL2 cycle time (X drivers on both side)	t_{TCL2D}	266		ns	
CL2 high-level width (X drivers on both side)	t_{TCL2HD}	80		ns	
CL2 low-level width (X drivers on both side)	t_{TCL2LD}	80		ns	
CL2 rise time	t_{CL2r}		30	ns	
CL2 fall time	t_{CL2f}		30	ns	
CL1 high-level width	t_{TCL1H}	200		ns	
CL1 rise time	t_{CL1r}		30	ns	
CL1 fall time	t_{CL1f}		30	ns	
Data delay time	t_{DD1}	−20	20	ns	
Data set up time	t_{LDS}	15		ns	
Data hold time	t_{LDH}	15		ns	
CL1 setup time	t_{TSCL1}	500		ns	
CL1 hold time	t_{THCL1}	200		ns	
CL3 delay time	t_{DCL3}	50		ns	
M delay time	t_{DM}		300	ns	
FLM hold time	t_{TFH}	200		ns	
LDOTCK cycle time	t_{WLDOT}	33		ns	

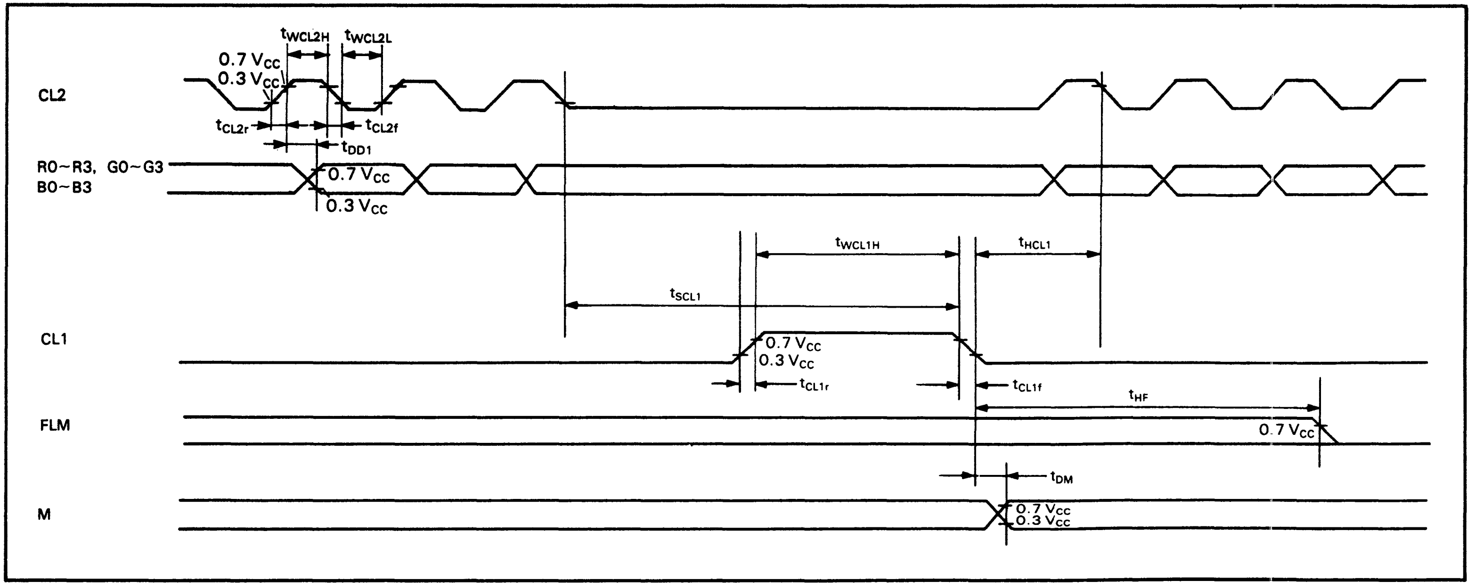


Figure 32. LCD Driver Interface (TN-Type LCD Driver Interface)

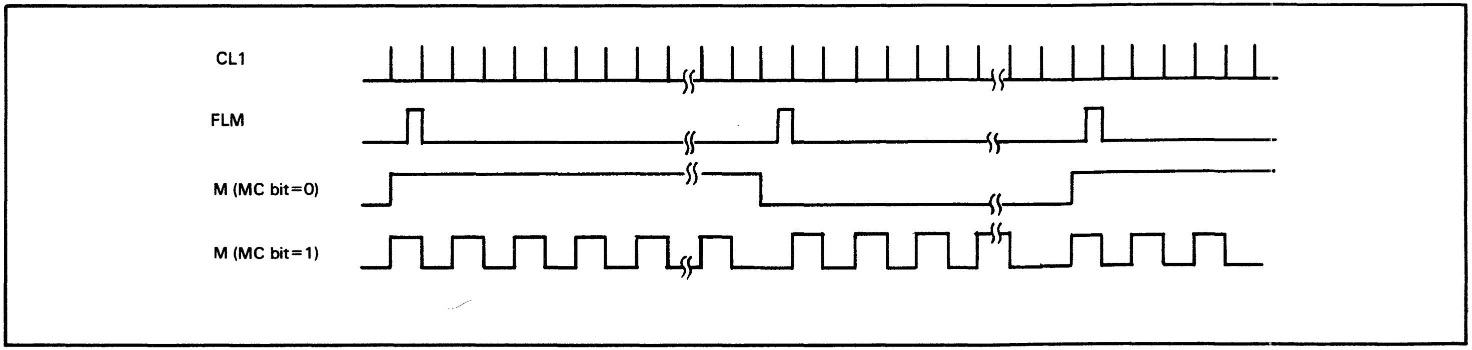


Figure 33. CL1, FLM and M (Reduced View of Figure 32)

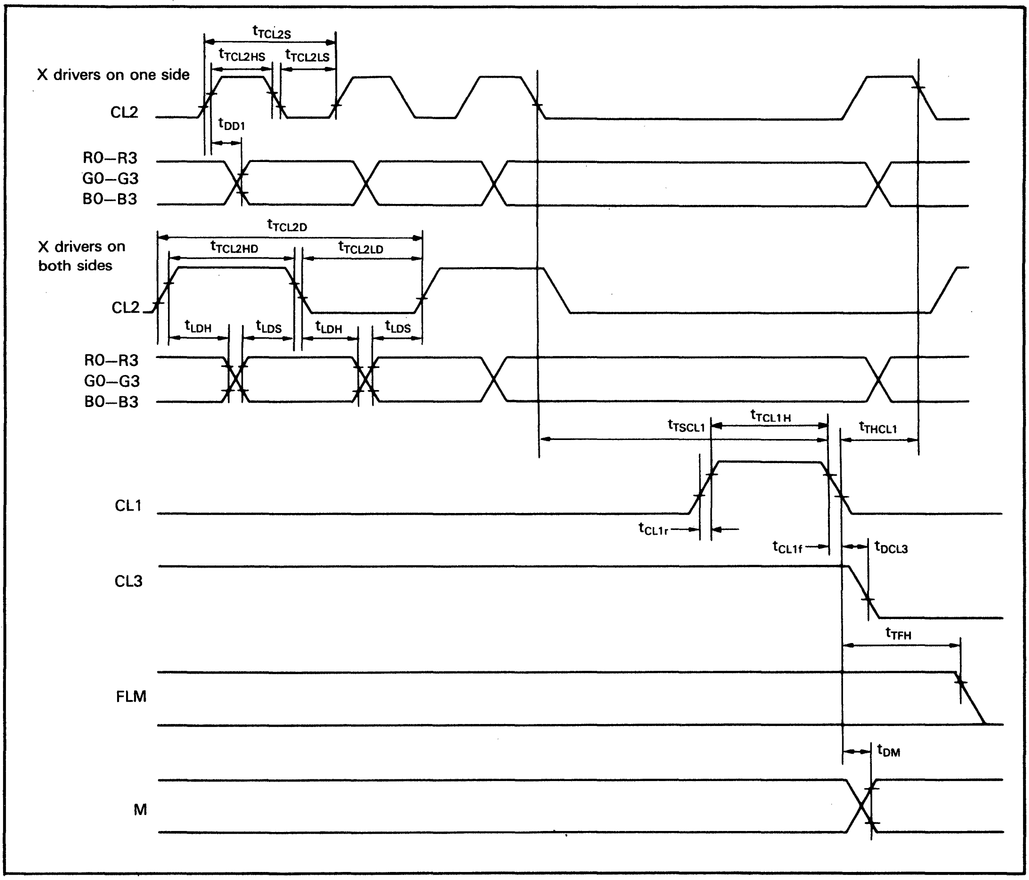


Figure 34. LCD Driver Interface (TFT-type LCD Driver Interface)

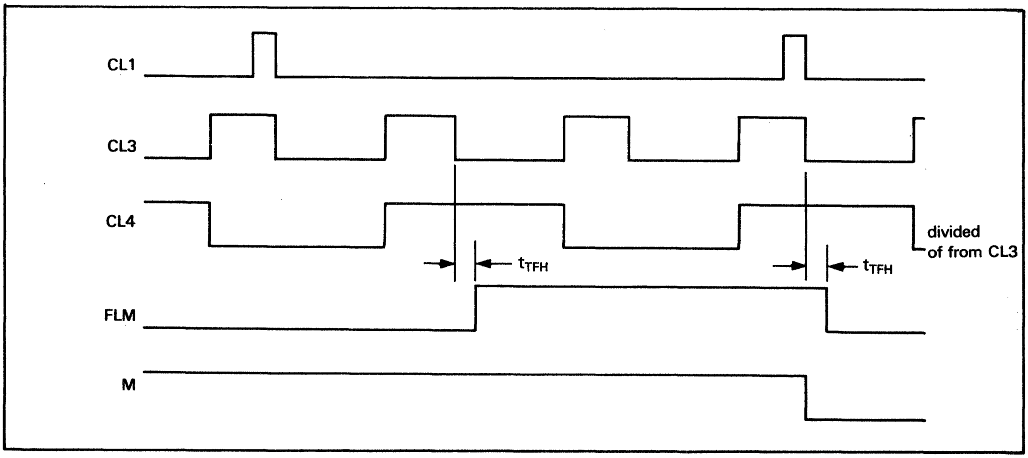


Figure 35. CL1, CL3, CL4, FLM, M (Reduced view of figure 34 at the horizontal stripe mode)

Register Progrmming, MPU Write

Item	**Symbol**	**Min**	**Max**	**Unit**
$\overline{\text{RD}}$ high-level pulse width	t_{WRDH}	190	—	ns
$\overline{\text{RD}}$ low-level pulse width	t_{WRDL}	190	—	ns
$\overline{\text{WE}}$ high-level pulse width	t_{WWEH}	190	—	ns
$\overline{\text{WE}}$ low-level pulse width	t_{WWEL}	190	—	ns
$\overline{\text{CS}}$, RS setup time	t_{AS}	0	—	ns
$\overline{\text{CS}}$, RS hold time	t_{AH}	0	—	ns
D0-D3 setup time	t_{DSW}	100	—	ns
D0-D3 hold time	t_{DHW}	0	—	ns
D0-D3 output delay time	t_{DDR}	—	150	ns
D0-D3 output hold time	t_{DHR}	10	—	ns

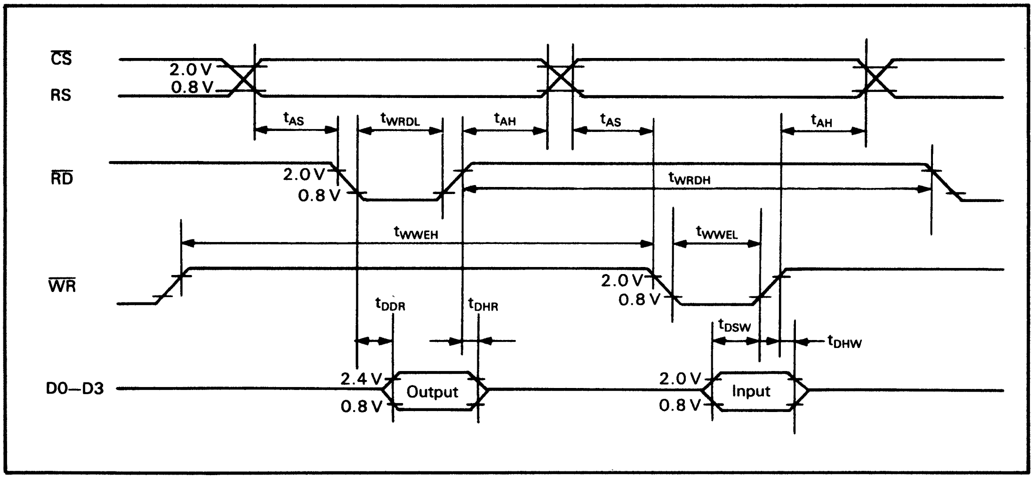


Figure 36. MPU Write Timing

Register Programming, ROM Write

Item	Symbol	Min	Max	Unit
A cycle time	t_{CYCA}	528	—	ns
A rise time	t_{Ar}	—	100	ns
A fall time	t_{Af}	—	100	ns
D ROM data setup time	t_{DSWD}	120	—	ns
D ROM data hold time	t_{DHWD}	0	—	ns

Note: t_{CYCA} = 16 t_{CYCD}

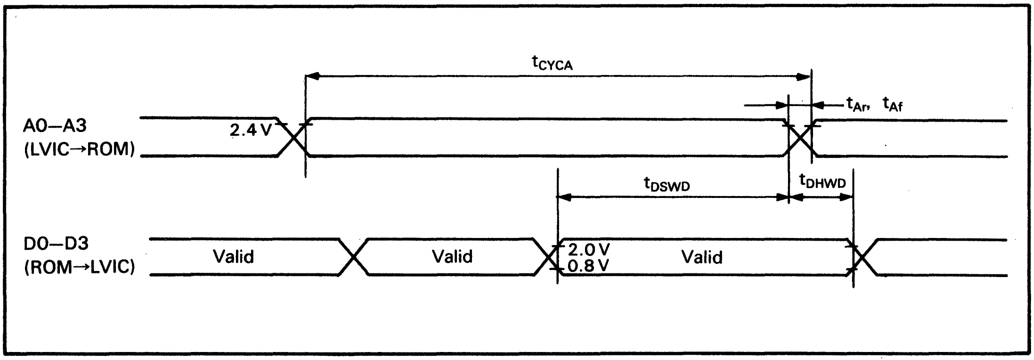


Figure 37. ROM Write Timing

PLL Interface

Item	Symbol	Min	Max	Unit
$\overline{\text{CU}}$ fall delay time	t_{Uf}	—	80	ns
$\overline{\text{CU}}$ rise delay time	t_{Ur}	—	80	ns
$\overline{\text{CD}}$ fall delay time	t_{Df}	—	80	ns
$\overline{\text{CD}}$ rise delay time	t_{Dr}	—	80	ns

Reset Input

Item	Symbol	Min	Max	Unit
$\overline{\text{RES}}$ input pulse width	$t_{\overline{RES}}$	1	—	μs

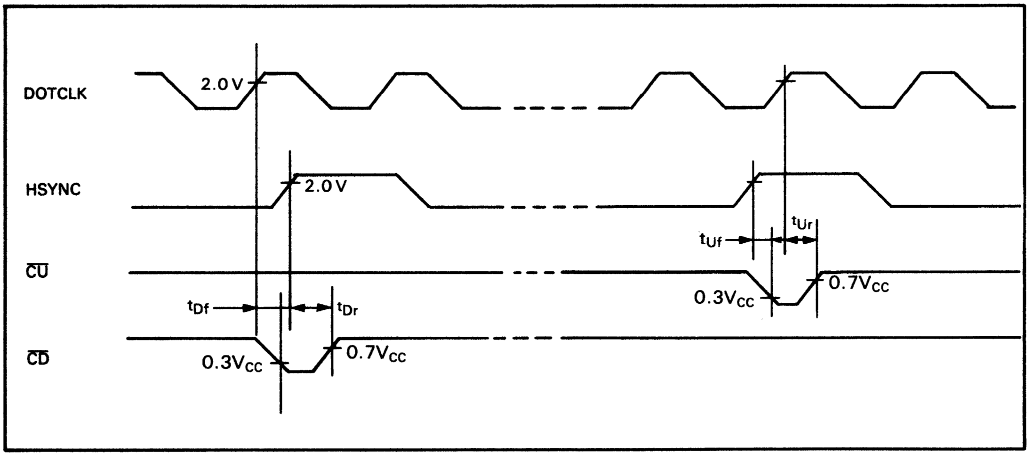


Figure 38. PLL Interface

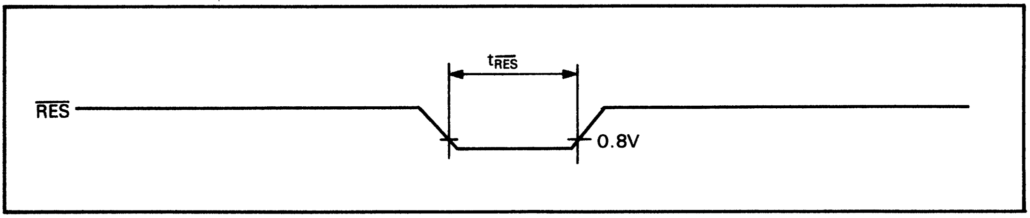


Figure 39. Reset Input

Load Circuits

TTL Load

Pin	**R_L**	**R**	**C_L**	**Remarks**
MA0-MA15, $\overline{\text{MWE}}$, $\overline{\text{MCS0}}$,$\overline{\text{MCS1}}$, RD0-RD7, GD0-GD7, BD0-BD7	2.4 kΩ	11 kΩ	40 pF	tr, tf: Not specified
A0/RD/XDOT, A1/YL0-A3/YL2	2.4 kΩ	11 kΩ	40 pF	tr, tf: Specified

Capacitive Load

Pin	**C**	**Remarks**
CL1, CL2, CL3, CL4	40 pF	tr, tf: Specified
R0-R3, G0-G3, B0-B3, FLM $\overline{\text{CU}}$, $\overline{\text{CD}}$	40 pF	tr, tf: Not specified

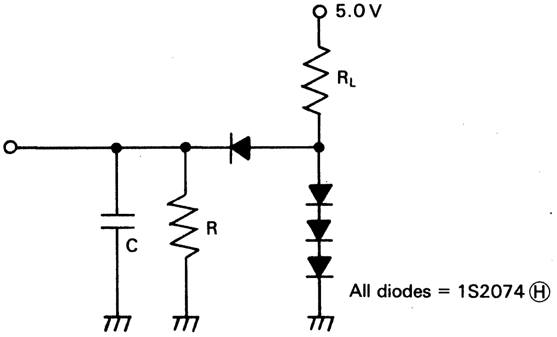


Figure 40. TTL Load Circuit

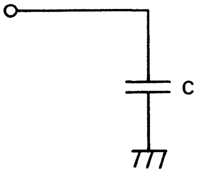


Figure 41. Capacitive Load Circuit

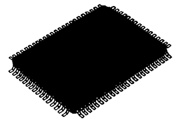
HD61602/HD61603
(Segment Type LCD Driver)

DESCRIPTION

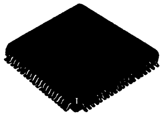
The HD61602 and the HD61603 are liquid crystal display driver LSIs with TTL and CMOS compatible interface. Each of the LSIs can be connected to various microcomputers such as the HMCS6800 series.

The HD61602 incorporates the power supply circuit for liquid crystal display driver. By the software-controlled liquid crystal driving method, several types of liquid crystals can be connected according to the applications.

The HD61603 is a liquid crystal display driver LSI only for static drive and has 64 segment outputs that can display 8 digits per chip.



(FP-80)



(FP-80A)

■ FEATURES

- Wide-range operating voltage

  Operates in a wide range of supply voltage 2.2V to 5.5V.
  Compatible with TTL interface at 4.5V to 5.5V.

- Low current consumption

  Can drive from a battery power supply (100μA max. on 5V).
  Standby input enables a standby operation at lower current consumption (5μA max. on 5V).

- Internal power supply circuit for liquid crystal display driver (HD61602).

  Internal power supply circuit for liquid crystal display driver facilitates the connection to a microcomputer system.

- Versatile segment driving capacity

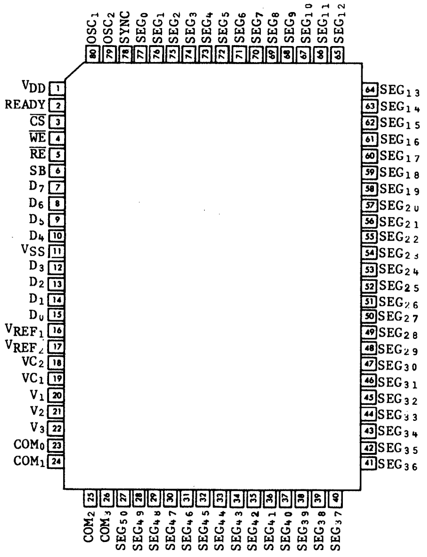
Type No.	Driving method		Display segments	Example of use	Frame freq.(Hz) at fosc=100kHz	Package
HD61602	Static		51	8 segments × 6 digits +3 marks	33	80-pin Plastic QFP (FP-80 FP-80A)
	1/2 bias	1/2 duty	102	8 segments × 12 digits +6 marks	65	
	1/3 bias	1/3 duty	153	9 segments × 17 digits	208	
		1/4 duty	204	8 segments × 25 digits +4 marks	223	
HD61603	Static		64	8 segments × 8 digits	33	80-pin Plastic QFP (FP-80)

■ ORDERING INFORMATION

Type No.	Package
HD61602R	80-pin plastic QFP (FP-80)
HD61602RH	80-pin plastic QFP (FP-80A)
HD61603R	80-pin plastic QFP (FP-80)

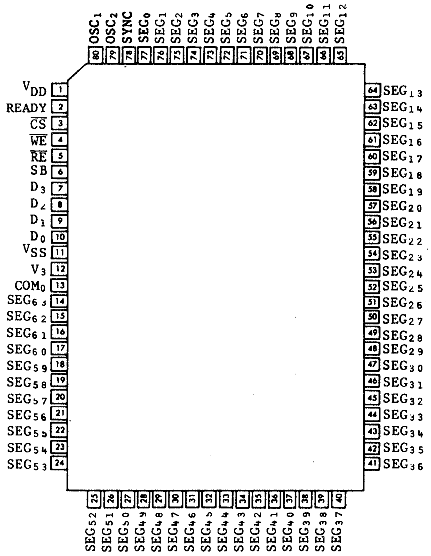
■ PIN ARRANGEMENT (TOP VIEW)

HD61602



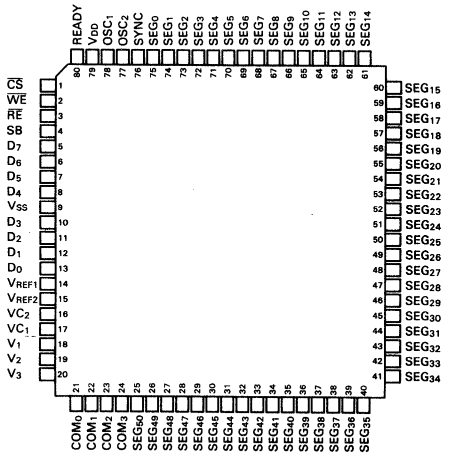
(FP-80)

HD61603



(FP-80)

HD61602

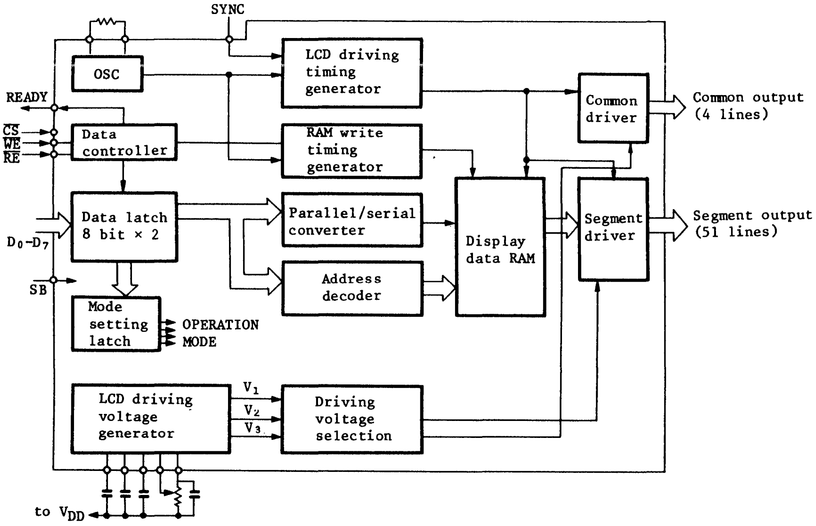


(FP-80A)

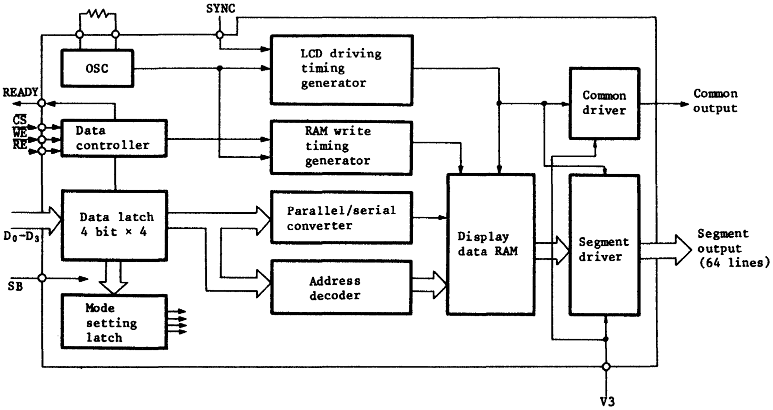
(Top View)

■ BLOCK DIAGRAM

HD61602



● HD61603



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Limit	Unit
Power supply voltage*	V_{DD}, V1, V2, V3	0.3 ∿ +7.0	V
Terminal voltage*	V_T	0.3 ∿ V_{DD} -0.3	V
Operating temperature	Topr	-20 ∿ +75	°C
Storage temperature	Tstg	-55 ∿ +125	°C

* Value referred to V_{SS}=0V.

Note: If LSIs are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristics limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Limit			Unit
		Min.	Typ	Max.	
Power supply voltage	V_{DD}	2.2	-	5.5	V
	V1, V2, V3	0.3	-	$-V_{DD}$ +0.3	V
Terminal voltage*	V_T	0	-	$-V_{DD}$	V
Operating temperature	Topr	-20	-	75	°C

* Value referred to V_{SS}=0V.

■ ELECTRICAL CHARACTERISTICS

● DC Characteristics (1)

(V_{SS}=0V, V_{DD}=4.5 to 5.5V, Ta=-20 to +75°C, unless otherwise noted)

Item		Symbol	Test condition	Limit			Unit
				Min.	Typ	Max.	
Input "High" voltage	OSC1	V_{IH1}		$0.8V_{DD}$	-	V_{DD}	V
	Others	V_{IH2}		2.0	-	V_{DD}	V
Input "Low" voltage	OSC1	V_{IL1}		0	-	$0.2V_{DD}$	V
	Others	V_{IL2}		0	-	0.8	V
Output leakage current	READY	I_{OH}	$V_O=V_{DD}$	-	-	5	μA
Output "Low" voltage	READY	V_{OL}	I_{OL}=0.4mA	-	-	0.4	V
Input leakage current *1	Input terminal	I_{IL1}	$V_{IN}=0 \sim V_{DD}$	-1.0	-	1.0	μA
	V1	I_{IL2}	$V_{In}=0 \sim V3$	- 20	-	20	μA
	V2,V3	I_{IL3}		-5.0	-	5.0	μA
LCD driver voltage drop	COM0∼COM3	V_{d1}	±Id=3μA for each COM $V3=V_{DD}-3V$	-	-	0.3	V
	SEG0∼SEG50	V_{d2}	±Id=3μA for each SEG $V3=V_{DD}-3V$	-	-	0.6	V
Power supply current		I_{DD}	During display* Rosc=360kΩ	-	-	100	μA
		I_{DD}	At standby	-	-	5	μA
Internal Driving voltage drop	V1,V2,V3	V_{TR}	$V_{REF2}=V_{DD}-1V$, $C_1 \sim C_4$=0.3μF RL=3MΩ	-	-	0.4	V

* Except the transfer operation of display data and bit data.
*1 V1, V2 : applied only to HD61602.

● DC Characteristics (2)

(V_{SS}=0V, V_{DD}=2.2 to 3.8V, Ta=-20 to +75°C, unless otherwise noted)

Item		Symbol	Test condition	Limit			Unit
				Min.	Typ	Max.	
Input "High" voltage		V_{IH}		$0.8V_{DD}$	-	V_{DD}	V
Input "Low" voltage		V_{IL}		0	-	$0.1V_{DD}$	V
Output leakage current	READY	I_{OH}	$V_{IN}=V_{DD}$	-	-	5	μA
Output "Low" voltage	READY	V_{OL}	I_{OL}=0.04mA	-	-	$0.1V_{DD}$	V
Input leakage current *1	Input terminal	I_{IL1}	$V_{IN}=0 \sim V_{DD}$	-1.0	0	1.0	μA
	V1	I_{IL2}	$V_{In}=0 \sim V3$	- 20	-	20	μA
	V2,V3	I_{IL3}		-5.0	-	5.0	μA
LCD driver voltage drop	COM0∼COM3	V_{d1}	±Id=3μA for each COM $V3=V_{DD}-3V$	-	-	0.3	V
	SEG0∼SEG50	V_{d2}	±Id=3μA for each SEG $V3=V_{DD}-3V$	-	-	0.6	V
Power supply current		I_{SS}	During display* Rosc=330kΩ	-	-	50	μA
		I_{SS}	At standby	-	-	5	μA
Internal Driving voltage drop	V1,V2,V3	V_{TR}	$V_{REF2}=V_{DD}-1V$, $C1 \sim C4$=0.3μF R_L=3MΩ, $V_{DD}=3 \sim 3.8V$	-	-	0.4	V

* Except the transfer operation of display data and bit data.
*1 V1, V2 : applied only to HD61602.

- AC Characteristics (1)

(V_{SS}=0V, V_{DD}=4.5 to 5.5V, Ta=−20 to +75°C, unless otherwise noted)

Item		Symbol	Test condition	Limit			Unit
				Min.	Typ	Max.	
Oscillation frequency	OSC2	fosc	R_{osc}=360kΩ	70	100	130	kHz
External clock frequency	OSC1	f_{osc}		70	100	130	kHz
External clock duty	OSC1	Duty		40	50	60	%
I/O signal timing		t_S		400	-	-	ns
		t_H		10	-	-	ns
		t_{WH}		300	-	-	ns
		t_{WL}		400	-	-	ns
		t_{WR}		400	-	-	ns
		t_{DL}	Fig. 5	-	-	1.0	μs
		t_{EN}		400	-	-	ns
		t_{OP1}	For display data transfer	9.5	-	10.5	Clock
		t_{OP2}	For bit and mode data transfer	2.5	-	3.5	Clock
Input signal rise time and fall time		t_r,t_f		-	-	25	ns

- AC Characteristics (2)

(V_{SS}=0V, V_{DD}=2.2 to 3.8V, Ta=−20 to +75°C, unless otherwise noted)

Item		Symbol	Test condition	Limit			Unit
				Min.	Typ	Max.	
Oscillation frequency	OSC2	f_{osc}	R_{osc}=330kΩ	70	100	130	kHz
External clock frequency	OSC1	f_{osc}		70	100	130	kHz
External clock duty	OSC1	Duty		40	50	60	%
I/O signal timing (V_{DD}=3.0∿3.8V)		t_S		1.5	-	-	μs
		t_H		1.0	-	-	μs
		t_{WH}		1.5	-	-	μs
		t_{WL}		1.5	-	-	μs
		t_{DL}	Fig. 6	-	-	2.0	μs
		t_{WR}		1.5	-	-	μs
		t_{EN}		2.0	-	-	μs
		t_{OP1}	For display data transfer	9.5	-	10.5	Clock
		t_{OP2}	For bit and mode data transfer	2.5	-	3.5	Clock
Input signal rise time and fall time		tr, tf		-	-	25	ns

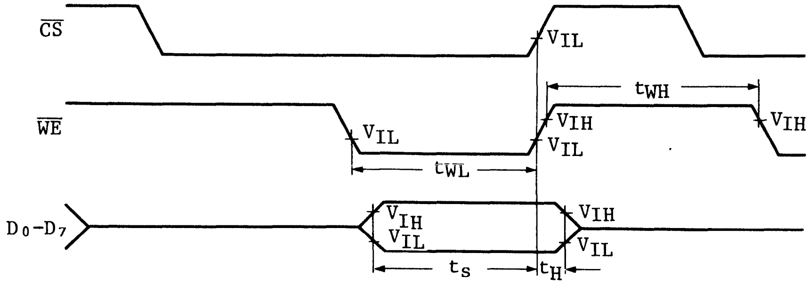


Fig. 1 Write Timing
(RE is fixed on "High" level, and SYNC on "Low" level)

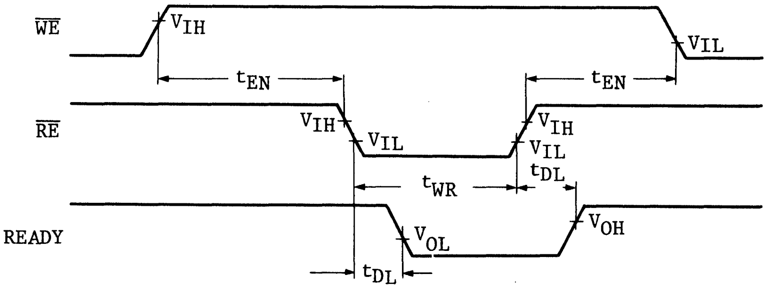


Fig. 2 Reset/Read Timing
(CS and SYNC are fixed on "Low" level)

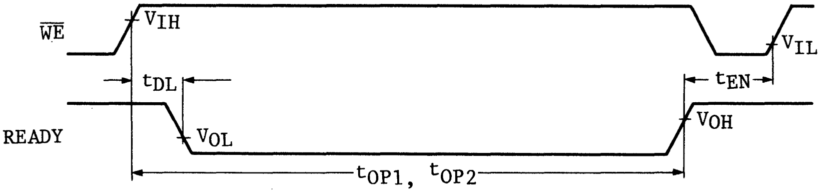


Fig. 3 READY Timing
(When the READY output is always available)

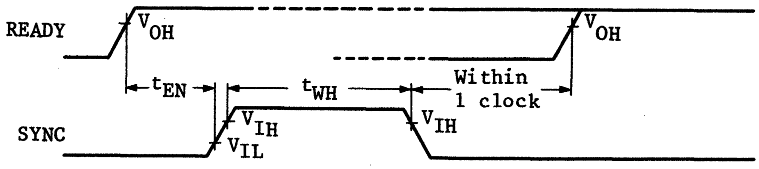
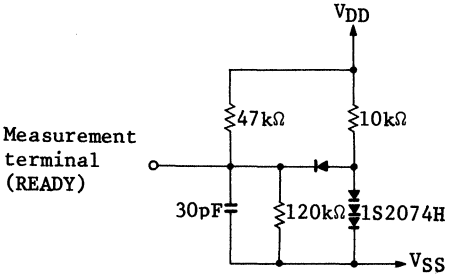


Fig. 4 SYNC Timing



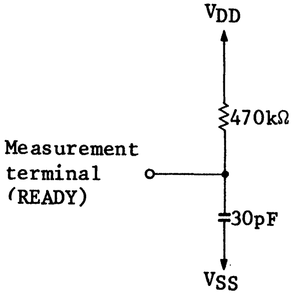


Fig. 5 Bus Timing Load Circuit (LS-TTL Load)

Fig. 6 Bus Timing Load Circuit (CMOS Load)

■ TERMINAL FUNCTIONS

- HD61602 Terminal Functions

Terminal name	No. of lines	Input/output	Connected to	Function
V_{DD}	1	Power supply		⊕ -side power supply
READY	1	NMOS open drain output	MCU	During setting data in the display data RAM and mode setting latch in the LSI after data transfer, "Low" is output to the READY terminal to inhibit the next data input. There are two types of modes: one in which "Low" is output only when both of $\overline{CS}$ and $\overline{RE}$ are "Low", and the other in which "Low" is output regardless of $\overline{CS}$ and $\overline{RE}$.
$\overline{CS}$	1	Input	MCU	Chip select input. Data can be written only when this terminal is "Low".
$\overline{WE}$	1	Input	MCU	Write enable input. Input data of D0 to D7 is latched at the rising edge of $\overline{WE}$.
$\overline{RE}$	1	Input	MCU	Resets the input data byte counter. After both of $\overline{CS}$ and $\overline{RE}$ are "Low", the first data is recognized as the 1st byte data.
SB	1	Input	MCU	"High" level input stops the LSI operations. (i) Stops oscillation and clock input. (ii) Stops LCD driver. (iii) Stops writing data into display RAM.
D0∿D7	8	Input	MCU	Data input terminal from where 8-bit × 2-byte data are input.
V_{SS}	1	Power supply		⊖ -side power supply
V_{REF1}	1	Output	External R	Reference voltage output. LCD driving voltage is generated by this voltage.
V_{REF2}	1	Input	External R	Divides the reference voltage of V_{REF1} with external R to determine LCD driving voltage. $V_{REF2}=V1$
V_{C1}, V_{C2}	2	Output	External C	Connection terminals for boosting C of LCD driving voltage generator. An external C is connected between V_{C1} and V_{C2}.

Terminal name	No. of lines	Input/output	Connected to	Function
V1, V2, V3	3	Output (Input)	External C	LCD driving voltages are output. An external C is connected to each terminal.
COM0∿COM3	4	Output	LCD	LCD common (backplate) driving output.
SEG0∿SEG50	51	Output	LCD	LCD segment driving output.
SYNC	1	Input	MCU	Synchronous input for 2 or more chips application. LCD driver timing circuit is reset by "High" input. LCD is off.
OSC1 OSC2	2	Input Output	External R	Attaches external R to these terminals for oscillation. An external clock (100kHz) can be input from OSC1.

Note: Logic polarity is positive. "1"="H"=active.

o HD61603 Terminal Functions

Terminal name	No. of lines	Input/output	Connected to	Function
V_{DD}	1	Power supply		⊕ -side power supply
READY	1	NMOS open drain output	MCU	During setting data in the display data RAM and mode setting latch in the LSI after data transfer, "Low" is output to the READY terminal to inhibit the next data input. There are two types of modes: one in which "Low" is output only when both of $\overline{CS}$ and $\overline{RE}$ are "Low", and the other in which "Low" is output regardless of $\overline{CS}$ and $\overline{RE}$.
$\overline{CS}$	1	Input	MCU	Chip select input. Data can be written only when this terminal is "Low".
$\overline{WE}$	1	Input	MCU	Write enable input. Input data of D0 to D3 is latched at the rising edge of $\overline{WE}$.
$\overline{RE}$	1	Input	MCU	Reset the input data byte counter. After both of $\overline{CS}$ and $\overline{RE}$ are "Low", the first data is recognized as the 1st byte data.

Terminal name	No. of lines	Input/output	Connected to	Function
SB	1	Input	MCU	"High" level input stops the LSI operations. (i) Stops oscillation and clock input. (ii) Stops LCD driver. (iii) Stops writing data into display RAM.
D0∼D3	4	Input	MCU	Data input terminal from where 4-bit X4 data are input.
V_{SS}	1	Power supply		⊖ -side power supply
V3	1	Input	Power supply	Power supply input for LCD drive. Voltage between V_{DD} and V3 is used as driving voltage.
COM0	1	Output	LCD	LCD common (backplate) driving output.
SEG0∼SEG63	64	Output	LCD	LCD segment driving output.
SYNC	1	Input	MCU	Synchronous input for 2 or more chips application. LCD driver timing circuit is reset by "High" input. LCD is off.
OSC1 OSC2	2	Input Output	External R	Attaches external R to these terminals for oscillation. An external clock (100kHz) can be input from OSC1.

Note: Logic polarity is positive. "1"="H"=active.

■ DISPLAY RAM

< HD61602 Display RAM >

The HD61602 has an internal display RAM shown in Fig. 7. Display data is stored in the RAM, or is read according to the LCD driving timing to display on the LCD. One bit of the RAM corresponds to the 1 segment of LCD. Note that some bits of the RAM cannot be displayed depending on LCD driving mode.

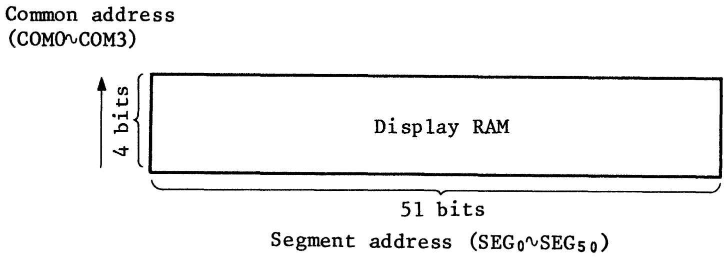


Fig. 7 Display RAM

• Reading Data from Display RAM

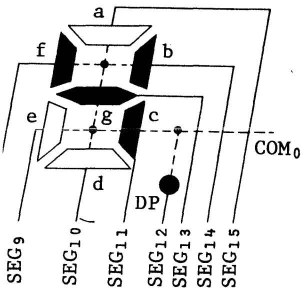
A display RAM segment address corresponds to a segment output. The data at segment address SEGn is output to segment output SEGn terminal.
A common address corresponds to the output timings of a common output and a segment output. The same common address data is simultaneously read. The data of display RAM is reproduced on the LCD panel.

When a 7-segment type LCD driver is connected, for example, the correspondence between the display RAM and the display pattern in each mode is as follows:

(1) Static drive

In the static drive, only the column of COM0 of display RAM is output. COM1 to COM3 are not displayed.

LCD connection

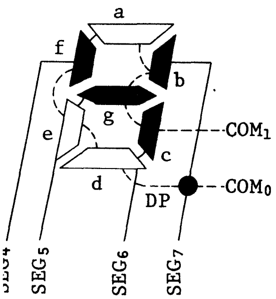


Display RAM

COM$_3$								
COM$_2$								
COM$_1$								
COM$_0$	f	e	d	c	DP	g	b	a
	SEG$_8$	SEG$_9$	SEG$_{10}$	SEG$_{11}$	SEG$_{12}$	SEG$_{13}$	SEG$_{14}$	SEG$_{15}$

(2) 1/2 duty drive

LCD connection



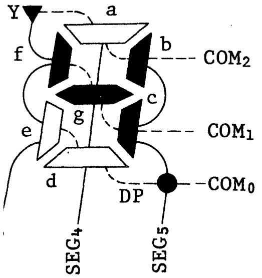
Display RAM

COM$_3$							
COM$_2$							
COM$_1$	a	g	c	b			
COM$_0$	f	e	d	DP			
	SEG$_4$	SEG$_5$	SEG$_6$	SEG$_7$	SEG$_8$	SEG$_9$	

In the 1/2 duty drive, the columns of COM0 and COM1 of display RAM are output in time sharing. The columns of COM2 and COM3 are not displayed.

(3) 1/3 duty drive

LCD connection



Display RAM

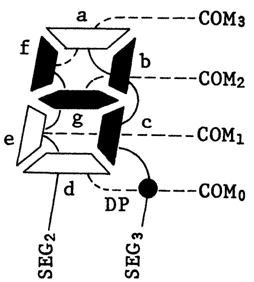
COM$_3$					
COM$_2$	Y	a	b		
COM$_1$	f	g	c		
COM$_0$	e	d	DP		
	SEG$_3$	SEG$_4$	SEG$_5$	SEG$_6$	

In the 1/3 duty drive, the columns of COM0 to COM2 are output in time sharing. No column of COM3 is displayed.

"Y" cannot be rewritten by display data (input on an 8-segment basis). Please use bit manipulation in turning on/off the display of "Y".

(4) 1/4 duty drive

LCD connection



Display RAM

COM$_3$	f	a		
COM$_2$	g	b		
COM$_1$	e	c		
COM$_0$	d	DP		
	SEG$_2$	SEG$_3$	SEG$_4$	

In the 1/4 duty drive, all the columns of COM0 to COM3 are displayed.

- Writing Data into Display RAM

Data is written into the display RAM in the following five methods:

(1) Bit manipulation
Data is written into any bit of RAM on a bit basis.

(2) Static display mode
8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.

(3) 1/2 duty display mode
8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/2 duty drive.

(4) 1/3 duty display mode
8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/3 duty drive.

(5) 1/4 duty display mode
8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/4 duty drive.

The RAM area and the allocation of the segment data for 1-digit display depend on the driving methods as described in the selection of "Reading Data from Display RAM".

8-bit data is written on a digit basis corresponding to the above duty driving methods. The digits are allocated as shown Fig. 8 (allocation of digit). As the data can be transferred on a digit basis from a microcomputer, transfer efficiency is improved by allocating the LCD pattern according to the allocation of each bit data of the digit in the data RAM.

Fig. 8 shows the digit address (displayed as Adn) to specify the store address of the transferred 8-bit data on a digit basis.

Fig. 9 shows the correspondence between each segment in an Adn and the 8-bit input data.

When data is transferred on a digit basis, 8-bit display data and digit address should be specified as described above.

However, when the digit address is Ad6 of static, Ad12 of 1/2 duty, or Ad25 of 1/4 duty, display RAM does not have enough bits for the data. Thus the extra bits of the input 8-bit data are ignored.

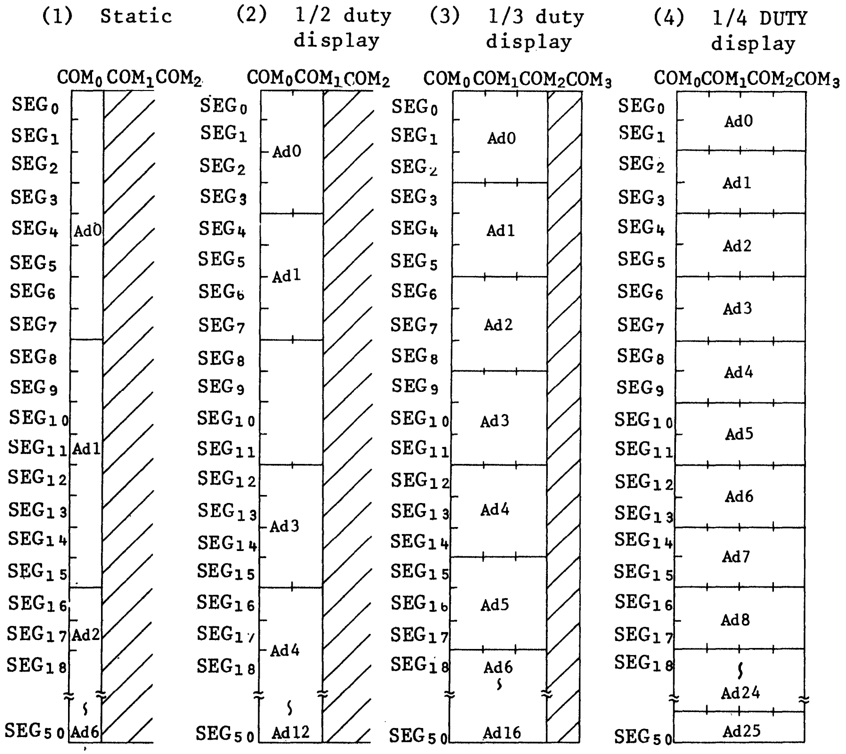


Fig. 8 Allocation of Digit (HD61602)

(1) Static display

	COM_0
SEG_8	Bit 7
SEG_{8n+1}	6
SEG_{8n+2}	5
SEG_{8n+3}	4
SEG_{8n+4}	3
SEG_{8n+5}	2
SEG_{8n+6}	1
SEG_{8n+7}	Bit 0

(2) 1/2 duty display

	COM_0	COM_1
SEG_{4n}	Bit 7	6
SEG_{4n+1}	5	4
SEG_{4n+2}	3	2
SEG_{4n+3}	1	Bit 0

(3) 1/3 duty display

	COM_0	COM_1	COM_2
SEG_{3n}	Bit 7	6	☒
SEG_{3n+1}	5	4	3
SEG_{3n+2}	2	1	Bit 0

(4) 1/4 duty display

	COM_0	COM_1	COM_2	COM_3
SEG_{2n}	Bit 7	6	5	4
SEG_{2n+1}	3	2	1	Bit 0

Fig. 9 Bit Assignment in an Adn (HD61602)

In the bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data, a segment address (6 bits) and a common address (2 bits) should be specified.

< HD61603 Display RAM >

The HD61603 has an internal display RAM as shown in Fig. 10. Display data is stored in the RAM and output to the segment output terminal.

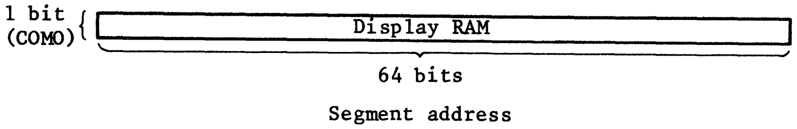


Fig. 10 Display RAM (HD61603)

- **Reading Data from Display RAM**

Each bit of the display RAM corresponds to each LCD segment. The data at segment address SEGn is output to segment output SEGn terminal. Fig. 11 shows an example of the correspondence between the display RAM bit and the display pattern when a 7-segment type LCD is connected.

LCD connection

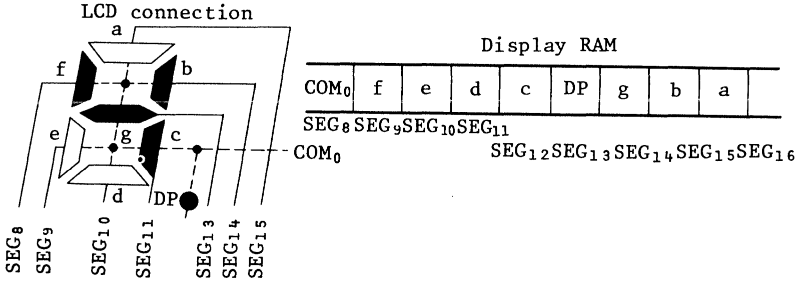


Fig. 11 Example of Correspondence between Display RAM Bit and Display Pattern (HD61603)

- Writing Data into Display RAM

Data is written into the display RAM in the following two methods:

(1) Bit manipulation

Data is written into any bit of RAM on a bit basis.

(2) Static display mode

8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.

The 8-bit data is written on a digit basis into the digit address (displayed as Adn) shown in Fig. 12. When data is transferred from a microcomputer, four 4 bit data are needed to specify the digit address and an 8-bit display data. Fig. 13 shows the correspondence between each segment in an Adn and the transferred 8-bit data.

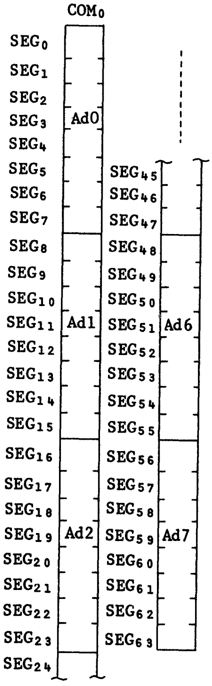


Fig. 12 Allocation of Digit (HD61603)

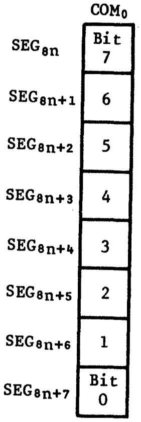


Fig. 13 Bit Assignment in an Adn (HD61603)

In the bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data and a segment address (6 bits) should be specified.

Operating Modes

< HD61602 Operating Modes >

The HD61602 has the following operating modes:

(1) LCD drive mode
Determines the LCD driving method.

(a) Static drive mode
LCD is driven statically.

(b) 1/2 duty drive mode
LCD is driven at 1/2 duty and 1/2 bias.

(c) 1/3 duty drive mode
LCD is driven at 1/3 duty and 1/3 bias.

(d) 1/4 duty drive mode
LCD is driven at 1/4 duty and 1/3 bias.

(2) Data display mode

Determines how to write display data into the data RAM.

(a) Static display mode
8-bit data is written into the display RAM according to the digit in the static drive.

(b) 1/2 duty display mode
8-bit data is written into the display RAM according to the digit in the 1/2 duty drive.

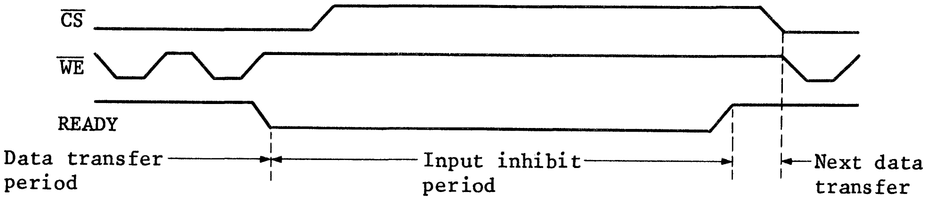
(c) 1/3 duty display mode
8-bit data is written into the display RAM according to the digit in the 1/3 duty drive.

(d) 1/4 duty display mode
8-bit data is written into the display RAM according to the digit in the 1/4 duty display drive.

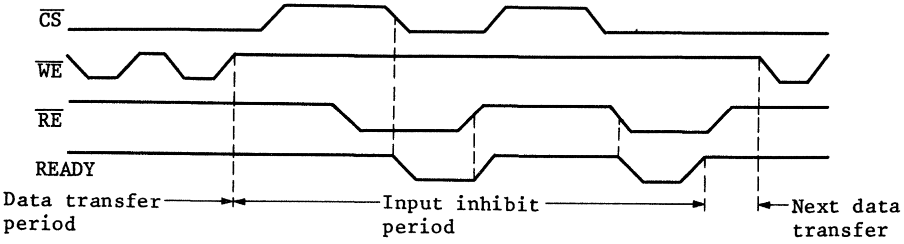
(3) READY output mode

Determines the READY output timing.
After data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when the READY is output can be selected from the following two modes:

(a) READY is always available.



(b) READY is available by $\overline{CS}$ and $\overline{RE}$.



(4) LCD OFF mode

In this mode, the HD61602 stops driving LCD and turns it off.

(5) External driving voltage mode

A mode for using external driving voltage (V1, V2 and V3).

The above 5 modes are specified by mode setting data. The modes are independent of each other and can be used in any combination. The bit manipulation is independent of data display mode and can be used regardless of it.

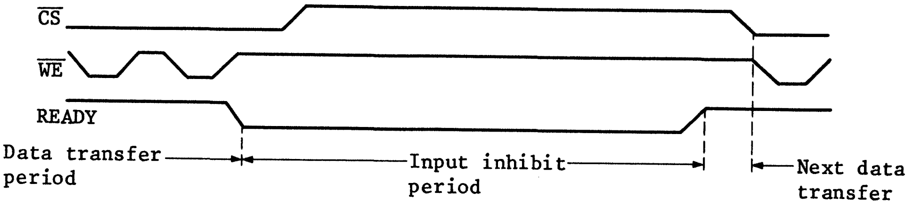
< HD61603 Operating Modes >

The HD61603 has the following modes:

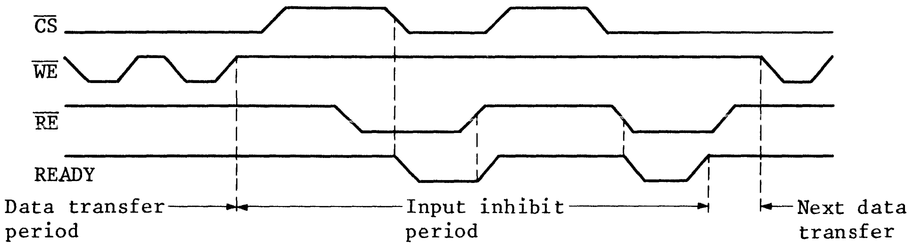
(1) READY output mode

Determines READY output timing.
After data set is transferred, the data is processed internally.
The next data cannot be acknowledged during the processing period.
The READY output reports the period to the MPU. The timing when READY is output can be selected from the following two modes:

(a) READY is always available.



(b) READY is available by $\overline{CS}$ and $\overline{RE}$.



(2) LCD OFF mode

In this mode, the HD61603 stops driving LCD and turns it off.

INPUT DATA FORMATS

HD61602 Input Data Formats

Input data is composed of 8 bits × 2. Input them as 2-byte data after READY output is changed from "Low" to "High" or "Low" pulse is entered into $\overline{RE}$ terminal.

(1) Display data (Updates display on an 8-segment basis.)

1st byte

7	6	5	4	3	2	1	0
0	0	×	Display address (Digit address Adn)				

2nd byte

7	6	5	4	3	2	1	0
Display data							

(i) Display address: Digit address Adn in accordance with each display mode.

(ii) Display data : Pattern data that is written into the display RAM according to each display mode and the address.

(2) Bit manipulation data (Updates display on a segment basis.)

1st byte

7	6	5	4	3	2	1	0
0	1	Display data	×	×	×	COM address	

2nd byte

7	6	5	4	3	2	1	0
×	×	SEG address					

(i) Display data : Data that is written into 1 bit of the specified display RAM.

(ii) COM address : Common address of display RAM.

(iii) SEG address : Segment address of display RAM

(3) Mode setting data

External power supply

1st byte

1	0	×	0		READY bit	Drive mode bits	
7	6	5	4	3	2	1	0

2nd byte

×	×	×	×	×	OFF/ON bit	Display mode bits	
7	6	5	4	3	2	1	0

(i) Display mode bits : 00; Static display mode
01; 1/2 duty display mode
10; 1/3 duty display mode
11; 1/4 duty display mode

(ii) OFF/ON bit : 1; LCD OFF (It is set to "1" when SYNC is entered.)
0; LCD ON

(iii) Drive mode bits : 00; Static drive
01; 1/2 duty drive
10; 1/3 duty drive
11; 1/4 duty drive

(iv) READY bit : 0; READY outputs "0" only while $\overline{CS}$ and $\overline{RE}$ is "0". (It is reset to "0" when SYNC is entered.) .... READY bus mode
1; READY outputs "0" regardless of $\overline{CS}$ and $\overline{RE}$. .... READY port mode

(v) External power supply bit : 0; Driving voltage is generated internally.
1; Driving voltage is supplied from external. (It is set to "1" when SYNC is entered.)

(4) 1-byte instruction

1st byte

1	1	×	×	×	×	×	×
7	6	5	4	3	2	1	0

The first data (first byte) is ignored when the bit 6 and bit 7 in the byte are "1".

< HD61603 Input Data Formats >

Input data is composed of 4 bits × 4. Input them as four 4 bit data after READY output is changed from "Low" to "High" or "Low" pulse is entered into $\overline{RE}$ terminal.

(1) Display data (Updates display on an 8-segment basis.)

	3	2	1	0
1st byte	0	0	×	×
2nd byte	×	Display address (Digit address Ada)		
3rd byte	Display data bit7	6	5	4
4th byte	Display data bit3	2	1	0

(i) Display address: Digit address Adn shown in Fig. 12.

(ii) Display data : Pattern data that is written into the display RAM as shown in Fig. 13.

(2) Bit manipulation data (Updates display on a segment basis.)

	3	2	1	0
1st byte	0	1	Display data	×
2nd byte	×	×	0	0
3rd byte	×	×	SEG address bit5	4
4th byte	SEG address bit3	2	1	0

(i) Display data : Data that is written into the 1 bit of the specified display RAM.

(ii) SEG address : Segment address of display RAM (segment output).

(3) Mode setting data

	3	2	1	0
1st byte	1	0	×	0
2nd type	×	READY bit	×	×
3rd byte	×	×	×	×
4th byte	×	OFF/ON bit	0	0

(i) OFF/ON bit : 1; LCD OFF (It is set to "1" when SYNC is entered.)
0; LCD ON

(ii) READY bit : 0; READY outputs "0" only while $\overline{\text{CS}}$ and $\overline{\text{RE}}$ are "0". (It is reset to "0" when SYNC is entered).
.... READY bus mode
1; READY outputs "0" regardless of $\overline{\text{CS}}$ and $\overline{\text{RE}}$.
.... READY port mode

(4) 1-byte instruction

	3	2	1	0
1st byte	1	1	×	×

The first data (4 bits) is ignored when the bit 3 and 2 in the data are "1".

■ HOW TO INPUT DATA

< How to Input HD61602 Data >

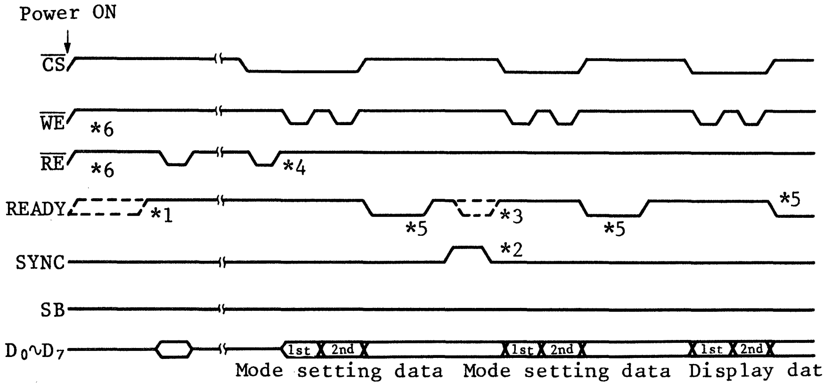
Input data is composed of 8 bits × 2. Take care that the data transfer is not interrupted. Because the first 8-bit data is distinguished from the second one depending on the sequence only.

If data transfer is interrupted or at the power ON the following two methods can be used to reset the count of the number of bytes (count of the first and second bytes):

(1) Set $\overline{CS}$ and $\overline{RE}$ inputs in "Low" (no display data changes).

(2) Input 2 or more "1-byte instruction data" which bit 7 and 6 are "1" (display data may change).

The data input method via data input terminals ($\overline{CS}$, $\overline{WE}$, D0 to D7) is similar to that of static RAM such as HM6116. An access of the LSI can be made through same bus line as ROM and RAM. When output ports of a microcomputer are used for an access, refer to the timing specifications and Fig. 14.



*1: READY output is indefinite during 12 clocks after the oscillation start when power ON (clock: OSC_2 clock).

*2: "High" pulse should be applied to SYNC terminal when using two or more chips synchronously.

*3: In the mode in which READY is always available, READY output is indefinite while "High" is being applied to SYNC.

*4: Reset the byte counter after power ON.

*5: READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.

*6: Connect a proper pull-up resistor if $\overline{WE}$ or $\overline{RE}$ may be floating.

*7: It is not always necessary to follow this example.

Fig. 14 Example of Data Transfer Sequence

< How to Input HD61603 Data >

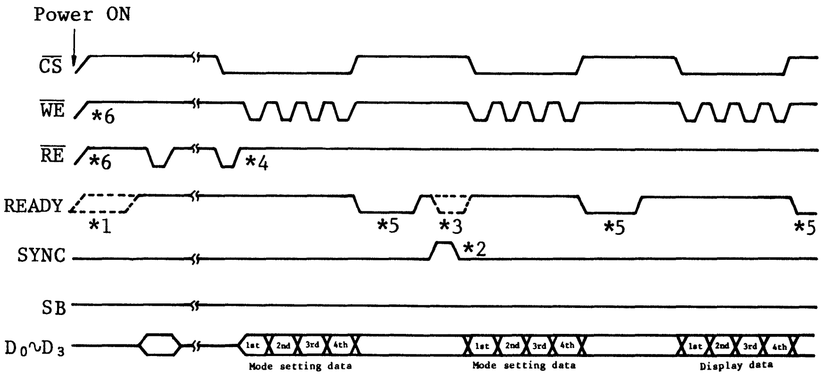
Input data is composed of 4 bits × 4. Take care that data transfer is not interrupted. Because the first 4-bit data to the fourth 4-bit data are distinguished from each other depending on the sequence only.

If data transfer is interrupted or at the Power ON, the following two methods can be used to reset the count of the number of data (count of the first 4 bit data to the fourth 4-bit data):

(1) Set $\overline{CS}$ and $\overline{RE}$ in "Low".

(2) Input 4 or more "1-byte instruction" data (4-bit data) which bit 3 and 2 are "1" (display data may change).

The data input method via data input terminals ($\overline{CS}$, $\overline{WE}$, D0 to D3) is similar to that of static RAM such as HM6116. An access of the LSI can be made through the same bus line as ROM and RAM. When output ports of a microcomputer are used for an access, refer to the timing specifications and Fig. 15.



*1: READY output is indefinite during 12 clocks after the oscillation start when power ON (clock: OSC_2 clock).

*2: "High" pulse should be applied to SYNC terminal when using two or more chips synchronously.

*3: In the mode in which READY is always available, READY output is indefinite while "High" is being applied to SYNC.

*4: Reset the 4-bit data counter after power ON.

*5: READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.

*6: Connect a proper pull-up resistor if $\overline{WE}$ or $\overline{RE}$ may be floating.

*7: It is not always necessary to follow this example.

Fig. 15 Example of Data Transfer Sequence

Notes on READY Output

Note that the READY output will be unsettled during 1.5 clocks (max) after inputting the first 2-byte data for setting the mode after turning the power on. This is because the READY bit data of mode setting latches and the mode of READY pin (READY bus or port mode) are unsettled untill the completion of mode setting.

There are two kinds of the READY output waveforms depending of the modes.

(1)READY bus mode (READY bit = 0)

(2)READY port mode (READY bit = 1)

However, if you input SYNC before mode setting, waveform will be determined; when you choose REDAY bus mode, (1) a will be output, and when you choose READY port mode, (2) a will be output. The figures can be applied both to HD61602 and HD61603.

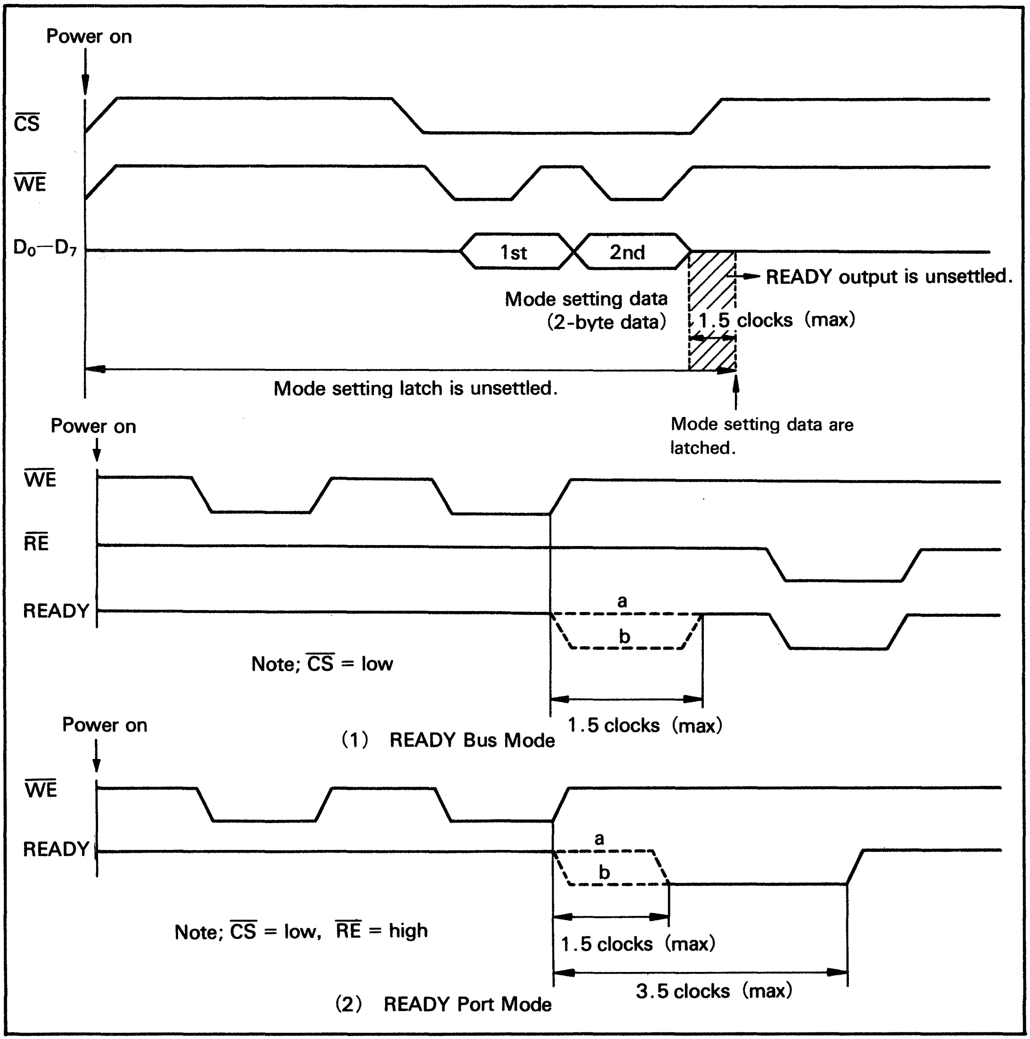


Figure 16. READY Output According to Modes

Standby Operation

Standby operation with low power consumption can be activated when pin SB is used. Normal operation of the LSI is activated when pin SB is low level, and the LSI goes into the standby state when pin SB is high level. The standby state of the LSI is as follows.

(a) LCD driver is stopped (LCD is off)
(b) Display data and operating mode are held.
(c) The operation is suspended while changing display (= while READY is outputting low.) In this case, READY outputs high within 10.5 clocks or 3.5 clocks after release from the standby mode.
(d) Oscillation is stopped.

When this mode is not used, connect pin SB to V_{SS}.

Multi-Chip Operation

When an LCD is driven with two or more chips, the driving timing of LCD must be synchronized. In this case, the chips are synchronized with each other by using SYNC input. If SYNC input is high, the LCD driver timing circuit is reset. Apply high pulse to the SYNC input after the operating mode is set.

A high pulse to the SYNC input causes the change of the mode setting data (The OFF/ON bit is set and the READY bit is reset. See (3) Mode Setting Data in "Input Data Formats".) Transfer the mode setting data into the LSI after every SYNC operation.

If a power on reset signal is applied to the SYNC pin, the LCD can be off-state when the power is turned on.

When SYNC input is not used. connect pin SYNC to V_{SS}.

In the case SB input is used, after standby mode is released, high pulse must be applied to the SYNC input, and mode setting data must be set again.

Restriction on Usage

Minimize the noise by inserting a noise bypass capacitor (≧ 1 μF) between V_{DD} and V_{SS} pins. (Insert one as near chip as possible.)

Liquid Crystal Display Drive Voltage Circuit (HD61602)

What is LCD Voltage?

HD61602 drives liquid crystal display using four levels of voltages; V_{DD}, V_1, V_2 and V_3 (V_{DD} is the highest and V_3 is the lowest). The voltage between V_{DD} and V_3 is called V_{LCD} and it is necessary to apply the appropriate V_{LCD} according to liquid crystal displays. V_3 always needs to be supplied power regardless of the display duty ratio since it supplies the voltage to the LCD drive circuit of HD61602.

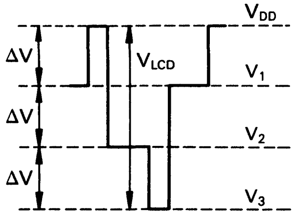


Figure 17. LCD Output Waveform and Output Levels

When internal drive power supply is used.

When the internal drive power supply is used, attach C_1-C_4 for charge pump circuits and variable resistance R_1 for deciding display drive voltage to HD61602 as shown in figure 18.
Internal voltage is available by setting external voltage switching bits of mode setting data "0".

Figure 19 shows voltage characteristics between V_{DD} and V_{REF1}.
Voltage is divided at R_1, and then into V_{REF2}. Voltage between V_{DD} and V_{REF2} is equivalent to ΔV in figure 19, and so V_{LCD} can be change by regulating the voltage.

V_{REF2} is usually regurlated by variable reistance, but in case of replacing R_1 with two invariable resistance take V_{REF1} between max and min into consideration as shown in figure 19.

Internal drive power supply is genarated by using capacity, and so much current cannot be streamed. When large liquid crystal display panel is used, examine the external drive power supply.

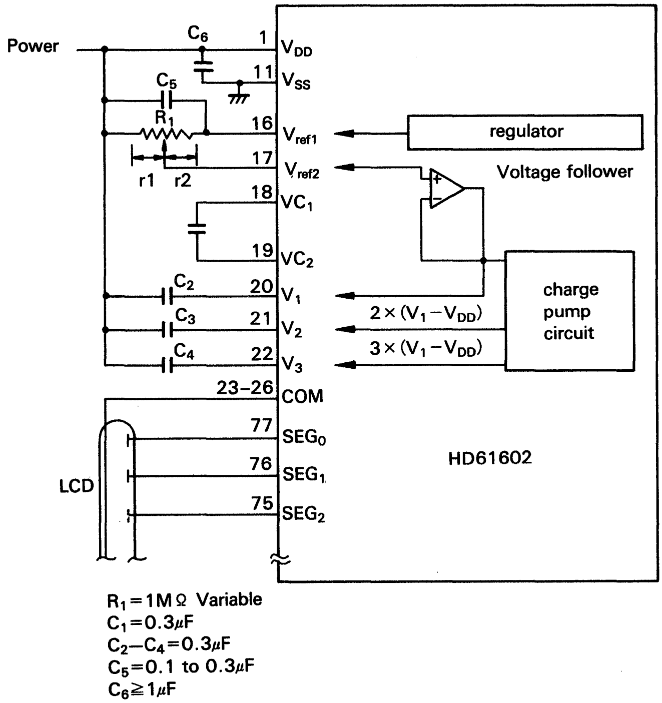


Figure 18. Example

When external drive power supply is used.

External power supply can be used by setting external voltage switching bits of mode setting data "1". When large liquid crystal display panel is used, in case of multi chip, on in need of accurate liquid crystal drive voltage, used the external power supply.

R_2-R_5 is connected in series between V_{DD} and V_{SS}, and by these resistance ratio each voltage of ΔV and V_{LCD} is generated and then supplied to V_1, V_2 and V_3. C_2-C_4 are capacities for smoothing.

When regulating shining degree, change the resistance value by setting R_5 variable resistance.

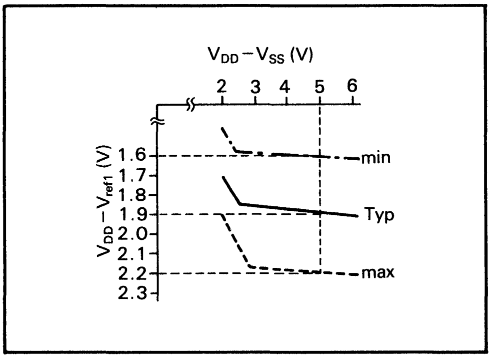
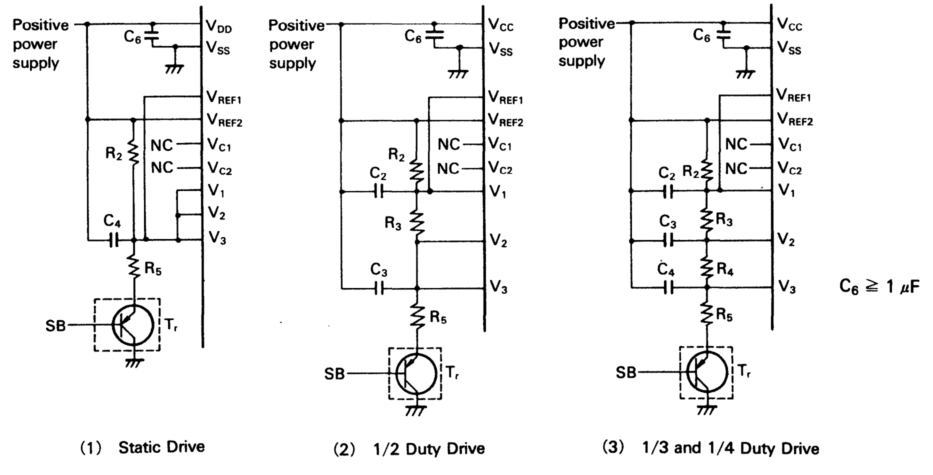


Figure 19. Voltage characteristics between V_{DD} and V_{ref1}



Note: 1. When standby mode is used, a transistor is required.
2. R_2-R_5 should be some kΩ-some tens of kΩ, and C_2-C_4 should be 0.1 μF−0.3 μF.

Figure 20. Example when External Drive Voltage is Used

Liquid Crystal Display Drive Voltage (HD61603)

As shown in figure 21 apply LCD drive voltage from the external power supply.

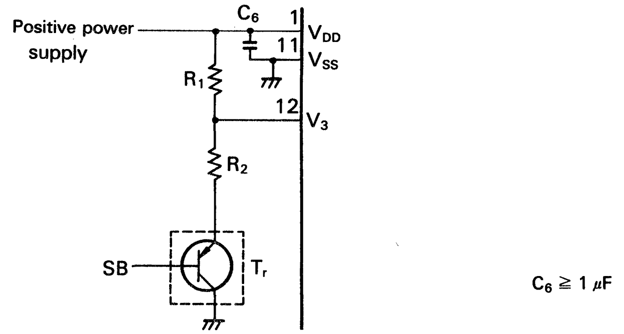
Oscillation Circuit

When Internal Oscillation Circuit is Used

When the internal oscillation cirucit is used, attach an external resistor R_{OSC} as shown in figure 22. (Insert R_{OSC} as near chip as possible, and make the OSC1 side shorter.)

When External Clock is Used

When an external clock of 100 kHz with CMOS level is provided, pin OSC1 can be used for the input pin. In this case, open pin OSC2.



Note: When standby mode is used, a transistor is required.

Figure 21. Example of Drive Voltage Generator

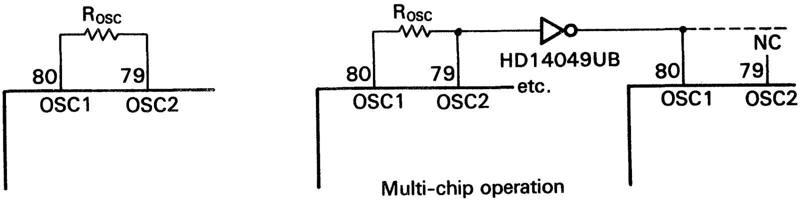


Figure 22. Example of Oscillation Circuit

Applications

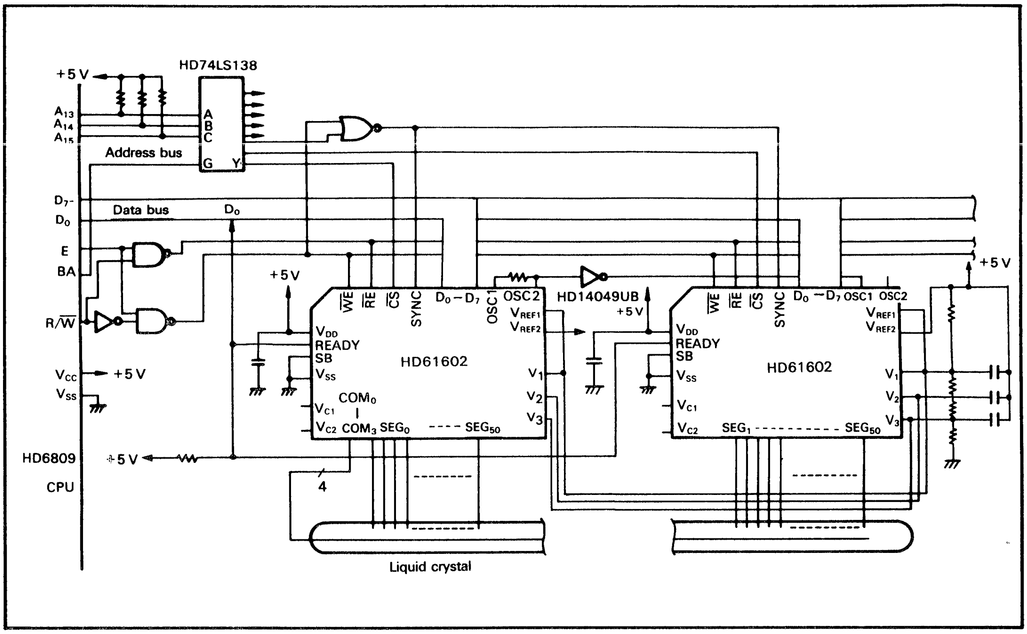


Figure 23. Example (1)

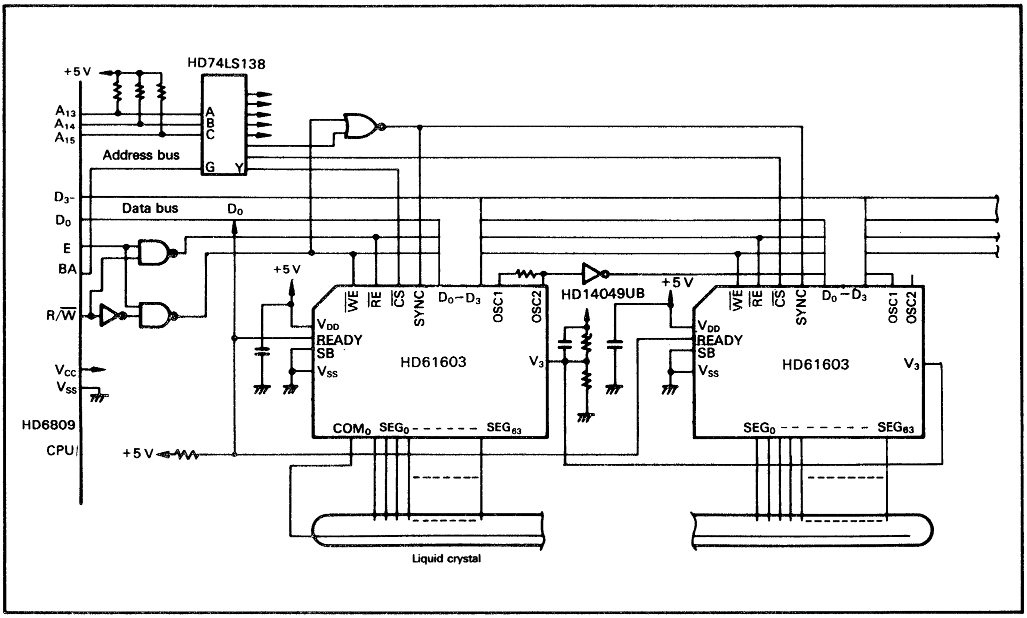


Figure 24. Example (2)

HD61604/HD61605
(Segment Type LCD Driver)

Description

The HD61604 and the HD61605 are liquid crystal display driver LSIs with TTL and CMOS compatible interface. Each of the LSIs can be connected to various microcomputers such as the HMCS6800 series.

Several types of liquid crystal displays can be connected to the HD61604 according to the applications because of the software-controlled liquid crystal dispay drive method.

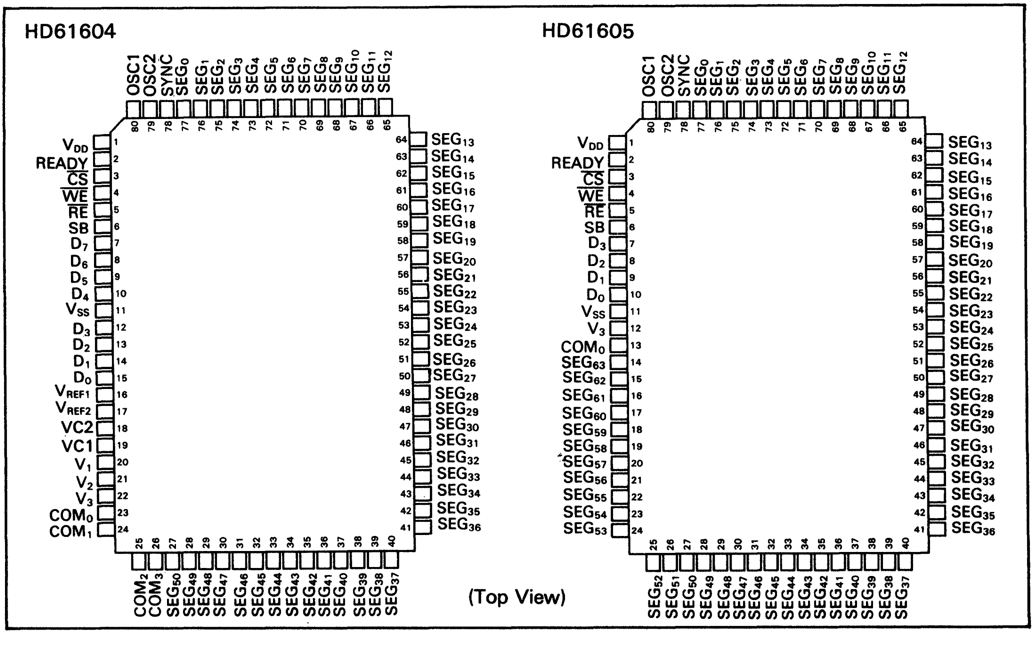
The HD61605 is a liquid crystal display driver LSI only for static drive and has 64 segment outputs that can display 8 digits per chip.

Features

- Low current consumption
  - —Can drive from a battery power supply (100 μA max on 5 V).
  - —Standby input enables a standby operation at lower current consumption (5 μA max on 5 V).
- Versatile segment drive capacity

Type No.	Drive Method		Display Segments	Example of Use	Frame Freq (Hz) at fosc=100 kHz
HD61604	Static		51	8 segments × 6 digits + 3 marks	98
	1/2 bias	1/2 duty	102	8 segments × 12 digits + 6 marks	195
	1/3 bias	1/3 duty	153	9 segments × 17 digits	521
		1/4 duty	204	8 segments × 25 digits + 4 marks	781
HD61605	Static		64	8 segments × 8 digits	98

Pin Arrangement



Block Diagram

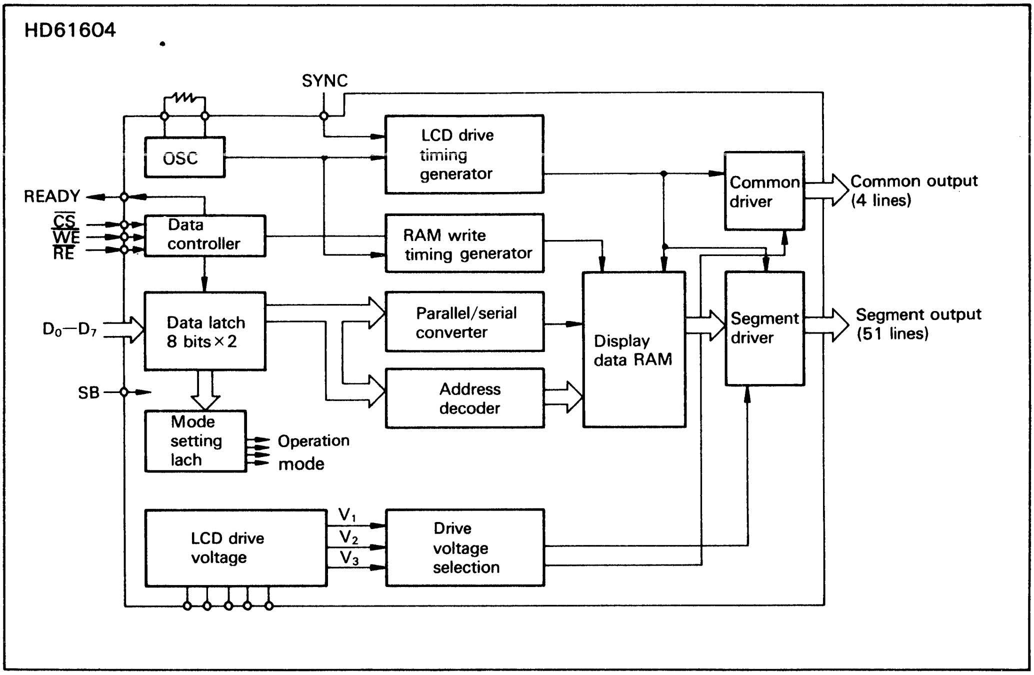


Figure 1. HD61604 Block Diagram

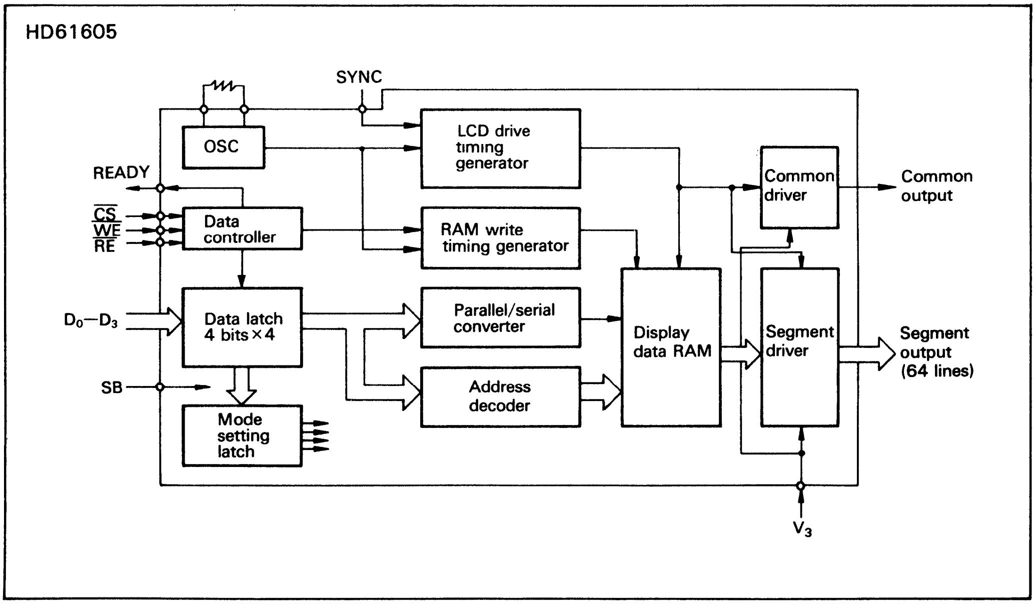


Figure 2. HD61605 Block Diagram

Pin Functions

Table 1 shows the HD61604 pin description. Table 2 shows the HD61605 pin description.

HD61604 Pin Function

READY (Ready): During setting data in the display data RAM and mode setting latch in the LSI after data transfer, low is output to the READY pin to inhibit the next data input.

There are two types of modes: one in which low is output only when both of $\overline{\text{CS}}$ and $\overline{\text{RE}}$ are low, and the other in which low is output regardless of $\overline{\text{CS}}$ and $\overline{\text{RE}}$.

$\overline{\text{CS}}$ (Chip Select): Chip select input. Data can be written only when this pin is low.

$\overline{\text{WE}}$ (Write Enable): Write enable input. Input data of D_0 to D_7 is latched at the positive edge of $\overline{\text{WE}}$.

$\overline{\text{RE}}$ (Reset): Resets the input data byte counter. After both of $\overline{\text{CS}}$ and $\overline{\text{RE}}$ are low, the first data is recognized as the 1st byte data.

SB (Standby): High level input stops the LSI operations.

(i) Stops oscillation and clock input.
(ii) Stops LCD driver.
(iii) Stops writing data into display RAM.

D_0-D_7 (Data Bus): Data input pin from which 8-bit × 2-byte data is input.

SYNC (Synchronous): Synchronous input for 2 or more chips application. LCD drive timing generator is reset by high input. LCD is off.

COM_0-COM_3 (Common): LCD common (backplate) drive output.

SEG_0-SEG_{50} (Segment): LCD segment drive output.

V_1, V_2, V_3 (LCD Voltage): Power supply for LCD drive.

OSC1, OSC2 (Oscillator): Attaches external R to these pins for oscillation. An external clock (100 kHz) can be input from OSC1.

V_{C1}, V_{C2}: Do not connect any wire.

V_{REF1}: Connect this pin to V1 pin.

V_{REF2}: Hold V_{DD} level.

V_{DD}: Positive power supply.

V_{SS}: Negative power supply.

HD61605 Pin Function

READY (Ready): During setting data in the display data RAM and mode setting latch in the LSI after data transfer, low is output to the READY pin to inhibit the next data input.

There are two types of modes: one in which low is output only when both of $\overline{\text{CS}}$ and $\overline{\text{RE}}$ are low, and the other in which low is output regardless of $\overline{\text{CS}}$ and $\overline{\text{RE}}$.

$\overline{\text{CS}}$ (Chip Select): Chip select input. Data can be written only when this pin is low.

$\overline{\text{WE}}$ (Write Enable): Write enable input. Input data of D_0 to D_3 is latched at the positive edge of $\overline{\text{WE}}$.

$\overline{\text{RE}}$ (Reset): Resets the input data byte counter. After both of $\overline{\text{CS}}$ and $\overline{\text{RE}}$ are low, the first data is recognized as the first byte data.

SB (Standby): High level input stops the LSI operations.

(i) Stops oscillation and clock input.
(ii) Stops LCD driver.
(iii) Stops writing data into display RAM.

D_0-D_3: Data input pin from which 4-bit × 4 -byte data is input.

SYNC (Synchronous): Synchronous input for 2 or more chips application. LCD drive timing generator is reset by high input. LCD is off.

COM_0 (Common): LCD common (backplate) drive output.

SEG_0-SEG_{63} (Segment): LCD segment drive output.

OSC1, OSC2 (Oscillator): Attaches external R to these pins for oscillation. An external clock (100 kHz) can be input from OSC1.

V_3 (LCD Voltage): Power supply input for LCD drive.

Voltage between V_{DD} and V_3 is used as drive voltage.

V_{SS}: Negative power supply.

V_{DD}: Positive power supply.

Table 1. HD61604 Pin Description

Pin Name	No.of Lines	Input/Output	Connected to
READY	1	NMOS open drain output	MCU
$\overline{CS}$	1	Input	MCU
$\overline{WE}$	1	Input	MCU
$\overline{RE}$	1	Input	MCU
SB	1	Input	MCU
$D_0 - D_7$	8	Input	MCU
SYNC	1	Input	MCU
$COM_0 -$ COM_3	4	Output	LCD
$SEG_0 -$ SEG_{50}	51	Output	LCD
V_1, V_2, V_3	3	Power supply	External R
OSC1, OSC2	2	Input, output	External R
V_{C1}, V_{C2}	2	Output	
V_{REF1}	1	Input	V_1
V_{REF2}	1	Input	V_{DD}
V_{DD}	1	Power supply	
V_{SS}	1	Power supply	

Note: Logic polarity is positive.
1 = high = active.

Table 2. HD61605 Pin Description

Pin Name	No.of Lines	Input/Output	Connected to
READY	1	NMOS open drain output	MCU
$\overline{CS}$	1	Input	MCU
$\overline{WE}$	1	Input	MCU
$\overline{RE}$	1	Input	MCU
SB	1	Input	MCU
$D_0 - D_3$	4	Input	MCU
SYNC	1	Input	MCU
COM_{01}	Output	LCD	
$SEG_0 -$ SEG_{63}	64	Output	LCD
OSC1, OSC2	2	Input, output	External R
V_3	1	Input	Power supply
V_{SS}	1	Power supply	
V_{DD}	1	Power supply	

Note: Logic polarity is positive.
1 = high = active.

Display RAM

HD61604 Display RAM

The HD61604 has an internal display RAM shown in figure 3. Display data is stored in the RAM, or is read according to the LCD drive timing to display on the LCD. One bit of the RAM corresponds to the 1 segment of LCD. Note that some bits of the RAM cannot be displayed depending on LCD drive modes.

Reading Data from HD61604 Display RAM

A display RAM segment address corresponds to a segment output. The data at segment address SEGn is output to segment output SEGn pin.

A common address corresponds to the output timings of a common output and a segment output. The same common address data is simultaneously read. The data of display RAM is reproduced on the LCD panel.

The following shows the correspondence between the 7-segment type LCD connection and the display RAM in each mode.

(1) **Static Drive:** In the static drive, only the column of COM_0 of display RAM is output. COM_1 to COM_3 are not displayed (figure 4).

(2) **1/2 Duty Drive:** In the 1/2 duty drive, the columns of COM_0 and COM_1 of display RAM are output in time sharing. The columns of COM_2 and COM_3 are not displayed (figure 5).

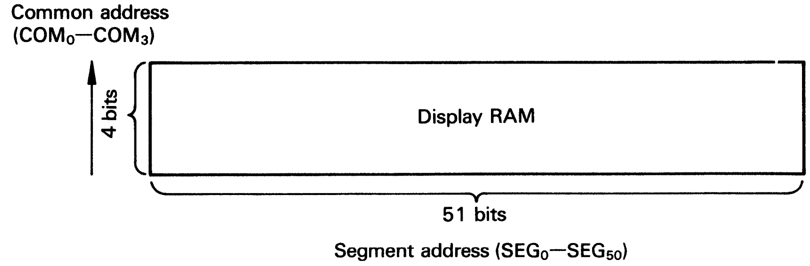
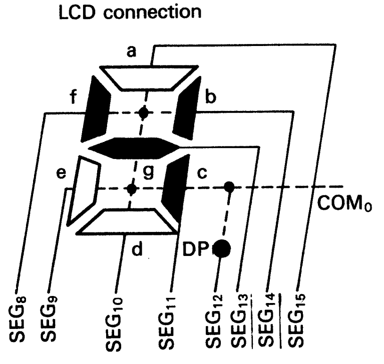


Figure 3. Display RAM (HD61604)



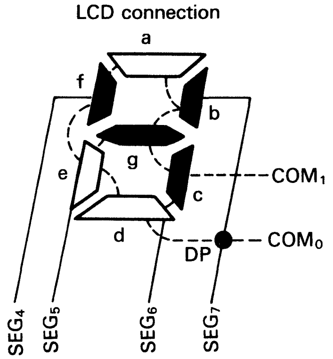
Display RAM

COM_3								
COM_2								
COM_1								
COM_0	f	e	d	c	DP	g	b	a
	SEG_8	SEG_9	SEG_{10}	SEG_{11}	SEG_{12}	SEG_{13}	SEG_{14}	SEG_{15}

Figure 4. Example of Correspondence between LCD Connection and Display RAM (Static Drive, HD61604)

(3) **1/3 Duty Drive:** In the 1/3 duty drive, the columns of COM_0 to COM_2 are output in time sharing. No column of COM_3 is displayed. "y" cannot be rewritten by display data (input on an 8-segment basis). Please use bit manipulation in turning on/off the display of "y"(figure 6).

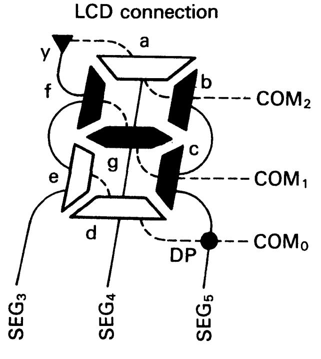
(4) **1/4 Duty Drive:** In the 1/4 duty drive, all the columns of COM_0 to COM_3 are displayed (figure 7).



Display RAM

COM_3	/	/	/	/
COM_2	/	/	/	/
COM_1	a	g	c	b
COM_0	f	e	d	DP
	SEG_4	SEG_5	SEG_6	SEG_7

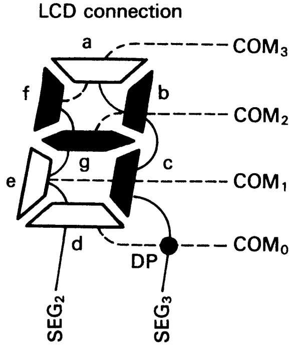
Figure 5. Example of Correspondence between LCD Connection and Display RAM (1/2 Duty, HD61604)



Display RAM

COM_3	/	/	/
COM_2	y	a	b
COM_1	f	g	c
COM_0	e	d	DP
	SEG_3	SEG_4	SEG_5

Figure 6. Example of Correspondence between LCD Connection and Display RAM (1/3 Duty, HD61604)



Display RAM

COM_3	f	a
COM_2	g	b
COM_1	e	c
COM_0	d	DP
	SEG_2	SEG_3

Figure 7. Example of Correspondence between LCD Connection and Display RAM (1/4 Duty, HD61604)

Writing Data into HD61604 Display RAM

Data is written into the display RAM in the following five methods:

(1) **Bit Manipulation:** Data is written into any bit of RAM on a bit basis.

(2) **Static Display Mode:** 8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.

(3) **1/2 Duty Display Mode:** 8-bit data is written on a digit basis according to the 7 -segment type LCD pattern of 1/2 duty drive.

(4) **1/3 Duty Display Mode:** 8-bit data is written on a digit basis according to the 7 -segment type LCD pattern of 1/3 duty drive.

(5) **1/4 Duty Display Mode:** 8-bit data is written on a digit basis according to the 7 -segment type LCD pattern of 1/4 duty drive.

The RAM area and the allocation of the segment data for 1-digit display depend on the drive methods as described in the section of "Reading Data from Display RAM".

8-bit data is written on a digit basis corresponding to the above duty drive methods. The digits are allocated as shown in figure 8.

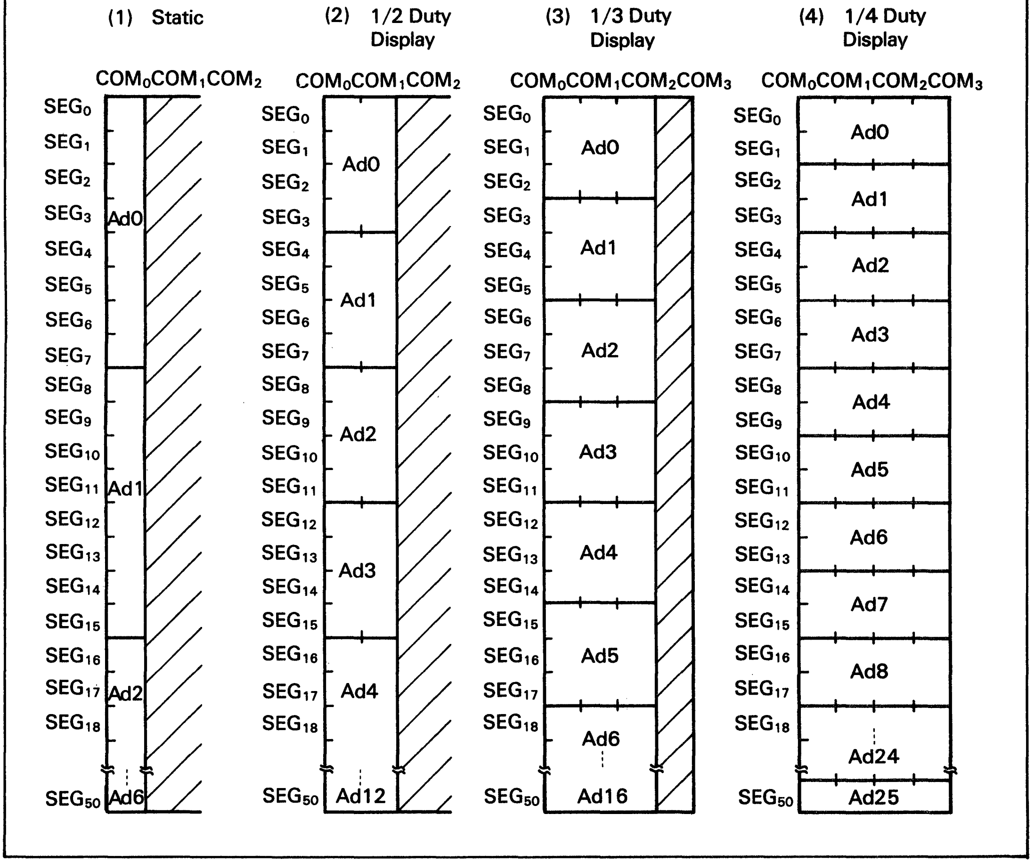


Figure 8. Allocation of Digit (HD61604)

As the data can be transferred on a digit basis from a microcomputer, transfer efficiency is improved by allocating the LCD pattern according to the allocation of each bit data of the digit in the data RAM.

Figure 8 shows the digit address (displayed as Adn) to specify the store address of the transferred 8-bit data on a digit basis.

Figure 9 shows the correspondence between each segment in an Adn and the 8-bit input data.

When data is transferred on a digit basis, 8-bit display data and digit address should be specified as described above.

However, when the digit address is Ad6 of static, Ad12 of 1/2 duty, or Ad25 of 1/4 duty, display RAM does not have enough bits for the data. Thus the extra bits of the input 8-bit data are ignored.

In the bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data, a segment address (6 bits) and a common address (2 bits) should be specified.

HD61605 Display RAM

The HD61605 has an internal display RAM as shown in figure 10. Display data is stored in the RAM and output to the segment output pin.

(1) Static Display

	COM$_0$
SEG$_8$	Bit 7
SEG$_{8n+1}$	6
SEG$_{8n+2}$	5
SEG$_{8n+3}$	4
SEG$_{8n+4}$	3
SEG$_{8n+5}$	2
SEG$_{8n+6}$	1
SEG$_{8n+7}$	Bit 0

(2) 1/2 Duty Display

	COM$_0$	COM$_1$
SEG$_{4n}$	Bit 7	6
SEG$_{4n+1}$	5	4
SEG$_{4n+2}$	3	2
SEG$_{4n+3}$	1	Bit 0

(3) 1/3 Duty Display

	COM$_0$	COM$_1$	COM$_2$
SEG$_{3n}$	Bit 7	6	
SEG$_{3n+1}$	5	4	3
SEG$_{3n+2}$	2	1	Bit 0

(4) 1/4 Duty Display

	COM$_0$	COM$_1$	COM$_2$	COM$_3$
SEG$_{2n}$	Bit 7	6	5	4
SEG$_{2n+1}$	3	2	1	Bit 0

Figure 9. Bit Assignment in an Adn (HD61604)

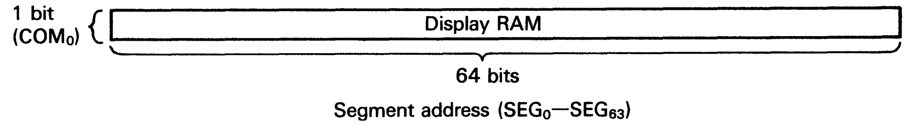


Figure 10. Display RAM (HD61605)

Reading Data from HD61605 Display RAM

Each bit of the display RAM corresponds to each LCD segment. The data at segment address SEGn is output to segment output SEGn pin. Figure 11 shows the correspondence between the 7-segment type LCD connection and the display RAM .

Writing Data into HD61605 Display RAM

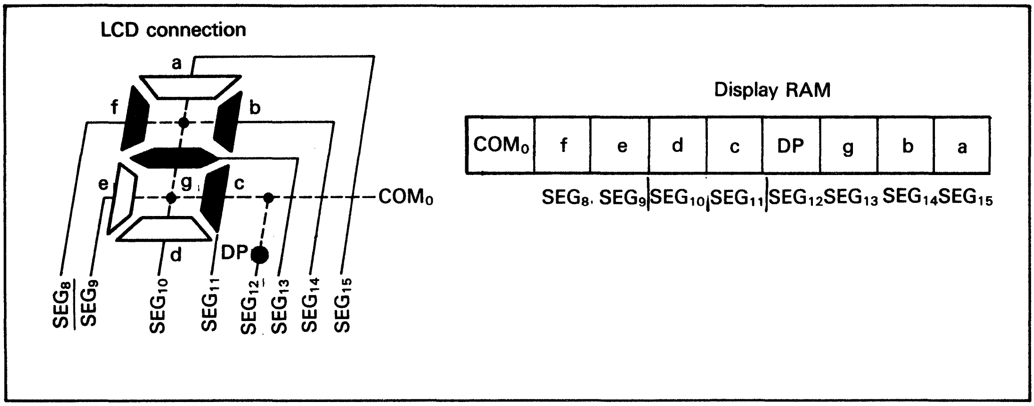
Data is written into the display RAM in the following two methods:

(1) **Bit Manipulation:** Data is written into any bit of RAM on a bit basis.

(2) **Static Display Mode:** 8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.

The 8-bit data is written on a digit basis into the digit address (displayed as Adn) shown in figure 12. When data is transferred from a microcomputer, four 4-bit data are needed to specify the digit address and an 8-bit display data. Figure 13 shows the correspondence between each segment in an Adn and the transferred 8-bit data.

In the bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data and a segment address (6 bits) should be specified.



COM$_0$	f	e	d	c	DP	g	b	a
	SEG$_8$	SEG$_9$	SEG$_{10}$	SEG$_{11}$	SEG$_{12}$	SEG$_{13}$	SEG$_{14}$	SEG$_{15}$

Figure 11. Example of Correspondence between LCD Connection and Display RAM (HD61605)

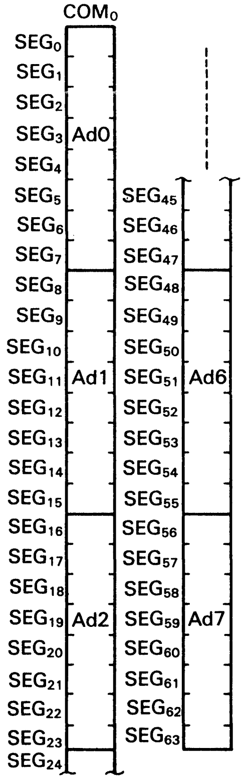


Figure 12. Allocation of Digit (HD61605)

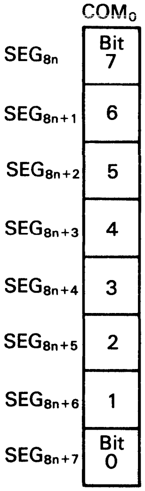


Figure 13. Bit Assignment in an Adn (HD 61605)

Operating Modes

HD61604 Operating Modes

The HD61604 has the following operating modes:

(1) **LCD Drive Mode:** Determines the LCD drive method.

- Static drive mode: LCD is driven statically.
- 1/2 duty drive mode: LCD is driven with 1/2 duty and 1/2 bias.
- 1/3 duty drive mode: LCD is driven with 1/3 duty and 1/3 bias.
- 1/4 duty drive mode: LCD is driven with 1/4 duty and 1/3 bias.

(2) **Data Display Mode:** Determines how to write display data into the data RAM.

- Static display mode: 8-bit data is written into the display RAM according to the digit in the static drive.
- 1/2 duty display mode: 8-bit data is written into the display RAM according to the digit in the 1/2 duty drive.
- 1/3 duty display mode: 8-bit data is written into the display RAM according to the digit in the 1/3 duty drive.
- 1/4 duty display mode: 8-bit data is written into the display RAM according to the digit in the 1/4 duty display drive.

(3) **READY Output Mode:** Determines the READY output timing.

After data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when READY is output can be selected from the following two modes:

- READY is always available (figure 14).
- READY is available by $\overline{\text{CS}}$ and $\overline{\text{RE}}$ (figure 15).

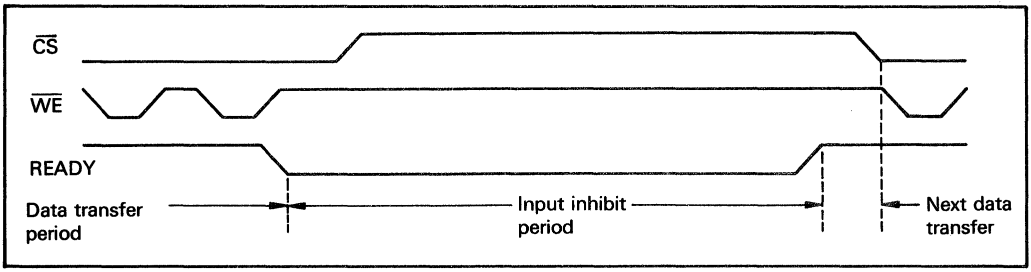


Figure 14. READY Output Timing (When It is Always Available)

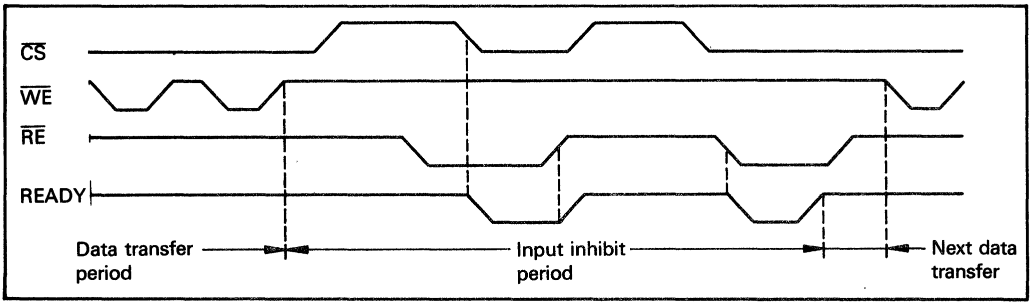


Figure 15. READY Output Timing (When It is Available by $\overline{\text{CS}}$ and $\overline{\text{RE}}$)

(4) **LCD Off Mode:** In this mode, the HD61604 stops driving LCD and turns it off.

The above 4 modes are specified by mode setting data. The modes are independent of each other and can be used in any combination. The bit manipulation is independent of data display mode and can be used regardless of it.

HD61605 Operating Modes

The HD61605 has the following operating modes:

(1) **READY Output Mode:** Determines the READY output timing.

After data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when READY is output can be selected from the following two modes:

- READY is always available (figure 16).
- READY is available by $\overline{CS}$ and $\overline{RE}$ (figure 17).

(2) **LCD Off Mode:** In this mode, the HD61605 stops driving LCD and turns it off.

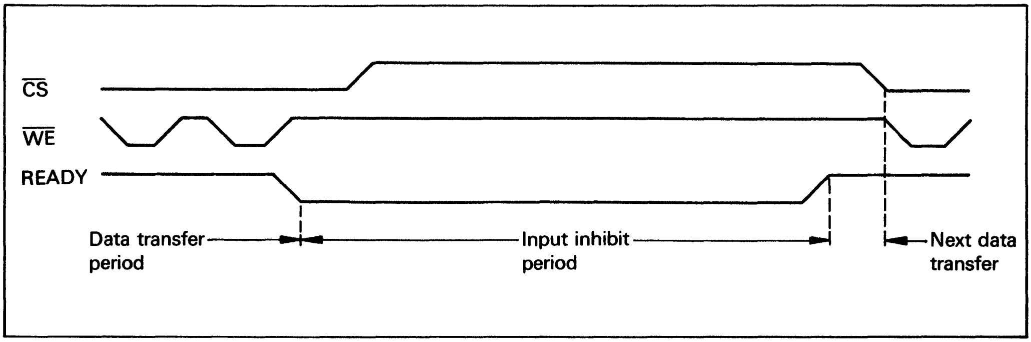


Figure 16. READY Output Timing (When It is Always Available)

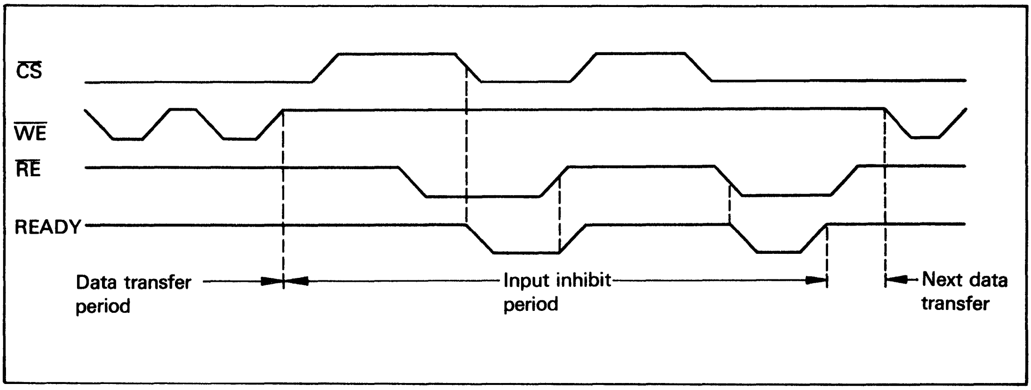


Figure 17. READY Output Timing (When It is Available by $\overline{CS}$ and $\overline{RE}$.)

Input Data Formats

HD61604 Input Data Formats

Input data is composed of 8 bits × 2 bytes. Input them as 2-byte data after READY output changes from low to high or low pulse enters into $\overline{RE}$ pin.

(1) **Display Data:** Updates display on an 8-segment basis.

1st byte

0	0	×	Display address (Digit address Adn)				
7	6	5	4	3	2	1	0

2nd byte

Display data							
7	6	5	4	3	2	1	0

- Display address: Digit address Adn in accordance with each display mode
- Display data: Pattern data written into the display RAM according to each display mode and the address

(2) **Bit Manipulation Data:** Updates display on a segment basis.

1st byte

0	1	Display data	×	×	×	COM address	
7	6	5	4	3	2	1	0

2nd byte

×	×	SEG address					
7	6	5	4	3	2	1	0

- Display data: Data written into 1 bit of the specified display RAM
- COM address: Common address of display RAM
- SEG address: Segment address of display RAM

(3) **Mode Setting Data:**

1st byte

1	0	×	0	1	READY bit	Drive mode bits	
7	6	5	4	3	2	1	0

2nd byte

×	×	×	×	×	OFF/ON bit	Display mode bits	
7	6	5	4	3	2	1	0

- Display mode bits:
  00: Static display mode
  01: 1/2 duty display mode
  10: 1/3 duty display mode
  11: 1/4 duty display mode
- OFF/ON bit:
  1: LCD off (It is set to 1 when SYNC is entered.)
  0: LCD on
- Drive mode bits:
  00: Static drive
  01: 1/2 duty drive
  10: 1/3 duty drive
  11: 1/4 duty drive
- READY bit:
  0: READY outputs 0 only while $\overline{CS}$ and $\overline{RE}$ are 0. (It is reset to 0 when SYNC is entered.) ···READY bus mode
  1: READY outputs 0 regardless of $\overline{CS}$ and $\overline{RE}$. ···READY port mode

Note: Input the same data to display mode bits and drive mode bits.

(4) **1-Byte Instruction:** The first data (first byte) is ignored when the bit 6 and bit 7 in the data are 1.

1st byte

1	1	×	×	×	×	×	×
7	6	5	4	3	2	1	0

HD61605 Input Data Formats

Input data is composed of 4 bits × 4 bytes. Input them as four 4-bit data after READY output changes from low to high or low pulse enters into $\overline{RE}$ pin.

(1) **Display Data:** Updates display on an 8-segment basis.

1st byte

3	2	1	0
0	0	×	×

2nd byte

3	2	1	0
×	Display address (Digit address Adn)		

3rd byte

3	2	1	0
Display data			
Bit7	6	5	4

4th byte

3	2	1	0
Display data			
Bit3	2	1	0

- Display address: Digit address Adn shown in figure 12.
- Display data: Pattern data written into the display RAM as shown in figure 13.

(2) **Bit Manipulation Data:** Updates display on a segment basis.

1st byte

3	2	1	0
0	1	Display data	×

2nd byte

3	2	1	0
×	×	0	0

3rd byte

3	2	1	0
×	×	SEGaddress	
		Bit5	4

4th byte

3	2	1	0
SEG address			
Bit3	2	1	0

- Display data: Data written into the 1 bit of the specified display RAM.
- SEG address: Segment address of display RAM (segment output).

(3) **Mode Setting Data:**

1st byte

3	2	1	0
1	0	×	0

2nd byte

3	2	1	0
×	READY bit	×	×

3rd byte

3	2	1	0
×	×	×	×

4th byte

3	2	1	0
×	OFF/ON bit	0	0

- OFF/ON bit:
  1: LCD off (It is set to 1 when SYNC is entered.)
  0: LCD on
- READY bit:
  0: READY outputs 0 only while $\overline{CS}$ and $\overline{RE}$ are 0. (It is reset to 0 when SYNC is entered). ···READY bus mode
  1: READY outputs 0 regardless of $\overline{CS}$ and $\overline{RE}$. ···READY port mode

(4) **1-Byte Instruction:** The first data (4 bits) is ignored when the bit 3 and bit 2 in the data are 1.

1st byte

3	2	1	0
1	1	×	×

HITACHI

How to Input Data

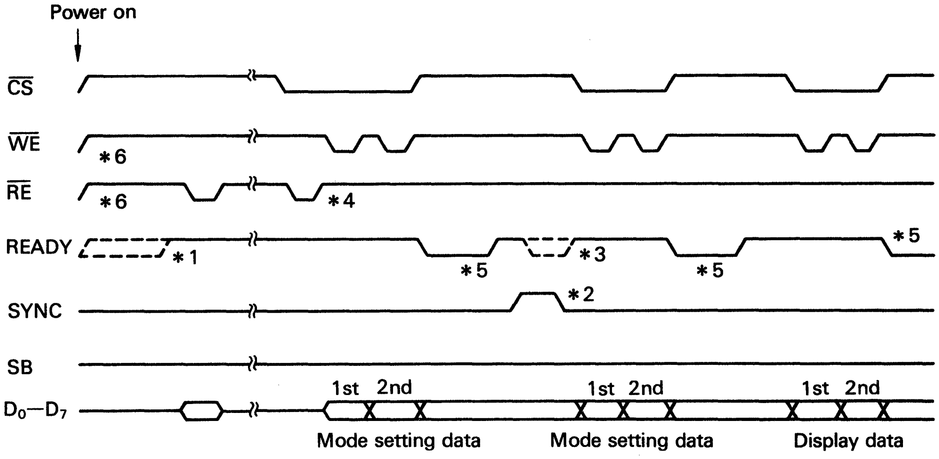
How to Input Data into HD61604

Input data is composed of 8 bits × 2 bytes. Take care that the data transfer is not interrupted because the first 8-bit data is distinguished from the second one depending on the sequence only.

When data transfer is interrupted, or at the power on, the following two methods can be used to reset the count of the number of bytes (count of the first and second bytes):

(1) Set $\overline{CS}$ and $\overline{RE}$ to low (no display data changes).
(2) Input 2 or more 1-byte instruction data whose bit 7 and 6 are high (display data may change).

The data input method via data input pins ($\overline{CS}$, $\overline{WE}$, D_0 to D_7) is similar to that of static RAM such as HM6116. An access of the LSI can be made through the same bus line as ROM and RAM. When output ports of a microcomputer are used for an access, refer to the timing specifications and figure 18.



*1: READY output is indefinite during 12 clocks after the oscillation starts when power on (clock: OSC2 clock).
*2: High pulse should be applied to SYNC pin when using two or more chips simultaneously.
*3: In the mode in which READY is always available, READY output is indefinite while high is being appliad to SYNC.
*4: Reset the byte counter after power on.
*5: READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.
*6: Connect a proper pull-up resistor if $\overline{WE}$ or $\overline{RE}$ is floating.
*7: It is not always necessary to follow this example.

Figure 18. Example of Data Transfer Sequence

How to Input Data into HD61605

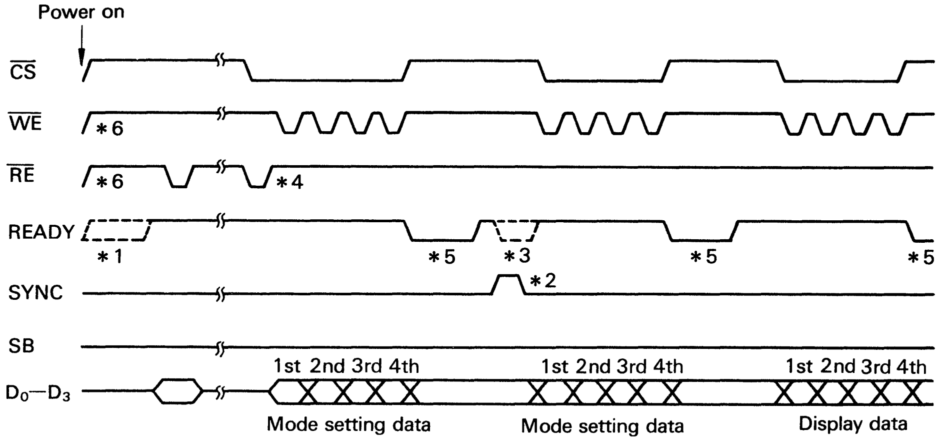
Input data is composed of 4 bits × 4 bytes. Take care that the data transfer is not interrupted because the first 4-bit data to the fourth 4-bit data are distinguished from each other depending on the sequence only.

When data transfer is interrupted, or at the power on, the following two methods can be used to reset the count of the number of data (count of the first 4-bit data to the fourth 4-bit data):

(1) Set $\overline{CS}$ and $\overline{RE}$ to low (no display data changes.)

(2) Input 4 or more 1-byte instruction data (4-bit data) whose bit 3 and 2 are high (display data may change).

The data input method via data input pins ($\overline{CS}$, $\overline{WE}$ D_0 to D_3) is similar to that of static RAM such as HM6116. An access of the LSI can be made through the same bus line as ROM and RAM. When output ports of a microcomputer are used for an access, refer to the timing specifications and figure 19.



*1: READY output is indefinite during 12 clocks after the oscillation starts when power on (clock: OSC2 clock).

*2: High pulse should be applied to SYNC pin when using two or more chips simultaneously.

*3: In the mode in which READY is always available, READY output is indefinite while high is being applied to SYNC.

*4: Reset the 4-bit data counter after power on.

*5: READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.

*6: Connect a proper pull-up resistor if $\overline{WE}$ or $\overline{RE}$ is floating.

*7: It is not always necessary to follow this example.

Figure 19. Example of Data Transfer Sequence

Notes on READY Output

Note that the READY output will be unsettled during 1.5 clocks (max) after inputting the first 2-byte data for setting the mode after turning the power on. This is because the READY bit data of mode setting latches and the mode of READY pin (READY bus or port mode) are unsettled untill the completion of mode setting.

There are two kinds of the READY output waveforms depending on the modes.

(1) READY bus mode (READY bit = 0)

(2) READY port mode (READY bit = 1)

However, if you input SYNC before mode setting, waveform will be determined; when you choose READY bus mode, (1) a will be output, and when you choose READY port mode, (2) a will be output. The figures can be applied both to HD61604 and HD61605.

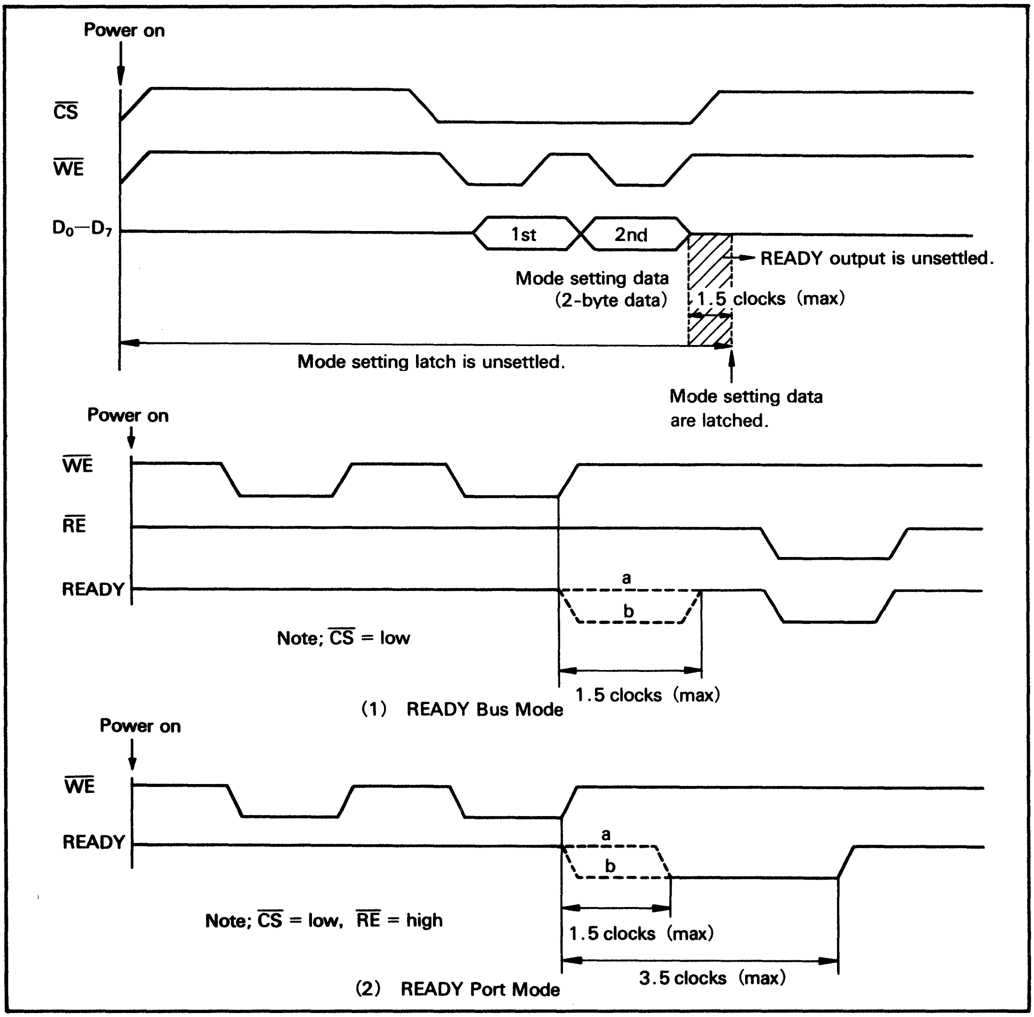


Figure 20. READY Output According to Modes

Standby Operation

Standby operation with low power consumption can be activated when pin SB is used. Normal operation of the LSI is activated when pin SB is low level, and the LSI goes into the standby state when pin SB is high level. The standby state of the LSI is as follows:

(a) LCD driver is stopped (LCD is off).
(b) Display data and operating mode are held.
(c) The operation is suspended while changing display (= while READY is outputting low.) In this case, READY outputs high within 10.5 clocks or 3.5 clocks after release from the standby mode.
(d) Oscillation is stopped.

When this mode is not used, connect pin SB to V_{SS}.

Multi-Chip Operation

When an LCD is driven with two or more chips, the driving timing of LCD must be synchronized. In this case, the chips are synchronized with each other by using SYNC input. If SYNC input is high, the LCD driver timing circuit is reset. Apply high pulse to the SYNC input after the operating mode is set.

A high pulse to the SYNC input causes the change of the mode setting data (The OFF/ON bit is set and the READY bit is reset. See (3) Mode Setting Data in "Input Data Formats".) Transfer the mode setting data into the LSI after every SYNC operation.

If a power on reset signal is applied to the SYNC pin, the LCD can be off-state when the power is turned on.

When SYNC input is not used, connect pin SYNC to V_{SS}.

In the case SB input is used, after standby mode is released, high pulse must be applied to the SYNC input, and mode setting data must be set again.

Restriction on Usage

Minimize the noise by inserting a noise by-pass capacitor ($\geqq 1\ \mu F$) between V_{DD} and V_{SS} pins. (Insert one as near chip as possible.)

Liquid Crystal Display Drive Voltage Circuit (HD61604)

What is LCD Voltage?

HD61604 drives liquid crystal display using four levels of voltages; V_{DD}, V_1, V_2, and V_3 (V_{DD} is the highest and V_3 is the lowest). The voltage between V_{DD} and V_3 is called V_{LCD} and it is necessary to apply the appropriate V_{LCD} according to liquid crystal displays. V_3 always needs to be supplied power regardless of the display duty ratio since it supplies the voltage to the LCD drive circuit of HD61604.

Connecting R2−R5 in series between V_{DD} and V_{SS} generates ΔV or V_{LCD} by using this resistance ratio to supply these voltage to pins V_1, V_2, V_3. C2−C4 are the capacitors for smoothing. Connect a trimmer potentiometer for R5 and change its resistance value to control the contrast.

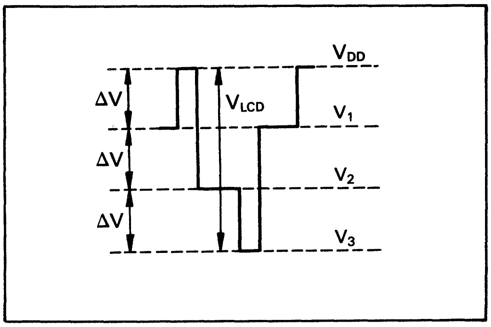
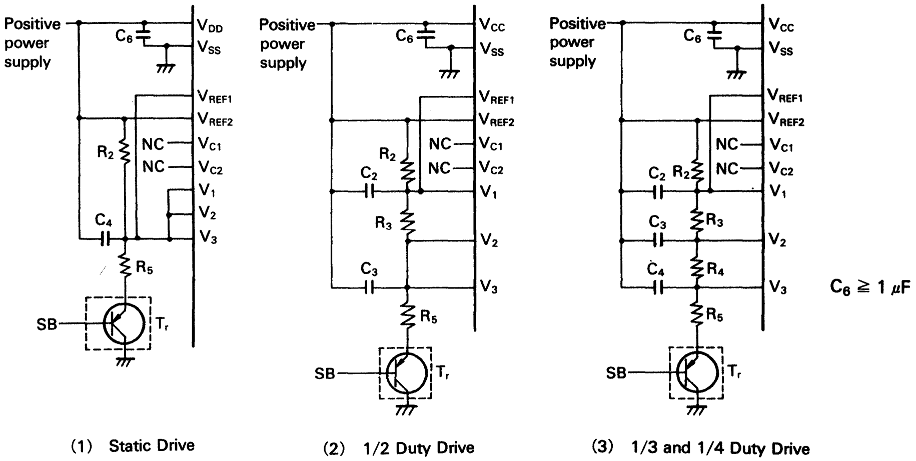


Figure 21. LCD Output Waveform and Output Levels (1/3 Duty, 1/3 Bias)



Note: 1 When standby mode is used, a transistor is required.
2 R2−R5 should be some kΩ−some tens of kΩ, and C2−C4 should be 0.1 μF−0.3 μF.

Figure 22. Example when External Drive Voltage is Used

Liquid Crystal Display Drive Voltage (HD61605)

As shown in figure 23, apply LCD drive voltage from the external power supply.

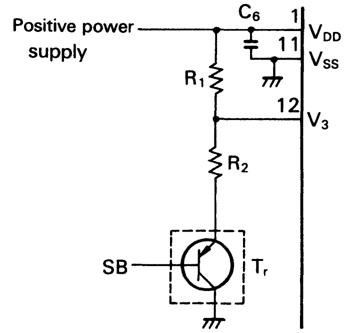
Oscillation Circuit

When Internal Oscillation Circuit is Used

When the internal oscillation circuit is used, attach an external resistor R_{OSC} as shown in figure 24. (Insert R_{OSC} as near chip as possible, and make the OSC1 side shorter.)

When External Clock is Used

When an external clock of 100 kHz with CMOS level is provided, pin OSC1 can be used for the input pin. In this case, open pin OSC2.



$C_6 \geqq 1\ \mu F$

Note: When standby mode is used, a transistor is required.

Figure 23. Example of Drive Voltage Generator

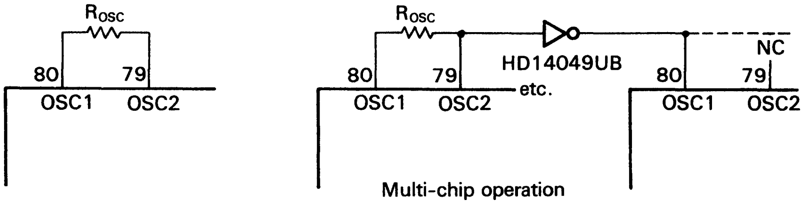


Figure 24. Example of Oscillation Circuit

Applications

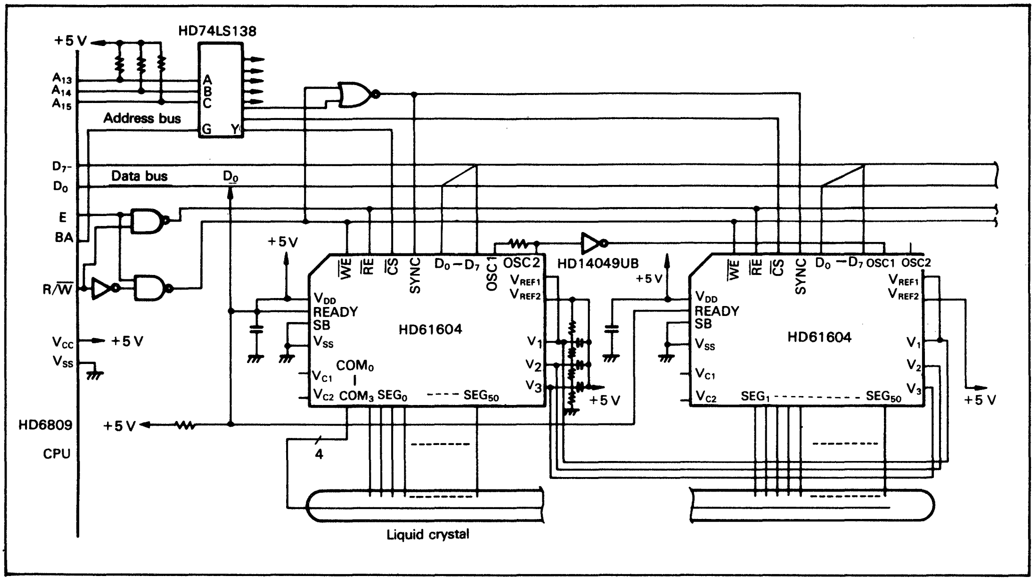


Figure 25. Example (1)

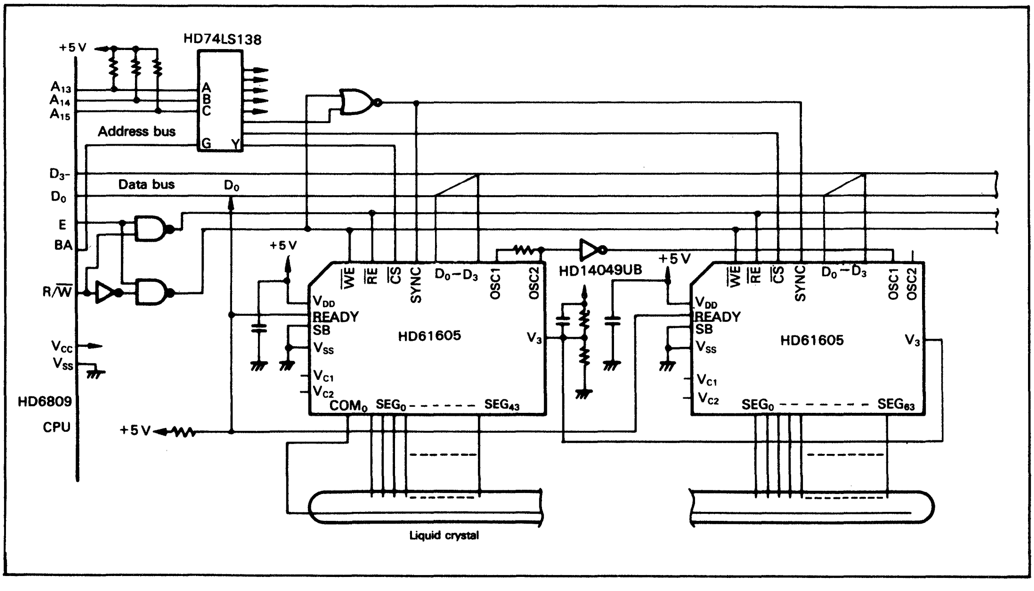


Figure 26. Example (2)

Absolute Maximum Ratings

Item	Symbol	Limit	Unit
Power supply voltage*	V_{DD}, V_1, V_2, V_3	−0.3 to + 7.0	V
Pin voltage *	V_T	−0.3 to V_{DD} + 0.3	V
Operating temperature	Topr	−20 to +75	°C
Storage temperature	Tstg	−55 to +125	°C

*Value referred to V_{SS}=0 V.

Note: If LSIs are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristics limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.

Recommended Operating Conditions

		Limit			
Item	Symbol	Min	Typ	Max	Unit
Power supply voltage*	V_{DD}	4.5	–	5.5	V
	V_1, V_2, V_3	0.3	–	V_{DD}	V
Pin voltage*	V_T	0	–	V_{DD}	V
Operating temperature	Topr	−20	–	+75	°C

*Value referred to V_{SS}=0 V.

Electrical Characteristics

DC Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 V to 5.5 V, Ta= −20 °C to +75 °C, unless otherwise noted)

Item		Symbol	Limit			Unit	Test Condition
			Min	Typ	Max		
Input high voltage	OSC1	V_{IH1}	0.8V_{DD}	–	V_{DD}	V	
	Others	V_{IH2}	2.0	–	V_{DD}	V	
Input low voltage	OSC1	V_{IL1}	0	–	0.2V_{DD}	V	
	Others	V_{IL2}	0	–	0.8	V	
Output leakage current	READY	I_{OH}	–	–	5	μA	Pull up the pin to V_{DD}
Output low voltage	READY	V_{OL}	–	–	0.4	V	I_{OL}=0.4 mA
Input leakage current *1	Input pin	I_{IL1}	−1.0		1.0	μA	V_{IN}=0 to V_{DD}
	V_1	I_{IL2}	−20	–	20	μA	V_{IN}=V_{DD} to V_3
	V_2, V_3	I_{IL3}	−5.0	–	5.0	μA	
LCD driver voltage drop	COM_0−COM_3	V_{d1}	–	–	0.3	V	±Id=3 μA for each COM, V_3=V_{DD} to 3 V
	SEG_0−SEG_{50}	V_{d2}	–	–	0.6	V	±Id=3 μA for each SEG, V_3=V_{DD} to 3 V
Current consumption *2		I_{DD}	–	–	100	μA	During display * R_{OSC}=360 kΩ
		I_{DD}	–	–	5	μA	At standby

* Except the transfer operation of display data and bit data.

*1 V_1, V_2: applied only to HD61604.

*2 Do not connect any wire to the output pins and connect the input pins to V_{DD} or V_{SS}.

AC Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 V to 5.5 V, Ta = −20 °C to +75 °C, unless otherwise noted)

Item		Symbol	Limit			Unit	Test Condition
			Min	Typ	Max		
Oscillation frequency	OSC2	f_{OSC}	70	100	130	kHz	R_{OSC}=360 kΩ
External clock frequency	OSC1	f_{OSC}	70	100	130	kHz	
External clock duty	OSC1	Duty	40	50	60	%	
I/O signal timing		t_S	400	–	–	ns	
		t_H	10	–	–	ns	
		t_{WH}	300	–	–	ns	
		t_{WL}	400	–	–	ns	
		t_{WR}	400	–	–	ns	
		t_{DL}	–	–	1.0	µs	Figure 31
		t_{EN}	400	–	–	ns	
		t_{OP1}	9.5	–	10.5	Clock	For display data transfer
		t_{OP2}	2.5	–	3.5	Clock	For bit and mode data transfer
Input signal rise time and fall time		t_r, t_f	–	–	25	ns	

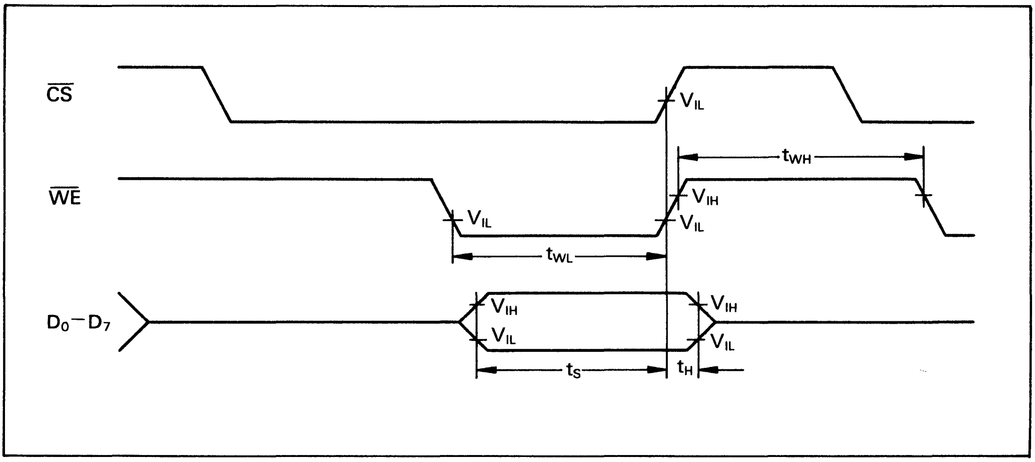


Figure 27. Write Timing ($\overline{RE}$ is fixed high and SYNC low)

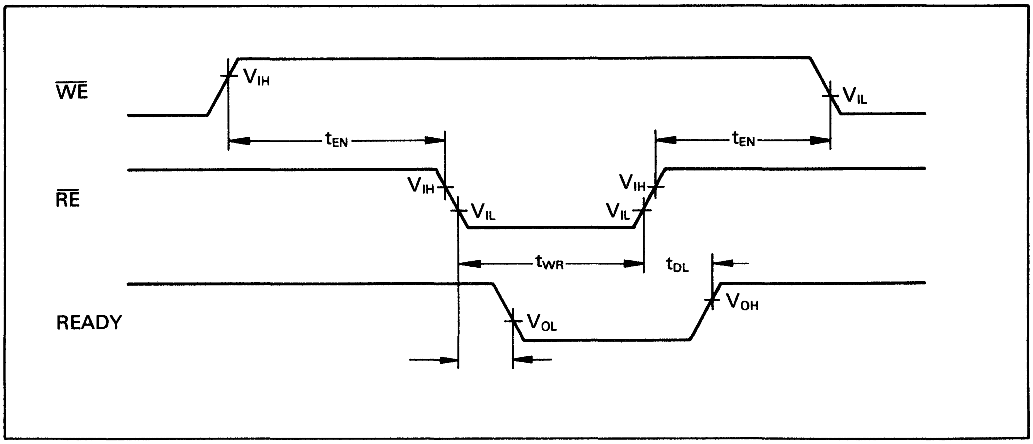


Figure 28. Reset/Read Timing ($\overline{CS}$ and SYNC are fixed low)

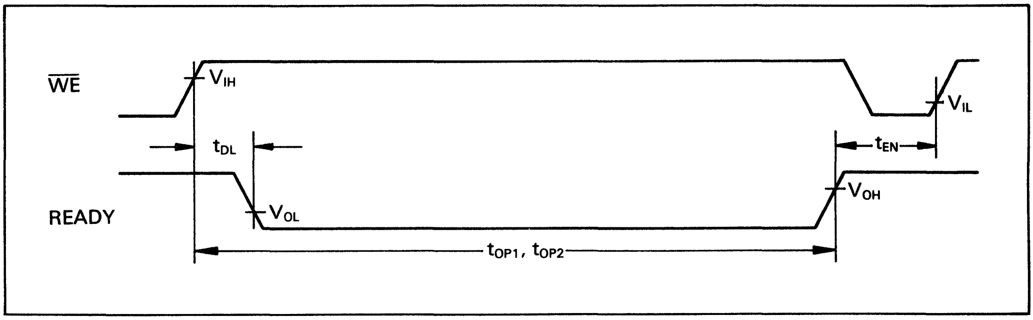


Figure 29. READY Timing (When the READY Output is Always Available)

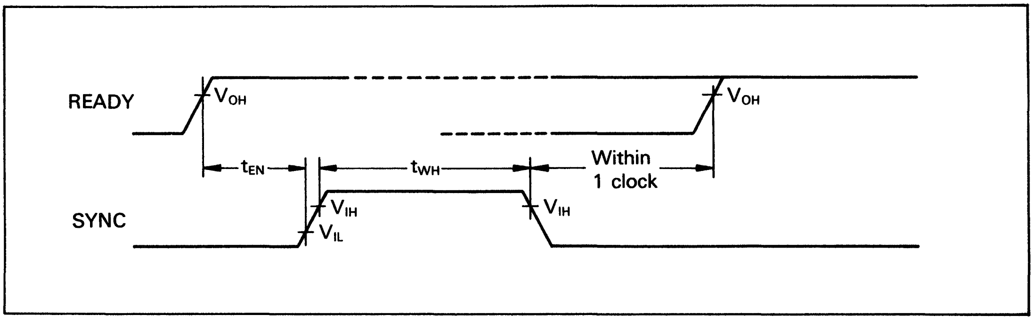


Figure 30. SYNC Timing

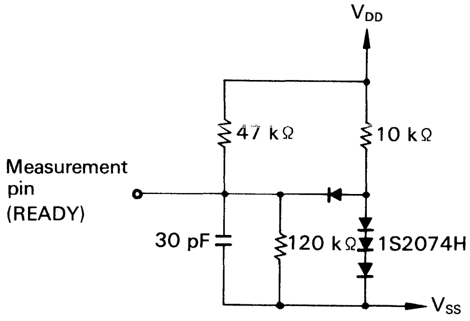


Figure 31. Bus Timing Load Circuit (LS-TTL Load)

Section Two

HD66300T
Horizontal Driver for TFT-Type LCD Color TV

Section Two

HD66300T Horizontal Driver for TFT-Type LCD Color TV

For additional information reference:

Section 1. LCD Controller/Driver LSI Data Book
Section 3. HD66840 Video Interface Controller (LVIC) Application Note
Section 4. HD63645F/HD64645F LCD Timing Controller (LCTC) Application Note
Section 5. HD63645/HD64645/HD64646 LCD Timing Controller (LCTC) User's Manual

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HD66300T

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HD66300T
Horizontal Driver for TFT-Type LCD Color TV

PRELIMINARY

Description

The HD66300T is a horizontal driver used for TFT-type (Thin Film Transistor) LCD color TVs. Specifically, it drives the drain bus signals of a TFT-type LCD panel.

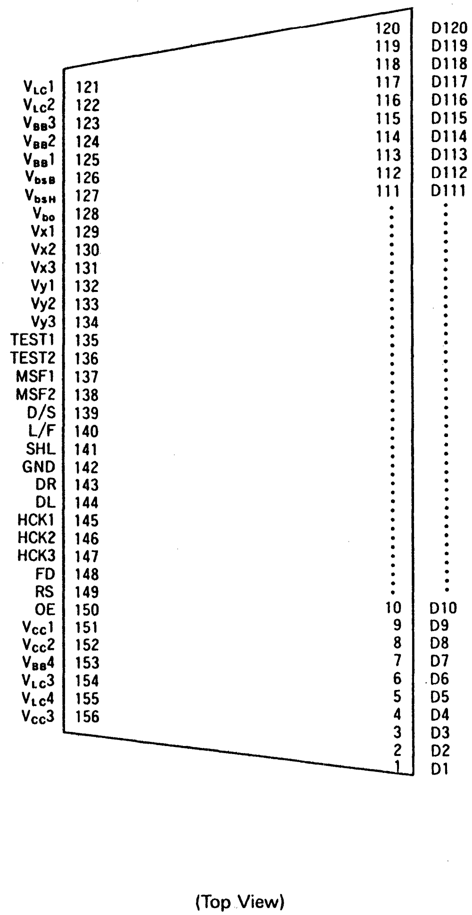
The HD66300T receives as input three video signals R, G, B, and their inverted signals $\overline{R}$, $\overline{G}$ and $\overline{B}$. Internal sample and hold circuitry then samples and holds these signals before outputting them via voltage followers to drive an TFT-type LCD panel.

The HD66300T can drive LCD panels from 480 x 240 pixels middle-resolution up to 720 x 480 pixels high-resolution. It has 120 LCD drive outputs and enables design of a compact LCD TV due to TAB (Tape Automated Bonding) technology.

Features

- LCD drive outputs: 120
- Internal sample and hold circuits: 480 (4 circuits per output)
- Support of single-rate sequential drive mode and double-rate sequential drive mode
- Support of various types of color filter arrangements through an internal color sequence controller
- Vertical pixels: 240 (middle-resolution) or 480 (high-resolution)
- Horizontal pixels: 480 to 720
- Support of monodirectional connection mode and bidirectional connection mode through a bidirectional shift register
- Dynamic range: 15 V_{PP}
- Package: 156-pin TAB
- Power supply: +5 V and –15 V
- CMOS process

Pin Arrangement



HD66300T Pin Arrangement

Pin Description

Pin List

Pin Name	No. of Pins	Input/ Output	Connected to	Functions (Refer to)
D1 - D120	120	O	LCD panel	1.
HCK1, HCK2, HCK3	3	I	Controller	2.
DL, DR	2	I/O	Controller or next HD66300T	3.
FD	1	I	Controller	4.
RS	1	I	GND	5.
OE	1	I	Controller	6.
SHL	1	I	V_{CC} or GND	7.
D/$\overline{S}$	1	I	V_{CC} or GND	8.
L/$\overline{F}$	1	I	V_{CC}or GND	9.
MSF1, MSF2	2	I	V_{CC} or GND	10.
TEST1, TEST2	2	I	GND	11.
Vx1, Vx2, Vx3, Vy1, Vy2, Vy3	6	I	Inverter	12.
V_{bo}	1	I	Power source	13.
V_{bsB}, V_{bsH}	2	I	Power source	14.
$V_{LC}1$, $V_{LC}2$, $V_{LC}3$, $V_{LC}4$	4	—	Power source	15.
$V_{CC}1$, $V_{CC}2$, $V_{CC}3$	3	—	Power source	16.
GND	1	—	Power source	17.
$V_{BB}1$, $V_{BB}2$, $V_{BB}3$, $V_{BB}4$	4	—	Power source	18.

Pin Functions

1. **D1 - D120:** These pins output LCD drive signals.

2. **HCK1, HCK2, HCK3:** These pins input three-phase clock pulses, which determine the signal sampling timing for sample and hold circuits.

3. **DL, DR:** These pins input or output data into or from the internal bidirectional shift register. The state of pin SHL determines whether these pins input or output data.

SHL	DL	DR
V_{CC}	Output	Input
GND	Input	Output

4. **FD:** This pin inputs the field determination signal, which allows the sample and hold circuitry and the shift matrix circuit to operate synchronously with TV signals, at its rising and falling edge.

FD = high: First field

FD = low: Second field

When a non-interlace signal is applied, it must be inverted every field.

When an interlace signal is applied in double-rate sequential drive mode with per-line inversion (mode 1, 2, 3), the signal must be set high in both fields. The signal must be set low, however, in each field's horizontal retrace period.

5. **RS:** This pin inputs a test signal and should be connected to pin GND.

6. **OE:** This pin inputs the signal which controls the controller of the shift matrix circuit; it changes the selection of a sample and hold circuit and the shift matrix (combination of color data), at its rising edge. It also switches the bias current of the output buffer, as shown in the following table.

OE	Bias Current of Output Buffer
High	Large current (determined by VbsB)
Low	Small current (determined by VbsH)

7. **SHL:** This pin selects the shift direction of the shift register.

SHL	Shift Direction
High	DL ← DR
Low	DL → DR

8. **D/$\overline{S}$:** This pin selects the LCD drive mode.

D/$\overline{S}$	Mode
High	Double-rate sequential drive mode
Low	Single-rate sequential drive mode

9. **L/$\overline{F}$:** This pin selects the inversion mode of LCD drive signals.

L/$\overline{F}$	Mode
High	Per-line inversion mode
Low	Per-field inversion mode

10. MSF1, MSF2: These pins select the function of the shift matrix circuit; they should be set according to both the type of color filter arrangement on a TFT-type LCD panel and the drive mode.

Filter Arrangement	Drive Mode	MSF1	MSF2
Diagonal mosaic	Single-rate	GND	V_{CC}/GND
pattern	Double-rate	GND	V_{CC}/GND
Vertical stripe	Single-rate	V_{CC}	V_{CC}
pattern	Double-rate	V_{CC}	V_{CC}
Unicolor triangular	Single-rate	V_{CC}	V_{CC}
pattern	Double-rate	V_{CC}	GND
Bicolor triangular	Single-rate	V_{CC}	GND
pattern	Double-rate	V_{CC}	GND

Single-rate: Single-rate sequential drive mode
Double-rate: Double-rate sequential drive mode

11. TEST1, TEST2: These pins input test signals and should be connected to pin GND.

12. Vx1, Vx2, Vx3, Vy1, Vy2, Vy3: Video signals are applied to these pins; in general, positive video signals are connected to pins Vxi and negative video signals to pins Vyi.

13. V_{bo}: Bias voltage is applied to this pin for the differential amplifier in the sample and hold circuitry.

14. V_{bsB}, V_{bsH}: Bias voltage is applied to this pin for the two power sources of the output buffer.

VbsB: The voltage for driving a capacitive load
VbsH: The voltage for holding the output voltage

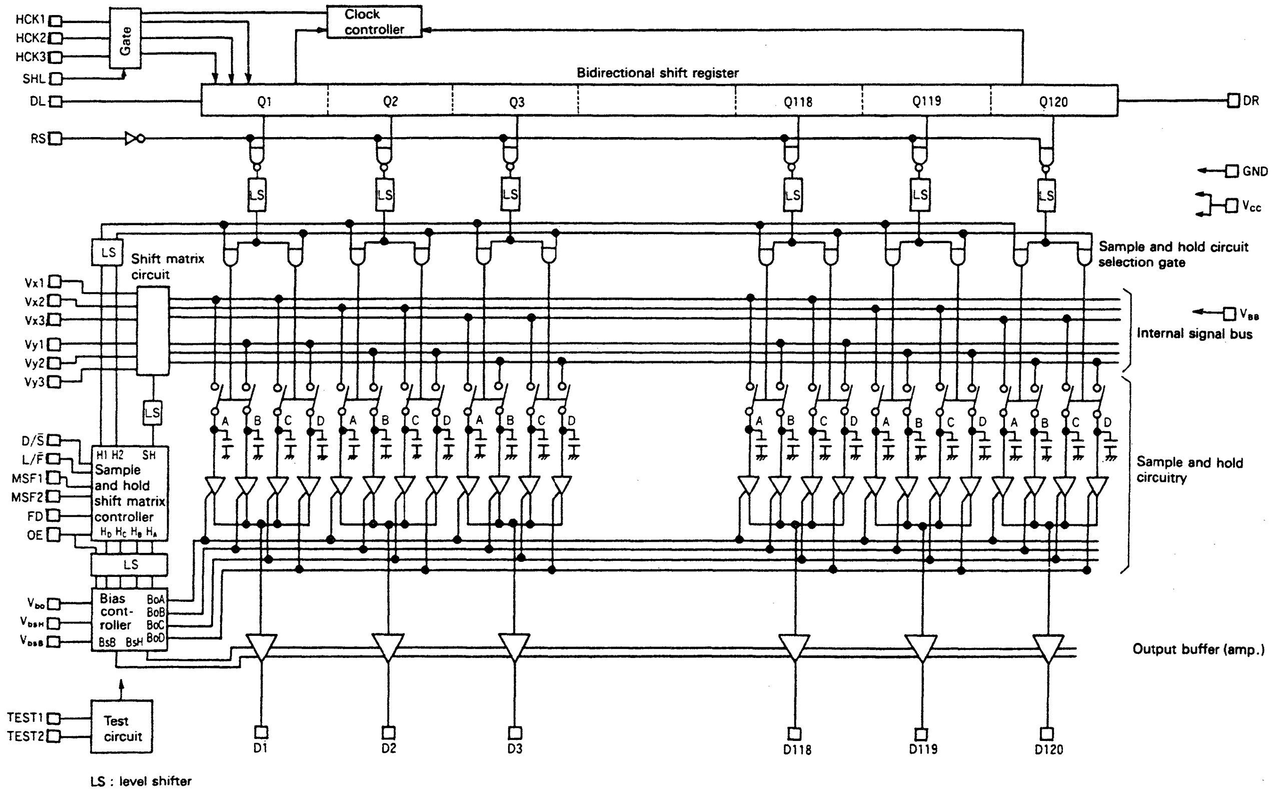
15. $V_{LC}1$, $V_{LC}2$, $V_{LC}3$, $V_{LC}4$: +5 V LCD drive voltage is applied to these pins.

16. $V_{CC}1$, $V_{CC}2$, $V_{CC}3$, $V_{CC}4$: +5 V is applied to these pins for the logic and the analog units.

17. GND: 0 V is applied to this pin for the logic unit.

18. $V_{BB}1$, $V_{BB}2$, $V_{BB}3$, $V_{BB}4$: –15 V is applied to these pins for the analog unit.

Internal Block Diagram



LS : level shifter

Block Functions

Shift Register: The shift register generates the sampling timing for video signals. It is driven by three-phase clocks HCK1, HCK2, and HCK3, whose phases are different from each other by 120°; each clock determines the sampling timing for one color signal so that three clocks support the three color signals R, G, and B. The shift direction of this register can be changed.

Level Shifter: The level shifter changes 5-V signals into 20-V signals.

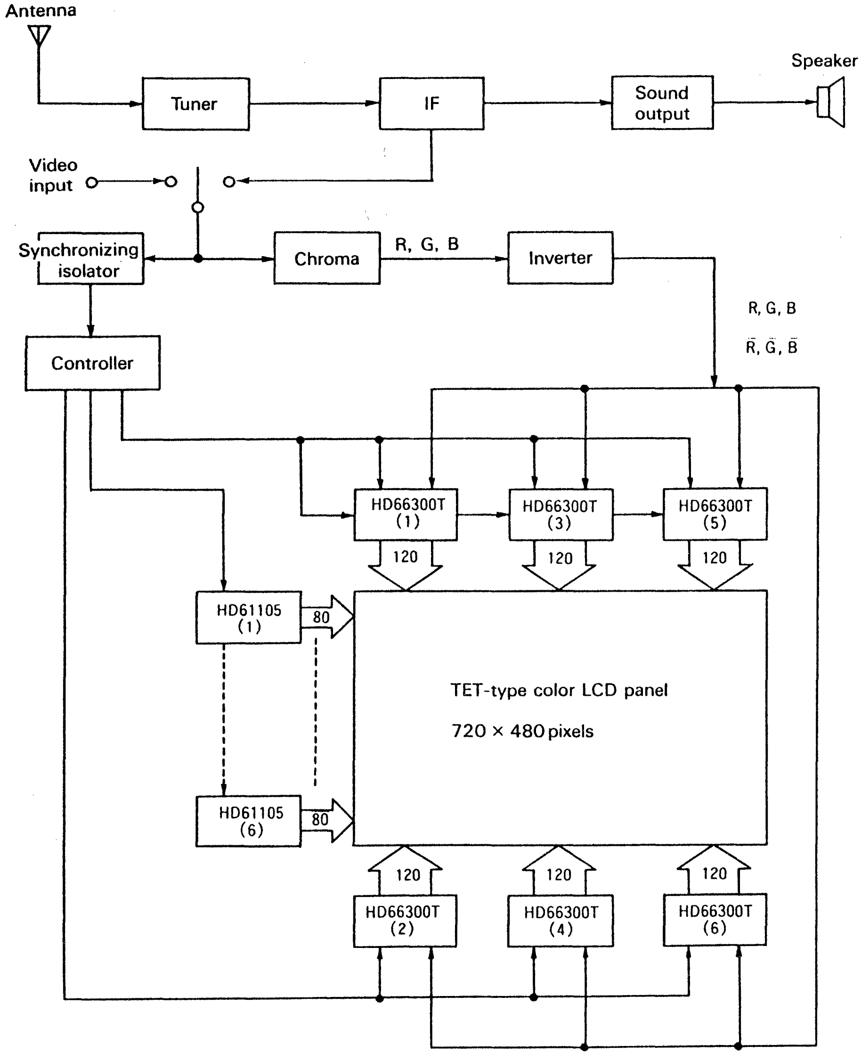
Sample and Hold Circuitry: In double-rate sequential drive mode, two sample and hold circuits are selected to sample video signals during one horizontal scanning period out of the four circuits attached to one LCD drive signal. One of the two selected circuits is read out in the first half of the following horizontal scanning period, and the other selected circuit is read out in the second half. While the two circuits are being read out, the other two circuits sample signals and are alternately read out in the same procedure mentioned above.

In single-rate sequential drive mode, one sample and hold circuit samples a signal during one horizontal scanning period, and is read out in the following horizontal scanning period. While it is being read out, one circuit out of the other three samples a signal.

Shift Matrix Circuit: The shift matrix circuit, a color sequence controller, changes over the sampled video signal every horizontal scanning period.

Output Buffer: The output buffer consists of a source follower circuit and can change the through-rate of an output signal by changing the external bias voltage.

System Block Configuration Example



Example of HD66300T Connection to LCD Panel

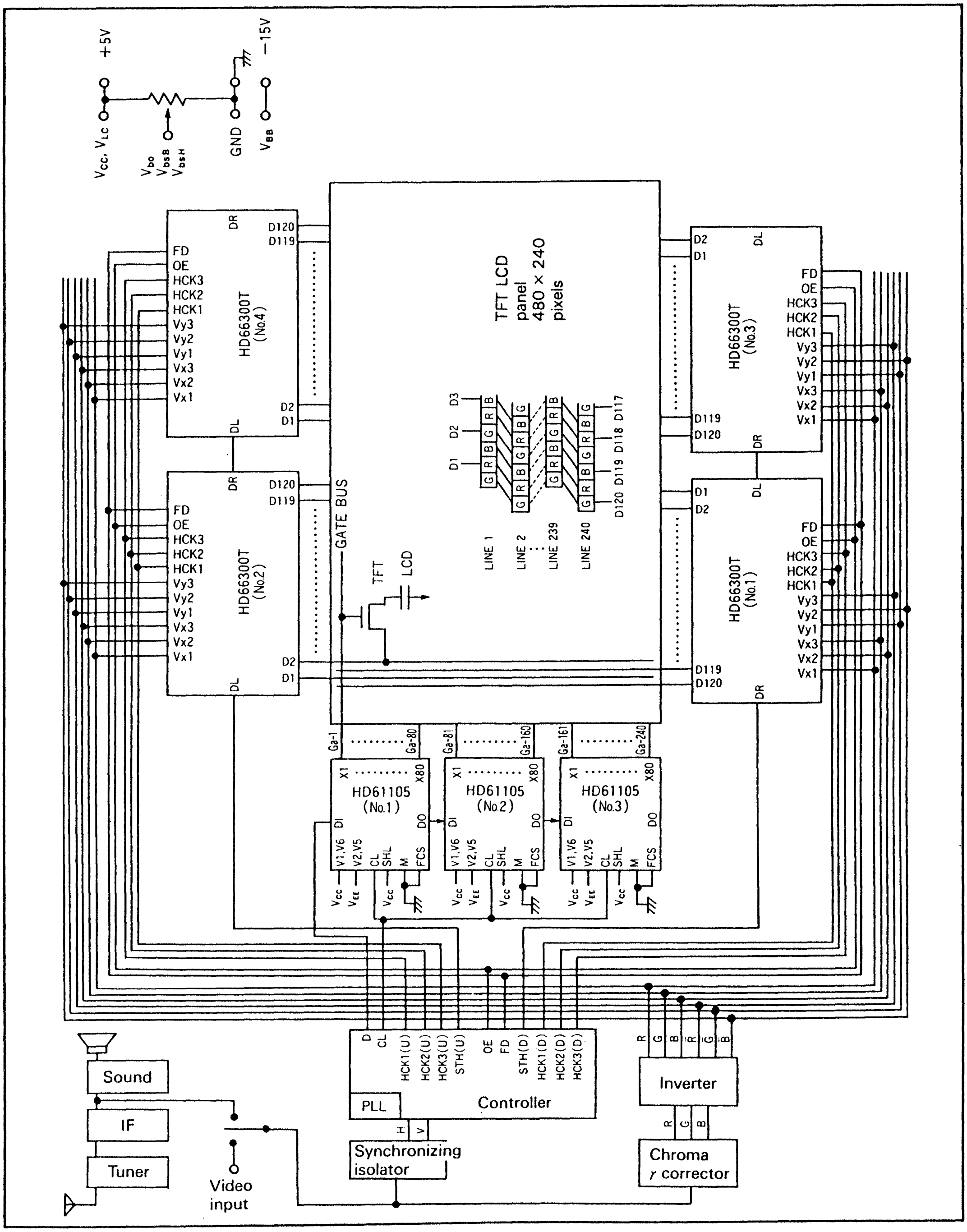


Figure 1 Example of HD66300T Connection to LCD Panel

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Functional Description

Screen Size

Number of horizontal pixels:
- 120, 240, 360, 600, and 720 in monodirectional connection mode
- 240, 480, and 720 in bidirectional connection mode

Number of vertical pixels:
- 240 in single-rate sequential drive mode
- 480 in double-rate sequential drive mode

Single-Rate Sequential Drive Mode and Double-Rate Sequential Drive Mode

Single-Rate Sequential Drive Mode: A typical TV signal (Note) has 525 scanning lines, 480 of which are part of the valid display period. In interlace scanning mode, 480 scanning lines are equally divided into a first field and a second field.

In single-rate sequential drive mode, a 240-pixel-high LCD panel is used. 240 scanning lines of the first and second fields of the TV signal are respectively assigned to the 240 lines of the LCD panel.

One line of an LCD panel is driven every horizontal scanning period in this mode.

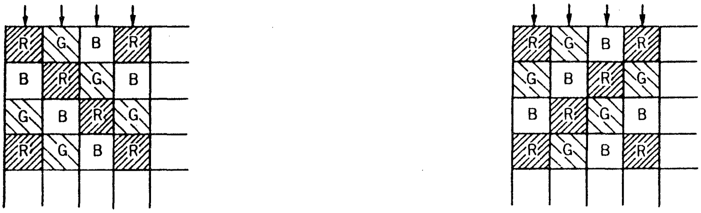
Double-Rate Sequential Drive Mode: To obtain a high-resolution display, a 480-pixel-high LCD panel is used. If 480 scanning lines are respectively assigned to the 480 lines of the LCD panel, the LCD alternating frequency becomes 15 Hz, which causes flickering and degrades display quality. To avoid this problem, the following method is employed. In the first field, the first scanning line is assigned to the first and second lines of the LCD panel, the second scanning line is assigned to the third and fourth lines, and so on. In the second field, the first scanning line is assigned to the second and third lines, the second scanning line is assigned to the fourth and fifth lines, and so on.

Two lines of an LCD panel are driven every horizontal scanning period in this mode.

Refer to the index for the further information of NTSC TV system signals and LCD.

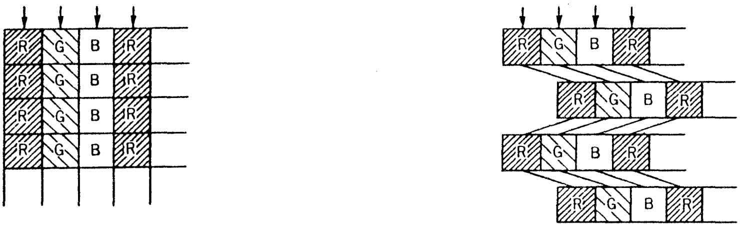
Supportable Types of Color Filter Arrangements

The order and timing for the HD66300T to output color signals depend on the color filter arrangement on a TFT-type LCD panel. The HD66300T can support TFT-type LCD panels having the following color filter arrangements by specifying the operation of the internal color sequence controller and by changing the external signals to be supplied.



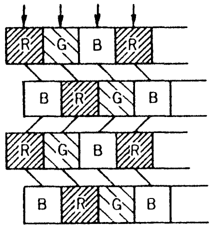
(a) Diagonal from top-left to bottom-right mosaic pattern

(d) Unicolor triangular pattern



(b) Diagonal from top-right to bottom-left mosaic pattern

(e) Bicolor triangular pattern



(c) Vertical stripe pattern

Figure 3 Supportable Types of Color Filter Arrangements

Mode Setting Pins

Mode setting pins MSF1, MSF2, and D/$\overline{S}$ must be set according to both the type of color filter arrangement on the TFT-type LCD panel and the drive mode (single-rate sequential drive mode or double-rate sequential drive mode). These pins activate the internal color sequence controller, which changes the sequence of color video signals corresponding to each sample and hold circuit and allows the LSI to output color data in the right order for the LCD panel being used.

Table 1. Mode Setting Pins

Filter Arrangement	Drive Mode	D/S	MSF1	MSF2	Referential Timing Charts
Diagonal mosaic pattern	Single-rate	GND	GND	V_{CC}, GND	MODES 15, 16, 18, and 19
	Double-rate	V_{CC}	GND	V_{CC}, GND	MODES 1, 2, 5, 6, 8, 9, 12, and 13
Vertical stripe pattern	Single-rate	GND	V_{CC}	V_{CC}	MODES 17 and 20
	Double-rate	V_{CC}	V_{CC}	V_{CC}	MODES 3, 7, 10, and 14
Unicolor triangular pattern	Single-rate	GND	V_{CC}	V_{CC}	MODES 17 and 20
	Double-rate	V_{CC}	V_{CC}	GND	MODES 4 and 11
Bicolor triangular pattern	Single-rate	GND	V_{CC}	GND	MODE 17
	Double-rate	V_{CC}	V_{CC}	GND	MODES 4 and 11

Single-rate: Single-rate sequential drive mode
Double-rate: Double-rate sequential drive mode

Per-Field Inversion and Per-Line Inversion

The inversion mode of LCD drive signals can be selected by pin L/$\overline{F}$.

Per-Field Inversion (available with L/$\overline{F}$ = low)

In a certain field, all LCD drive signals have one polarity and in the following field, they all have the inverted polarity.

Per-Line Inversion (available with L/$\overline{F}$ = high)

In a certain field, all LCD drive signals have positive polarity in odd number lines and negative polarity in even number lines, while in the following field, the situation is reversed, that is, negative polarity in odd number lines and positive polarity in even number lines.

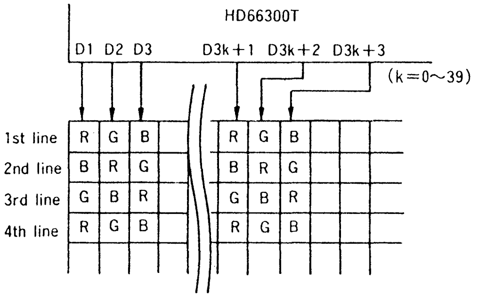
Interface

Video Signals Connection

Video signals must be connected to pins Vx1, Vx2, Vx3, Vy1, Vy2, and Vy3; in principle, positive video signals R, G, and B signals must be input to pins Vx1, Vx2, and Vx3, and negative video signals $\overline{R}$, $\overline{G}$, and $\overline{B}$ to pins Vy1, Vy2, and Vy3. For actual connection between an LCD panel and the LCD drive signal output pins, refer to the following example.

In the case of Diagonal from top-left to bottom-right mosaic pattern.

This example describes the case in which an LCD panel having a diagonal from top-left to bottom-right mosaic pattern is driven in double-rate sequential drive mode and monodirectional connection mode.



The Color Sequence for Each Output Pin

Output Pin	Color Sequence
D1 (=D3k + 1)	R → B → G → R
D2 (=D3k + 2)	G → R → B → G
D3 (=D3k + 3)	B → G → R → B

The Signal Sequence for Each Output Pin

Output Pin	Color Sequence
D1 (=D3k + 1)	Vx1 → Vx3 → Vx2 → Vx1 →
D2 (=D3k + 2)	Vx2 → Vx1 → Vx3 → Vx2 →
D3 (=D3k + 3)	Vx3 → Vx2 → Vx1 → Vx3 →

(Refer to MODE 5)

The Connection of Signals

Signal	Color
Vx1	R
Vx2	G
Vy3	B
Vy1	$\overline{R}$
Vy2	$\overline{G}$
Vy3	$\overline{B}$

In the case of Diagonal from top-right to bottom-left mosaic pattern, Vertical stripe pattern

The same procedure for video signal connection applies to the case in which a TFT-type LCD panel having a diagonal from top-right to bottom-left mosaic pattern or a vertical stripe pattern is used, as well as to the cases where a panel of any pattern is used through the bidirectional connection mode.

Triangular Pattern, Single-Rate Sequential Drive Mode

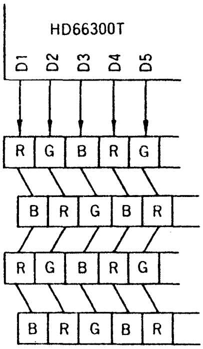
The following procedures are required when a panel of unicolor or bicolor triangular pattern is used:

1. Unicolor Triangular Pattern, Single-Rate Sequential Drive Mode

The clock phase must be changed every line because of the 1.5-pixel phase shift between even number lines and odd number lines. (Refer to the explanation of sampling clocks.)
The connection of signals here is the same as that described above.

2. Bicolor Triangular Pattern, Single-Rate Sequential Drive Mode

The clock phase must be changed every line because of the 0.5-pixel phase shift between even number lines and odd number lines. (Refer to the explanation of sampling clocks.)
The connection of video signals in the second field must be changed from that in the first field. See the following tables.



The Color Sequence for each Output Pin

Output Pin	Color Sequence
D1 (=D3k + 1)	R → B → R → B →
D2 (=D3k + 2)	G → R → G → R →
D3 (=D3k + 3)	B → G → B → G →

The Signal Sequence for each Output Pin

Output Pin		Signal Sequence
1st field	D1 (=D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
	D2 (=D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (=D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd field	D1 (=D3k + 1)	Vy1 → Vx1 → Vy1 → Vx1 →
	D2 (=D3k + 2)	Vy2 → Vx2 → Vy2 → Vx2 →
	D3 (=D3k + 3)	Vy3 → Vx3 → Vy3 → Vx3 →

(Refer to MODE 17)

The Connection of Signal in Each Field

	Per-Field Inversion Mode (L/$\overline{F}$ = low)		Per-Field Inversion Mode (L/$\overline{F}$ =high)	
	1st Field	2nd Field	1st Field	2nd Field
Vx1	R	$\overline{B}$	R	B
Vx2	G	$\overline{R}$	G	R
Vx3	B	$\overline{G}$	B	G
Vy1	B	$\overline{R}$	$\overline{B}$	$\overline{R}$
Vy2	R	$\overline{G}$	$\overline{R}$	$\overline{G}$
Vy3	G	$\overline{B}$	$\overline{G}$	$\overline{B}$

Triangular Pattern, Double-Rate Sequential Drive Mode

Changing the phase of the sampling clocks is sufficient when the panel is driven in single-rate sequential drive mode. However, when the panel is driven in double-rate sequential drive mode, the above countermeasure does not work, since the display data for two lines is sampled at one time here. Consequently, delaying the input video signal for a time period corresponding to the shift between pixels is required.

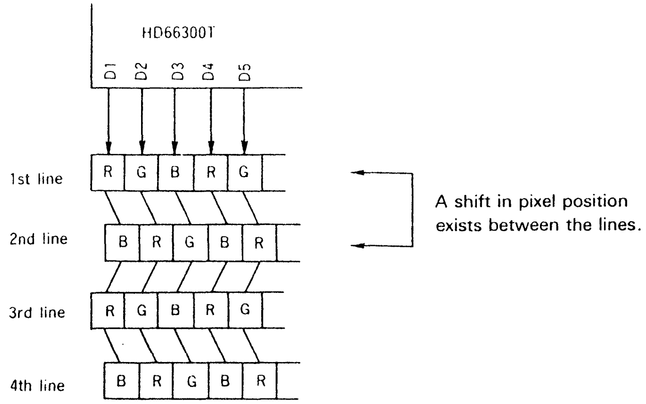


Figure 4

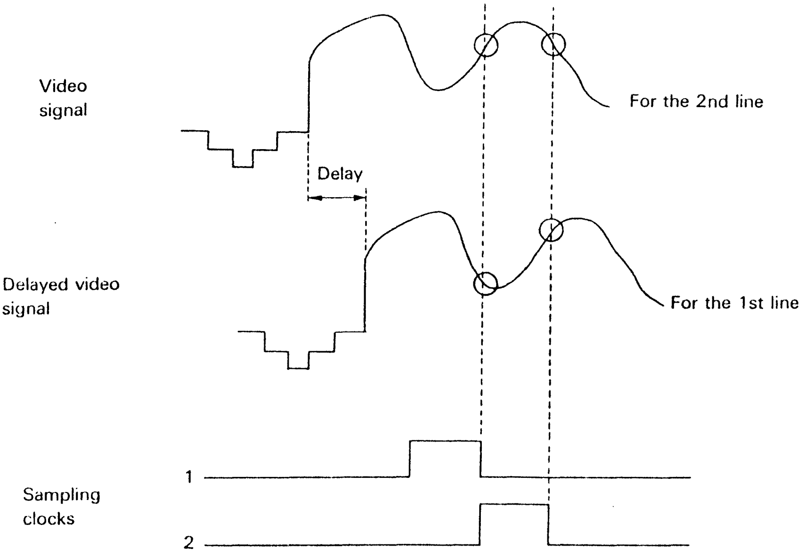
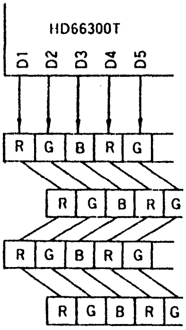


Figure 5

1. Unicolor Triangular Pattern, Double-Rate Sequential Drive Mode



The Color Sequence for Each Output Pin

Output Pin	Color Sequence
D1 (=D3k + 1)	R → R → R → R →
D2 (=D3k + 2)	G → G → G → G →
D3 (=D3k + 3)	B → B → B → B →

The Signal Sequence for each Output Pin (In Interlace mode)

Output Pin		Signal Sequence
1st	D1 (=D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
field	D2 (=D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (=D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd	D1 (=D3k + 1)	Vy1 → Vx1 → Vy1 → Vx1 →
field	D2 (=D3k + 2)	Vy2 → Vx2 → Vy2 → Vx2 →
	D3 (=D3k + 3)	Vy3 → Vx3 → Vy3 → Vx3 →

(Refer to MODE 4)

In non-interlace mode:

The Signal Sequence for each Output Pin (In non-interlace mode)

Output Pin		Signal Sequence
1st	D1 (=D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
field	D2 (=D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (=D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd	D1 (=D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
field	D2 (=D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (=D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →

(Refer to MODE 11)

1. Unicolor Triangular Pattern, Double-Rate Sequential Drive Mode (Cont.)

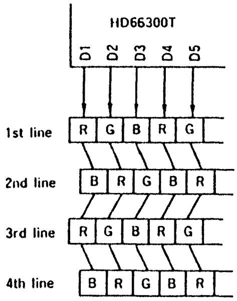
The Connection of Signals in each Field in Interlace Mode

	Per-Field Inversion Mode ($L/\overline{F}$ = low)		Per-Line Inversion Mode ($L/\overline{F}$ =high)	
	1st Field	2nd Field	1st Field	2nd Field
Vx1	Delayed R	$\overline{R}$	Delayed R	R
Vx2	Delayed G	$\overline{G}$	Delayed G	G
Vx3	Delayed B	$\overline{B}$	Delayed B	B
Vy1	R	Delayed $\overline{R}$	$\overline{R}$	Delayed $\overline{R}$
Vy2	G	Delayed $\overline{G}$	$\overline{G}$	Delayed $\overline{G}$
Vy3	B	Delayed $\overline{B}$	$\overline{B}$	Delayed $\overline{B}$

The Connection of Signals in each Field in Non-interlace Mode

	Per-Field Inversion Mode ($L/\overline{F}$ = low)		Per-Line Inversion Mode ($L/\overline{F}$ =high)	
	1st Field	2nd Field	1st Field	2nd Field
Vx1	Delayed R	Delayed $\overline{R}$	Delayed R	Delayed $\overline{R}$
Vx2	Delayed G	Delayed $\overline{G}$	Delayed G	Delayed $\overline{G}$
Vx3	Delayed B	Delayed $\overline{B}$	Delayed B	Delayed $\overline{B}$
Vy1	R	$\overline{R}$	$\overline{R}$	R
Vy2	G	$\overline{G}$	$\overline{G}$	G
Vy3	B	$\overline{B}$	$\overline{B}$	B

2. Bicolor Triangular Pattern, Double-Rate Sequential Drive Mode



The Color Sequence for each Output Pin

Output Pin	Color Sequence
D1 (=D3k + 1)	R → B → R → B →
D2 (=D3k + 2)	G → R → G → R →
D3 (=D3k + 3)	B → G → B → G →

The Signal Sequence for each Output Pin (In interlace mode)

	Output Pin	Signal Sequence
1st field	D1 (=D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
	D2 (=D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (=D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd field	D1 (=D3k + 1)	Vy1 → Vx1 → Vy1 → Vx1 →
	D2 (=D3k + 2)	Vy2 → Vx2 → Vy2 → Vx2 →
	D3 (=D3k + 3)	Vy3 → Vx3 → Vy3 → Vx3 →

(Refer to MODE 4)

The Signal Sequence for each Output Pin (In non-interlace mode)

	Output Pin	Signal Sequence
1st field	D1 (=D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
	D2 (=D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (=D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd field	D1 (=D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
	D2 (=D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (=D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →

(Refer to MODE 11)

2. Bicolor Triangular Pattern, Double-Rate Sequential Drive Mode (Cont.)

The Connection of Signals in each Field in Interlace Mode

	Per-Field Inversion Mode ($L/\overline{F}$ = low)		Per-Line Inversion Mode ($L/\overline{F}$ =high)	
	1st Field	2nd Field	1st Field	2nd Field
Vx1	Delayed R	$\overline{B}$	Delayed R	B
Vx2	Delayed G	$\overline{R}$	Delayed G	R
Vx3	Delayed B	$\overline{G}$	Delayed B	G
Vy1	B	Delayed $\overline{R}$	$\overline{B}$	Delayed $\overline{R}$
Vy2	R	Delayed $\overline{G}$	$\overline{R}$	Delayed $\overline{G}$
Vy3	G	Delayed $\overline{B}$	$\overline{G}$	Delayed $\overline{B}$

The Connection of Signals in each Field in Non-interlace Mode

	Per-Field Inversion Mode ($L/\overline{F}$ = low)		Per-Line Inversion Mode ($L/\overline{F}$ =high)	
	1st Field	2nd Field	1st Field	2nd Field
Vx1	Delayed R	Delayed $\overline{R}$	Delayed R	Delayed $\overline{R}$
Vx2	Delayed G	Delayed $\overline{G}$	Delayed G	Delayed $\overline{G}$
Vx3	Delayed B	Delayed $\overline{B}$	Delayed B	Delayed $\overline{B}$
Vy1	B	$\overline{B}$	$\overline{B}$	B
Vy2	R	$\overline{R}$	$\overline{R}$	R
Vy3	G	$\overline{G}$	$\overline{G}$	G

Connection to LCD Panels

There are two modes of connecting HD66300T chips to an LCD panel:

1) monodirectional connection mode
2) bidirectional connection mode

In the former mode, the HD66300Ts are set on either the upper side or lower side of the panel, while in the latter mode, the HD66300Ts are set on both sides and the upper drivers and the lower drivers are alternately connected to each pixel-column.

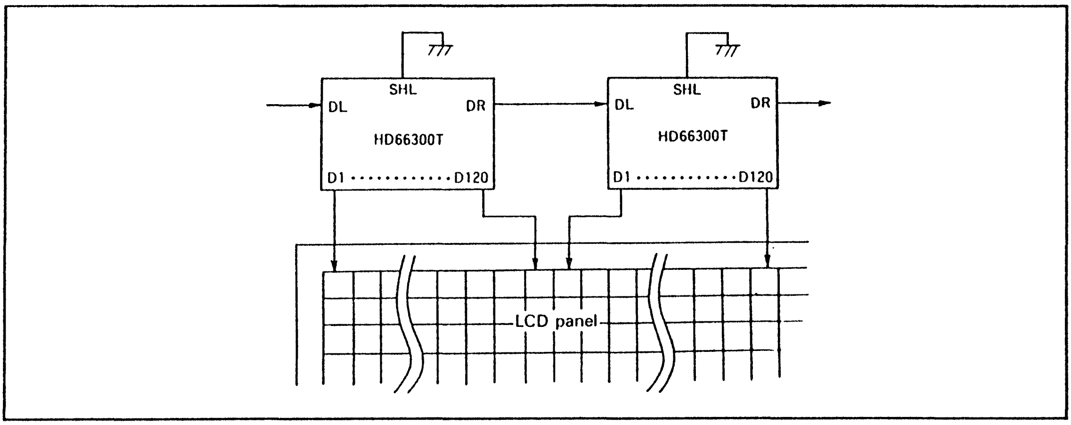


Figure 6 Monodirectional Connection Mode

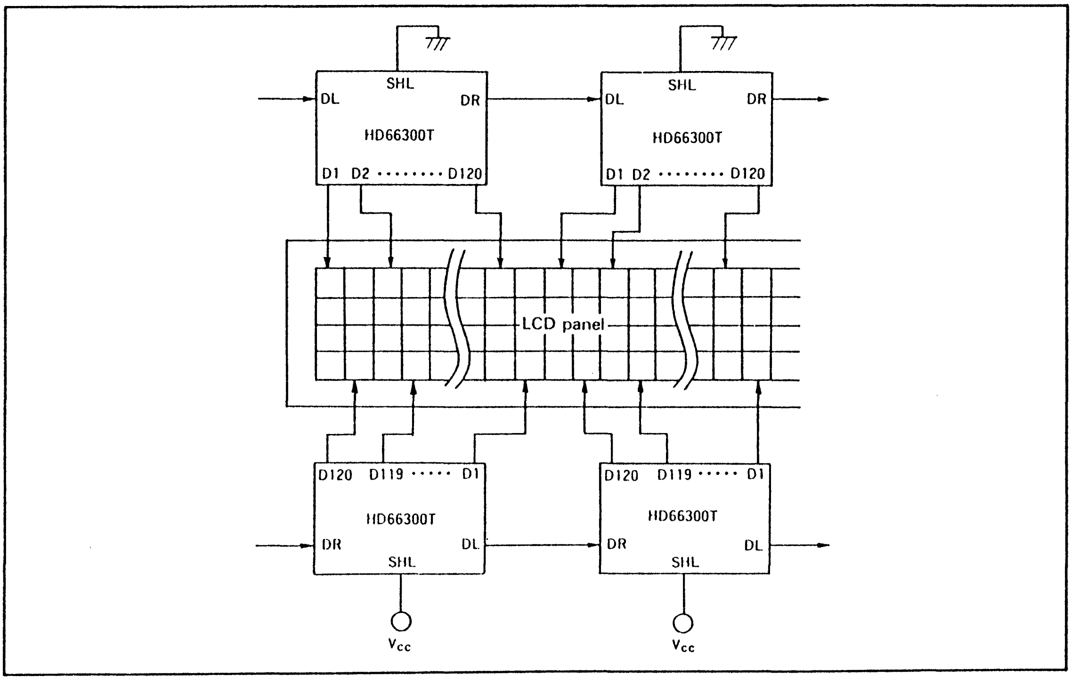


Figure 7 Bidirectional Connection Mode

Internal Operation

The HD66300T has four sample and hold circuits for each outputs as shown in the block diagram, and its internal bidirectional shift register controls which circuits to sample data.

It has three-phase shift clocks with mutual phase difference of 120° to drive the shift register, which enables driving an LCD panel with mosaic pattern and triangular pattern.

The operation of sample and hold circuits and sampling operation are described below followed by the description of the relationship between three-phase shift clock phases and frequencies.

After the above description, determination of bias voltage is described; bias voltage controls driving characteristics of a differential amplifier and output buffer of the sample and hold circuits.

Finally, the OE and FD signals are described; they determine the operation of the sample and hold shift matrix circuit. Timing charts for each mode follow the description.

Sample and Hold Circuitry

Operation of Sample and Hold Circuitry

The HD66300T has four sample and hold circuits A, B, C, and D per LCD drive signal output. Sample and hold circuit pair A and B is supplied with the same sampling clock pulses as circuit pair C and D. One of the signals output by these circuits is connected to an output driver.

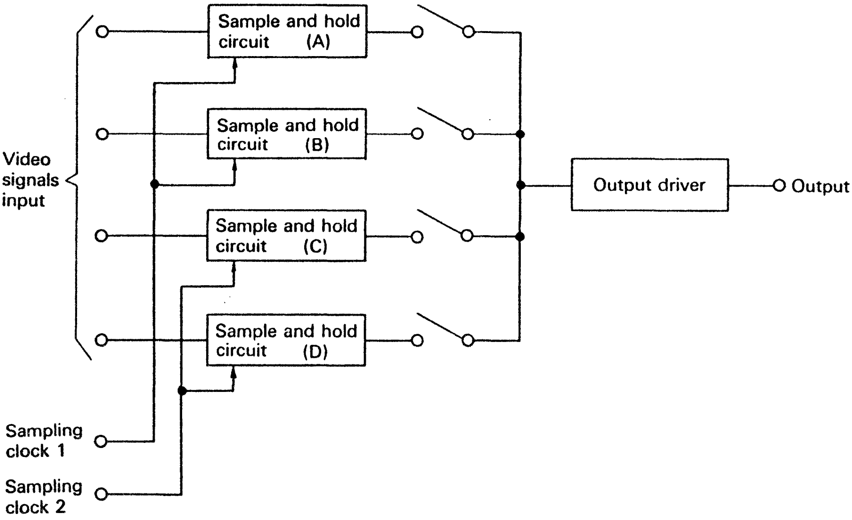

Video signals input
Sample and hold circuit (A)
Sample and hold circuit (B)
Sample and hold circuit (C)
Sample and hold circuit (D)
Output driver
Output
Sampling clock 1
Sampling clock 2

Figure 8 Sample and Hold Circuitry

These sample and hold circuits repeat sampling and outputting of signals alternately to drive an TFT-type LCD panel.

In single-rate sequential drive mode, sample and hold circuits A and D are alternately used; circuits B and C perform sampling operation, but are not used since they are not connected to the output driver.

In single-rate sequential drive mode, one sample and hold circuit samples the signal during one horizontal scanning period, and outputs it as an LCD drive signal in the following horizontal scanning period.

In double-rate sequential drive mode, all sample and hold circuits A, B, C, and D are alternately used.

In double-rate sequential drive mode, two sample and hold circuits sample two signals during one horizontal scanning period, and output one of them as an LCD drive signal in the first half of the following horizontal scanning period, and output the other signal in the second half.

The following shows the timing charts of sampling and outputting operation.

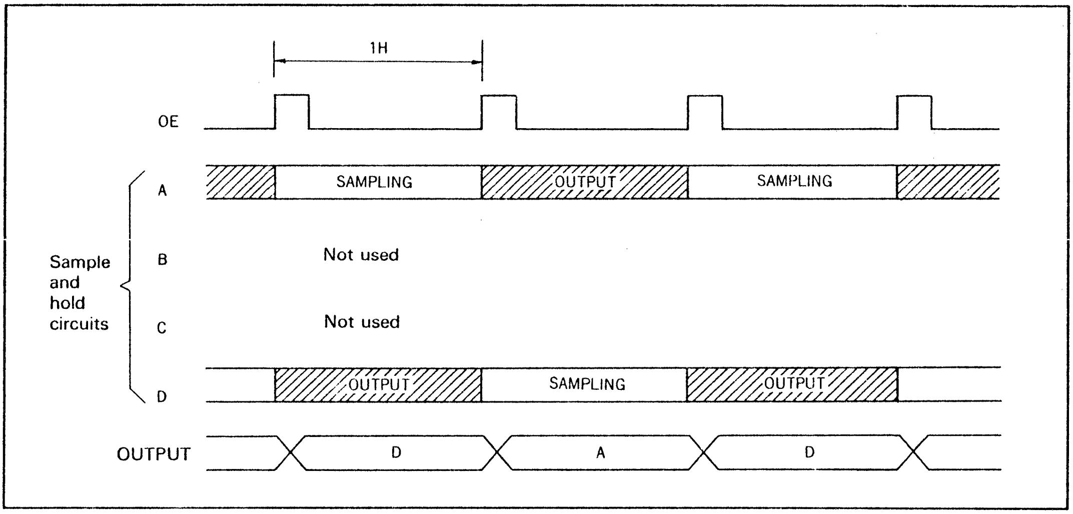


Figure 9 Sampling Timing charts of Single-Rate Sequential Drive Mode

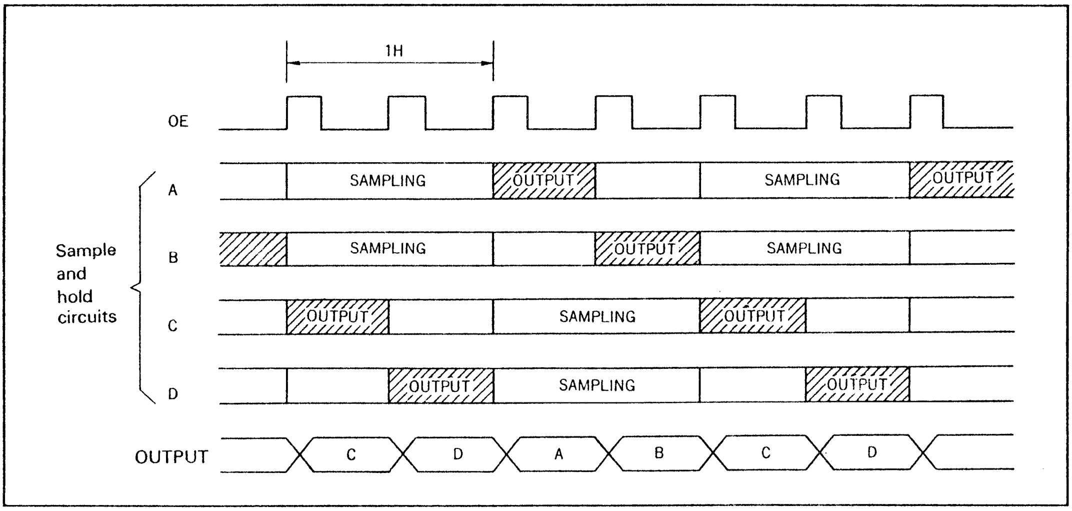


Figure 10 Sampling Timing charts of Double-Rate Sequential Drive Mode

Sampling Operation

The HD66300T has a bidirectional shift register composed of 120 bits and each bit of the shift register generates the sampling pulses to control the sampling operation of the four sample and hold circuits connected to each LCD drive signal output pin. When a bit of the shift register is 1, the corresponding sample and hold circuits are in the sampling state; when it is 0, the corresponding sample and hold circuits are in the hold state. Consequently, shifting a 1 into the shift register activates in turn the sample and hold circuits corresponding to each LCD drive signal output pin.

Figure 11 is a shift register sketch illustrating the relationship between the shift register and the shift clocks HCK1, HCK2, and HCK3. Note that the order of sampling pulse generation depends on the state of pin SHL. D1 corresponds to DL and D120 to DR.

Figure 12 is a timing chart of sampling pulses generated by the shift register.

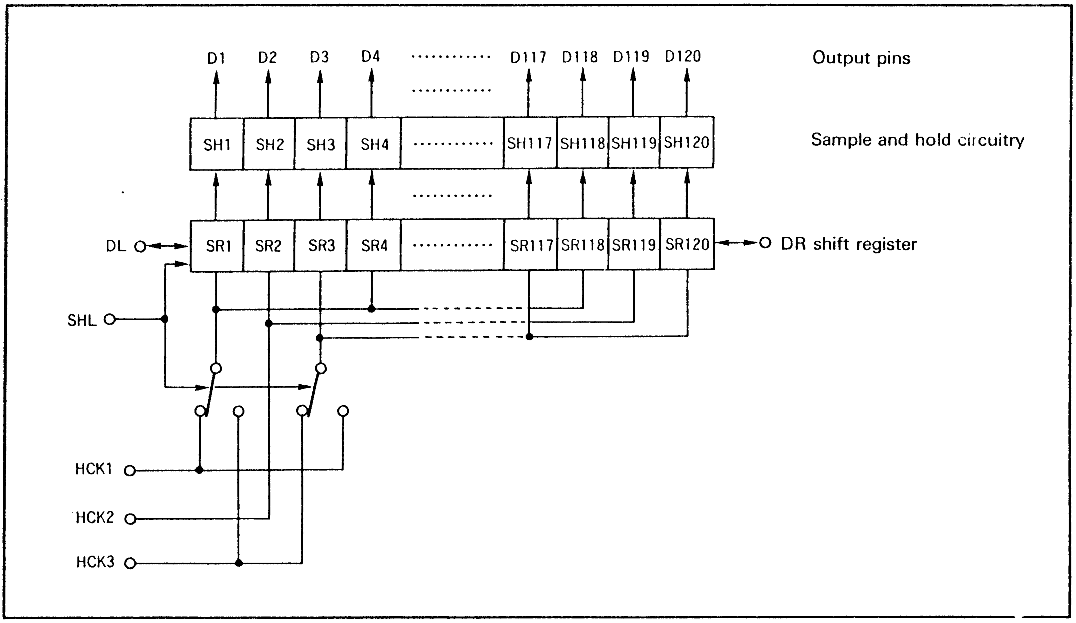
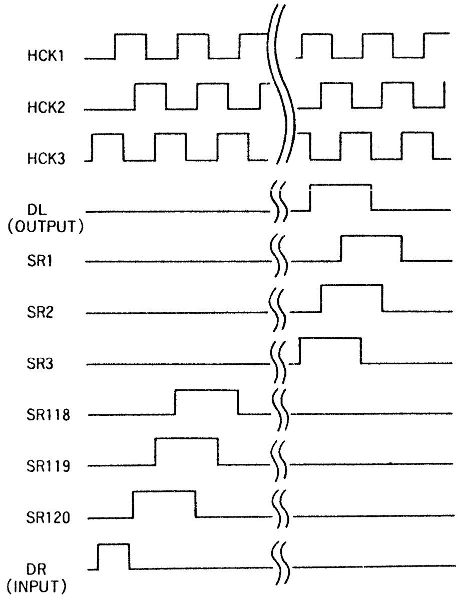
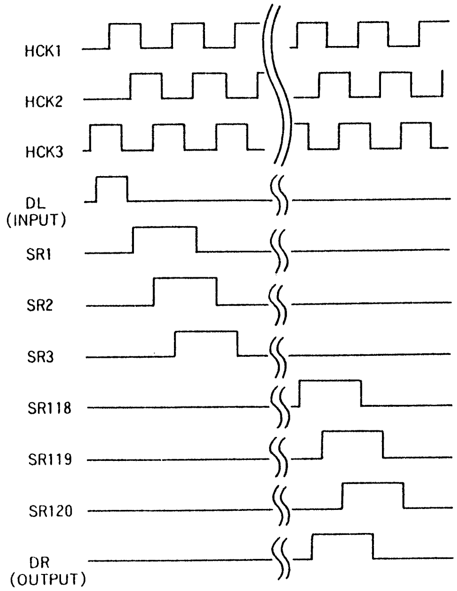


Figure 11 Shift Register Sketch



(a) SHL=Low



(b) SHL=High

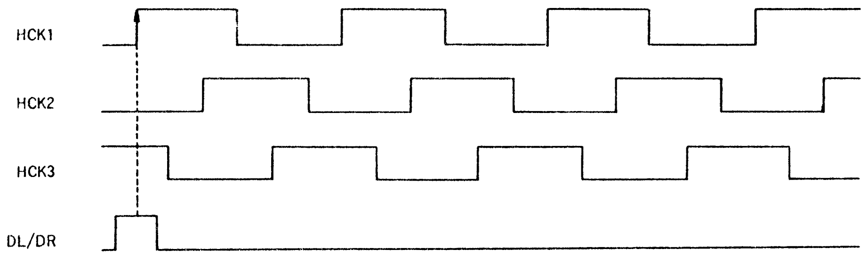
Figure 12 Sampling Pulse Timing Chart

Three-Phase Shift Clocks

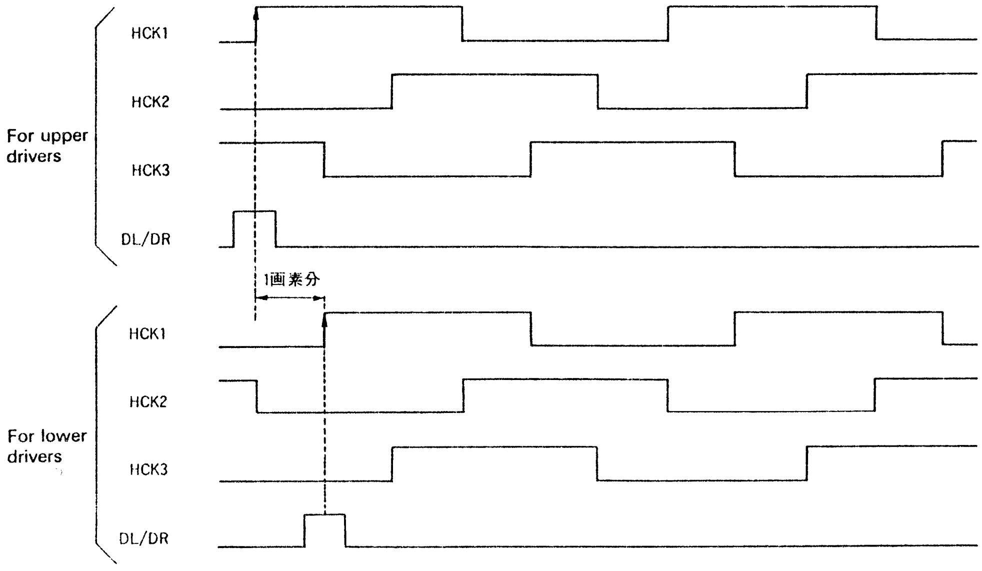
Three-Phase Shift Clocks and Sample Start Signal

Shift clocks HCK1, HCK2, and HCK3, which are operation clocks for the shift register, must be three-phase clocks with 50-percent duty. The HCK2 clock must be generated 120° after the HCK1 clock, and the HCK3 clock 240° after the HCK1 clock. Sampling operation starts when 1 is input from pin DL or DR at a rising edge of the HCK1 clock pulse.

In monodirectional connection mode, all the HD66300T chips must be supplied with the same three-phase shift clock pulses. In bidirectional connection mode, the frequency of the three-phase shift clock pulses. In bidirectional connection mode, the frequency of the three-phase shift clocks must be half of that in monodirectional connection mode, and the phase shift between the upper drivers clocks and the lower drivers clocks must be one pixel.



(a) In Monodirectional Connection Mode

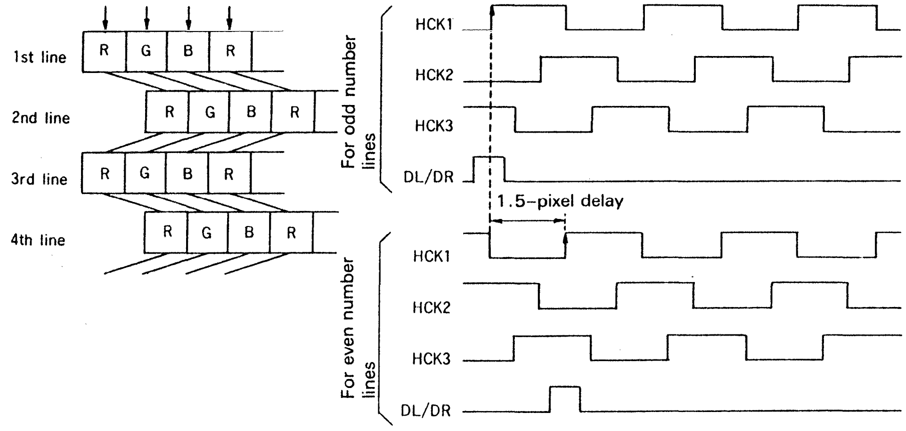


The lower driver clock pulses follow the upper driver clock pulses by one pixel.

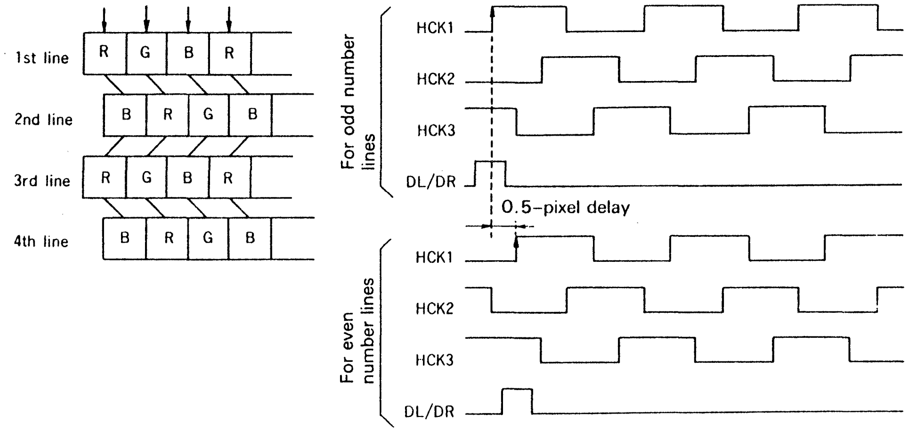
(b) In Bidirectional Connection Mode

Figure 13 Three-Phase Shift Clocks and Sample Start Signal

Some position shift exists between the pixels of even number lines and those of odd number lines for LCD panels having triangular patterns. This requires generating a phase shift between the three-phase clocks for even number lines and those for odd number lines. The required phase shift is 1.5 pixels for LCD panels having a unicolor triangular pattern, while it is 0.5 pixels for those having a bicolor triangular pattern.



(a) Unicolor Triangular Patterr



(b) Bicolor Triangular Pattern

Figure 14

How to Generate Three-Phase Shift Clocks

Three-phase shift clocks can be generated by dividing the base clock, which is generated from a horizontal synchronizing clock, through the use of a frequency multiplier such as a PLL circuit.

The number of horizontal pixels of the LCD panel and the valid display ratio determines the base clock frequency f.

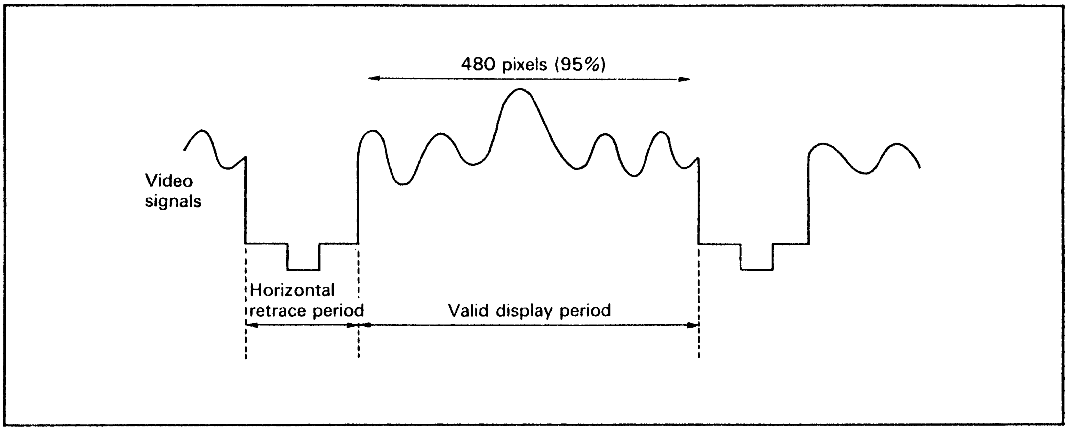
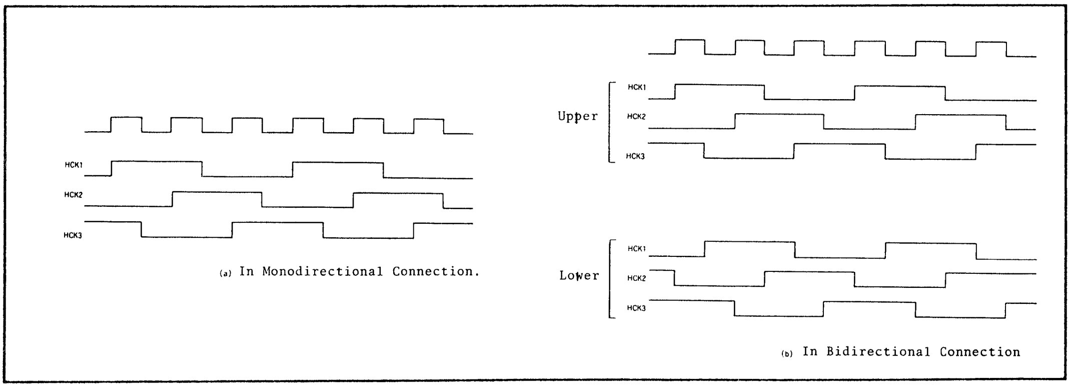


Figure 15 Base Clock

If the number of horizontal pixels is 480 and the valid display ratio is 95% in the NTSC system, the base clock frequency f is about 9.59 MHz according to the following equation.

$$
\begin{aligned}
f &= (1/\text{valid display period}) \times (\text{no. of horizontal pixels}/\text{valid display ratio}) \\
&= 480/(52.7\ \mu\text{sec} \times 0.95) \\
&= 9.59\ (\text{MHz})
\end{aligned}
$$

In general, this clock frequency is again doubled to generate a base clock of 2f in order to achieve a clock duty of 50%.



(a) In Monodirectional Connection.

(b) In Bidirectional Connection

Figure 16 Three-Phase Shift Clocks

Bias Voltage

The drive capability of the output buffer and differential amplifier is controlled by voltages V_{bsB} V_{bsI}, and V_{bo}. Usually, the same level of voltage should be applied to these pins.

The LSI must be used in the range of

$$V_{CC} - 4.0\text{ V} \leqq V_{bsB} = V_{bsI} = V_{bo} \leqq V_{CC} - 2.0\text{ V}$$

As voltages V_{bsB}, V_{bsI}, and V_{bo} are brought nearer to the V_{CC} level, the current consumption is reduced but rising and falling times increase. On the other hand, as they are brought nearer to the GND level, rising and falling times are reduced but current consumption increases.

OE Signal

The OE signal has the following functions:

Clock for internal circuits: Controls the sample and hold circuitry and the controller of the shift matrix circuit, and switches the output signal at the OE signal rising edge.

Switching of drive capability of the output buffer: Determines the current drive capability of the output buffer;

OE = high: Drives with large current (300 µA, typ)
OE = low: Drives with small current (20 µA, typ)

This function allows the output buffer to operate with large current during the transition of an output signal, thus shortening its falling time. At the same time it allows the output buffer to operate with small current while an output signal is stable, lowering current consumption.

The drive current is controlled by bias voltages V_{bsB} (large current) and V_{bsI} (small current).

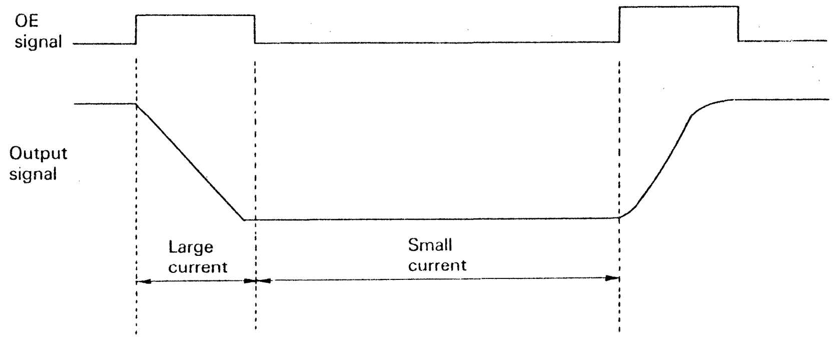


Figure 17 Switching of Drive Capability of the Output Buffer

FD Signal

The FD signal is the field determination signal; a field is determined by the state of this signal at the rising edge of the OE signal. This signal synchronizes the internal controllers with TV signals.

The order of outputting signals is determined at the fourth rising edge of the OE signal after the rising or falling edge of the FD signal in double-rate sequential drive mode, while it is determined at the third rising edge in single-rate sequential drive mode; hereinafter, as long as the FD signal is not changed, signals will be output in the determined order at most every 12 pulses of the OE signal in double-rate sequential drive mode, while at most every 6 pulses in single-rate sequential drive mode.

The FD signal should usually be high in the first field and low in the second field. In some modes, however, it should be high in both fields, but low for at least one-pulse time period of the OE signal during the horizontal scanning period.

The order of outputting signals and the timing of inputting the FD signal vary depending on the mode. For more details, refer to the appropriate timing charts.

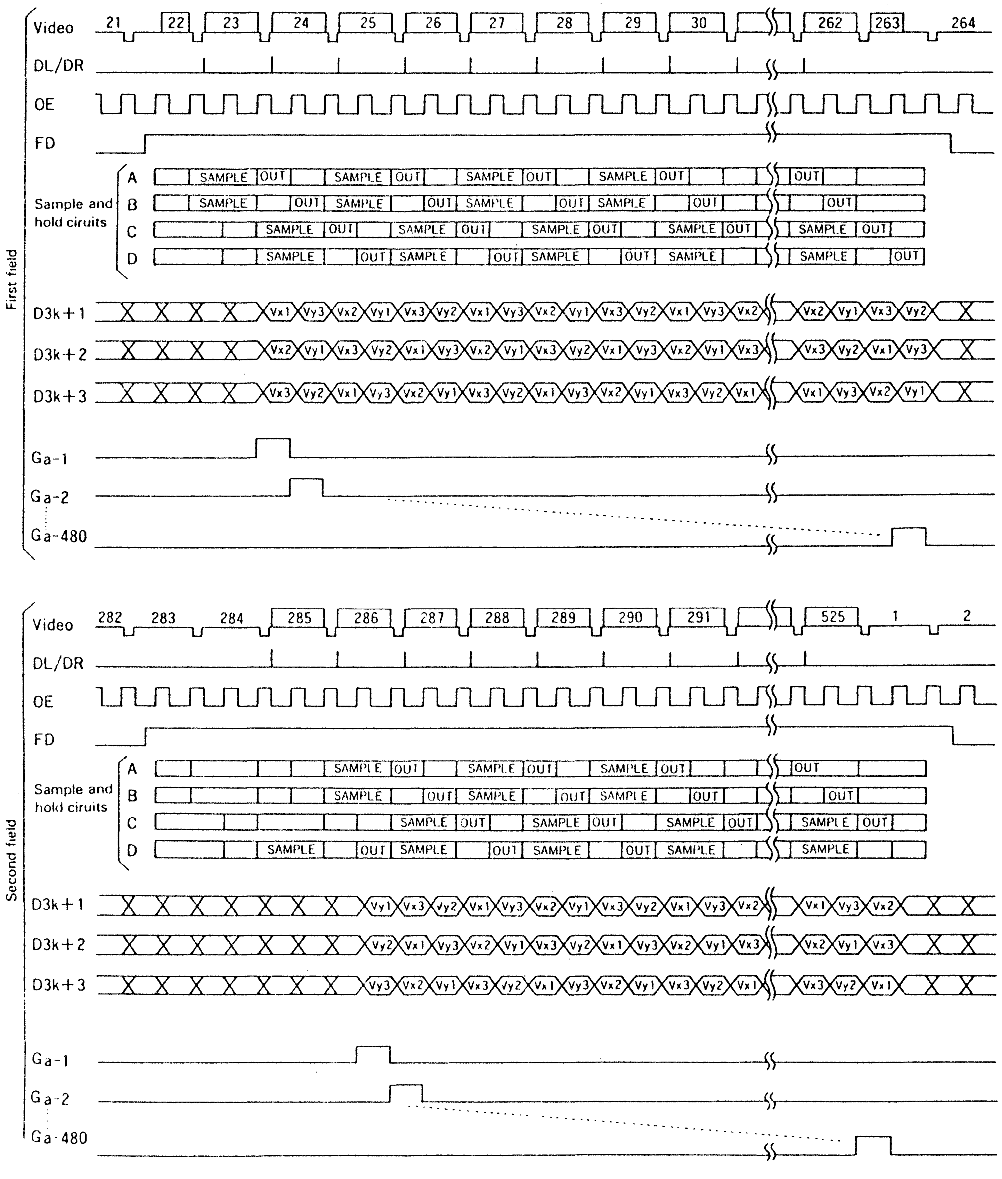
Timing Charts for Each Mode

Table 2. Reference timing charts for each mode

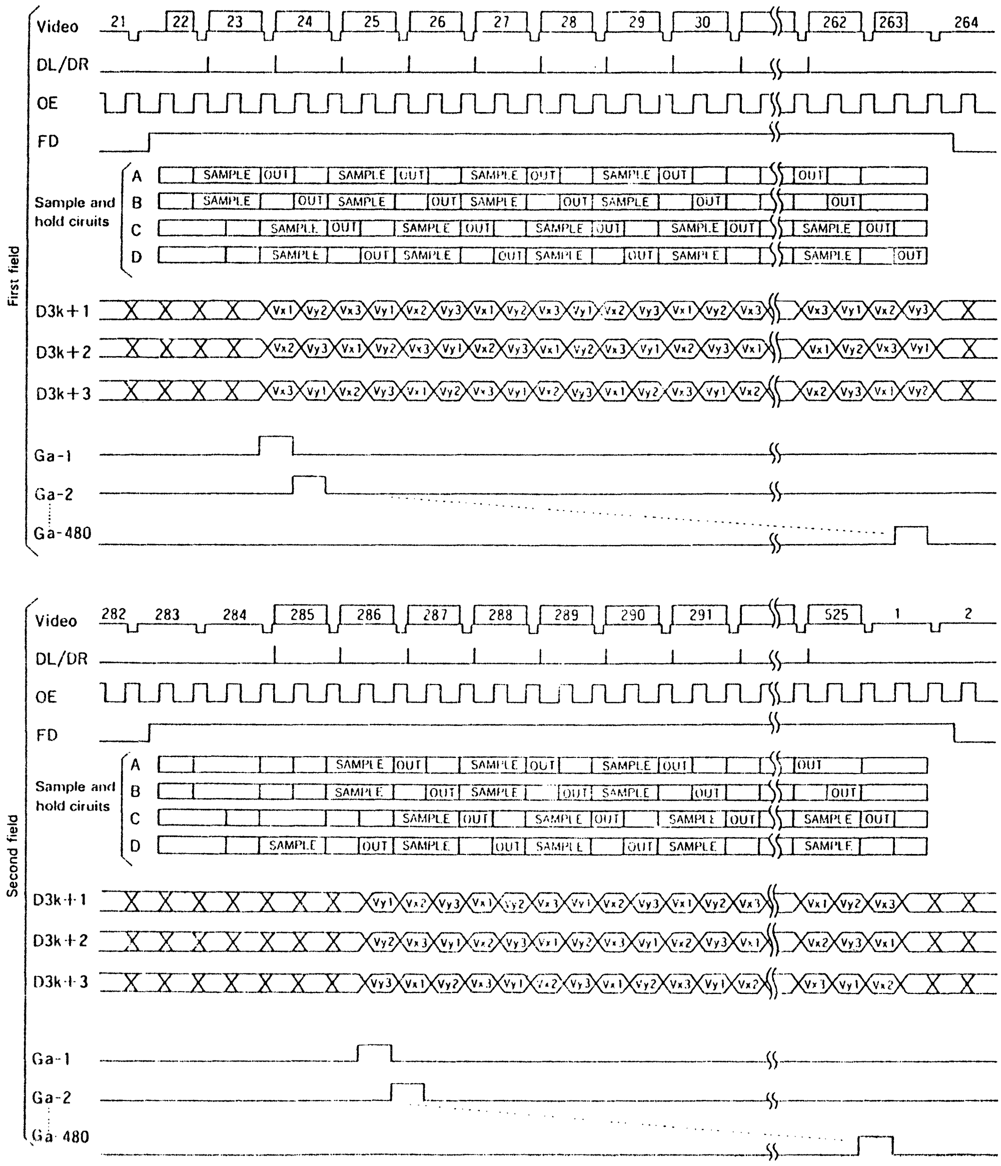
			Single (D/S = Low)		Double (D/S = High)			
					Interlace		Non-Interlace	
Filter Arrangement			Per-Line	Per-Field	Per-Line	Per-Field	Per-Line	Per-Field
Mosaic	Top-left to bottom-right	Bidirectional	MODE 15	MODE 18	MODE 2	MODE 6	MODE 9	MODE 13
		Monodirectional	MODE 16	MODE 19	MODE 1	MODE 5	MODE 8	MODE 12
	Top-right to bottom-left	Bidirectional	MODE 16	MODE 19	MODE 1	MODE 5	MODE8	MODE 12
		Monodirectional	MODE 15	MODE 18	MODE 2	MODE 6	MODE 9	MODE 13
Vertical stripe			MODE 17	MODE 20	MODE 3	MODE 7	MODE 10	MODE 14
Unicolor triangular			MODE 17	MODE 20	MODE 4	MODE 4	MODE 11	MODE 11
Bicolor triangular			MODE 17	MODE 17	MODE 4	MODE 4	MODE 11	MODE 11

Single: Single-rate sequential drive mode
Double: Double-rate sequential drive mode
Per-Line: Per-line inversion mode
Per-Field: Per-field inversion mode
Bidirectional: Bidirectional connection mode
Monodirectional: Monodirectional connection mode

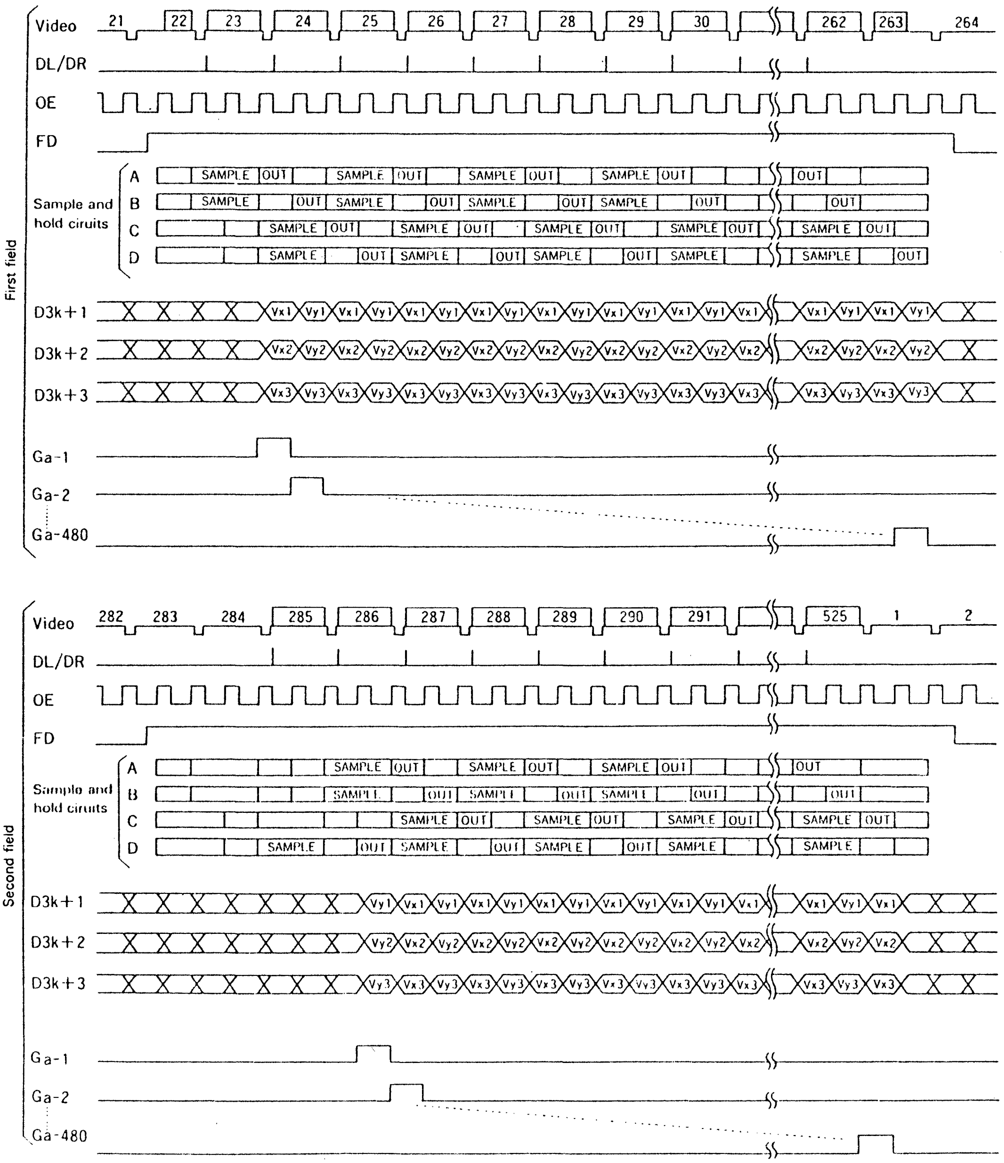
MODE 1	
D/S	V_{cc}
L/F	V_{cc}
MSF1	GND
MSF2	V_{cc}



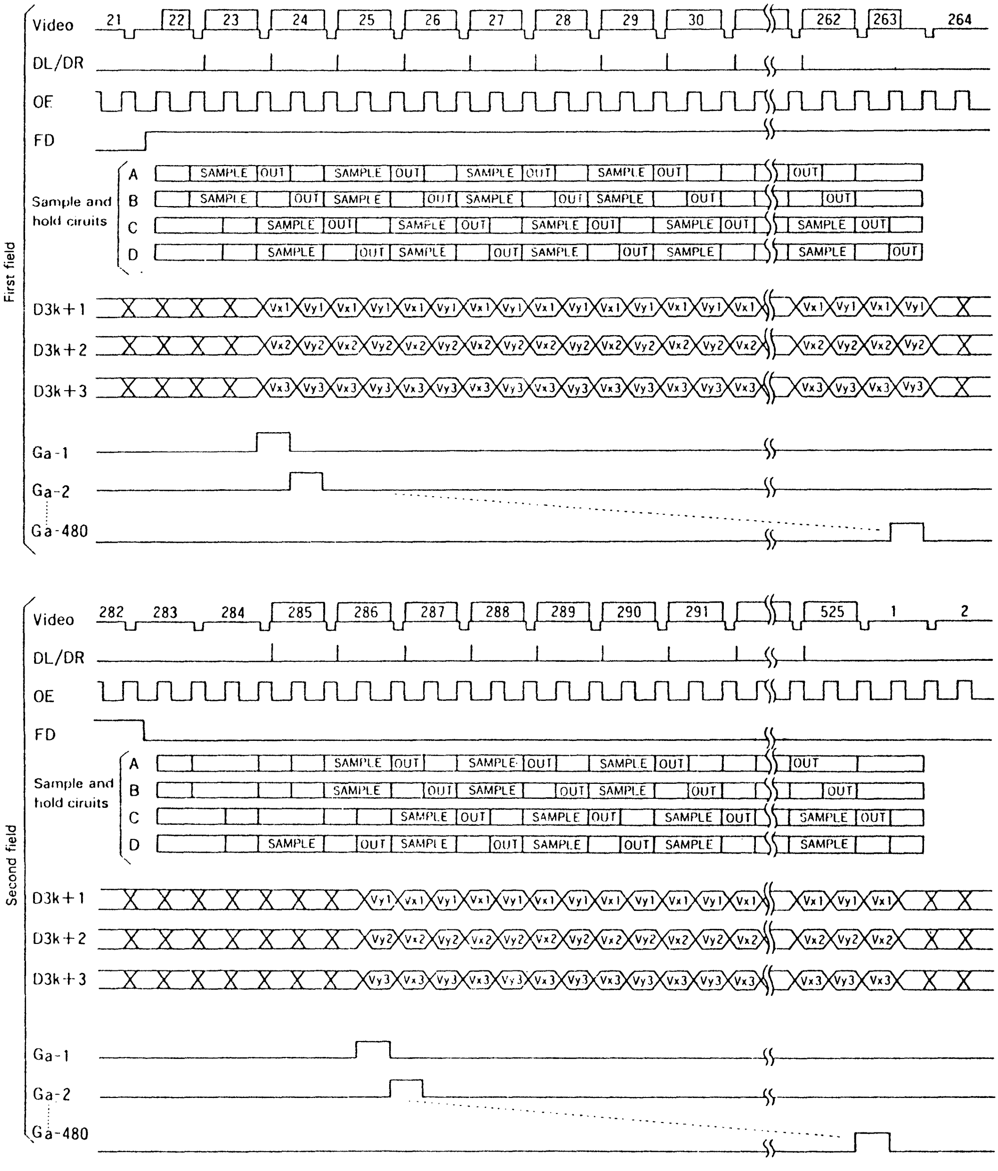
MODE 2	
D/S	V_{cc}
L/F	V_{cc}
MSF1	GND
MSF2	GND



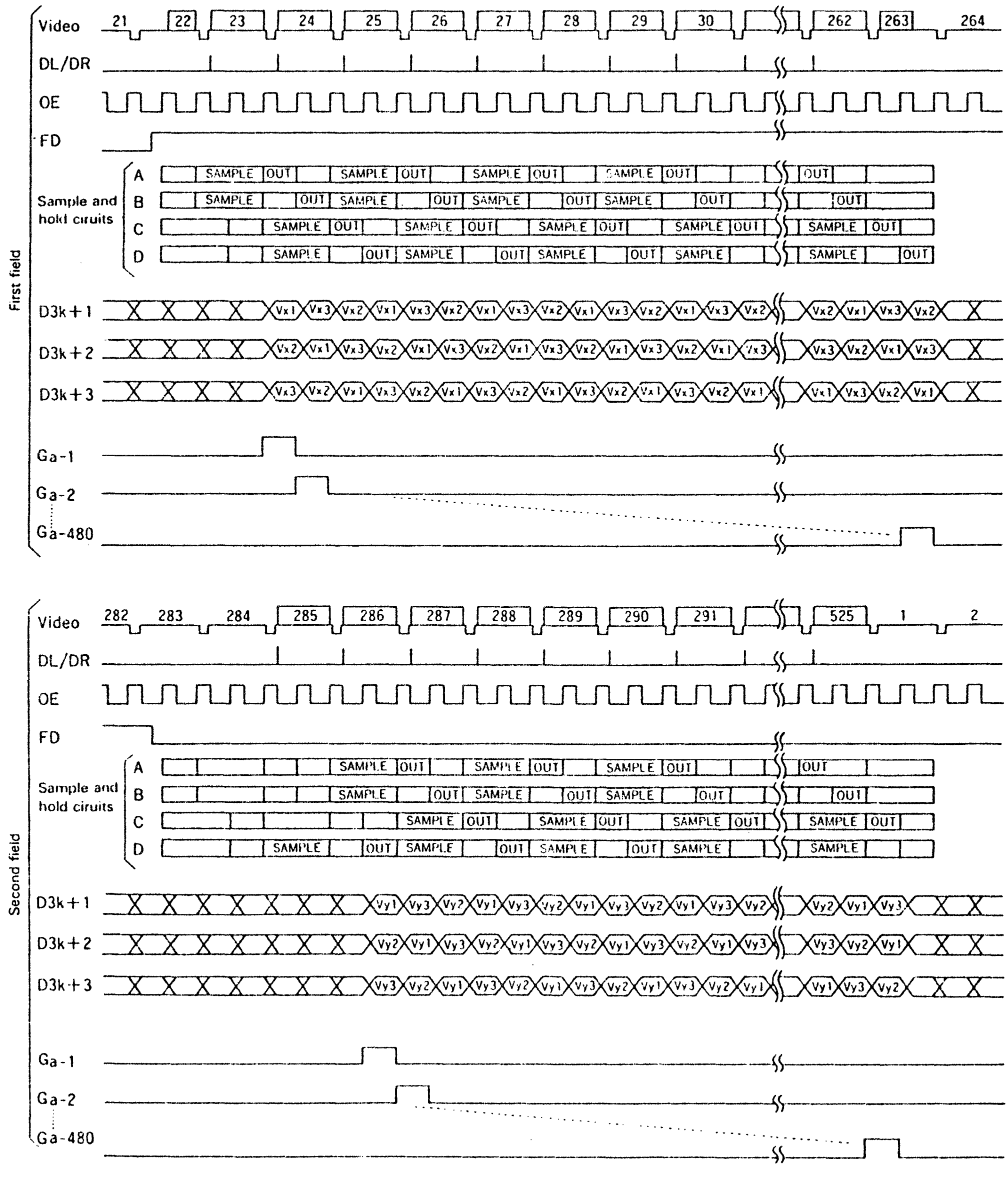
MODE 3	
D/S	V_{cc}
L/F	V_{cc}
MSF1	V_{cc}
MSF2	V_{cc}



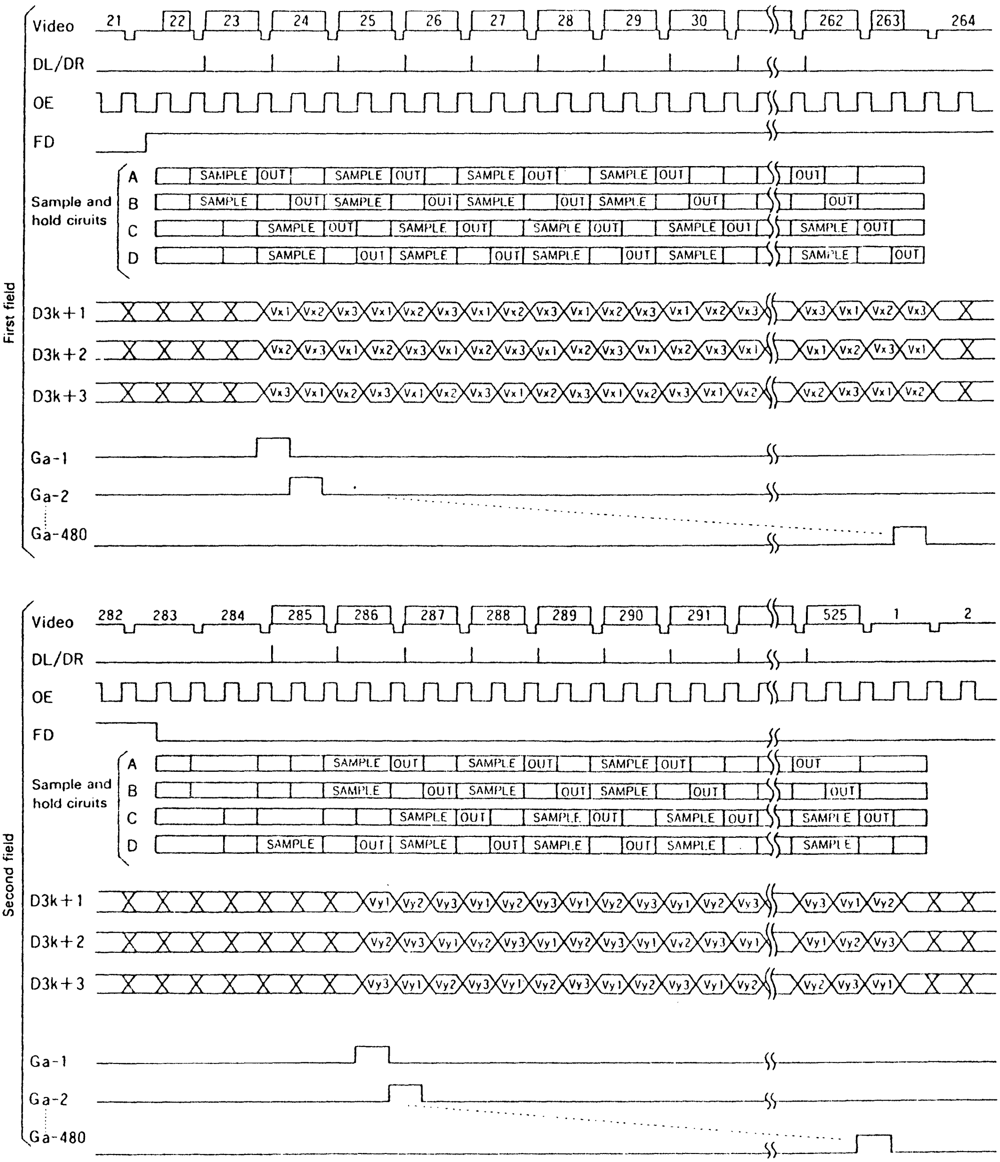
MODE 4	
D/S	V_{cc}
L/F	V_{cc}/GND
MSF1	V_{cc}
MSF2	GND



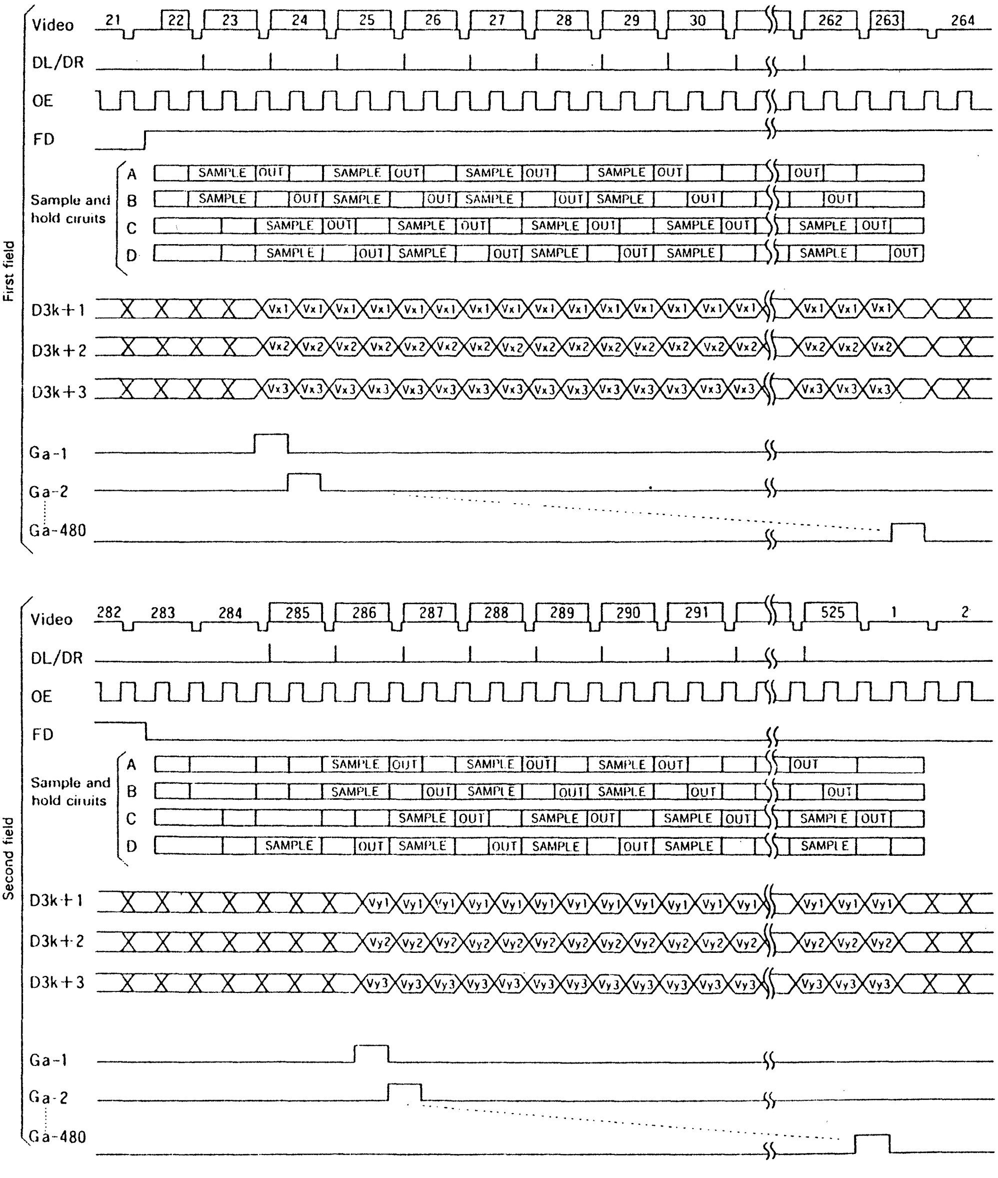
MODE 5	
D/S	V_{cc}
L/F	GND
MSF1	GND
MSF2	V_{cc}



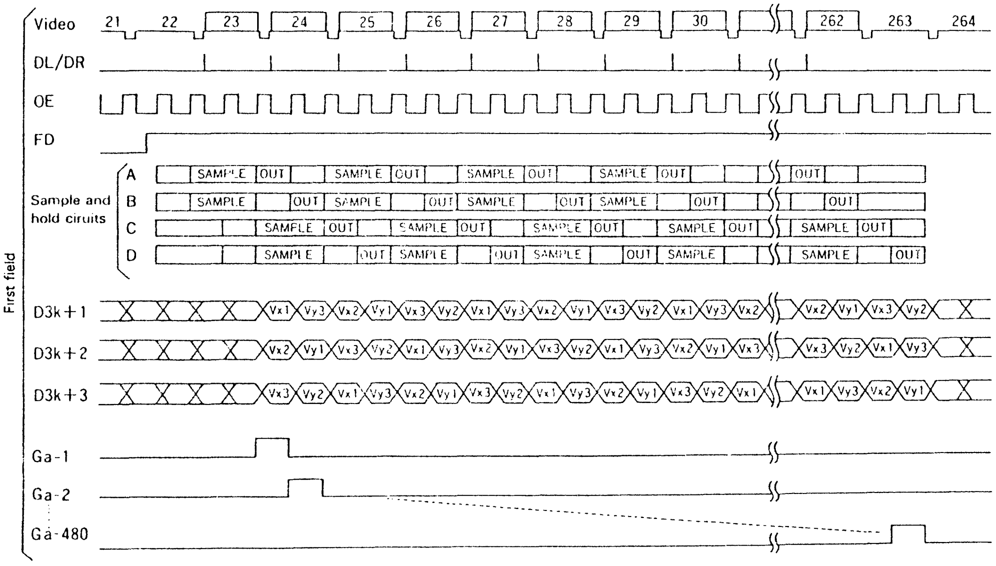
MODE 6	
D/S	V_{CC}
L/F	GND
MSF1	GND
MSF2	GND

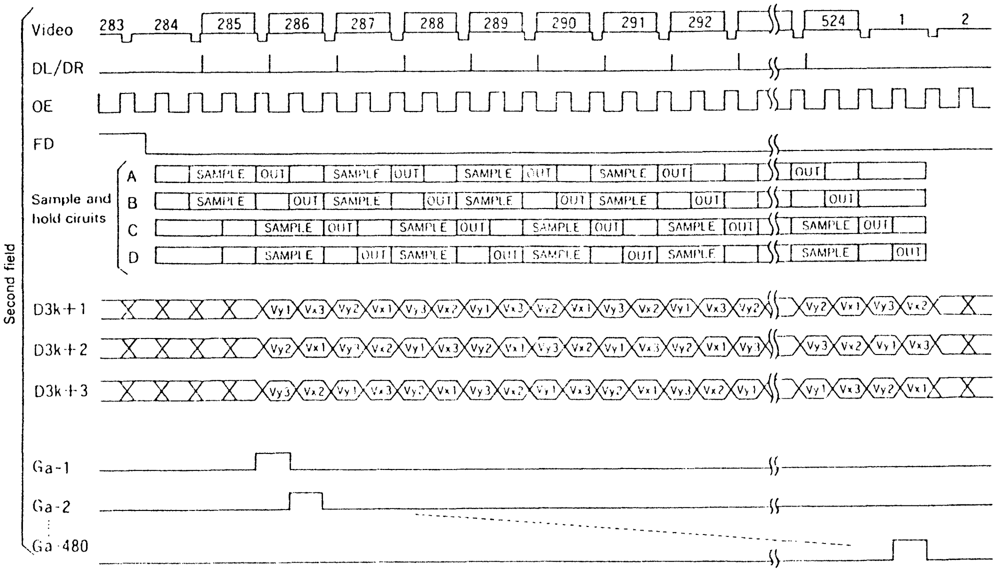


MODE 7	
D/S	V_{CC}
L/F	GND
MSF1	V_{CC}
MSF2	V_{CC}

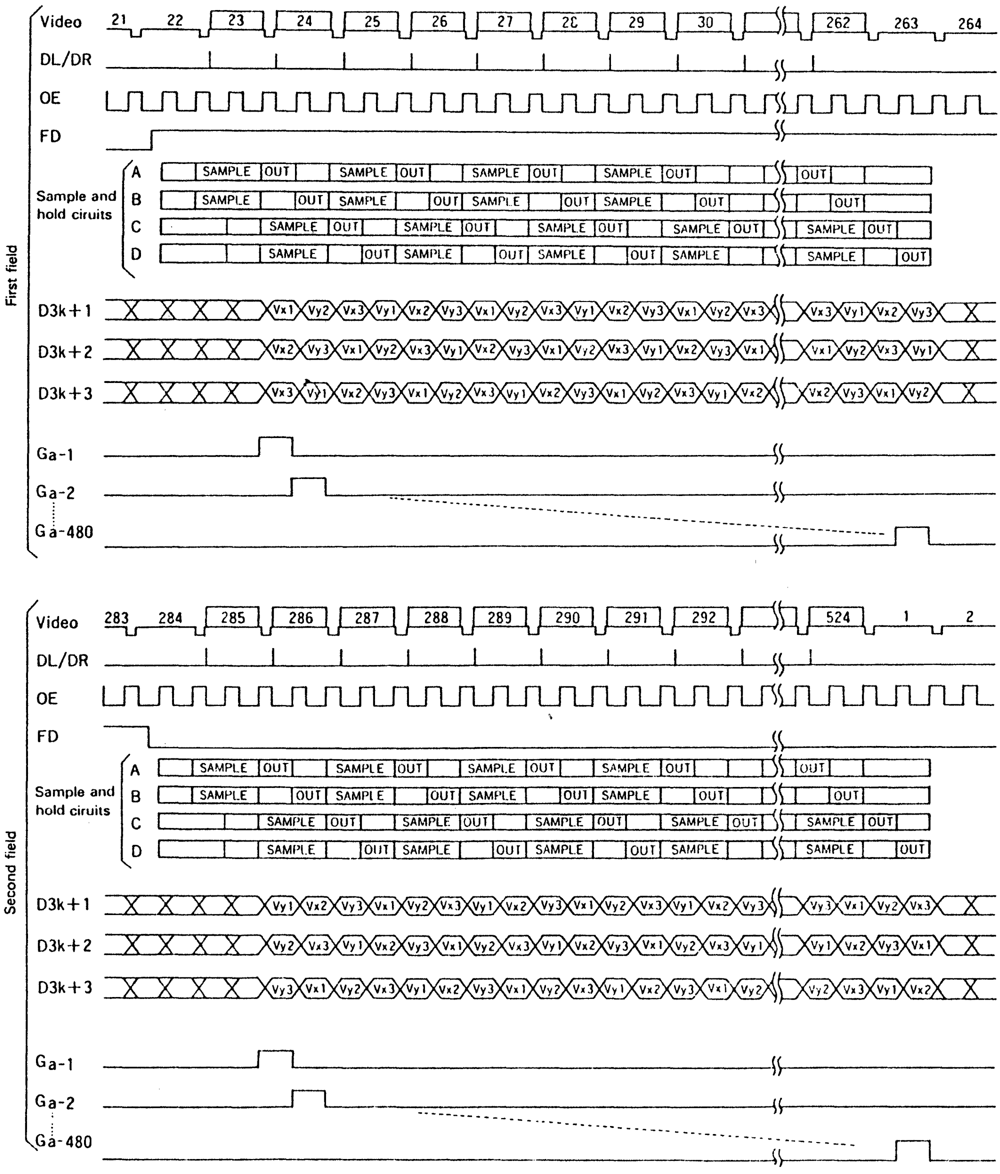


MODE 8	
D/S	V_{CC}
L/F	V_{CC}
MSF1	GND
MSF2	V_{CC}

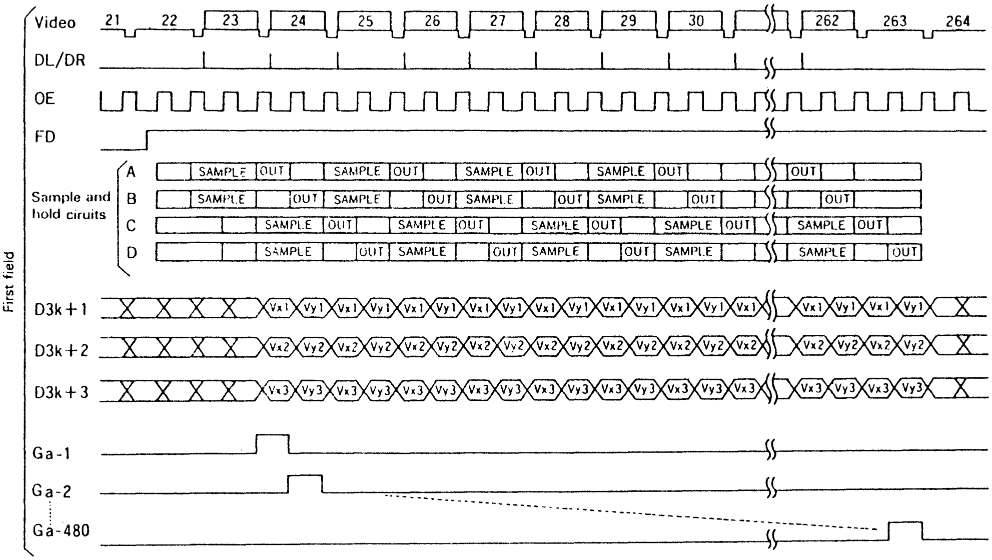


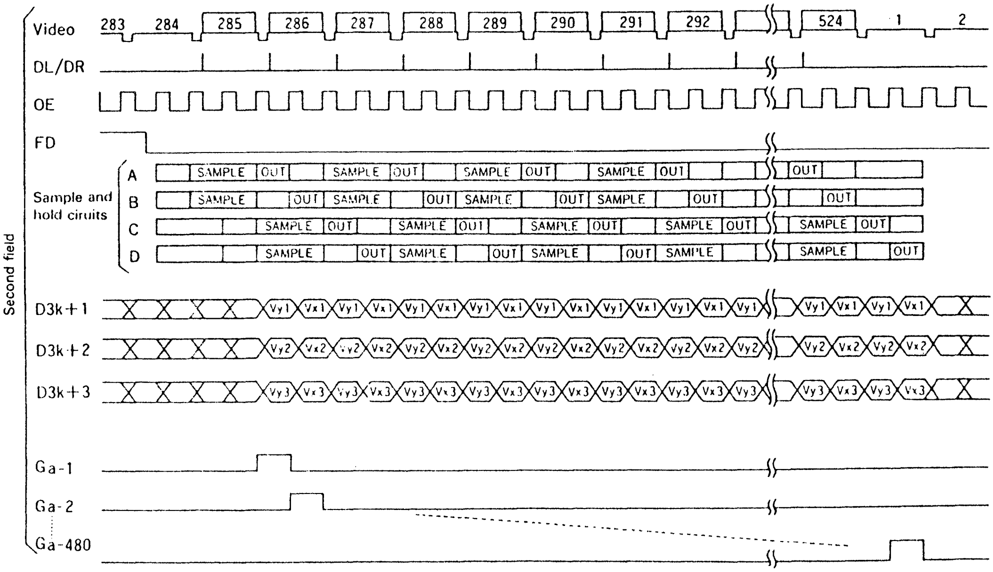


MODE 9	
D/S	V_{cc}
L/F	V_{cc}
MSF1	GND
MSF2	GND

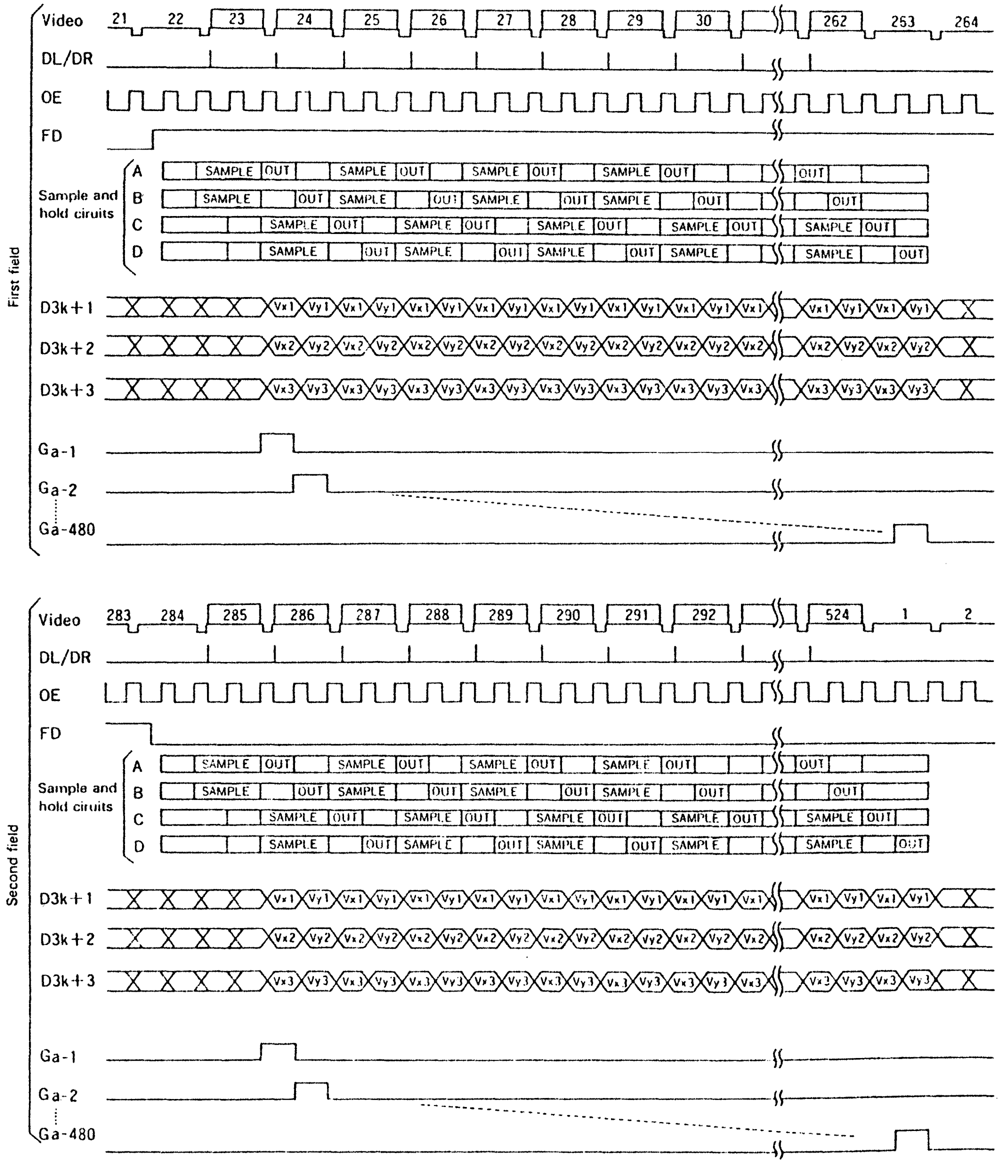


MODE10	
D/S	V_{cc}
L/F	V_{cc}
MSF1	V_{cc}
MSF2	V_{cc}

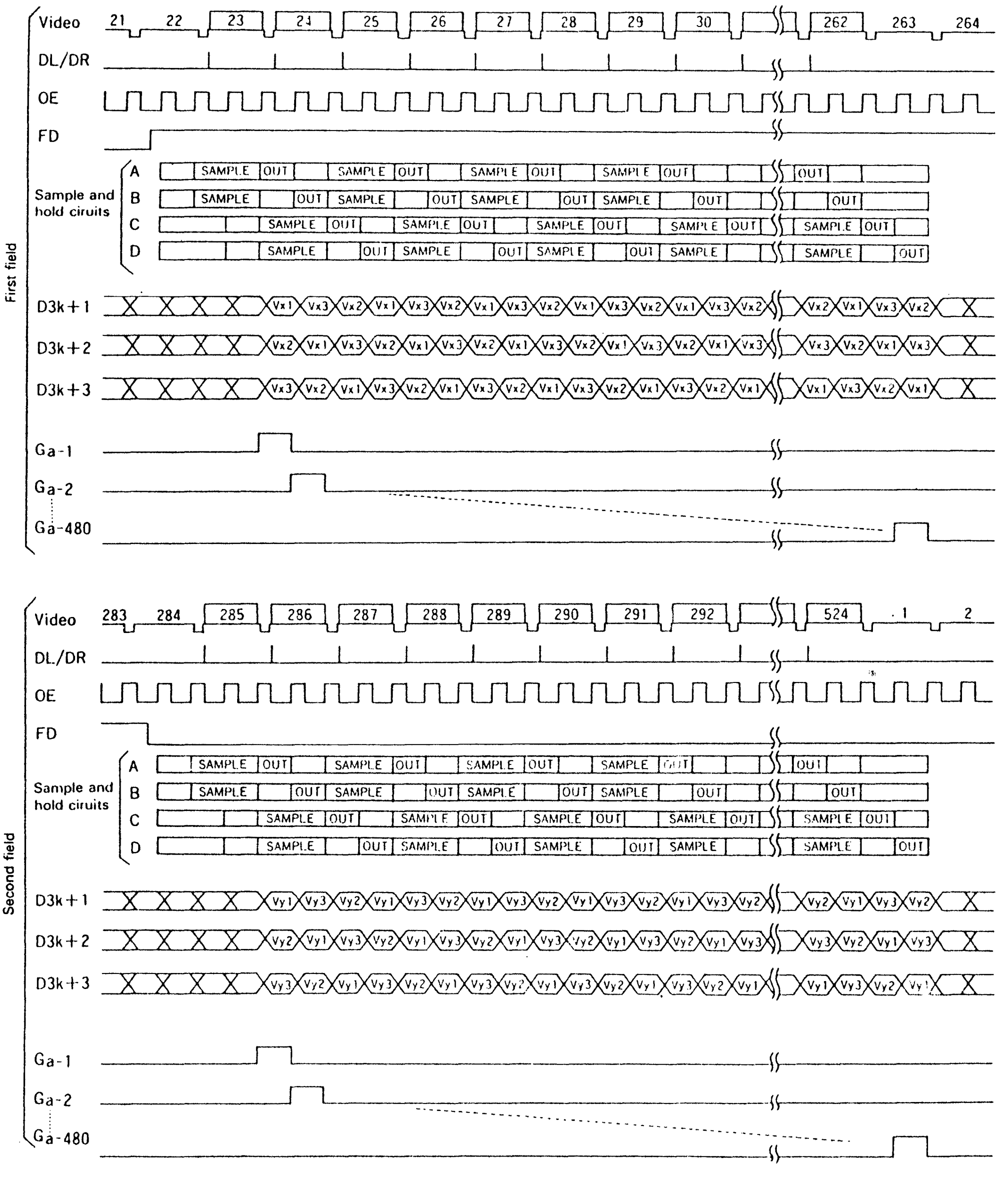




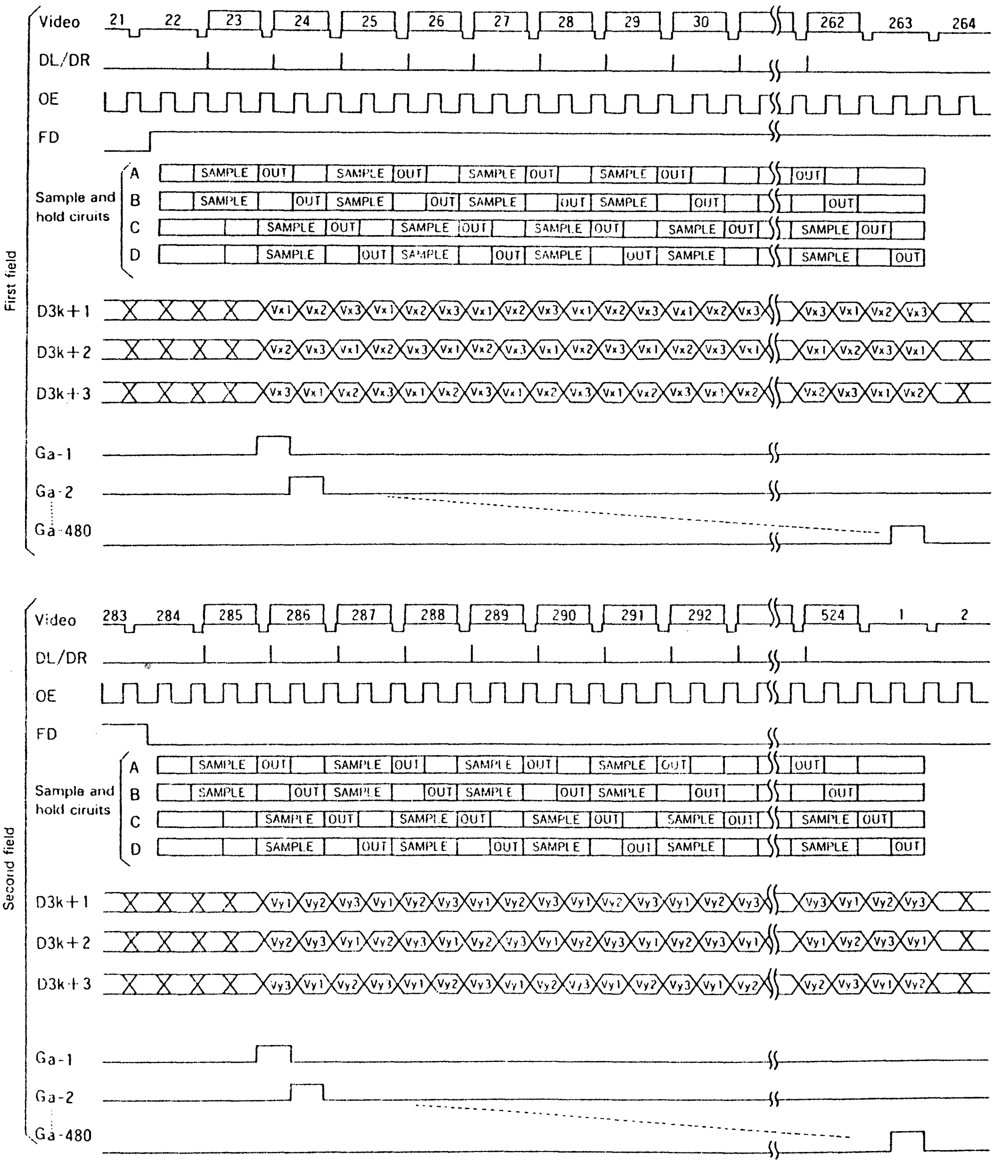
MODE11	
D/S	V_{cc}
L/F	V_{cc}/GND
MSF1	V_{cc}
MSF2	GND



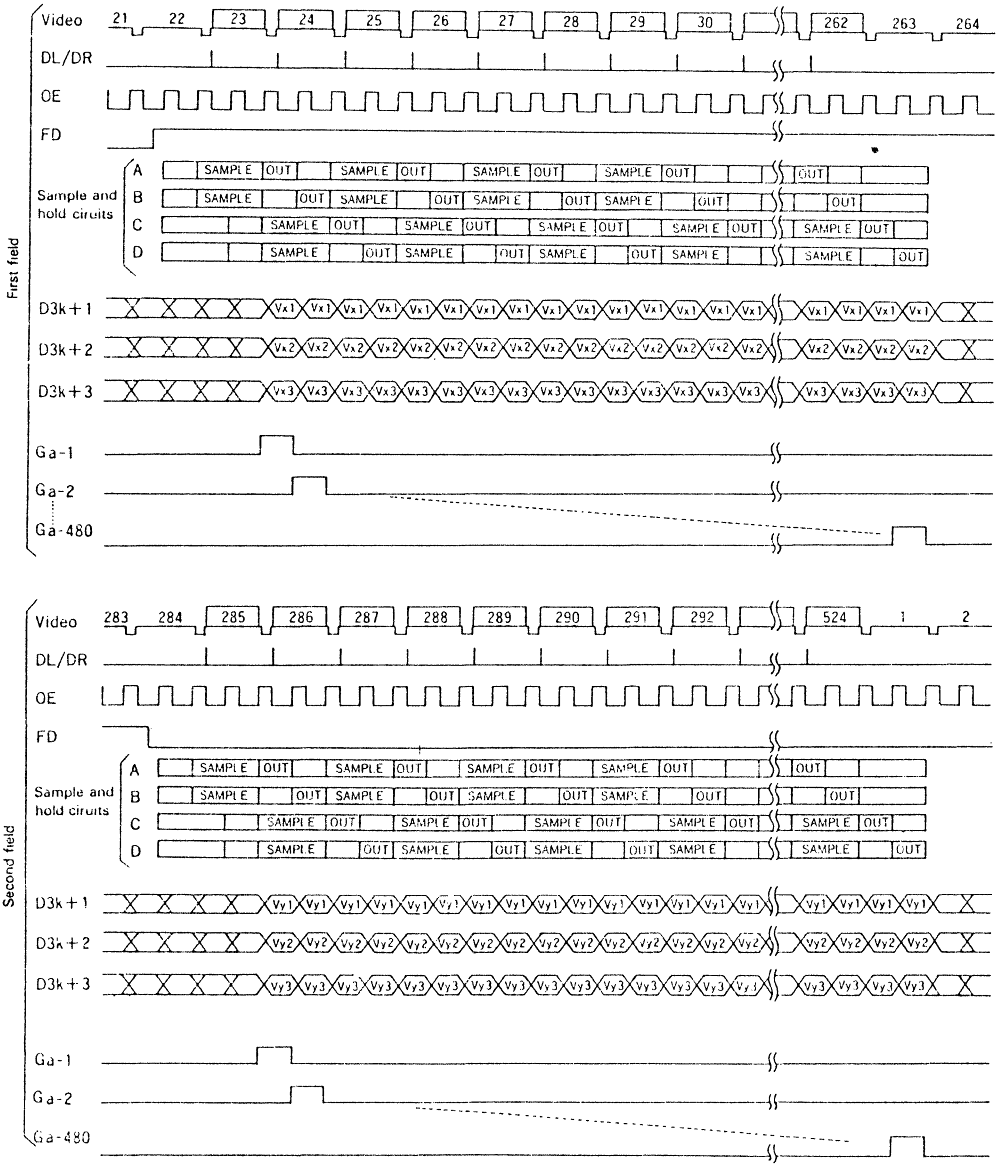
MODE12	
D/S	V_{cc}
L/F	GND
MSF1	GND
MSF2	V_{cc}



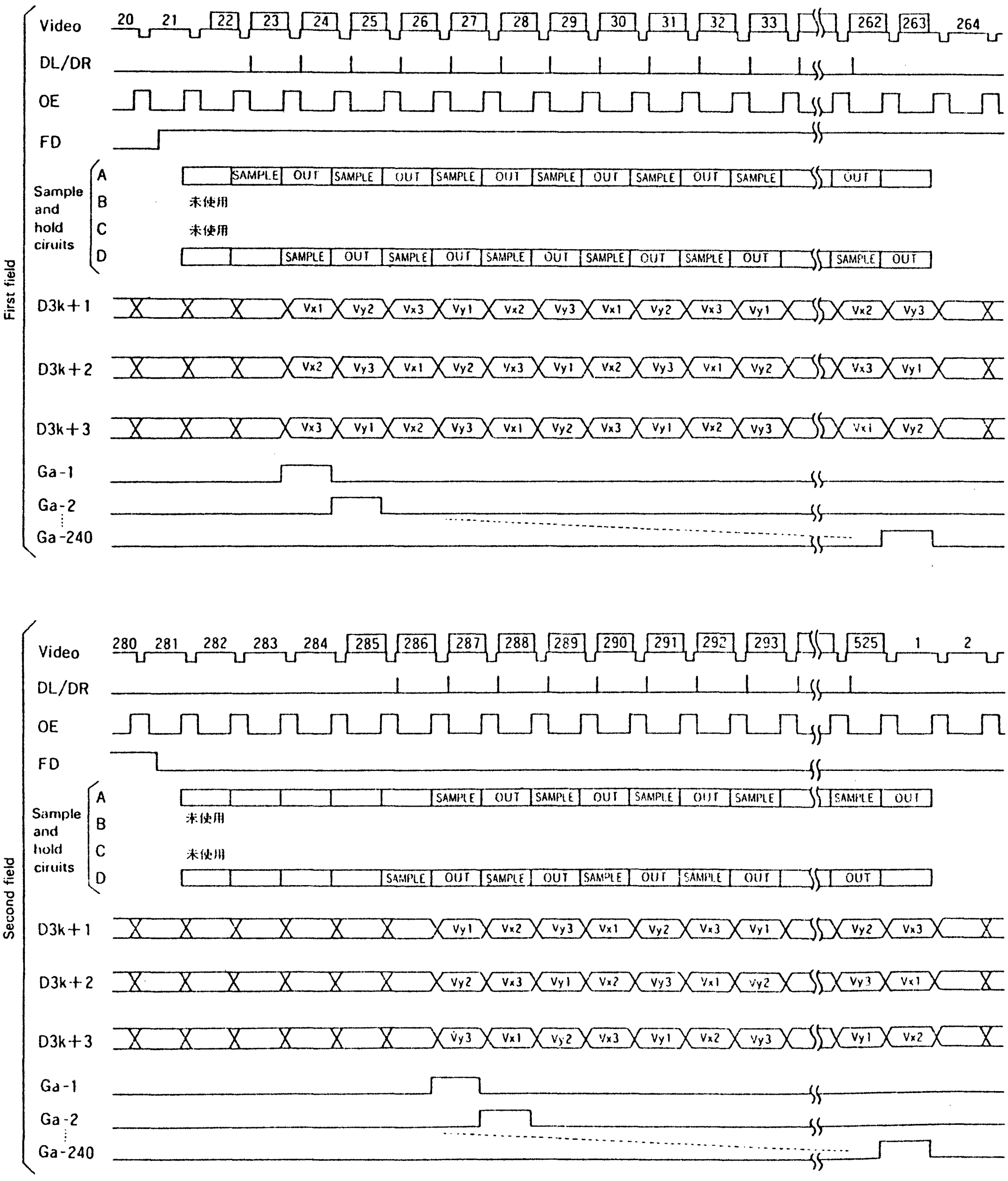
MODE13	
D/S	V_{CC}
L/F	GND
MSF1	GND
MSF2	GND



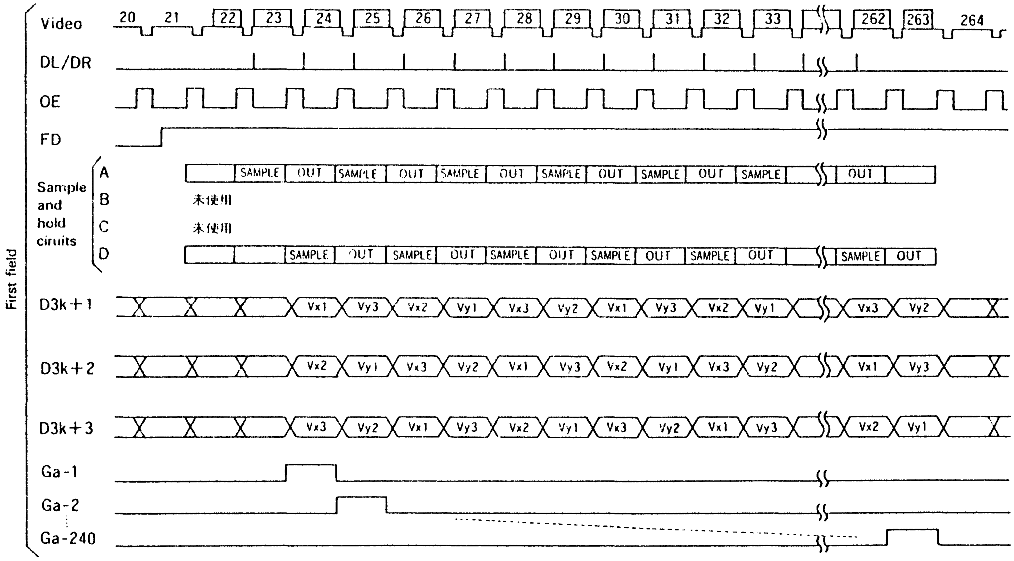
MODE14	
D/S	Vcc
L/F	GND
MSF1	Vcc
MSF2	Vcc

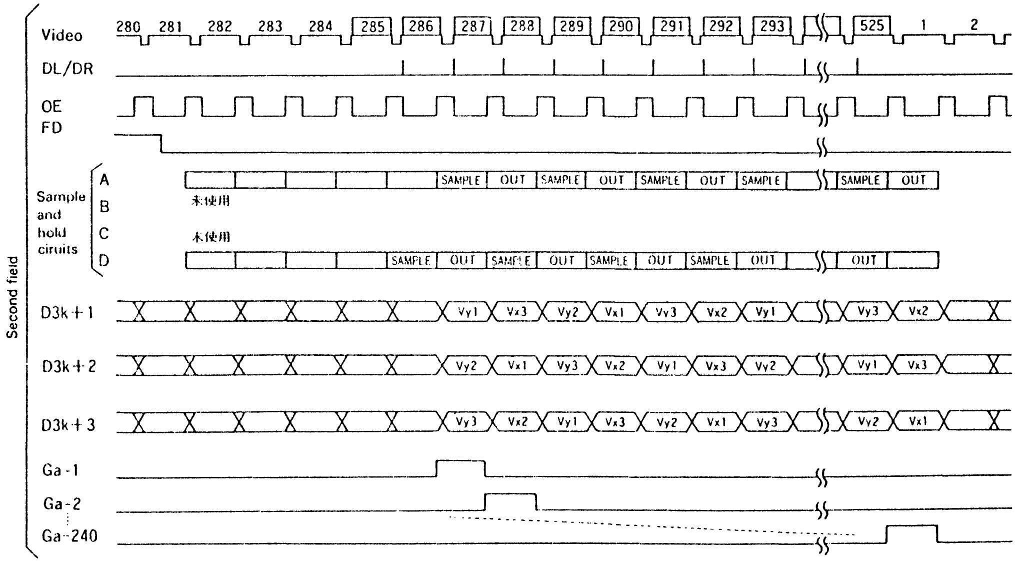


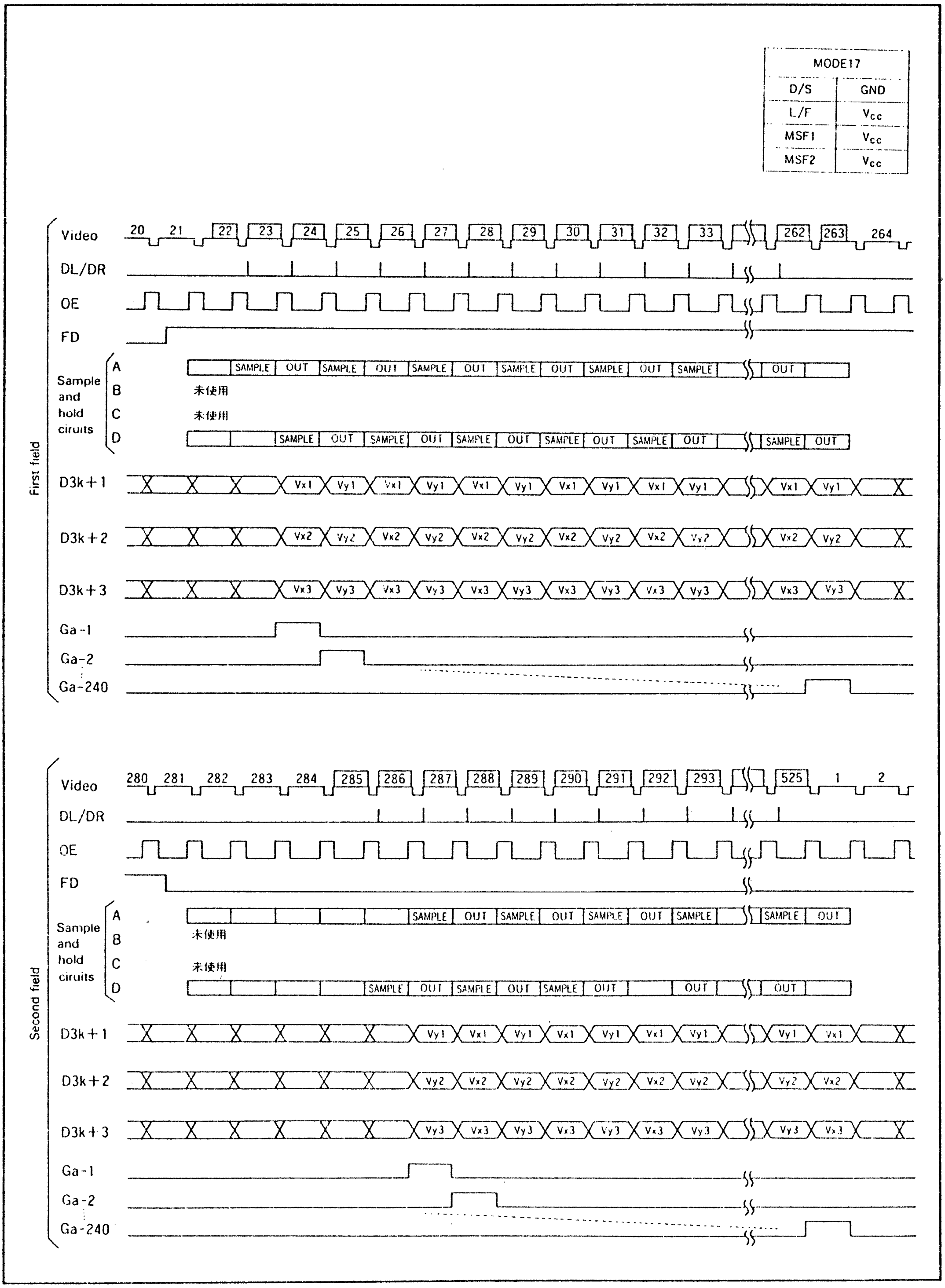
MODE15	
D/S	GND
L/F	V_{CC}
MSF1	GND
MSF2	V_{CC}



MODE16	
D/S	GND
L/F	V_{CC}
MSF1	GND
MSF2	GND

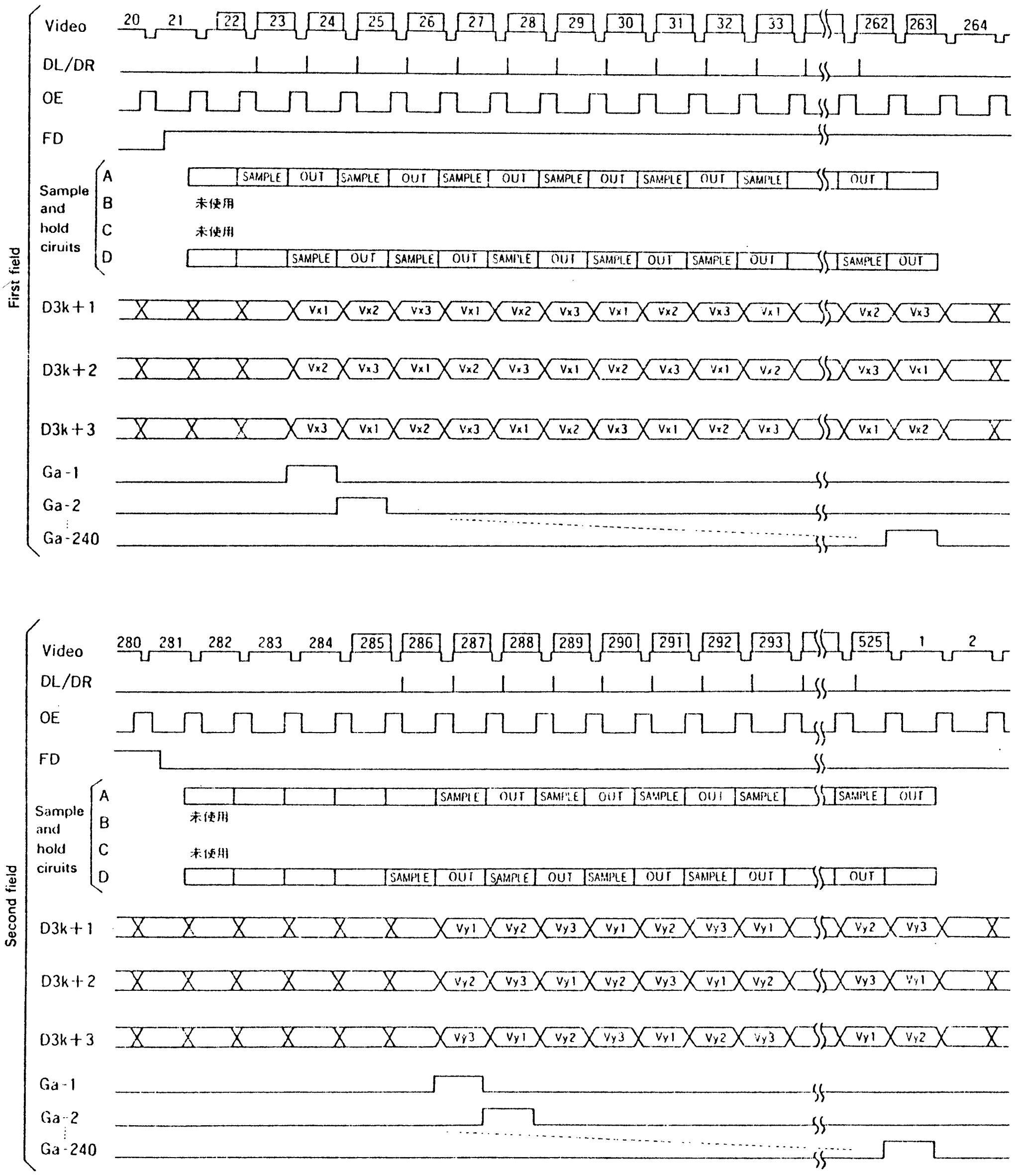




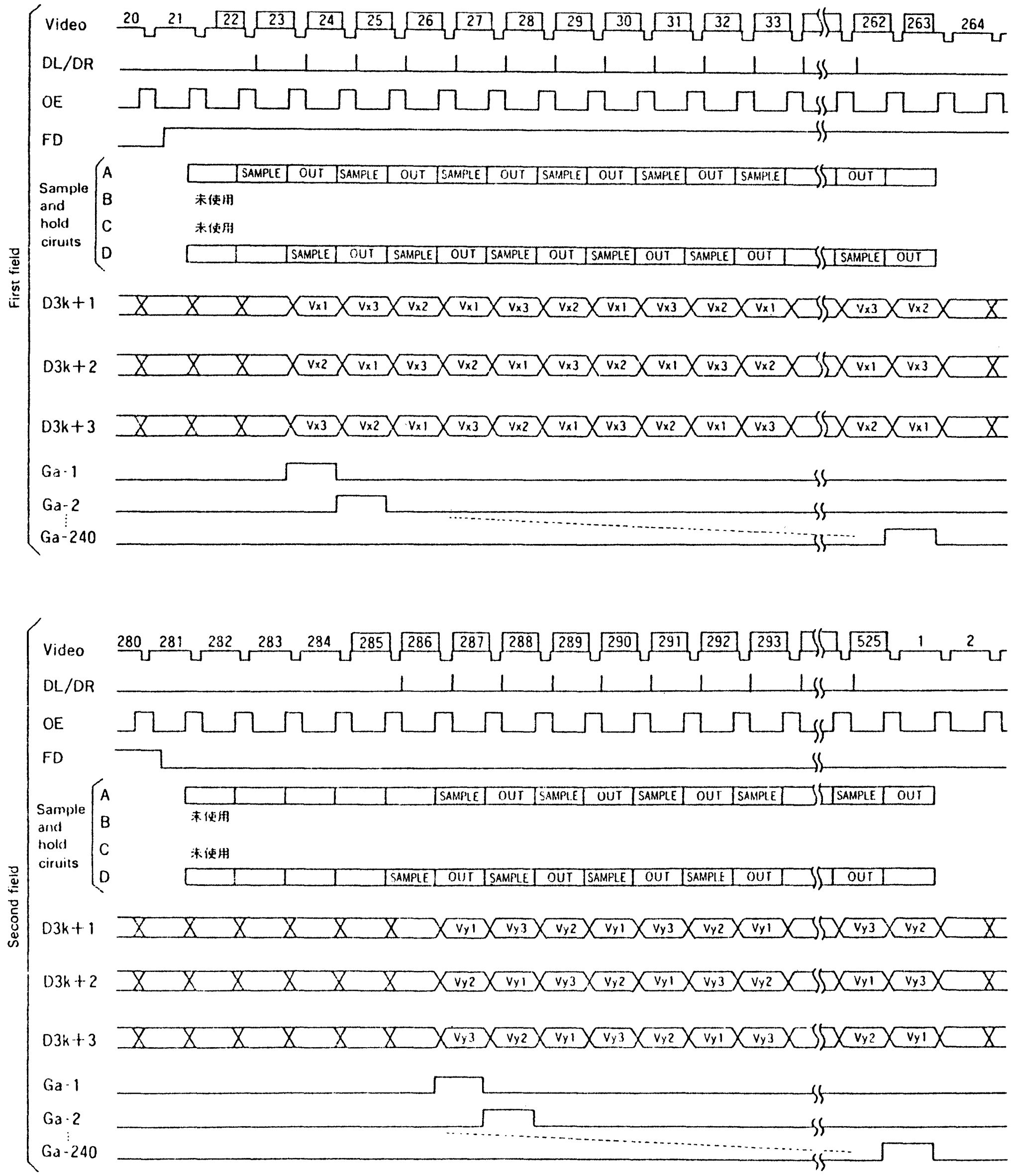


MODE17	
D/S	GND
L/F	V_{cc}
MSF1	V_{cc}
MSF2	V_{cc}

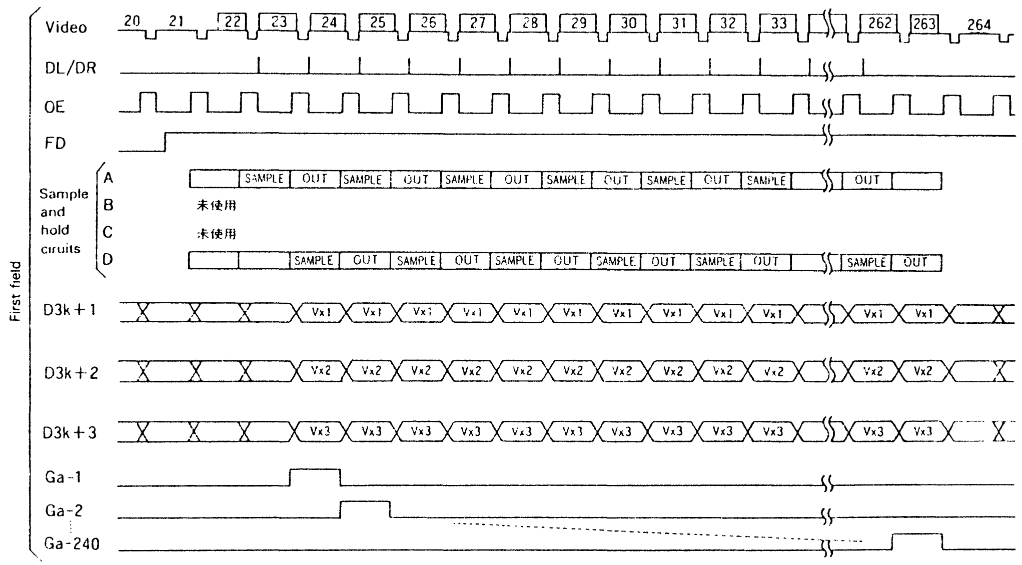
MODE18	
D/S	GND
L/F	GND
MSF1	GND
MSF2	V_{cc}

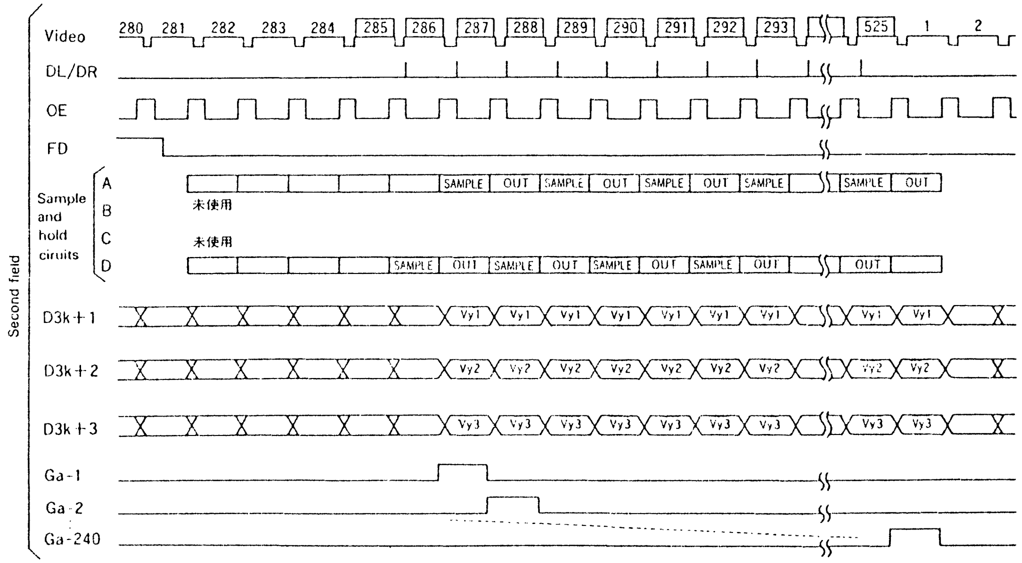


MODE19	
D/S	GND
L/F	GND
MSF1	GND
MSF2	GND



MODE20	
D/S	GND
L/F	GND
MSF1	V_{cc}
MSF2	V_{cc}





HITACHI

NTSC System TV Signals and LCD

A TV screen display, which is updated 30 times per second, is called a "frame" and is composed of 525 scanning lines. One frame contains two fields; scanning lines 1 to 262.5 scan the display in the first field, and scanning lines 262.5 to 525 scan the display in the second field to fill the gaps which are left unscanned in the first field. This scanning mode is called an "interlace scan."

The time period in which one scanning line scans the display is called a "horizontal scanning period" and is about 63.5 µs. Within the horizontal scanning period, the time period that display operation is actually performed is called the "valid display". The other period is called the "horizontal retrace period".

There are two modes for displaying a TV screen image on an LCD panel. In the first mode, each scanning line in the two fields is assigned to one line of the LCD panel; thus, each of the 240 lines of the panel are driven by the positive signal in the first field and by the negative signal in the second field. Here, 30-Hz alternating frequency is available, but the number of vertical pixels is limited to 240.

(Single-rate sequential drive mode)

In the second mode, every other line of the LCD panel can be driven by the first field and the remaining lines can be driven likewise by the second field. In this case, if one pixel of the LCD panel is considered, it is recognized that the pixel is driven by signals with opposite polarity every frame. This lowers the alternating frequency to 15 MHz, which is only half of the frame frequency. Driving LCD elements with signals of such low alternating frequency causes flickering and degrades display quality. To raise the alternating frequency to 30 MHz, a method can be employed in which LCD elements are driven once every field instead of once every frame.

Specifically, in the first field, the first and second lines of the LCD panel are driven respectively during the first half and second half of the complete horizontal scanning period. The same rule is repeated for the following lines. In the second field, on the other hand, the combination of two lines is different. The first line is driven during the second half of the horizontal scanning period, and then the second and third lines are driven respectively during the first and second half of the following horizontal scanning period. The same rule is repeated for the following lines.

Employing this method enables the implementation of 480 vertical pixels.

(Double-rate sequential drive mode)

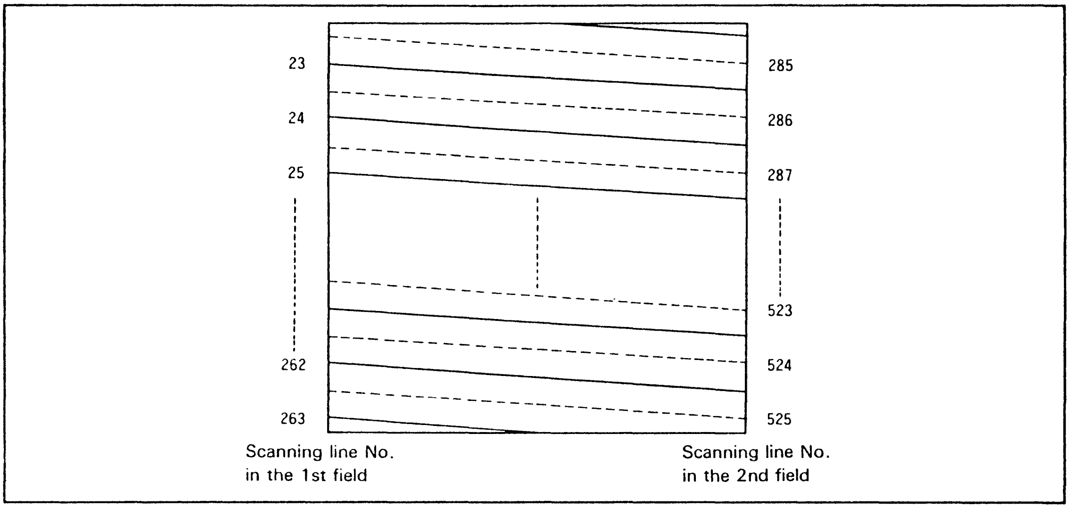


Figure 18 Example of NTSC System TV Signals Scanning

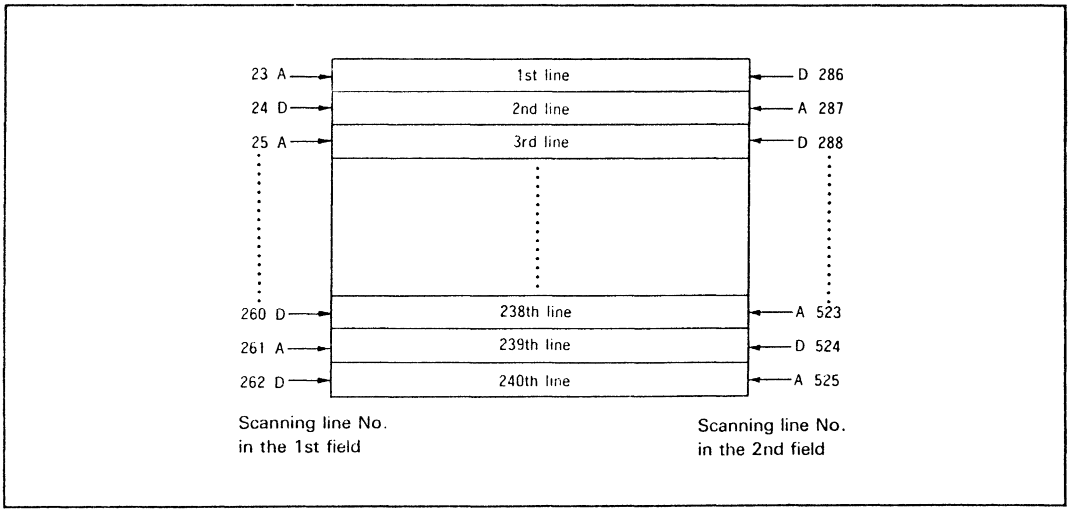


Figure 19 Middle-Resolution Display by Single-Rate Sequential Drive Mode

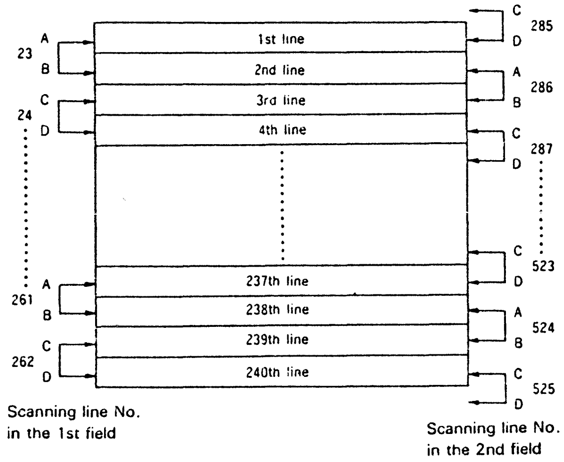


Figure 20 High-Resolution Display by Double-Rate Sequential Drive Mode

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Remarks	Note
Power supply for logic unit	V_{CC}	–0.3 to +7.0	V		
Power supply for analog unit	V_{BB}	V_{CC}– 23 to V_{CC}+ 0.3	V		
Input voltage for logic unit	V_{TC}	–0.3 to V_{CC}+ 0.3	V		3
Input voltage for analog unit	V_{TB}	V_{BB}– 0.3 to V_{CC}+ 0.3	V		4
Operating temperature	T_{opr}	–20 to +75	° C	Assures logic unit operation.	
		–10 to +60	° C	Assures analog unit operation.	
Storage temperature	T_{stg}	–20 to +85	° C		
LCD level voltage	V_{LCD}	$V_{BB}$to V_{CC}+ 0.3	V		

Notes:
1. Value referred to V_{SS} = 0 V.
2. If LSIs are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristics limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.
3. Applies to pins HCK1, HCK2, HCK3, DL, DR, FD, RS, OE, SHL, D/S, L/F, MSF1, MSF2, TEST1, TEST2, Vbo, VbsH, and VbsB.
4. Applies to pins Vx1, Vx2, Vx3, Vy1, Vy2, and Vy3.

Electrical Characteristics

DC Characteristics (V_{LCD} = V_{CC} = 5 V ±10%, GND = 0 V, V_{CC} – V_{BB} = 16 to 20 V, Ta = –20 to +75 °C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Input high-level voltage	V_{IH}	0.7 V_{CC}		V_{CC}	V		3
Input low-level voltage	V_{IL}	GND		0.3V_{CC}	V		
Output high-level voltage	V_{OH}	V_{CC} – 0.4			V	–I_{OH} = 0.3 mA	4
Output low-level voltage	V_{OL}			0.4	V	I_{OH} = 0.3 mA	
Input leakage current (1)	I_{LI1}	–10		+10	µA	VI = 0 V, V_{CC}	1
Input leakage current (2)	I_{LI2}	–10		+10	µA	VI = V_{BB}, V_{CC}	2
Output current (1)	I_{OUT}			–150	µA	V_{CC} - V_{BB} = 20 V Dk = V_{in} – 0.5 V OE = V_{CC}	5
				–10	µA	Apply V_{in} to Vx and Vy. V_{in} = (V_{CC} = V_{BB})/2 OE =	
Output current (2)	I_{IN}	+150			µA	GND V_{bo} = V_{CC} – 3 V DK = V_{in} + 0.5 V OE = V_{CC}	
		+10			µA	V_{bsH} = V_{CC} – 3 V V_{bsB} = V_{CC} - 3 V DK = V_{in} + 0.5 V OE = GND	
Current consumption	I_{GND}			3.0	mA	f_{ck} = 2.5 MHz, V_{bo} = V_{CC} – 3 V	6
	I_{BB}		15	30	mA	V_{bsH} = VCC – 3 V, V_{bsB} = V_{CC} - 3 V OE = 33 kHz, FD = 30 Hz OE duty = 7/32	
Bias voltage	V_b	V_{CC} – 4.0	V_{CC} – 3.0		V	V_{bo} = V_{bsH} = V_{bsB}, CL = 100 pF, T_{DDR} < 6.3 µs	
Dynamic range	V_{DY}	V_{BB} + 1.5		V_{CC} – 3.5	V	V_{CC} – V_{BB} = 20 V, T_a = –10 to +60°C –0.5 V < V_{off} < +0.5 V V_{bo} = V_{bsH} = V_{bsB} = V_{CC} – 3 V	5, 7
Offset voltage	$V_{off\ (L)}$	–5 – 180		–5 + 180	mV	V_{CC} – V_{BB} = 20 V V_{in} = –11 V T_a = –10 to + 60°C	5, 8
	$V_{off\ (H)}$	+55 – 180		+55 + 180	mV	f_{ck} = 2.5 MHz V_{in} = –1 V V_{bo} = V_{bsH} = V_{bsB} = V_{CC} – 3 V	

Notes:
1. Applies to pins HCK1, HCK2, HCK3, DL, DR, FD, RS, OE, SHL, D/S, L/F, MSF1, MSF2, TEST1, TEST2, V_{bo}, V_{bsH}, and V_{bsB}.
2. Applies to pins Vx1, Vx2, Vx3, Vy1, Vy2, and Vy3.
3. Applies to pins HCK1, HCK2, HCK3, DL, DR, FD, RS, OE, SHL, D/S, L/F, MSF1, MSF2, TEST1, and TEST2.
4. Applies to pins DL and DR.
5. Applies to pins D1 - D120.
6. The shift register is constantly shifting one 1.
   Mode setting: $L/\overline{F} = V_{CC}$, $D/\overline{S} = V_{CC}$, MSF1 = GND, MSF2 = V_{CC}
   (The other input pins must be V_{CC} or GND level.)
7. The operations are the same as those when offset voltage is measured.
8. Definition of "offset voltage" is shown figure 21.

AC Characteristics ($V_{LCD} = V_{CC} = 5$ V ± 10%, GND = 0 V, $V_{CC} - V_{BB} = 16$ to 20 V, $T_a = -20$ to +75°C)

		Ratings				
Item	**Symbol**	**Min**	**Max**	**Unit**	**Test Condition**	**Notes**
Three-phase clock period	t_{CKCK}	210	1000	ns		
Three-phase clock pulse width	t_{CWH} t_{CWL}	100		ns		
Interval between three-phase clock falling edge and rising edge	t_{fr1} t_{fr2} t_{fr3}	30		ns		1
Interval between three-phase clock rising edge and falling edge	t_{rf}	20		ns		2
Clock rise and fall times	t_{CT}		30	ns		
DL, DR input setup time	t_{SU}	50		ns		
DL, DR input hold time	t_{HLI}	20		ns		
DL, DR output delay time	t_{pd}		90	ns	CL = 15 pF	
DL, DR output hold time	t_{HLO}	5		ns		
OE input period	t_{CYCO}	30	80	µs		
OE input high-level pulse width	t_{OWH}	3	15	µs		
OE rise and fall times	t_{or} t_{of}		30	ns		
FD input setup time	t_{FS}	100		ns		
FD input hold time	t_{FH}	100		ns		

Note:
1. Necessary for preventing the three-phase shift register from racing.
2. t_{rf} must satisfy the DR and DL input hold time (t_{HLI}) of the next horizontal driver. ($t_{rf} + t_{HLO} > t_{HLI}$)

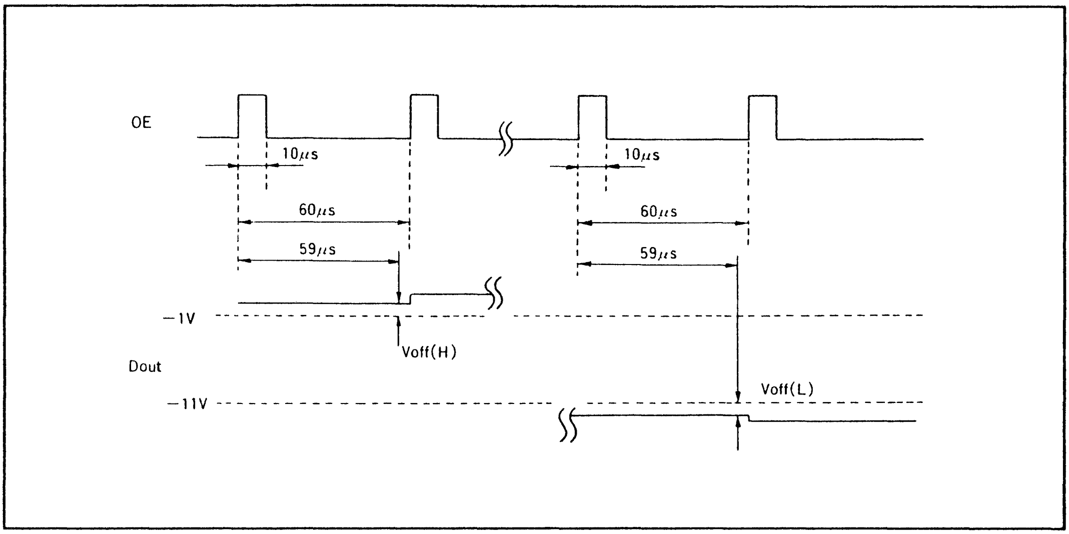


Figure 21 Offset Voltage

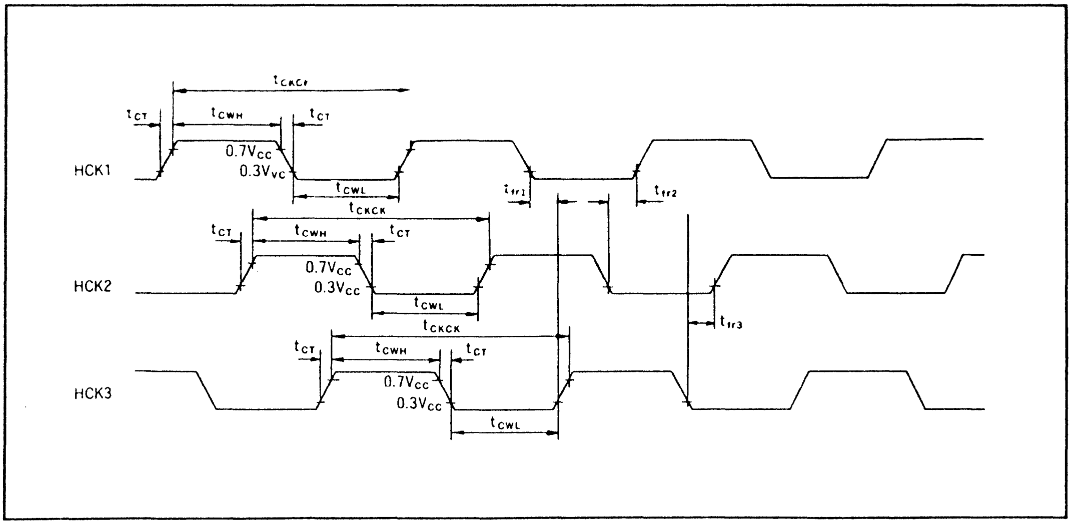


Figure 22 Three-Phase Clock Timing

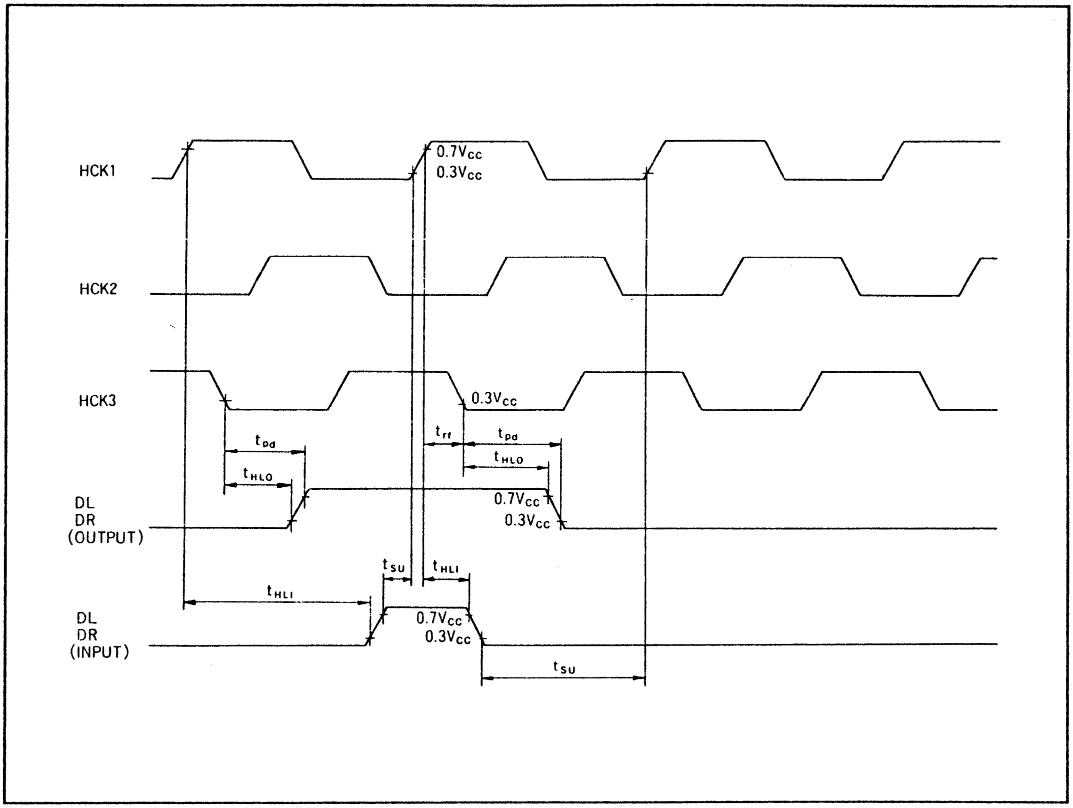


Figure 23 Input and Output Timing

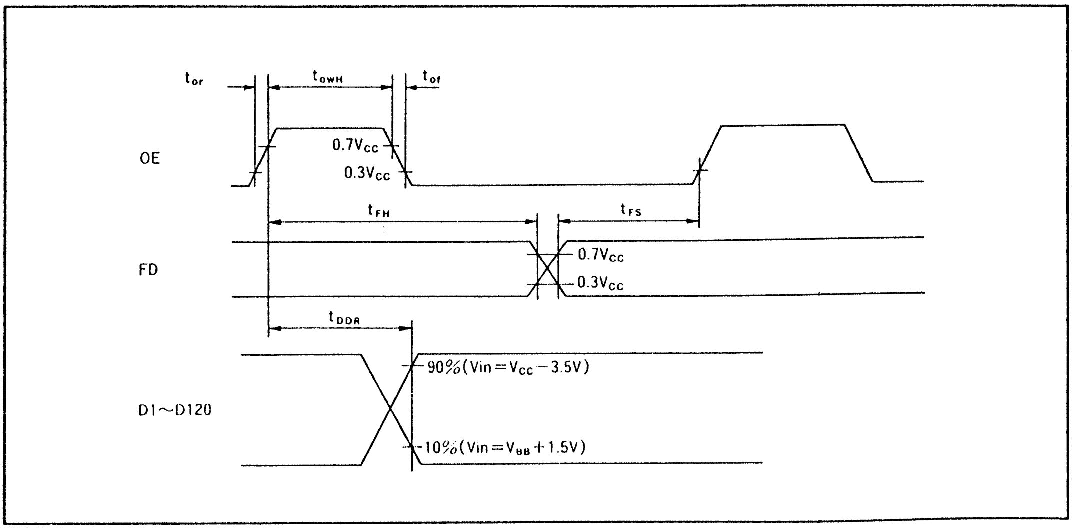
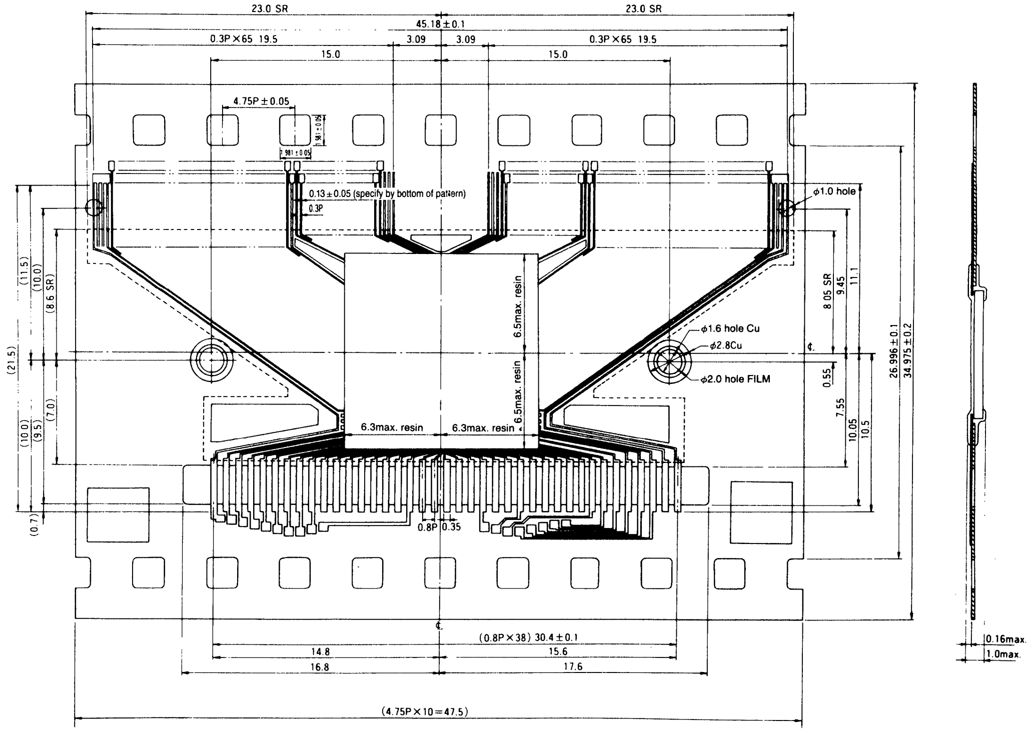


Figure 24 OE, FD Input Timing, Driver Output Timing

Package Dimensions

Unit: mm (inch)



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Section Three

HD66840 Video Interface Controller (LVIC) Application Note

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For additional information reference:

Section 1. LCD Controller/Driver LSI Data Book
Section 2. HD66300T Horizontal Driver for TFT-Type LCD Color TV
Section 4. HD63645F/HD64645F LCD Timing Controller (LCTC) Application Note
Section 5. HD63645/HD64645/HD64646 LCD Timing Controller (LCTC) User's Manual

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Section 1 LVIC Overview

1.1 Description

The HD66840 LVIC (LCD Video Interface Controller) converts the standard RGB video signals for CRT display into LCD data. It enables a CRT display system to be replaced by an LCD system without any changes. It also enables software that was originally intended for CRT display to control an LCD.

The LVIC features a high operating frequency of 30 MHz, corresponding to the CRT display dot clock (DOTCLK). It enables screen size programming and control of a large-panel LCD of up to 720 × 512 dots.

Since the LVIC can control TFT-type LCDs in addition to the current TN-type LCDs, it can support monochrome, 8-level gray scale, and 8-color displays.

1.2 Features

- Conversion of RGB video signals for CRT display into LCD data:
  - Monochrome display data
  - 8-level gray scale data
  - 8-color display data
- Selectable LVIC control method:
  - Pin programming method
  - Internal register programming method (using either an MPU or ROM)
- Programmable screen size:
  - 640 or 720 dots (80 or 90 characters) in width and 200, 350, 400, 480, 512, or 540 dots (lines) in height, using the pin programming method
  - 32 to 4048 dots (4 to 506 characters) in width and 4 to 1024 dots (lines), using the internal register programming method
- Double-height display capability
- Generation of a display timing signal (DISPTMG) from the horizontal synchronization (HSYNC) and the vertical synchronization (VSYNC) signals
- Internal PLL circuit capable of generating the CRT display dot clock (DOTCLK) (external charge pump, low-pass filter (LPF), and voltage-controlled oscillator (VCO) required)
- Both TN-type LCDs and TFT-type LCDs controllable

- Maximum operating frequency: 30 MHz (DOTCLK)
- LCD driver interface: 4-, 8-, or 12-bit (4 bits for each of R, G, and B) parallel data transfer
- Recommended LCD drivers: HD61104, HD61105, HD66106, and HD66107T
- Direct interface with buffer memory (no external decoder required)
- CMOS 1.3 µm process
- Single power supply: +5 V ±5%
- 100-pin quad flat package (FP-100A)

1.3 System Configuration

Figure 1-1 shows a basic system configuration using the LVIC.

The LVIC converts RGB serial data sent from a personal computer into parallel data and temporarily writes it to the buffer memory. It reads out the data in sequence and outputs it to LCD drivers to drive an LCD. In this case, a CRT display dot clock (DOTCLK), which is the latch clock for serial data, is generated by a PLL circuit from the horizontal synchronization signal (HSYNC). The DOTCLK signal frequency is specified by PLL frequency-division register (R10 and R11). A display timing signal (DISPTMG) is generated internally from the HSYNC and VSYNC (vertical synchronization) signals. The information required for generating the DISPTMG signal is given by horizontal back porch register (R14 and R15) and vertical back porch register (R12 and R13). The MPU is used for writing this data into the LVIC's internal registers.

A system may be configured without a VCO and an LPF if the DOTCLK signal is supplied externally, and a system may be configured without an MPU if the LVIC is controlled by the pin programming method.

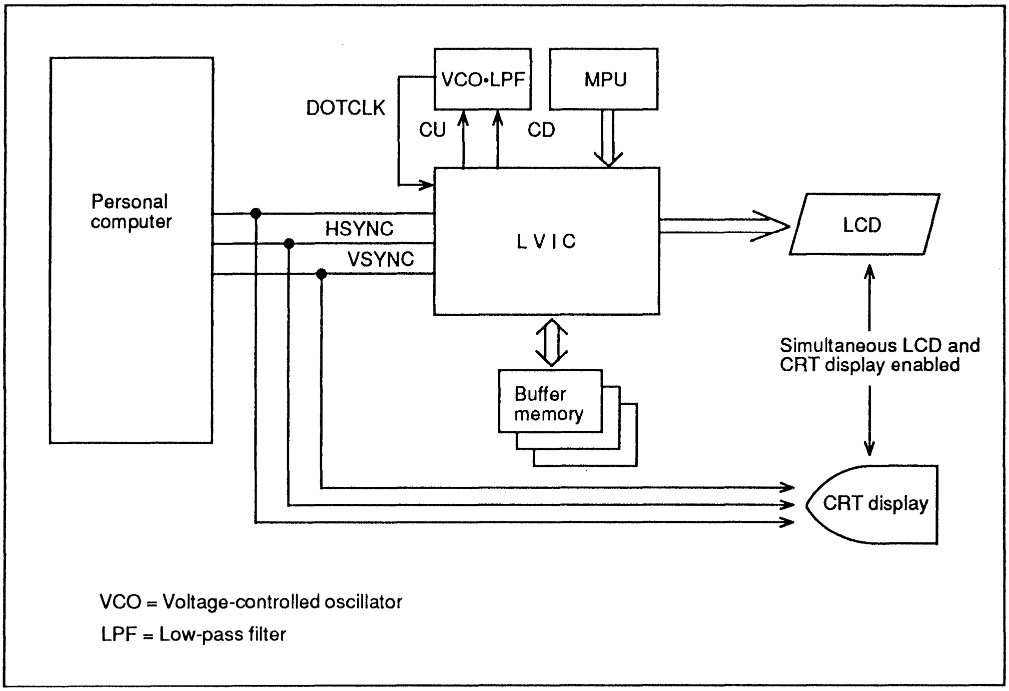


Figure 1-1 Basic System Configuration (Using MPU Programming Method and Generated DOTCLK and DISPTMG Signals)

1.4 LVIC Configuration

Figure 1-2 is the internal block diagram of the LVIC. The functions of each block are described below.

1.4.1 Dot Clock Generator (Programmable Counter and Phase Comparator)

The dot clock generator generates a CRT display dot clock (DOTCLK) in conjunction with an external charge pump, a low-pass filter (LPF), and a voltage-controlled oscillator (VCO) when the DOTCLK signal is not supplied externally.

1.4.2 Display Timing Signal Generator

The display timing signal generator generates a display timing signal (DISPTMG). The DISPTMG signal indicates which RGB data is valid of all the video data sent from a video controller. This generator adjusts the phase shift between the DISPTMG signal and the valid RGB data when the DISPTMG signal is not supplied externally.

1.4.3 CRT Display (Video Signal) and Buffer Memory Interface Unit

This unit converts serial RGB data into parallel data and writes it to buffer memory.

1.4.4 Timing Clock Generator

The timing clock generator generates various clock signals which control the LVIC's internal operations.

1.4.5 Write Address Counter

The write address counter generates memory addresses which enable the LVIC to write data sent from a video controller to buffer memory.

1.4.6 Read Address Counter

The read address counter generates memory addresses which enable the LVIC to read data to be sent to LCD drivers from buffer memory.

1.4.7 Address Multiplexer

The address multiplexer controls the output of the read address counter and the write address counter. The multiplexer allows the read address counter to output an address in a read cycle, and the write address counter to output an address in a write cycle.

1.4.8 $\overline{\text{MCS}}$ and $\overline{\text{MWE}}$ Signal Generator

The $\overline{\text{MCS}}$ and $\overline{\text{MWE}}$ signal generator generates a buffer memory chip select signal ($\overline{\text{MCS}}$) and a buffer memory write enable signal ($\overline{\text{MWE}}$).

1.4.9 Synchronizer (Data Latch Circuit)

The CRT display (video signal) interface unit of the LVIC writes data to or reads data from buffer memory synchronized by the CRT display dot clock (DOTCLK), while the LCD interface unit (refer to section 1.4.11) operates synchronized by the LCD dot clock (LDOTCK). Since these two clocks operate asynchronously, the synchronizer synchronizes the data transfer timing of the two interface units.

1.4.10 Gray Scale Display Data Generator

The gray scale display data generator converts RGB signals into 8-level gray scale display data.

1.4.11 LCD Interface Unit

The LCD interface unit transfers LCD data to LCD drivers in parallel in 4-, 8-, or 12-bit units, depending on the display mode.

1.4.12 LCD Timing Signal Generator

The LCD timing signal generator generates LCD control timing clocks CL1, CL2, CL3, CL4, FLM, and M.

1.4.13 MPU/ROM Interface Unit and Display Mode Decoder

MPU Interface Unit: Receives control signals from an MPU, and transfers internal register data to and from the MPU.

ROM Interface Unit: Outputs addresses to ROM and receives data to be written into internal registers from the ROM.

Display Mode Decoder: Selects one out of 16 display modes, depending on the input through the DM3–DM0 pins.

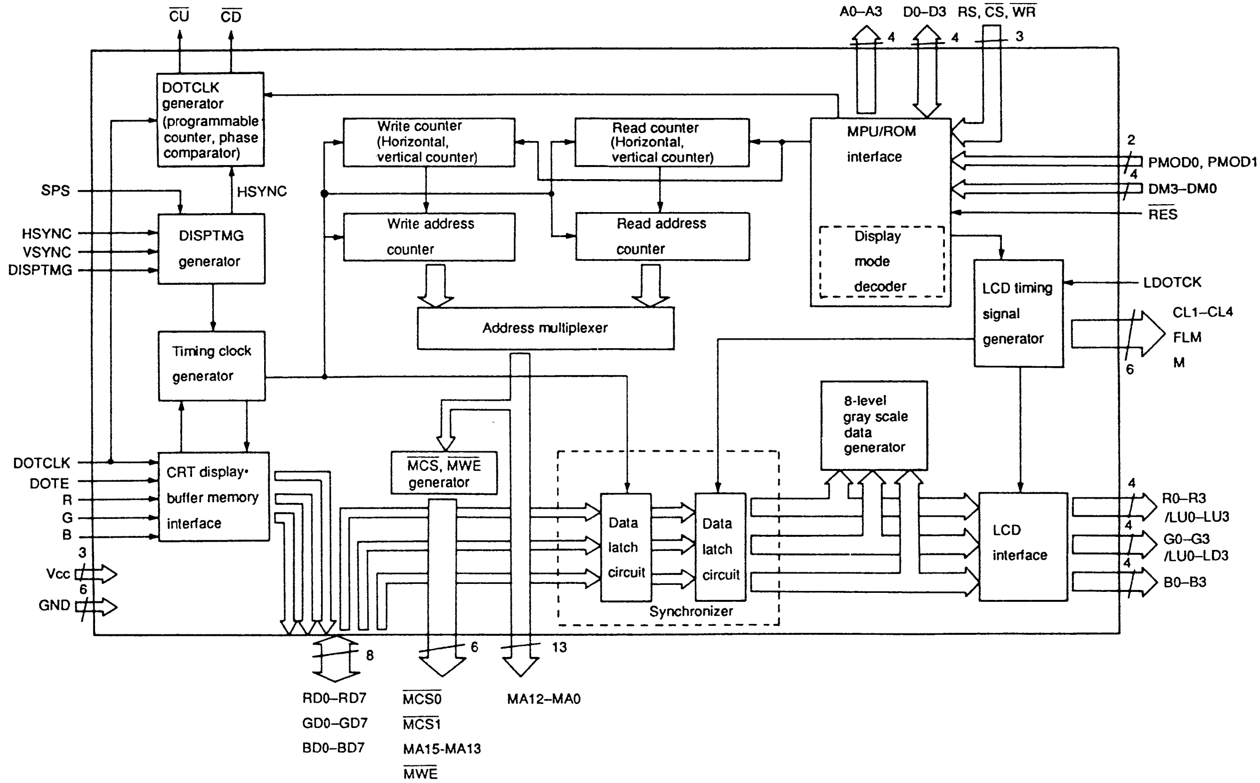


Figure 1-2 Internal Block Diagram

SECTION 3

1.5 Pin Description

The LVIC pins are divided into power supply pins, video signal interface pins, LCD interface pins, buffer memory interface pins, mode setting pins, MPU interface pins, ROM interface pins, and PLL interface pins.

Figure 1-3 shows the LVIC pin arrangement and table 1-1 provides a complete listing of the pins.

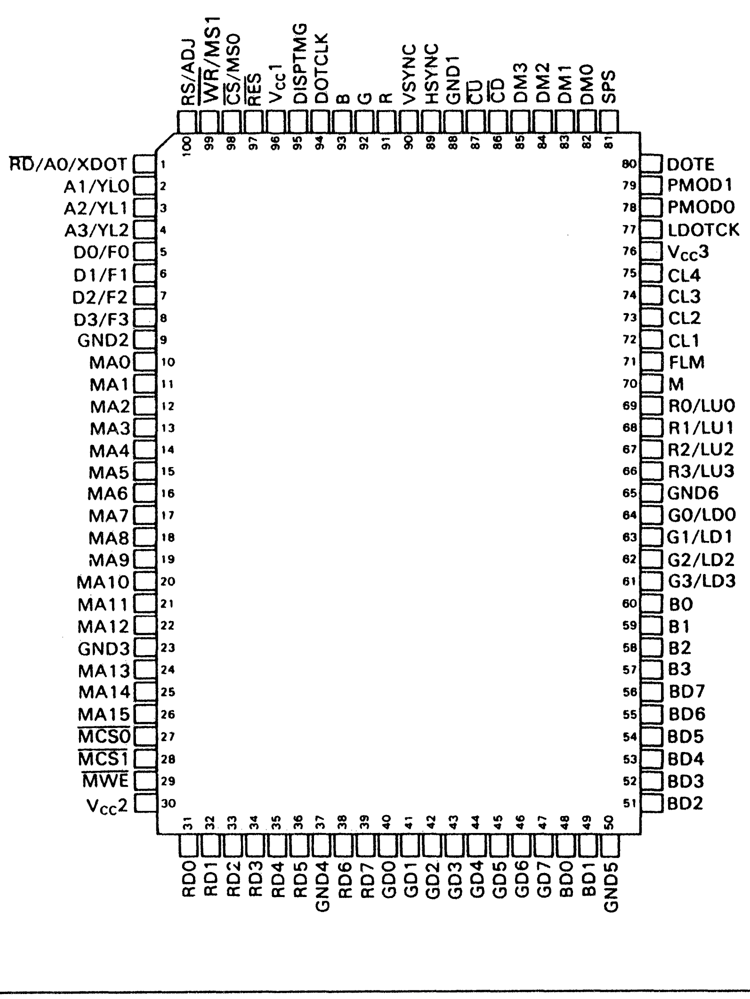


Figure 1-3 Pin Arrangement

Table 1-1 Pins

Classification	Symbol	Pin Number	Pin Name	I/O
Power Supply	Vcc1, Vcc2, Vcc3	96, 30, 76	Vcc1, Vcc2, Vcc3	—
	GND1, GND2, GND3, GND4, GND5, GND6	88, 9, 23, 37, 50, 65	Ground1, ground2, ground3, ground4, ground5, ground6	—
Video Signal Interface	R, G, B	91, 92, 93	Red, green, blue serial data	I
	HSYNC	89	Horizontal synchronization	I
	VSYNC	90	Vertical synchronization	I
	DISPTMG	95	Display timing	I
	DOTCLK	94	Dot clock	I
LCD Interface	R0–R3	69–66	LCD red data 0–3	O
	LU0–LU3	69–66	LCD upper panel data 0–3	O
	G0–G3	64–61	LCD green data 0–3	O
	LD0–LD3	64–61	LCD lower panel data 0–3	O
	B0–B3	60–57	LCD blue data 0–3	O
	CL1	72	LCD data latch clock	O
	CL2	73	LCD data shift clock	O
	CL3	74	Y-driver shift clock 1	O
	CL4	75	Y-driver shift clock 2	O
	FLM	71	First line marker	O
	M	70	LCD driving signal alternation	O
	LDOTCK	77	LCD dot clock	O
Buffer Memory Interface	$\overline{\text{MCS0}}$, $\overline{\text{MCS1}}$	27, 28	Memory chip select 0, 1	O
	$\overline{\text{MWE}}$	29	Memory write enable	O
	MA0–MA15	10–22, 24–26	Memory address 0–15	O
	RD0–RD7	31–36, 38, 39	Memory red data 0–7	I/O
	GD0–GD7	40–47	Memory green data 0–7	I/O
	BD0–BD7	48, 49, 51–56	Memory blue data 0–7	I/O
Mode Setting	PMOD0, PMOD1	78, 79	Program mode 0, 1	I
	DOTE	80	Dot clock edge change	I
	SPS	81	Synchronization polarity select	I
	DM0–DM3	82–85	Display mode 0–3	I
	MS0, MS1	98, 99 (Note)	Memory select 0, 1	I
	XDOT	1 (Note)	X-dot	I
	YL0–YL2	2–4 (Note)	Y-line 0–2	I
	ADJ	100 (Note)	Adjust	I
	F0–F3	5–8 (Note)	Fine adjust 0–3	I

Table 1-1 Pins (cont.)

Classification	Symbol	Pin Number	Pin Name	I/O
MPU Interface	$\overline{\text{CS}}$	98 (Note)	Chip select	I
	$\overline{\text{WR}}$	99 (Note)	Write	I
	$\overline{\text{RD}}$	1 (Note)	Read	I
	RS	100 (Note)	Register select	I
	D0–D3	5–8 (Note)	Data 0–3	I/O
	$\overline{\text{RES}}$	97	Reset	I
ROM Interface	A0–A3	1–4 (Note)	Address 0–3	O
	D0–D3	5–8 (Note)	Data 0–3	I
PLL Interface	$\overline{\text{CD}}$	86	Charge down	O
	$\overline{\text{CU}}$	87	Charge up	O

Note: Common pins shared by more than one signal (refer to table 1-2).

Table 1-2 Common Pins and Signal Names

	Signal Name by Classification			
Pin No.	MPU Interface	ROM Interface	Mode Setting	Handling When not in Use
1	$\overline{\text{RD}}$	A0	XDOT	—
2–4	Not used	A1–A3	YL0–YL2	Fix high or low
5–8	D0–D3	D0–D3	F0–F3	—
98	$\overline{\text{CS}}$	Not used	MS0	Fix high or low
99	$\overline{\text{WR}}$	Not used	MS1	Fix high or low
100	RS	Not used	ADJ	Fix high or low

1.5.1 Power Supply Pins

Vcc1–Vcc3 (Pins 96, 30, and 76): These pins are power supply pins and must all be connected to +5 V. When attaching an external PLL circuit, connect a thick cable to the Vcc3 pin and isolate it from Vcc1 and Vcc2.

GND1–GND6 (Pins 88, 9, 23, 37, 50, and 65): These pins are ground pins and must all be grounded. When attaching an external PLL circuit, connect a thick cable to the GND6 pin and isolate it from GND1–GND5.

1.5.2 Video Signal Interface Pins

R, G, B (Input, Pins 91, 92, and 93): Input RGB CRT display signals. When CRT display data is monochrome, input the data to the R pin and fix the G and B pins low.

HSYNC (Input, Pin 89): Inputs the CRT horizontal synchronization signal.

VSYNC (Input, Pin 90): Inputs the CRT vertical synchronization signal.

DISPTMG (Input, Pin 95): Inputs the display timing signal which indicates horizontal or vertical display period. When the display timing signal is internally generated, fix this pin either high or low.

DOTCLK (Input, Pin 94): Inputs the CRT display dot clock.

1.5.3 LCD Interface Pins

R0–R3/LU0–LU3 (Output, Pins 69–66), G0–G3/LD0–LD3 (Output, Pins 64–61), B0–B3 (Output, Pins 60–57): These pins all output LCD data. Connect them to the display data input pins of X-drivers (column drivers). The specific type of data output by these pins depends on the display color, screen configuration, and size of data transfer (table 1-3).

Table 1-3 LCD Data Output

	Monochrome or 8-Level Gray Scale Display			**8-Color Display**
	Single Screen		**Dual Screen**	**Single Screen**
Pins	**4-Bit Transfer**	**8-Bit Transfer**	**4-Bit Transfer**	**12-Bit Transfer**
LU0–LU3/ R0–R3	Data output	Data output	Upper panel data output	R data output
LD0–LD3/ G0–G3	Open	Data output	Lower panel data output	G data output
B0–B3	Open	Open	Open	B data output

CL1 (Output, Pin 72): Outputs the CL1 signal which acts as a clock for X- and Y-drivers. The LVIC sends display data for one line within one CL1 signal period. The functions of the CL1 signal in different display modes are as follows:

- In display modes 1, 2, 4, and 6–8 with normal display (TN-type LCD), the CL1 signal provides X-drivers with the timing to latch and output display data. Connect this pin to the data latch clock input pins of the X-drivers.

  It also provides Y-drivers with the timing to shift the line scan signal. Connect it to the line shift clock input pins of the Y-drivers.

- In display modes 1, 2, 4, and 6–8 with double-height display (TN-type LCD), the CL1 signal provides X-drivers with the timing to latch and output display data. Connect this pin to the data latch clock input pins of the X-drivers.

- In display modes 3, 5, and 9–16 (TFT-type LCD), the CL1 signal provides the X-drivers with the timing to latch and output display data. Connect this pin to the data latch clock input pins of the X-drivers.

CL2 (Output, Pin 73): Outputs the CL2 signal which is a clock for the X-drivers. The LVIC sends display data in synchronism with the CL2 signal. Connect this pin to the data shift clock input pins of the X-drivers.

CL3 (Output, Pin 74): Outputs the CL3 signal which is a clock for the X- and Y-drivers. The functions of the CL3 signal in different display modes are as follows:

- In display modes 1, 2, 4, and 6–8 with double-height display (TN-type LCD), and in display modes 9 and 11 (TFT-type LCD with vertical stripes, Y-drivers on one side), the CL3 signal provides the Y-drivers with the timing to shift the line scan signal. Connect this pin to the line shift clock input pins of the Y-drivers.

- In display modes 13 and 15 (TFT-type LCD with horizontal stripes, Y-drivers on one side), the CL3 signal provides the X-drivers with the timing to select and output RGB data in sequence. Connect this pin to the color data select clock input pins of the X-drivers.

  This pin also provides the Y-drivers with the timing to shift the line scan signal. Connect it to the line shift clock input pins of the Y-drivers.

- In display modes 14 and 16 (TFT-type LCD with horizontal stripes, Y-drivers on both sides), the CL3 signal provides the X-drivers with the timing to select and output RGB data in sequence. Connect this pin to the color data select clock input pins of the X-drivers.

Leave the CL3 pin open in all other display modes.

CL4 (Output, Pin 75): Outputs the CL4 signal which is a clock providing the Y-drivers with the timing to shift the line scan signal. Connect this pin to the line shift clock input pins of the Y-drivers; leave it open in display modes 1, 2, 4, 6–9, 11 13, and 15, that is, in the display modes that are not for a TFT-type LCD with Y-drivers on both sides.

FLM (Output, Pin 71): Outputs the FLM signal which is a clock indicating the start of a frame. Connect this pin to the line scan data input pins of the Y-drivers.

M (Output, Pin 70): Outputs the M signal which converts LCD driving signals to AC. LCD driving signals must be converted to AC since the liquid-crystal molecular configuration quickly degrades if DC is applied. Connect this pin to the X- and Y-driver alternating signal input pins for LCD driving.

LDOTCK (Input, Pin 77): Inputs the LCD dot clock. The LCD interface unit of the LVIC operates in synchronism with the LCD dot clock.

1.5.4 Buffer memory Interface Pins

$\overline{\text{MCS0}}$ and $\overline{\text{MCS1}}$ (Output, Pins 27 and 28): Output the buffer memory chip select signal. The LVIC writes data to or reads data from buffer memory when the $\overline{\text{MCS0}}$ or $\overline{\text{MCS1}}$ signal is low. Leave these pins open if the chip select signal is not necessary.

$\overline{\text{MWE}}$ (Output, Pin 19): Outputs the buffer memory write enable signal. The LVIC writes data to buffer memory when the $\overline{\text{MWE}}$ signal is low. Leave this pin open when buffer memory is not being used, that is, in through mode.

MA0–MA15 (Output, Pins 10–22 and 24–26): Output buffer memory addresses. Up to 64 kwords (0–65535) of addresses can be specified with these signals. Leave these pins open when buffer memory is not being used, that is, in through mode.

The MA13–MA15 pins output buffer memory chip select signals according to the type of memory used (table 1-4). Leave them open if chip select signals are not necessary.

Table 1-4 Memory Type and Buffer Memory Chip Select Signal Output Pins

Memory Type	Chip Select Signal Output Pins
No Memory (Through Mode)	—
8-kbyte	$\overline{\text{MCS0}}$, $\overline{\text{MCS1}}$, MA15, MA14, MA13
32-kbyte	$\overline{\text{MCS0}}$, $\overline{\text{MCS1}}$, MA15
64-kbyte	$\overline{\text{MCS0}}$, $\overline{\text{MCS1}}$

RD0–RD7 (Input/Output, Pins 31–36, 38, and 39), GD0–GD7 (Input/Output, Pins 40–47), BD0–BD7 (Input/Output, Pins 48, 49, and 51–56): Transfer data between the LVIC and R-, G-, and B-plane memories in the 8-level gray scale display modes and the 8-color display modes. Leave these pins open when buffer memory is not being used, that is, in through mode.

The LVIC writes an OR of the RGB signals into R-plane memory in monochrome display modes. Therefore, it is not necessary to provide memories for the G- and B- planes; pull up the GD0–GD7 and BD0–BD7 pins with about 20kΩ resistors. If memories are connected to the G- and B-planes in monochrome display modes, the LVIC will write G and B signals to those memories. However, this has no effect on the R-plane memory contents or display.

1.5.5 Mode Setting Pins

PMOD0, PMOD1 (Input, Pins 78 and 79): Signals input through these pins select the LVIC control method (programming method) (table 1-5).

Table 1-5 Programming Method Selection

PMOD1	PMOD0	Programming Method	
0	0	Pin programming	
0	1	Internal register programming	With MPU
1	0		With ROM
1	1	Inhibited (Note)	

Note: This combination is for test mode only: it disables display.

DOTE (Input, Pin 80): Inputs a signal that selects at which edge of the DOTCLK signal the LVIC latches the RGB signals. The LVIC latches the RGB signals at the falling edge of the display timing signal (DOTCLK) when this pin is high, or at the rising edge when it is low.

SPS (Input, Pin 81): Inputs a signal that selects the polarity of the CRT vertical synchronization signal (VSYNC). Set this pin high when the VSYNC signal is active-high, or low when the signal is active-low.

DM0–DM3 (Input, Pins 82–85): Input signals that select the display mode. These signals determine display color, LCD screen configuration, data transfer size, and LCD driver configuration. For more details of display modes, refer to section 6, Display Mode Settings and Contents.

MS0 and MS1 (Input, Pins 98 and 99): Input signals that select the type of memory used (table 1-6).

The MS0 and MS1 pins are also used by the $\overline{\mathrm{CS}}$ and $\overline{\mathrm{WR}}$ signals, respectively. Both the $\overline{\mathrm{CS}}$ and $\overline{\mathrm{WR}}$ signals are MPU interface signals. Fix them either high or low when controlling the LVIC by the ROM programming method.

Table 1-6 Buffer Memory Selection

MS1	MS0	Memory Type
0	0	No memory (through mode)
0	1	8-kbyte
1	0	32-kbyte
1	1	64-kbyte

XDOT (Input, Pin 1): Inputs a signal that specifies the number of horizontal displayed characters. Set this pin high when the number of characters is 90 (720 dots), or low when it is 80 (640 dots).

This pin is shared with the $\overline{\mathrm{RD}}$ and A0 signals. The $\overline{\mathrm{RD}}$ signal is an MPU interface signal and the A0 signal is a ROM interface signal.

YL0–YL2 (Input, Pins 2–4): Input signals that specify the number of vertical displayed lines (that is, the number of lines counted in the vertical direction) (table 1-7).

The YL0–YL2 pins are shared with the A1–A3 signals, respectively.

Table 1-7 Setting of Number of Vertical Displayed Lines

YL2	YL1	YL0	Number of Vertical Displayed Lines
0	0	0	200
0	0	1	350
0	1	0	400
0	1	1	480
1	0	0	512
1	0	1	540
1	1	0	Inhibited (Note)
1	1	1	Inhibited (Note)

Note: 1024 lines are displayed, but they are practically invisible.

ADJ (Input, Pin 100): Inputs a signal that determines whether the F0–F3 signals adjust the number of vertical displayed lines or whether the display timing signal (DISPTMG) which is supplied externally. The F0–F3 signals adjust the DISPTMG signal when the ADJ pin is high, or adjust the number of vertical displayed lines when it is low.

The ADJ pin is also used by the RS signal (MPU interface signal). Fix this pin either high or low when controlling the LVIC by the ROM programming method.

F0–F3 (Input, Pins 5–8): Input signals that adjust the display timing signal (DISPTMG) which is supplied externally when the ADJ signal is high, or the number of vertical displayed lines when it is low.

For details of the adjustment of the DISPTMG signal, refer to section 3.4, Display Timing Signal Fine Adjustment.

When the F0–F3 signals adjust the number of vertical displayed lines, they add up to 15 lines to the number of vertical displayed lines specified by the YL2–YL0 signals, as shown in table 1-8. For example, a setting of ADJ = 0 and F3, F2, F1, F0 = 1, 0, 1, 0 adds 10 lines to the number of vertical displayed lines originally specified by the YL2–YL0 pins.

The F0–F3 pins are also used by the D0–D3 signals (MPU and ROM interface signals), respectively.

Table 1-8 Fine Adjustment of Number of Vertical Displayed Lines

F3	F2	F1	F0	Number of Lines Adjusted
0	0	0	0	±0
0	0	0	1	+1
0	0	1	0	+2
⋮	⋮	⋮	⋮	⋮
1	1	0	1	+13
1	1	1	0	+14
1	1	1	1	+15

1.5.6 MPU Interface Pins

$\overline{\text{CS}}$ (Input, Pin 98): Inputs a chip select signal from the MPU. The MPU selects the LVIC and can read data from and write data to the LVIC's internal registers when the $\overline{\text{CS}}$ signal is low.

The $\overline{\text{CS}}$ pin is also used by the MS0 signal (mode setting signal). Fix this pin either high or low when controlling the LVIC by the ROM programming method.

$\overline{\text{WR}}$ (Input, Pin 99): Inputs a write signal from the MPU. The MPU can write data into the LVIC's internal registers when the $\overline{\text{WR}}$ signal is low. The $\overline{\text{WR}}$ signal and the $\overline{\text{RD}}$ signal must not be set low at the same time.

The $\overline{\text{WR}}$ pin is also used by the MS1 signal (mode setting signal). Fix this pin either high or low when controlling the LVIC by the ROM programming method.

$\overline{\text{RD}}$ (Input, Pin 1): Inputs a read signal from the MPU. The MPU can read data from the LVIC internal registers when the $\overline{\text{RD}}$ signal is low. The $\overline{\text{RD}}$ signal and the $\overline{\text{WR}}$ signal must not be set low at the same time.

The $\overline{\text{RD}}$ pin is also used by the A0 signal (ROM interface signal) and the XDOT signal (mode setting signal).

RS (Input, Pin 100): Inputs a register select signal from the MPU. The MPU selects the LVIC's data registers (R0–R15) when the RS signal is high, or selects the LVIC's address register (AR) when it is low.
The RS pin is also used by the ADJ signal (mode setting signal). Fix this pin either high or low when controlling the LVIC by the ROM programming method.

D0–D3 (Input/Output, Pins 5–8): Transfer internal register data between the LVIC and the MPU.

The D0–D3 pins are also used by the D0–D3 signals (ROM interface signals) and the F0–F3 signals (mode setting signals).

$\overline{\text{RES}}$ (Input, Pin 97): Inputs a signal that resets the LVIC externally. For more details of LVIC reset state, refer to appendix B.

Note that a reset signal must be input after power-on.

1.5.7 ROM Interface Pins

A0–A3 (Output, Pins 1–4): Output external ROM addresses.

The A0 pin is also used by the $\overline{\text{RD}}$ signal (MPU interface signal) and the XDOT signal (mode setting signal). The A1–A3 pins are also used by the YL0–YL2 signals. Fix the A1–A3 pins either high or low when controlling the LVIC by the MPU programming method.

D0–D3 (Input, Pins 5–8): Input LVIC internal register data from an external ROM chip.

The D0–D3 pins are also used by the D0–D3 signals (MPU interface signals) and the F0–F3 signals (mode setting signals).

1.5.8 PLL Interface Pins

$\overline{\text{CD}}$ and $\overline{\text{CU}}$ (Output, Pins 86 and 87): The $\overline{\text{CD}}$ pin outputs a charge-down signal to an external charge pump and the $\overline{\text{CU}}$ pin outputs a charge-up signal when the CRT dot clock (DOTCLK) is generated by a PLL circuit. Leave these pins open when the DOTCLK signal is supplied externally.

1.6 Internal Registers

1.6.1 Registers

The LVIC has one address register and 16 data registers. Table 1-9 lists the LVIC's internal registers and figure 1-4 shows the bit assignment for each of these registers.

Table 1-9 Registers

		Reg. Address				Reg.		Program	Specified	Read/
CS	RS	3	2	1	0	No.	Register Name	Unit	Value Symbol	Write[1]
1	—	—	—	—	—	—	Invalid	—	—	—
0	0	—	—	—	—	AR	Address register[2]	—	—	W
0	1	0	0	0	0	R0	Control register 1	—	—	R/W
0	1	0	0	0	1	R1	Control register 2	—	—	R/W
0	1	0	0	1	0	R2	Vertical displayed lines register (middle-order)[3]	Lines	Nvd	R/W
0	1	0	0	1	1	R3	Vertical displayed lines register (low-order)[3]	Lines	Nvd	R/W
0	1	0	1	0	0	R4	Vertical displayed lines register (high-order)[3]/ CL3 period register (high-order)[3]	Lines/ Chars.[4]	Nvd/ Npc	R/W
0	1	0	1	0	1	R5	CL3 period register (low-order)[3]	Chars.[4]	Npc	R/W
0	1	0	1	1	0	R6	Horizontal displayed characters register (high-order)	Chars.[4]	Nhd	R/W
0	1	0	1	1	1	R7	Horizontal displayed characters register (low-order)	Chars.[4]	Nhd	R/W
0	1	1	0	0	0	R8	CL3 pulse width register	Chars.[4]	Npw	R/W
0	1	1	0	0	1	R9	Fine adjust register	Dots	Nda	R/W
0	1	1	0	1	0	R10	PLL frequency-division register (high-order)	—	NPLL	R/W
0	1	1	0	1	1	R11	PLL frequency-division register (low-order)	—	NPLL	R/W

Table 1-9 Registers (cont.)

$\overline{CS}$	RS	Reg. Address 3	2	1	0	Reg. No.	Register Name	Program Unit	Specified Value Symbol	Read/ Write[1]
0	1	1	1	0	0	R12	Vertical back porch register (high-order)[3]	Lines	Ncvbp	R/W
0	1	1	1	0	1	R13	Vertical back porch register (low-order)[3]	Lines	Ncvbp	R/W
0	1	1	1	1	0	R14	Horizontal back porch register (high-order)[3]	Dots	Nchbp	R/W
0	1	1	1	1	1	R15	Horizontal back porch register (low-order)[3]	Dots	Nchbp	R/W

Notes:

1. W indicates the register can only be written to, and R/W indicates the register can both be written to and read.
2. If an attempt is made to read data from this register with RS = 0, the bus is driven to high-impedance state and the output data is undefined.
3. Write (specified value –1) into these registers.
4. A character is considered to be composed of eight horizontal dots.

CS	RS	Reg•Address 3	2	1	0	Reg. No.	Data Bit 3	2	1	0	
1	–	–	–	–	–	–	▨	▨	▨	▨	
0	0	–	–	–	–	AR					Address register
0	1	0	0	0	1	R0	0	0	DSP	DCK	Control register 1
0	1	0	0	0	0	R1	MC	DON	MS1	MS0	Control register 2
0	1	0	0	1	1	R2					Vertical displayed lines register
0	1	0	0	1	0	R3					
0	1	0	1	0	1	R4					
0	1	0	1	0	0	R5					CL3 period register
0	1	0	1	1	1	R6					Horizontal displayed characters register
0	1	0	1	1	0	R7					
0	1	1	0	0	1	R8					CL3 pulse width register
0	1	1	0	0	0	R9					Fine adjust register
0	1	1	0	1	1	R10					PLL frequency-division Register
0	1	1	0	1	0	R11					
0	1	1	1	0	1	R12					Vertical back porch register
0	1	1	1	0	0	R13					
0	1	1	1	1	1	R14					Horizontal back porch register
0	1	1	1	1	0	R15					

Notes:

1. ▨ indicates invalid bits. Any attempt to read data from these register bits will return undefined data.
2. Data bits 3 and 2 of control register 1 are reserved bits. Write 0 to them.

Figure 1-4 Register Bit Assignment

1.6.2 Validation and Invalidation of Internal Registers

The internal registers are all invalid when the LVIC is controlled by the pin programming method. They are valid only when the LVIC is controlled by the internal register programming method. However, some registers or bits are invalid even when the LVIC is controlled by the internal register programming method, as described below. Any value can be set in invalid registers (bits).

DSP Bit of Control Register 1 (R0): Invalid when the DCK bit of that register is 1. In this case the LVIC generates the display timing signal (DISPTMG) even when the DSP bit is 0.

CL3 Period Register (R5 and Low-Order 2 Bits of R4): Invalid in the monochrome display modes, 8-level gray scale display modes, and 8-color display modes with vertical stripes. Valid only in the 8-color display modes with horizontal stripes, that is, only in display modes 13–16.

MSB of Horizontal Displayed Characters Register (R6): Invalid in the dual screen modes, that is, in display modes 1 and 6.

Fine Adjust Register (R9): Invalid when the display timing signal (DISPTMG) is generated internally, that is, when either the DCK bit or the DSP bit of control register 1 (R0) is 1.

PLL Frequency-Division Register (R10 and R11): Invalid when the CRT display dot clock (DOTCLK) is supplied externally, that is, when the DCK bit of control register 1 (R0) is 0.

Vertical and Horizontal Back Porch Registers (R12–R15): Invalid when the display timing signal (DISPTMG) is supplied externally, that is, when both the DCK and the DSP bits are 0.

Set any value less than the CL3 signal period in the CL3 pulse width register (R8) since that register is not invalid in the TN-type LCD modes.

1.6.3 Register Functions

Address Register (AR): Used to select one of the 16 data registers, as shown in figure 1-5. The address register itself is selected when the RS signal is low. In order to select a certain data register, that register address must be written into the address register using the MPU.

AR

Data Bit	3	2	1	0
Value	Register address			

Figure 1-5 Address Register

Control Register 1 (R0): Specifies whether the display timing signal (DISPTMG) and the CRT display dot clock (DOTCLK) are supplied externally or generated internally (figure 1-6).

Data bits 3 and 2 are reserved bits: write 0 to them.

- DSP bit:
  - DSP = 1: The DISPTMG signal is generated internally.
  - DSP = 0: The DISPTMG signal is supplied externally. (However, if DCK = 1, the DISPTMG signal is generated internally, regardless of the value in the DSP bit.)
- DCK bit:
  - DCK = 1: The DOTCLK signal is generated internally.
  - DCK = 0: The DOTCLK signal is supplied externally.

R0

Data Bit	3	2	1	0
Function	0 (Reserved)	0	DSP	DCK

Figure 1-6 Control Register 1

Control Register 2 (R1): Specifies M signal output, which determines LCD driving signal alternation type, as well as LCD on/off and buffer memory type (figure 1-7).

- MC bit: Specifies M signal output.
  - MC = 1: The M signal alternates every line.
  - MC = 0: The M signal alternates every frame.

For details, refer to section 3.5, LCD Driving Signal Alternation.

- DON bit: Specifies whether the LCD is on or off.
  - DON = 1: LCD on.
  - DON = 1: LCD off.

For details, refer to section 3.7, Display On/Off Control.

- MS1, MS0 bits: Specify buffer memory type.
  - MS1, MS0 = 0, 0: No memory (through mode)
  - MS1, MS0 = 0, 1: 8-kbyte memory
  - MS1, MS0 = 1, 0: 32-kbyte memory
  - MS1, MS0 = 1, 1: 64-kbyte memory

For details, refer to section 3.6, Buffer Memory Selection.

	R1			
Data Bit	3	2	1	0
Function	MC	DON	MS1	MS0

Figure 1-7 Control Register 2

Vertical Displayed Lines Register (R2, R3, and High-Order 2 Bits of R4): Specifies the number of lines displayed from screen top to bottom (figure 1-8). Note that this register does not specify a multiplexing duty ratio. This means that the specified value does not depend on screen configuration. This register can contain either an odd or an even number in the single screen modes with Y-drivers on one side, that is, in display modes 2, 4, 7–9, but can contain only an even number in other modes. For details, refer to section 3.1, Screen Size Setting.

	R4		R2				R3			
Data Bit	3	2	3	2	1	0	3	2	1	0
Value	Nvd – 1									

(Unit: Lines)

Nvd: Number of vertical displayed lines

Figure 1-8 Vertical Displayed Lines Register

CL3 Period Register (R5 and Low-Order 2 Bits of R4): Specifies the CL3 signal period in the 8-color display modes with horizontal stripes (display modes 13–16) (figure 1-9). Therefore, this register is invalid in other modes (its parameters are ignored).

Specifying the CL3 signal period automatically specifies the CL4 signal period. The CL4 signal period is always twice that of CL3 signal since the CL4 signal changes at the rising edge of the CL3 signal. For details, refer to section 7.2, CL3 and CL4 Signal Output and Register Setting.

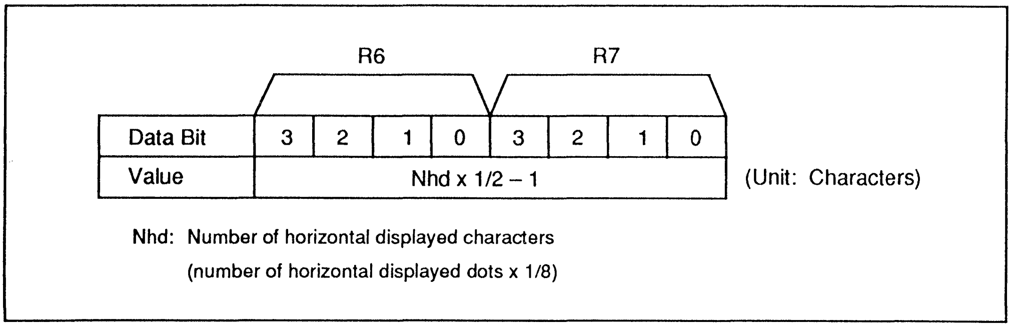
	R4		R5			
Data Bit	1	0	3	2	1	0
Value	Npc – 1					

(Unit: Characters)

Npc:	CL3 signal period = (Nhd + 6) x 1/3
Nhd:	Number of horizontal displayed characters (number of horizontal displayed dots x 1/8)
Note:	When (Nhd + 6) is not divisible by 3, the quotient is rounded off.

Figure 1-9 CL3 Period Register

Horizontal Displayed Characters Register (R6 and R7): Specifies the number of characters displayed on one line (figure 1-10). This register can contain an even number only. In the dual screen modes (display modes 1 and 6), the most significant bit of this register is invalid and set parameters are ignored. For details, refer to section 3.1, Screen Size Setting.



	R6				R7			
Data Bit	3	2	1	0	3	2	1	0
Value	Nhd x 1/2 – 1							

(Unit: Characters)

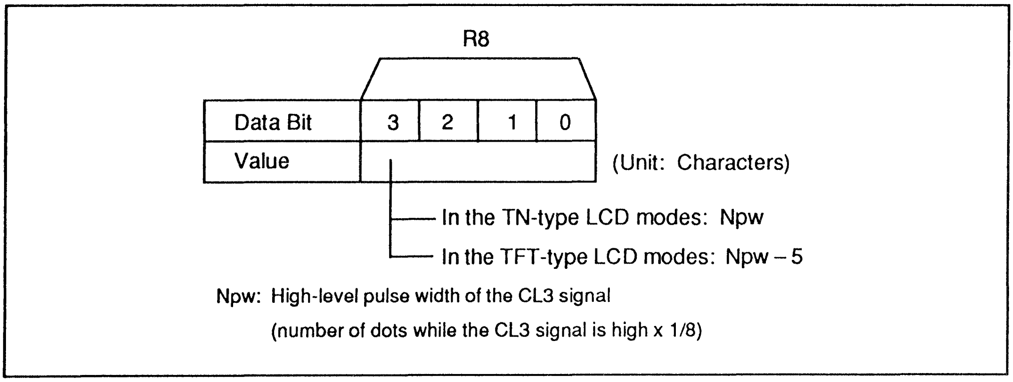
Nhd: Number of horizontal displayed characters
(number of horizontal displayed dots x 1/8)

Figure 1-10 Horizontal Displayed Characters Register

CL3 Pulse Width Register (R8): Specifies the high-level pulse width of the CL3 signal (figure 1-11). To control a TFT-type LCD, a data hold time is necessary and it is controlled by the high-level pulse width of the CL3 signal. For details of data hold time, refer to section 7.1.2, High-Level Pulse Width of CL3 Signal.

The CL3 signal is output with the high-level pulse width specified by this register even when it is not controlling a TFT-type LCD.

For details of determining the high-level pulse width of the CL3 signal, refer to section 7.2.2, Parameter Setting in Internal Register Programming Method.



	R8			
Data Bit	3	2	1	0
Value				

(Unit: Characters)

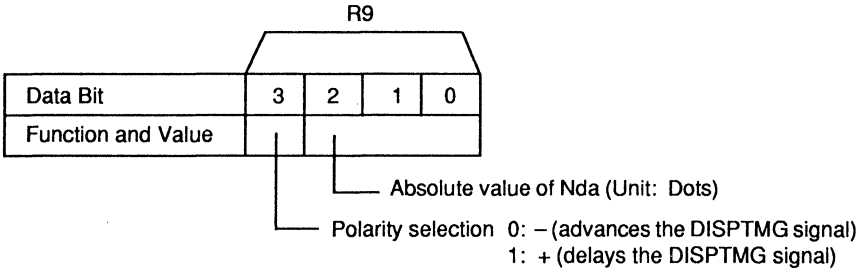
In the TN-type LCD modes: Npw
In the TFT-type LCD modes: Npw – 5

Npw: High-level pulse width of the CL3 signal
(number of dots while the CL3 signal is high x 1/8)

Figure 1-11 CL3 Pulse Width Register

Fine Adjust Register (R9): Adjusts the externally supplied display timing signal (DISPTMG) to synchronize its phase with that of LCD data (figure 1-12). The value to be written into this register depends on the interval between the rising edge of the DISPTMG signal and the display start position. For details of DISPTMG signal fine adjustment, refer to section 3.4, Display Timing Signal Fine Adjustment.

This register is invalid when the DISPTMG signal is generated internally, that is, when either the DCK bit or the DSP bit of control register 1 (R0) is 1.


R9
Data Bit
3
2
1
0
Function and Value
Absolute value of Nda (Unit: Dots)
Polarity selection 0: – (advances the DISPTMG signal)
1: + (delays the DISPTMG signal)

Nda: Number of adjustment dots

Figure 1-12 Fine Adjust Register

PLL Frequency-Division Register (R10 and R11): Specifies the PLL frequency-division ratio for generating the CRT display dot clock (DOTCLK) by a PLL circuit (figure 1-13). The PLL frequency-division ratio is the ratio of the DOTCLK signal frequency to the horizontal synchronization signal (HSYNC) frequency. The LVIC generates the DOTCLK signal according to this ratio. The PLL frequency-division register can contain a ratio from 731 to 986. For details of DOTCLK signal generation, refer to section 3.3, Dot Clock Generation.

This register is invalid when the DOTCLK signal is supplied externally, that is, when the DCK bit of control register 1 (R0) is 0.

	R10				R11			
Data Bit	3	2	1	0	3	2	1	0
Value	NPLL − 731							

NPLL : PLL frequency-division ratio
= DOTCLK frequency/HSYNC frequency

Figure 1-13 PLL Frequency-Division Register

Vertical Back Porch Register (R12 and R13): Specifies the vertical back porch which is the number of lines between the active edge of the vertical synchronization signal (VSYNC) and the rising edge of the display timing signal (DISPTMG) when the DISPTMG signal is generated internally (figure 1-14). For details of vertical back porch, refer to section 3.2.2, Display Timing Signal Generation and Register Setting.

This register is invalid when the DISPTMG signal is supplied externally, that is, when both the DCK bit and the DSP bit of control register 1 (R0) are 0.

	R12				R13				
Data Bit	3	2	1	0	3	2	1	0	
Value	Ncvbp − 1								(Unit: Lines)

Ncvbp: Vertical back porch = number of lines between the active edge of the VSYNC signal and the rising edge of the DISPTMG signal. (The SPS pin must be set high when the VSYNC signal is active-high or low when it is active-low.)

Figure 1-14 Vertical Back Porch Register

Horizontal Back Porch Register (R14 and R15): Specifies the horizontal back porch which is the number of dots between the rising edge of the horizontal synchronization signal (HSYNC) just before the rising edge of the display timing signal (DISPTMG) and the rising edge of the DISPTMG signal, when the DISPTMG signal is generated internally (figure 1-15). For details of horizontal back porch, refer to section 3.2.2, Display Timing Signal Generation and Register Setting.

This register is invalid when the DISPTMG signal is supplied externally, that is, when both the DCK bit and the DSP bit of control register 1 (R0) are 0.

	R14				R15			
Data Bit	3	2	1	0	3	2	1	0
Value	Nchbp – 1							

(Unit: Dots)

Nchbp: Horizontal back porch = number of dots between the rising edge of the HSYNC signal (just before the rising edge of the DISPTMG signal) and the rising edge of the DISPTMG signal)

Figure 1-15 Horizontal Back Porch Register

1.6.4 Register Programming Limits

The values written into the LVIC's internal registers have the limits listed in table 1-10. The symbols in table 1-10 are defined as shown in table 1-11 and figure 1-16.

Table 1-10 Limits of Values Written into Registers

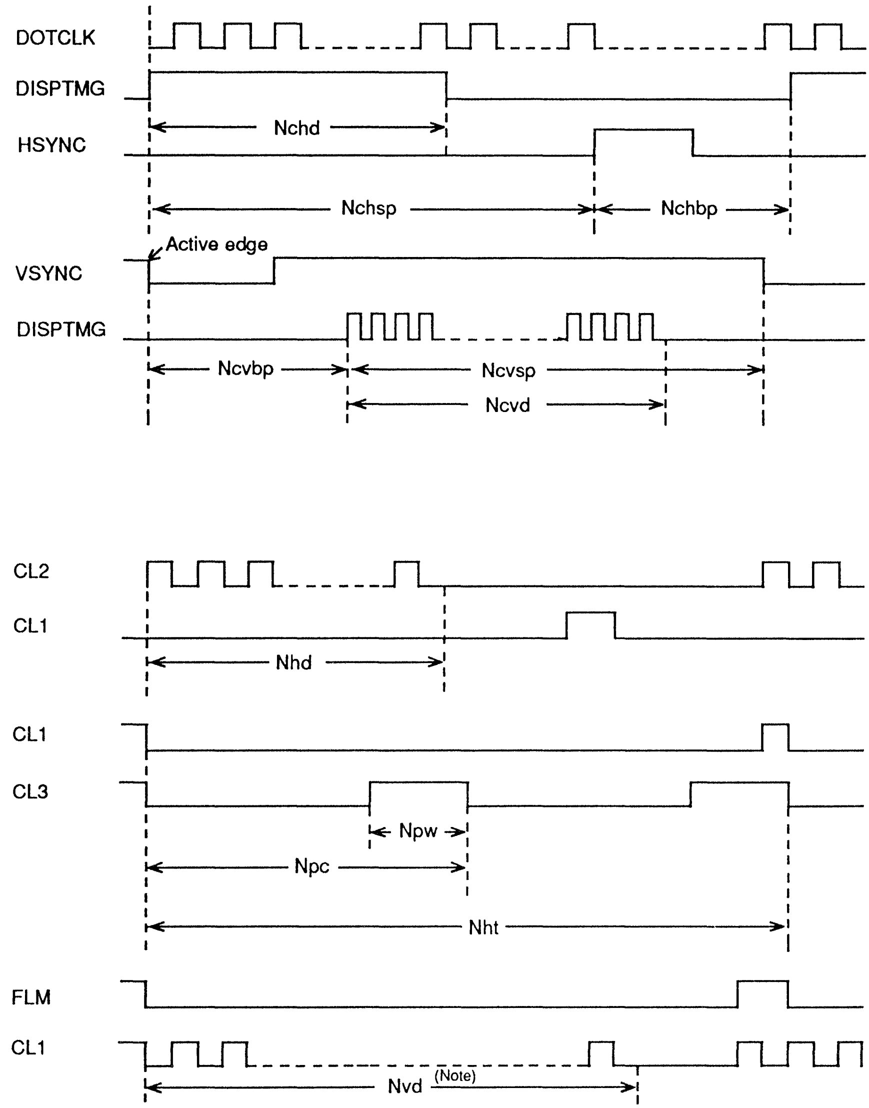
Item	Limits	Notes	Applicable Registers
Screen Configuration	$4 \leqq \mathrm{Nvd} \leqq (\mathrm{Ncvbp} + \mathrm{Ncvsp}) - 1 \leqq 1024$		R2, R3, R4, R6, R7
	$4 \leqq \mathrm{Nhd} \leqq (\mathrm{Nchbp} \times 1/n + \mathrm{Nchsp}) - 1 \leqq 506$	1, 2	
	$(\mathrm{Nhd} + 6) \times n \times \mathrm{Nvd} \times f_{\mathrm{FLM}} \leqq f_{\mathrm{DOTCLK}} \leqq 30\ \mathrm{MHz}$	1, 3	
CL3 Signal Control	$1 \leqq \mathrm{Npw} \leqq (\mathrm{Nhd} + 6)/2 - 1$	4	R4, R5, R6, R7, R8
	$1 \leqq \mathrm{Npw} \leqq \mathrm{Nhd}$	5	
	$1 \leqq \mathrm{Npw} \leqq \mathrm{Npc} - 1$	6	
DISPTMG Signal Generation	$1 \leqq \mathrm{Nchbp} \leqq 256$	7	R12, R13
	$1 \leqq \mathrm{Ncvbp} \leqq 256$	7	R14, R15
No Memory (Through Mode)	$4 \leqq \mathrm{Nhd} \leqq \mathrm{Nchsp} - 4$	8	R2, R3, R4, R6, R7
	$4 \leqq \mathrm{Nvd} \leqq \mathrm{Ncvsp} - 1$	8	

Notes:

1. n indicates the horizontal character pitch which is the number of horizontal dots making up one character.
2. $\mathrm{Nhd} \leqq 250$ in dual screen modes (display modes 1 and 6).
3. f_{FLM} is the FLM signal frequency and f_{DOTCLK} is the CRT display dot clock (DOTCLK) frequency.
   $f_{\mathrm{LDOTCK}} < f_{\mathrm{DOTCLK}} \times 15/16$ or $f_{\mathrm{LDOTCK}} = f_{\mathrm{DOTCLK}}$
   (f_{LDOTCK} is the LCD dot clock (LDOTCK) frequency)
4. In display modes 1, 2, 4, and 6–8
5. In display modes 3, 5, and 9–12 where Npw = (value in R8) + 5
6. In display modes 13–16 where Npw = (value in R8) + 5
7. (Value in R14 and R15) $\leqq (\mathrm{Nchsp} \times n + \mathrm{Nchbp}) - \mathrm{Nhd} \times n - 2$
   (n = horizontal character pitch)
   (Value in R12 and R13) $\leqq (\mathrm{Ncvsp} \times n + \mathrm{Ncvbp}) - \mathrm{Nvd} - 2$
8. $\mathrm{Nht} = \mathrm{Nchsp} + (\mathrm{Nchbp} \times 1/n)$, $\mathrm{Nvd} < \mathrm{Ncvbp} + \mathrm{Ncvsp}$
   ($\mathrm{Nht} = (\mathrm{Nhd} + 6)$ when buffer memory is used)
   (n = horizontal character pitch)

Table 1-11 Symbol Definitions

Symbol	Definition
Nchd	Number of horizontal displayed characters on the CRT display ((number of horizontal displayed dots on the CRT display) × 1/8)
Nchsp	Number of characters between the rising edge of the DISPTMG signal and that of the HSYNC signal ((number of dots between the rising edge of the DISPTMG signal and that of the HSYNC signal) × 1/8) (= horizontal synchronized position)
Nchbp	Number of dots between the rising edge of the HSYNC signal and that of the DISPTMG signal (just after the rising edge of the HSYNC signal) (= horizontal back porch)
Ncvbp	Number of lines between the active edge of the VSYNC signal and the rising edge of the DISPTMG signal (just after the active edge of the VSYNC signal) (= vertical back porch)
Ncvsp	Number of dots between the rising edge of the DISPTMG signal and the active edge of the VSYNC signal (= vertical syncronized position)
Ncvd	Number of vertical displayed lines on the CRT display
Nhd	Number of horizontal displayed characters on the LCD ((number of horizontal displayed dots) × 1/8)
Npc	Number of characters during a CL3 signal period ((number of dots during a CL3 signal period) × 1/8)
Npw	Number of characters while the CL3 signal is high ((number of dots while the CL3 signal is high) × 1/8)
Nht	Number of characters during a CL1 signal period ((number of dots during a CL1 signal period) × 1/8)
Nvd	Number of vertical displayed lines on the LCD



Note: When the screen is dual, the Nvd period is doubled.

Figure 1-16 Symbol Definitions

Section 2 Interface

2.1 Video Signal Interface

The LVIC converts the standard video signals for CRT display into LCD data through the use of a sevenpin video signal interface.

Figure 2-1 shows an example of connecting video signals to the LVIC. Since the dot clock (DOTCLK) and the display timing signal (DISPTMG) are not usually output as standard video signals, these signals must be generated. For the generation of these signals, refer to section 2.5, PLL Interface, and section 3.2, Display Timing Signal Generation. The case in which all the video signals are supplied to the LVIC is described below.

The DOTCLK signal, which acts as a latch clock for serial RGB data, is the basic clock of the LVIC. The LVIC latches the serial data at the DOTCLK signal and converts it into 8-bit parallel data for output to buffer memory.

The horizontal and vertical synchronization signals (HSYNC and VSYNC) are necessary to synchronize the LVIC with the CRT display system. They act as basic clocks when the DISPTMG signal and the DOTCLK are generated internally.

The DISPTMG signal marks the display start position with its rising edge. It does not matter whether the high-level pulse width of the signal is larger than the number of horizontal displayed characters. However, the number of horizontal displayed characters must be smaller than the total number of horizontal characters of the CRT display.

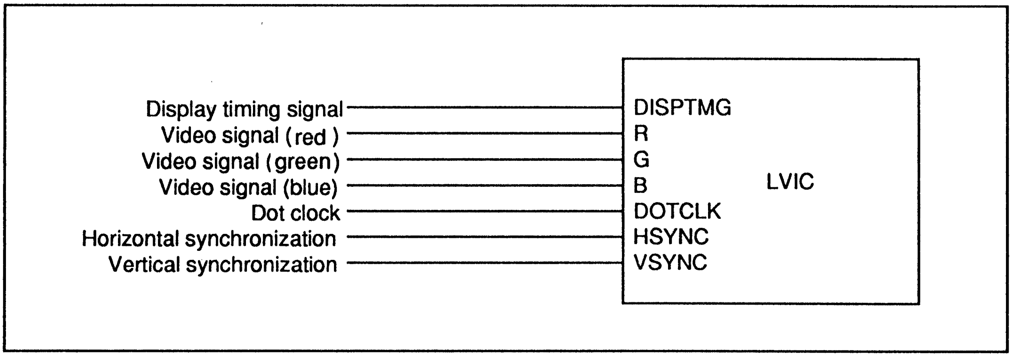
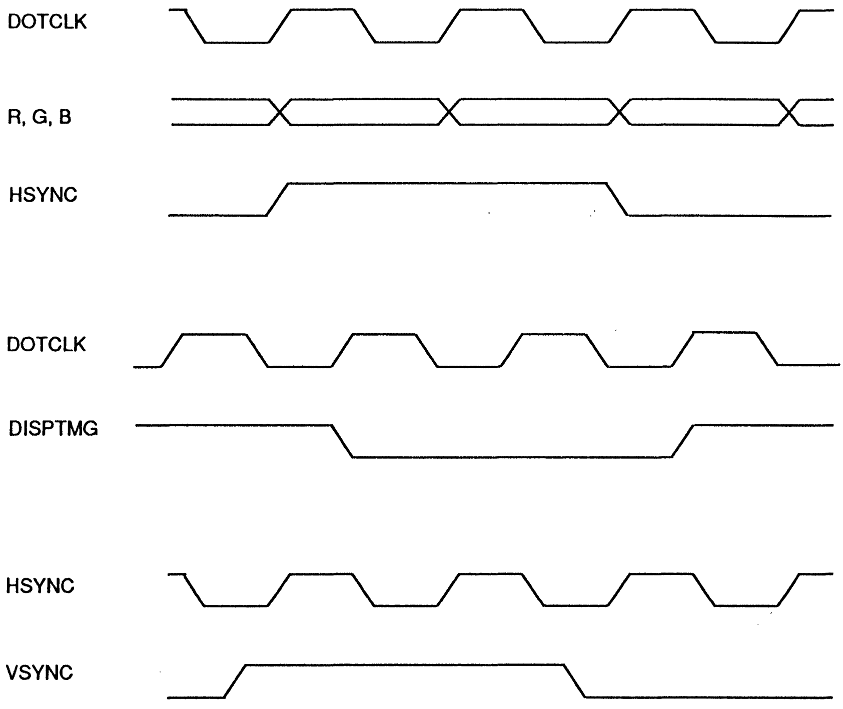


Figure 2-1 Video Signal Interface

Figure 2-2 is the timing charts for the video interface signals. Set the DOTE pin high when the LVIC latches the RGB data at the falling edge of the DOTCLK signal, and set it low at the rising edge. If the display start position shifts, adjust the DISPTMG signal. (Refer to section 3.4, Display Timing Signal Fine Adjustment, for details.)



Note: See the data book for detailed timing specifications

Figure 2-2 Timing of Video Interface Signals

2.2 LCD Interface

2.2.1 LDOTCK Signal Frequency Calculation

The frequencies of the CRT display dot clock (DOTCLK) and the LCD dot clock (LDOTCK) of the LVIC can be set independently. However, the range of the LDOTCK signal frequency is limited since data read and write operations between the LVIC and buffer memory are all based on the DOTCLK signal.

The LDOTCK signal serves as the basic clock for LCD signals. The LDOTCK signal frequency (f_{LDOTCK}) is determined by LCD screen size and the FLM signal frequency (f_{FLM}), and is obtained by the following equation:

$$f_{LDOTCK} = (Nhd + 6) \times n \times Nvd/m \times f_{FLM} \quad \text{(2-1)}$$

Nhd: Number of horizontal displayed characters
(number of horizontal displayed dots × 1/8)
Nvd: Number of vertical displayed lines
n: Horizontal character pitch (number of horizontal dots for one character)
m: 1... Single screen
2... Dual screens

Set the FLM signal frequency according to the specification of the LCD module being used. About 70 Hz is usually suitable. If the frequency is too low, the display may be uneven or it may flicker, while if the frequency is too high, the LDOTCK signal frequency becomes higher than the DOTCLK signal frequency, preventing normal display. One of the following relationships must hold between the LDOTCK signal frequency (f_{LDOTCK}) and the DOTCLK signal frequency (f_{DOTCLK}):

$$f_{LDOTCK} < f_{DOTCLK} \times 15/16 \quad \text{(2-2)}$$

or

$$f_{LDOTCK} = f_{DOTCLK} \quad \text{(2-3)}$$

(In this case, the phases of the LDOTCK signal and the DOTCLK signal must be opposite.)

Table 2-1 lists the optimum LDOTCK frequencies for different CRT display systems.

Table 2-1 LDOTCK Signal Frequencies for Different CRT Display systems

CRT Display System	CRT Display Screen Size (Dots)	LCD Screen Size (Dots)	Dot Clock Frequency (MHz)	LCD Dot Clock Frequency (MHz)	FLM Signal Frequency (Hz)
CGA	640 × 200	640 × 200	14.318	9.632	70
EGA	640 × 350	640 × 350	16.257	16.257	67.5
PC-9801™	640 × 400	640 × 400	21.053	19.264	70
VGA	640 × 480	640 × 480	25.175	23.117	70
	720 × 480	720 × 480	28.321	25.805	70

CGA: Color Graphics Adapter™

EGA: Enhanced Graphics Adapter™

VGA: Video Graphics Adapter™

2.2.2 TN-Type LCD Interface

The LVIC uses the FLM, M, CL1, and CL2 signals as TN-type LCD interface signals, and it uses the LU0–LU3 and LD0–LD3 pins for outputting display data.

Figure 2-3 shows an example of connecting a TN-type LCD to the LVIC. In this figure, the HD61104s are used as X-drivers (column drivers) and the HD61105s are used as Y-drivers (row drivers). This circuit supports display mode 2 (monochrome display, 4-bit data transfer, single screen).

The LVIC outputs four bits of display data via the LU0–LU3 pins at the rising edge of the CL2 signal, and the X-drivers latch the data at its falling edge.

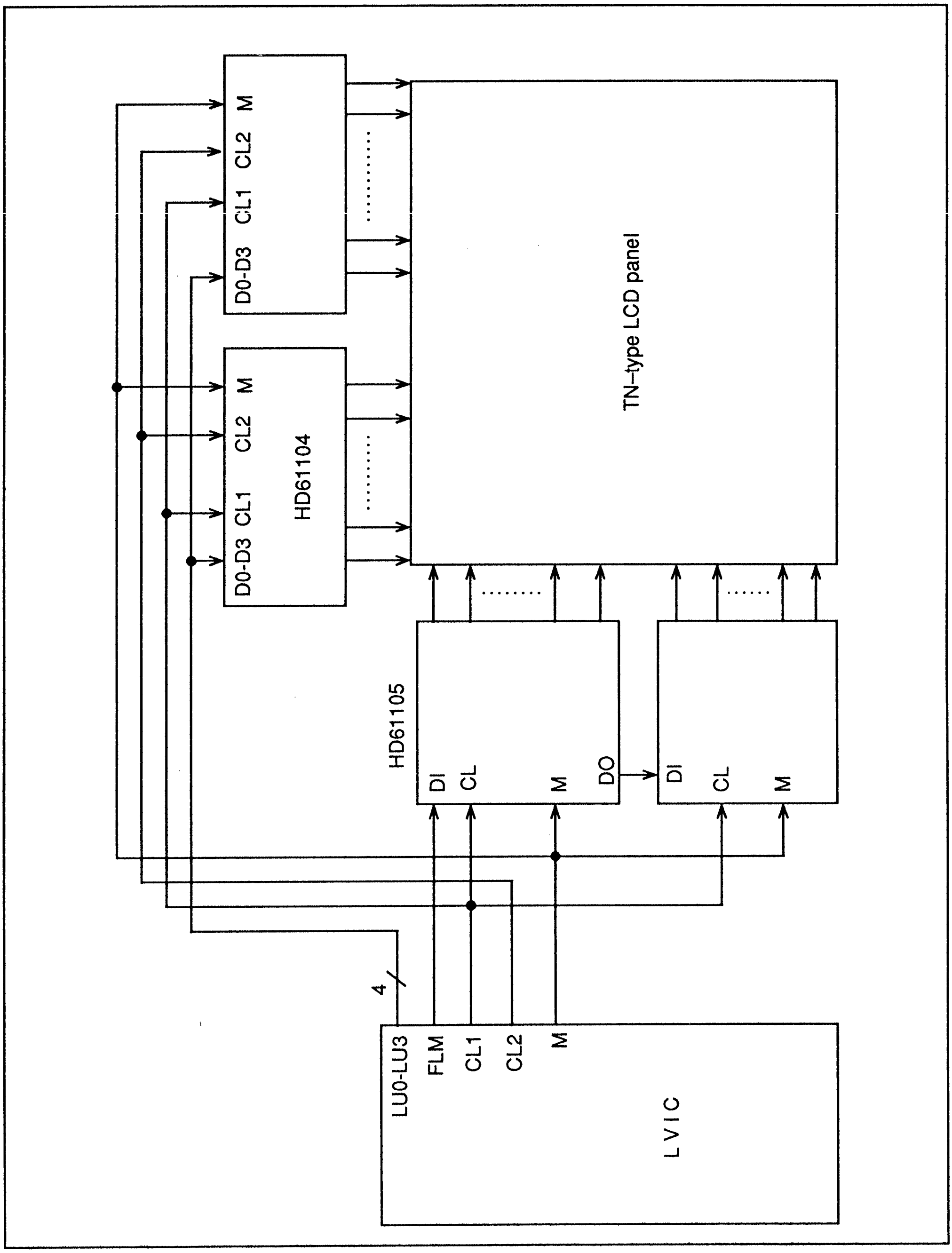


Figure 2-3 TN-Type LCD Interface

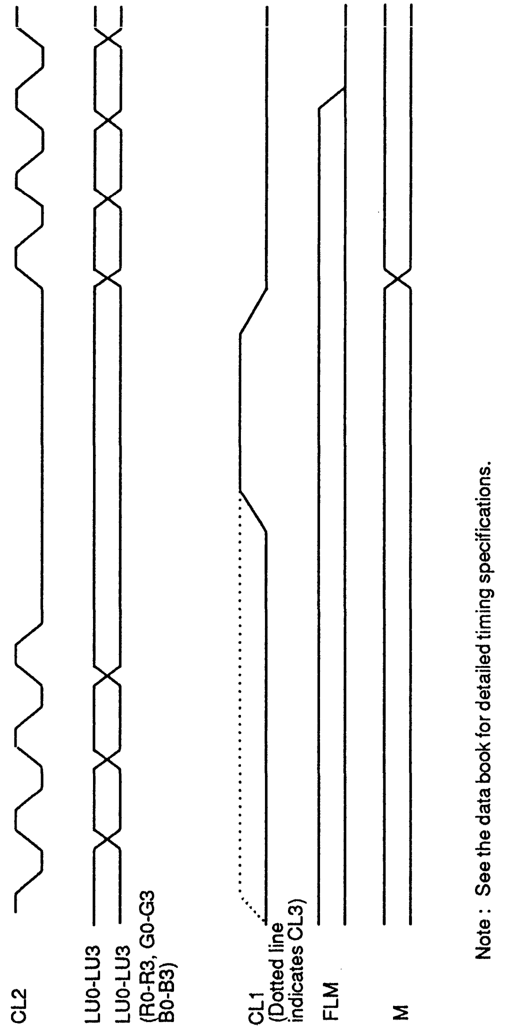
Figure 2-4 is a timing chart for LCD interface signals and figure 2-5 is an expanded view of the same timing.

The LVIC outputs a number of CL2 signal pulses equal to a quarter of the horizontal displayed dots during one line display period. However, the LVIC has a retrace period of six characters (48 dots) long, and does not output CL2 signal pulses during this period. Accordingly, the CL1 signal pulses do not overlap with the CL2 signal pulses. The retrace period is fixed and cannot be changed.

The CL2 signal period depends on the display mode; the CL2 signal period in the 4-bit data transfer and single screen modes is half that in the 4-bit data transfer and dual screen modes and the 8-bit data transfer and single screen modes. Therefore, the amount of data transferred to the LCD drivers per unit time is the same in all display modes.

The CL2 signal frequency (f_{CL2}) is expressed as follows:

$f_{CL2} = f_{LDOTCK} \times 1/4$ (in display modes 2, 3, 7, 9, 10, 13, and 14) .... (2-4)
$f_{CL2} = f_{LDOTCK} \times 1/8$ (in display modes 1, 4, 5, 6, 8, 11, 12, 15, and 16) ...... (2-5)
f_{LDOTCK}: LCD dot clock (LDOTCK) frequency



Note : See the data book for detailed timing specifications.

Figure 2-4 Timing of LCD Interface Signals

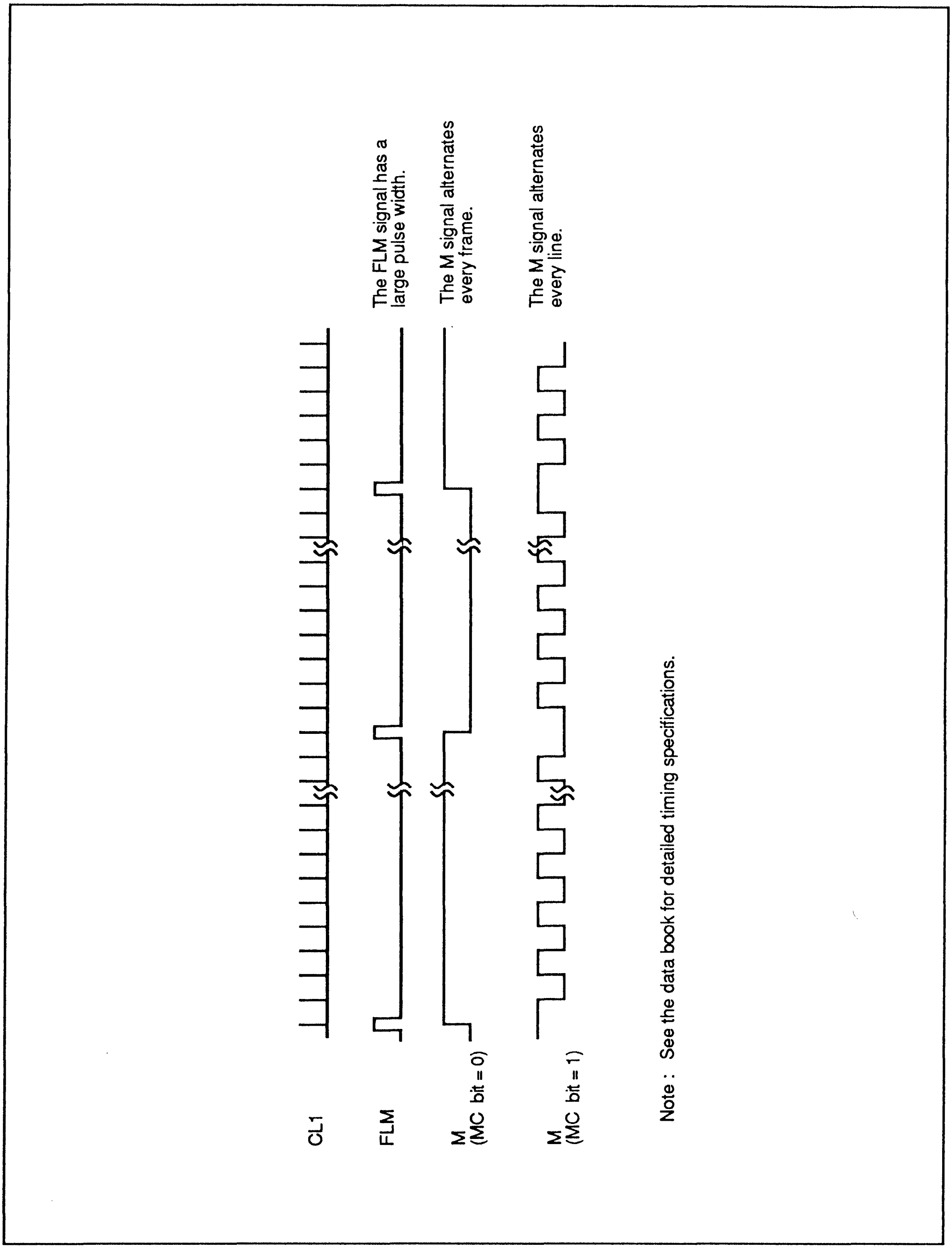

CL1
FLM
M
(MC bit = 0)
M
(MC bit = 1)
The FLM signal has a large pulse width.
The M signal alternates every frame.
The M signal alternates every line.
Note : See the data book for detailed timing specifications.

Figure 2-5 Expanded View of Figure 2-4

2.2.3 TFT-Type LCD Interface

The LVIC uses the CL3 and CL4 signals as TFT-type LCD interface signals in addition to the TN-type LCD interface signals, and it uses the R0–R3, G0–G3, and B0–B3 pins for outputting display data in the 8-color display modes. (In the monochrome display modes, the LVIC uses the LU0–LU3 and LD0–LD3 pins in the same way as in the TN-type LCD modes.) Both the CL3 and CL4 signals are line shift clocks for Y-drivers (row drivers).

Figure 2-6 shows an example of connecting a TFT-type LCD to the LVIC. In this figure, the HD61104s are used as X-drivers (column drivers) and the HD61105s are used as Y-drivers (row drivers). This circuit supports display mode 9 (8-color display, X-, Y-drivers on one side, vertical stripes). In this case, the X-drivers are divided into R data output drivers, G data output drivers, and B data output drivers. The LVIC sends RGB data to the corresponding drivers. The Y-drivers drive the gate electrodes of the TFT-type LCD panel, and the CL3 signal acts as a line shift clock for the Y-drivers. For details of the CL3 and CL4 signals, refer to section 7.1, CL3 and CL4 Signal Functions.

In this case, the output timing of the TFT-Type LCD interface signals is basically the same as that of the TN-type LCD interface signals. In particular, the output timings of the CL3 signal and the CL1 signal are almost the same. Their periods and falling edges are identical, but their rising edges are not always identical (refer to figures 2-4 and 2-5).

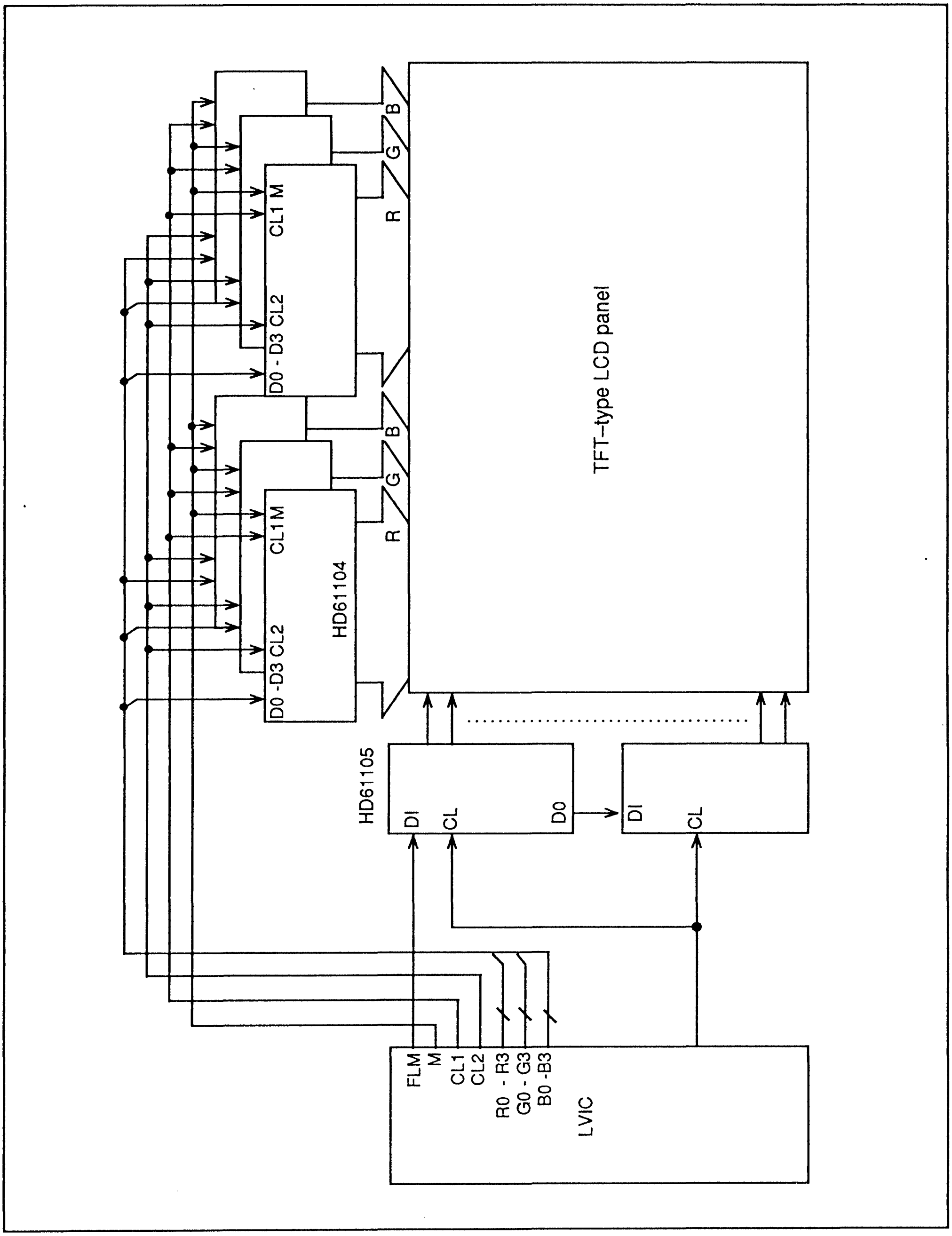


Figure 2-6 TFT-Type LCD Interface

2.3 Buffer Memory Interface

2.3.1 Memory Type and Memory Capacity Calculations

Memory Type: The type of memory which can be employed as buffer memory is limited by the CRT display dot clock frequency (f_{DOTCLK}). Specifically, the memory must satisfy the conditions given in equations 2-6 and 2-7 below, where t_{CYCD} is the dot clock cycle time ($1/f_{DOTCLK}$).

$$\begin{aligned}\text{Memory access time} &\leqq \text{LVIC read cycle time} - \text{LVIC read data setup time} \\ &\leqq 5 \cdot t_{CYCD} - 50 - 25 \text{ (ns)} \\ &\leqq 5 \cdot t_{CYCD} - 75 \quad \text{(ns)} \quad \text{.......... (2-6)}\end{aligned}$$

$$\begin{aligned}\text{Memory write (input) data setup time} &\leqq \text{LVIC write (output) data setup time} \\ &\leqq 2 \cdot t_{CYCD} - 25 \text{ (ns)} \quad \text{.......... (2-7)}\end{aligned}$$

For example, the following calculations show that a memory whose access time is less than or equal to 274 ns and whose write data setup time is less than or equal to 115 ns can be used for the LVIC used with a CGA board (f_{DOTCLK} =14.318 MHz):

$$\begin{aligned}\text{Memory access time} &\leqq (5/14.318 \times 10^{6})/(1 \times 10^{-9}) - 75 \text{ (ns)} \\ &\leqq 274 \quad \text{(ns)}\end{aligned}$$

$$\begin{aligned}\text{Memory write data setup time} &\leqq (2/14.318 \times 10^{6})/(1 \times 10^{-9}) - 25 \text{ (ns)} \\ &\leqq 115 \quad \text{(ns)}\end{aligned}$$

Memory Capacity Calculation: The memory capacity required per plane is determined by the display screen size and can be obtained from the following equation:

$$\text{Memory capacity (bits)} = Nhd \times Nvd \times 8 \quad \text{.......... (2-8)}$$

Nhd: Number of horizontal displayed characters
(number of horizontal displayed dots × 1/8)
Nvd: Number of vertical displayed lines

For instance, a display screen of 640 × 200 dots requires 128 kbits in the monochrome display modes and 3 × 128 kbits in the 8-level gray scale display modes and 8-color display modes.

Table 2-2 lists the optimum memory devices and their quantities for different CRT display systems.

Memory capacity is selected with the MS0 and MS1 pins or with the MS0 and MS1 bits of control register 2 (R1). For details, refer to section 3.6, Buffer Memory Selection.

Table 2-2 Optimum Memory Devices and Quantities for Different CRT Display Systems

				Device Quantities	
CRT Display System	**Display Screen Size (Dots/Bits)**	**f_{DOTCLK} (MHz)**	**Optimum Memory Device**	**Monochrome Display**	**Gray Scale, Color Display**
CGA	640 × 200/125k	14.318	HM6264P-15	2	6
EGA	640 × 350/218.75k	16.257	HM62256P-15	1	3
PC-9801	640 × 400/250k	21.053	HM62256P-15	1	3
VGA	640 × 480/299.8k	25.175	HM62256P-12	2	6
	640 × 520/325k	28.321	HM62256P-10	2	6

f_{DOTCLK}: CRT display dot clock (DOTCLK) frequency

HM6264P-15: 64-kbit memory with access time of 150 ns

HM62256P-15: 256-kbit memory with access time of 150 ns

HM62256P-12: 256-kbit memory with access time of 120 ns

HM62256P-10: 256-kbit memory with access time of 100 ns

2.3.2 Buffer Memory Interface

The LVIC uses memory address lines (MA0–MA15), memory chip select signals ($\overline{\text{MCS0}}$, $\overline{\text{MCS1}}$), and a memory write enable signal ($\overline{\text{MWE}}$) as buffer memory interface signals, and it uses the RD0–RD7, GD0–GD7, and BD0–BD7 pins for outputting display data.

Figure 2-7 shows an example of connecting HM62256s (32-kbyte memories) to the LVIC. Since the MA13–MA15 pins are also used by the memory addresses and the memory chip select signals, the connection of these pins to memory devices depends on the type of memory being used. For details, refer to section 3.6, Buffer Memory Selection.

Figures 2-8 and 2-9 are timing charts of the buffer memory interface timing signals.

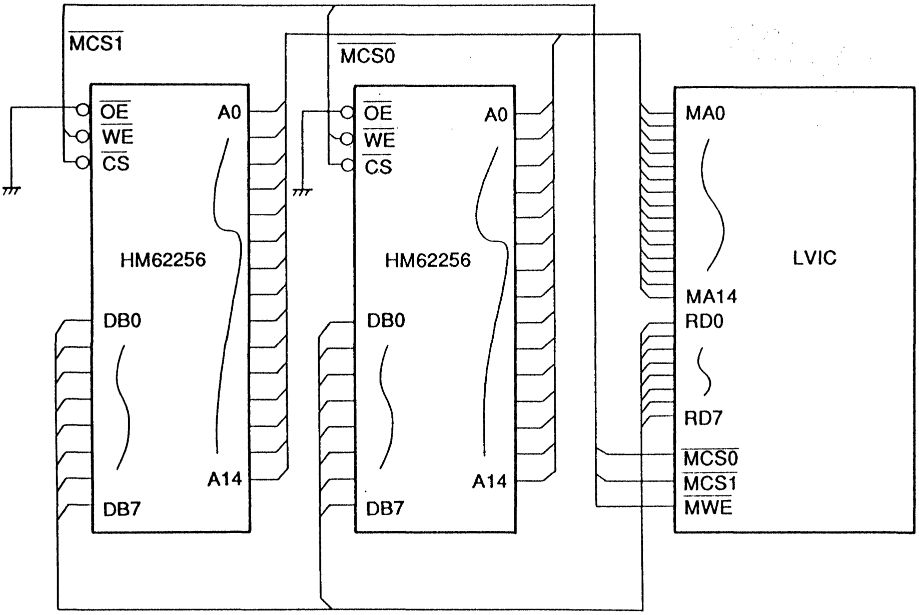


Figure 2-7 Buffer Memory Interface

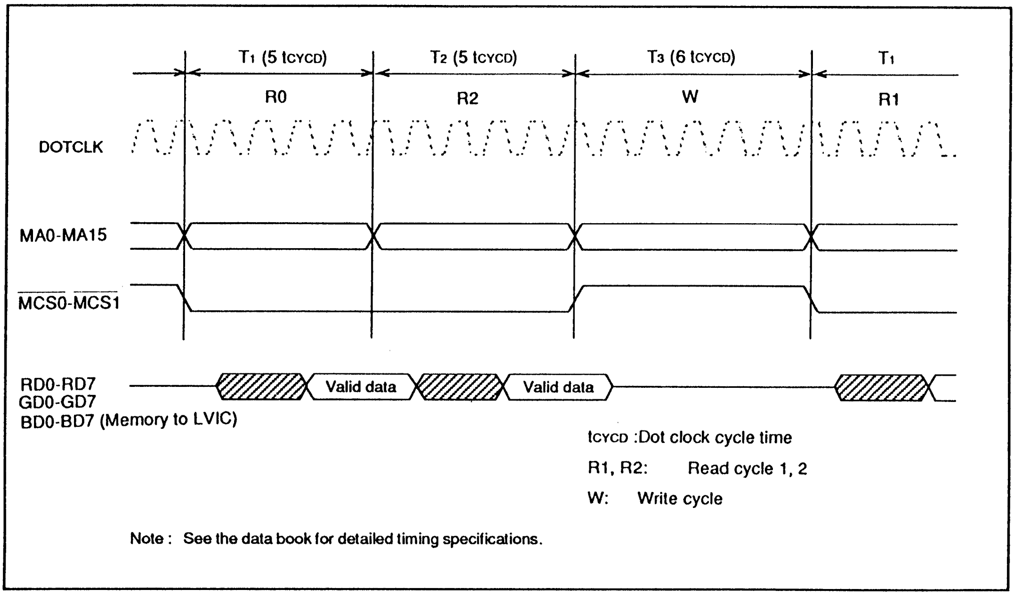


Figure 2-8 Buffer Memory Read Timing

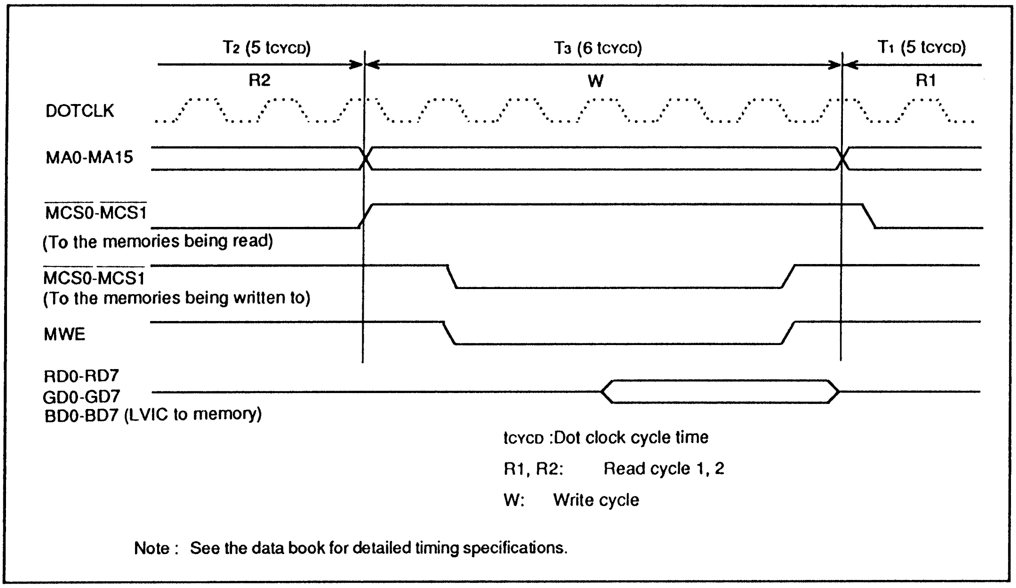


Figure 2-9 Buffer Memory Write Timing

The LVIC writes data corresponding to half a CRT display screen into buffer memories for each frame, which means it takes two frames for the LVIC to write data corresponding to one CRT display screen.

In single screen modes, the LVIC writes data to the buffer memories as shown in figure 2-10 in a specific order. In the first frame, the LVIC writes data 1, 3, 5, ..., with the A0 signal fixed low. In the second frame, the LVIC writes data 2, 4, 6, ..., with the A0 signal fixed high.

In dual screen modes, on the other hand, the LVIC writes data to the buffer memories as shown in figure 2-11. In the first frame, the LVIC writes data 1, 3, 5, ... corresponding to the top half of the screen with both the A0 and A1 signals fixed low. The LVIC then writes data A, C, E, ... corresponding to the bottom half of the screen with the A0 signal fixed high and the A1 signal low. Similarly, in the second frame, the LVIC writes data 2, 4, 6, ... for the top half of the screen with the A0 signal fixed low and the A1 signal high, then it writes data B, D, F, ... for the bottom half of the screen with both the A0 and A1 signals fixed high.

When reading from the buffer memories, the LVIC simply reads out the data from low-order addresses to high-order addresses in order.

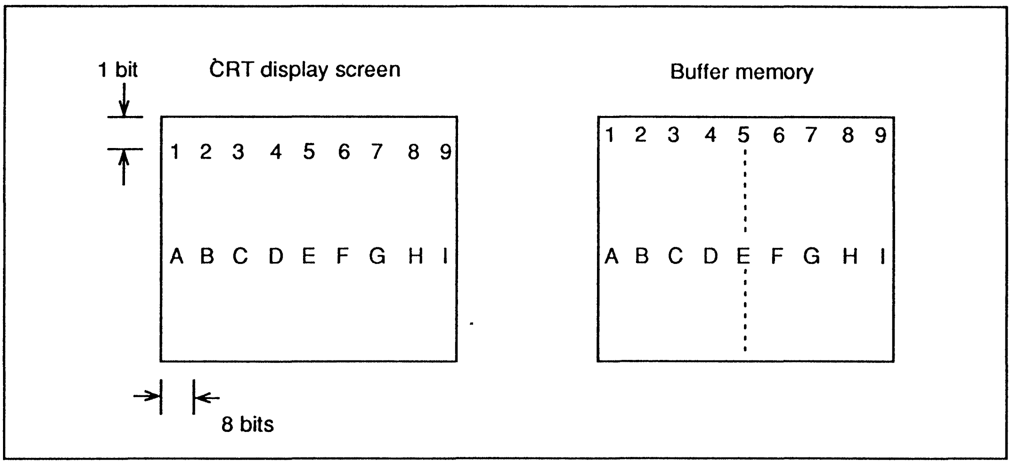


Figure 2-10 Data Arrangement in Buffer Memory in Single Screen Modes

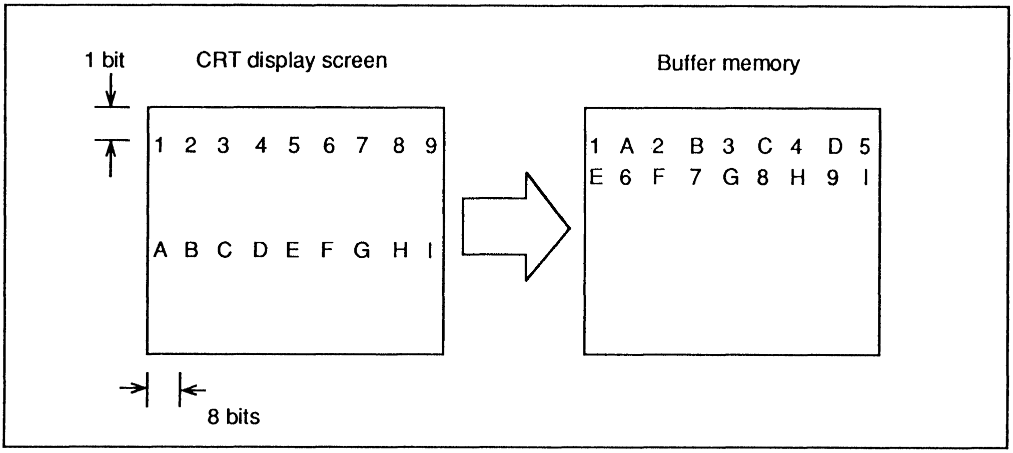


Figure 2-11 Data Arrangement in Buffer Memory in Dual Screen Modes

2.3.3 Through Mode

The LVIC can also convert CRT display data into LCD data without using buffer memory by a process called through mode. Through mode is enabled by selecting the no-memory mode with the MS0 and MS1 pins or with the MS0 and MS1 bits of control register 2 (R1).

In through mode, all LVIC operations are synchronized with the CRT display horizontal synchronization signal (HSYNC) and the vertical synchronization signal (VSYNC). Therefore, in this case it is impossible to control the LCD frame frequency (the FLM signal frequency) independently.

Figure 2-12 is the timing chart of the LCD control signals in through mode. As shown in the figure, the CL1 signal period is identical to the HSYNC signal period, and the LCD frame frequency is identical to the CRT display frame frequency (the VSYNC signal frequency). Accordingly, the CRT display frame frequency must be set to 70 Hz in order to obtain a 70 Hz LCD frame frequency, which requires rewriting the value set in the CRT controller.

The following limitations are due to the fact that it is impossible to control the LCD frame frequency and the CRT display frame frequency independently in this mode:

- Double-height displays and LCDs with Y-drivers on both sides are disabled since the LVIC cannot control the phase relation between the CL3 signal and the CL1 signal.

- The falling edge of the HSYNC signal must be synchronized with the rising edge of the VSYNC signal since the input timings of the HSYNC and the VSYNC signals are limited.
- The CL1 signal pulses for more than the number of specified displayed lines. (Refer to figure 2-12.)
- The pins for transferring data between the LVIC and buffer memory must be left open since these pins are all driven into output state.

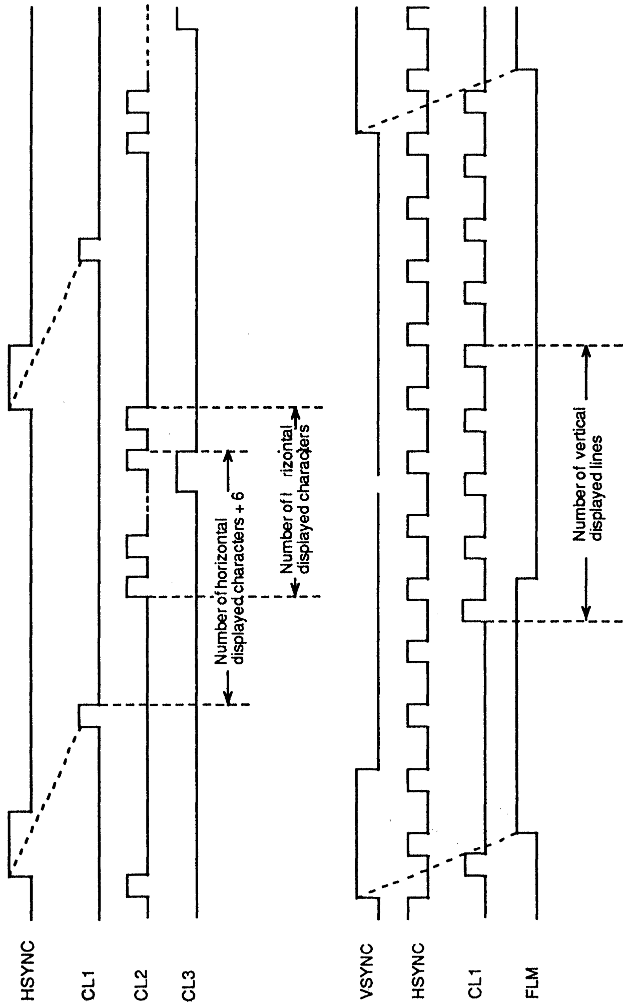

HSYNC
CL1
CL2
CL3
Number of horizontal displayed characters + 6
Number of horizontal displayed characters
VSYNC
HSYNC
CL1
FLM
Number of vertical displayed lines

Figure 2-12 Timing of LCD Control Signals in Through Mode

In addition to the limitations, note that dual screen LCDs are disabled in through mode. Setting the DM3–DM0 pins for dual screen modes prevents normal display since the LVIC transfers the high-order four bits of display data to the upper screen and the low-order four bits to the lower screen (figure 2-13).

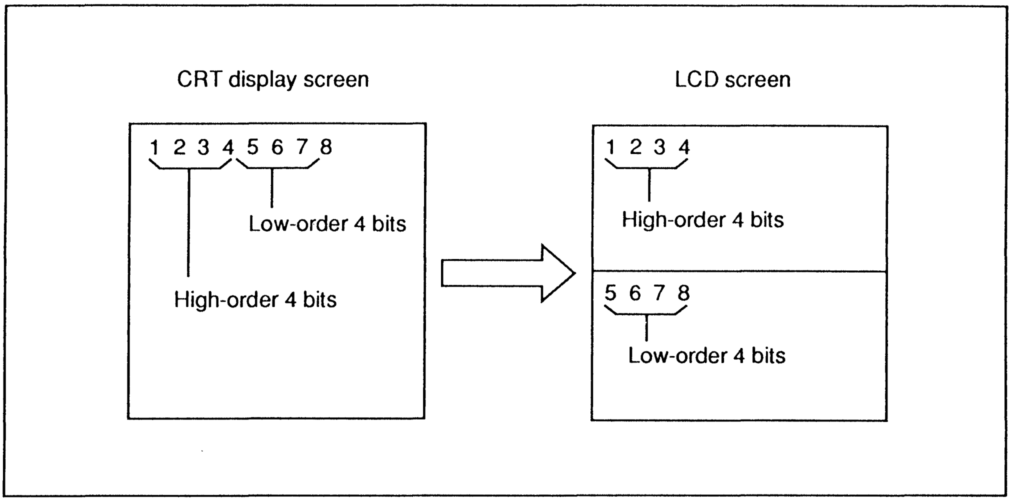


Figure 2-13 Dual Screen Mode Display in Through Mode

2.4 MPU/ROM Interface (For Programming Internal Registers)

There are two methods of controlling the LVIC: a pin programming method and an internal register programming method. The latter method is divided into an MPU programming method and a ROM programming method. The interfacing of the LVIC with an MPU or ROM for programming internal registers is described below.

2.4.1 MPU Interface

Figure 2-14 shows examples of connecting an HD64180 and an HD6301 (8-bit MPUs) to the LVIC. When an HD64180 is connected to the LVIC, input an ORed signal of the $\overline{RD}$ and $\overline{IOE}$ signals of the MPU through the LVIC's $\overline{RD}$ pin, and an ORed signal of the $\overline{WR}$ and $\overline{IOE}$ signals of the MPU through the LVIC's $\overline{WR}$ pin. The reason for this is that the MPU considers the LVIC to be an I/O device. When an HD6301 is connected to the LVIC, generate the LVIC's $\overline{RD}$ and $\overline{WR}$ signals from the HD6301's $R/\overline{W}$ and E signals, as shown in the figure.

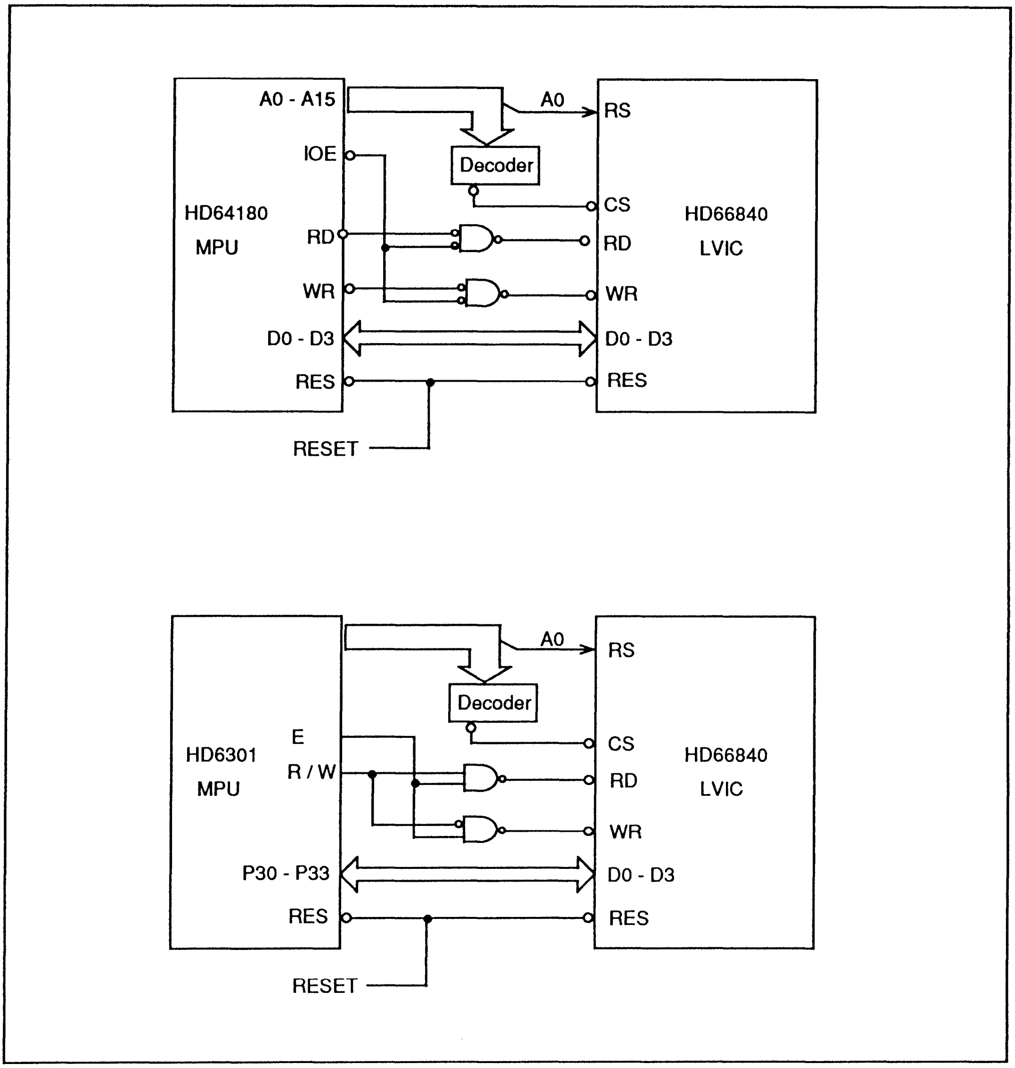


Figure 2-14 MPU Interface

Figure 2-15 is the timing chart of the MPU interface signals.

When writing data into an internal register, first set the RS signal low to select the address register (AR), then write the address of the desired register into the address register. Finally, set the RS signal high and write the data.

The procedure for reading data from a register is exactly the same as that for writing data.

Since all the internal registers consist of four bits, the high-order four bits from the MPU are not used. In addition, data write/read operations are all performed while the $\overline{CS}$ signal is low.

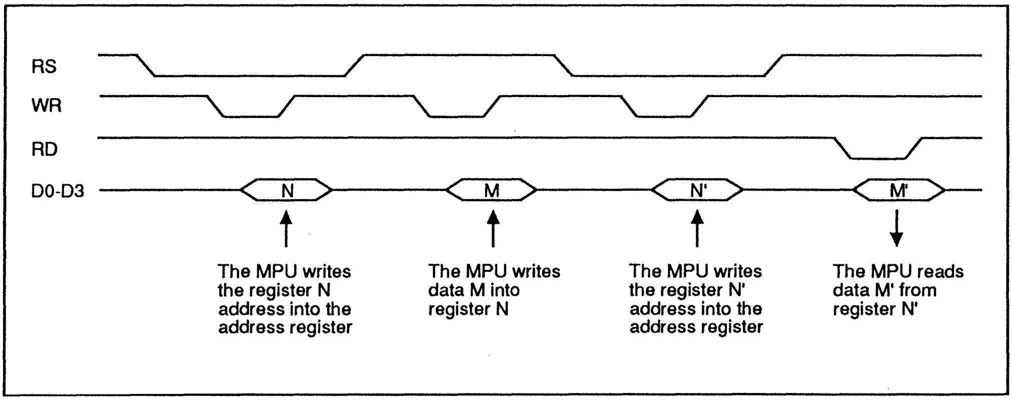

RS
WR
RD
D0-D3
N
M
N'
M'
The MPU writes the register N address into the address register
The MPU writes data M into register N
The MPU writes the register N' address into the address register
The MPU reads data M' from register N'

Figure 2-15 Timing of MPU Interface Signals

2.4.2 ROM Interface

Figure 2-16 shows an example of connecting an HN27C64 (ROM) to the LVIC. The RS, $\overline{CS}$, and $\overline{WR}$ pins must be fixed either high or low in this case. If the ROM programming method is specified, the LVIC outputs addresses $0 to $F in sequence through the A0–A3 pins. The D0–D3 pins are always in input state. Connecting the A0–A3 signals to the low-order four bits of the ROM address lines enables the LVIC to read data from the ROM and write it into the internal registers. Figure 2-17 shows the timing for this process.

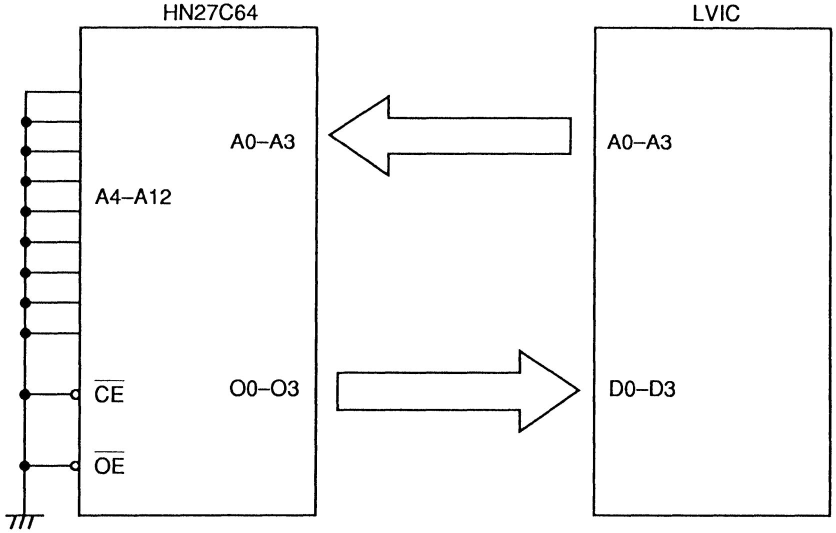


Figure 2-16 ROM Interface

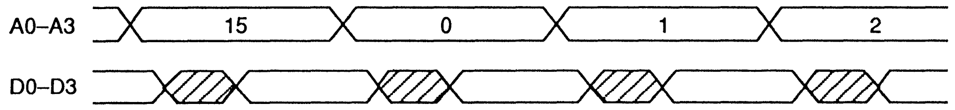


Figure 2-17 Timing of ROM Interface Signals

2.5 PLL Interface

The dot clock (DOTCLK), which is the latch clock for serial RGB data, is not a standard video signal and is not output from the CRT plug. Consequently, the DOTCLK signal must be generated outside the system. The LVIC has a programmable counter and a phase comparator. Therefore, a PLL circuit can be configured to generate the DOTCLK signal if a charge pump, a low-pass filter (LPF), and a voltage-controlled oscillator (VCO) are connected to the programmable counter and the phase comparator. Figure 2-18 is a PLL circuit diagram.

A PLL circuit is a feedback controller whose internal programmable counter generates a clock of a frequency and phase identical to those of the base clock.

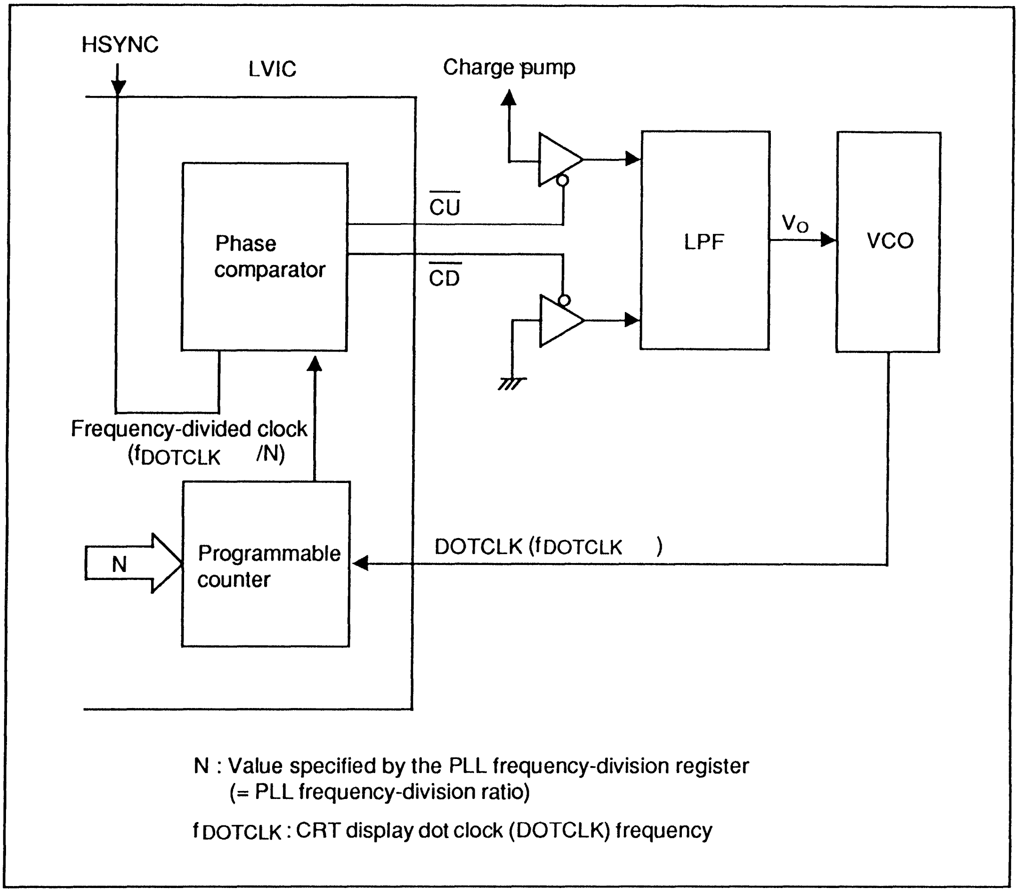
In the PLL circuit, the VCO oscillates with a frequency determined by the voltage at power-on and outputs a clock to the programmable counter. The programmable counter divides the frequency of the clock according to the value specified in the PLL frequency-division register (R10 and R11) and outputs the frequency-divided clock to the phase comparator.

The phase comparator compares the edges of the frequency-divided clock and the base clock, where the base clock is the horizontal synchronization signal (HSYNC). The phase comparator outputs the $\overline{\text{CD}}$ signal to the charge pump and the LPF when the frequency of the frequency-divided clock is higher than that of the HSYNC signal, or when the phase of the frequency-divided clock is ahead of that of the HSYNC signal. Otherwise, the phase comparator outputs the $\overline{\text{CU}}$ signal. Figure 2-19 shows the timing for the phase comparator outputs.

The charge pump and the LPF apply a voltage to the VCO according to the $\overline{\text{CD}}$ or the $\overline{\text{CU}}$ signal.

The PLL circuit repeats this operation until the phase and frequency of the frequency-divided clock coincide with those of the HSYNC signal. The PLL circuit subsequently supplies a stable DOTCLK signal.

Since the LVIC outputs the $\overline{\text{CD}}$ and $\overline{\text{CU}}$ signals at CMOS levels, both CMOS-level and TTL-level elements can be used for the charge pump.



N : Value specified by the PLL frequency-division register
(= PLL frequency-division ratio)

f DOTCLK : CRT display dot clock (DOTCLK) frequency

Figure 2-18 Phase Comprator Output Timing

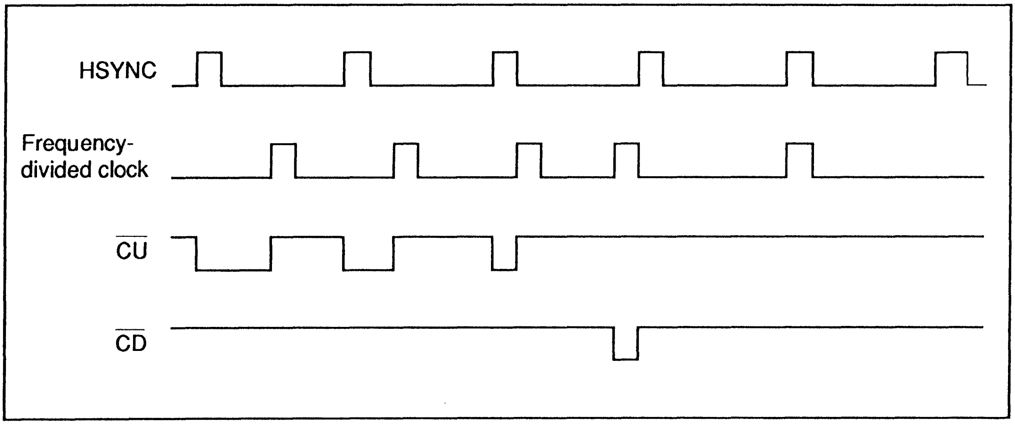


Figure 2-19 PLL Circuit Block Diagram

Section 3 LVIC Functions and Register and Pin Settings

Either of two methods may be selected to control LVIC functions: an internal register programming method or a pin programming method. The former method controls LVIC functions by setting parameters in the internal registers, and the latter method controls them by setting mode setting pins high or low. The internal register programming method can be subdivided into an MPU programming method and a ROM programming method, as described in section 2.

When using the LVIC, first select a programming method with the PMOD0 and PMOD1 pins. For details of programming method selection, see table 1-5 in section 1.5.5, Mode Setting Pins. The internal register programming method must be selected, by setting (PMOD0, PMOD1) = (0, 1) or (1, 0), in the following cases:

- When programming a screen size which the pin programming method cannot support.
- When generating the display timing signal (DISPTMG) internally.
- When generating the dot clock (DOTCLK) with the PLL circuit.
- When alternating the M signal every line in a monochrome or 8-level gray scale display mode.
- When controlling LCD on/off.

Select either the pin programming method or the internal register programming method in all other cases.

Table 3-1 shows what is actually used to control the various LVIC functions after a programming method is selected with the PMOD0 and PMOD1 pins.

This section explains the LVIC functions and how to control them by the internal registers or pins.

Table 3-1 LVIC Functions and Control Methods

Function	Controlled by:	Note	Reference Section
Display Mode Setting	Pins	1	6 Display Mode Settings and Contents
Screen Size Setting	Pins or internal registers	2	3.1 Screen Size Setting
Display Timing Signal Generation (Horizontal and Vertical Back Porch Specification)	Internal registers	—	3.2 Display Timing Signal Generation
Dot Clock Generation (PLL Frequency-Division Ratio Specification)	Internal registers	—	3.3 Dot Clock Generation
Display Timing Signal Fine Adjustment	Pins or internal registers	—	3.4 Display Timing Signal Fine Adjustment
LCD Driving Signal Alternation Selection	Internal registers	3	3.5 LCD Driving Signal Alternation
Buffer Memory Selection	Pins or internal registers	—	3.6 Buffer Memory Selection
Display On/Off Control	Internal registers	4	3.7 Display On/Off Control
RGB Signal Latch Timing Selection	Pins	1	3.8 Video Signal Latch Timing Selection
VSYNC Signal Polarity Selection	Pins	1	3.9 Vertical Synchronization Polarity Selection

Notes:

1. Only pins can control this function, even if the internal register programming method is selected with the PMOD0 and PMOD1 pins.
2. The pin programming method cannot support all sizes.
3. The pin programming method fixes LCD driving signals to alternate every frame in display modes 1–8 and every line in display modes 9–16.
4. The pin programming method fixes the LCD to be always on.

3.1 Screen Size Setting

3.1.1 Screen Size Control

Either the internal registers or the pins can be used to control screen size.

In the internal register programming method, any even number from 4 to 506 (32 to 4048 dots) can be selected as the number of horizontal displayed characters), using the horizontal displayed characters register (R6 and R7). Similarly, any even number from 4 to 1028 can be selected as the number of vertical displayed lines with the vertical displayed lines register (R2, R3, and the high-order two bits of R4). However, an odd number of lines can also be selected in the single screen modes with Y-drivers on one side, that is, in display modes 2, 4, 7–9, 11, 13, and 15. Note that it is not the multiplexing duty ratio but the number of displayed lines that is specified. This means that the specified value does not depend on screen configuration.

In the pin programming method, 80 or 90 characters (640 or 720 dots) can be selected as the number of horizontal displayed characters with the XDOT pin, and 200, 350, 400, 480, 512, or 540 lines can be selected as the number of vertical displayed lines with the YL–YL0 pins (table 1-7). Up to 15 lines can be added with the ADJ and F3–F0 pins to the number of vertical displayed lines specified with the YL2–YL0 pins. (Refer to section 1.5.5, Mode Setting Pins.)

Figure 3-1 shows the relationship between an LCD screen and the pins and internal registers controlling screen size.

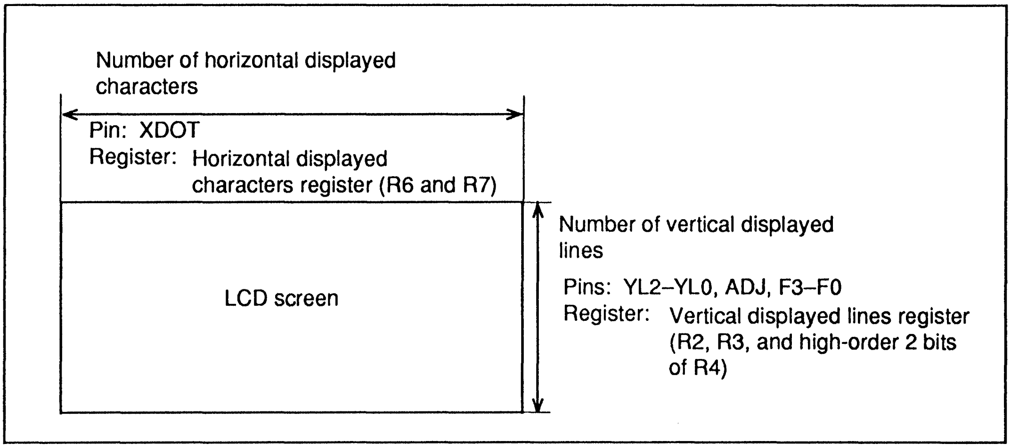

Number of horizontal displayed characters
Pin: XDOT
Register: Horizontal displayed characters register (R6 and R7)
LCD screen
Number of vertical displayed lines
Pins: YL2–YL0, ADJ, F3–F0
Register: Vertical displayed lines register (R2, R3, and high-order 2 bits of R4)

Figure 3-1 Relationship between LCD Screen and Pins/Internal Registers

3.1.2 Setting Examples

Figures 3-2 to 3-5 show screen size examples. Tables 3-2 and 3-3 show the setting of registers and pins corresponding to each of the screen sizes.

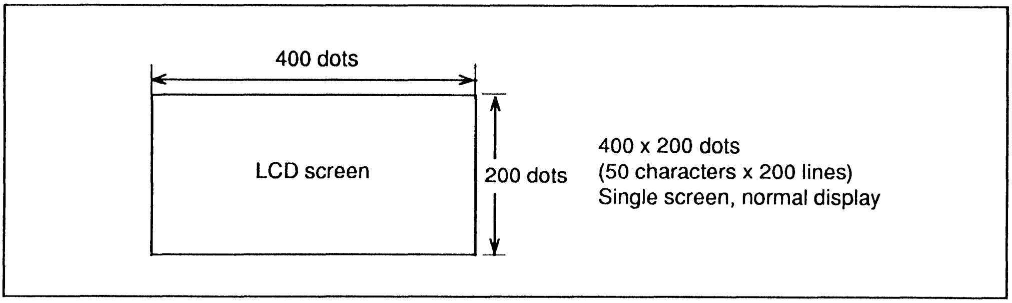


Figure 3-2 LCD Screen Example 1

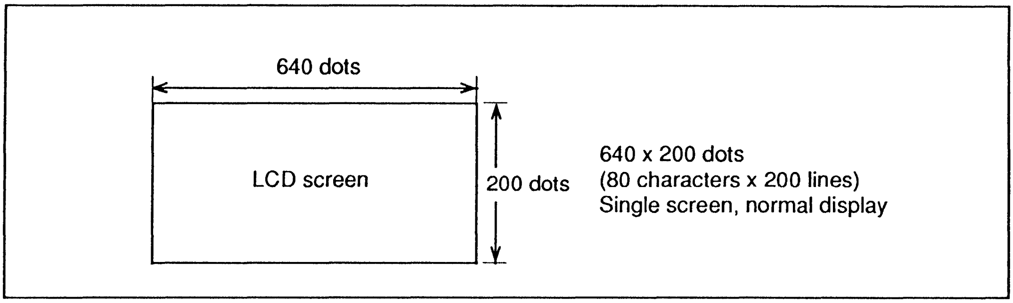


Figure 3-3 LCD Screen Example 2

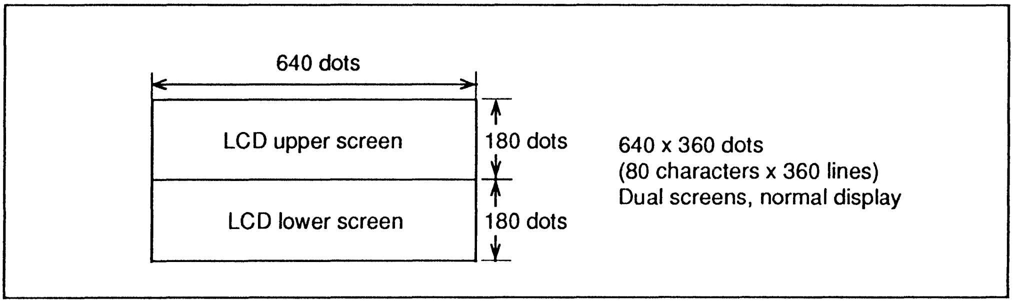
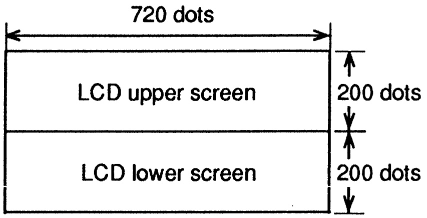


Figure 3-4 LCD Screen Example 3



720 x 400 dots
(90 characters x 400 lines)
Dual screens,
double-height display

Figure 3-5 LCD Screen Example 4

Table 3-2 Internal Register Settings for Different LCD Screen Sizes

	Values to be Written	
Reference Figure	**Horizontal Displayed Characters Register**	**Vertical Displayed Lines Register**
3-2	24 (00011000)	199 (0011000111)
3-3	39 (00100111)	199 (0011000111)
3-4	39 (00100111)	359 (0101100111)
3-5	44 (00101100)	199 (0011000111)

Table 3-3 Pin Settings for Different LCD Screen Sizes

Reference Figure	XDOT	YL2	YL1	YL0	ADJ	F3	F2	F1	F0	Note
3-2	—	—	—	—	—	—	—	—	—	1
3-3	0	0	0	0	—	—	—	—	—	2
3-4	0	0	0	1	0	1	0	1	0	3
3-5	1	0	0	0	—	—	—	—	—	2

Notes:

1. Cannot be programmed with pins.
2. The ADJ and F3–F0 pin settings depend on whether the display timing signal (DISPTMG) is adjusted.
3. Ten lines are added to the number of vertical displayed lines originally specified by the vertical displayed lines register.

3.2 Display Timing Signal Generation

The display timing signal (DISPTMG) function and the register setting for generating the signal are described below.

3.2.1 Display Timing Signal Function

CRT display data is divided into display period data and retrace period data, but only display period data is necessary for an LCD. Therefore, the LVIC requires the display timing signal (DISPTMG) which indicates whether the data transferred is display period data or retrace period data. The LVIC writes to buffer memory as valid data only the data transferred during the display period.

Figure 3-6 is a conceptual diagram illustrating the relationship between the CRT display period, retrace period, and an LCD screen. Figure 3-7 is the corresponding timing chart.

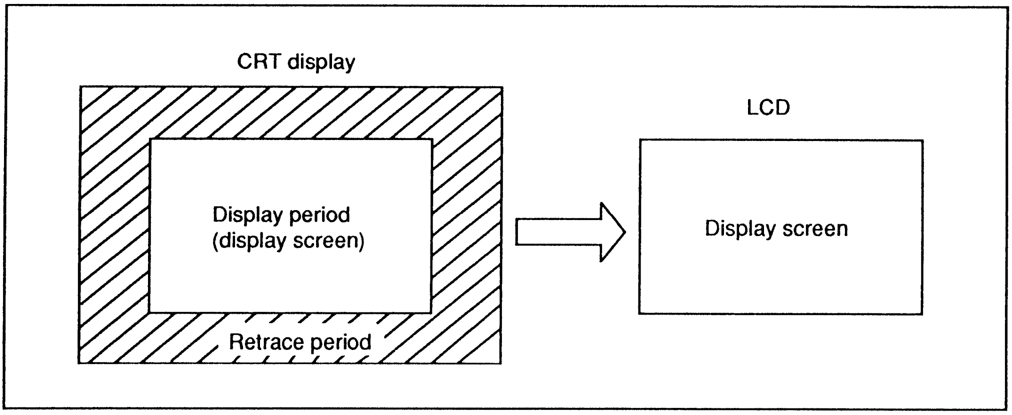


Figure 3-6 CRT Display Period, Retrace Period, and LCD Screen

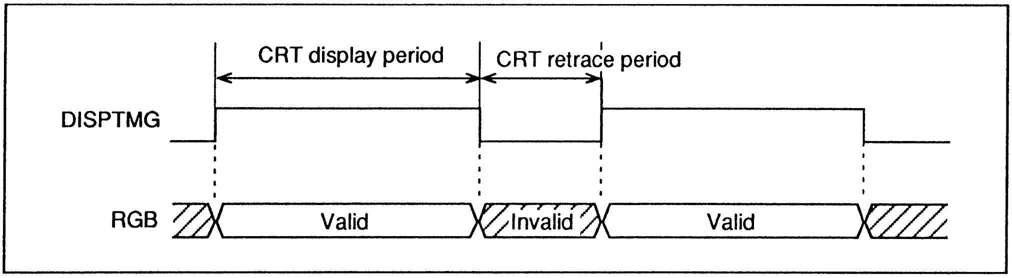
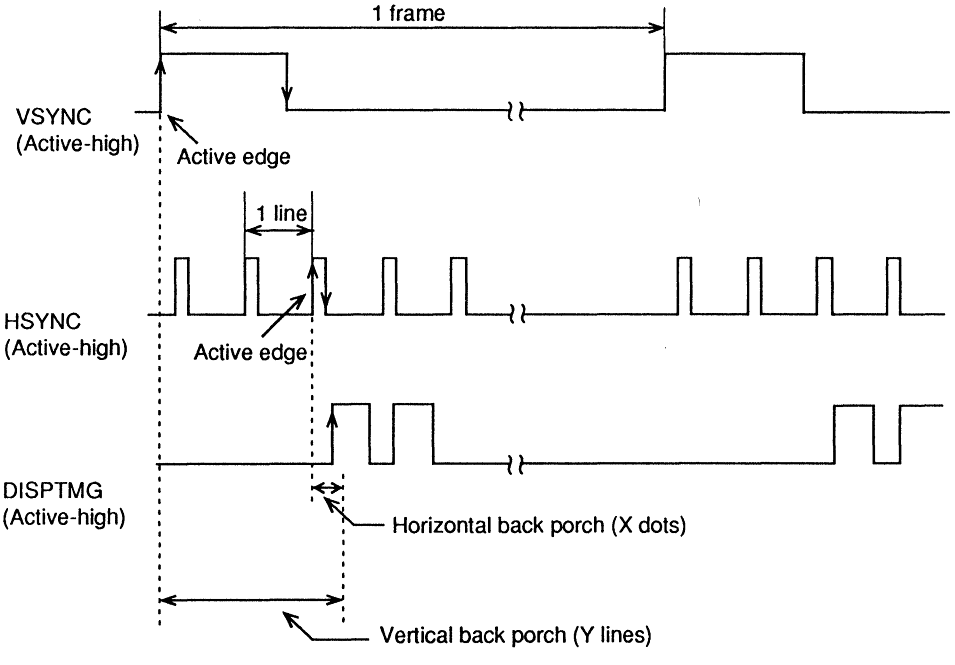


Figure 3-7 Display Timing Signal (DISPTMG) and RGB Signal

3.2.2 Display Timing Signal Generation and Register Setting

The LVIC can generate the display timing signal (DISPTMG) from the vertical synchronization (VSYNC) and horizontal synchronization (HSYNC) signals.

Figure 3-8 shows the relationships between the timings of the HSYNC, VSYNC, and DISPTMG signals. In this figure, the rising edge of the HSYNC signal appears at the same time or a little after the falling edge of the VSYNC signal. Similarly, the rising edge of the DISPTMG signal (display start position) appears at the same time or a little after the rising edge of the HSYNC signal. The phase shift between the rising edge of the VSYNC signal and that of the DISPTMG signal is called the vertical back porch and the phase shift between the rising edge of the HSYNC signal (the rising edge just before the rising edge of the DISPTMG signal) and that of the DISPTMG signal is called the horizontal back porch.



Note: The VSYNC and HSYNC signals can be active-low.

Figure 3-8 Vertical and Horizontal Back Porches

The vertical and horizontal back porches must be specified with the internal registers to generate the DISPTMG signal. The vertical back porch is expressed by a number of lines Y, and the horizontal back porch by a number of dots X.

First set 1 in the DSP bit or the DCK bit of control register 1 (R0) to specify the vertical back porch register (R12: high-order, R13: low-order) and the horizontal back porch register (R14: high-order, R15: low-order). Then write the appropriate values into the registers. The values to be written into the registers can be obtained from the following equations:

Value in R12 and R13 = vertical back porch time × f_{HSYNC} – 1 ....(3-1)
Value in R14 and R15 = horizontal back porch time × f_{DOTCLK} – 1 ....(3-2)
f_{HSYNC}: HSYNC signal frequency
f_{DOTCLK}: CRT display dot clock (DOTCLK) frequency

The back porch times must be actually measured, since they depend on the CRT display system. When measuring the back porch times, note that the back porch time definitions of the LVIC differ from those of a CRT display and that the back porch times in equations 3-1 and 3-2 follow the LVIC definitions (table 3-4, figure 3-9).

Table 3-4 Comparison of Back Porch Time Definitions

Term	CRT or LVIC	Definition
Vertical Back Porch Time	CRT	Interval between active edges of the VSYNC signal and the DISPTMG signal
	LVIC	Same as above
Horizontal Back Porch Time	CRT	Interval between the **active** edge of the HSYNC signal (just before the rising edge of the DISPTMG signal) and the rising edge of the DISPTMG signal
	LVIC	Interval between the **rising** edge of the HSYNC signal (just before the rising edge of the DISPTMG signal) and the rising edge of the DISPTMG signal

Note: The SPS pin must be high when the VSYNC signal is active-high, or low otherwise.

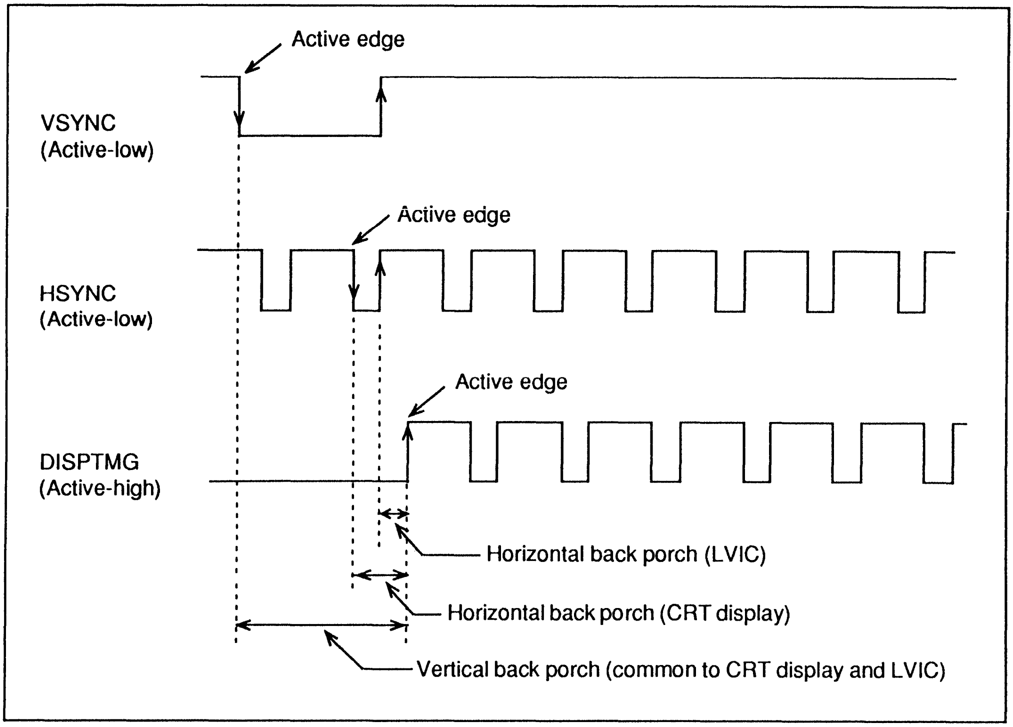

Active edge
VSYNC
(Active-low)
Active edge
HSYNC
(Active-low)
Active edge
DISPTMG
(Active-high)
Horizontal back porch (LVIC)
Horizontal back porch (CRT display)
Vertical back porch (common to CRT display and LVIC)

Figure 3-9 Comparison of Back Porch Time Definitions

Table 3-5 shows the settings for R12–R15 when the LVIC is used with an IBM-PC/AT CGA board.

Table 3-5 Back Porch Register Settings for the IBM-PC/AT CGA Board

	Data Bits				
Register	**3**	**2**	**1**	**0**	**Contents**
R12	0	0	1	0	Vertical back porch: 37 lines
R13	0	1	0	0	
R14	1	0	1	1	Horizontal back porch: 177 dots
R15	0	0	0	0	

Notes:

1. The above back porches were actually measured.
2. The SPS pin is high.

3.3 Dot Clock Generation

The LVIC can generate a dot clock (DOTCLK), which acts as a latch clock for CRT display data, from the horizontal synchronization signal (HSYNC). The parameter setting for DOTCLK signal generation by a PLL circuit and how to design the PLL circuit are described below. Refer to section 2.5, PLL Interface, for information on how the PLL circuit generates the DOTCLK signal.

3.3.1 Parameter Setting for Dot Clock Generation

To generate the dot clock (DOTCLK), first set 1 in the DCK bit of control register 1 (R0) to specify the PLL frequency-division register (R10: high-order, R11: low-order). Then set the parameter into the register. The PLL circuit generates the DOTCLK signal according to the frequency-division ratio specified by this register.

The value to be written into the frequency-division register is (frequency-division ratio (NPLL)) – 731. NPLL can be obtained from one of the following equations:

NPLL = fDOTCLK/fHSYNC .... (3-3)

fDOTCLK: DOTCLK signal frequency

fHSYNC: HSYNC signal frequency

or

NPLL = (total number of horizontal characters on the CRT display) × (horizontal character pitch) .... (3-4)

Horizontal character pitch: Number of horizontal dots for one character

Table 3-6 lists the PLL frequency-division ratios for major personal computers.

Table 3-6 PLL Frequency-Division Ratios for Major Personal Computers

Personal Computer	Screen Size (Dots)	f_{DOTCLK} (MHz)	f_{HSYNC} (kHz)	PLL Frequency-Division Ratio	Value in R10 and R11
PC-8801	640 × 200	14.318	15.98	896	$A5 = 10100101 (binary)
PC-9801	640 × 400	21.0526	24.83	848	$75 = 01110101 (binary)
FM-11	640 × 400	21.0526	24.366	864	$85 = 10000101 (binary)
FM-16B	640 × 400	21.0526	24.366	864	$85 = 10000101 (binary)
B16/SX	640 × 400	21.0526	24.83	848	$75 = 01110101 (binary)
B16/MX	640 × 400	23.9616	29.36	816	$55 = 01010101 (binary)
IBM-PC™/AT CGA	640 × 200	14.318	15.75	912	$B5 = 10110101 (binary)
EGA	640 × 350	16.257	21.85	744	$0D = 00001101 (binary)
VGA	640 × 480	28.321	31.5	899	$A8 = 10101000 (binary)
	720 × 350	25.175	31.5	796	$41 = 01000001 (binary)

3.3.2 PLL Circuit Design

This section explains how to design a PLL circuit to suit a CGA or EGA board.

VCO Design: An LPF must be designed to determine the response characteristics of the entire PLL circuit. However, before the LPF is designed, K_V (Mrad/s/V), which is the control sensitivity factor of a VCO, must be determined.

In this case, a Clapp oscillator circuit is used as a high-frequency oscillator, as shown in figure 3-10. The oscillation frequency (f) of this circuit can be obtained from the following equations:

$$f = 1/2\pi\sqrt{LC} \ldots\ldots\ldots\ldots \quad (3\text{-}5)$$

$$C = C_O + C_T + \{1/(1/C_{11} + 1/C_{12} + 1/C_{13})\} = C_O + C_T + C_I \ldots\ldots \quad (3\text{-}6)$$

Check whether the circuit is oscillating after setting L and C to obtain the desired frequency f or not. Increase the value of C_O with $C_{11} = C_{12} = C_{13} = 100$ pF. Use a 100-pF capacitor as C_T and fix the C_T value to half the value of its maximum capacitance, that is, to about 50 pF, to stop the oscillation at a certain point. The resulting value of C_O is called C_{Omax}.

Construct C_O with varicaps and capacitors as shown in figure 3-11. The capacitance of the varicaps depends on V_{ref}, the reverse voltage. In this case, the value of C_O is expressed as follows:

$C_O = 1/(2/C_D + 1/C_{10})$ .... (3-7)
C_D: Varicap capacitance

Set C_{10} to a value such that C_O is about $0.8C_{Omax}$. The varicaps used here are ISV149s which have a maximum capacitance of 300 pF when the LPF outputs a voltage from 2 V to 8 V. Therefore the correct value of C_{10} is around 330 pF.

Next, determine the value of L that makes the VCO oscillate at the same frequency as that of the PLL circuit. In the circuit shown here, f is 18 MHz, C_D is 25 pF, and C_T is 15 pF when V_{ref} is 8 V. The value of L is expressed as follows:

$L = 1/(2\pi f)^2 c = 1.29\ (\mu H)$ .... (3-8)

When V_{ref} is 2 V, f is 11.2 MHz.

If the upper and lower limits of the control voltage are expressed as V_{refH} and V_{refL}, respectively, and the oscillation frequency at each voltage is expressed as f_H (18 MHz) and f_L (11.2 MHz), respectively, K_V, the control sensitivity factor of the VCO, is expressed as follows:

$K_V = \{(f_H - f_L)/(V_{refH} - V_{refL})\} \times 2\pi$ .... (3-9)
$\therefore K_V = 7.1$ (Mrad/s/V)

However, the value of K_V in equations below is assumed to be 8.0, since this is the actually measured value.

Bias the circuit according to the transistors' values; any lag in the oscillation frequency can be adjusted with C_T.

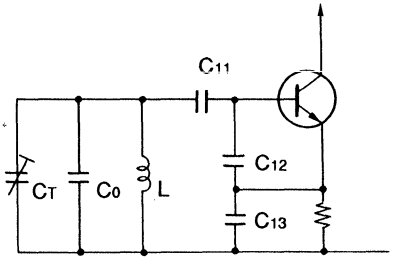
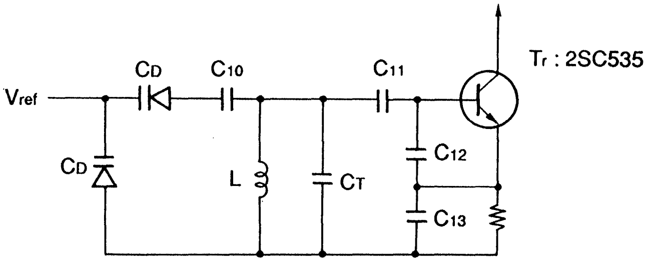


Figure 3-10 Clapp Oscillator Circuit



$C_{11}=C_{12}=C_{13}=100$ pF

$C_{10}=330$ pF

C_D ; ISV149 Ⓐ

Figure 3-11 Co Structure

LPF Design: An active filter is used as the LPF in figure 3-12. In this case, the entire PLL circuit is considered to be a secondary feedback control system. Therefore, first calculate the damping factor ζ and the natural frequency ωn, which determine the control system characteristics, then determine the values of C and R.

- **Damping Factor ζ:** According to figure 3-13, when frequency overshoot does not exceed 25%, ζ is 0.6.
- **Natural Frequency ωn:** From the frequency step response shown in figure 3-13, when the frequency difference does not exceed 5%, $\omega n \cdot t$ is 4.5. t is the pull-in time, and if t = 10 (ms), $\omega n \cdot t$ is expressed as follows:

$$\omega n \cdot t = 4.5/t = 450 \text{ (rad/s)}$$

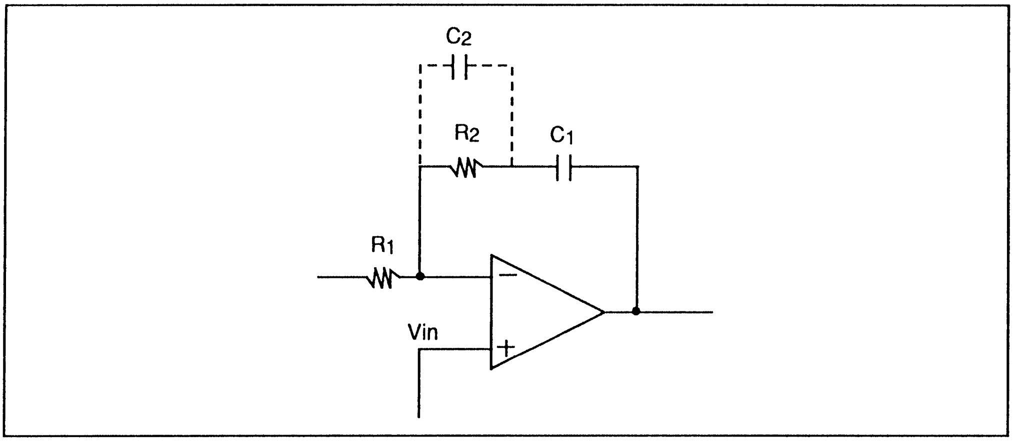


Figure 3-12 Active Filter

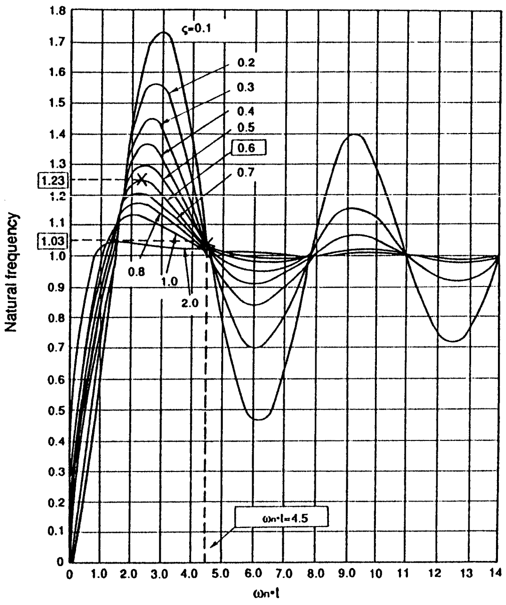


Figure 3-13 Second-Order Step Response

The values of C and R of the active filter can be obtained from the following equations:

$\zeta = (T_2/2)\sqrt{K_C \cdot K_P \cdot K_V / N \cdot T_1}$ .... (3-10)

$\omega n = \sqrt{K_C \cdot K_P \cdot K_V / N \cdot T_1}$ .... (3-11)

Where $T_1 = C_1 \cdot R_1$, $T_2 = C_1 \cdot R_2$, $K_C \fallingdotseq 1.0$ (from actual measurements), and N is the frequency-division ratio (986). K_P is the gain constant of the phase comparator (charge pump) and is expressed as follows:

$K_P = (V_{OH} - V_{OL})/4\pi$ (V/rad) .... (3-12)

The charge pump's output is at TTL level in this case, so, if $V_{OH} = 2.3$ and $V_{OL} = 0.9$, $K_P = 0.111$ V/rad. C_1 in equations 3-10 and 3-11 remains unknown. However, the values of R_1 and R_2 can be determined as follows, assuming that $C_1 = 0.22$ μF:

$R_1 = K_C \cdot K_P \cdot K_V / \omega n^2 \cdot N \cdot C_1 = 20.2 \approx 22$ (kΩ)
$R_2 = 2\zeta / \omega n \cdot C_1 = 12.1 \approx 12$ (kΩ)

Since a high-frequency element appears in the LPF's output because of the LPF's own frequency characteristics, connect a capacitor C2 of a capacitance about 1/10 that of C1 in parallel with R2 to reduce spike noise.

Operational Amplifier Standard Voltage: In figure 3-14, the three-state buffer applies 2.3 V when the $\overline{\text{CD}}$ signal is low, and 0.9 V when the $\overline{\text{CU}}$ signal is low. The operational amplifier charges C1 when the buffer outputs 2.3 V, and discharges it when the buffer outputs 0.9 V. Therefore, the value of Vin for the operational amplifier should be set to a value midway between VOH and VOL. Since the output voltage from the operational amplifier is the inverse of the input voltage, it may be a negative voltage. To cope with this, a clamp diode is connected to the operational amplifier's output in this case. Diode D2 corrects phase shift.

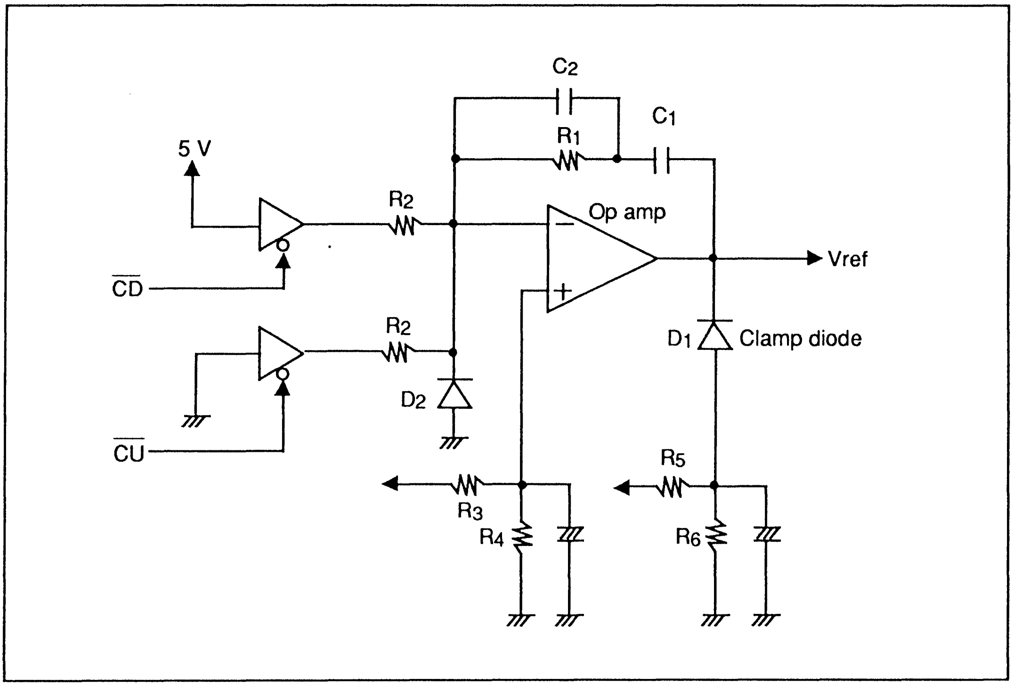


Figure 3-14 Charge Pump and LPF

This completes the design of the PLL circuit. For a complete circuit diagram, see figure 8-4. Tr2 in the figure is an emitter follower which supplies clock pulses to external circuits.

Figures 3-15 and 3-16 show two more examples of PLL circuits. The circuit shown in figure 3-15 can generate both 21-MHz and 14-MHz DOTCLK signals. The circuit shown in figure 3-16 has less jitter than the circuit of figure 3-15 and generates a 30-MHz DOTCLK signal.

Note the following suggestions for designing PLL circuits:

- Isolate Vcc and GND of analog units from those of digital units.
- Shorten the wires used for analog units to reduce noise.

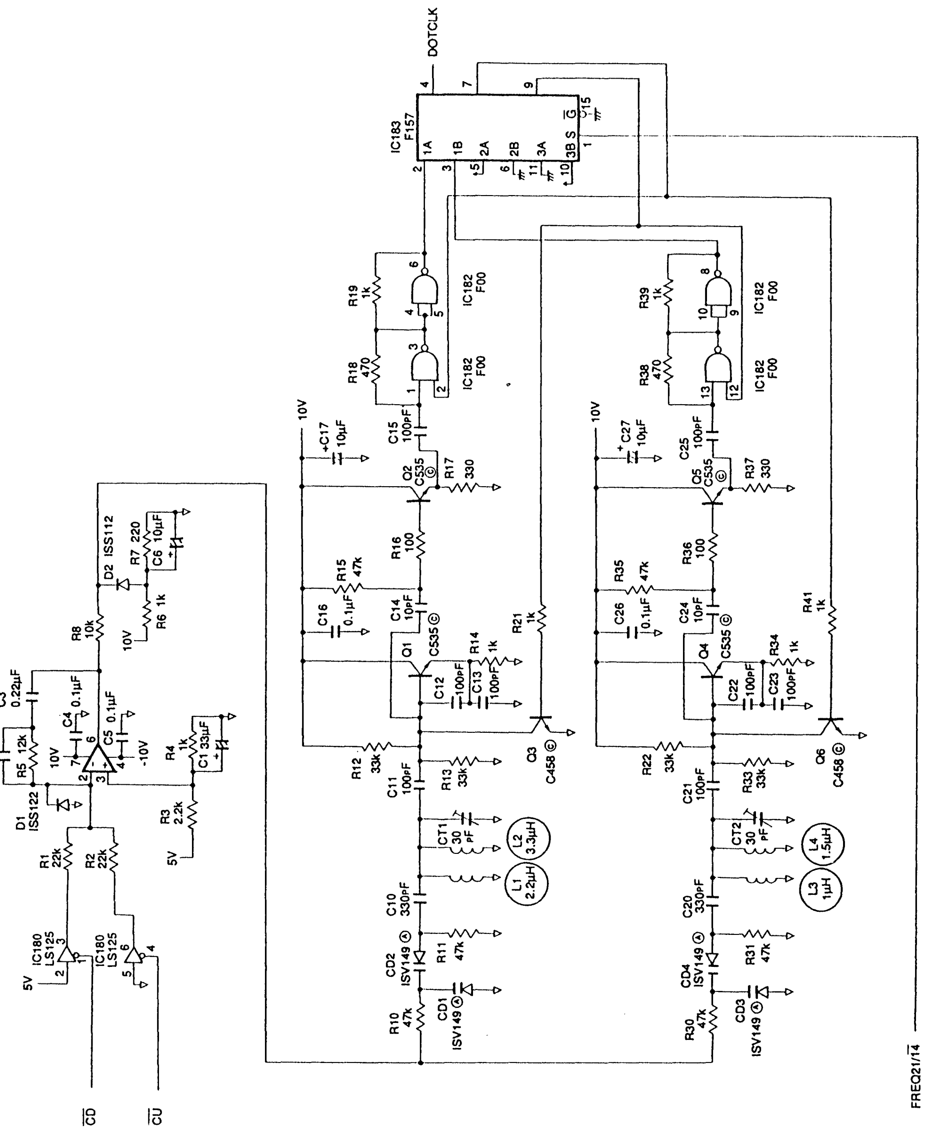


Figure 3-15 PLL Circuit Example 1

(Oscillation Frequencies: 21 MHz and 14 MHz)

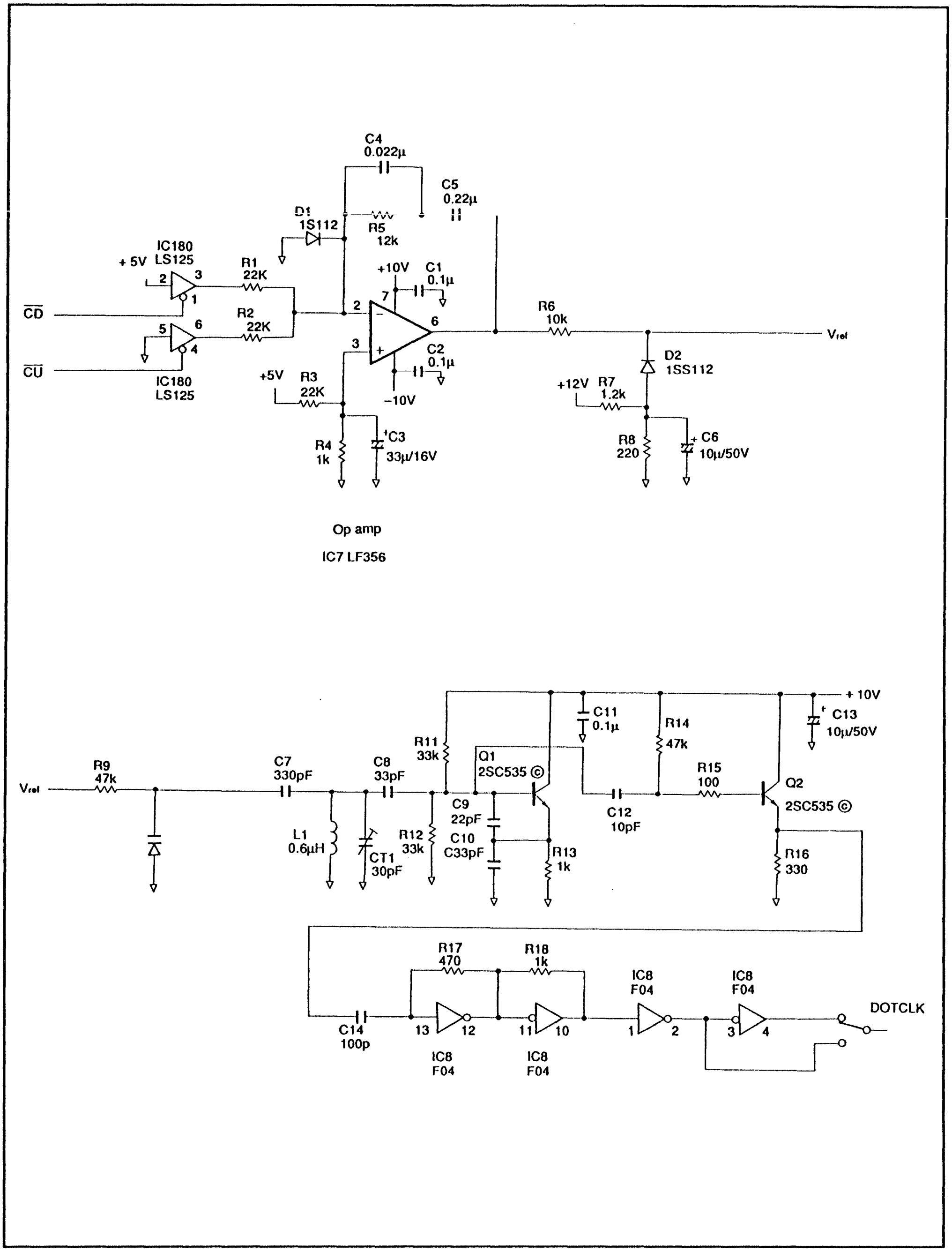


Figure 3-16 PLL Circuit Example 2
(Low-Jitter Type, Oscillation Frequency: 30 MHz)

3.4 Display Timing Signal Fine Adjustment

When the display timing signal (DISPTMG) is supplied externally, a phase shift may appear between the CRT display data and the DISPTMG signal. This is because each signal has its own specific lag characteristics. The DISPTMG signal can be adjusted with the F3–F0 pins of the LVIC or with its fine adjust register (R9) to correct the phase shift.

Table 3-7 shows the relationship between the F3–F0 pins, the fine adjust register, and the fine adjustment. In the table,–indicates advancing the DISPTMG signal phase, and + indicates delaying it. The F3 pin or data bit 3 of the fine adjust register selects the polarity. The adjustment reference point is the display start position.

Table 3-7 Fine Adjustment with F3–F0 Pins or R9

Pin:	**F3**	**F2**	**F1**	**F0**	
R9 Bit:	**3**	**2**	**1**	**0**	**Number of Adjustment Dots**
	0	0	0	0	0
		0	0	1	−1
		⋮	⋮	⋮	⋮
		1	1	0	−6
		1	1	1	−7
	1	0	0	0	0
		0	0	1	+1
		⋮	⋮	⋮	⋮
		1	1	0	+6
		1	1	1	+7

Figure 3-17 shows examples of adjusting the DISPTMG signal. In example (1), since the signal is two dots ahead of the display start position, either (F3, F2, F1, F0) or (R9 bits 3, 2, 1, 0) should be set to (1, 0, 1, 0) to delay the signal two dots. In example (2), since the signal is two dots behind the display start position, the pins or bits should be set to (0, 0, 1, 0) to advance the signal two dots. If there is no need to adjust the signal, a setting of either (0, 0, 0, 0) or (1, 0, 1, 0) will do.

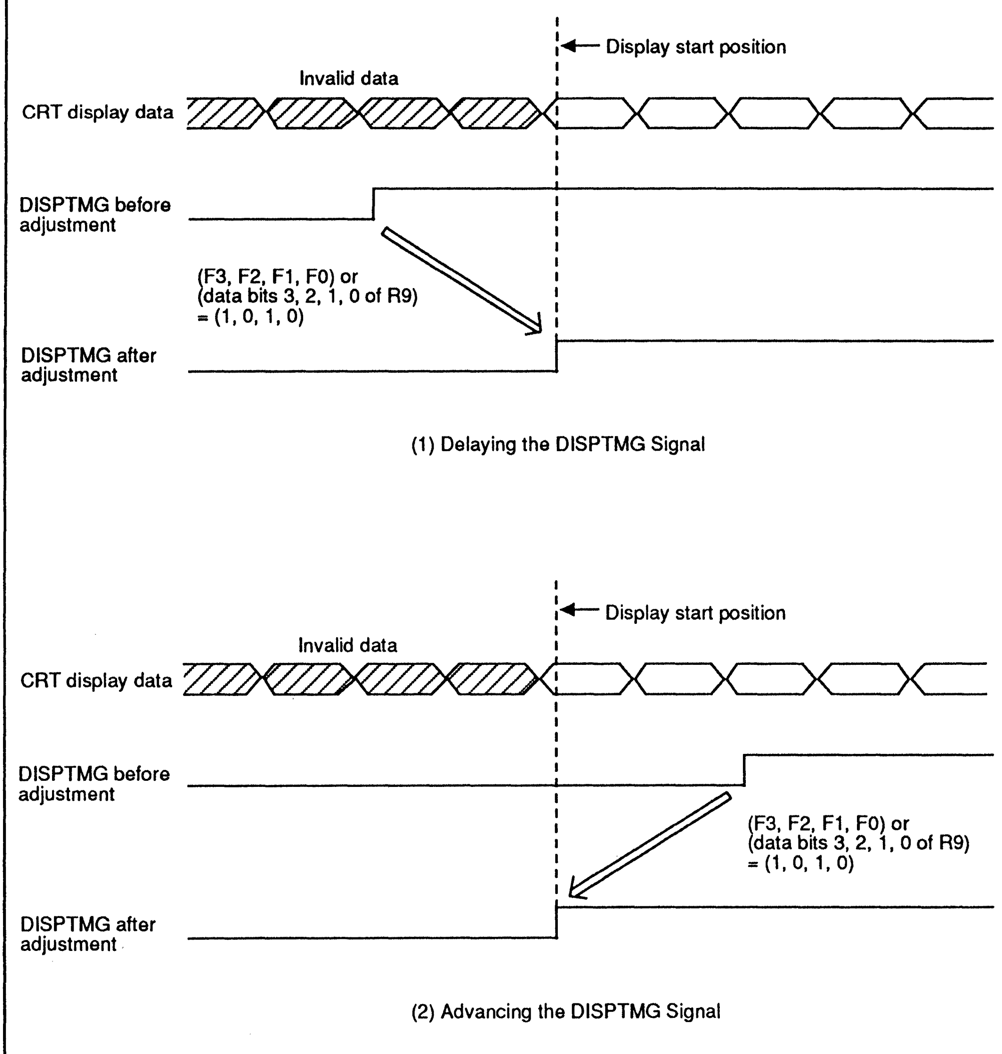

Display start position
Invalid data
CRT display data
DISPTMG before adjustment
(F3, F2, F1, F0) or (data bits 3, 2, 1, 0 of R9) = (1, 0, 1, 0)
DISPTMG after adjustment
(1) Delaying the DISPTMG Signal
Display start position
Invalid data
CRT display data
DISPTMG before adjustment
(F3, F2, F1, F0) or (data bits 3, 2, 1, 0 of R9) = (1, 0, 1, 0)
DISPTMG after adjustment
(2) Advancing the DISPTMG Signal

Figure 3-17 DISPTMG Signal Adjustment

3.5 LCD Driving Signal Alternation

Since the application of a DC voltage degrades liquid-crystal molecules, the LCD driving signals must be converted into AC voltages. The LVIC outputs the M signal which converts the LCD driving signals into AC voltages. There are two types of M signal alternation: frame alternation and line alternation. The alternation of LCD driving signals depends on that of the M signal.

3.5.1 Frame Alternation and Line Alternation

Figure 3-18 shows M signal timing. The M signal changes polarity (high or low) every frame in frame alternation and every line in line alternation. In line alternation, however, looking along a certain line shows that the M signal changes polarity every frame as well. That is, if the M signal is high in the first line of the first frame, it is low in the first line of the second frame.

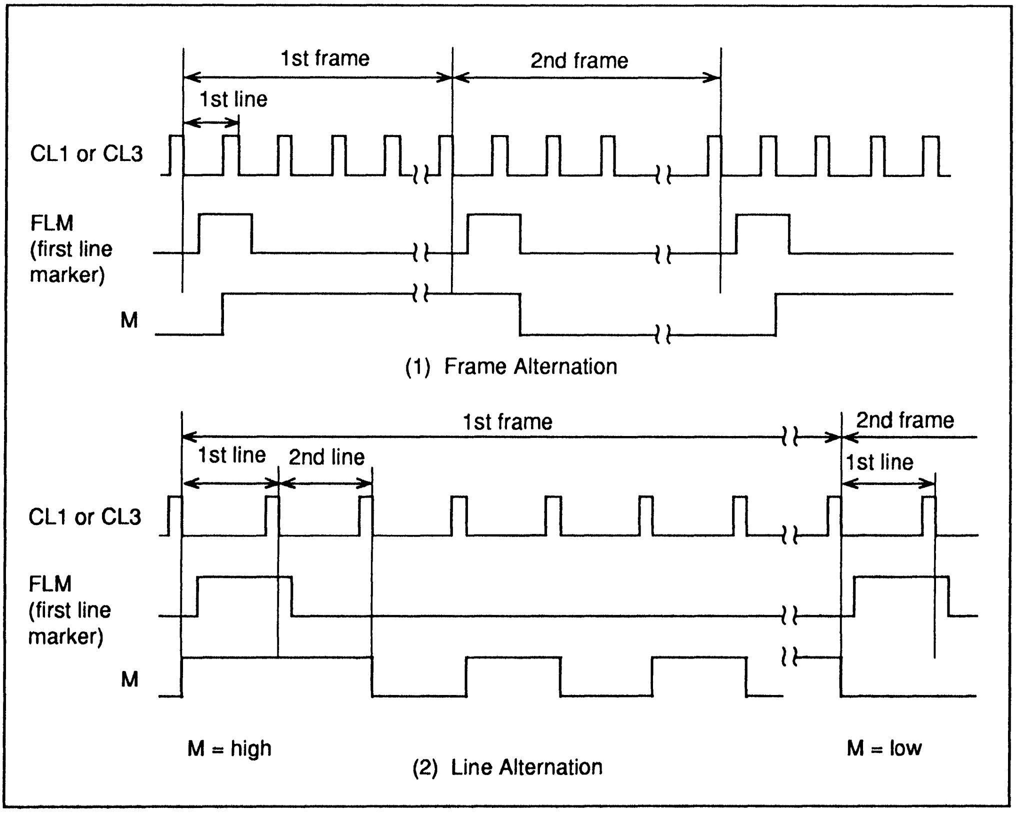


Figure 3-18 M Signal Timing

3.5.2 Alternation Type Selection

The alternation type of the M signal is fixed when the LVIC is controlled by the pin programming method. The M signal alternates every frame in display modes 1–8, and every line in display modes 9–16.

You can select the alternation type with the MC bit of control register 2 (R1) when the LVIC is controlled by the internal register programming method. Set 0 into the MC bit for frame alternation and set 1 for line alternation.

3.6 Buffer Memory Selection

An 8-, 32-, or 64-kbyte SRAM may be selected as buffer memory for the LVIC. The SRAM type is selected by the MS1 and MS0 pins or the MS1 and MS0 bits of control register 2 (R1). Table 3-8 shows memory selection settings and pin address assignments.

Refer to section 2.3.1, Memory Type and Memory Capacity Calculations, for details of how to calculate memory capacity.

Table 3-8 Memory Selection and Address Pins Assignment

Pins or Bits					Address
MS1	**MS0**	**Memory**	**Address Pins**	**Chip Select Pins**	**Assignment**
0	0	No memory (Through mode)	—	—	—
0	1	8-kbyte	MA0–MA12	$\overline{\text{MCS0}}$	\$0000–\$1FFF
				$\overline{\text{MSC1}}$	\$2000–\$3FFF
				MA13	\$4000–\$5FFF
				MA14	\$6000–\$7FFF
				MA15	\$8000–\$9FFF
1	0	32-kbyte	MA0–MA14	$\overline{\text{MCS0}}$	\$00000–\$07FFF
				$\overline{\text{MCS1}}$	\$08000–\$0FFFF
				MA15	\$10000–\$17FFF
1	1	64-kbyte	MA0–MA15	$\overline{\text{MCS0}}$	\$00000–\$0FFFF
				$\overline{\text{MCS1}}$	\$10000–\$1FFFF

3.7 Display On/Off Control

Display on means that the LVIC is outputting LCD data and display off means that the LVIC is not outputting LCD data. When the LVIC is controlled by the pin programming method, the turning on and off of an LCD cannot be controlled, and display is always fixed to on. This control can be provided by the DON bit of control register 2 (R1) when the LVIC is controlled by the internal register programming method. Display is on when DON = 1 and off when DON = 0.

3.8 Video Signal Latch Timing Selection

The latch timing of RGB signals is selected with the DOTE pin. Setting the pin low enables the LVIC to latch data at the rising edge of the dot clock (DOTCLK), while setting the pin high enables the LVIC to latch data at the falling edge of the DOTCLK signal.

Figure 3-19 shows the timing for latching video signals.

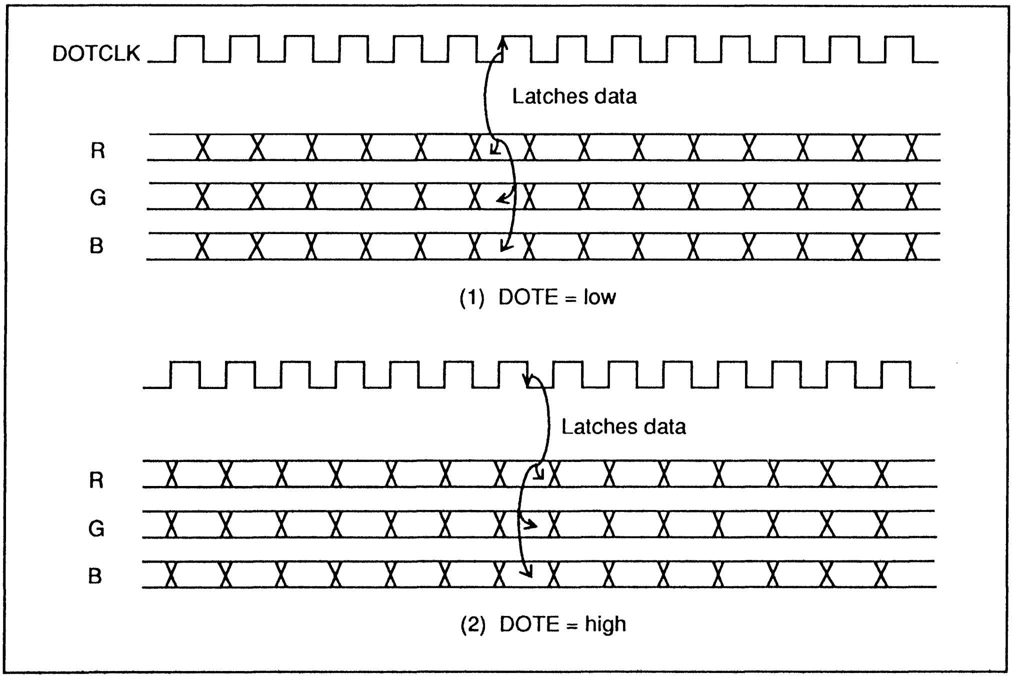


Figure 3-19 Data Latch Timing

3.9 Vertical Synchronization Polarity Selection

The vertical synchronization signal (VSYNC) may be either active-high or active-low; the LVIC supports both cases. Set the SPS pin high when the VSYNC signal is active-high, and set the SPS pin low when it is active-low.

Section 4 Double-Height Display

The LVIC provides double-height display which doubles the height of characters and pictures. This section explains the double-height display processing and how to use it.

4.1 Double-Height Display Process

In the TN-type LCD modes (display modes 1, 2, 4, and 6–8), the CL3 signal period is half that of the CL1 signal, as shown in figure 4-1. Consequently, if the CL3 signal is used instead of the CL1 signal as a line shift clock for the Y-drivers (scan drivers), two lines can be selected while the X-drivers (data output drivers) are outputting the same data, enabling the double-height display shown in figure 4-2. This double-height display function enables software intended for a CRT display of 640 × 200 dots to be displayed on an LCD of 640 × 400 dots.

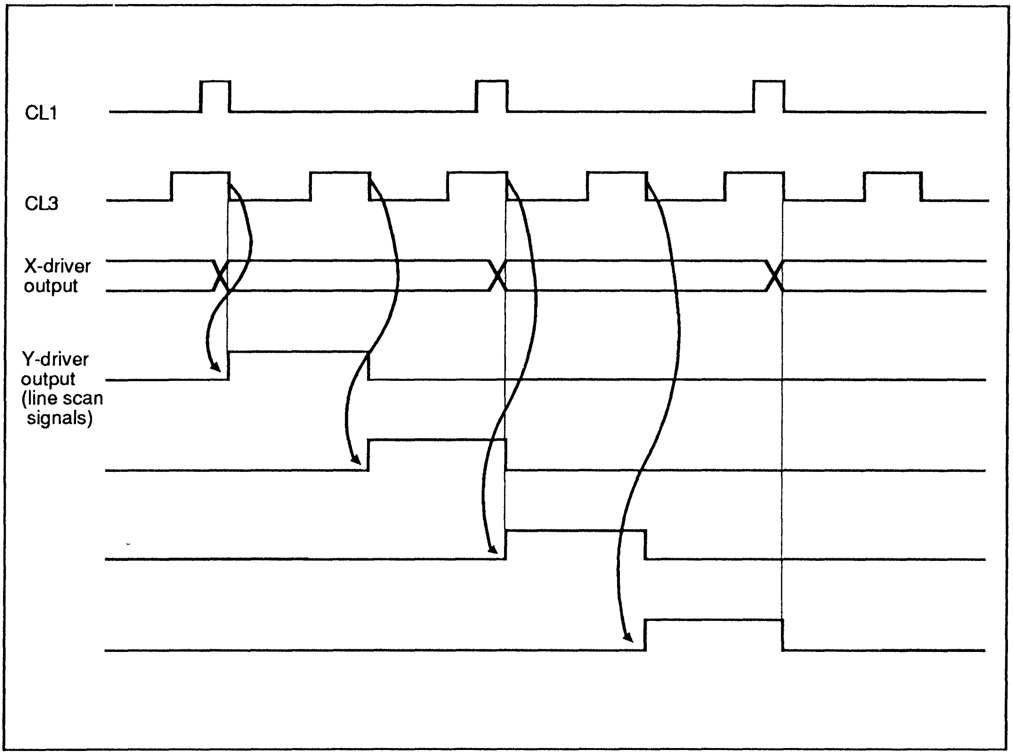


Figure 4-1 Relationship between CL1 and CL3 Signals in TN-Type LCD Modes

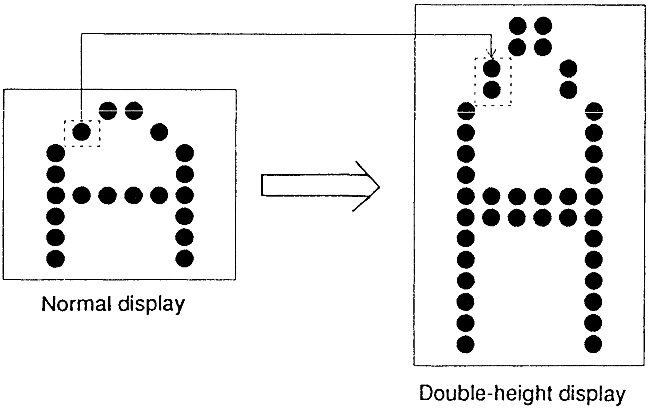


Figure 4-2 Double-Height Display Example

4.2 How To Use Double-Height Display

The double-height display function is available only in the TN-type LCD modes (display modes 1, 2, 4, and 6–8); it is not available in the TFT-type LCD modes (display modes 3, 5, and 9–16).

As shown in figure 4-3, connecting the CL3 signal instead of the CL1 signal as a line shift clock to the Y-drivers (scan drivers) enables double-height display. Note that this display requires the following procedure since the LVIC displays twice as many lines as the number of lines specified by the pins or the internal registers:

1. Halve the LCD dot clock (LDOTCK) frequency calculated from the number of vertical displayed lines of the LCD panel.
2. Specify half number of vertical displayed lines of the LCD panel as the number of vertical displayed lines. (For instance, if the number of vertical displayed lines of the LCD panel is 400, specify 200 by the YL2–YL0 pins or the vertical displayed lines register.)

The relation between the LDOTCK frequency and the CRT display dot clock (DOTCLK) frequency in double-height display is the same as that in normal display. That is, f_{LDOTCK}', which is the frequency of the LDOTCK signal obtained by step 1, should satisfy the condition expressed by equation 4-1, not that of equation 4-2.

$f_{LDOTCK}' < f_{DOTCLK} \times 15/16$ .... (4-1) (right)

$f_{LDOTCK}' < f_{DOTCLK} \times 1/2 \times 15/16$ .... (4-2) (wrong)

f_{DOTCLK} = DOTCLK signal frequency

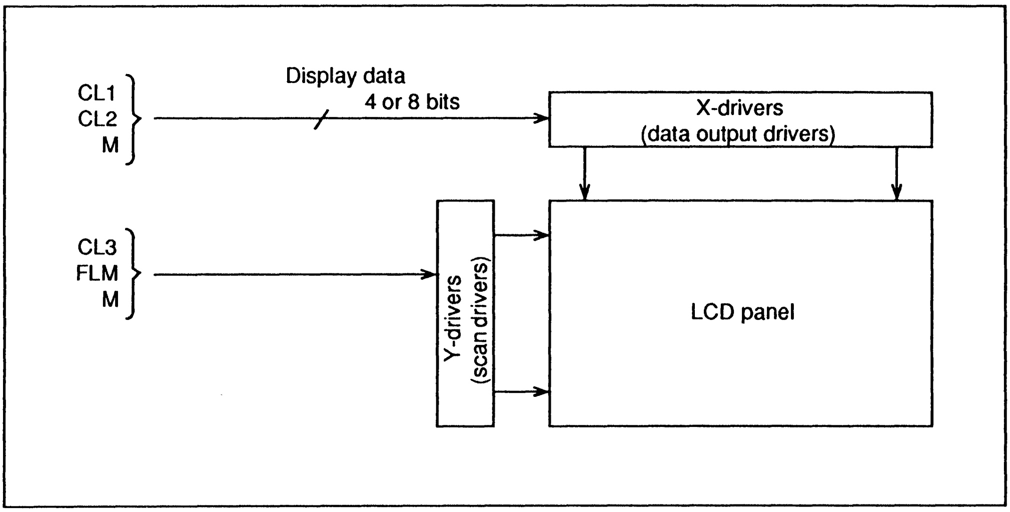


Figure 4-3 Connections for Double-Height Display

Section 5 Buffer Memory Clear Function

After it is reset, the LVIC writes 0s into all the addresses of buffer memory specified by the MS1 and MS0 pins or the MS1 and MS0 bits of control register 2 (R1) (table 5-1), regardless of what RGB data is transferred. The LCD data output pins are set to low level at this time. When this process is completed, the LVIC restarts writing CRT display data into buffer memory. This function is effective when the display timing signal (DISPTMG) is supplied externally and the CRT display screen size differs from the LCD screen size.

When the CRT display screen size is 640 × 350 dots and the LCD screen size is 640 × 400 dots, as shown in figure 5-1, the bottom 50 lines of data are usually undefined since SRAMs are used as buffer memory. However, the LVIC does not display undefined data since the bottom 50 lines of data are always 0 because of the action of the buffer memory clear function. This function is enabled by inputting the reset signal ($\overline{\text{RES}}$) when the display screen size is changed.

Table 5-1 MS1 and MS0 and Addresses after Memory Clear

MS1	MS0	Addresses
0	0	—
0	1	\$0000–\$9FFF
1	0	\$0000–\$17FFF
1	1	\$0000–\$1FFFF

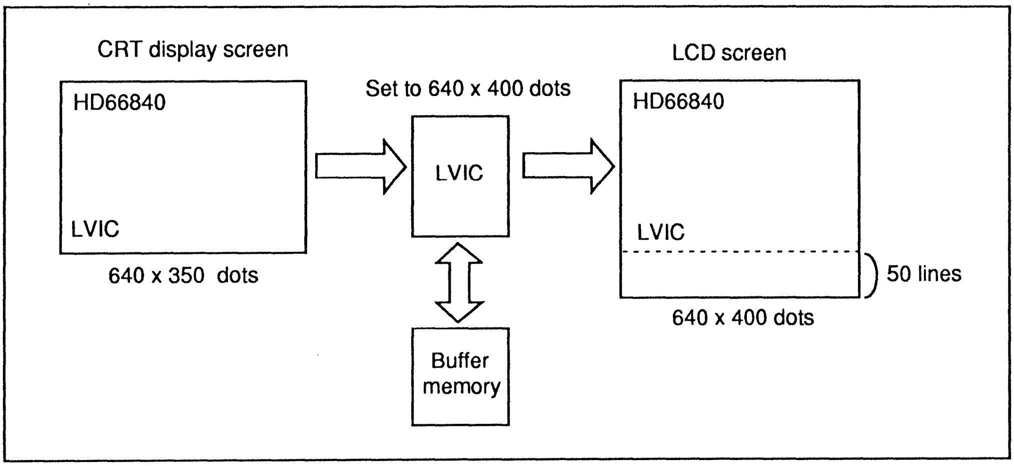


Figure 5-1 Buffer Memory Clear Function

Section 6 Display Mode Settings and Contents

The LVIC supports the 16 display modes listed in table 6-1. They are selectable by the DM3–DM0 pins. (Display mode can only be selected with these pins; internal registers cannot be used.)

Display modes are characterized by display color, type of data transfer, screen configuration, the configuration of LCD drivers about the LCD screen, type of stripes (color data arrangement) in the 8-color display modes, and LCD driving signal alternation. Note that either type of LCD driving signal alternation can be selected when the LVIC is controlled by the internal register programming method, while the type is fixed as shown in table 6-1 in the pin programming method. (Refer to section 3.5, LCD Driving Signal Alternation, for details.)

This section describes the display mode contents.

Table 6-1 Display Modes

Mode	Pins				Display	Data Transfer	Screen	LCD Driver Positions			
No.	DM3	DM2	DM1	DM0	Color	Type	Config.	X-Drivers	Y-Drivers	Stripes	Alternation
1	0	0	0	0	Monochrome	4 bits	Dual	One side	One side	—	Frame
2	0	0	0	1			Single				
3	0	0	1	0					Both sides		
4	0	0	1	1		8 bits			One side		
5	0	1	0	0					Both sides		
6	0	1	0	1	8-level	4 bits	Dual		One side		
7	0	1	1	0	gray scale		Single				
8	0	1	1	1		8 bits					
9	1	0	0	0	8-color	12 bits				Vertical	Line
10	1	0	0	1		(4 bits each			Both sides		
11	1	0	1	0		for R, G, and B)		Both sides	One side		
12	1	0	1	1					Both sides		
13	1	1	0	0				One side	One side	Horizontal	
14	1	1	0	1					Both sides		
15	1	1	1	0				Both sides	One side		
16	1	1	1	1					Both sides		

Note: Display modes 3, 5, and 9–16 are for TFT type LCDs.

6-1 Display Colors

There are three display color types: monochrome, 8-level gray scale, and 8-color.

6.1.1 Monochrome Display (Display Modes 1 to 5)

In the monochrome display mode, the LVIC displays two "colors", black (display on) and white (display off). As shown in figure 6-1, the LVIC writes an OR of the CRT RGB display data into the R-plane buffer memory, which means that G- and B-plane memories are not required in these modes.

If memory is connected to the G- or B-plane, the LVIC writes G or B data to that memory. However, the connection of memory to the G- or B-plane does not affect the R-plane memory contents or display.

Table 6-2 shows the correspondence between CRT display colors and LCD display.

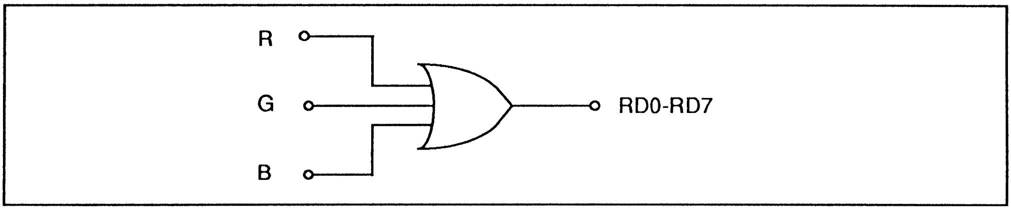


Figure 6-1 Monochrome Display Mechanism

Table 6-2 CRT and LCD Display Colors

CRT Display Data				LCD Display	
R	**G**	**B**	**CRT Display Color**	**On/Off**	
1	1	1	White	On	(Black)
1	1	0	Yellow	On	(Black)
0	1	1	Cyan	On	(Black)
0	1	0	Green	On	(Black)
1	0	1	Magenta	On	(Black)
1	0	0	Red	On	(Black)
0	0	1	Blue	On	(Black)
0	0	0	Black	Off	(White)

6.1.2 8-Level Gray Scale Display (Display Modes 6 to 8)

In the 8-level gray scale display modes, the LVIC thins out LCD data in frame units according to the CRT display color. For instance, if the CRT display color is green, data for a certain pixel (cell) of the LCD will appear in only two frames (display on) out of one frame (display off in the third frame). In this manner, the LVIC changes the voltage ratio applied to a pixel according to the CRT display color to realize an 8-level gray scale display. Table 6-3 shows the correspondence between the CRT display color, the effective voltage ratio, and the resulting LCD gray scale.

Table 6-3 Correspondence between CRT Display Color, Effective Voltage Ratio, and LCD Gray Scale

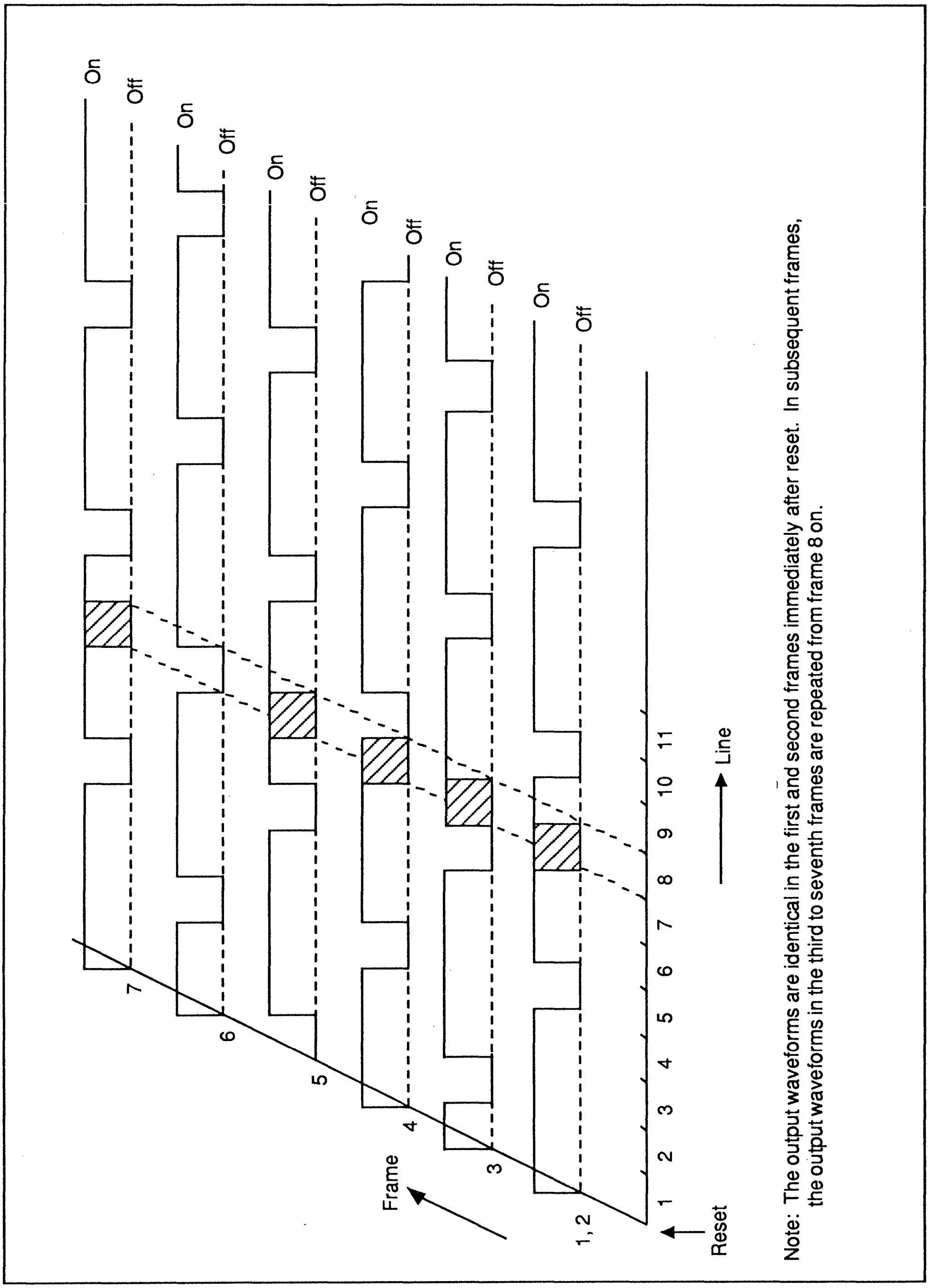
CRT Display Color	Effective Voltage Ratio	LCD Gray Scale
White	Vs	
Yellow	7/8 Vs + 1/8 Vns	
Cyan	4/5 Vs + 1/5 Vns	
Green	2/3 Vs + 1/3 Vns	
Magenta	1/2 Vs + 1/2 Vns	
Red	1/3 Vs + 2/3 Vns	
Blue	1/5 Vs + 4/5 Vns	
Black	Vns	

Vs: Display-on level (selected level)

Vns: Display-off level (non-selected level)

In the 8-level gray scale display modes, the LVIC shifts the phase of display data so that the lines in which data is being thinned out is constantly changing frame-by-frame. This is to reduce flickering of the screen in these modes. For instance, if the LVIC is to display cyan on the whole screen, data will not appear on every (5n)th line from the top of the LCD panel (n = 0, 1, 2, ...) in the frame just after reset and in the following frame. In the next frame, data will not appear on every (5n + 2)th line (n = 0, 1, 2, ...). See figure 6-2 for the LVIC operations in the subsequent frames. In this case, the LVIC thins out data every five lines in each frame. For a certain line, data will not appear in one frame of five frames (the area marked by dotted lines in figure 6-2).

The other CRT display colors are handled in a similar way.

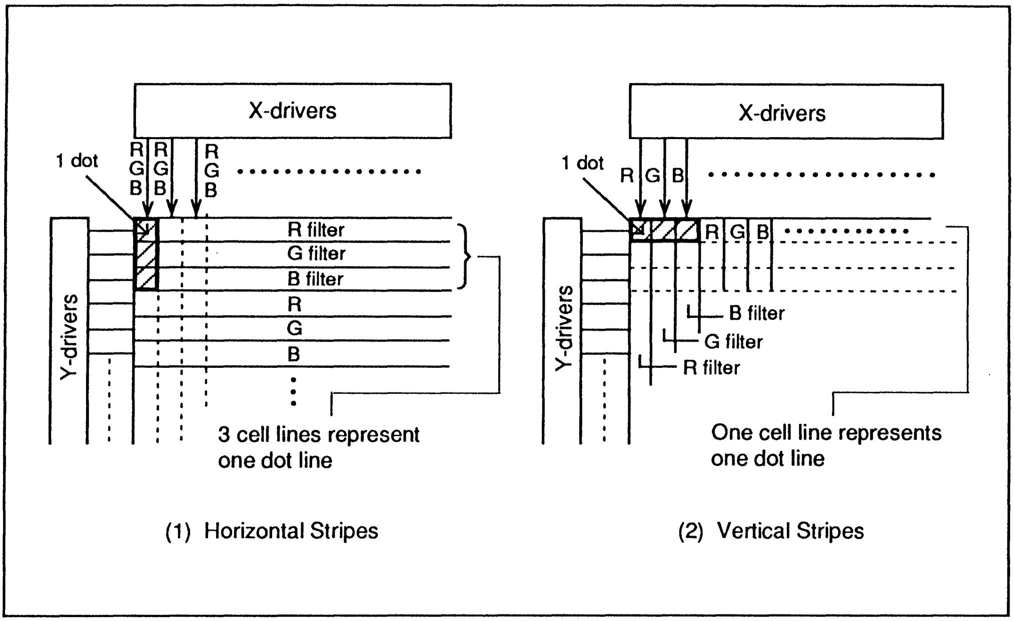


Note: The output waveforms are identical in the first and second frames immediately after reset. In subsequent frames, the output waveforms in the third to seventh frames are repeated from frame 8 on.

Figure 6-2 Phase Shift of Display Data (When the CRT Display Color is Cyan)

6.1.3 8-Color Display (Display Modes 9 to 16)

In the 8-color display modes, the LVIC displays eight colors using red (R), green (G), and blue (B) filters placed on liquid-crystal cells. The eight colors are the same as those provided by the CRT display. For example, yellow and blue on the CRT display screen are also displayed as yellow and blue on the LCD screen. As shown in figure 6-3, the 8-color display has two stripe modes; a horizontal stripe mode and a vertical stripe mode. The LVIC arranges RGB data horizontally with horizontal filters in the former mode, and vertically with vertical filters in the latter mode. Three cells represent one dot in both modes.



(1) Horizontal Stripes

(2) Vertical Stripes

Figure 6-3 Stripes in 8-Color Display Modes

6.2 LCD System Configuration

When an LCD system is configured, a screen configuration and a configuration of LCD drivers around the LCD screen must be selected.

6.2.1 Screen Configuration

There are two types of screen configuration: single screen and dual screen. A single screen is composed of one panel and a dual screen is composed of an upper panel and a lower panel.

A cheaper, more compact LCD system is configured with a single screen than with a dual screen. On the other hand, a dual screen exhibits a better display quality and can use lower voltage drive type LCD drivers than a single screen.

6.2.2 LCD Driver Positioning

LCD drivers can be classified into column drivers, which output display data, and row drivers, which scan lines of an LCD panel. Column drivers are set horizontally with respect to the LCD panel, while row drivers are set vertically with respect to the LCD panel. Since column drivers and row drivers are set parallel to the X-axis and Y-axis, respectively, they are called X-drivers and Y-drivers (figure 6-4).

The LVIC's operations depend on whether each group of X- and Y-drivers is set on one side of the LCD panel or on both sides.

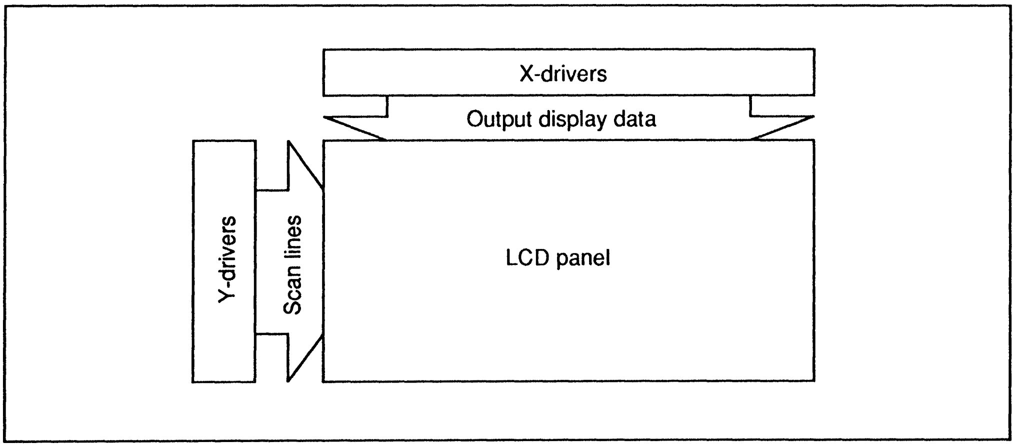


Figure 6-4 X-Drivers and Y-Drivers

X-Driver Positioning: Figure 6-5 shows the difference between configurations with X-drivers on one side and X-drivers on both sides. In the display modes for X-drivers on one side, the X-drivers output display data corresponding to a line from one direction, while in the display modes for X-drivers on both sides, the upper X-drivers and the lower X-drivers alternate in outputting display data. Consequently, the spacing between the LCD data output wires in these modes is wider than that in the display modes for X-drivers on one side.

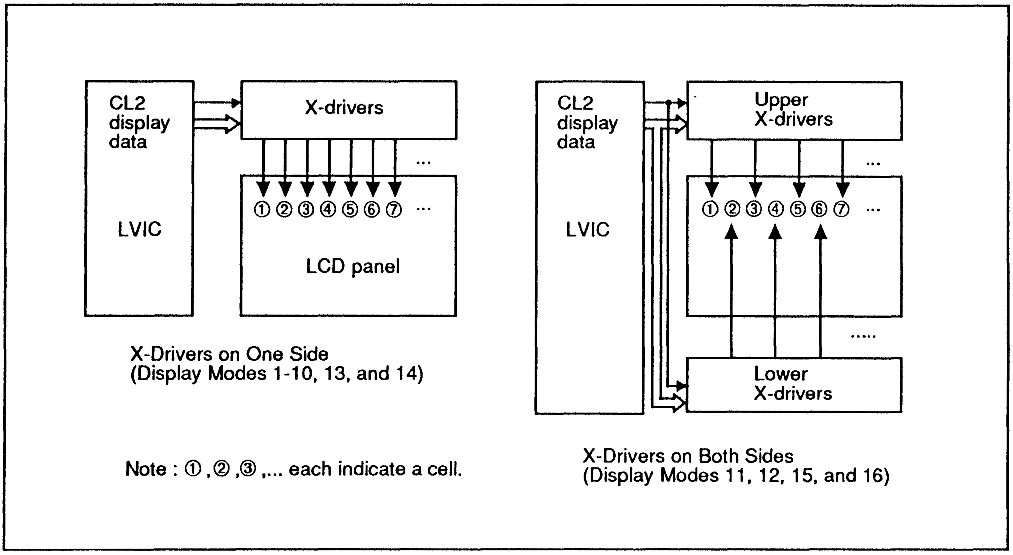


Figure 6-5 X-Drivers on One Side and on Both Sides

Figure 6-6 shows the phase relationship between the CL2 signal and display data. In the display modes for X-drivers on one side, the X-drivers latch the data sent from the LVIC at the falling edge of the CL2 signal. In the display modes for X-drivers on both sides, the upper X-drivers latch the upper data sent from the LVIC at the rising edge of the CL2 signal, and lower X-drivers latch the lower data sentfrom the LVIC at the falling edge of CL2 signal.

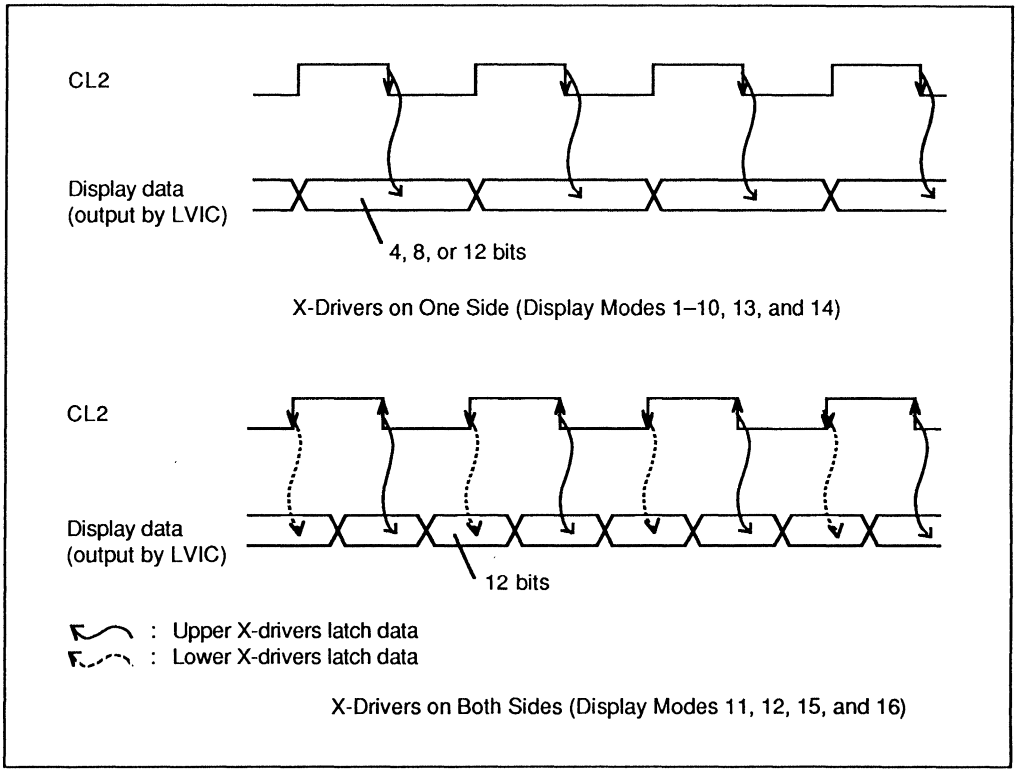
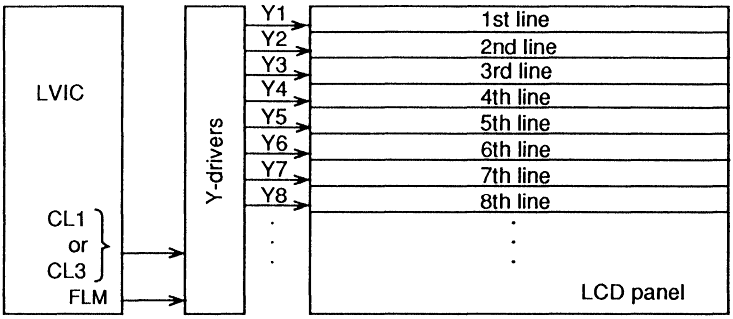
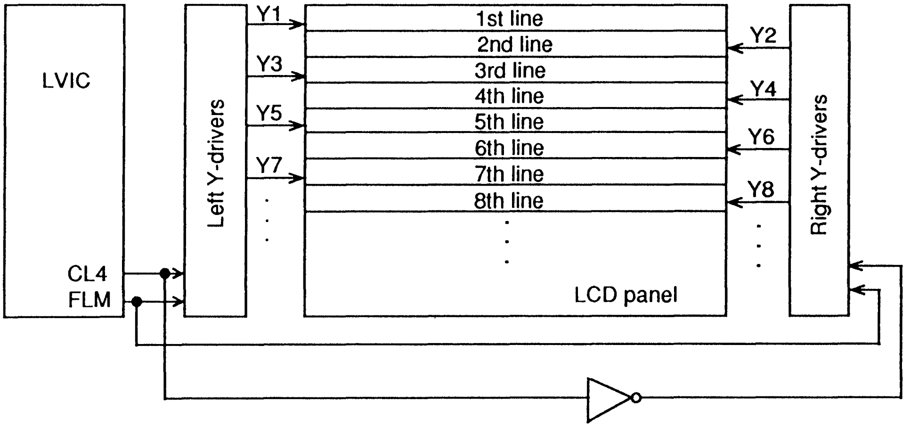

CL2
Display data
(output by LVIC)
4, 8, or 12 bits
X-Drivers on One Side (Display Modes 1–10, 13, and 14)
CL2
Display data
(output by LVIC)
12 bits
: Upper X-drivers latch data
: Lower X-drivers latch data
X-Drivers on Both Sides (Display Modes 11, 12, 15, and 16)

Figure 6-6 Data Latch Timing of X-Drivers

Y-Driver Positioning: Figure 6-7 shows the difference between configurations with Y-drivers on one side and Y-drivers on both sides. In the display modes for Y-drivers on one side, the Y-drivers output line scan signals from one direction, while in the display modes for Y-drivers on both sides, the left Y-drivers and the right Y-drivers alternate in outputting line scan signals. Consequently, the spacing between the line scan signal output wires in these modes is wider than that in the display modes for Y-drivers on one side.



Y-Drivers on One Side (Display Modes 1, 2, 4, 6, 7–9, 11, 13, and 15)



Y-Drivers on Both Sides (Display Modes 3, 5, 10, 12, 14, and 16)

Note: Each line indicates a cell line, not a dot line.

Figure 6-7 Y-Drivers on One Side and on Both Sides

Figure 6-8 shows the phase relationships between the CL1 or CL3 signal, the FLM signal, line scan signals, and display data in the display modes for Y-drivers on one side. In the TN-type LCD modes (normal display), the Y-drivers shift line scan signals at the falling edge of the CL1 signal, while in the TFT-type LCD modes, the Y-drivers shift line scan signals at the rising edge of the CL3 signal.

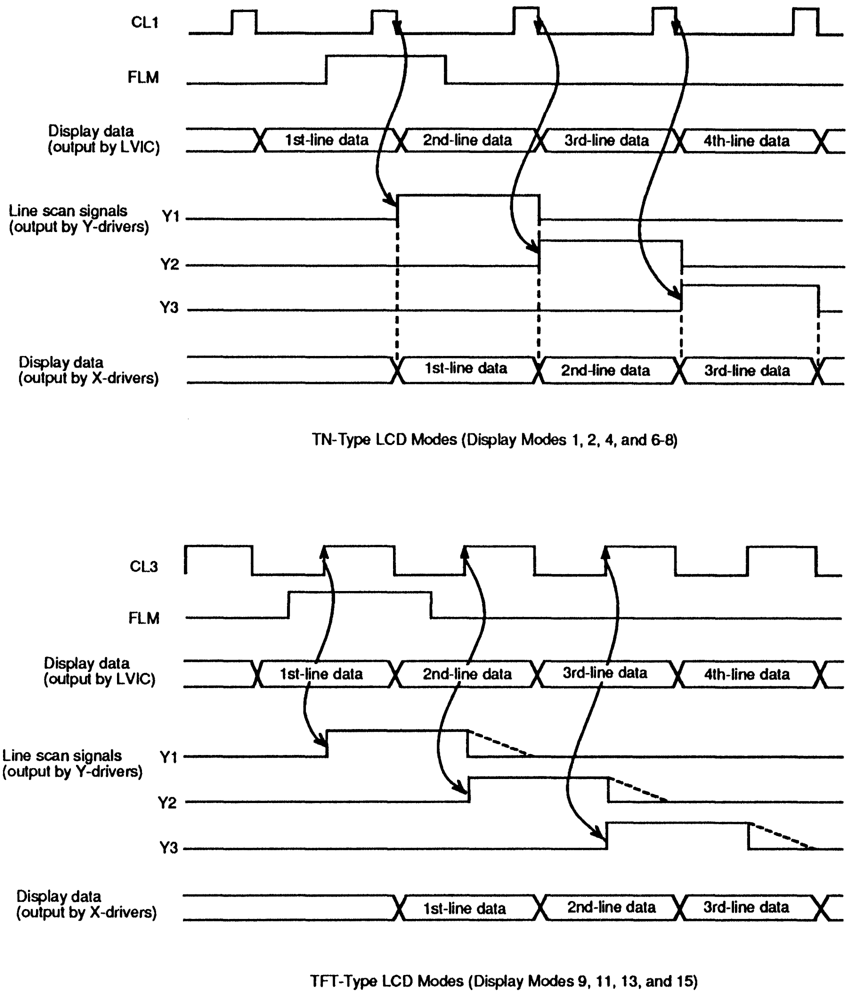

CL1
FLM
Display data (output by LVIC)
1st-line data
2nd-line data
3rd-line data
4th-line data
Line scan signals (output by Y-drivers)
Y1
Y2
Y3
Display data (output by X-drivers)
1st-line data
2nd-line data
3rd-line data
TN-Type LCD Modes (Display Modes 1, 2, 4, and 6-8)
CL3
FLM
Display data (output by LVIC)
1st-line data
2nd-line data
3rd-line data
4th-line data
Line scan signals (output by Y-drivers)
Y1
Y2
Y3
Display data (output by X-drivers)
1st-line data
2nd-line data
3rd-line data
TFT-Type LCD Modes (Display Modes 9, 11, 13, and 15)

Figure 6-8 Timing of Line Scan Signal Shift in Display Modes for Y-Drivers on One Side (Display Modes 1, 2, 4, 6–8, 9, 11, 13, and 15)

Figure 6-9 shows the phase relationships between the CL4 signal, the FLM signal, line scan signals, and display data in the display modes for Y-drivers on both sides. The left Y-drivers shift line scan signals at the falling edge of the CL4 signal, and the right Y-drivers shift them at its rising edge. Each line scan signal must output a high-level pulse for a two-line period.

For the relationships between the CL1, CL3, and CL4 signals, refer to figures 7-3 to 7-5 in section 7.2.1, CL3 and CL4 Signal Output in Pin Programming Method.

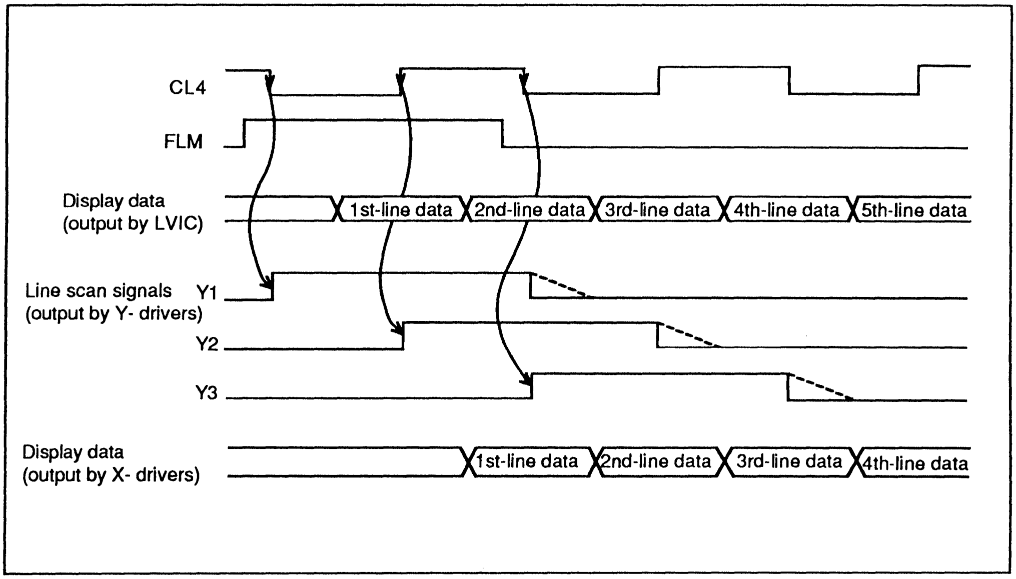


Figure 6-9 Timing of Line Scan Signal Shift in Display Modes for Y-Drivers on Both Sides (Display Modes 3, 5, 10, 12, 14, and 16)

6.3 LCD Data Output and Display Screen

The LCD data output type depends on the type of data transfer, screen configuration, and X-driver positioning. It also depends on the stripe mode in the 8-color display modes. The LVIC supports the following LCD data output types:

- 4-bit transfer, dual screen, X-drivers on one side
- 4-bit transfer, single screen, X-drivers on one side
- 8-bit transfer, single screen, X-drivers on one side or on both sides
- 4-bit transfer for each of R, G, and B, single screen, vertical stripes, X-drivers on one side
- 4-bit transfer for each of R, G, and B, single screen, vertical stripes, X-drivers on both sides
- 4-bit transfer for each of R, G, and B, single screen, horizontal stripes, X-drivers on one side
- 4-bit transfer for each of R, G, and B, single screen, horizontal stripes, X-drivers on both sides

LCD data output type does not depend on Y-driver positioning.

The relationships between LCD data output types 1 to 7 and the corresponding display screens are described below.

Table 6-4 lists several Hitachi LCD modules (LCM) and the corresponding display modes.

Table 6-4 Hitachi LCMs and Display Modes

LCM	Screen Size (Dots)	Data Transfer Type/ Screen Configuration	Display Mode Nos.	Reference Figures System	Reference Figures Display
LM225S LM250X	640 × 200	4-bit/single	2, 3, 7	6-12	6-13
LM236SB LM585S	640 × 200	4-bit/dual	1, 6	6-10	6-11
LM252X	640 × 400	4-bit/dual	1, 6	6-10	6-11

6.3.1 4-Bit Transfer, Dual Screen, X-Drivers on One Side (Display Modes 1 and 6)

Figure 6-10 shows the display system configuration for display modes 1 and 6. In these modes, the LCD panel is divided into upper and lower panels which are driven by upper panel X-drivers and lower panel X-drivers. Accordingly, the LVIC outputs upper panel data in 4-bit units to the upper panel X-drivers through the LU0–LU3 pins, and outputs lower panel data in 4-bit units to the lower panel X-drivers through the LD0–LD3 pins.

Figure 6-11 shows the relationship between the display data output by the LVIC and the display screen in display modes 1 and 6. The upper and lower panel X-drivers both latch display data at the falling edge of the CL2 signal. Having latched data for one line, the upper and lower X-drivers output it all at once to the LCD's upper and lower panels at the falling edge of the CL1 signal.

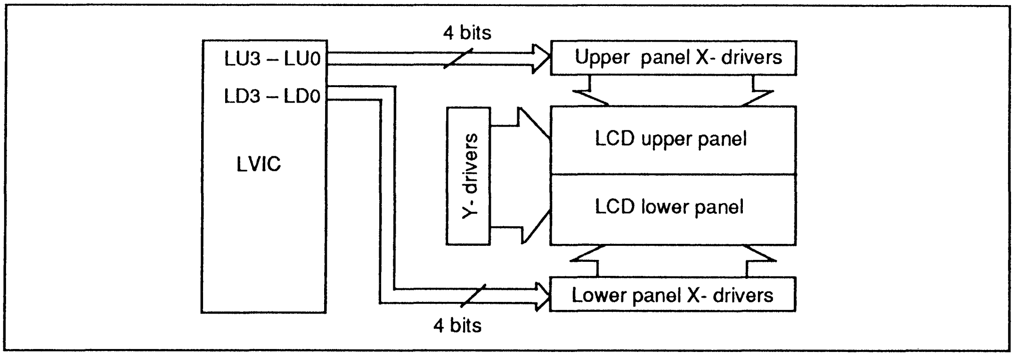


Figure 6-10 Display System Configuration for Display Modes 1 and 6

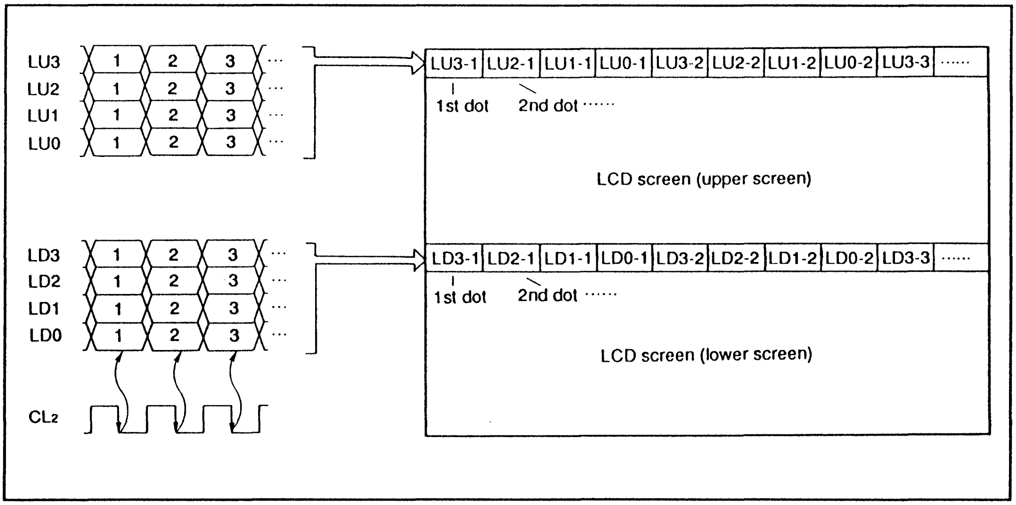
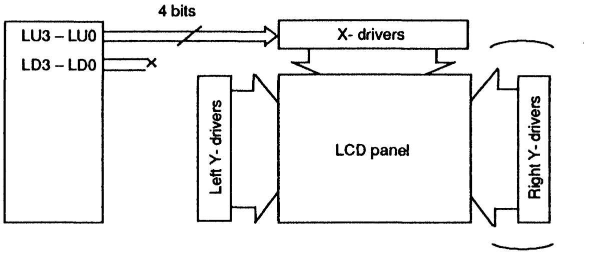


Figure 6-11 Data Output and Display Screen in Display Modes 1 and 6 (4-Bit Transfer, Dual Screen, X-Drivers on One Side)

6.3.2 4-Bit Transfer, Single Screen, X-Drivers on One Side (Display Modes 2, 3, and 7)

Figure 6-12 shows the display system configuration for display modes 2, 3, and 7. Although the Y-drivers are set on one side of the LCD panel in display modes 2 and 7, but on both sides in display mode 3, the LVIC outputs display data to the X-drivers in the same way in all these modes. The LVIC outputs display data in 4-bit units to the X-drivers through the LU0–LU3 pins.

Figure 6-13 shows the relationship between the display data output by the LVIC and the display screen in display modes 2, 3, and 7. The display screen does not depend on how the Y-drivers are positioned. The X-drivers latch display data at the falling edge of the CL2 signal. Having latched the data for one line, the X-drivers output it all at once to the LCD panel at the falling edge of the CL1 signal.



Note: Y- drivers are positioned on one side in display modes 2 and 7 and on both sides in display mode 3.

Figure 6-12 Display System Configuration for Display Modes 2, 3, and 7

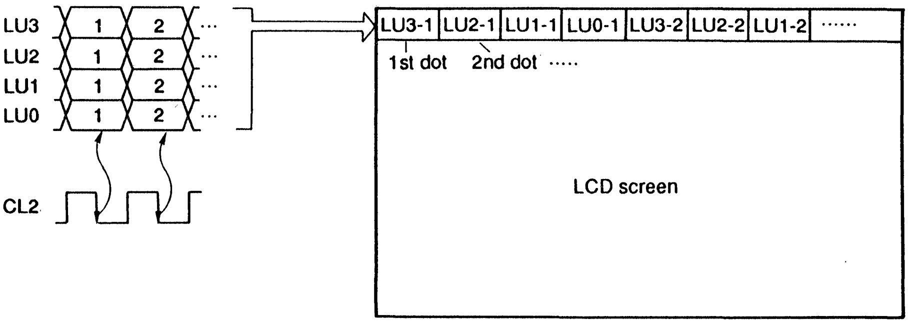


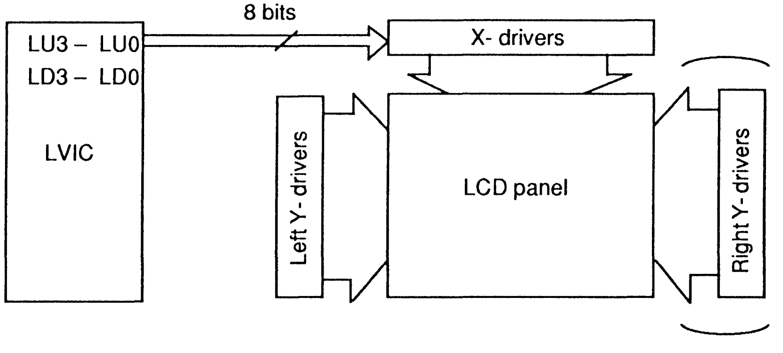
Figure 6-13 Data Output and Display Screen in Display Modes 2, 3, and 7 (4-Bit Transfer, Single Screen, X-Drivers on One Side)

6.3.3 8-Bit Transfer, Single Screen, X-Drivers on One Side (Display Modes 4, 5, and 8)

Figure 6-14 shows the display system configuration for display modes 4, 5, and 8. Although the Y-drivers are set on one side of the LCD panel in display modes 4 and 8, but on both sides in display mode 5, the LVIC outputs display data to the X-drivers in the same way in all these modes. The LVIC outputs display data in 8-bit units to X-drivers through the LU0–LU3 and LD0–LD3 pins.

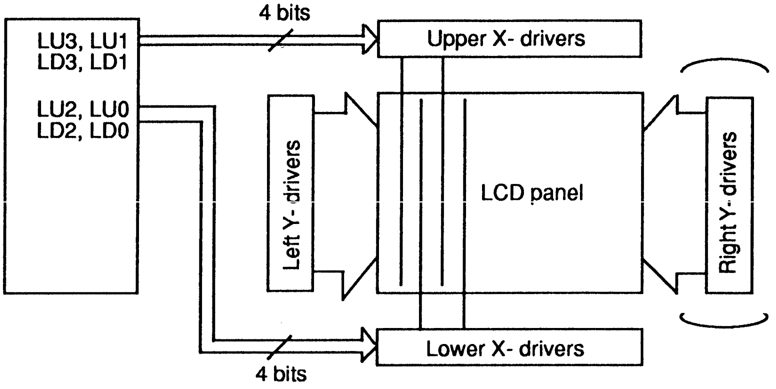
A display system can also be configured for these modes by setting the X-drivers of a 4-bit data interface instead of an 8-bit data interface on both sides of the LCD panel. In this configuration, the LVIC outputs display data in 4-bit units to the upper X-drivers through the LU3, LU1, LD3, LD1 pins, and to the lower X-drivers through the LU2, LU0, LD2, LD0 pins. In this case, the upper X-drivers are connected to odd-numbered dot cells of the LCD panel and the lower X-drivers are connected to even-numbered dot cells (figure 6-15).

Figure 6-16 shows the relationship between the display data output by the LVIC and the display screen in display modes 4, 5, and 8. The display screen does not depend on how the X- and Y-drivers are positioned. The X-drivers latch display data at the falling edge of the CL2 signal. Having latched the data for one line, the X-drivers output it all at once to the LCD panel at the falling edge of the CL1 signal.



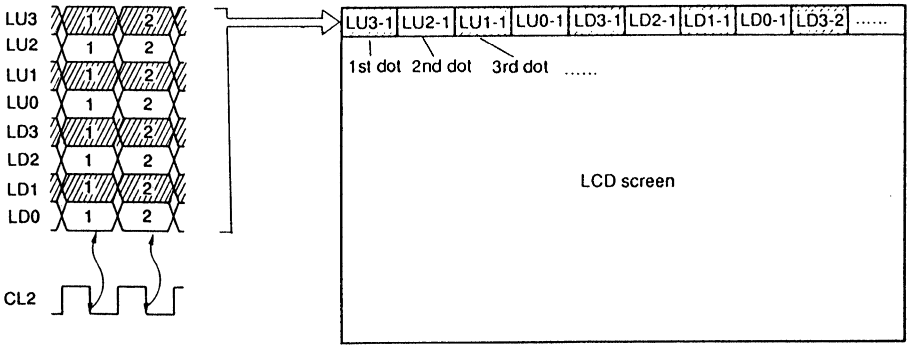
Note: Y- drivers are positioned on one side in display modes 4 and 8 and on both sides in display mode 5.

Figure 6-14 Display System Configuration 1 for Display Modes 4, 5 and 8 (X-Drivers on One Side)



Note: 1. The upper X-drivers output odd-numbered dot data and the lower X-drivers output even-numbered dot data.
2. Y- drivers are set on one side in display modes 4 and 8 and on both sides in display mode 5.

Figure 6-15 Display System Configuration 2 for Display Modes 4, 5, and 8 (X-Drivers on Both Sides)



Note : The upper X-drivers output the data in the shaded area when X-drivers are set on both sides.

Figure 6-16 Data Output and Display Screen in Display Modes 4, 5, and 8 (8-Bit Transfer, Single Screen, X-Drivers on One Side or Both Sides)

6.3.4 4-Bit Transfer for Each of R, G, and B, Single Screen, Vertical Stripes, X-Drivers on One Side (Display Modes 9 and 10)

Figure 6-17 shows the display system configuration for display modes 9 and 10. Although Y-drivers are set on one side of the LCD panel in display mode 9, but on both sides in display mode 10, the LVIC outputs display data to the X-drivers in the same way in both of these modes. The X-drivers are divided into three output groups in these modes: R data only, G data only, and B data only. The LVIC outputs R data, G data, and B data in 4-bit units to the corresponding X-drivers through the R3–R0, G3–G0, and B3–B0 pins.

Figure 6-18 shows the relationship between the display data output by the LVIC and the display screen in display modes 9 and 10. The display screen does not depend on how the Y-drivers are positioned. The LVIC reads data from buffer memory in the order shown in the figure, and outputs it to the X-drivers. The X-drivers latch display data at the falling edge of the CL2 signal. Having latched the data for one line, the X-drivers output it all at once to the LCD panel at the falling edge of the CL1 signal.

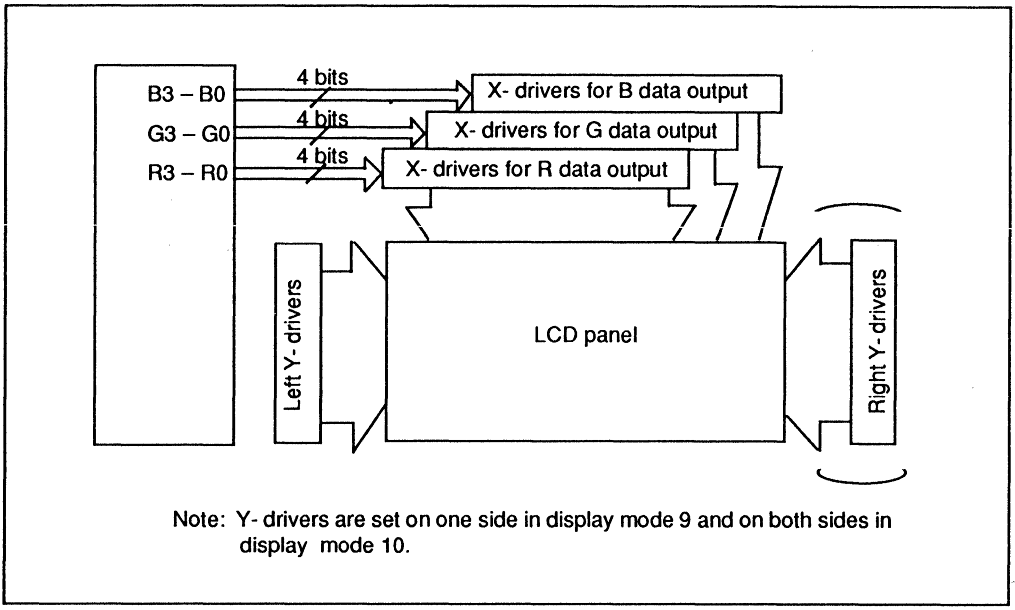

B3 – B0
G3 – G0
R3 – R0
4 bits
4 bits
4 bits
X- drivers for B data output
X- drivers for G data output
X- drivers for R data output
Left Y- drivers
LCD panel
Right Y- drivers
Note: Y- drivers are set on one side in display mode 9 and on both sides in display mode 10.

Figure 6-17 Display System Configuration for Display Modes 9 and 10

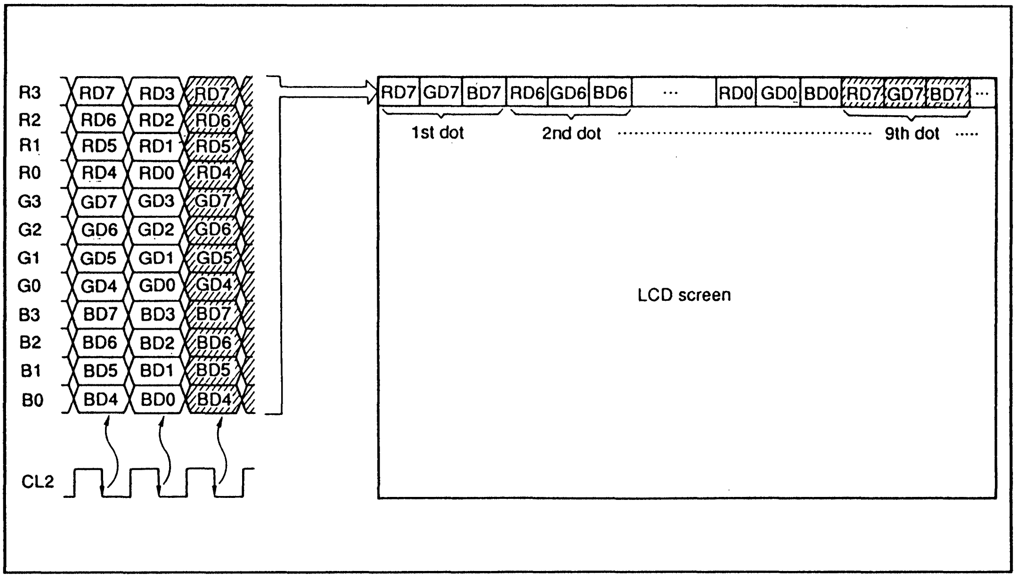
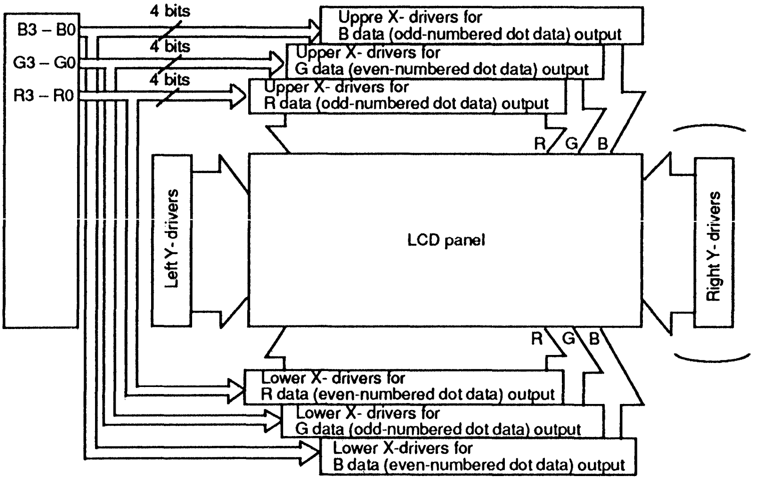


Figure 6-18 Data Output and Display Screen in Display Modes 9 and 10 (4-Bit Transfer for Each of R, G, and B, Single Screen, Vertical Stripes, X-Drivers on One Side)

6.3.5 4-Bit Transfer for Each of R, G, and B, Single Screen, Vertical Stripes, X-Drivers on Both Sides (Display Modes 11 and 12)

Figure 6-19 shows the display system configuration for display modes 11 and 12. Although Y-drivers are set on one side of the LCD panel in display mode 11, but on both sides in display mode 12, the LVIC outputs display data to the X-drivers in the same way in both of these modes. The upper and lower X-drivers are divided into three output groups in these modes: R data only, G data only, and B data only. The LVIC outputs R data, G data, and B data in 4-bit units to the corresponding X-drivers through the R3–R0, G3–G0, and B3–B0 pins. In this case, the upper X-drivers for outputting R data only and B data only and the lower X-drivers for outputting G data only are connected to odd-numbered dot cells of the LCD panel, while the lower X-drivers for outputting R data only and B data only and the upper X-drivers for outputting G data only are connected to even-numbered dot cells.

Figure 6-20 shows the relationship between the display data output by the LVIC and the display screen in display modes 11 and 12. The display screen does not depend on how the Y-drivers are positioned. The LVIC reads data from buffer memory in the order shown in the figure, and outputs it to the upper and lower X-drivers. The upper X-drivers latch display data at the rising edge of the CL2 signal, and the lower X-drivers latch it at its falling edge. Having latched the data for one line, the upper and lower X-drivers output it all at once to the LCD panel at the falling edge of the CL1 signal.


B3 – B0
G3 – G0
R3 – R0
4 bits
4 bits
4 bits
Uppre X- drivers for B data (odd-numbered dot data) output
Upper X- drivers for G data (even-numbered dot data) output
Upper X- drivers for R data (odd-numbered dot data) output
R
G
B
Left Y- drivers
LCD panel
Right Y- drivers
R
G
B
Lower X- drivers for R data (even-numbered dot data) output
Lower X- drivers for G data (odd-numbered dot data) output
Lower X-drivers for B data (even-numbered dot data) output

Note: Y- drivers are positioned on one side in display mode 11 and on both sides in display mode 12.

Figure 6-19 Display System Configuration for Display Modes 11 and 12

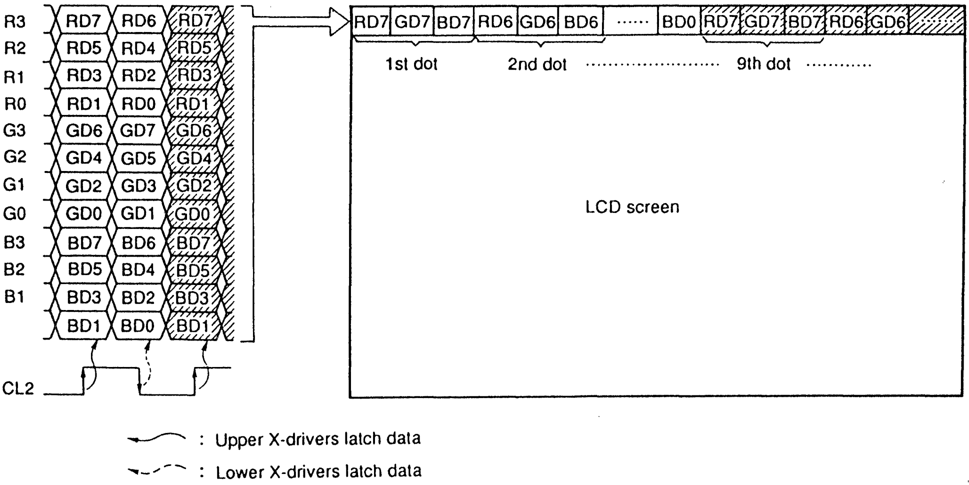
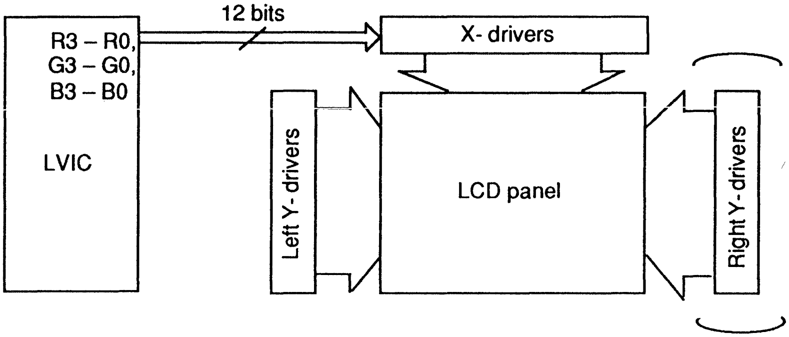


Figure 6-20 Data Output and Display Screen in Display Modes 11 and 12 (4-Bit Transfer for Each of R, G, and B, Single Screen, Vertical Stripes, X-Drivers on Both Sides)

6.3.6 4-Bit Transfer for Each of R, G, and B, Single Screen, Horizontal Stripes, X-Drivers on One Side (Display Modes 13 and 14)

Figure 6-21 shows the display system configuration for display modes 13 and 14. Although Y-drivers are set on one side of the LCD panel in display mode 13, but on both sides in display mode 14, the LVIC outputs display data to the X-drivers in the same way in both of these modes. The LVIC outputs the RGB data in 4-bit units to the X-drivers through the R0–R3, G0–G3, and B0–B3 pins.

Figure 6-22 shows the relationship between the display data output by the LVIC and the display screen in display modes 13 and 14. The display screen does not depend on how the Y-drivers are positioned. The LVIC reads data from buffer memory in the order shown in the figure, and outputs it to the X-drivers. The X-drivers latch display data at the falling edge of the CL2 signal. Having latched the data for one dot line, the X-drivers output the R data, G data, and B data in that order to the LCD panel at each falling edge of the CL3 signal.



Note: Y- drivers are positioned on one side in display mode 13 and on both sides in display mode 14.

Figure 6-21 Display System Configuration for Display Modes 13 and 14

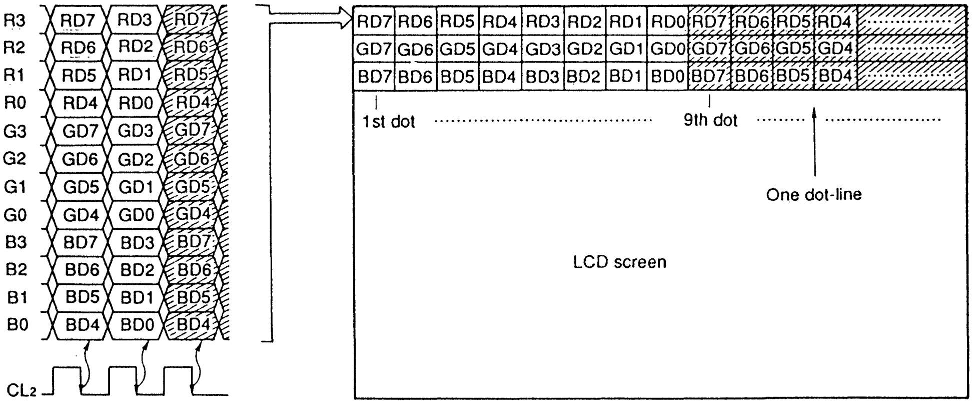
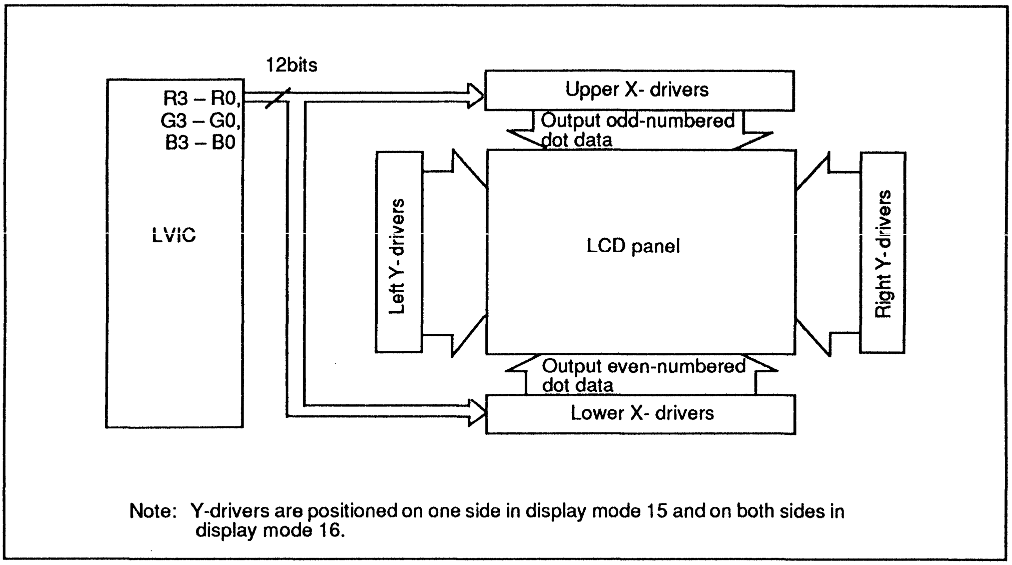


Figure 6-22 Data Output and Display Screen in Display Modes 13 and 14 (4-Bit Transfer for Each of R, G, and B, Single Screen, Horizontal Stripes, X-Drivers on One side)

6.3.7 4-Bit Transfer for Each of R, G, and B, Single Screen, Horizontal Stripes, X-Drivers on Both Sides (Display Modes 15 and 16)

Figure 6-23 shows the display system configuration for display modes 15 and 16. Although Y-drivers are set on one side of the LCD panel in display mode 15, but on both sides in display mode 16, the LVIC outputs display data to the X-drivers in the same way in both of these modes. The LVIC outputs R, G, and B data in 4-bit units to the upper and lower X-drivers through the R3–R0, G3–G0, and B3–B0 pins. In this case, the upper X-drivers are connected to the odd-numbered dot cells of the LCD panel, and the lower X-drivers are connected to the even-numbered dot cells.

Figure 6-24 shows the relationship between the display data output by the LVIC and the display screen in display modes 15 and 16. The display screen does not depend on how the Y-drivers are positioned. The LVIC reads data from buffer memory in the order shown in the figure, and outputs it to the upper and lower X-drivers. The upper X-drivers latch display data at the rising edge of the CL2 signal, and the lower X-drivers latch it at its falling edge. Having latched the data for one dot line, the upper and lower X-drivers output the R data, G data, and B data in that order to the LCD panel at each falling edge of the CL3 signal.



Note: Y-drivers are positioned on one side in display mode 15 and on both sides in display mode 16.

Figure 6-23 Display System Configuration for Display Modes 15 and 16

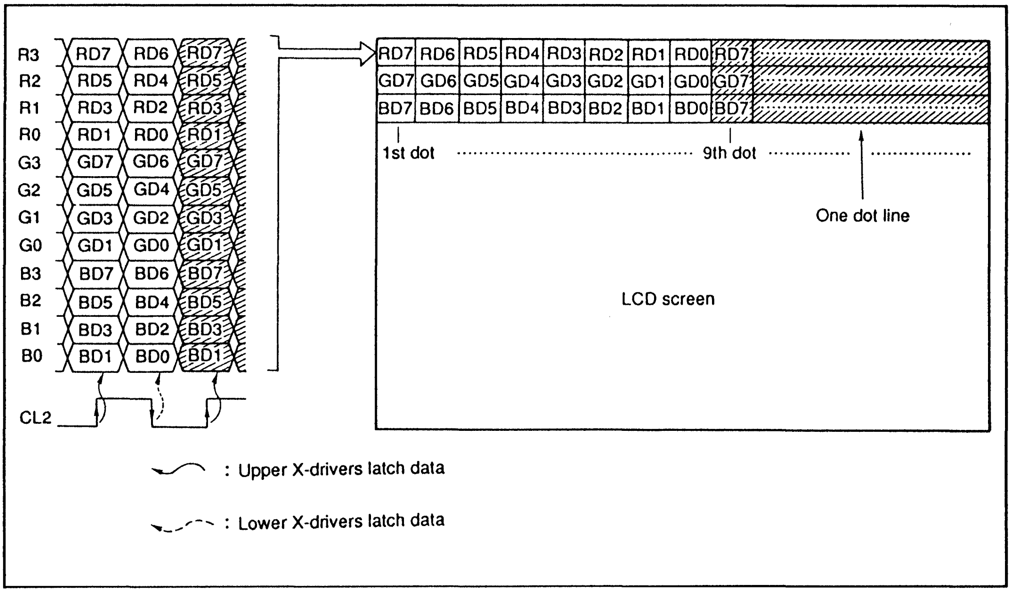


Figure 6-24 Data Output and Display Screen in Display Modes 15 and 16 (4-Bit Transfer for Each of R, G, and B, Single Screen, Horizontal Stripes, X-Drivers on Both Sides)

Section 7 TFT-Type LCD Control

The LVIC can control TFT (thin-film transistor)-type LCDs in addition to the current TN (twisted nematic)-type LCDs. Each pixel (cell) of a TFT-type LCD employs a transistor, which enables highly-improved contrast and high-quality display. Using a TFT-type LCD enables color display.

The LVIC has ten display modes for TFT-type LCDs: display modes 3, 5, and 9 to 16. Display modes 3 and 5 are monochrome display modes; the others are 8-color display modes. The 8-color display modes are either vertical stripe modes (display modes 9 to 12) or horizontal stripe modes (display modes 13 to 16). For details of stripe modes, refer to section 6.1.3, 8-Color Display.

The control of TFT-type LCDs requires the CL3 and CL4 signals in addition to the signals necessary for controlling TN-type LCDs, as shown in table 7-1. The CL3 and CL4 signals and the setting of the internal registers to control TFT-type LCDs are described below.

Table 7-1 LCD Control Signal Comparison

TN-Type LCD Control Signals	TFT-Type LCD Control Signals
CL1, CL2, FLM, M	CL1, CL2, CL3, CL4, FLM, M

Note: Double-height display requires the CL3 signal, even in the TN-type LCD modes.

7.1 CL3 and CL4 Signal Functions

In the TFT-type LCD modes, the CL3 signal functions as a line shift clock or a color data select clock, while the CL4 signal acts as a line shift clock. The high-level pulse width of the CL3 signal controls the data hold time of the LCD cells. Section 7.1.1 describes the use of the CL3 and CL4 signals as a line shift clock and a color data select clock, and section 7.1.2 describes the function of the high-level pulse width of the CL3 signal.

7.1.1 CL3 and CL4 Signals as Line Shift Clock and Color Data Select Clock

The CL3 and CL4 signals' functions depend on the display mode. Table 7-2 lists the clock functions by display mode (including the CL1 and CL2 signals).

Table 7-2 Clock Functions by Display Mode

Display Mode	Function				Reference Figure
	CL1	CL2	CL3	CL4	
1, 2, 4, 6–8 (TN-Type LCD, Normal Display)	Data latch Line shift	Data shift	—	—	7-3
1, 2, 4, 6–8 (TN-Type LCD, Double-Height Display[1])	Data latch	Data shift	Line shift	—	
9, 11 (TFT-Type LCD, Vertical Stripes, Y-Drivers on One Side)	Data latch	Data shift	Line shift	—	7-4
3, 5, 10, 12[2] (TFT-Type LCD, Vertical Stripes, Y-Drivers on Both Sides)	Data latch	Data shift	—	Line shift	
13, 15 (TFT-Type LCD, Horizontal Stripes, Y-Drivers on One Side)	Data latch	Data shift	Color data selection Line Shift	—	7-5
14, 16 (TFT-Type LCD, Horizontal Stripes, Y-Drivers on Both Sides)	Data latch	Data shift	Color data selection	Line shift	

Notes:

1. For details, refer to section 4, Double-Height Display.
2. Although display modes 3 and 5 are monochrome display modes, they are classified as vertical stripe modes.

The X- and Y-drivers operate in the TFT-type LCD modes as follows:

In Display Modes 9 and 11 (Vertical Stripes, Y-Drivers on One Side): The X-drivers latch the data for one line, and output it to the LCD panel at the falling edge of the CL1 signal. The Y-drivers scan a line of the LCD panel while the X-drivers are outputting data. The Y-drivers shift the line scan signal at the rising edge of the CL3 signal.

In Display Modes 3, 5, 10, and 12 (Vertical Stripes, Y-Drivers on Both Sides): The X-drivers latch the data for one line, and output it to the LCD panel at the falling edge of the CL1 signal. The right and left Y-drivers alternate in scanning a line of the LCD panel while the X-drivers are outputting data. The left Y-drivers shift the line scan signal at the rising edge of the CL4 signal, and the right Y-drivers shift it at the falling edge.

In Display Modes 13 and 15 (Horizontal Stripes, Y-Drivers on One Side): The X-drivers latch the data for one dot line (three cell lines) at the falling edge of the CL1 signal, and output the R data, G data, and B data in that order to the LCD panel at each falling edge of the CL3 signal. The Y-drivers scan a line (cell line) of the LCD panel while the X-drivers are outputting data. The Y-drivers shift the line (cell line) scan signal at the rising edge of the CL3 signal. (See figures 6-3 and 7-5 for the relationships between dot lines and cell lines.)

In Display Modes 14 and 16 (Horizontal Stripes, Y-Drivers on Both Sides): The X-drivers latch the data for one dot line (three cell lines) at the falling edge of the CL1 signal, and output the R data, G data, and B data in that order to the LCD panel at each falling edge of the CL3 signal. The right and left Y-drivers alternate in scanning a line (cell line) of the LCD panel while the X-drivers are outputting data. The left Y-drivers shift the line (cell line) scan signal at the rising edge of the CL4 signal and the right Y-drivers shift it at the falling edge. (See figures 6-3 and 7-5 for the relationships between dot lines and cell lines.)

Table 7-3 lists the connection of the CL1, CL2, CL3, and CL4 signals to the X- and Y-drivers in each mode.

Table 7-3 Clock and LCD Driver Connections by Display Mode

	CL1	**CL2**	**CL3**	**CL4**
Display Mode	**Connected to:**			
1, 2, 4, 6–8 (TN-Type LCD, Normal Display)	X- and Y-drivers	X-drivers	Open	Open
1, 2, 4, 6–8 (TN-Type LCD, Double-Height Display[1])	X-drivers	X-drivers	Y-drivers	Open
9, 11 (TFT-Type LCD, Vertical Stripes, Y-Drivers on One Side)	X-drivers	X-drivers	Y-drivers	Open

Table 7-3 Clock and LCD Driver Connections by Display Mode (cont.)

	CL1	CL2	CL3	CL4
Display Mode	**Connected to:**			
3, 5, 10, 12[2] (TFT-Type LCD, Vertical Stripes, Y-Drivers on Both Sides)	X-drivers	X-drivers	Open	Y-drivers
13, 15 (TFT-Type LCD, Horizontal Stripes, Y-Drivers on One Side)	X-drivers	X-drivers	X- and Y-drivers	Open
14, 16 (TFT-Type LCD, Horizontal Stripes, Y-Drivers on Both Sides)	X-drivers	X-drivers	X-drivers	Y-drivers

Notes:

1. For details, refer to section 4, Double-Height Display.
2. Although display modes 3 and 5 are monochrome display modes, they are classified as vertical stripe modes.

7.1.2 High-Level Pulse Width of CL3 Signal

Figure 7-1 shows the structure of a TFT-type LCD. Since the panel has a large number of elements attached to each liquid-crystal cell, the load capacity of the gate and drain electrodes is large. This delays the rising and falling times of the drain voltage waveform. The drain voltage applied to the liquid-crystal cells must not change until the gates of lines that are not selected have been completely shut. The rising edge of the CL3 signal provides the Y-drivers with the timing necessary for shutting the gates.

If the high-level pulse width of the CL3 signal is too short, liquid-crystal cells may latch the data for the next line (the shaded parts of figure 7-2). To solve this problem, the high-level pulse width of the CL3 signal must be increased to generate a data hold time. However, if the high-level pulse width of the CL3 signal is too big, the data write time is insufficient. Therefore, the high-level pulse width of the CL3 signal must be determined in consideration of both the data hold time and the data write time of the TFT-type LCD panel.

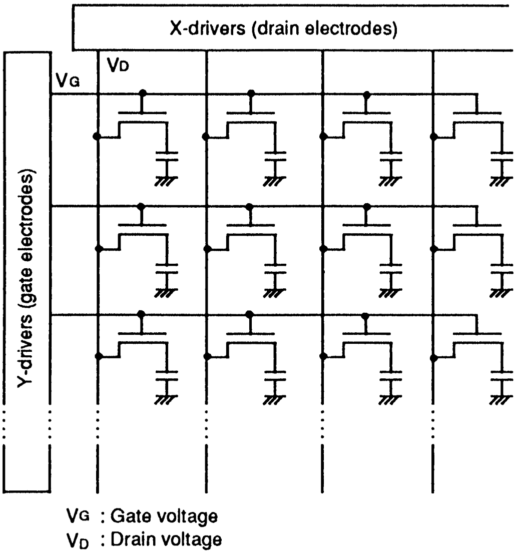
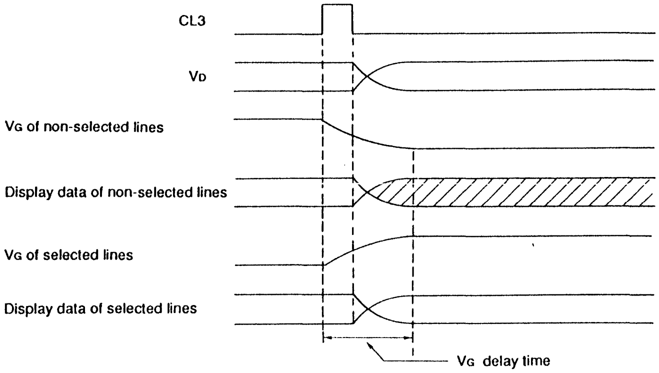
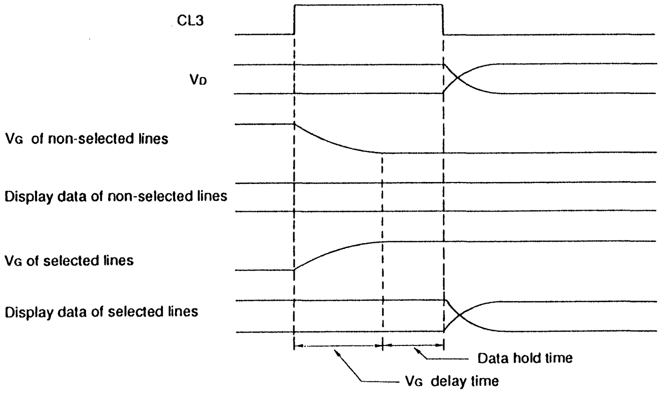


Figure 7-1 TFT-Type LCD Structure


CL3
VD
VG of non-selected lines
Display data of non-selected lines
VG of selected lines
Display data of selected lines
VG delay time

When the high-level pulse width of the CL3 signal is insufficient



When the high-level pulse width of the CL3 signal is appropriate

V_G: Gate voltage

V_D: Drain voltage

Figure 7-2 CL3 Signal High-Level Pulse Width

7.2 CL3 and CL4 Signal Output and Register Setting

Both the pin and the internal register programming methods can be used to control TFT-type LCDs. There is no need to do anything particular with the pin programming method, since the display mode automatically determines the CL3 and CL4 signal output (period and high-level pulse width). However, parameters must be set in the CL3 pulse width register (R8) when the internal register programming method is used. Section 7.2.1 describes the CL3 and CL4 signal outputs for different display modes for the pin programming method, and section 7.2.2 describes the parameter setting in registers for the internal register programming method.

7.2.1 CL3 and CL4 Signal Output in Pin Programming Method

Table 7-4 lists the CL3 signal outputs for different display modes with the pin programming method. As shown in the table, there are three classifications of CL3 signal period: the CL3 signal period is 1/2, 1/3, or the same as the CL1 signal period. Each case is described below in turn. Since the CL4 signal changes at the rising edge of the CL3 signal, its period is always twice that of the CL3 signal.

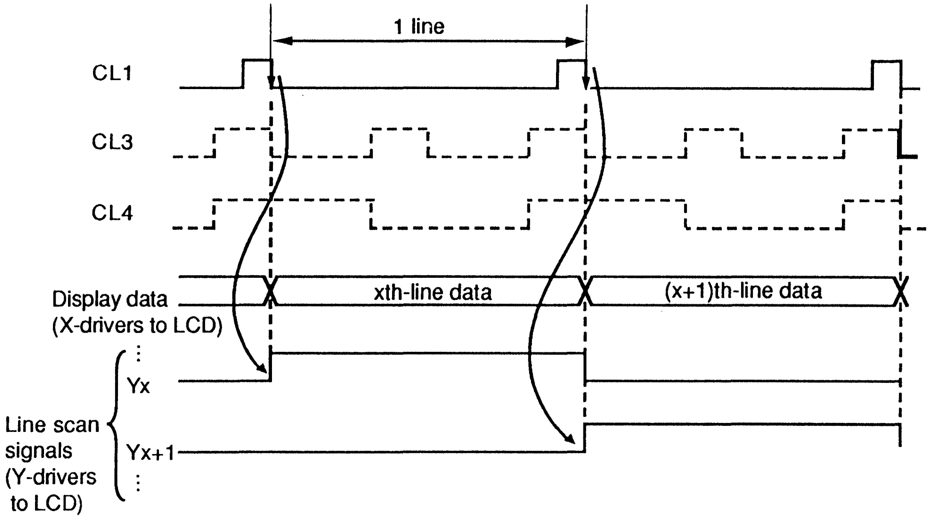
Table 7-4 CL3 Signal Output for Different Display Modes with Pin Programming Method

	CL3 Signal		CL1 Signal		
Display Modes	**Period A[1,2]**	**High-Level Pulse Width[1,2]**	**Period B[1,2]**	**A/B**	**Reference Figure**
1, 2, 4, 6– 8 (TN-Type LCD)	43 48	9 11	86 96	1/2	7-3
3, 5, 9–12 (TFT-Type LCD, Vertical Stripes)	86 96	14 16	86 96	1	7-4
13–16 (TFT-Type LCD, Horizontal Stripes)	27 31	14 16	86 96	≒ 1/3	7-5

Notes:

1. The unit is one character (where one character consists of eight dots).
2. The numbers on the upper row correspond to the configuration in which the number of horizontal characters is 80 (640 dots), and the numbers on the lower row to that in which it is 90 (720 dots).

CL3 and CL4 Signal Output in TN-Type LCD Modes (Display Modes 1, 2, 4, and 6-8): Figure 7-3 shows the CL3 and CL4 signal output timing in the TN-type LCD modes. The CL3 signal period is half the CL1 signal period in these modes. Normal display does not require the CL3 or CL4 signal. However, double-height display is enabled when the CL3 signal is connected to the Y-drivers and is used as a line shift clock instead of the CL1 signal. For details of double-height display, refer to section 4, Double-Height Dispaly.



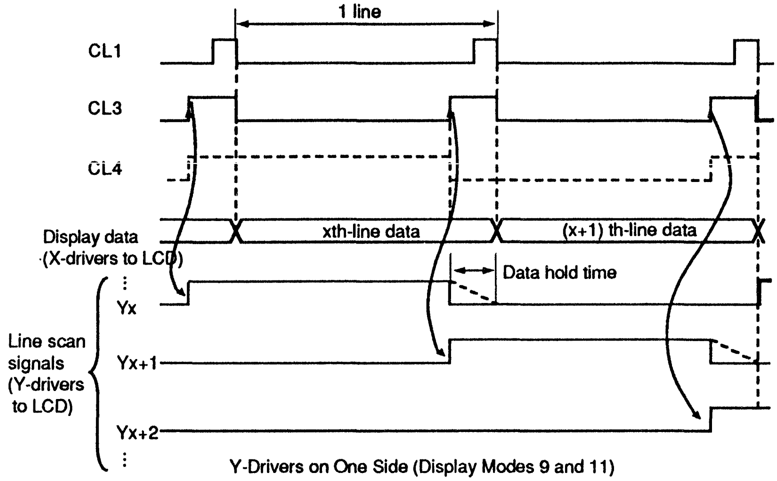
Note : See table 7-4 for the specifications of the CL3 signal period and high-level pulse width.

Figure 7-3 Timing of CL3 and CL4 Signal Output in TN-Type LCD Modes (Display Modes 1, 2, 4, and 6–8)

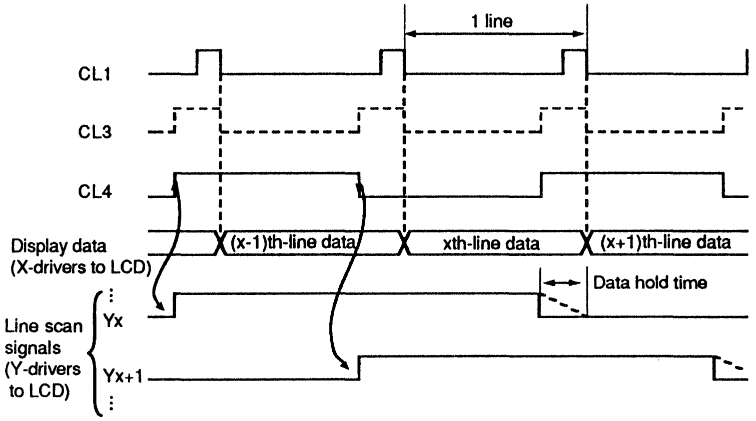
CL3 and CL4 Signal Output in TFT-Type LCD Modes with Vertical Stripes (Display Modes 3, 5, and 9–12): Figure 7-4 shows the CL3 and CL4 signal output timing in the TFT-type LCD modes with vertical stripes. The CL3 signal period is the same as the CL1 signal period in these modes.

In the modes for Y-drivers on one side, the CL1 signal is a data latch clock for the X-drivers and the CL3 signal is a line shift clock for the Y-drivers. The CL3 signal also controls the data hold time. The CL4 signal is not necessary. (Refer to tables 7-2 and 7-3.)

In the modes for Y-drivers on both sides, the CL1 signal is a data latch clock for the X-drivers and the CL4 signal is a line shift clock for the Y-drivers. The high-level pulse width of the CL3 signal controls the data hold time, but it is not necessary to connect the CL3 signal to the drivers since the CL4 signal includes information for controlling the data hold time. (Refer to table 7-2 and 7-3.)



Y-Drivers on One Side (Display Modes 9 and 11)



Y-Drivers on Both Sides (Display Modes 3, 5, 10, and 12)

Note : See table 7-4 for the specifications of the CL3 signal period and high-level pulse width.

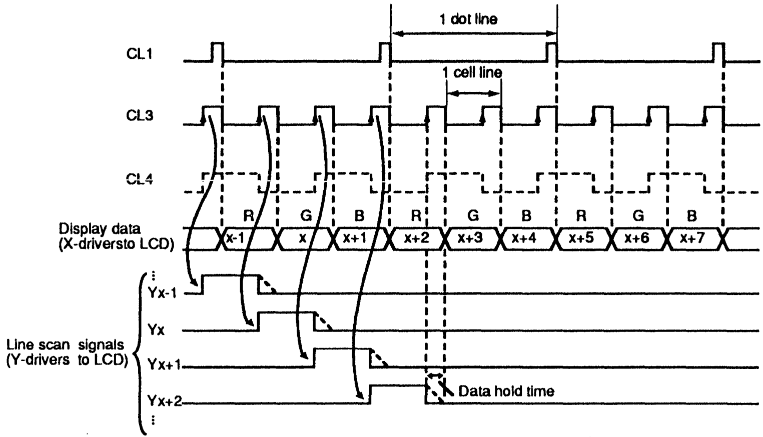
Figure 7-4 Timing of CL3 and CL4 Signal Output in TFT-Type LCD Modes with Vertical Stripes (Display Modes 3, 5, and 9–12)

CL3 and CL4 Signal Output in TFT-Type LCD Modes with Horizontal Stripes (Display Modes 13–16): Figure 7-5 shows the CL3 and CL4 signal output timing in the TFT-type LCD modes with horizontal stripes. The CL3 signal period is a third of the CL1 signal period in these modes.

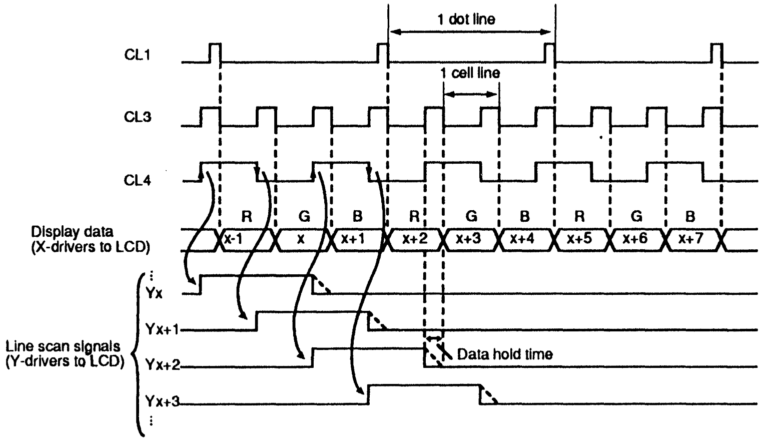
In the horizontal stripe modes, R, G, and B data is each arranged horizontally on the LCD panel and three cell lines represent one dot line. (For details of cell lines and dot lines, refer to section 6.1.3, 8-Color Display. Therefore, X-drivers output R, G, and B data in that order during one dot-line period.

In the modes for Y-drivers on one side, the CL1 signal is a data latch clock for the X-drivers and the CL3 signal is both a color data select clock for the X-drivers and a cell line shift clock for the Y-drivers. The CL3 signal also controls data hold time. The CL4 signal is not necessary. (Refer to tables 7-2 and 7-3.)

In the modes for Y-drivers on both sides, the CL1 signal is a data latch clock for the X-drivers and the CL3 signal is a color data select clock for the X-drivers; the CL3 signal also controls data hold time. The CL4 signal is a cell line shift clock for the Y-drivers. (Refer to tables 7-2 and 7-3.)



Y-Drivers on One Side (Display Modes 13 and 15)



Y-Drivers on Both Sides (Display Modes 14 and 16)

Note : See table 7-4 for the specifications of the CL3 signal period and high–level pulse width.

Figure 7-5 Timing of CL3 and CL4 Signal Output in TFT-Type LCD Modes with Horizontal Stripes (Display Modes 13–16)

7.2.2 Parameter Setting in Internal Register Programming Method

The CL3 signal period must be specified in such a way that it maintains the correct relationship with the CL1 signal in TFT-type LCD modes. The CL3 signal high-level pulse width must also be specified since different TFT-type LCD panels have different appropriate data hold times. This is because the load capacity of gate electrodes depends on panel size.

Specify CL3 signal period with the CL3 period register (R5) and the CL3 signal high-level pulse width with the CL3 pulse width register (R8).

As shown in table 7-5, the number of horizontal displayed characters (Nhd) automatically determines the CL3 signal period so the CL3 period register is invalid in display modes other than those for TFT-type LCDs with horizontal stripes, i.e., display modes 1 to 12. Therefore, there is no need to set a parameter in the CL3 period register in these modes. However, a parameter must be set in the CL3 pulse register in each mode.

Table 7-5 CL3 Signal Output for Different Display Modes with Internal Register Programming Method

	CL3 Signal	
Display Mode	**Period**	**High-Level Pulse Width**
1, 6 (TN-Type LCD, Dual Screen)	Fixed to (Nhd + 6)	Specified by CL3 pulse width register
2, 4, 7, 8 (TN-Type LCD, Single Screen)	Fixed to 1/2 (Nhd + 6)	
3, 5, 9–12 (TFT-Type LCD, Vertical Stripes)	Fixed to (Nhd + 6)	
13–16 (TFT-Type LCD, Horizontal Stripes)	Specified by CL3 period register	

Nhd: Number of horizontal displayed characters (number of horizontal displayed dots × 1/8)

CL3 Signal Period Setting: The CL3 signal period must be one third of the CL1 signal period in the display modes for TFT-type LCDs with horizontal stripes (display modes 13–16). Therefore, the value to be written into the CL3 period register (R5) is (Nhd + 6) × 1/3 – 1, where Nhd is the number of horizontal displayed characters (number of horizontal displayed dots × 1/8).

Table 7-6 shows the correspondences between the number of horizontal displayed characters, the CL3 signal period, and the value to be written into the CL3 period register (R5).

Table 7-6 Number of Horizontal Displayed Characters and Value in CL3 Period Register

No. of Horizontal Displayed Characters	CL3 Signal Period (Character)	Value in CL3 Period Register (R5)
90 (720 dots)	32	31 ⟶ (11111)
80 (640 dots)	28 or 29	27 ⟶ (11011) or 28 ⟶(11100)
60 (480 dots)	22	21 ⟶ (10101)
50 (400 dots)	18 or 19	17 ⟶ (10001) or 18 ⟶(10010)

CL3 Signal High-Level Pulse Width Setting: The optimum value of the CL3 signal high-level pulse width, namely Npw (number of dots during the CL3 signal high-level pulse width × 1/8), is determined by the gate voltage waveform delay time as described in section 7.1.2, High-Level Pulse Width of CL3 Signal. The gate voltage waveform delay time depends on the LCD panel specifications.

First find Npw from the specifications for the LCD panel, then set that parameter in the CL3 pulse width register (R8). Write (Npw – 5) for the TFT-type LCD modes (display modes 3, 5, and 9–16), or Npw for the TN-type LCD modes (display modes 1, 2, 4, and 6–8). However, since the CL3 signal high-level pulse width is meaningless in the TN-type LCD modes, any value less than the CL3 signal period can be written. (Writing a value other than (Npw – 5) does not affect the LVIC's operations as long as it is less than the CL3 signal period.) Refer to table 7-5 for the CL3 signal period used in the internal register programming method.

When using the internal register programming method, always set a parameter in the CL3 pulse width register even if the display mode does not require the CL3 or CL4 signal.

Section 8 Application Circuits

8.1 LVIC Installed in Personal Computer

There are two configurations for installing an LVIC in a personal computer:

- LVIC installed on the CRT display board.
- LVIC installed independently on a extension board for LCD display.

The installation of an LVIC on an extension board is described below. Table 8-1 lists the circuit specifications and figure 8-1 is a circuit diagram.

8.1.1 Circuit Specifications

Table 8-1 Circuit Specifications 1

Item	Specification
Display Format	Single screen, 8-level gray scale display (display mode 7)
Display Screen Size	640 × 200 dots
Clock Frequency	f_{DOTCLK} = 14.31818 MHz (system clock) f_{LDOTCK} = 9.632 MHz
Buffer Memory	32-kbyte memory × 3 (SRAM HM62256 × 3)
Address Assignment	LVIC address register: $3ED LVIC data register: $3EE
LCD Interface	4 bits parallel × 1
LCD Specifications	LCD module LM250X (multiplexing duty ratio: 1/200)
Bus Interface	IBM-PC internal slot 8086 (8088) bus interface
CRT Display Interface	RGB video signals: TTL level, positive logic HSYNC signal: TTL level, positive logic VSYNC signal: TTL level, positive logic

f_{DOTCLK}: CRT display dot clock (DOTCLK) frequency

f_{LDOTCK}: LCD dot clock (LDOTCK) frequency

8.1.2 Circuit Diagram

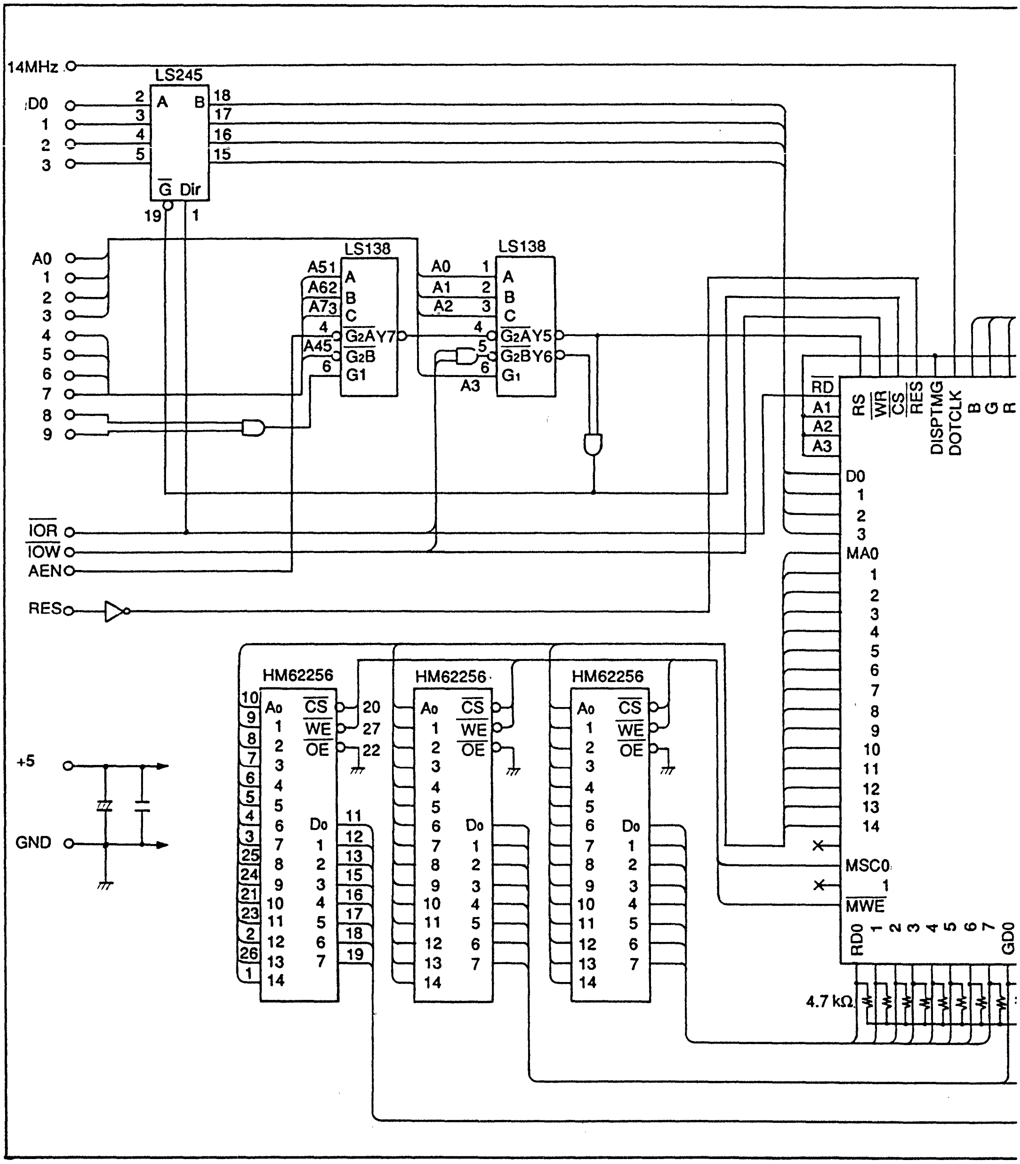
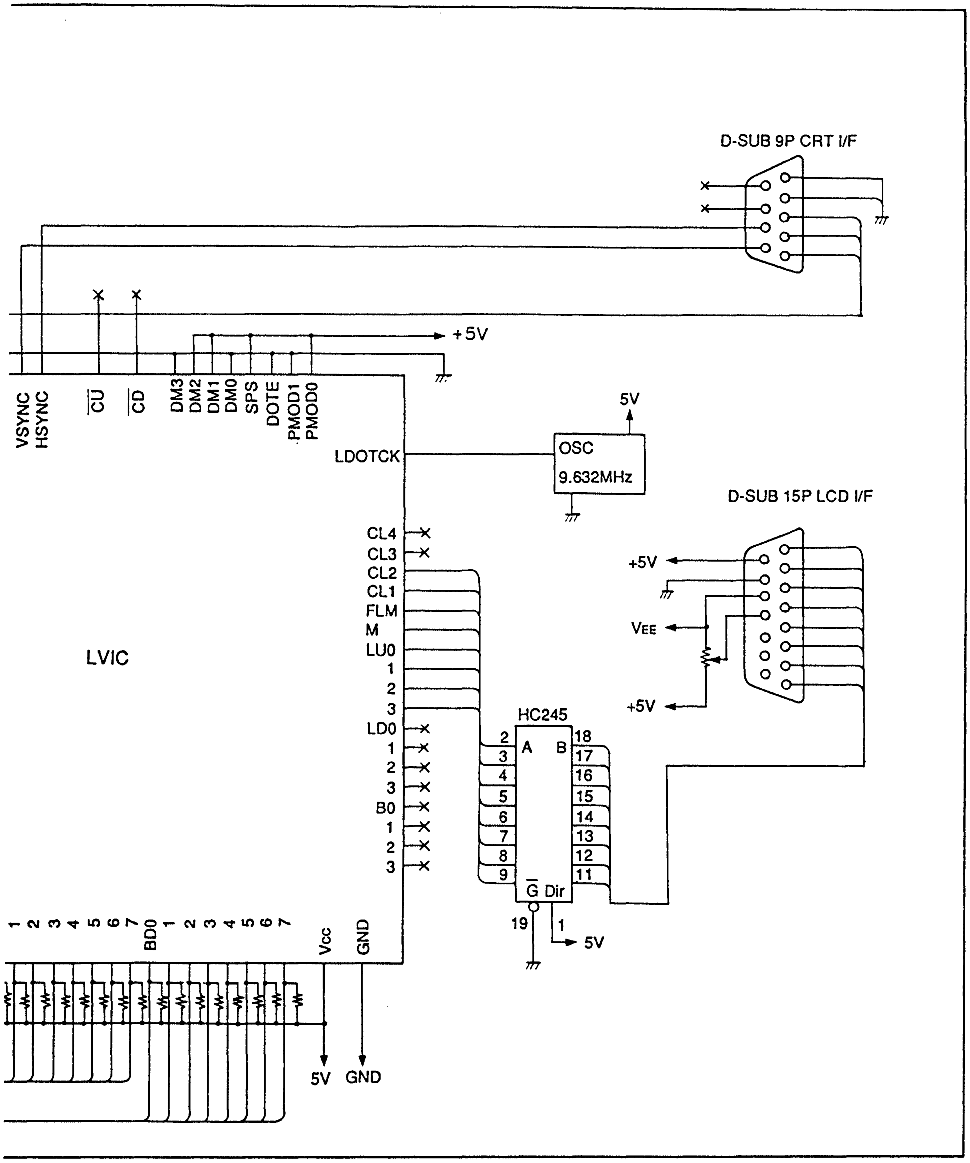


Figure 8-1 Circuit Example of LVIC Mounted on Extension-Slot Board (Suitable for CGA Board)


D-SUB 9P CRT I/F
+5V
VSYNC
HSYNC
CU
CD
DM3
DM2
DM1
DM0
SPS
DOTE
PMOD1
PMOD0
5V
LDOTCK
OSC
9.632MHz
D-SUB 15P LCD I/F
CL4
CL3
CL2
CL1
FLM
M
LU0
1
2
3
LD0
1
2
3
B0
1
2
3
+5V
VEE
+5V
LVIC
HC245
A
B
G Dir
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
19
1
5V
1
2
3
4
5
6
7
BD0
1
2
3
4
5
6
7
Vcc
GND
5V
GND

8.1.3 Circuit Description

The circuit described here receives video signals (R, G, and B data), and HSYNC and VSYNC signals through the output connector of the CGA board, and generates LCD signals. Since the display timing signal (DISPTMG) is not supplied, this circuit generates the signal internally from the parameters set in the LVIC internal registers by the MPU. The I/O decoder shown in the diagram generates the $\overline{CS}$ and RS signals. The LVIC address register is assigned to I/O port $3ED and the data register is assigned to $3EE. The LVIC internal registers can be read from and written to directly through the I/O port.

Figure 8-2 shows a program for initializing this circuit. Saving the auto-exec batch file shown in figure 8-3 in the same directory as the system program enables automatic LVIC initialization after power-on. Note, however, that the display on the screen will be random for several seconds after power-on since the data in the internal registers is undefined for a short period. In addition, this board cannot be used at the same time as another extension board or software which addresses I/O port $3ED or $3EE. In such a case, the I/O addresses must be changed.

If a ROM is used instead of an MPU to set parameters in the internal registers, set the parameters shown in table 8-4 into the ROM. This enables the circuit to be initialized immediately after power-on, avoiding the problem of display flickering. It also enables control of the board independently of the system software and hardware.

```
CODE_SET   SEGMENT
           ASSUME  CS:CODE_SET,DS:CODE_SET,SS:STACK_SET
           ORG   0100H
INIT:
           mov dx,3edh
           mov ax,0200h
           out  dx,ax                  ;Generate DISPTMG signal and supply DOTCLK
           mov ax,060lh                 signal supplied
           out  dx,ax                  ;Set display on, use 32-kbyte memories
           mov ax,0c02h
           out  dx,ax
           mov ax,0703h
           out  dx,ax                  ;Number of vertical displayed lines = 200
           mov ax,0104h
           out  dx,ax
           mov ax,0b05h
           out  dx,ax                  ;CL3 signal period = 27 characters[1]
           mov ax,0206h
           out  dx,ax
           mov ax,0707h
           out  dx,ax                  ;Number of horizontal displayed characters = 80
           mov ax,0408h
           out  dx,ax                  ;CL3 signal high-level pulse width = 4 characters[2]
           mov ax,0009h
           out  dx,ax                  ;Invalid
           mov ax,0b0ah
           out  dx,ax
           mov ax,050bh
           out  dx,ax                  ;PLL frequency-division ratio = 912[1]
           mov ax,020ch
           out  dx,ax
           mov ax,040dh
           out  dx,ax                  ;Vertical back porch = 37 lines
           mov ax,0b0eh
           out  dx,ax
           mov ax,000fh
           out  dx,ax                  ;Horizontal back porch = 177 dots
           mov ah,4ch
           int  21h
CODE_SET   ENDS
STACK_SET  SEGMENT
           DB ?
STACK_SET  ENDS
           END INIT
```

Notes:

1. This circuit example ignores these values. Any value can be set.
2. Although this circuit example does not use the function controlled by this register, it does not ignore the value set in it, so this value is necessary.

Figure 8-2 Initialization Program

```
ECHO OFF
INIT
ECHO ON
DATE
TIME
```

Figure 8-3 Auto-Exec Batch File

8.2 LVIC Installed Outside Personal Computer (Dot Clock Generated)

This section describes a circuit in which the LVIC is installed outside a personal computer and the LVIC generates its dot clock (DOTCLK) internally. This circuit is suitable for use with the IBM-PC EGA board. Table 8-2 lists the circuit specifications and figure 8-4 is a circuit diagram.

8.2.1 Circuit Specifications

Table 8-2 Circuit Specifications 2

Item	Specification
Display Format	Dual screen, monochrome or 8-level gray scale display
Display Screen Size	640 × 400 dots
Clock Frequency	f_{DOTCLK} = 16.257 MHz (generated by PLL circuit) f_{LDOTCK} = 16.257 MHz (identical to DOTCLK)
Buffer Memory	32-kbyte memory × 3 (SRAM HM62256 × 3)
LCD Interface	4 bits parallel × 2 (drives dual screen)
LCD Specifications	LCD module LM252X (multiplexing duty ratio: 1/200)
PLL Circuit Specifications	Oscillation frequency range: 11 MHz to 17 MHz Pull-in time: less than or equal to 10 ms Dot clock jitter quantity: less than or equal to 1/4 clock
CRT Display Interface	RGB video signals: TTL level, positive logic HSYNC signal: TTL level, positive logic VSYNC signal: TTL level, negative logic

f_{DOTCLK}: CRT display dot clock (DOTCLK) frequency

f_{LDOTCK}: LCD dot clock (LDOTCK) frequency

8.2.2 Circuit Diagram

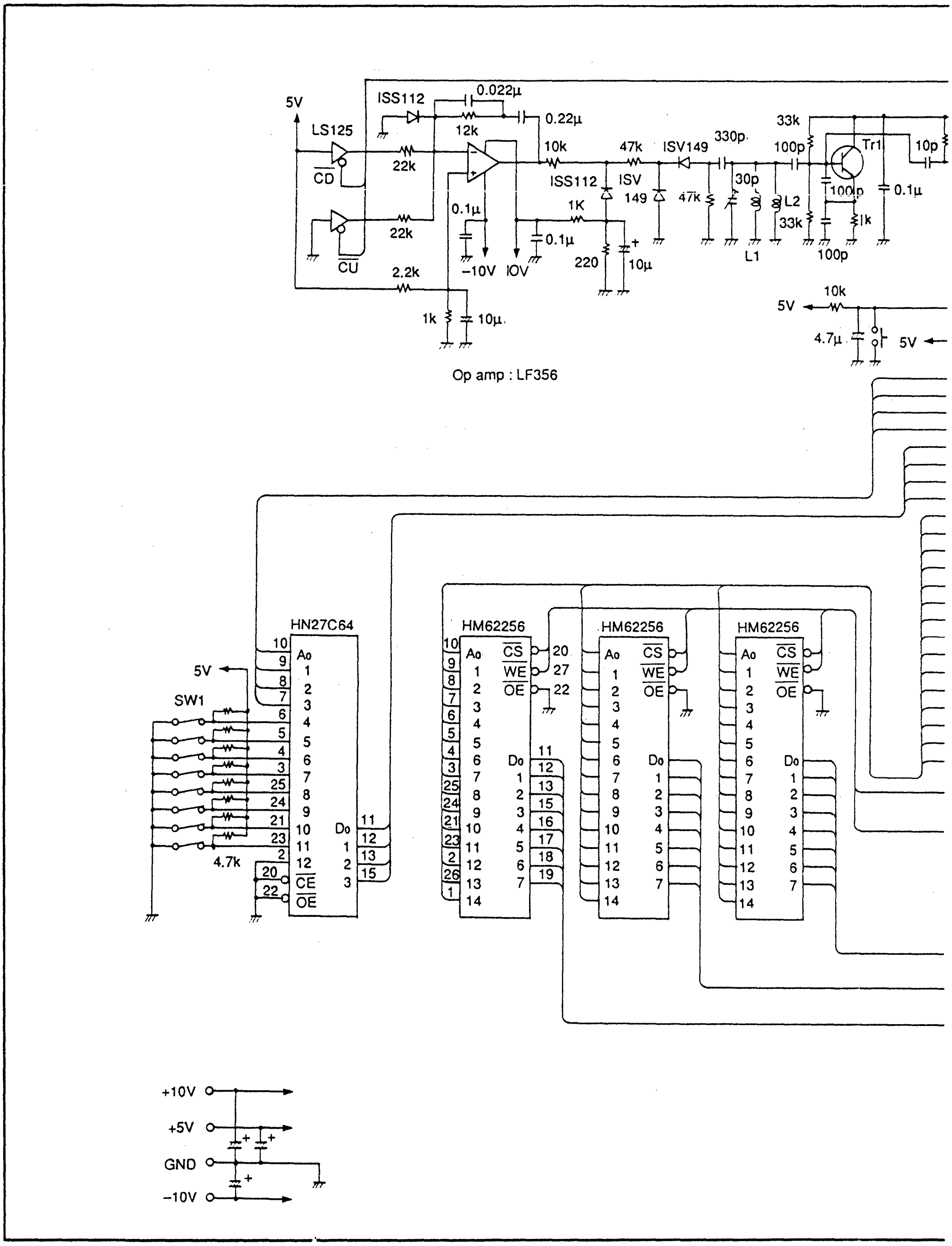
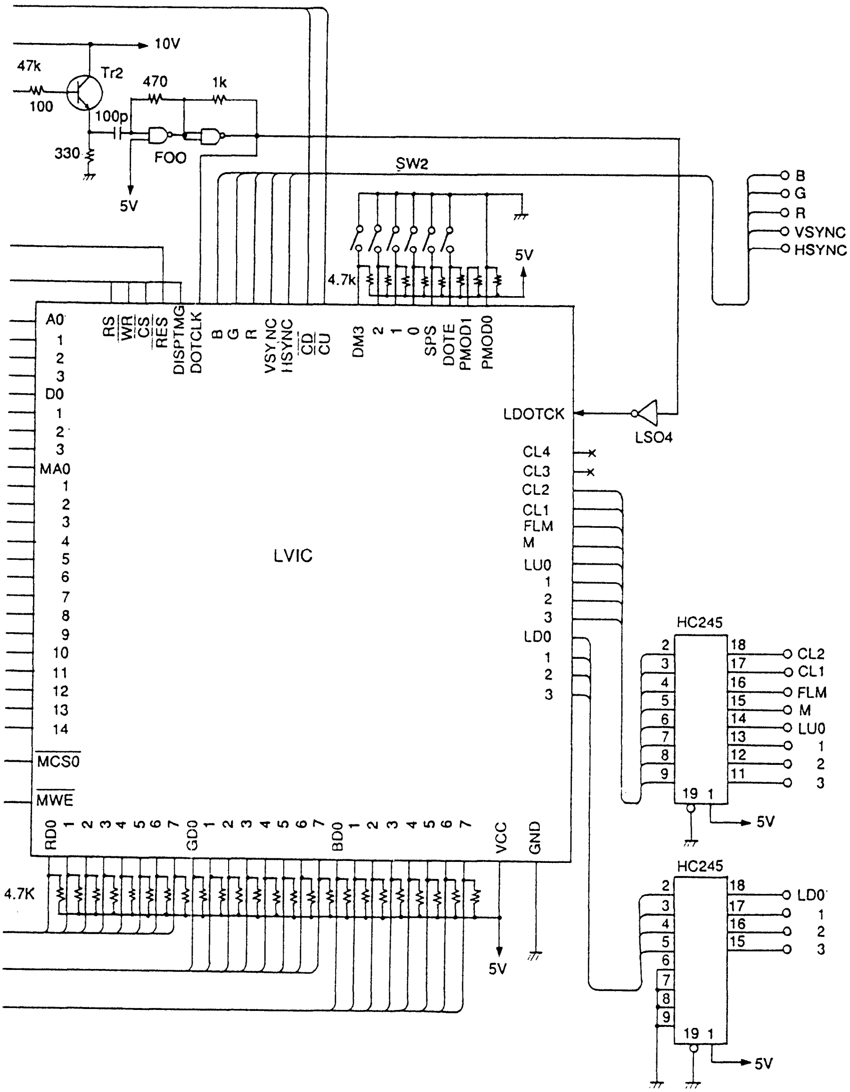


Figure 8-4 CRT Plug-Compatible Circuit Example 1
(Suitable for EGA Board)


10V
47k
Tr2
100
470
1k
100p
330
FOO
5V
SW2
4.7k
5V
B
G
R
VSYNC
HSYNC
A0
1
2
3
D0
1
2
3
MA0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
MCS0
MWE
RS
WR
CS
RES
DISPTMG
DOTCLK
B
G
R
VSYNC
HSYNC
CD
CU
DM3
2
1
0
SPS
DOTE
PMOD1
PMOD0
LDOTCK
LS04
CL4
CL3
CL2
CL1
FLM
M
LU0
1
2
3
LD0
1
2
3
LVIC
RD0 1 2 3 4 5 6 7
GD0 1 2 3 4 5 6 7
BD0 1 2 3 4 5 6 7
VCC
GND
4.7K
5V
HC245
2 3 4 5 6 7 8 9
18 17 16 15 14 13 12 11
19 1
CL2
CL1
FLM
M
LU0
1
2
3
5V
HC245
2 3 4 5 6 7 8 9
18 17 16 15
19 1
LD0
1
2
3
5V

8.2.3 Circuit Description

Figure 8-5 is the block diagram of this circuit. The circuit is composed of the LVIC, a buffer memory, a PLL circuit, an output buffer, and a ROM. The ROM is used for setting parameters in the LVIC's internal registers. The parameters to be set in the ROM when an EGA-compatible board (EGA master) is used are listed in table 8-5. Since the vertical and horizontal back porches may differ in various compatible boards, these values should be measured. Specify 400 lines as the number of vertical displayed lines, even if the CRT's display screen size is 640 × 350 dots. This is because the screen is displayed on an LCD panel of 640 × 400 dots. In this case, the frame frequency (FLM signal frequency) is 59 Hz.

The dot clock (DOTCLK) is not included among the standard video interface signals, and the EGA board does not supply the DOTCLK signal either. Therefore, the analog PLL circuit in this circuit, which is composed of the LVIC internal programmable counter, the phase comparator, and other external circuits, generates the DOTCLK signal. Since instability of the oscillation frequency or the phase of the PLL circuit could cause LCD screen distortion, take extra care to reduce noise in the PLL circuit and its power-supplying wires when designing the circuit. (For more details, refer to section 3.3.2, PLL Circuit Design.)

Since the EGA board supports the same screen size as a CGA board (640 × 200 dots), the LVIC pins or registers must be reset when software for controlling a screen size of 640 × 200 dots is used. Switching SW1 to change the ROM addresses enables CGA support. In this case, change the LCD dot clock (LDOTCK) frequency. When displaying a screen of 640 × 200 dots on an LCD panel of 640 × 400 dots, use the double-height display. Use the CL3 signal instead of the CL1 signal as a shift clock for the LCD module's Y-drivers. (Refer to section 4, Double-Height Display, for details.)

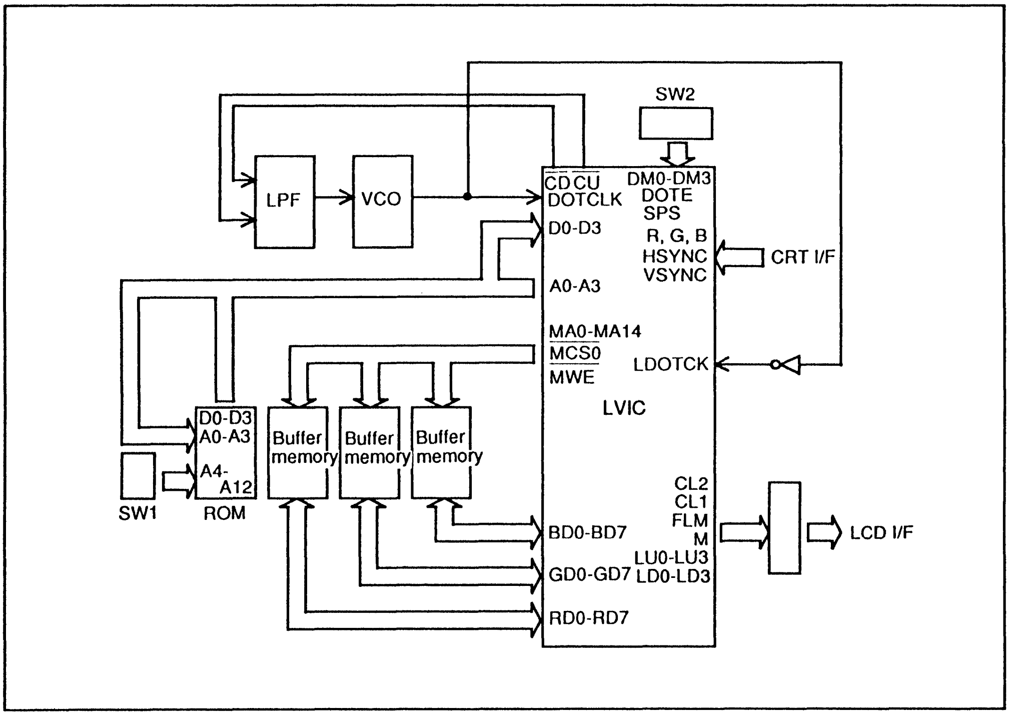


Figure 8-5 CRT Plug-Compatible Board Block Diagram (Suitable for EGA Board)

8.3 LVIC Installed Outside Personal Computer (Dot Clock Supplied)

This section describes a circuit in which the LVIC is installed outside a personal computer, with the dot clock (DOTCLK) supplied externally. In the specific example given below, the PC-9801 supplies the DOTCLK signal as one of the CRT display interface signals. Table 8-3 lists the circuit specifications and figure 8-6 is a circuit diagram.

8.3.1 Circuit Specifications

Table 8-3 Circuit Specifications 3

Item	Specification
Display Format	Dual screen, monochrome or 8-level gray scale display
Display Screen Size	640 × 400 dots
Clock Frequency	f_{DOTCLK} = 21.0526 MHz (system clock) f_{LDOTCK} = 19.264 MHz
Buffer Memory	32-kbyte memory × 3 (SRAM HM62256 × 3)
LCD Interface	4 bits parallel × 2 (drives dual screen)
LCD Specifications	LCD module LM252X (multiplexing duty ratio: 1/200)
CRT Display Interface	RGB video signals: TTL level, positive logic HSYNC signal: TTL level, negative logic VSYNC signal: TTL level, negative logic Dot clock: TTL level

f_{DOTCLK}: CRT display dot clock (DOTCLK) frequency

f_{LDOTCK}: LCD dot clock (LDOTCK) frequency

8.3.2 Circuit Diagram

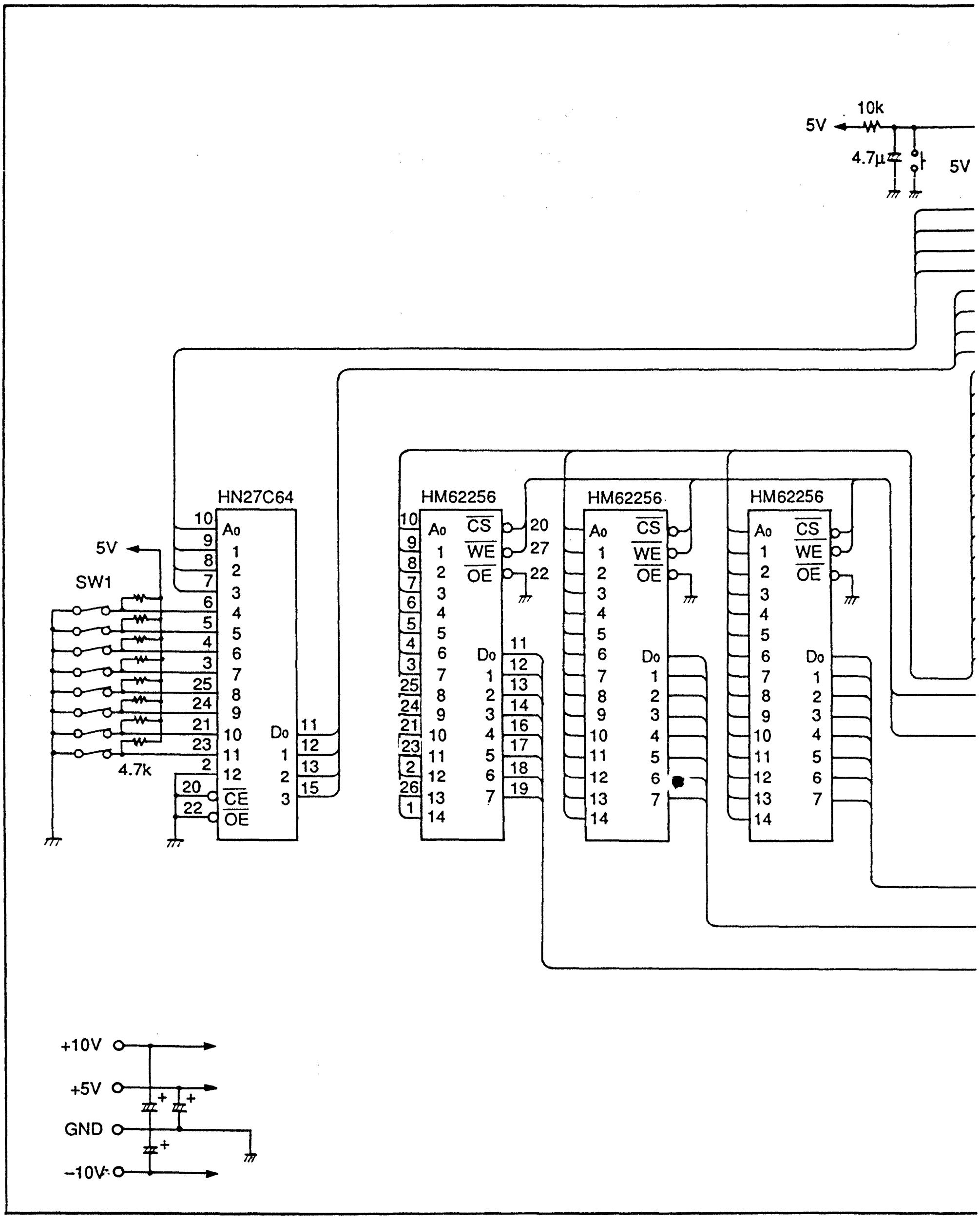
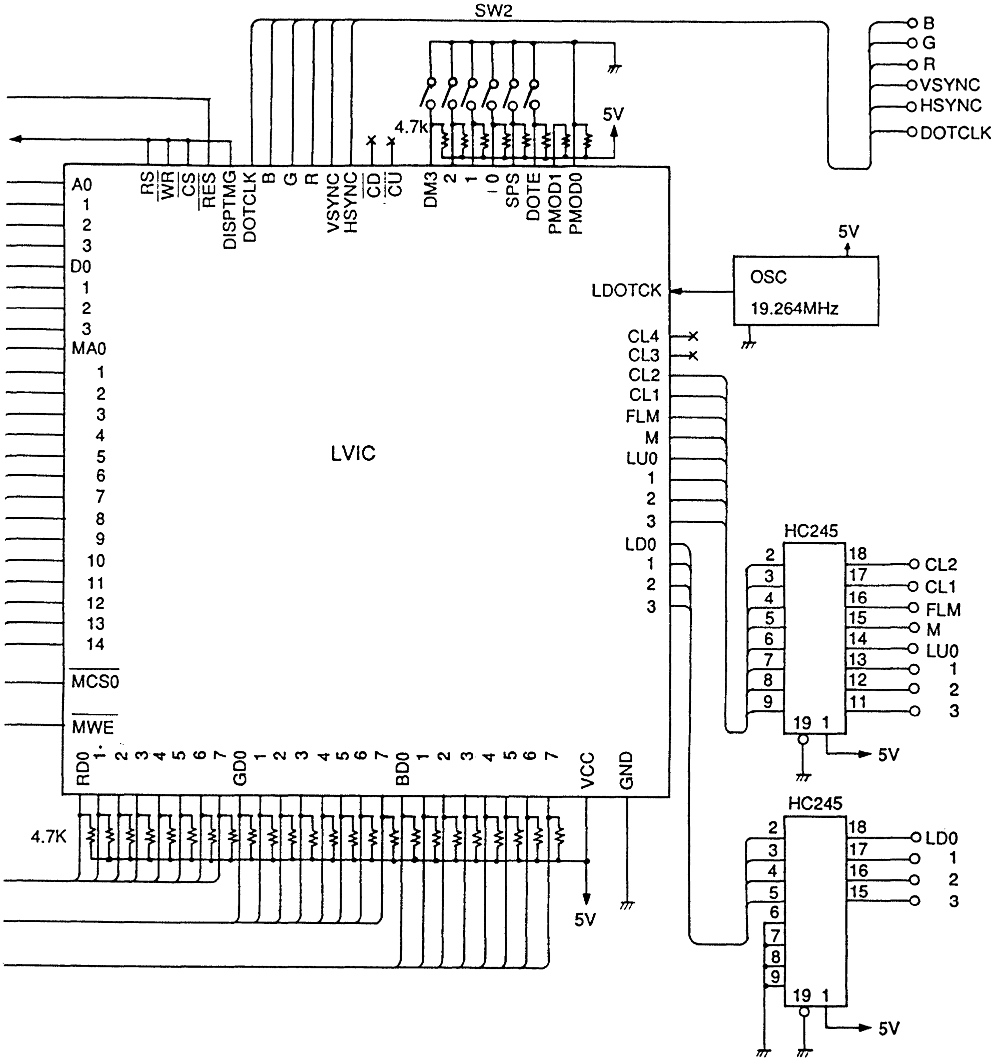


Figure 8-6 CRT Plug-Compatible Circuit Example 2
(Suitable for PC-9801 Board)


SW2
B
G
R
VSYNC
HSYNC
DOTCLK
4.7k
5V
RS
WR
CS
RES
DISPTMG
DOTCLK
B
G
R
VSYNC
HSYNC
CD
CU
DM3
2
1
0
SPS
DOTE
PMOD1
PMOD0
A0
1
2
3
D0
1
2
3
MA0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
MCS0
MWE
LVIC
LDOTCK
OSC
19.264MHz
5V
CL4
CL3
CL2
CL1
FLM
M
LU0
1
2
3
LD0
1
2
3
RD0
1
2
3
4
5
6
7
GD0
1
2
3
4
5
6
7
BD0
1
2
3
4
5
6
7
VCC
GND
4.7K
5V
HC245
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
19
1
CL2
CL1
FLM
M
LU0
1
2
3
5V
HC245
2
3
4
5
6
7
8
9
18
17
16
15
19
1
LD0
1
2
3
5V

8.3.3 Circuit Description

The circuit given here is almost the same as the circuit for the EGA board shown in figure 8-4, except for the following two points: this circuit receives the dot clock (DOTCLK) from the system whereas that for the EGA board generates it internally, and the LCD dot clock (LDOTCK) differs from the DOTCLK signal in this circuit. However, the vertical and the horizontal back porches are different. Refer to table 8-6 in section 8.4, Values in Internal Registers for Different CRT Display Systems, for details.

8.4 Values in Internal Registers for Different CRT Display Systems

When the LVIC is controlled by the internal register programming method, parameters are set in the internal registers. Parameters must always be set in control registers 1 and 2, the horizontal displayed characters register, and the vertical displayed lines register. The setting of parameters in the other registers depends on which CRT display system is used. (Refer to section 1.6.2, Validation and Invalidation of Internal Registers, for details of when registers are valid or invalid.)

Tables 8-4 to 8-8 list the values to be set in the internal registers for major CRT display systems.

Table 8-4 Values in Internal Registers for CGA (640 × 200 Dots)

Reg. No.	Value	Contents
R0	/ / 1 0	DISPTMG signal generated
R1	0 1 1 0	Display on, 32-kbyte memories used
R2	1 1 0 0	Number of vertical displayed lines: 200
R3	0 1 1 1	
R4	0 0 0 1	CL3 signal period: 27 characters
R5	1 0 1 1	
R6	0 0 1 0	Number of horizontal displayed characters: 80
R7	0 1 1 1	
R8	0 1 0 0	CL3 signal high-level pulse width: 4 characters
R9	* * * *	Don't care
R10	* * * *	Don't care
R11	* * * *	

Table 8-4 Values in Internal Registers for CGA (640 × 200 Dots) (cont.)

Reg. No.	Value	Contents
R12	0 0 1 0	Vertical back porch: 37 lines(Note)
R13	0 1 0 0	
R14	1 0 1 1	Horizontal back porch: 177 dots
R15	0 0 0 0	

Note: SPS = high

Table 8-5 Values in Internal Registers for EGA (640 × 350 Dots, EGA Master)

Reg. No.	Value	Contents
R0	/ / 1 1	DISPTMG and DOTCLK signals generated
R1	0 1 1 0	Display on, 32-kbyte memories used
R2	1 0 0 0	Number of vertical displayed lines: 400
R3	1 1 1 1	
R4	0 1 0 1	CL3 signal period: 27 characters
R5	1 0 1 1	
R6	0 0 1 0	Number of horizontal displayed characters: 80
R7	0 1 1 1	
R8	0 1 0 0	CL3 signal high-level pulse width: 4 characters
R9	* * * *	Don't care
R10	0 0 0 0	PLL frequency-division ratio: 744
R11	1 1 0 1	
R12	0 0 0 1	Vertical back porch: 32 lines(Note)
R13	1 1 1 1	
R14	0 1 1 0	Horizontal back porch: 108 dots
R15	1 0 1 1	

Note: SPS = low

Table 8-6 Values in Internal Registers for PC-9801 (640 × 400 Dots)

Reg. No.	Value	Contents
R0	/ / 1 0	DISPTMG signal generated
R1	0 1 1 0	Display on, 32-kbyte memories used
R2	1 0 0 0	Number of vertical displayed lines: 400
R3	1 1 1 1	

Table 8-6 Values in Internal Registers for PC-9801 (640 × 400 Dots) (cont.)

Reg. No.	Value	Contents
R4	0 1 0 1	CL3 signal period: 27 characters
R5	1 0 1 1	
R6	0 0 1 0	Number of horizontal displayed characters: 80
R7	0 1 1 1	
R8	0 1 0 0	CL3 signal high-level pulse width: 4 characters
R9	* * * *	Don't care
R10	* * * *	Don't care
R11	* * * *	
R12	0 0 0 1	Vertical back porch: 32 lines (Note)
R13	1 1 1 1	
R14	0 1 0 1	Horizontal back porch: 85 dots
R15	0 1 0 0	

Note: SPS = low

Table 8-7 Values in Internal Registers for PC-9801 (640 × 200 Dots)

Reg. No.	Value	Contents
R0	/ / 1 0	DISPTMG signal generated
R1	0 1 1 0	Display on, 32-kbyte memories used
R2	1 1 0 0	Number of vertical displayed lines: 200
R3	0 1 1 1	
R4	0 0 0 1	CL3 signal period: 27 characters
R5	1 0 1 1	
R6	0 0 1 0	Number of horizontal displayed characters: 80
R7	0 1 1 1	
R8	0 1 0 0	CL3 signal high-level pulse width: 4 characters
R9	* * * *	Don't care
R10	* * * *	Don't care
R11	* * * *	
R12	0 0 1 0	Vertical back porch: 36 lines (Note)
R13	0 0 1 1	
R14	1 0 0 0	Horizontal back porch: 133 dots
R15	0 1 0 0	

Note: SPS = low

Table 8-8 Values in Internal Registers for VGA (640 × 480 Dots)

Reg. No.	Value	Contents
R0	/ / 1 1	DISPTMG and DOTCLK signals generated
R1	0 1 1 0	Display on, 32-kbyte memories used
R2	1 1 0 1	Number of vertical displayed lines: 480
R3	1 1 1 1	
R4	0 1 0 1	CL3 signal period: 27 characters
R5	1 0 1 1	
R6	0 0 1 0	Number of horizontal displayed characters: 80
R7	0 1 1 1	
R8	0 1 0 0	CL3 signal high-level pulse width: 4 characters
R9	* * * *	Don't care
R10	0 1 0 0	PLL frequency-division ratio: 800
R11	0 1 0 1	
R12	0 0 1 0	Vertical back porch: 32 lines [1]
R13	0 0 1 0	
R14	1 0 0 0	Horizontal back porch: 144 dots[2]
R15	1 1 1 1	

Notes:

1. SPS = low
2. This value is the number of dots between the rising edge of the HSYNC signal and that of the DISPTMG signal after the HSYNC signal has been inverted by an inverter to be active-high.

Section 9 Additional Functions and External Circuits

This section describes some additional functions provided by the LVIC, and how to use these functions.

9.1 Centering Display Vertically (With External Circuit)

If the vertical size of a CRT display is less than that of an LCD panel but nothing is done to correct the positioning, the display will begin at the top of the panel, resulting in a blank space at the bottom. The frame frequency (FLM signal frequency) is also reduced.

It is easy to center the display vertically, without using an external circuit, by adjusting the vertical back porch. This method, however, is effective only when the number of HSYNC signal pulses during the vertical retrace period is more than the difference between the number of vertical displayed lines of the LCD and that of the CRT display. In addition, this method cannot prevent the reduction in frame frequency.

Adding the centering circuit shown in figure 9-1 can center the display as shown in figure 9-3, even if the number of HSYNC signal pulses during the vertical retrace period is less than the difference between the number of vertical displayed lines of the LCD and that of the CRT display. This method can also prevent the reduction in frame frequency.

Refer to section 9.2, Centering Display Horizontally, for details of how to center the display horizontally.

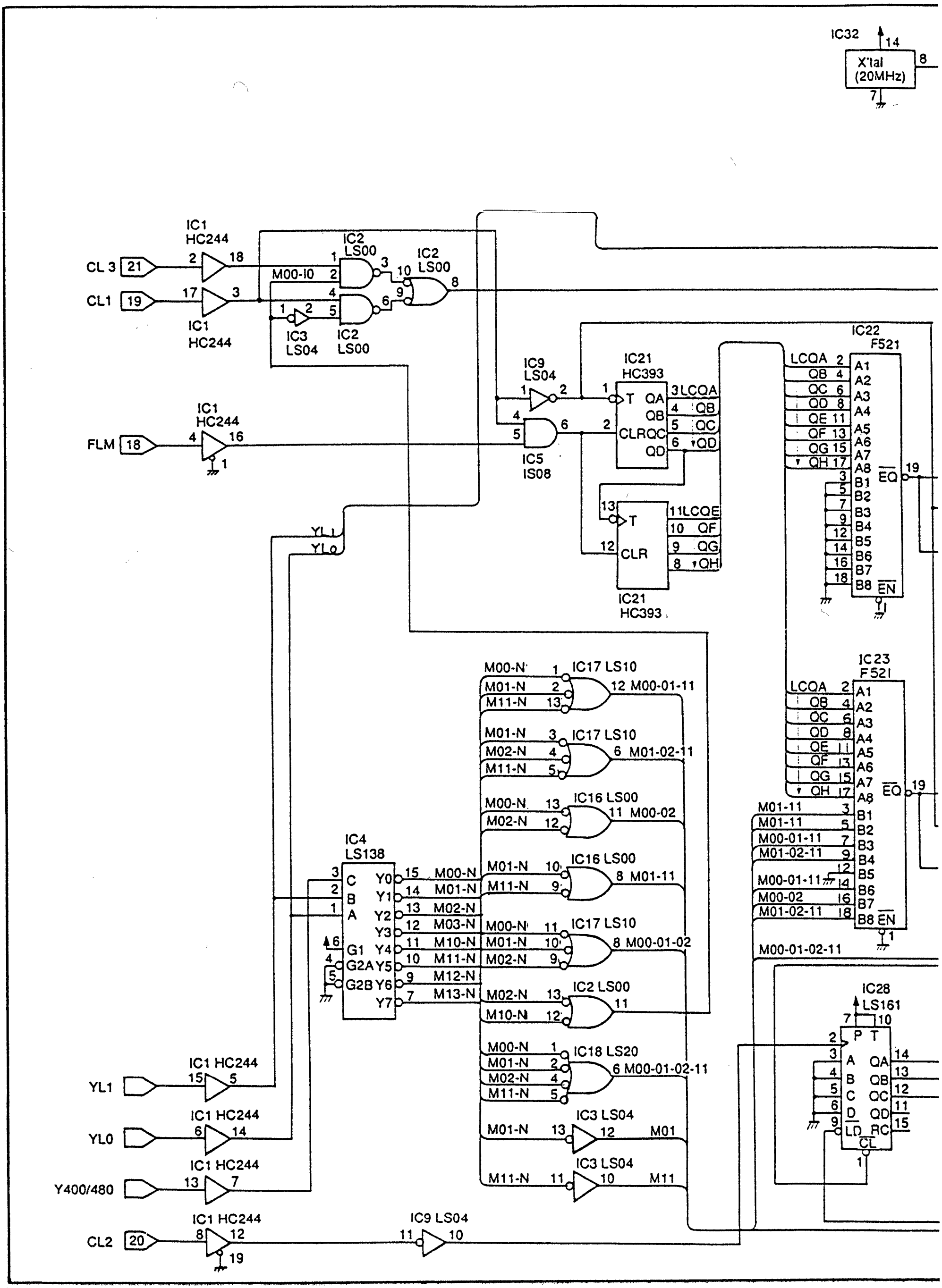
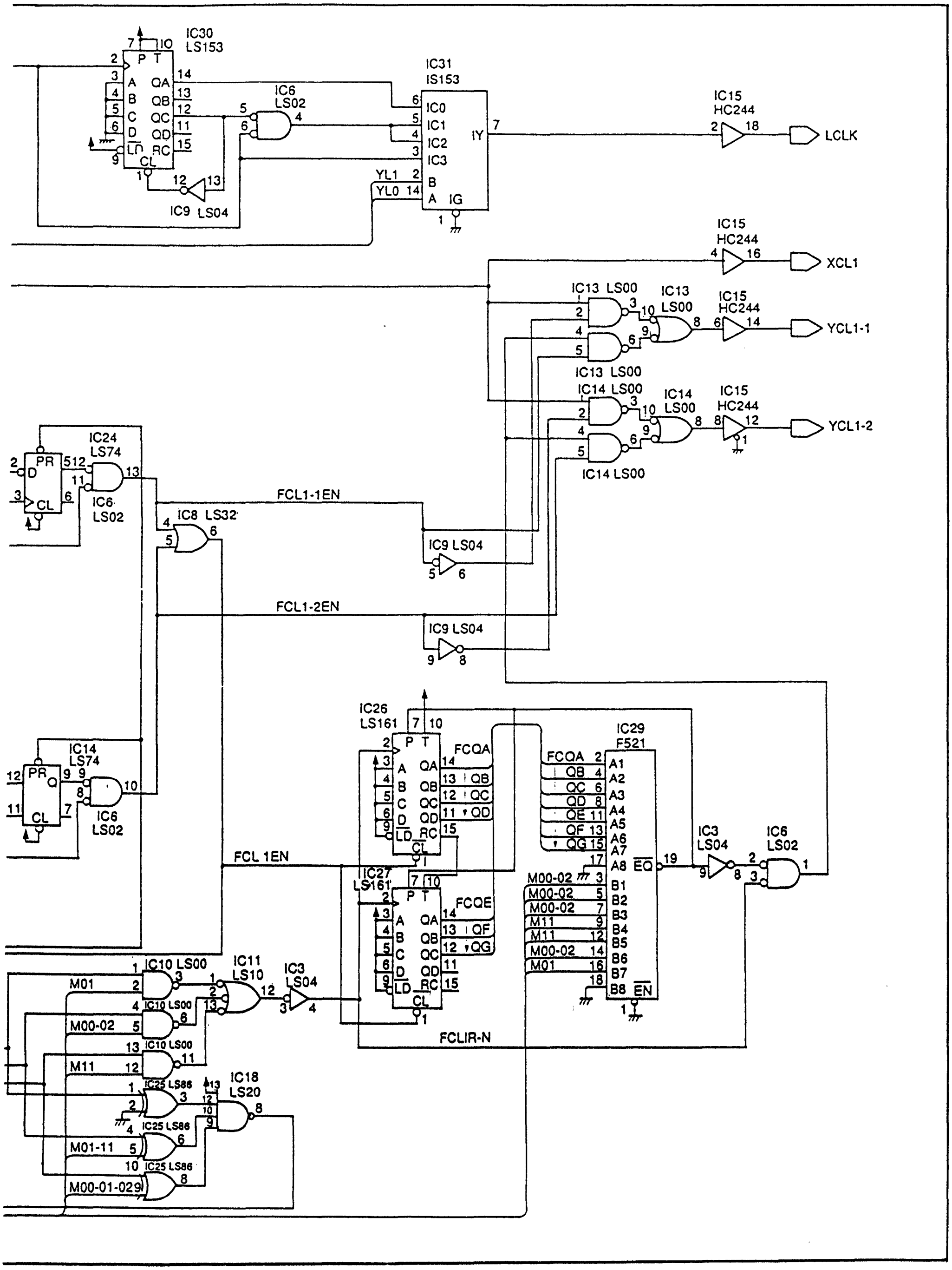
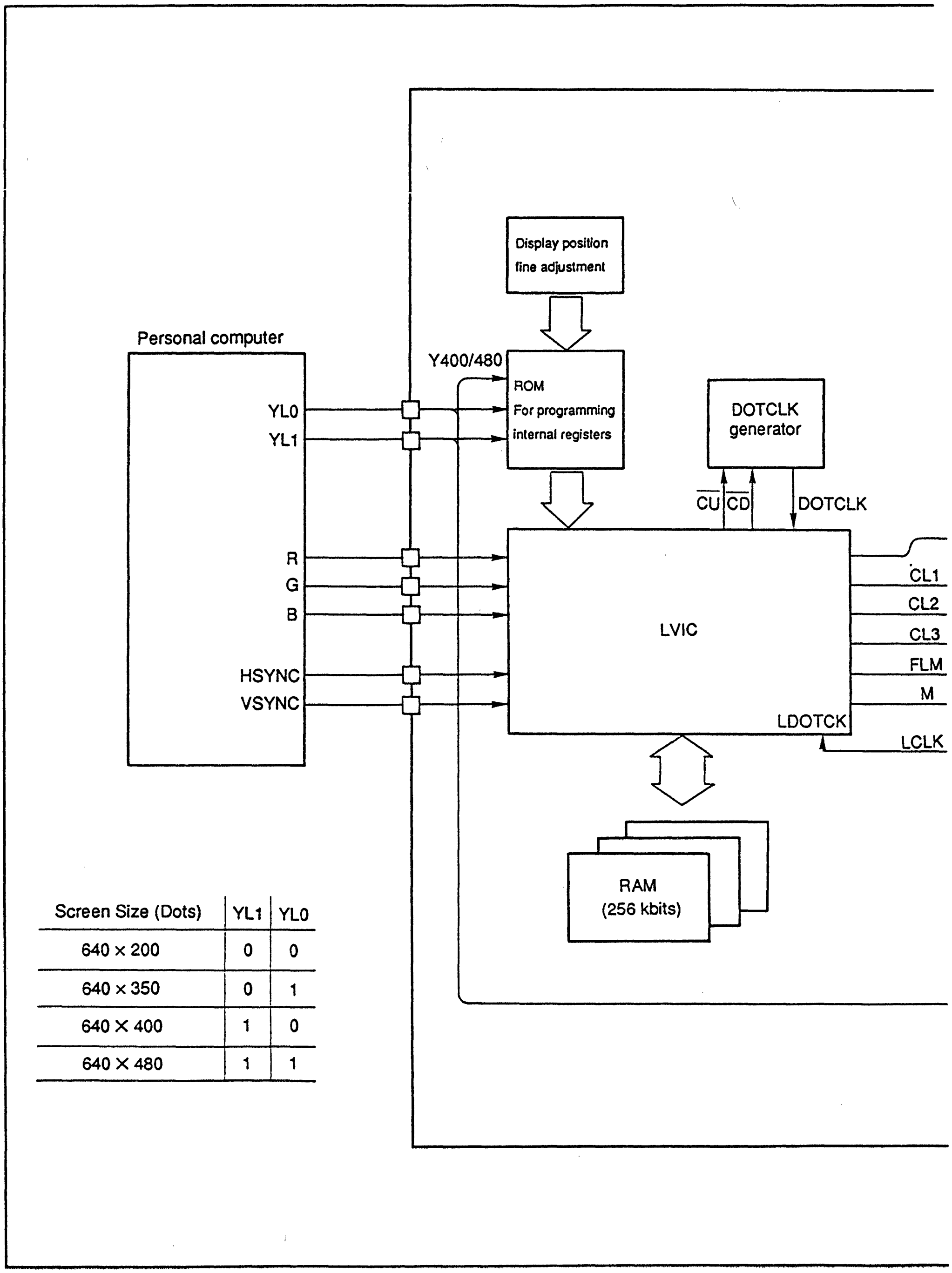


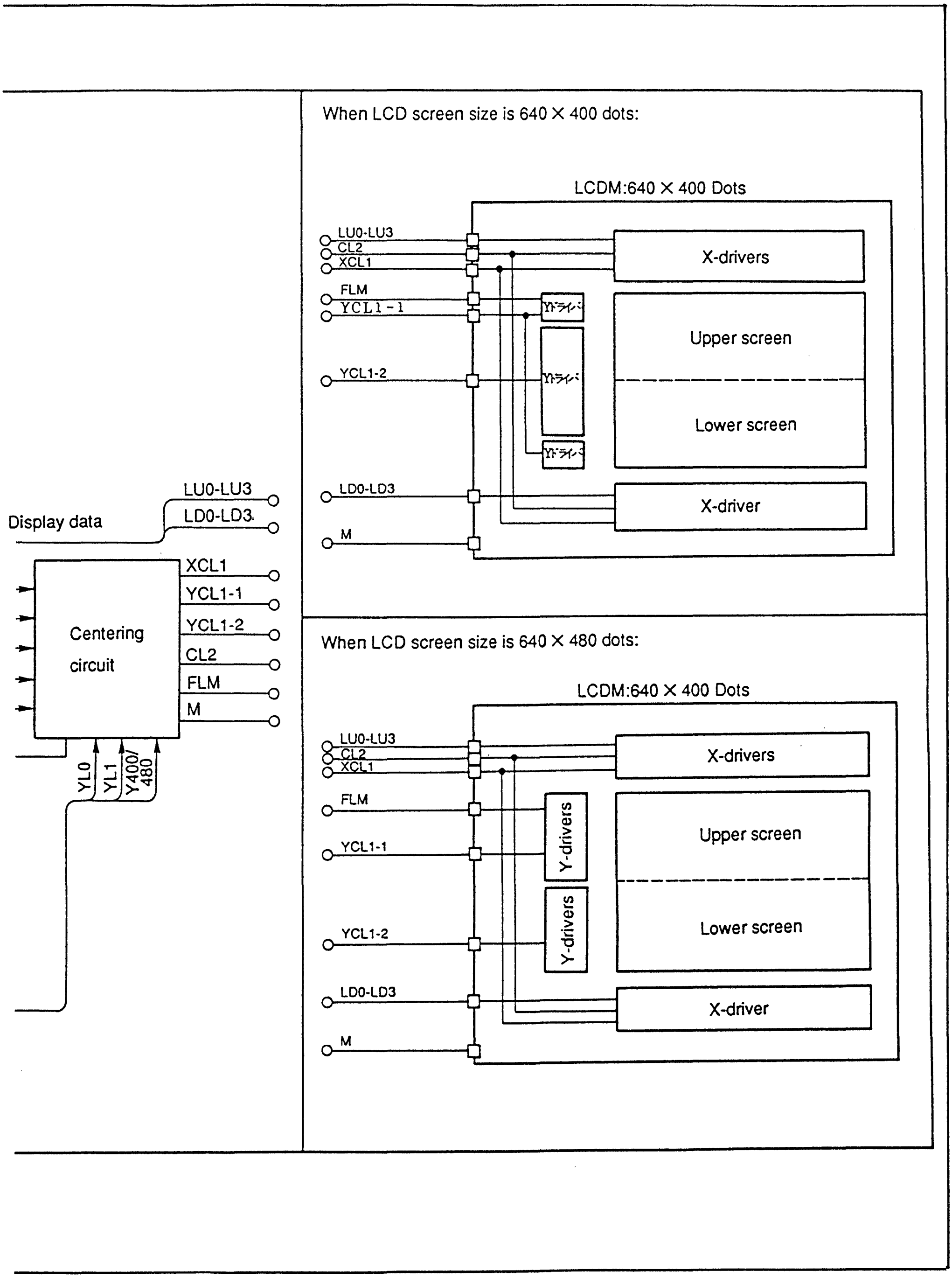
Figure 9-1 Centering Circuit

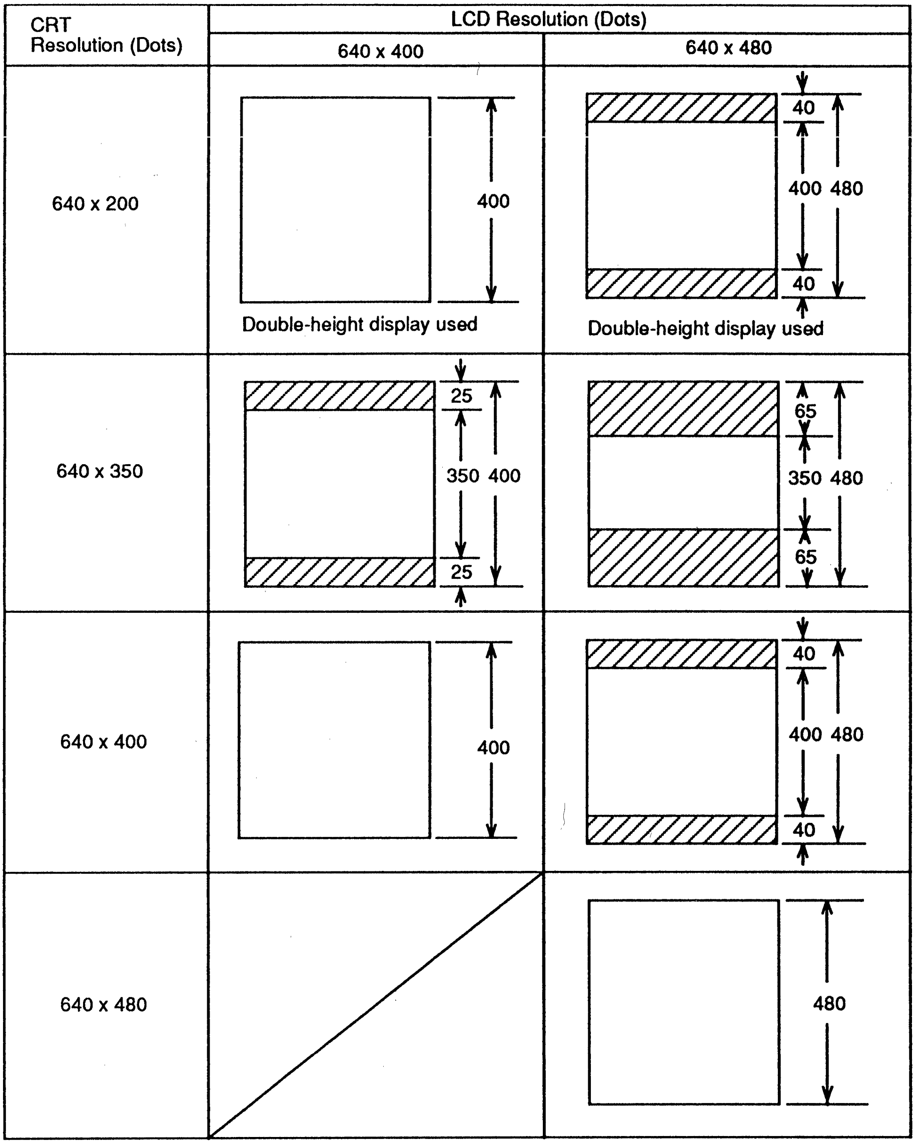

IC30
LS153
IC31
IS153
IC6
LS02
IC9 LS04
ICO
IC1
IC2
IC3
IY
IG
YL1
YL0
IC15
HC244
LCLK
XCL1
IC13 LS00
YCL1-1
IC14 LS00
YCL1-2
IC24
LS74
PR
D
CL
IC8 LS32
FCL1-1EN
FCL1-2EN
IC14
LS74
IC26
LS161
FCQA
QB
QC
QD
IC29
F521
FCQA
QB
QC
QD
QE
QF
QG
EQ
EN
IC3
LS04
IC6
LS02
FCL 1EN
IC27
LS161
FCQE
QF
QG
M00-02
M00-02
M00-02
M11
M11
M00-02
M01
IC10 LS00
IC11
LS10
IC3
LS04
M01
M00-02
M11
IC25 LS86
IC18
LS20
M01-11
M00-01-029
FCLIR-N



Screen Size (Dots)	YL1	YL0
640 × 200	0	0
640 × 350	0	1
640 X 400	1	0
640 X 480	1	1

Figure 9-2 System Configuration Incorporating Centering Circuit


When LCD screen size is 640 × 400 dots:
LCDM:640 × 400 Dots
LU0-LU3
CL2
XCL1
FLM
YCL1-1
YCL1-2
LD0-LD3
M
X-drivers
Yドライバ
Yドライバ
Yドライバ
Upper screen
Lower screen
X-driver
Display data
LU0-LU3
LD0-LD3
XCL1
YCL1-1
YCL1-2
CL2
FLM
M
Centering circuit
YL0
YL1
Y400/480
When LCD screen size is 640 × 480 dots:
LCDM:640 × 400 Dots
LU0-LU3
CL2
XCL1
FLM
YCL1-1
YCL1-2
LD0-LD3
M
X-drivers
Y-drivers
Y-drivers
Upper screen
Lower screen
X-driver



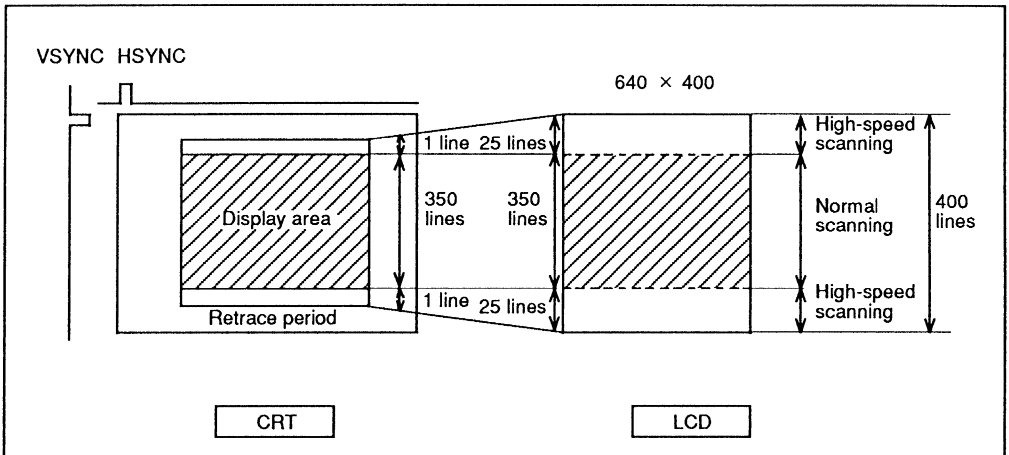
Note: ▨ indicates blank areas.

Figure 9-3 Centering Display

9.1.1 Operation

Figure 9-4 is a conceptual diagram illustrating how the centering circuit shown in figure 9-1 operates. As shown in the figure, the LVIC outputs the same number of high-speed CL1 signal pulses to the Y-drivers as the number of specified during the retrace period of one CRT display line. This shifts the display start position. In this case, the data for the retrace period is scanned so rapidly that the contrast is very low.

If the CRT display screen's size is 640 × 200 dots, double-height display is used in parallel.



Note : In high-speed scanning, a CL1 signal with a frequency of about a hundred times that of the normal CL1 signal is used to rapidly shift the lines being selected .

Figure 9-4 Conceptual Diagram of Centering Operation

9.1.2 Values in Internal Registers

Table 9-1 lists the values to be set in the internal registers for different CRT display screen sizes and LCD screen sizes when display centering is used. Refer to tables 8-4 to 8-8 for other values.

Table 9-1 Values in Internal Registers for Centering Display

LCD Resolution (Dots)	CRT Display Resolution (Dots)	Value in: Vertical Displayed Lines Register	Value in: Vertical Back Porch Register
640 × 400	640 × 200(Note)	Normal value (= 199)	Normal value
	640 × 350	Normal value + 2 (= 351)	Normal value – 1
	640 × 400	Normal value (= 399)	Normal value
640 × 480	640 × 200(Note)	Normal value + 2 (= 201)	Normal value – 1
	640 × 350	Normal value + 2 (= 351)	Normal value – 1
	640 × 400	Normal value + 2 (= 401)	Normal value – 1
	640 × 480	Normal value (= 479)	Normal value

Normal value: Value in the internal registers when display is not centered

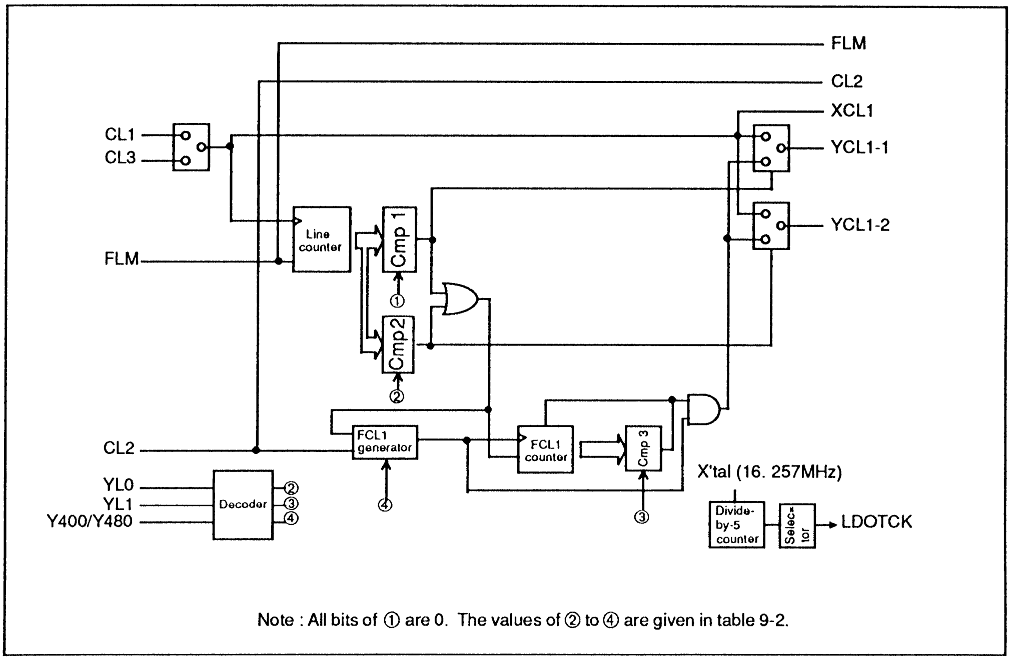
Note: Double-height display used

9.1.3 Centering Circuit

Figure 9-5 is the block diagram of a centering circuit. The line counter counts the number of displayed lines and is reset by the FLM signal. Comparators 1 and 2 compare the signal output from this counter with outputs ① and ②, respectively.

The signal output from comparator 1 goes high at the first display line, which activates the FCL1 counter and makes the FCL1 generator output a signal through the AND gate. When the signal output from the FCL1 counter matches output ③, comparator 3 outputs a low-level pulse which stops the FCL1 counter. This fixes the output signal from comparator 3 low and stops the FCL1 signal. Comparator 1 then outputs a low-level pulse to reset the FCL1 counter. The logical AND of the FCL1 signal and comparator 1's signal output through the AND gate generates the CL1 signal for scanning the upper lines at high-speed.

Next, the signal output from comparator 2 goes high at the specified line which activates the FCL1 counter. To generate the high-speed CL1 signal for the lower lines, the centering circuit subsequently operates in the same way as when it is generating the high-speed CL1 signal for the upper lines.



Note : All bits of ① are 0. The values of ② to ④ are given in table 9-2.

Figure 9-5 Centering Circuit Block Diagram

Table 9-2 Values ② – ④ of Centering Circuit

LCD Panel Size (Dots)	**Display Screen Size (Dots)**	**Value of** ②	③	④
640 × 400	640 × 200	– (Output of Comparator 2 fixed low)	Don't care	Don't care
	640 × 350	10101111	00100100	00000101
	640 × 400	– (Output of comparator 2 Fixed low)	Don't care	Don't care
640 × 480	640 × 200	01100100	00111001	00000011
	640 × 350	10101111	01100100	00000001
	640 × 400	11001000	00111001	00000011
	640 × 480	– (Output of comparator 2 Fixed low)	Don't care	Don't care

Figure 9-6 is the timing chart of the operations described above.

Table 9-3 lists the frequencies of the LCD frame (FLM signal) and other signals in this circuit. Change the LCD dot clock (LDOTCK) frequency when changing the frame frequency.

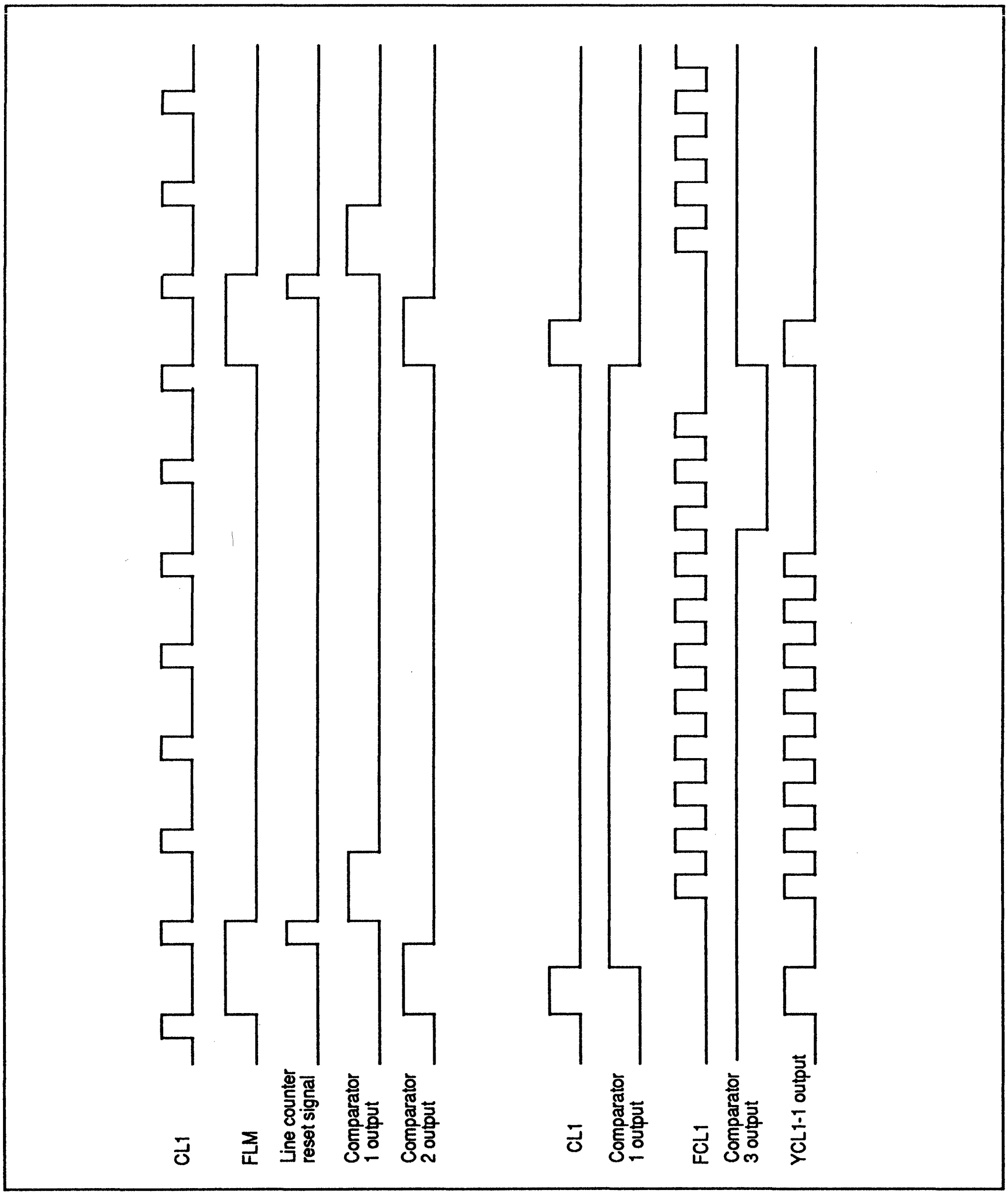


Figure 9-6 High-Speed CL1 Signal Output Timing

Table 9-3 LCD Signal Specifications

LCD Resolution (Dots)	CRT Display Resolution (Dots)	f_{DOTCLK} (MHz)	f_{LDOTCK} (MHz)	f_{CL1} (kHz)	f_{HCL1} (kHz)	Multiplexing Duty Ratio	f_{FLM} (Hz)	$\frac{f_{LDOTCK}}{f_{HCL1}}$
640 × 400	640 × 200	14.318	8.129	6.1	—	1/200	61	—
	640 × 350	16.257	16.257	12.2	339	1/176	69	48
	640 × 400	16.257	16.257	12.2	—	1/200	61	—
640 × 480	640 × 200	14.318	8.129	6.1	254	1/202	60	32
	640 × 350	16.257	16.257	12.2	1020	1/176	69	16
	640 × 400	16.257	16.257	12.2	508	1/201	61	32
	640 × 480	25.0	20.32	15.3	—	1/240	64	—

f_{DOTCLK}: CRT display dot clock (DOTCLK) frequency

f_{LDOTCK}: LCD dot clock (LDOTCK) frequency

f_{CL1}: CL1 signal frequency

f_{HCL1}: High-speed CL1 signal frequency

f_{FLM}: LCD frame frequency (FLM signal frequency)

9.2 Centering Display Horizontally (Without External Circuit)

Adjusting the horizontal back porch value (in the horizontal back porch register (R14 and R15)) enables horizontal centering of a display without an external circuit.

For example, to display a CRT screen of 480 × 200 dots at the center of an LCD panel of 640 × 200 dots, subtract 80 from the normal horizontal back porch value to advance the phase of the display timing signal (DISPTMG) by 80 dots (figure 9-7). Specify 60 characters (480 dots) instead of 80 characters (640 dots) as the number of horizontal displayed characters in this case.

Note that horizontal centering is available only when the CRT retrace period is larger than the difference between the horizontal sizes (dots) of the LCD panel and CRT screen. This means, for example, that the retrace period must be at least 160 dots to display a CRT screen of 480 × 200 dots at the center of an LCD panel of 640 × 200 dots.

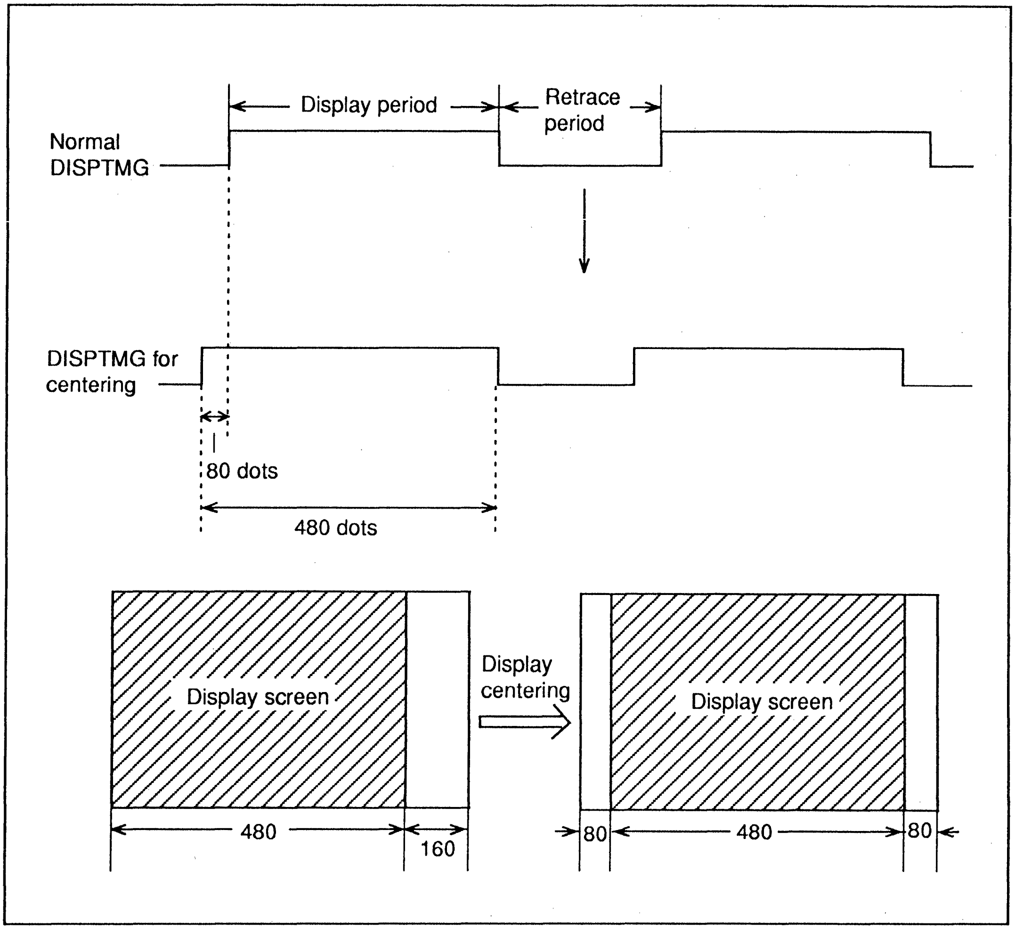


Figure 9-7 Centering Display Horizontally

9.3 Changing Display Screen Size on the Same LCD Panel (Without External Circuit)

There are two methods of displaying a CRT screen that is smaller than the LCD panel being used. One is to display the screen at the center of the LCD panel as described in section 9.1, Centering Display Vertically, and section 9.2, Centering Display Horizontally. The other is to display the screen in the top or left part of the LCD panel without any centering. This latter method does not require an external circuit; all that is required is to change the setting of the LVIC's pins or internal registers to specify the screen size.

This section describes how to display CRT screens of different sizes on an LCD panel of 640 × 400 dots or 640 × 200 dots.

9.3.1 Changing Display Screen Size on an LCD Panel of 640 × 400 Dots

Displaying a CRT Screen of 640 × 350 Dots: To change a CRT display screen size of 640 × 400 dots to one of 640 × 350 dots, set the LVIC's pins or internal registers to 640 × 400 dots if the LCD panel has a dual screen configuration. Data corresponding to the bottom 50 lines of the panel may or may not be displayed, as follows:

- If the display timing signal (DISPTMG) is internally generated, the data for the retrace period of the screen of 640 × 400 dots is displayed.
- If the DISPTMG signal is externally supplied (and the memory clear function is used), no data is displayed.
- If the DISPTMG signal is externally supplied (and the memory clear function is not used): The data for the bottom 50 lines of the previous display screen (screen of 640 × 400 dots) is displayed.

If the LCD panel has a single screen configuration, a setting of either 640 × 400 dots or 640 × 350 dots is acceptable. If 640 × 350 dots is set, no data is displayed on the bottom 50 lines of the LCD panel. If 640 × 400 dots is set, the above conditions are valid.

Displaying a CRT Screen of 640 × 200 Dots: There are two methods of changing a CRT screen size of 640 × 400 dots into one of 640 × 200 dots. One is to use double-height display. Refer to section 4.2, How to Use Double-Height Display, for details. The other is to change the setting of the LVIC's pins or internal registers from 640 × 400 dots to 640 × 200 dots after selecting a display mode for single screen configuration with the DM3–DM0 pins, regardless of the actual LCD panel configuration. In this case, the correct screen appears on the top 200 lines of the LCD panel, but G data is displayed on the bottom 200 lines. Note that display is disabled if the LVIC setting is left at 640 × 400 dots, since the frequency of the LCD dot clock (LDOTCK) will be higher than that of the CRT display dot clock (DOTCLK).

9.3.2 Changing Display Screen Size on an LCD Panel of 640 × 200 Dots

It is not necessary to change the LVIC setting of 640 × 200 dots when changing a CRT screen size of 640 × 200 dots to one of 320 × 200 dots. However, this is possible only when the display timing signal (DISPTMG) is generated inside the LVIC and when the retrace period of the 640 × 200 dot CRT screen is at least 320 dots. The correct screen appears on the left half of the LCD panel in this case. Correct display is not possible when the retrace period is less than 320 dots or when the DISPTMG signal is externally supplied, since data does not appear in the correct position. If the LVIC setting is changed to 320 × 200 dots, the correct screen appears on the left half of the LCD panel, but undefined data appears on the right half of the LCD panel.

To display a CRT screen of 320 × 200 dots on an LCD panel of 640 × 200 dots, the horizontal dimension can be doubled. Double the frequency of the CRT dot clock (DOTCLK) to ensure that the DOTCLK signal satisfies the LVIC's AC characteristics. In addition, set the LVIC to 640 × 200 dots, not 320 × 200 dots.

In principle, since the back porch and the dot clock frequency depend on CRT display mode (screen size, graphics/character mode), the setting of the LVIC's pins and internal registers will need to be changed.

9.4 4-Level Gray Scale Display (With External Circuit)

The number of gray scale levels can be reduced if it is felt that the contrast provided by the 8-level gray scale display is insufficient. Decoding the CRT RGB display data enables a reduction in the number of levels. Figure 9-8 shows a decoder realizing a 4-level gray scale display. The color arrangement given in table 9-4 can be provided by changing the inputs to the decoder. Change the inputs according to the software being used, to obtain a better display.

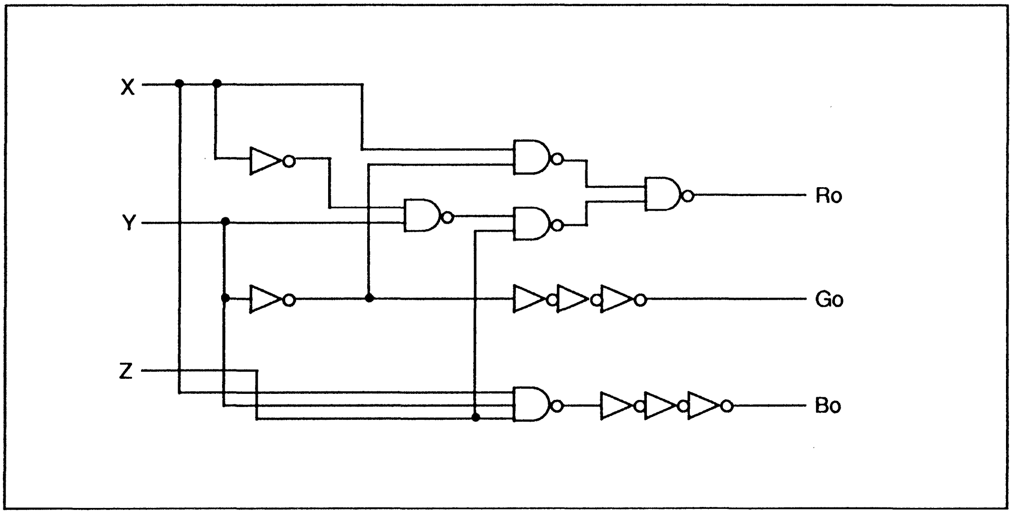


Figure 9-8 4-Level Gray Scale Display Circuit (Decoder)

Table 9-4 4-Level Gray Scale Display (Color Arrangement)

Input	Before Decoding	After Decoding
(X, Y, Z)	White	White
= (R, G, B)	Yellow, cyan, green	Green
or (B, G, R)	Magenta, red, blue	Red
	Black	Black
(X, Y, Z)	White	White
= (R, B, G)	Yellow, green, blue	Green
or (G, B, R)	Cyan, magenta, red	Red
	Black	Black
(X, Y, Z)	White	White
= (G, R, B)	Yellow, magenta, red	Green
or (B, R, G)	Cyan, green, blue	Red
	Black	Black

Note: (R, G, B) indicates the arrangement of the CRT RGB display data. (X, Y, Z) = (R, G, B) means that the R, G, and B signals are to be input to the X, Y, and Z lines in figure 9-8.

9.5 Pseudo-SRAM Interface (With External Circuit)

The LVIC was designed to be used with normal SRAMs acting as buffer memory. However, pseudo-SRAMs can be used if an external circuit is provided. This section describes the interface between the LVIC and the HM65256B 32-kbyte pseudo-SRAM.

9.5.1 Interface

Interface Signals: When pseudo-SRAMs are used as buffer memory, data can be read from memory, but it cannot be written to memory with the existing memory chip select signal ($\overline{\text{MCS}}$). Moreover, the LVIC cannot refresh memory, which is essential for pseudo-SRAMs. Therefore, when the LVIC is connected to pseudo-SRAMs, a memory chip enable signal ($\overline{\text{CE}}$) and a memory output enable signal ($\overline{\text{OE}}$) must be generated by an external circuit. The $\overline{\text{CE}}$ signal generates the memory chip enable precharge time and the $\overline{\text{OE}}$ signal generates the memory refresh precharge time.

Table 9-5 gives a comparison between the interface signals required for SRAMs and those required for pseudo-SRAMs.

Table 9-5 Comparison of Buffer Memory Interface Signals (SRAMs vs. Pseudo-SRAMs)

SRAM Interface Signals	Pseudo-SRAM Interface Signals
Memory chip select signal ($\overline{\text{MCS}}$)	Memory chip select signal ($\overline{\text{MCS}}$)
Memory write enable signal ($\overline{\text{MWE}}$)	Memory chip enable signal ($\overline{\text{CE}}$)
Memory addresses (MA)	Memory output enable signal ($\overline{\text{OE}}$)
Display data (RD, GD, BD)	Memory write enable signal ($\overline{\text{MWE}}$)
	Memory addresses (MA)
	Display data (RD, GD, BD)

Note: Of the pseudo-SRAM interface signals, the $\overline{\text{MCS}}$ signal is necessary only when a memory plane has more than one memory.

Connection to Pseudo-SRAMs: Figure 9-9 shows an example of connection between the LVIC and two HM65256Bs, and figure 9-10 shows an example of a $\overline{\text{CE}}$ and $\overline{\text{OE}}$ signal generator.

Figure 9-11 is the operation timing chart for the $\overline{\text{CE}}$ and $\overline{\text{OE}}$ signal generator. The $\overline{\text{CE}}$ signal shown in the figure enables data to be read from memory during read cycles 1 and 2 and data to be written to memory during a write cycle. The $\overline{\text{CE}}$ and $\overline{\text{OE}}$ signals enable memory to be refreshed up to eight times per line during the CRT horizontal retrace period (figure 9-12).

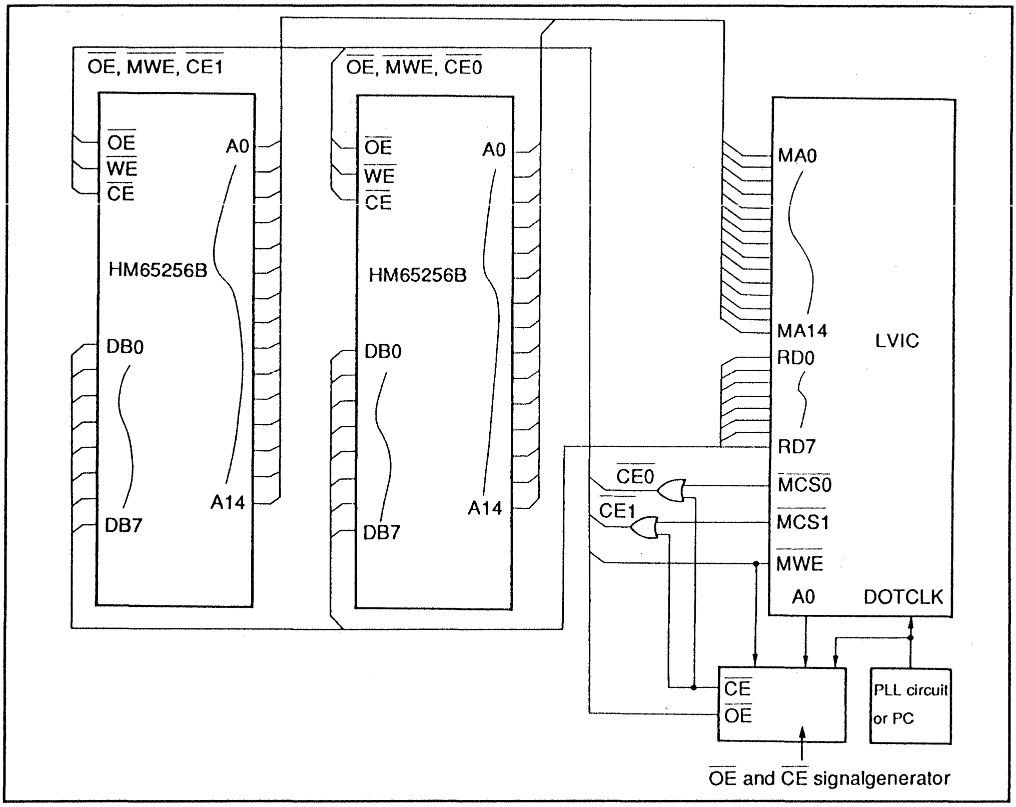
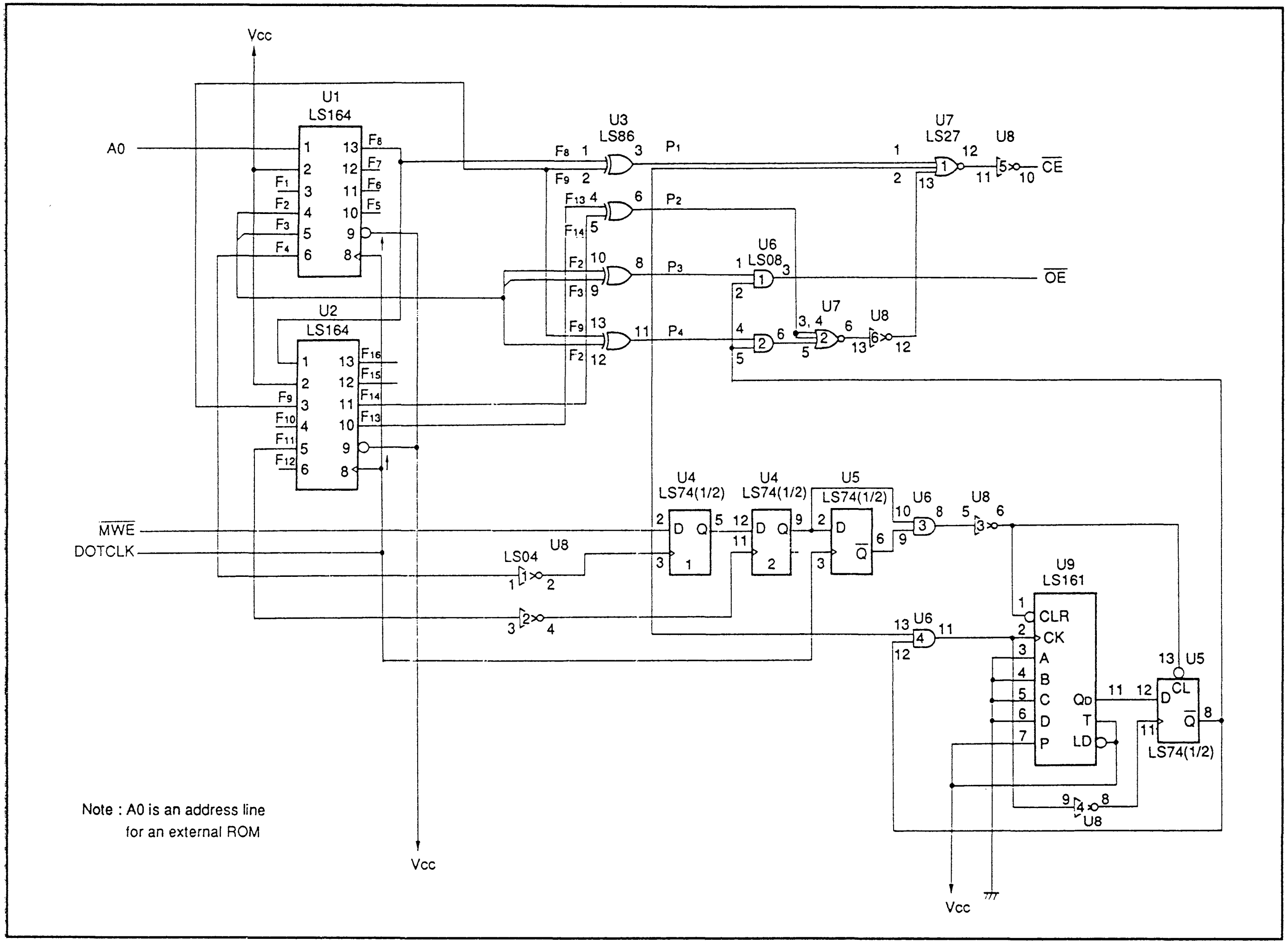


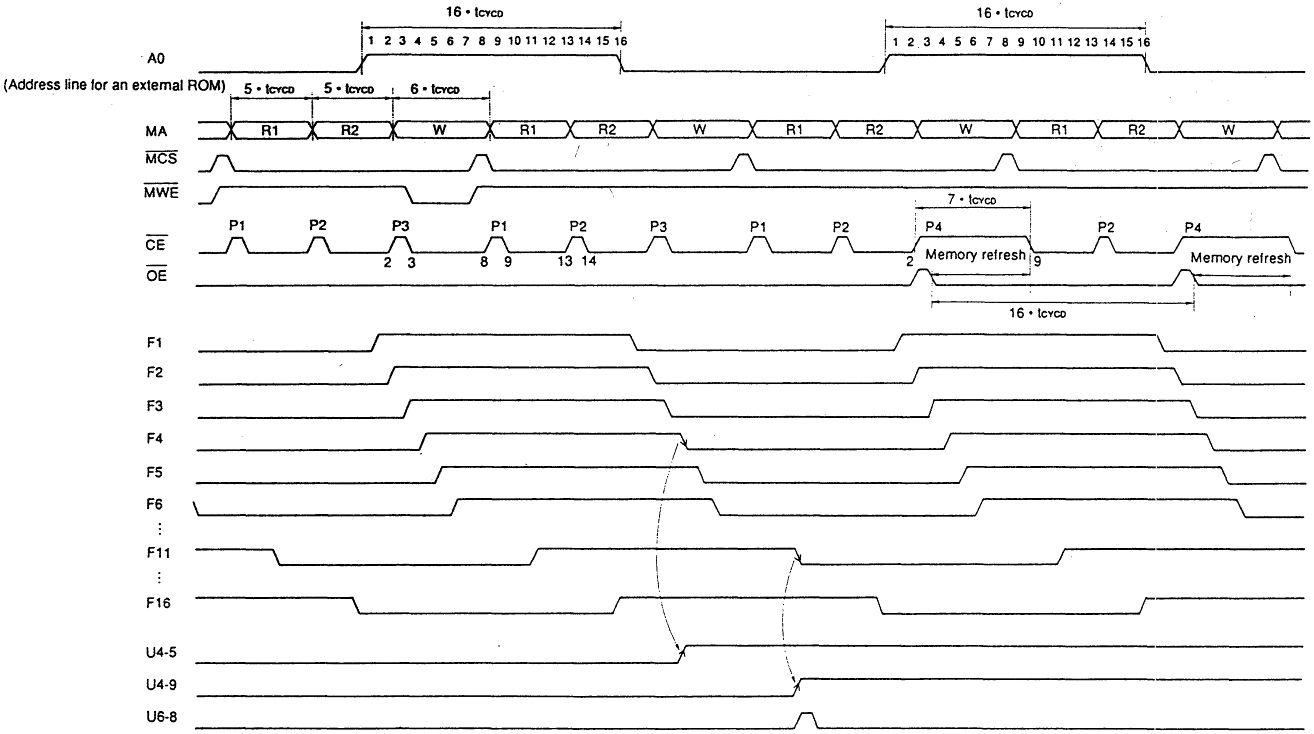
Figure 9-9 Example of Connection between LVIC and HM65256Bs



Note : A0 is an address line
for an external ROM

Figure 9-10 $\overline{CE}$ and $\overline{OE}$ Signal Generator

HITACHI



tCYCD : Dot clock cycle time

R1, R2: Read cycle 1, 2

W: Write cycle

Note: F1–F16 and P1–P4 are names of signals within the circuit, and U4-5 and U6-8 are units' names and their pin numbers (figure 9-10).

Figure 9-11 Operation Timing of $\overline{CE}$ and $\overline{OE}$ Signal Generator

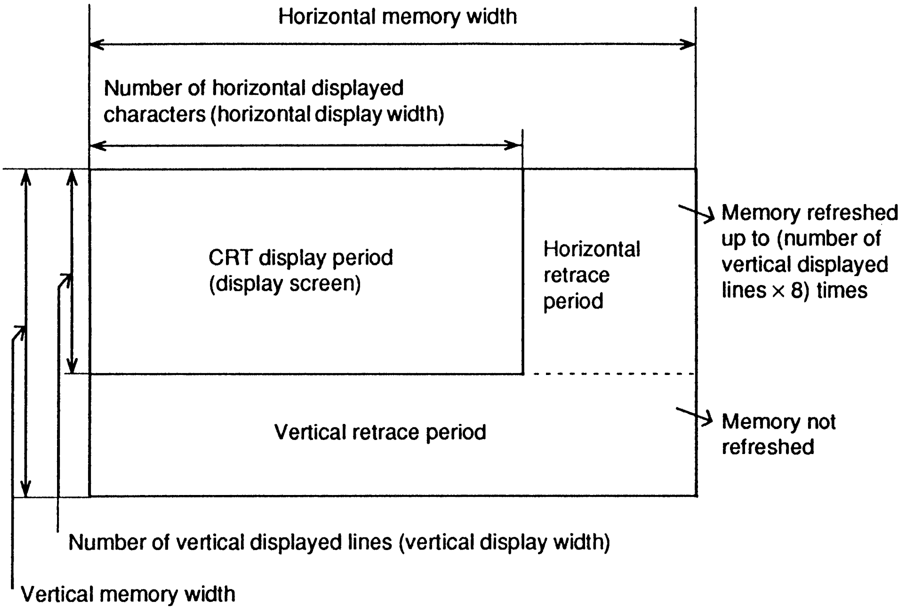

Horizontal memory width
Number of horizontal displayed characters (horizontal display width)
CRT display period (display screen)
Horizontal retrace period
Memory refreshed up to (number of vertical displayed lines × 8) times
Vertical retrace period
Memory not refreshed
Number of vertical displayed lines (vertical display width)
Vertical memory width

Figure 9-12 Memory Width and Memory Refresh Period

9.5.2 Limitations on Use

The following limitations hold when pseudo-SRAMs are used as buffer memory:

Limitations on LVIC Control Method: SRAMs can be used only with the ROM programming method since pin A0, the address for an external ROM, is necessary to generate the interface signals $\overline{CE}$ and $\overline{OE}$.

Limitations on Memories Used: As far as memory access time and write data setup time are concerned, the limitations are the same as those on normal SRAMs. (Refer to section 2.3.1, Memory Type and Memory Capacity Calculations, for details.) In addition, only memories satisfying the following three conditions can be used:

- Memory all-refresh cycle time $\geqq$ CRT vertical retrace period .... (9-1)

  CRT vertical retrace period = $1/f_{VSYNC}$ – (number of vertical displayed lines)/f_{HSYNC} .... (9-2)

  f_{VSYNC}: VSYNC signal frequency

  f_{HSYNC}: HSYNC signal frequency

  This condition is necessary because memory is not refreshed during the CRT vertical retrace period. The all-refresh cycle time is the maximum time required for refreshing all addresses of memory.

- (Memory refresh command delay time) + (refresh cycle time) $\leqq 7 \cdot t_{CYCD}$ .... (9-3)

  (See figure 9-13.)

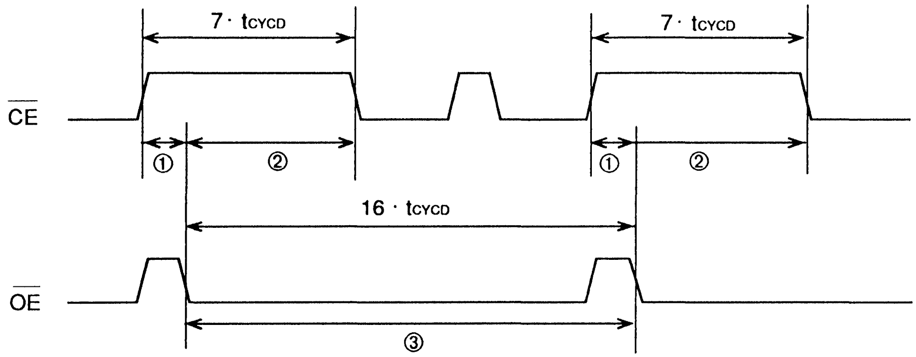
  t_{CYCD}: Dot clock cycle time

- Time between memory refreshes $\geqq 16 \cdot t_{CYCD}$ .... (9-4)

  Time between memory refreshes = (number of memory word lines) / (all-refresh cycle time) .... (9-5)

  (See figure 9-13.)

  t_{CYCD}: Dot clock cycle time



t_{CYCD} : Dot clock cycle time

① : Refresh command delay time

② : Refresh cycle time

③ : Time between refreshes

Figure 9-13 Pseudo-SRAM Refresh Timing

APPENDIXES

A. Malfunctions Caused by Rewriting Registers During Display

Rewriting the contents of an internal register during display may cause the LSI to malfunction. However, malfunctions usually appear only in the frame corresponding to the rewrite; the LSI will function normally in subsequent frames.

Table A-1 lists possible malfunctions by internal registers (or bits), and how to avoid them.

Table A-1 Malfunctions Caused by Rewriting Registers During Display, and Countermeasures

Reg. No.	Register Name	Bits	Malfunctions and Countermeasures	Rewritable?(Note)
R0	Control Register 1	DCK	Display will be jumbled until the oscillation frequency of the external PLL circuit stabilizes	No
		DSP	Display data will appear in the wrong position if the register is rewritten during the horizontal back porch period	Conditional
R1	Control Register 2	MS0, 1	The chip select signal and memory address output will be irregular	No
		DON	No malfunction	Yes
		MC	No malfunction	Yes
R2 | R4	Vertical Displayed Lines Register		Invalid data may appear or the display may flicker if the register is rewritten during the last line of a frame while data is transferred between the LSI and buffer memory	No
R4 R5	CL3 Period Register		In display modes 13–16, the CL3 signal period may become longer than that specified by the register	No
R6 R7	Horizontal Displayed Characters Register		Display data may appear in the wrong position or the display may flicker	No

Note: Yes means that the register can be rewritten without affecting the display, no means that malfunction cannot be prevented or countermeasures are difficult, and conditional means that the register can be rewritten only under certain conditions.

Table A-1 Malfunctions Caused by Rewriting Registers During Display, and Countermeasures (cont.)

Reg. No.	Register Name	Bits	Malfunctions and Countermeasures	Rewritable?(Note)
R8	CL3 Pulse Width Register		The CL3 signal period may become longer than that specified by the register	No
R9	Fine Adjust Register		Display data may appear in the wrong position: rewrite this register during the CRT retrace period	Conditional
R10 R11	PLL Frequency-Division Register		Display will be jumbled until the oscillation frequency of the external PLL circuit stabilizes	No
R12 | R15	Vertical and Horizontal Back Porch Registers		Display may flicker: rewrite these registers during the CRT display period	Conditional

Note: Yes means that the register can be rewritten without affecting the display, no means that malfunction cannot be prevented or countermeasures are difficult, and conditional means that the register can be rewritten only under certain conditions.

B. Reset

The $\overline{\text{RES}}$ pin resets and starts the LVIC. Make sure that the reset signal is held low for at least 1 µs after power-on.

Reset is defined as shown in figure B-1.

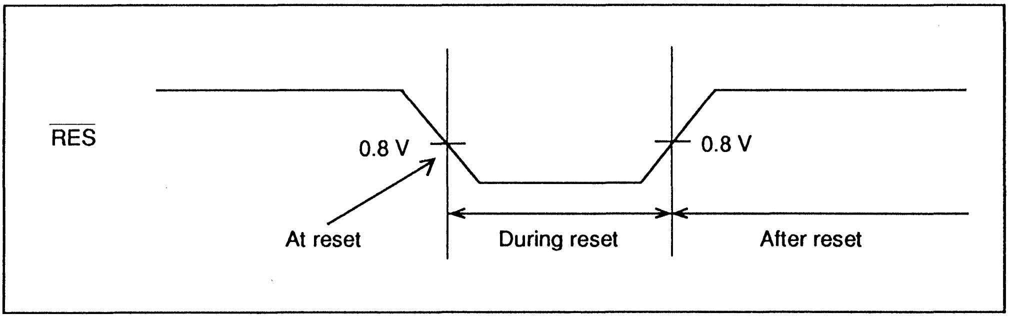


Figure B-1 Reset Definition

B.1 Status of Pins During Reset

In principle, the $\overline{\text{RES}}$ pin does not control output pins; it operates regardless of the other input pins. Output pins can be classified into the following five groups, depending on their reset status:

- Pin that maintains its pre-reset status: CL2
- Pins that are driven to high-impedance status (fixed low in through mode): RD0–RD7, GD0–GD7, BD0–BD7
- Pins that are fixed high: $\overline{\text{MWE}}$, CL4, M, $\overline{\text{CD}}$, $\overline{\text{MCS1}}$
- Pins that are fixed low: MA0–MA12, R0–R3, G0–G3, B0–B3, CL1, CL3, FLM, A0–A3, $\overline{\text{CU}}$
- Pins that are fixed high or low, depending on the type of memory being used (see table B-1): MA13–MA15, $\overline{\text{MCS0}}$

Table B-1 Memory Type and Status of Pins During Reset

Memory Type	MA13	MA14	MA15	$\overline{\text{MCS0}}$
No Memory (Through Mode)	Low	Low	High	High
8-kbyte Memory	High	High	High	Low
32-kbyte Memory	Low	Low	High	Low
64-kbyte Memory	Low	Low	Low	Low

B.2 Status of Registers During Reset

The $\overline{\text{RES}}$ pin does not affect register contents. Therefore, registers can be both read from and written to by an MPU even during reset. The registers keep their pre-reset contents until they are rewritten.

B.3 Buffer Memory Clear Function

After it is reset, the LVIC writes 0s into the memory area specified by the MS0 and MS1 pins or the MS0 and MS1 bits of control register 2 (R1). Refer to table 5-1 in section 5, Buffer Memory Clear Function, for details.

C. Programming Restrictions

Values written into the LVIC's internal registers have the restrictions listed in table C-1. The symbols in table C-1 are defined in table C-2 and figure C-1.

Table C-1 Limits of Values Written into Registers

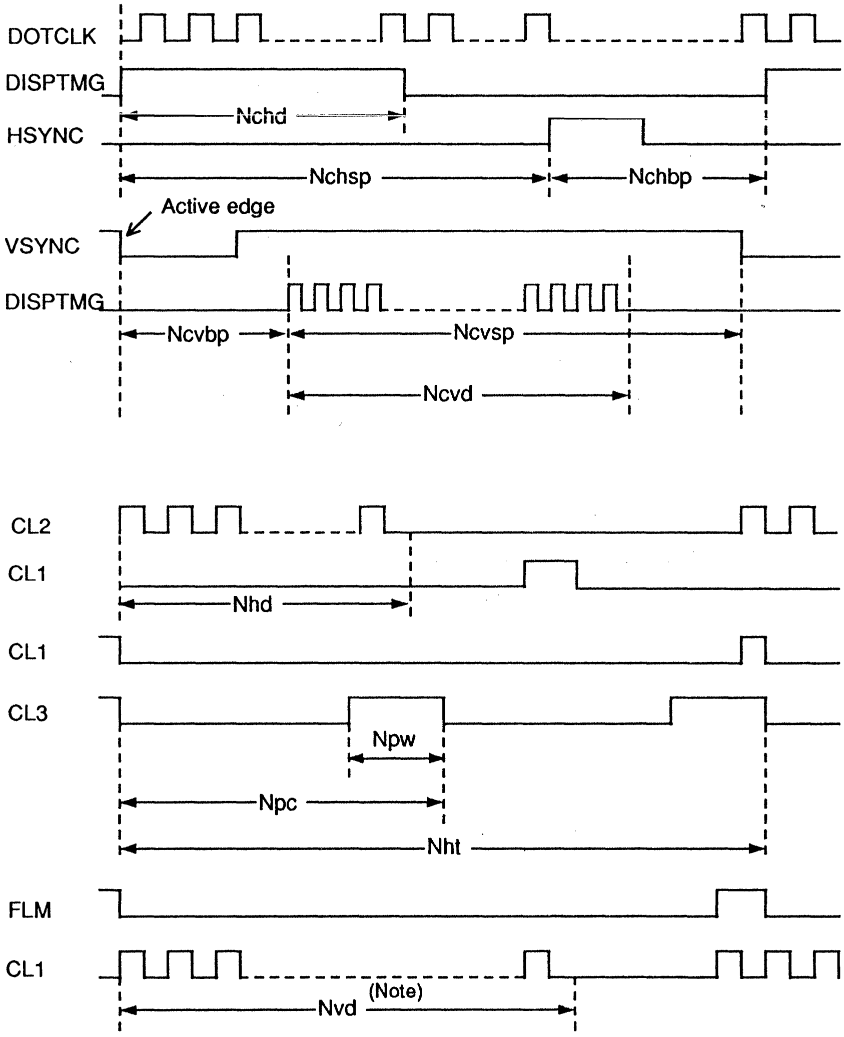
Item	Limits	Notes	Applicable Registers
Screen Configuration	$4 \leqq Nvd \leqq (Ncvbp + Ncvsp) - 1 \leqq 1024$		R2, R3, R4, R6, R7
	$4 \leqq Nhd \leqq (Nchbp \times 1/n + Nchsp) - 1 \leqq 506$	1, 2	
	$(Nhd + 6) \times n \times Nvd \times f_{FLM} \leqq f_{DOTCLK} \leqq 30\ \mathrm{MHz}$	1, 3	
CL3 Signal Control	$1 \leqq Npw \leqq (Nhd + 6)/2 - 1$	4	R4, R5, R6, R7, R8
	$1 \leqq Npw \leqq Nhd$	5	
	$1 \leqq Npw \leqq Npc - 1$	6	
DISPTMG Signal Generation	$1 \leqq Nchbp \leqq 256$	7	R12, R13
	$1 \leqq Ncvbp \leqq 256$	7	R14, R15
No Memory (Through Mode)	$4 \leqq Nhd \leqq Nchsp - 4$	8	R2, R3, R4, R6, R7
	$4 \leqq Nvd \leqq Ncvsp - 1$	8	

Notes:

1. n indicates the horizontal character pitch which is the number of horizontal dots making up one character.
2. $Nhd \leqq 250$ in dual screen modes (display modes 1 and 6).
3. f_{FLM} is the FLM signal frequency and f_{DOTCLK} is the CRT display dot clock (DOTCLK) frequency.
   $f_{LDOTCK} < f_{DOTCLK} \times 15/16$ or $f_{LDOTCK} = f_{DOTCLK}$
   (f_{LDOTCK} is the LCD dot clock (LDOTCK) frequency)
4. In display modes 1, 2, 4, and 6–8
5. In display modes 3, 5, and 9–12 where Npw = (value in R8) + 5
6. In display modes 13–16 where Npw = (value in R8) + 5
7. (Value in R14 and R15) $\leqq (Nchsp \times n + Nchbp) - Nhd \times n - 2$
   (n = horizontal character pitch)
   (Value in R12, R13) $\leqq (Ncvsp \times n + Ncvbp) - Nvd - 2$
8. $Nht = Nchsp + (Nchbp \times 1/n)$, $Nvd < Ncvbp + Ncvsp$
   ($Nht = (Nhd + 6)$ when buffer memory is used)
   (n = horizontal character pitch)

Table C-2 Symbol Definitions

Symbol	Definition
Nchd	Number of horizontal displayed characters on CRT display ((number of horizontal displayed dots on CRT display) × 1/8)
Nchsp	Number of characters between the rising edge of the DISPTMG signal and that of the HSYNC signal ((number of dots between the rising edge of the DISPTMG signal and that of the HSYNC signal) × 1/8) (= horizontal synch position)
Nchbp	Number of dots between the rising edge of the HSYNC signal and that of the DISPTMG signal (just after the rising edge of the HSYNC signal) (= horizontal back porch)
Ncvbp	Number of lines between the active edge of the VSYNC signal and the rising edge of the DISPTMG signal (just after the active edge of the VSYNC signal) (= vertical back porch)
Ncvsp	Number of dots between the rising edge of the DISPTMG signal and the active edge of the VSYNC signal (= vertical synch position)
Ncvd	Number of vertical displayed lines on CRT display
Nhd	Number of horizontal displayed characters on LCD ((number of horizontal displayed dots) × 1/8)
Npc	Number of characters during a CL3 signal period ((number of dots during a CL3 signal period) × 1/8)
Npw	Number of characters while the CL3 signal is high ((number of dots while the CL3 signal is high) × 1/8)
Nht	Number of characters during a CL1 signal period ((number of dots during a CL1 signal period) × 1/8)
Nvd	Number of vertical displayed lines on LCD



Note: When the screen is dual, the Nvd period is doubled.

D. Limitations of Gray Scale Display

With gray scale display, the display contrast may be weak or the display may "flow."

D.1 Weak Display Contrast

When gray scales are displayed, the contrast of a section below a gray section is sometimes weakened, as shown in figure D-1. This phenomenon depends on the gray scale and on the display pattern (character, figure, or table), and is most noticeable when a gray scale is at the top of the screen or when it is used as part of a table (figure D-2). This phenomenon becomes even more noticeable if the LCD panel has strong contrast frequency characteristics or if the LCD module has a high resistance between its liquid-crystal cells and the power supply driving the LCD (such as an operational amplifier).

If this phenomenon appears, change the LCD panel or reduce the resistance between the liquid-crystal cells and the power supply driving the LCD.

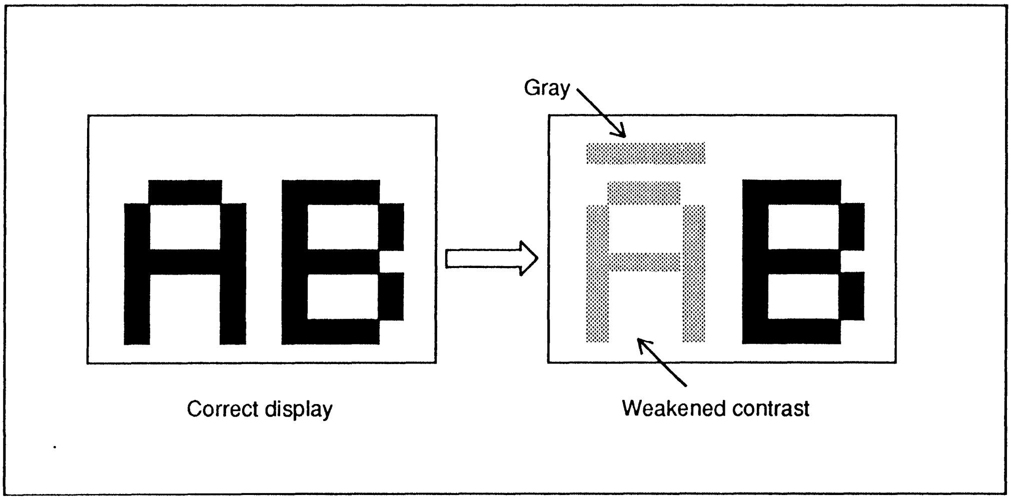


Figure D-1 Example of Figure Contrast Weakened by Gray Scale Display

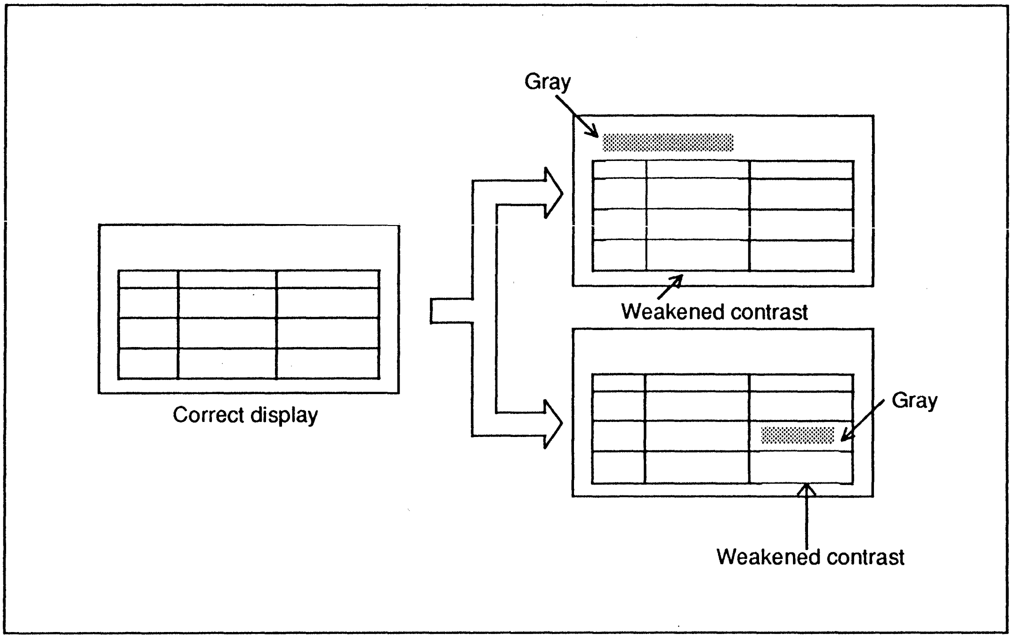


Figure D-2 Example of Table Contrast Weakened by Gray Scale Display

D.2 Display Flow

When gray scales are displayed on an LCD panel that has a quick response, a display pattern expressed by gray scales may look like it is flowing. A "flowing" display pattern means that the display-off lines visibly move in each frame as shown in figure D-3. This phenomenon does not depend on the display pattern, but it does depend on the gray scale. It may appear with only one or two of six gray scales in some cases, but with all of them in other cases. Conversely, it could be completely absent.

If this phenomenon appears, use an LCD panel with a slower response.

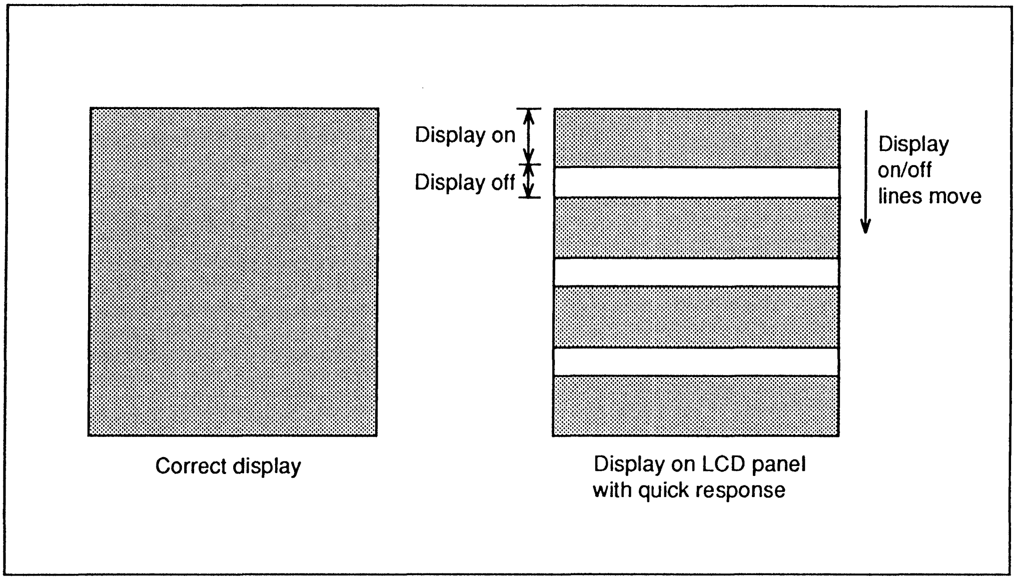


Figure D-3 Example of Display Pattern Flow with Gray Scales

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Section Four

HD63645F/ HD64645F LCD Timing Controller (LCTC) Application Note

Section Four

HD63645F/
HD64645F
LCD Timing
Controller (LCTC)
Application Note

For additional information reference:

Section 1. LCD Controller/Driver LSI Data Book
Section 2. HD66300T Horizontal Driver for TFT-Type LCD Color TV
Section 3. HD66840 Video Interface Controller (LVIC) Application Note
Section 5. HD63645/HD64645/HD64646 LCD Timing Controller (LCTC) User's Manual

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Tables

1. DISPLAY SCREEN AND VALUES IN REGISTERS

This chapter is an overview to help understanding of the following chapters. Refer to LCD Timing Controller(LCTC) HD63645F, HD64645F User's Manual for more details, especialy on software of each function.

1.1 Internal Registers

The LCTC has one address register and fourteen data registers (table 1-1). To select one out of the fourteen data registers, write the address of the data register to be selected into the address register (table 1-2). The MPU can transfer data to/from the data register corresponding to the written address.

Table 1-1 Internal Register Configuration

Register Name	Symbol	Data Bit							
		7	6	5	4	3	2	1	0
Address Register	-	▨	▨	▨					
Horizontal total characters *2	Nht								
Horizontal displayed characters	Nhd								
Maximum raster address	Nr	▨	▨	▨					
Cursor start raster	Ncs	▨	B	P					
Cursor end raster	Nce	▨	▨	▨					
Start address (H)	-								
Start address (L)	-								
Cursor address (H)	-								
Cursor address (L)	-								
Horizontal virtual screen width	Nir								
Multiplexing duty ratio (H)	Ndh	▨	▨	▨	▨	▨	▨	▨	
Multiplexing duty ratio (L) *2	Ndl								
Display start register	Nsr	▨	▨	▨					
Mode register *4	-	▨	▨	▨	ON/ OFF	G/C	WIDE	BLE	AT

Notes: 1. ▨ : Invalid data bits.

2. The "value to be specified-1" should be programmed in registers marked *2.

3. Data bits 5 and 6 of the cursor start register control the cursor display as shown below:

B	P	Cursor Mode
0	0	Cursor on, not blinking
0	1	Cursor off
1	0	Blinking every 32 frames
1	1	Blinking every 64 frames

4. The OR of the mode pin status and the mode register determine the mode.

Table 1-2 Register Addresses

CS	RS	Address Register 4	3	2	1	0	Reg. No.	Program Register Name	Unit	R/W
1	-	-	-	-	-	-	-	Invalid	-	-
0	0	-	-	-	-	-	AR	Address Register		W
0	1	0	0	0	0	0	R0	Horizontal total characters	Character	W
0	1	0	0	0	0	1	R1	Horizontal displayed characters	Character	W
0	1	0	1	0	0	1	R9	Maximum raster address	Raster	W
0	1	0	1	0	1	0	R10	Cursor start raster	Raster	W
0	1	0	1	0	1	1	R11	Cursor end raster	Raster	W
0	1	0	1	1	0	0	R12	Start address (H)	Mem addr	R/W
0	1	0	1	1	0	1	R13	Start address (L)	Mem addr	R/W
0	1	0	1	1	1	0	R14	Cursor address (H)	Mem addr	R/W
0	1	0	1	1	1	1	R15	Cursor address (L)	Mem addr	R/W
0	1	1	0	0	1	0	R18	Horizontal virtual screen width	Character	W
0	1	1	0	0	1	1	R19	Multiplexing duty ratio (H)	Raster	W
0	1	1	0	1	0	0	R20	Multiplexing duty ratio (L)	Raster	W
0	1	1	0	1	0	1	R21	Display start raster	Raster	W
0	1	1	0	1	1	0	R22	Mode register	-	W

Notes:

1. R/W shows whether the CPU can only write into the register, or can both read from and write into the register.
2. Registers R2-R8, R16, and R17 are not assigned for the LCTC. Programming these registers Nos. will be ignored.

Table 1-3 shows internal register description.

Table 1-3 Internal Register Desciption

Reg. No.	Register Name	Description
AR	Address register	Specifies the internal control registers (R0, R1, R9-R15, R18-R22) address to be accessed (5 bits).
R0	Horizontal total characters	Specifies the horizontal scanning period (8 bits).
R1	Horizontal displayed characters	Specifies the number of displayed characters per character row (8 bits).
R9	Maximum raster address	Specifies the number of rasters per character row; including the space between character rows (5 bits).
R10	Cursor start raster	Specifies the cursor start raster address and its blink mode (5 + 2 bits).
R11	Cursor end raster	Specifies the cursor end raster address (5 bits).
R12	Start address (h)	Specifies the display start address (16 bits).
R13	Start address (l)	
R14	Cursor address (H)	Specifies the cursor display address (16 bits).
R15	Cursor address (L)	
R18	Horizontal virtual screen width	Specifies the length of a character row in memory space, for horizontal scrolling (8 bits).
R19	Multiplexing duty ratio (H)	Specifies the number of rasters of a screen (16 bits).
R20	Multiplexing duty ratio (L)	
R21	Display start raster	Specifies the display start raster address of the first character row, for smooth scrolling (5 bits).
R22	Mode register	Controls the display mode (5 bits).

Note: For more details of registers, refer to
LCD Timing Controller (LCTC) HD63645F/HD64645F USER'S MANUAL.

1.2 Display Screen Size and Values in Registers

Figure 1-1 shows the relation between the LCTC internal registers and a display screen.

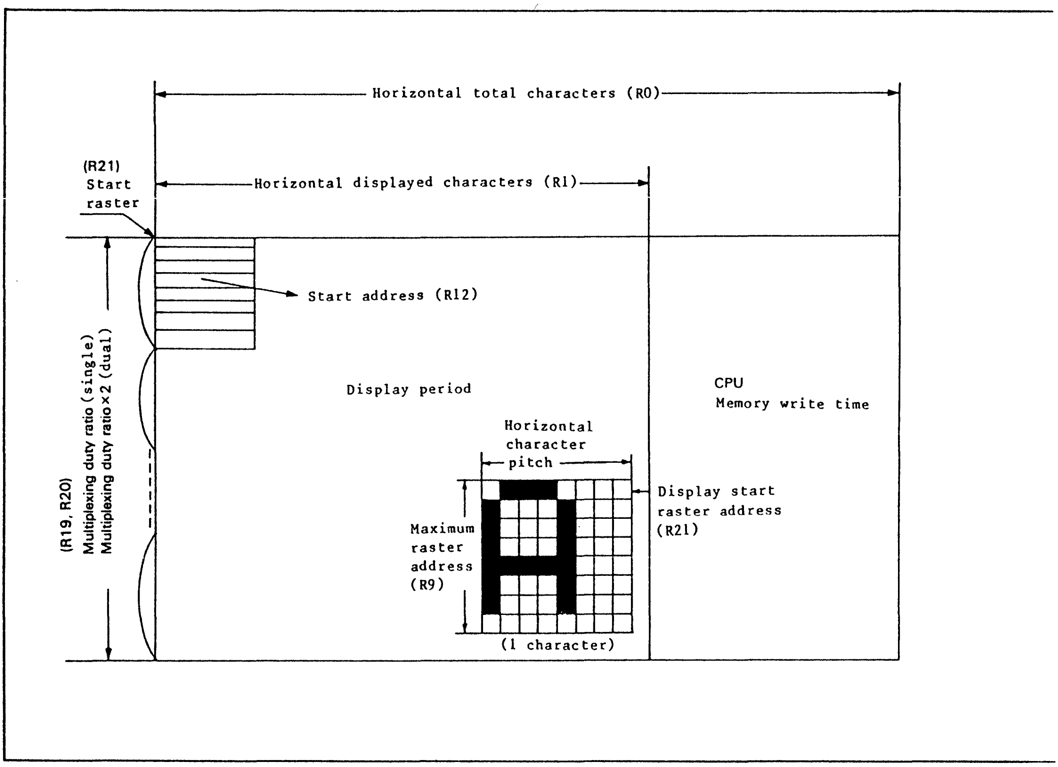

Horizontal total characters (R0)
(R21)
Start
raster
Horizontal displayed characters (R1)
Start address (R12)
Display period
CPU
Memory write time
Horizontal character pitch
Display start raster address (R21)
Maximum raster address (R9)
(1 character)
(R19, R20)
Multiplexing duty ratio (single)
Multiplexing duty ratio×2 (dual)

Figure 1-1 Relation between Display Screen and Registers

Table 1-4 shows the relation between the values in the registers and the size of an actual display screen. However, the relation depends on the modes.

Table 1-4 Screen Size Selection

Item	Mode No.	Actual Screen Size
Number of Horizontal Dots of a Screen	1, 5, 9	8 x Nhd
	2, 3, 4, 6, 7, 8, 10, 11, 12, 13	16 x Nhd
Number of Vertical Dots of a Screen	5, 6, 7, 8, 9, 10, 11, 12	Nd + 1
	1, 2, 3, 4, 13	2 x (Nd + 1)

Note: Nhd = horizontal displayed characters (R1)
Nd = Multiplexing duty ratio (R19, R20)

Table 1-5 shows the overall relation between the values in the registers and the screen size.

Table 1-5 Relation between Values in Internal Registers and Screen Size

No.	Mode No.	Character or Graphic	Screen Configuration	No. of Horizontal Dots of a Character	No. of Horizontal Dots of a Screen	No. of Vertical Dots of a Screen	Raster Time (us)
1	1	Character (Normal)	Dual	8	8 x Nhd	2 x Nd	$\frac{1}{f_{DCLK}} \times Nht \times 8$
2	5, 9	Character (Normal)	Single	8	8 x Nhd	Nd	$\frac{1}{f_{DCLK}} \times Nht \times 4$
3	2	Character (Wide)	Dual	16	16 x Nhd	2 x Nd	$\frac{1}{f_{DCLK}} \times Nht \times 16$
4	6, 10	Character (Wide)	Single	16	16 x Nhd	Nd	$\frac{1}{f_{DCLK}} \times Nht \times 8$
5	3, 4, 13	Graphic	Dual	16	16 x Nhd	2 x Nd	$\frac{1}{f_{DCLK}} \times Nht \times 16$
6	7, 8, 11, 12	Graphic	Single	16	16 x Nhd	Nd	$\frac{1}{f_{DCLK}} \times Nht \times 8$

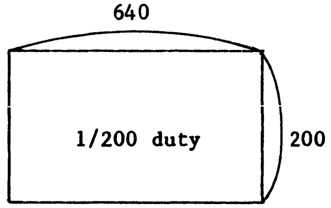
Note: Nht = horizontal total characters (R0)
Nhd = horizontal displayed characters (R1)
Nd = multiplexing duty ratio (R19, R20)
f_{DCLK} = DCLK frequency (MHz)

Figure 1-2 describes 3 cases of setting values for each screen configuration. In this case, f_{DCLK} = 10 MHz and f_F = 65 MHz to 70 MHz.

(1) 640 x 200 dots, 1/200 duty, single screen

(a) Mode 5 (character mode)

Nht = 178 (R0 set value)
Nhd = 80 (R1 set value)
Nd = 199 (R19, R20 set value)



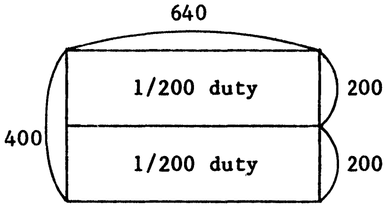
(b) Mode 7 (graphic 1 mode)

Nht = 89 (R0 set value)
Nhd = 40 (R1 set value)
Nd = 199 (R19, R20 set value)

(2) 640 x 400 dots, 1/200 duty, dual screen

(a) Mode 1 (character mode)

Nht = 89 (R0 set value)
Nhd = 80 (R1 set value)
Nd = 199 (R19, R20 set value)



(b) Mode 3 (graphic 1 mode)

Nht = 44 (R0 set value)
Nhd = 40 (R1 set value)
Nd = 199 (R19, R20 set value)

(c) Mode 13 (large screen graphic 1 mode)

Nht = 89 (R0 set value)
Nhd = 40 (R1 set value)
Nd = 199 (R19, R20 set value)

(3) 720 x 540 dots, 1/270 duty, dual screen

Mode 13 (large screen graphic 1 mode)

Nht = 58 (R0 set value)
Nhd = 45 (R1 set value)
Nd = 269 (R19, R20 set value)

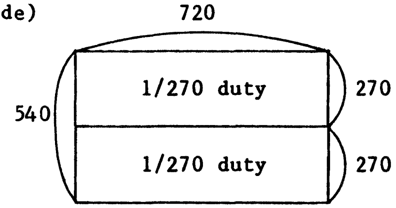


Figure 1-2 Screen Configurations

Since the set values in the registers determining the screen size have the following limitations, extra care should be taken in programming.

(1) $1 < Nhd < Nht + 1 \leq 256$

(2) $Nhd + \frac{16}{m^{*1}} \leq Nht + 1$

(3) (Number of vertical dots) x (number of horizontal dots) x (frame frequency; f_{FRM}) $\leq$ (data transfer speed; V)

$$\begin{Bmatrix} 1 \\ 2 \end{Bmatrix}^{*2} \times (Nd + 1) \times Nhd \times \begin{Bmatrix} 8 \\ 16 \end{Bmatrix}^{*3} \times f_{FRM} \leq V$$

(4) $0 \leq Nd \leq 511$

*1: The value of m depends on the mode, as shown in the following table.

Mode No.	m
5, 9	1
1, 6, 7, 8, 10, 11, 12, 13	2
2, 3, 4	4

*2: Set to 1 if the LCD screen has 1 panel (= single screen configuration), and to 2 if the LCD screen has 2 panels (= dual screen configuration). Refer to the following table.

Mode No.	Set Value
5, 6, 7, 8, 9, 10, 11, 12	1
1, 2, 3, 4, 13	2

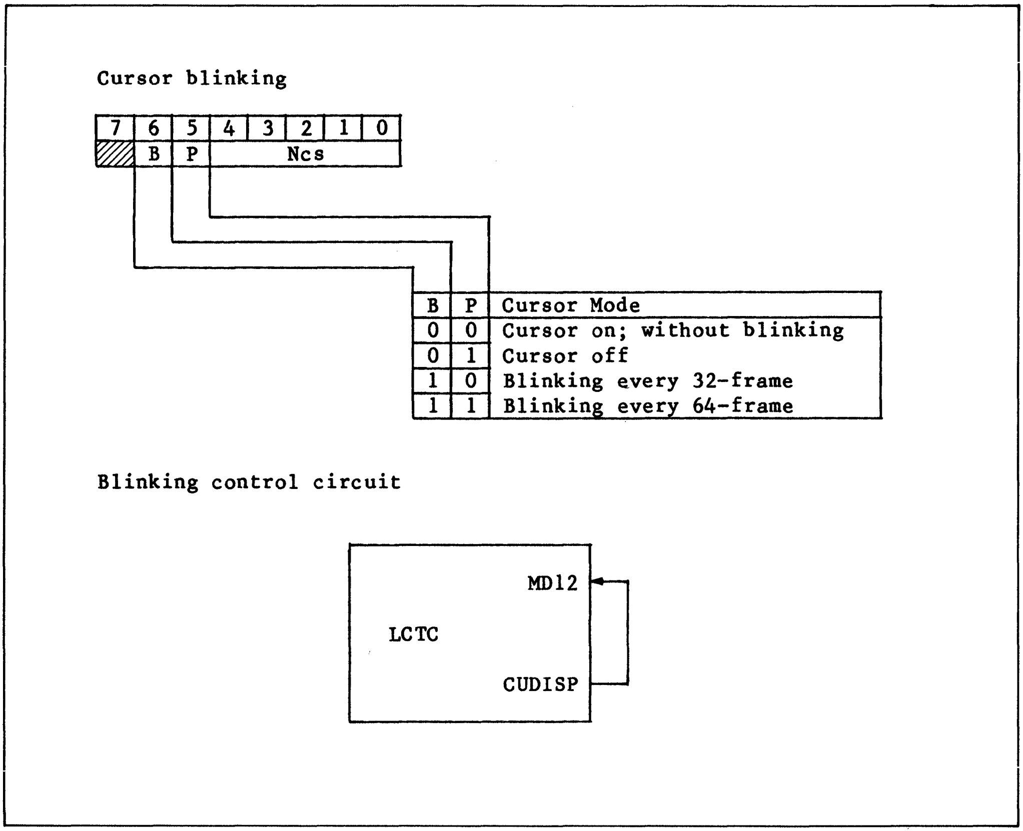
*3: Set to 8 if one character consists of 8 dots and to 16 if one character consists of 16 dots, as shown below.

Mode No.	Set Value
1, 5, 9	8
2, 3, 4, 6, 7, 8, 10, 11, 12, 13	16

1.3 Display Function and Values in Registers

1.3.1 Cursor display

The LCTC can program display mode of cursor as listed in figure 1-3 and display shape of cursor as shown in figure 1-4 set by cursor start raster register (R10) and cursor end raster register (R11). Therefore, the LCTC can not only realize cursor display required for the system, but also change display mode dynamically according to the system state.



B	P	Cursor Mode
0	0	Cursor on; without blinking
0	1	Cursor off
1	0	Blinking every 32-frame
1	1	Blinking every 64-frame

Figure 1-3 Cursor On/Off by CUDISP and Blinking Control Circuit

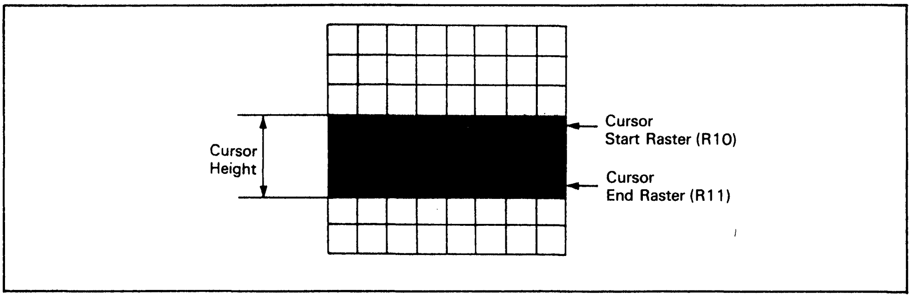


Figure 1-4 Cursor Display

The set values in the registers controlling cursor display have the following limitations:

(1) $0 \leq Ncs \leq Nce$

(2) $Nce \leq Nr$

Note: Ncs = cursor start raster (R10)
Nce = cursor end raster (R11)
Nr = maximum raster address (R9)

1.3.2 Start address

Start address registers (R12, R13) can provide an offset for the read address of a frame buffer. This function facilitates paging and scrolling.

Figure 1-6 shows the relation between the number of displayed characters and the memory addresses when the start address is 0. Setting Nhd as a start address shifts the display one character row upward. Scrolling is enabled by adding Nhd to the current start address in this way. (Nhd = number of horizontal displayed characters, set value in (R1).)

Writing $<\{(Nd + 1) / (Nr + 1)\} \times Nhd>$ as a start address enables paging. (Nd = multiplexing duty ratio, set value in (R19) and (R20), Nr = maximum raster address, set value in (R9).)

1.3.3 Cursor address

Cursor display position can be programmed by cursor address registers (R14, R15). In this case, the user is to program cursor address with linear addresses, not X and Y addresses.

1.3.4 Horizontal virtual screen width

Horizontal virtual screen width register (R18) can provide an offset for start addresses of adjoining two lines. This function facilitates horizontal scrolling.

Figure 1-5 shows the concept of horizontal virtual screen width, and figure 1-6 shows an example of setting horizontal virtual screen width.

If the user does not need this function, set the same value into the horizontal virtual screen width register (R18) as the value in the horizontal displayed characters register (R1).

The set value in the horizontal virtual screen width register has the following limitations:

(1) $Nhd \leq Nir$

(2) $0 \leq Nir \leq 255$

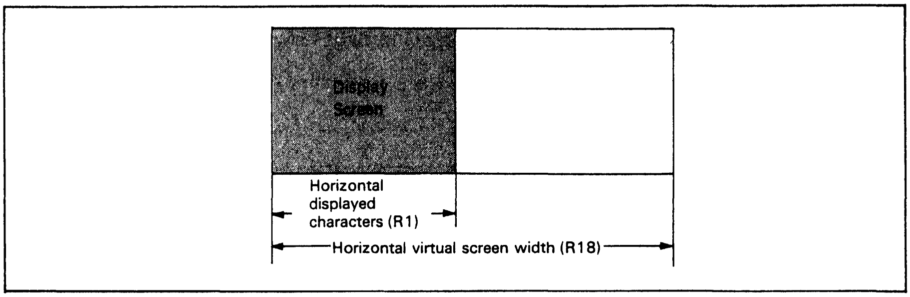

Display Screen
Horizontal displayed characters (R1)
Horizontal virtual screen width (R18)

Figure 1-5 **Horizontal Virtual Screen Width**

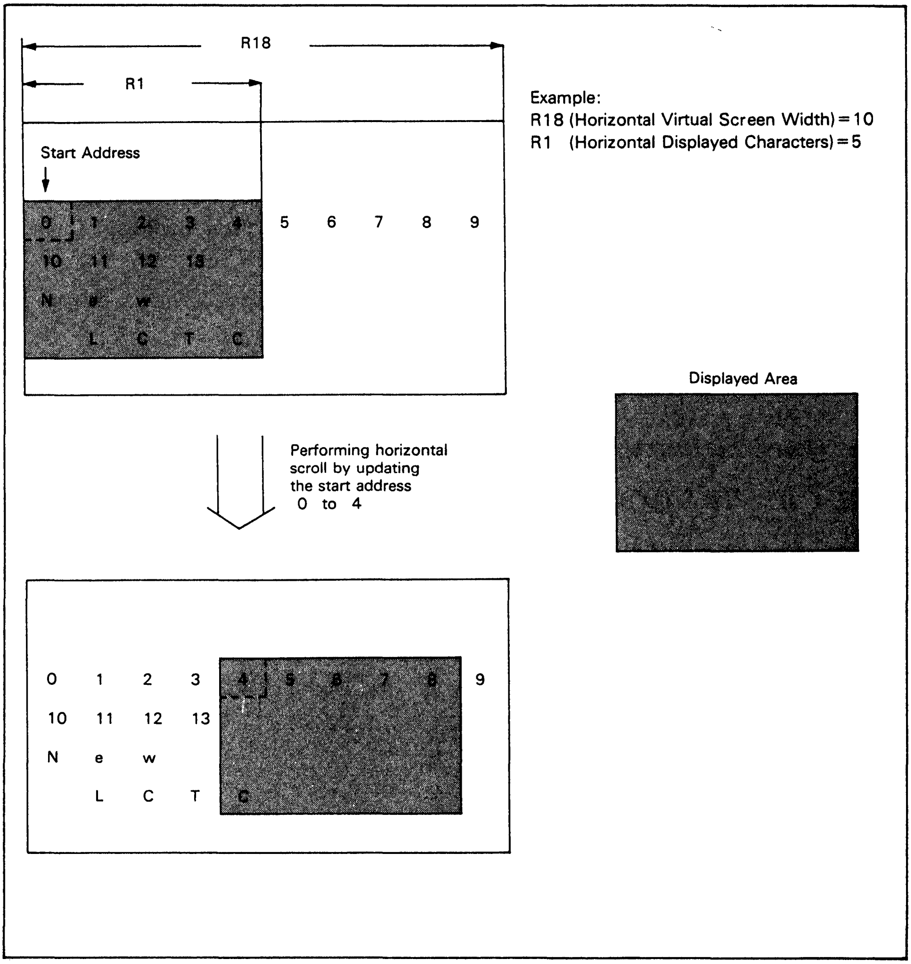

R18
R1
Start Address
0 1 2 3 4 5 6 7 8 9
10 11 12 13
N e w
L C T C
Example:
R18 (Horizontal Virtual Screen Width) = 10
R1 (Horizontal Displayed Characters) = 5
Performing horizontal scroll by updating the start address 0 to 4
Displayed Area
0 1 2 3 4 5 6 7 8 9
10 11 12 13
N e w
L C T C

Figure 1-6 **Example of Setting Horizontal Virtual Screen Width**

1.3.5 Display start raster

Display start raster register (R21) can provide an offset for the start raster of the first row. This function enables smooth scrolling.

Figure 1-7 shows an example of smooth scroll by setting display start raster address.

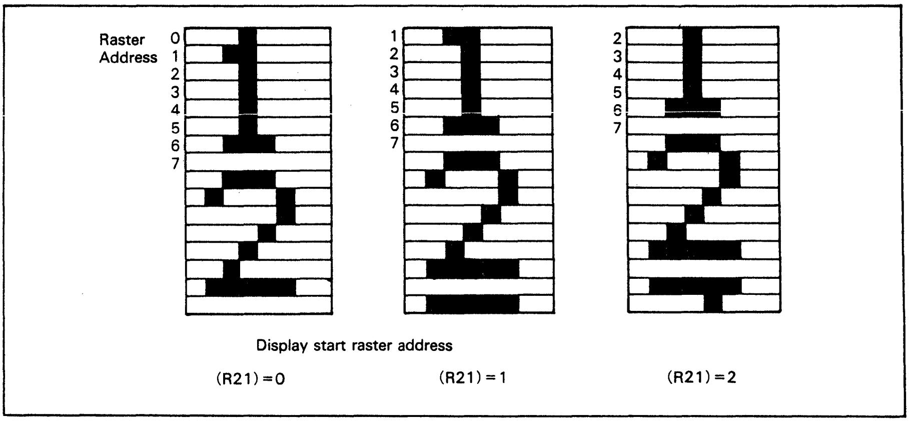


Figure 1-7. Example of Smooth Scroll by Setting Display Start Raster Address

The set value (Nsr) in the display start raster register has the following limitations.

$Nsr \leq Nr$

Note: Nr = set value in the maximum raster address register (R9)

1.3.6 Modes

The LCTC controls display modes (display on/off selection, wide display, etc.) with mode register (R22). For details, refer to "2. LCD SCREEN CONFIGURATION AND MODES."

1.4 Display Screen and Memory Addresses

Memory address changes at the fall of the MCLK signal. The relation between the frequency of the MCLK signal and that of memory address (MA) change differs from mode to mode. Table 1-6 shows the relation between modes and the frequency of memory address change.

Table 1-6 Modes and Frequency of MA Change

Mode No.	MA Change Frequency
1, 2, 3, 4, 9	f_{MCLK}
5, 13	f_{MCLK}
6, 7, 8	$f_{MCLK}/2$
10, 11, 12	$f_{MCLK}/2$

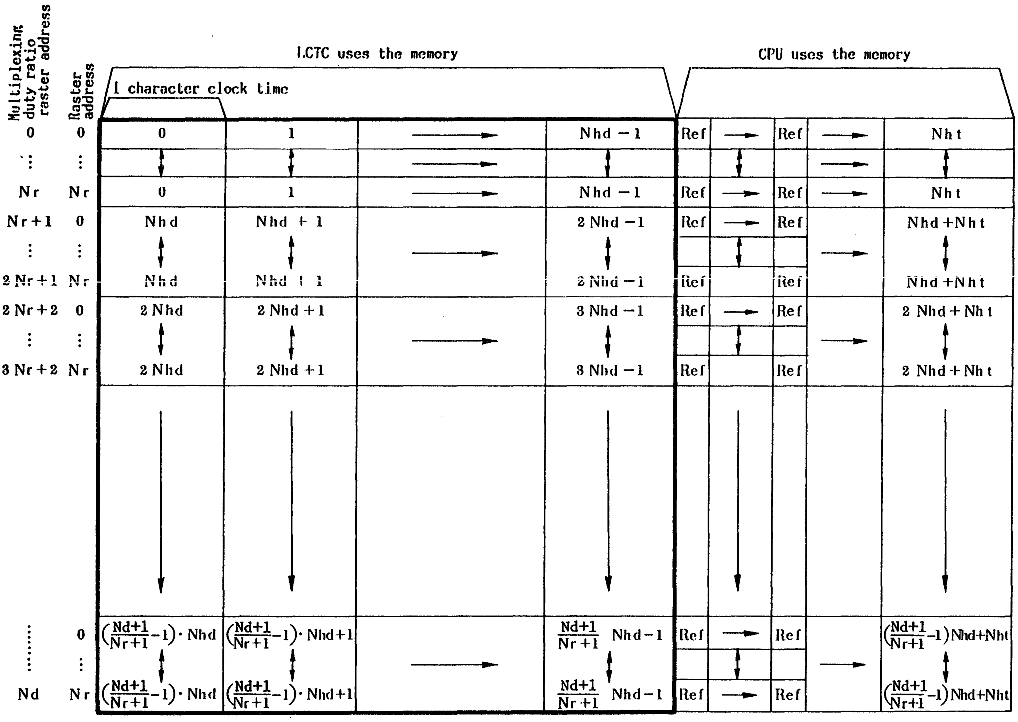
Memory address is counted up even though the display period, in which the LCTC uses the memory, is over. But it does not affect the display since data transfer to an LCD is suspended. (DISPTMG signal is high in the display period.)

The LCTC hands over the memory to the CPU in the data transfer suspended period. (DISPTMG signal is low in the period.)

Figure 1-8 shows the relation between the number of displayed characters and the memory addresses when the horizontal displayed characters (Nhd) is the same as the horizontal virtual screen width (Nir) and the start address is 0. The relation shown in this figure is the base of the character position and the memory addresses.

Figure 1-9 shows the relation between the number of displayed characters and the memory addresses when Nir > Nhd. This is the relation when horizontal scroll function is used.

Figure 1-10 shows the relation between the number of displayed characters and the memory addresses when the display start raster (Nsr) = 2. This is the relation when smooth scroll function is used.



Notes: 1. ☐ indicates the display screen.

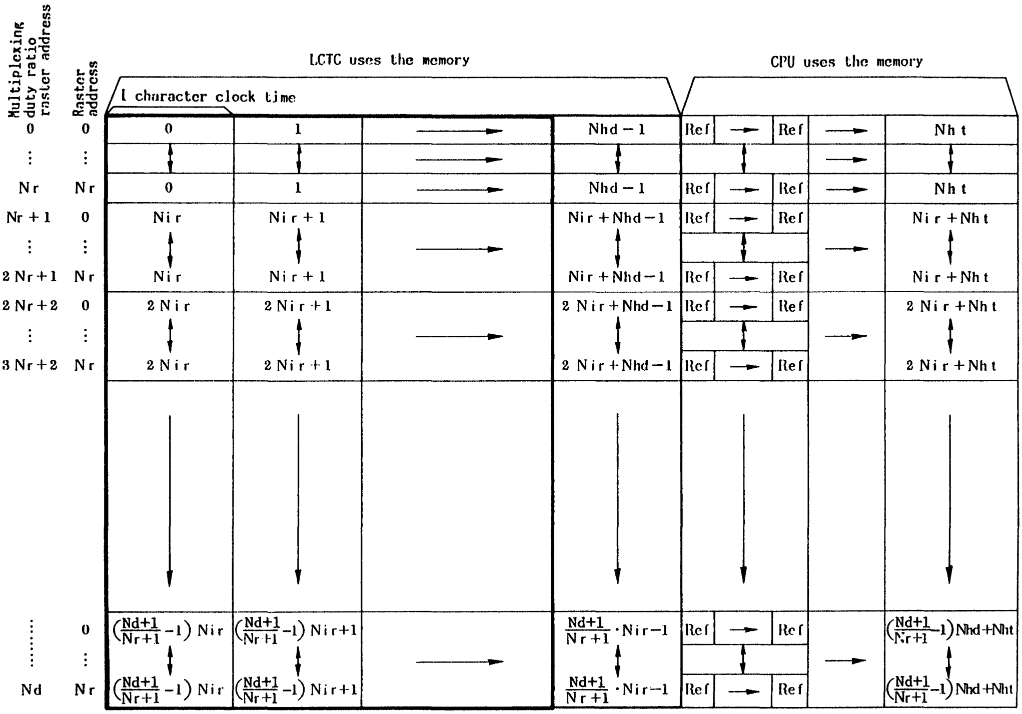
2. Ref: DRAM refresh address. See <u>LCD Timing Controller (LCTC) HD63645F/ HD64645F USER'S MANUAL</u>.

3. Register values corresponding to the screen in figure 1-8:

Register No.	Register Name	Set Value
R0	Horizontal total characters	Nht
R1	Horizontal displayed characters	Nhd
R9	Maximum raster address	Nr
R12, R13	Start address	0
R18	Horizontal virtual screen width	Nhd
R19, R20	Multiplexing duty ratio	Nd
R21	Display start raster	0

4. Figure 1-8 shows the screen in mode 5 (single screen, 4-bit data transfer, normal character mode).

Figure 1-8 Relation between Number of Displayed Characters and Memory Addresses When Nir = Nhd



Notes: 1. □ indicates the display screen.

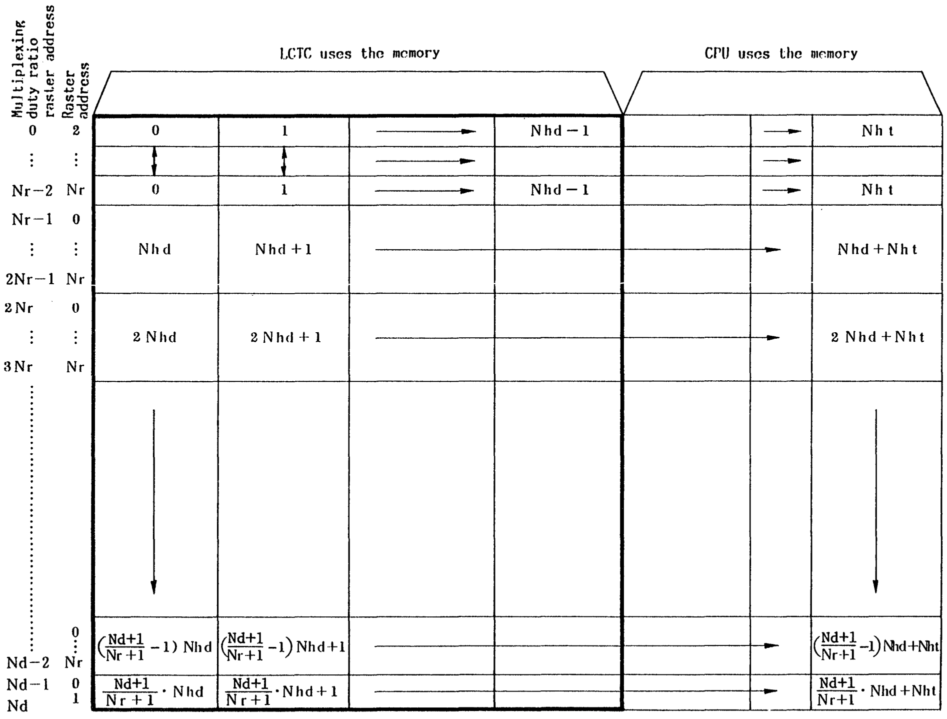
2. Ref: DRAM refresh address. See LCD Timing Controller (LCTC) HD63645F/ HD64645F USER'S MANUAL.

3. Register values corresponding to the screen in figure 1-9:

Register No.	Register Name	Set Value
R0	Horizontal total characters	Nht
R1	Horizontal displayed characters	Nhd
R9	Maximum raster address	Nr
R12, R13	Start address	0
R18	Horizontal virtual screen width	Nir
R19, R20	Multiplexing duty ratio	Nd
R21	Display start raster	0

4. Figure 1-9 shows the screen in mode 5 (single screen, 4-bit data transfer, normal character mode).

Figure 1-9 Relation between Number of Displayed Characters and Memory Addresses When Nir > Nhd


Multiplexing duty ratio raster address
Raster address
LCTC uses the memory
CPU uses the memory
0 2
Nr−2 Nr
Nr−1 0
2Nr−1 Nr
2Nr 0
3Nr Nr
Nd−2 Nr
Nd−1 0
Nd 1
0
1
Nhd−1
Nht
Nhd
Nhd+1
Nhd+Nht
2 Nhd
2 Nhd+1
2 Nhd+Nht
$(\frac{Nd+1}{Nr+1}-1)$ Nhd
$(\frac{Nd+1}{Nr+1}-1)$ Nhd+1
$(\frac{Nd+1}{Nr+1}-1)$ Nhd+Nht
$\frac{Nd+1}{Nr+1}\cdot$ Nhd
$\frac{Nd+1}{Nr+1}\cdot$ Nhd+1
$\frac{Nd+1}{Nr+1}\cdot$ Nhd+Nht

Notes: 1. ☐ indicates the display screen.

2. Register values corresponding to the screen in figure 1-10:

Register No.	Register Name	Set Value
R0	Horizontal total characters	Nht
R1	Horizontal displayed characters	Nhd
R9	Maximum raster address	Nr
R12, R13	Start address	0
R18	Horizontal virtual screen width	Nhd
R19, R20	Multiplexing duty ratio	Nd
R21	Display start raster	2

3. Figure 1-10 shows the screen in mode 5 (single screen, 4-bit data transfer, normal character mode).

Figure 1-10 Relation between Number of Displayed Characters and Memory Addresses When Nsr = 2

2. LCD SCREEN CONFIGURATION AND MODES

2.1 LCD Screen Configuration

In constructing an LCD system, the user needs to choose a single screen or a dual screen unlike CRT.

A single screen costs less than a dual screen because of the small number of column drivers for a display and of its small mounting size. However, it has limited duty ratio, LCD drive voltage, and display quality of the liquid crystal. A dual screen is necessary to improve these factors.

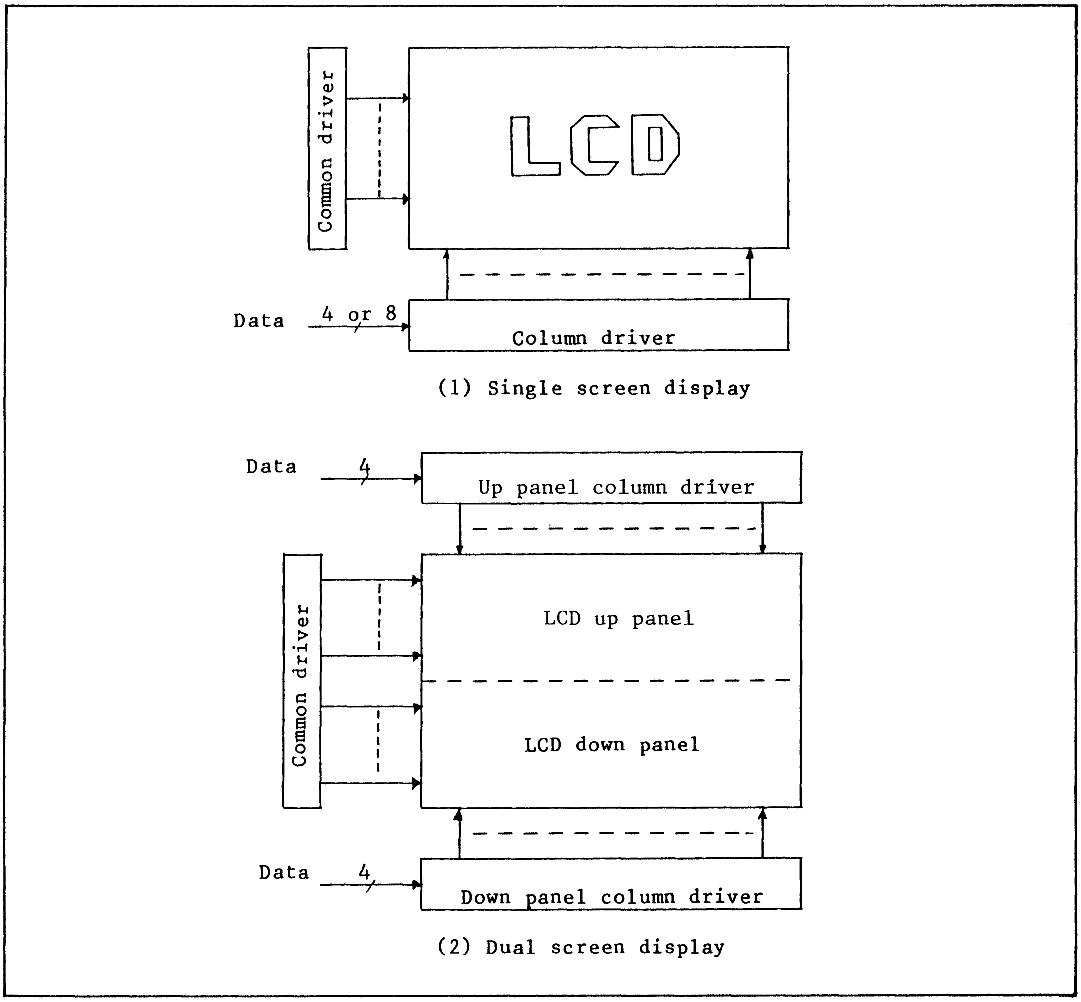


Figure 2-1 System Configuration Comparison of Single Screen and Dual Screen

2.2 Display Format

The LCTC display formats can be broadly divided into character display and graphic display. The following gives you general description. For more details, refer to LCD Timing Controller (LCTC) HD63645F/HD64645F USER'S MANUAL.

2.2.1 Character mode display

Character mode receives and displays the data of a CG ROM (Character generator ROM) according to VRAM data.

Figure 2-2 shows an example of system configuration and display in character mode.

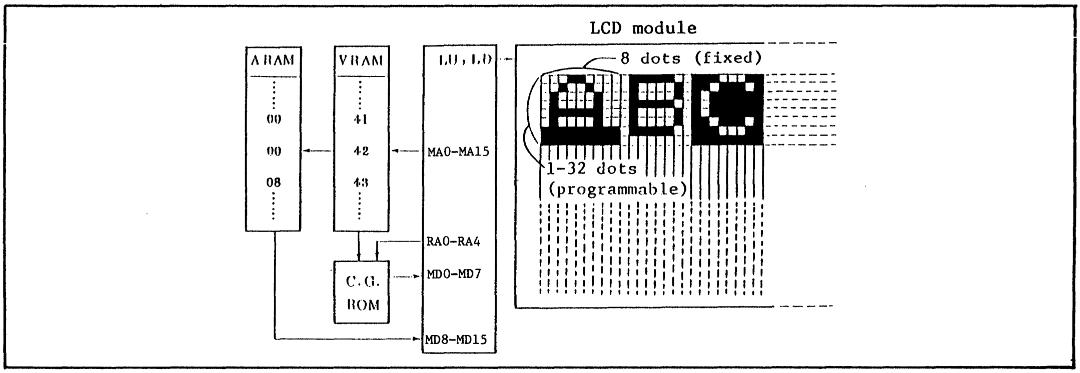
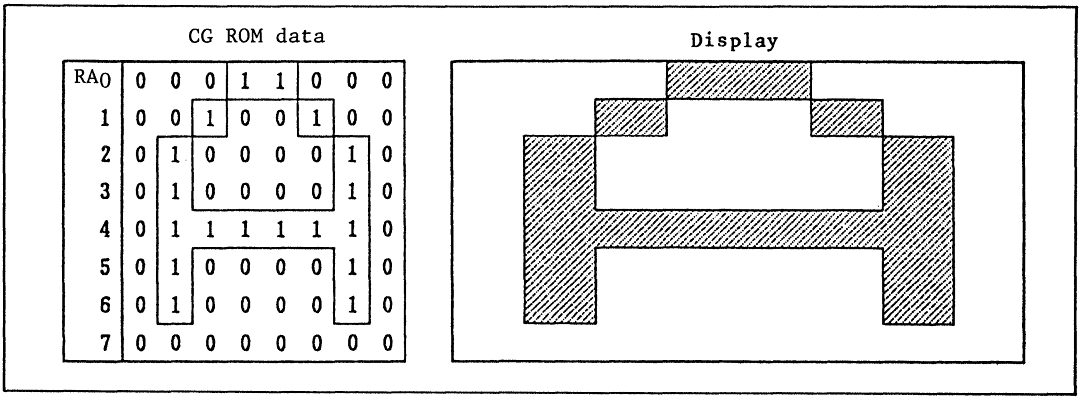


Figure 2-2 Example of System Configuration and Display in Character Mode

In this mode, it is possible to double the whole display in width. Figure 2-3 shows an example.



RA0	0	0	0	1	1	0	0	0
1	0	0	1	0	0	1	0	0
2	0	1	0	0	0	0	1	0
3	0	1	0	0	0	0	1	0
4	0	1	1	1	1	1	1	0
5	0	1	0	0	0	0	1	0
6	0	1	0	0	0	0	1	0
7	0	0	0	0	0	0	0	0

Figure 2-3 Wide Character Display

2.2.2 Graphic display

Graphic mode displays the data in a frame buffer as it is.

The LCTC provides three methods of graphic display.

(1) 1 RAM graphics

1 RAM graphics mode uses the LCTC in character mode with the maximum raster address set to 0. This mode is suitable for a rather small LCD since it needs only one RAM.

Figure 2-4 shows a graphic display system using 1 RAM.

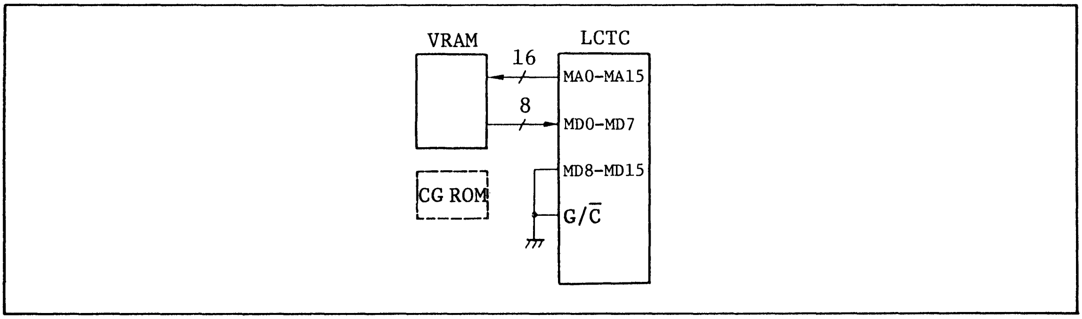


Figure 2-4 Graphic Display System Using 1 RAM

(2) Graphic 1 mode display

Graphic 1 mode displays 16-bit data entered into the MD0-MD15 pins as it is. Thus it requires 2 RAM's at least. This mode is suitable for displaying graphics by hardware originally configured for displaying characters with the attribute function.

In this mode, the value in the maximum raster address register does not affect the display.

Figure 2-5 shows an example of system configuration and display in graphic 1 mode.

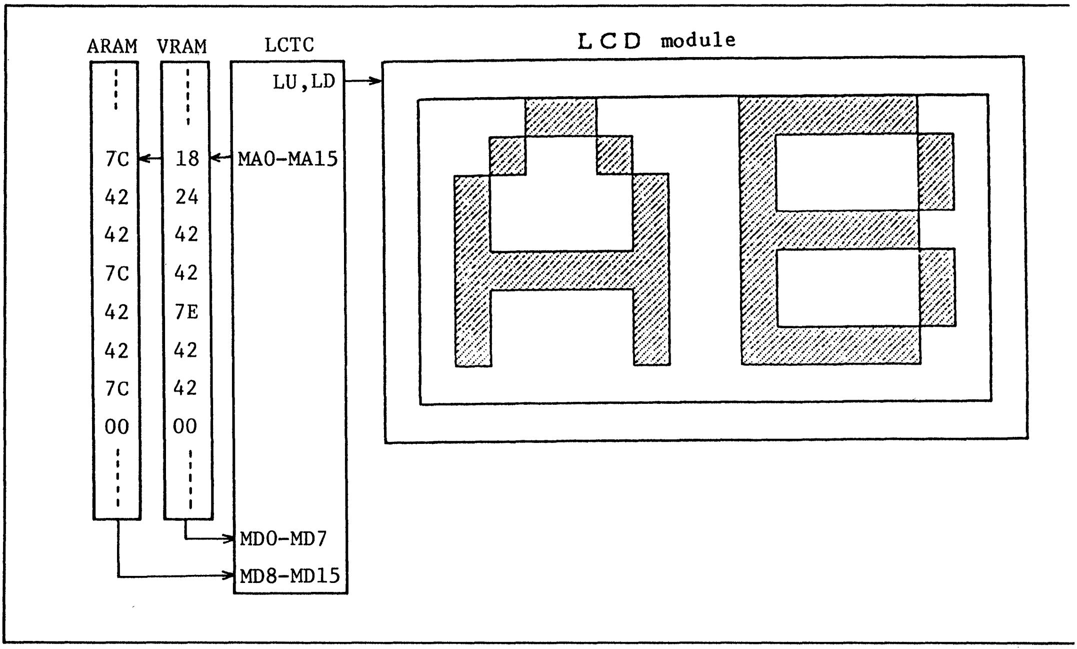


Figure 2-5 Example of System Configuration and Display in Graphic 1 Mode

(3) Graphic 2 mode display

Graphic 2 mode also displays the data entered into MD0-MD15 pins as graphic 1 mode does, and it requires 2 RAMs at least. However, the value in the maximum raster address register affects the display.

This mode can be used with the graphic software designed for a CRT display system with an HD6845 (CRTC).

2.3 Attribute Function and OR Function

2.3.1 Attribute function

The LCTC can give a variety of attributes (reverse video, cursor, blinking, white, or black) to a specified character in character mode display. As shown in table 2-1, the character code entered into MD7-MD0 determines which character should be given the attribute. The attribute codes entered into MD15-MD8 determine which attribute should be given. The data entered into MD10-MD8 is invalid.

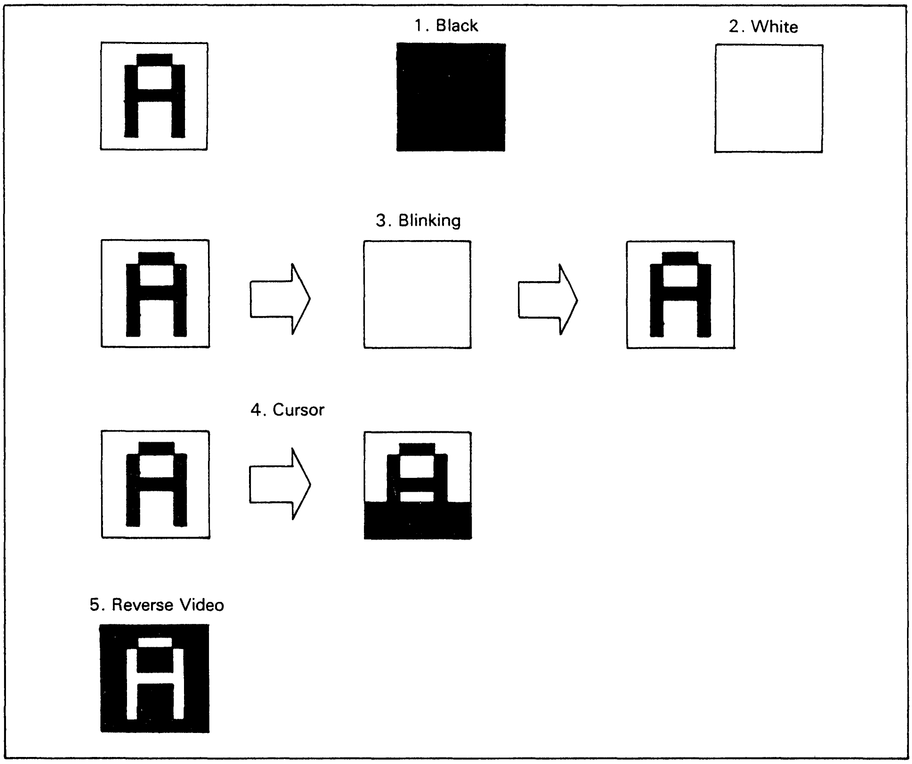


Figure 2-6 Display Example Using Attribute Functions

Table 2-1 Attribute Codes

MD Input	15	14	13	12	11	10-8	7-0
Function	Non-display (black)	Non-display (white)	Blinking	Cursor	Reverse video	Invalid	Character Code

2.3.2 OR function

In character mode, the LCTC can superimpose the data entered into MD7-MD0 and the data entered into MD15-MD8. This function is used when superimposing graphics and characters.

Figure 2-7 shows how the OR function works.

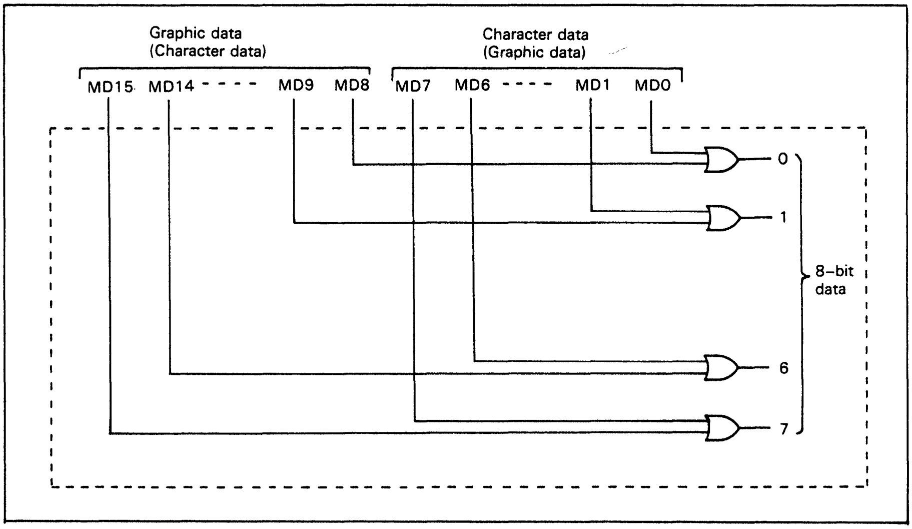


Figure 2-7 OR Function

Attribute function is disabled when OR function is used, and vice versa. For details, see LCD Timing Controller (LCTC) HD63645F/HD64645F USER'S MANUAL.

2.4 Mode Setting

2.4.1 Mode selection

Select the mode you use depending on the hardware configuration and display format.

Table 2-2 shows how to select the mode.

Table 2-2 Mode Selection

System Configuration			Display Format				
LCD Data Transfer	Screen Configuration	Screen Size	Character/ Graphic	Normal/ Wide	Attribute/ OR	Maximum Data Transfer Speed (MBPS)	Mode No.
4-bit	Single	Normal	Character	Normal	AT OR	20	5
				Wide	AT OR	10	6
			Graphic 1			20	7
			Graphic 2			20	8
	Dual	Normal	Character	Normal	AT OR	20	1
				Wide	AT OR	10	2
			Graphic 1			20	3
			Graphic 2			20	4
		Large	Graphic 1			40	13
8-bit	Single	Normal	Character	Normal	AT OR	20	9
				Wide	AT OR	10	10
			Graphic 1			20	11
			Graphic 2			20	12

2.4.2 Mode setting

The pins shown in table 2-3 determine the mode.

Table 2-3 Mode List

No.	Mode Name	Pin Name D/S	 G/C	 LS	 WIDE	 AT	Screen Config	Char/ Graph	Data Trans-fer	Wide/ Normal	Attri-bute	Trans-fer Speed (bps)
1	Dual screen normal char	1 1	0 0	0 0	0 0	0 1	Dual	Char	4-bit x 2	Normal	OR AT	2 x DCLK
2	Dual screen wide char	1 1	0 0	0 0	1 1	0 1				Wide	OR AT	
3	Dual screen graphic 1	1	1	0	0	1		Graph		-	-	
4	Dual screen graphic 2	1	1	0	0	0						
5	Single screen normal char	0 0	0 0	0 0	0 0	0 1	Single	Char	4-bit	Normal	OR AT	
6	Single screen wide char	0 0	0 0	0 0	1 1	0 1				Wide	OR AT	DCLK
7	Single screen graphic 1	0	1	0	0	1		Graph		-	-	2 x DCLK
8	Single screen graphic 2	0	1	0	0	0						
9	8-bit normal normal char	0 0	0 0	1 1	0 0	0 1		Char	8-bit	Normal	OR AT	
10	8-bit normal wide char	0 0	0 0	1 1	1 1	0 1				Wide	OR AT	1 x DCLK
11	8-bit normal graphic 1	0	1	1	0	1		Graph		-	-	2 x DCLK
12	8-bit normal graphic 2	0	1	1	0	0						
13	Large screen	1	1	1	0	1	Dual		4-bit x 2			4 x DCLK

Note: Char/Graph = Character or graphic

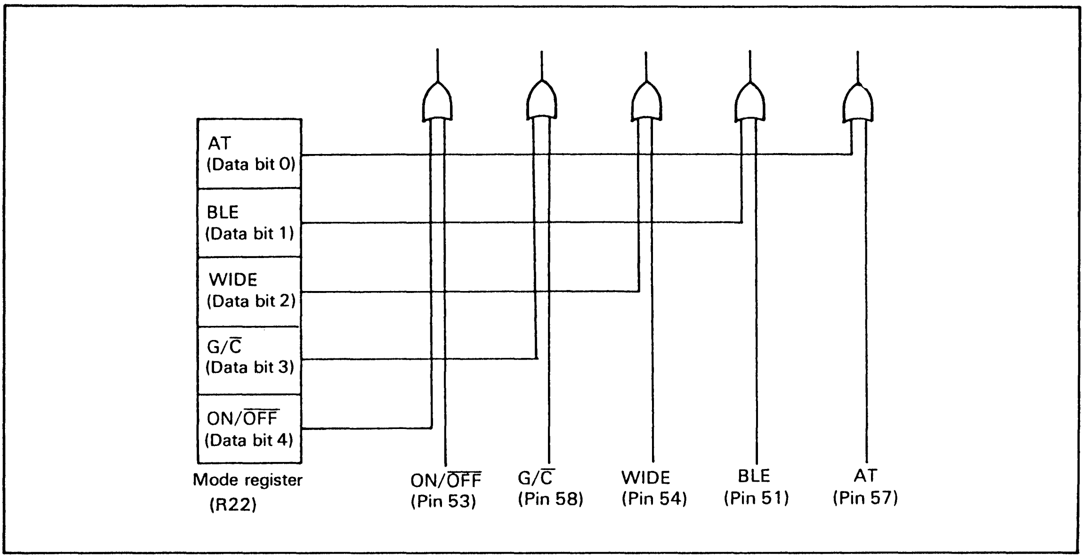


Figure 2-8 Correspondence between Mode Register and External Pins

SECTION
4

2.5 Timing Charts

Figure 2-9 (a)-figure 2-9 (j) show the timing charts of each mode when the values are set in the internal registers as in table 2-4.

Table 2-4 Register Values

Register No.	Register Name	Value
R0	Horizontal total characters	Nht
R1	Horizontal displayed characters	Nhd
R9	Maximum raster address	Nr
R10	Cursor start raster	Ncs
R11	Cursor end raster	Nce
R12	Start address (H)	-
R13	Start address (L)	-
R14	Cursor address (H)	-
R15	Cursor address (L)	-
R18	Horizontal virtual screen width	Nhd*
R19	Multiplexing duty ratio (H)	Ndh
R20	Multiplexing duty ratio (L)	Ndl
R21	Display start raster	Nsr
R22	Mode register	-

*: The horizontal virtual screen width register does not function since Nhd is set in (R18).

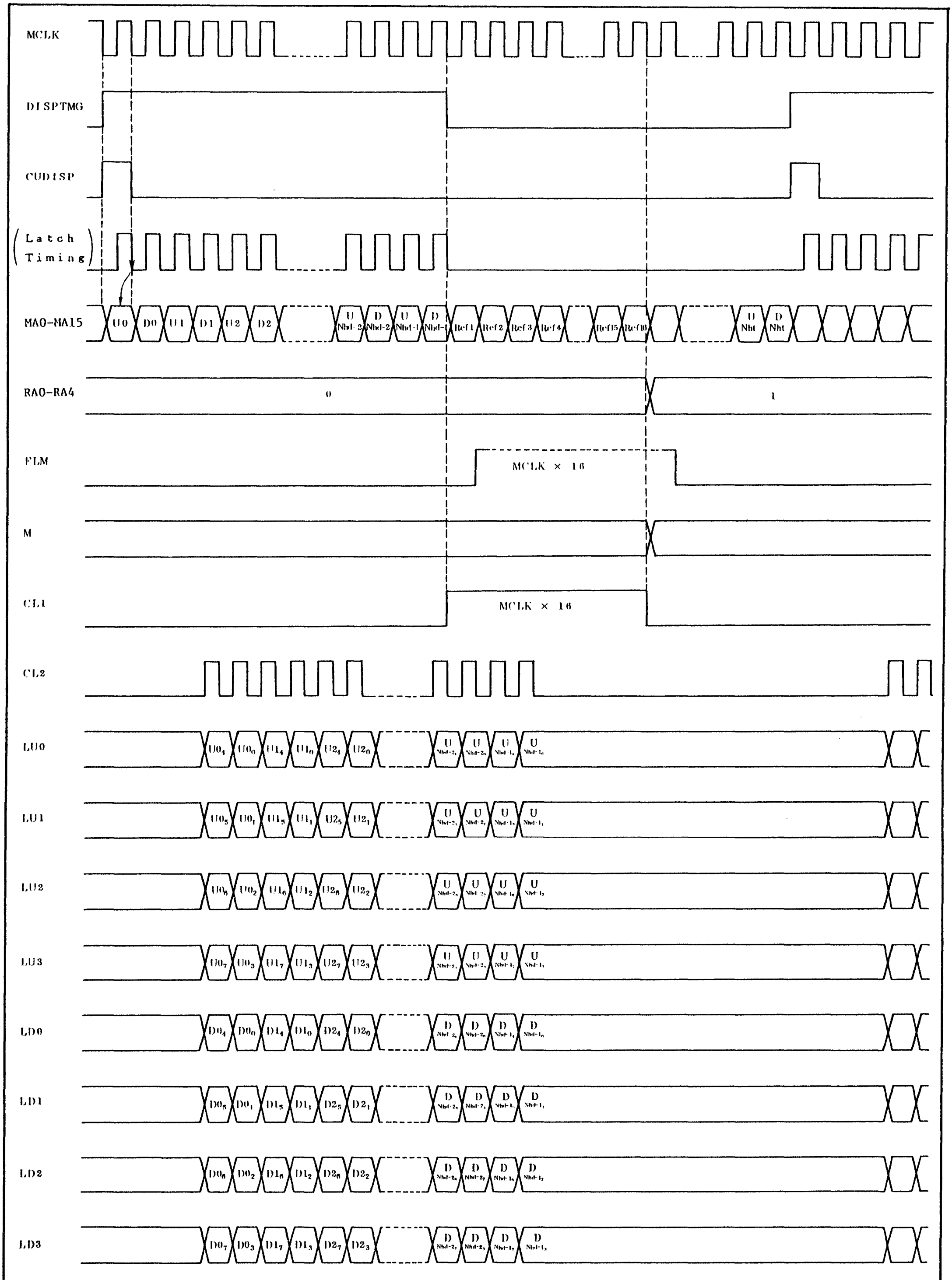
MCLK frequency is a quarter of DCLK frequency in every mode, but the relation between MCLK, the MA change frequency, and the CL2 frequency differs depending on the modes. Table 2-5 shows the relation. Refer to this table in choosing a memory IC and an LCD driver.

Table 2-5 Modes and Frequency of MA Change and CL2

Mode No.	MA Change Frequency	CL2 Frequency
1, 2, 3, 4, 9	f_{MCLK}	f_{MCLK}
5, 13	f_{MCLK}	2 x f_{MCLK}
6, 7, 8	$f_{MCLK}/2$	2 x f_{MCLK}
10, 11, 12	$f_{MCLK}/2$	f_{MCLK}

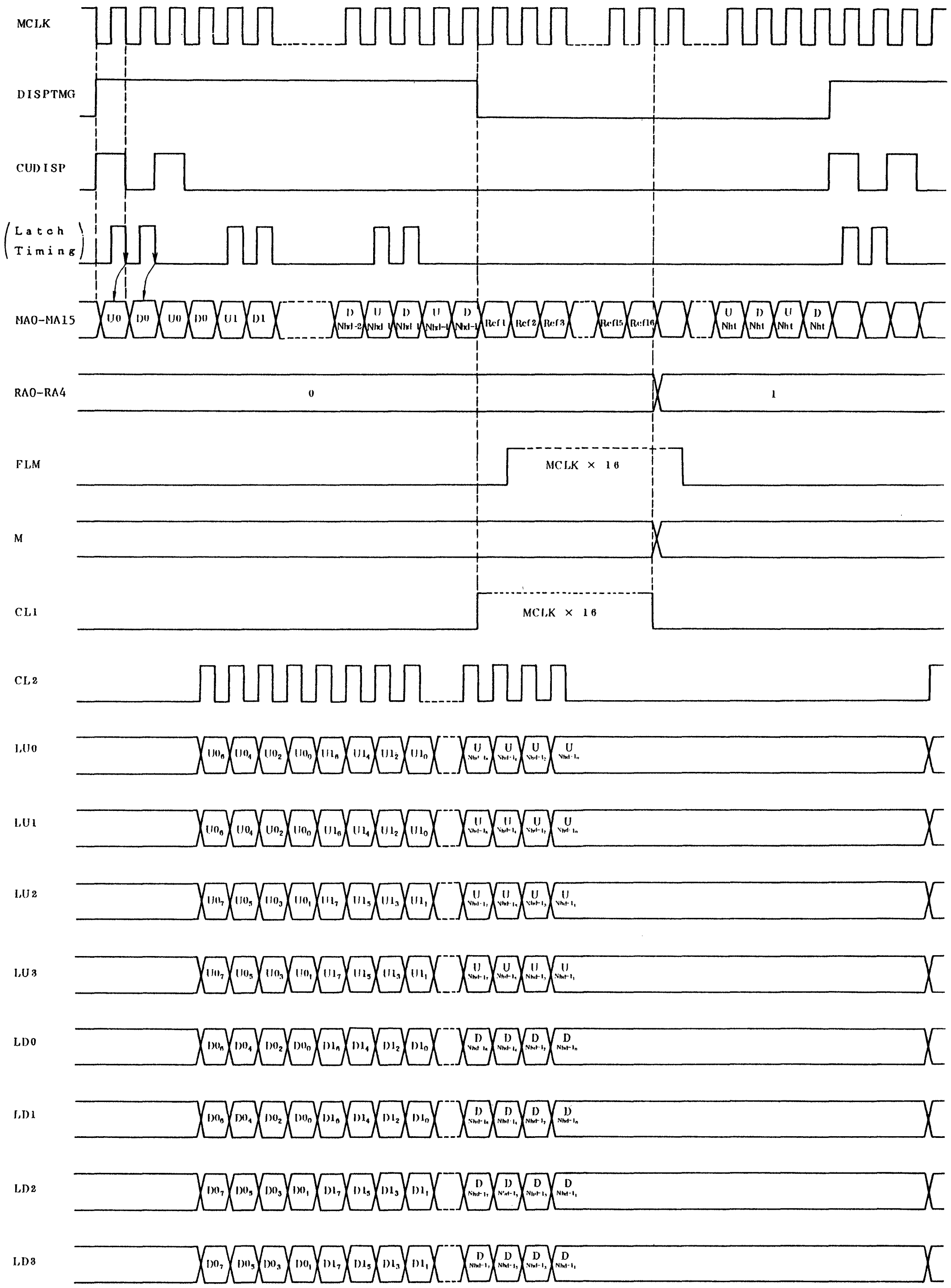
See each timing chart for the phase relation.

Figure 2-10 shows the timing chart of the period of a raster signal and a character row.



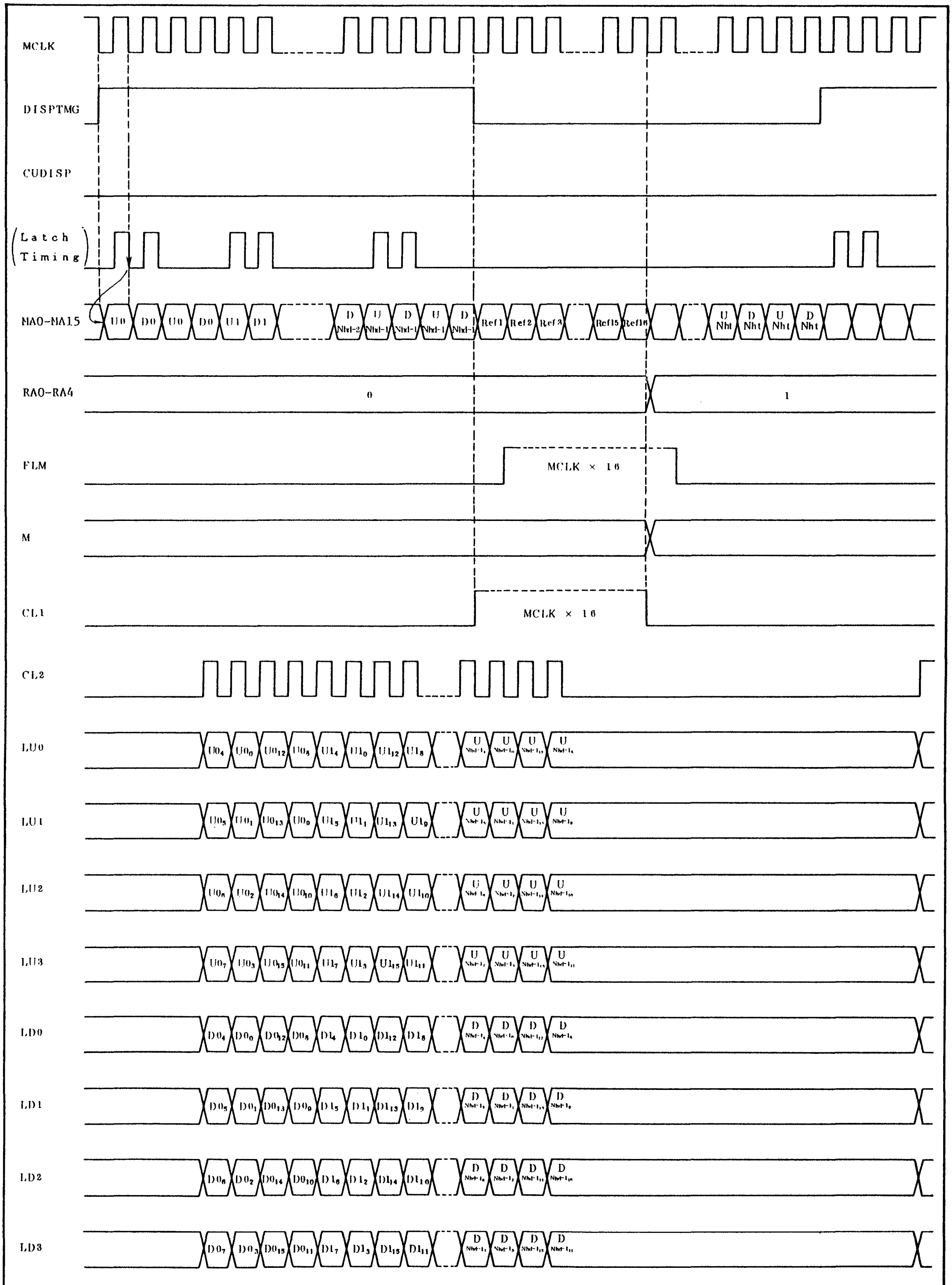
U = up panel address (data), D = down panel address (data), subscript = no. of MD pin,
Nhd = horizontal displayed characters, Nht = horizontal total characters

Figure 2-9 Timing Charts (a) Mode 1 (Dual screen normal character)



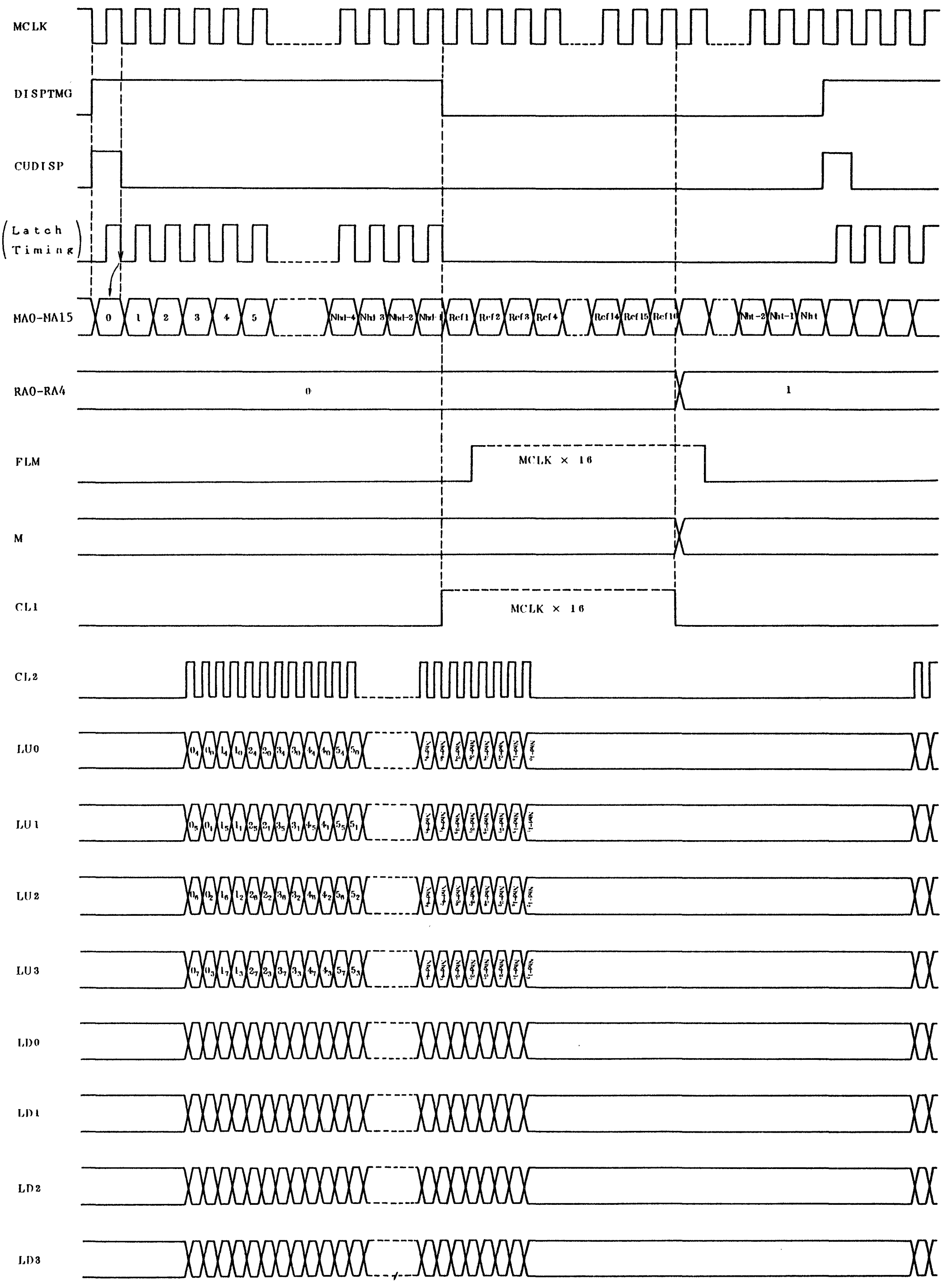
U = up panel address (data), D = down panel address (data), subscript = no. of MD pin, Nhd = horizontal displayed characters, Nht = horizontal total characters

Figure 2-9 Timing Charts (b) Mode 2 (Dual screen wide character)



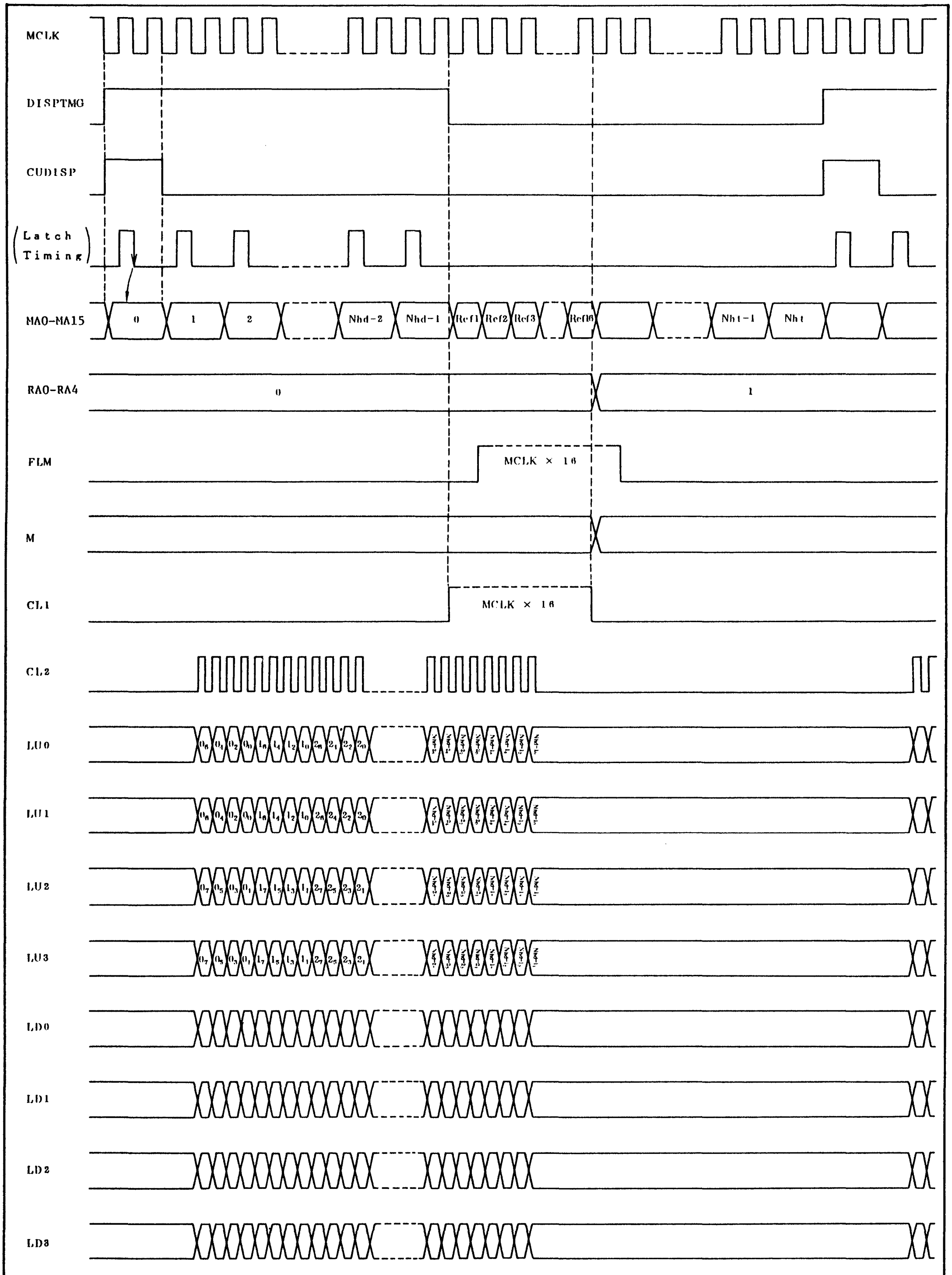
U = up panel address (data), D = down panel address (data), subscript = no. of MD pin,
Nhd = horizontal displayed characters, Nht = horizontal total characters

Figure 2-9 Timing Charts (c) Mode 3, 4 (Dual screen graphic 1 and 2)



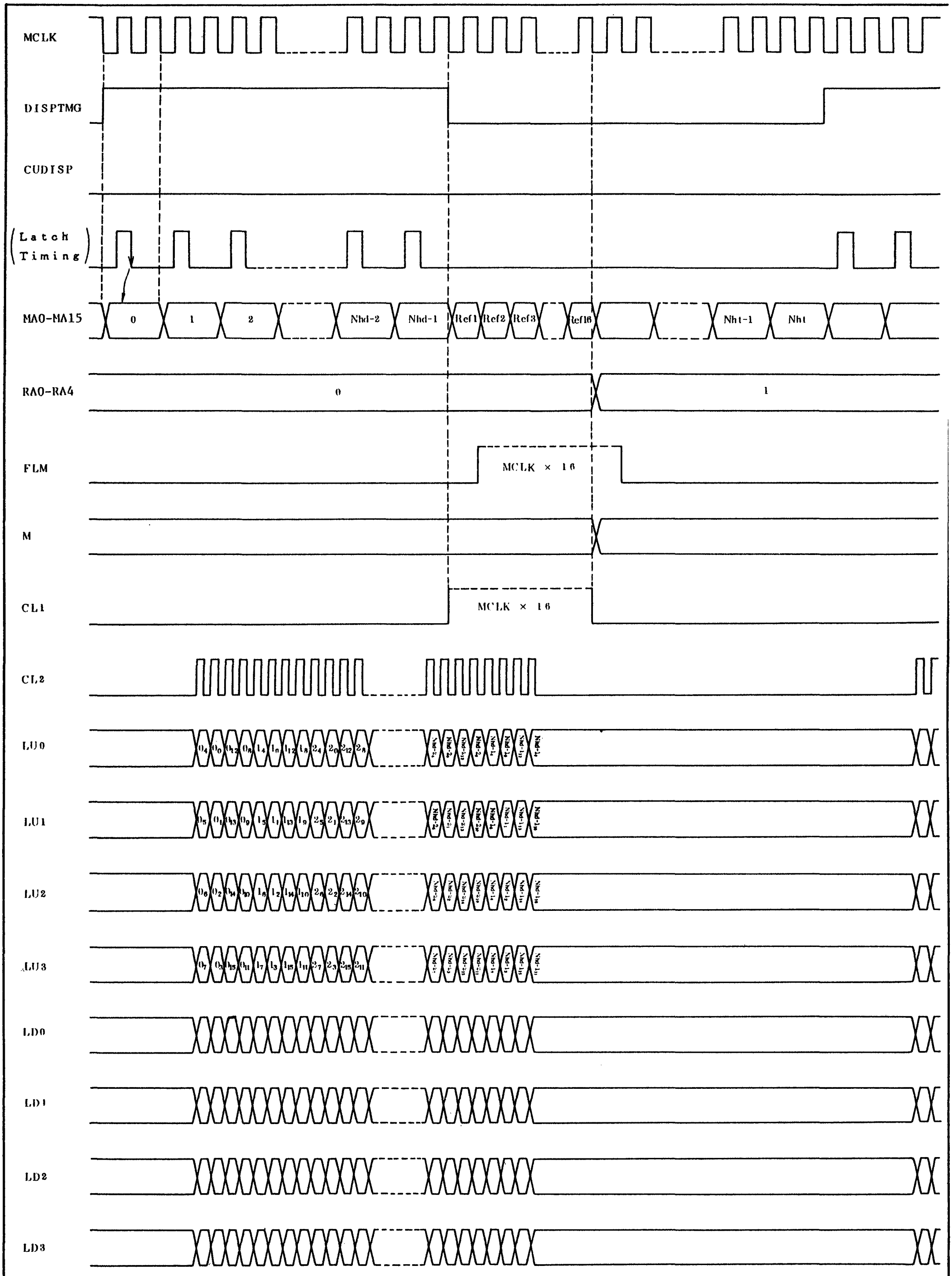
U = up panel address (data), D = down panel address (data), subscript = no. of MD pin,
Nhd = horizontal displayed characters, Nht = horizontal total characters

Figure 2-9 Timing Charts (d) Mode 5 (Single screen normal character)



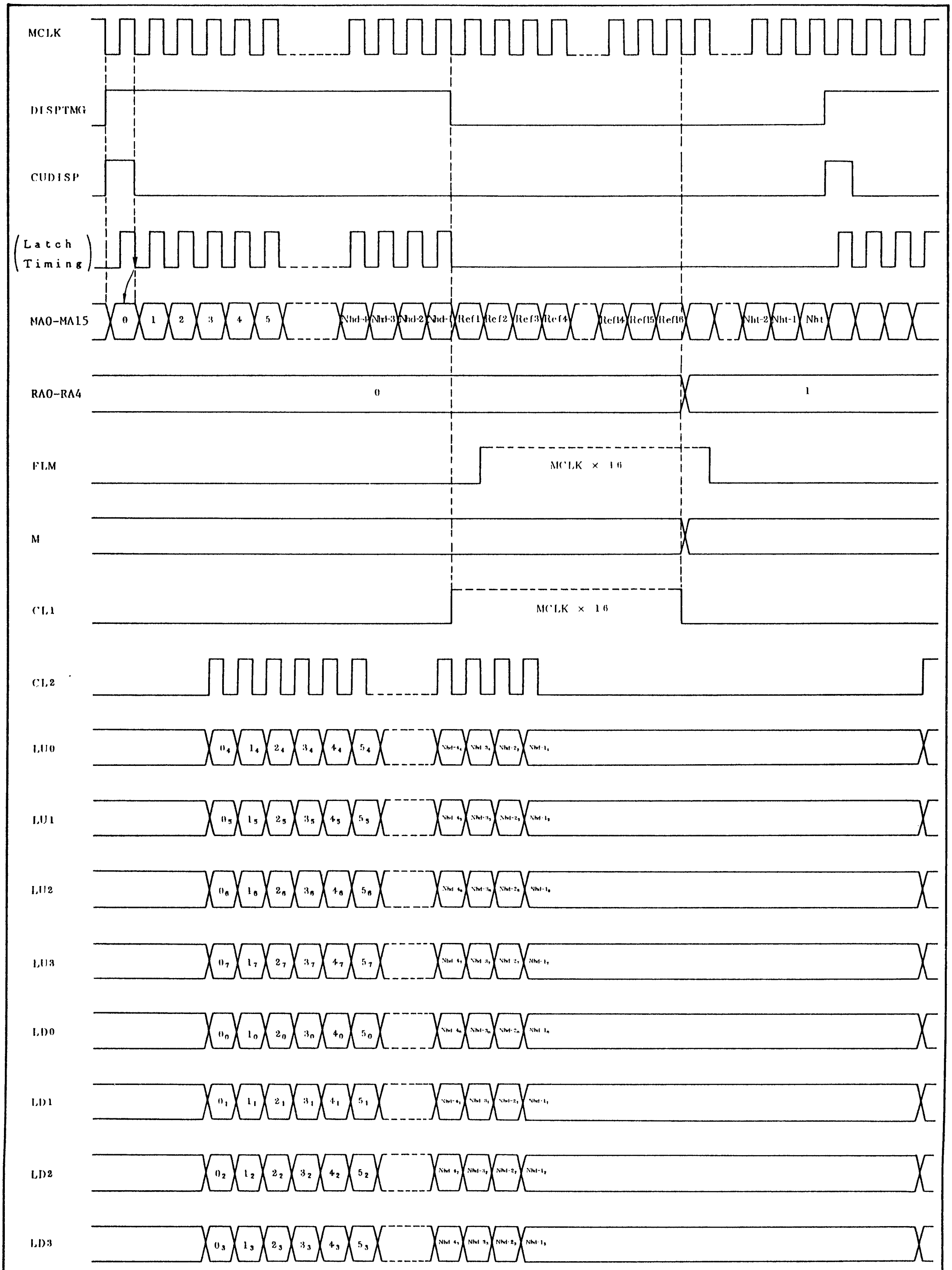
U = up panel address (data), D = down panel address (data), subscript = no. of MD pin,
Nhd = horizontal displayed characters, Nht = horizontal total characters

Figure 2-9 Timing Charts (e) Mode 6 (Single screen wide character)



U = up panel address (data), D = down panel address (data), subscript = no. of MD pin,
Nhd = horizontal displayed characters, Nht = horizontal total characters

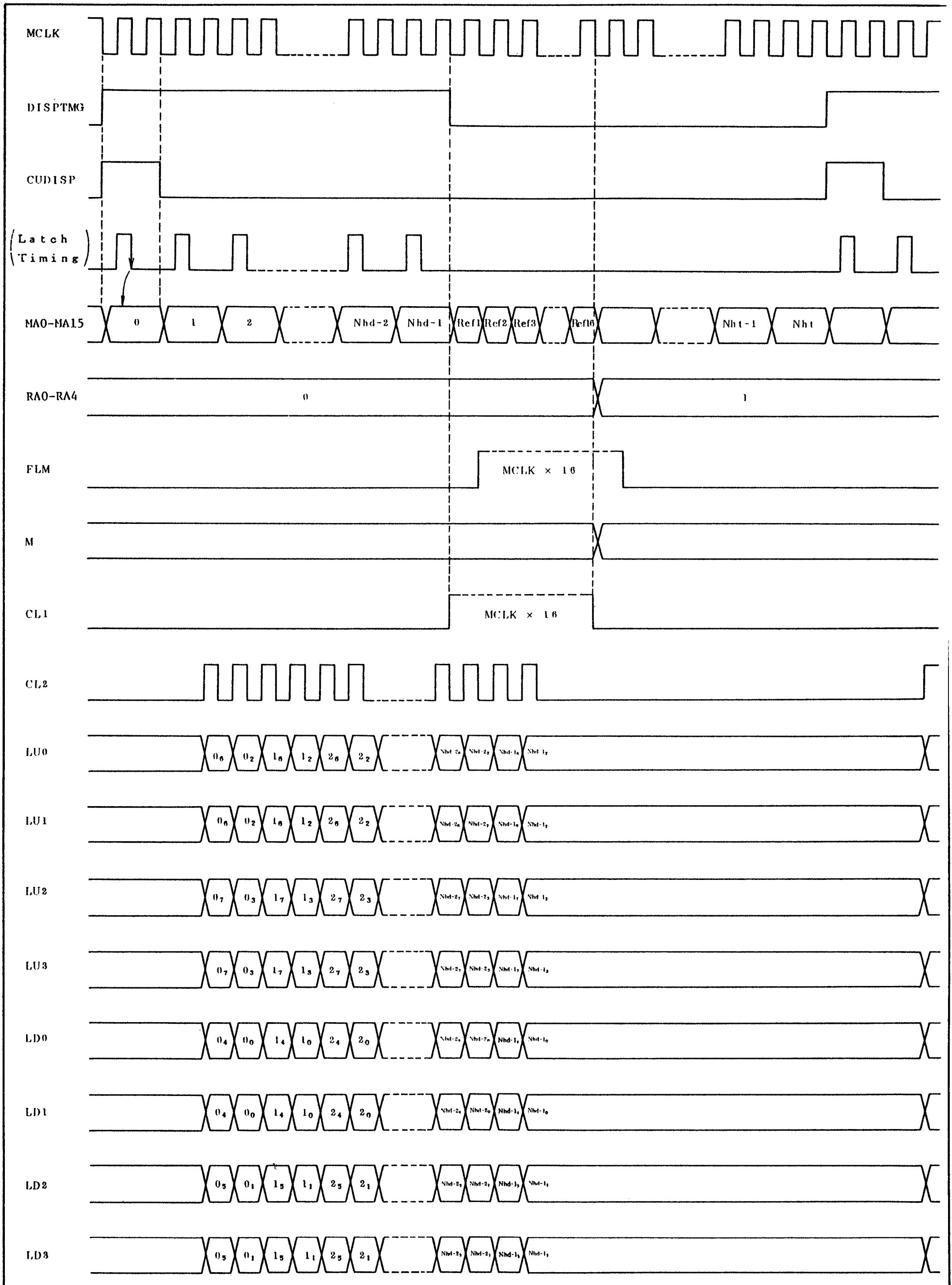
Figure 2-9 Timing Charts (f) Mode 7, 8 (Single screen graphic 1 and 2)



U = up panel address (data), D = down panel address (data), subscript = no. of MD pin,

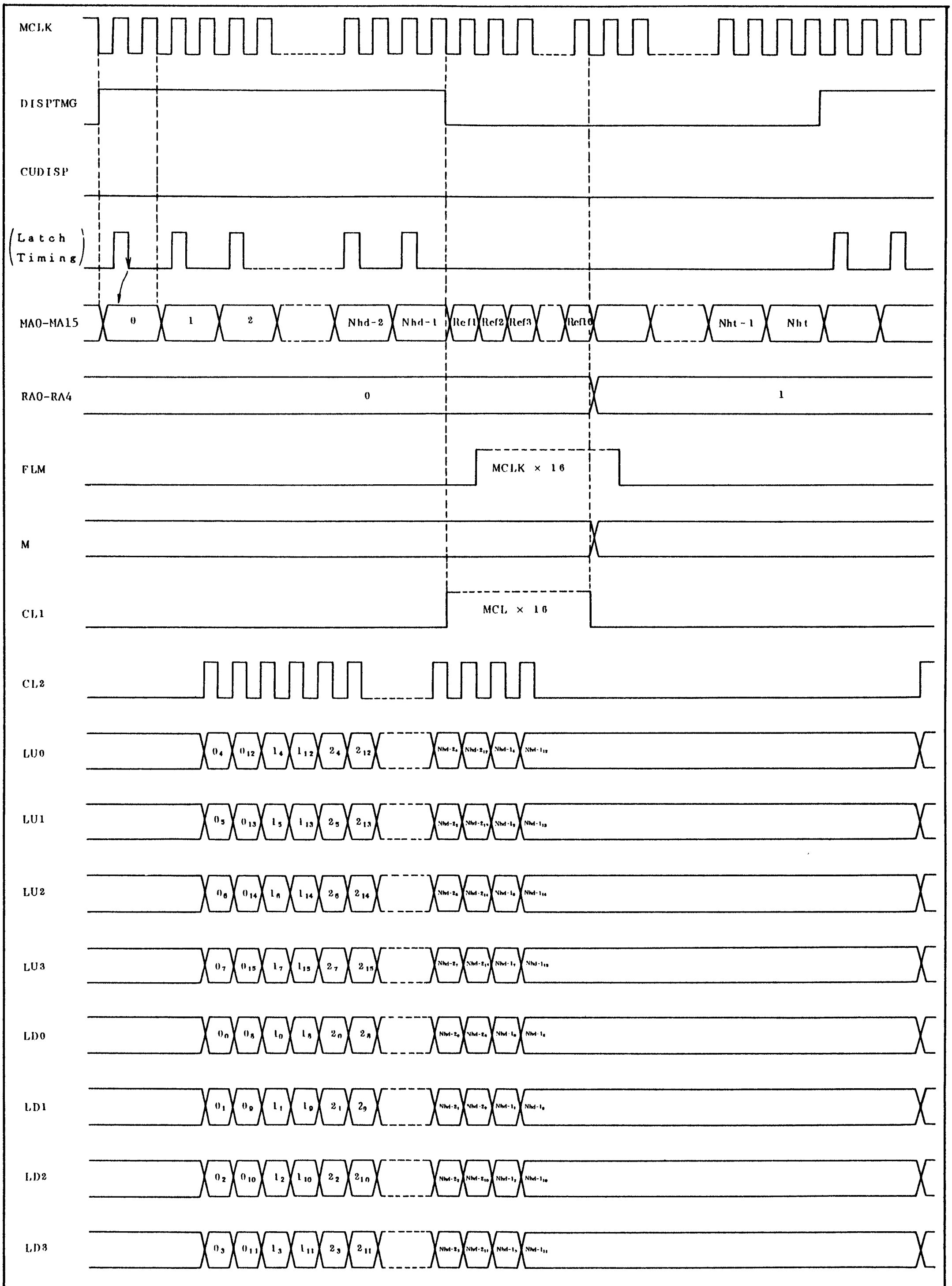
Nhd = horizontal displayed characters, Nht = horizontal total characters

Figure 2-9 Timing Charts (g) Mode 9 (8-bit normal character)



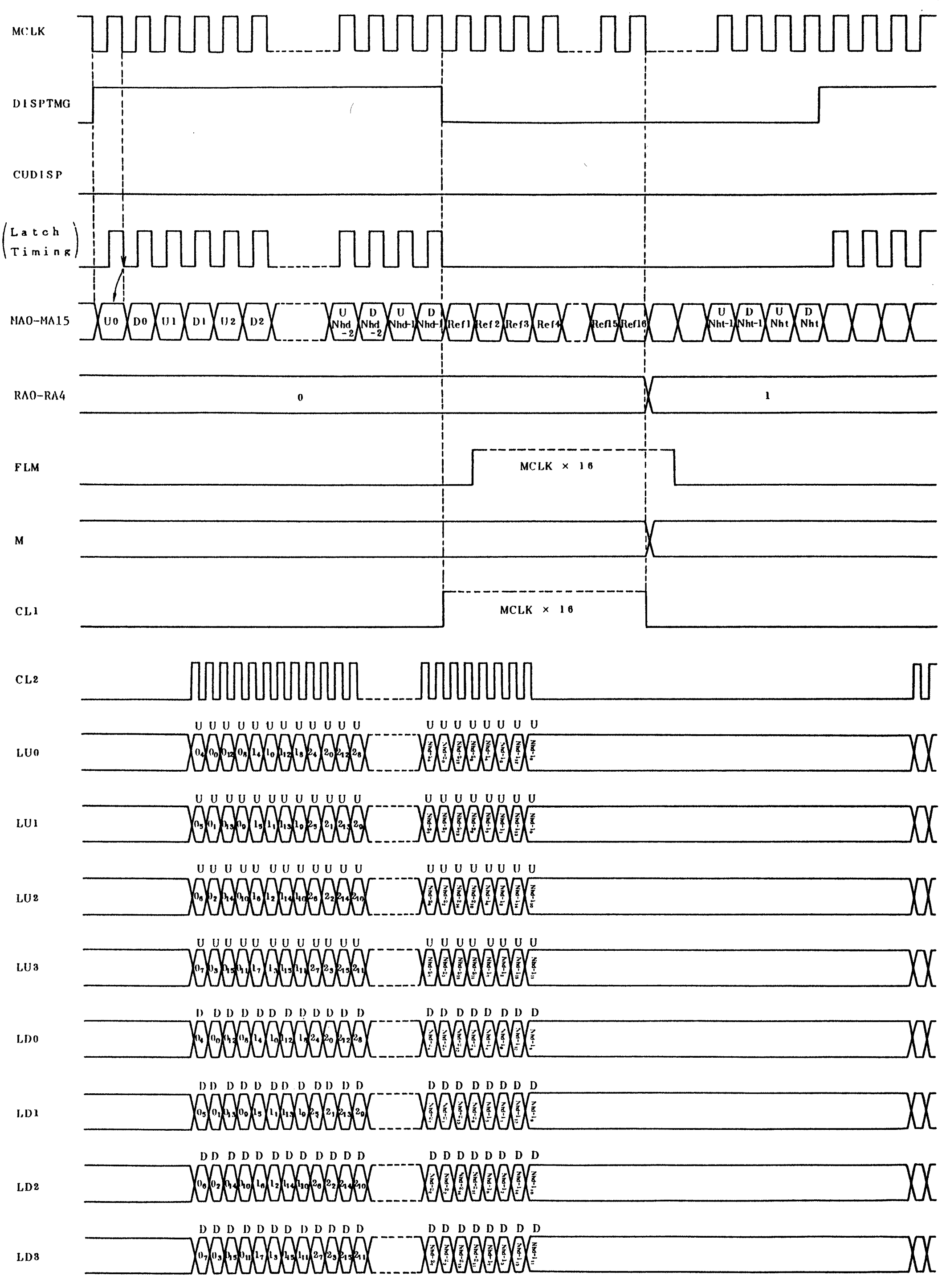
U = up panel address (data), D = down panel address (data), subscript = no. of MD pin,
Nhd = horizontal displayed characters, Nht = horizontal total characters

Figure 2-9 Timing Charts (h) Mode 10 (8-bit wide character)


MCLK
DISPTMG
CUDISP
(Latch Timing)
MA0-MA15
0
1
2
Nhd-2
Nhd-1
Ref1
Ref2
Ref3
Ref16
Nht-1
Nht
RA0-RA4
0
1
FLM
MCLK × 16
M
CL1
MCL × 16
CL2
LU0
0₄ 0₁₂ 1₄ 1₁₂ 2₄ 2₁₂ Nhd-2₄ Nhd-2₁₂ Nhd-1₄ Nhd-1₁₂
LU1
0₅ 0₁₃ 1₅ 1₁₃ 2₅ 2₁₃ Nhd-2₅ Nhd-2₁₃ Nhd-1₅ Nhd-1₁₃
LU2
0₆ 0₁₄ 1₆ 1₁₄ 2₆ 2₁₄ Nhd-2₆ Nhd-2₁₄ Nhd-1₆ Nhd-1₁₄
LU3
0₇ 0₁₅ 1₇ 1₁₅ 2₇ 2₁₅ Nhd-2₇ Nhd-2₁₅ Nhd-1₇ Nhd-1₁₅
LD0
0₀ 0₈ 1₀ 1₈ 2₀ 2₈ Nhd-2₀ Nhd-2₈ Nhd-1₀ Nhd-1₈
LD1
0₁ 0₉ 1₁ 1₉ 2₁ 2₉ Nhd-2₁ Nhd-2₉ Nhd-1₁ Nhd-1₉
LD2
0₂ 0₁₀ 1₂ 1₁₀ 2₂ 2₁₀ Nhd-2₂ Nhd-2₁₀ Nhd-1₂ Nhd-1₁₀
LD3
0₃ 0₁₁ 1₃ 1₁₁ 2₃ 2₁₁ Nhd-2₃ Nhd-2₁₁ Nhd-1₃ Nhd-1₁₁

U = up panel address (data), D = down panel address (data), subscript = no. of MD pin,
Nhd = horizontal displayed characters, Nht = horizontal total characters

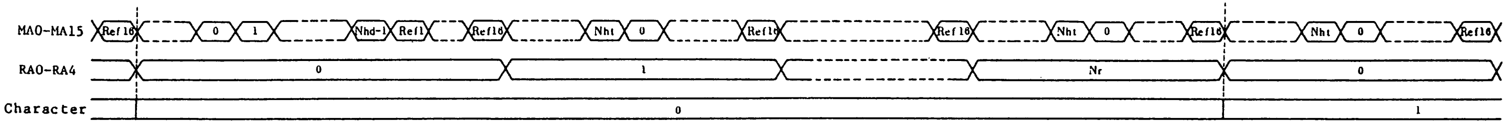
Figure 2-9 Timing Charts (i) Mode 11, 12 (8-bit graphic 1 and 2)



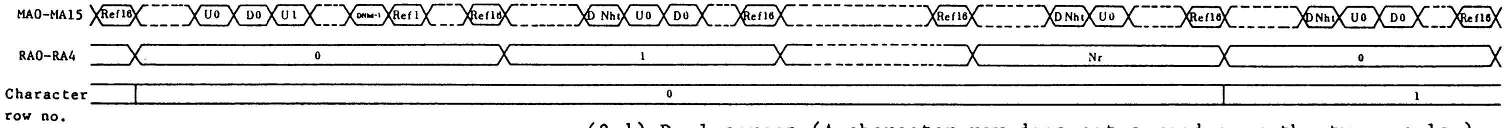
U = up panel address (data), D = down panel address (data), subscript = no. of MD pin,
Nhd = horizontal displayed characters, Nht = horizontal total characters

Figure 2-9 Timing Charts (j) Mode 13 (Large screen)

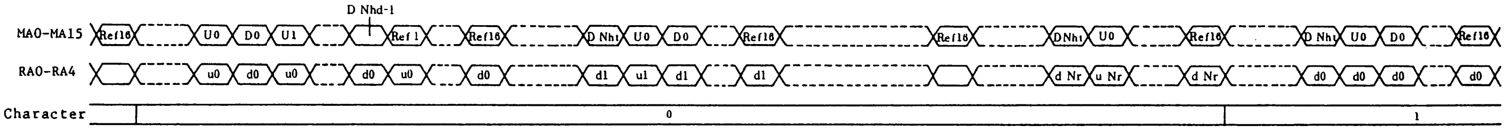
Figure 2-10 Timing Chart of Raster Signal and Character Row Periods



(1) Single screen



(2-1) Dual screen (A character row does not spread over the two panels.)



(2-2) Dual screen (A character row spreads over the two panels.)

U, u = up panel data

D, d = down panel data

3. CALCULATION OF CLOCK FREQUENCY

3.1 Calculation of DCLK

3.1.1 In asynchronous frame buffer access

LCTC operation clock frequency (DCLK) is specified depending on density of information on a screen and MPU memory access time.

The following shows how to calculate DCLK minimum frequency when the MPU is given top priority in accessing a frame buffer, that is, asynchronous access.

The symbols used in the following expressions are:

f_{DCLK}: DCLK frequency (Hz)
f_F: frame frequency (Hz)

Number of horizontal and vertical dots are defined as shown in figure 3-1.

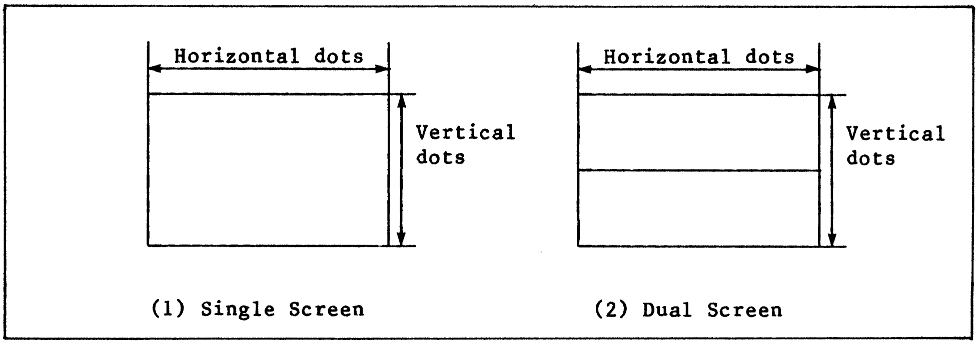
(1) All modes except mode 13

$$f_{DCLK} = \frac{\text{number of horizontal dots}}{8} + \frac{16}{2^*} \times \langle \text{number of vertical dots} \rangle \times f_F \times 4$$

* 16 is divided by 2 only in dual screen modes.

(2) Mode 13

$$f_{DCLK} = \frac{\text{number of horizontal dots}}{16} + 8 \times \langle \text{number of vertical dots} \rangle \times f_F \times 4$$



(1) Single Screen

(2) Dual Screen

Figure 3-1 Screen Configuration and Definition of Number of Dots

3.1.2 In synchronous frame buffer access

There are two methods for the MPU to access a frame buffer synchronously with the LCTC. One uses DISPTMG signal and the other uses cycle-steal.

This section first describes how to calculate DCLK when the MPU accesses a frame buffer with DISPTMG signal.

LCTC timing for one display period includes a time interval for which LCTC does not access memory. During this period the MPU can access memory.

Figure 3-2 shows the timing diagram for 1 raster period. This period's components are listed in table 3-1.

Table 3-1 1 Raster Period

No.	Item	DISPTMG	CL1	Period
1	LCTC Memory Access Time	High	Low	$n \cdot T_{DCLK} \cdot Nhd$
2	DRAM Refresh Time	Low	High	$64 \cdot T_{DCLK}$
3	MPU Memory Access Time	Low	Low	$n \cdot T_{DCLK} \cdot (Nht + 1 - Nhd) - 64 \cdot T_{DCLK}$

Notes: 1. Nhd = number of horizontal displayed characters
Nht = total number of horizontal characters (data to be written)
T_{DCLK} = DCLK period

2. n = constant

Relation between Mode No. and Constant n

Mode No.	Constant n
5, 9	4
1, 6, 7, 8, 10, 11, 13	8
2, 3, 4	16

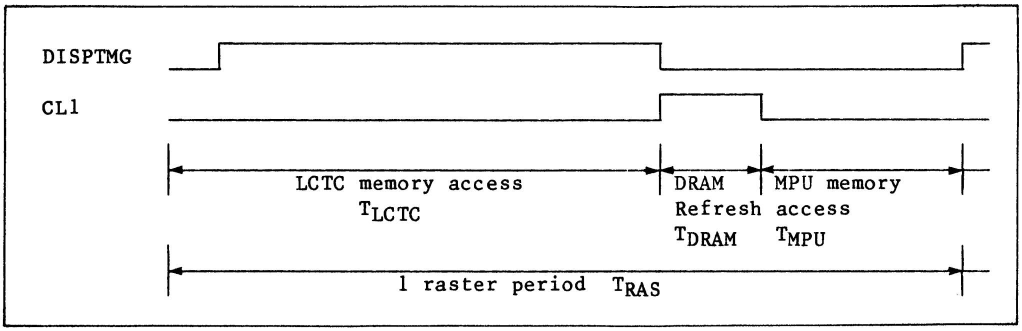


Figure 3-2 LCTC 1 Raster Period

There is the following relation between T_{RAS}, T_F (frame time), and Nd (multiplexing duty ratio, the set value in (R19) and (R20)).

$$T_F = n \cdot T_{DCLK}(Nht + 1)(Nd + 1)$$

Thus the following expression is derived from the relation.

$$T_{DCLK} = \left(\frac{T_F}{Nd + 1} - T_{MPU} \right) \cdot \frac{1}{n \cdot Nhd + 64}$$

T_F depends on the characteristics of liquid crystal, and Nhd and Nd depend on screen size as explained in chapter 1. Therefore, the value of T_{DCLK} is specified by T_{MPU}.

T_{MPU} depends on software and on the operation speed of the MPU. Refer to "5.1 Basic Application Circuit," which gives an example.

If T_{DCLK} is determined, Nht is also determined by the following expression:

$$Nht = \frac{T_F}{n \cdot T_{DCLK} \cdot (Nd + 1)} - 1$$

The user should take into account the following limitations:

(1) $T_{DCLK} \geqq 100$ ns

(2) $1 \leqq Nhd \leqq Nht + 1 \leqq 256$

(3) $Nhd + \frac{64}{n} \leqq Nht + 1$

The following describes how to calculate DCLK when the MPU accesses a frame buffer using cycle-steal.

DCLK frequency depends on the actual circuit as well as screen configuration. Refer to "5.2 CRTC Compatible Board," which gives an example of a concrete circuit using cycle-steal, and the register values.

Generally, DCLK signal should be synchronous with the MPU basic clock in cycle-steal mode. Its frequency must also be higher then its frequency when a frame buffer is accessed asynchronously.

3.1.3 Other limitations

DCLK frequency determines the frequency of memory address (MA) change and shift clock of an LCD driver (CL2). Thus you should check the access time of the memory you use and the relation between the operation clock of an LCD driver. Refer to "3.3 Calculation of Shift Clock (CL2)."

For example, if HD61104 is used as a segment driver, the maximum frequency of DCLK is 7 MHz in modes 5, 6, 7, 8, 13, and 10 MHz in the other modes.

3.2 Calculation of M Clock (MCLK)

MCLK output frequency (f_{MCLK}) is always a quarter of DCLK input frequency (f_{DCLK}). However, the frequency of memory address (MA) change depends on modes.

Table 3-2 shows this relation.

Table 3-2 Relation between DCLK, MCLK, and MA Change

Mode No.	f_{MCLK}	MA Change Frequency
1,2,3,4,5,9,13	1/4 f_{DCLK}	1/4 f_{DCLK}
6,7,8,10,11,12	1/4 f_{DCLK}	1/8 f_{DCLK}

3.3 Calculation of Shift Clock (CL2)

Table 3-3 shows the relation between CL2 output frequency and DCLK input frequency. The user should check the relation between them and the operation frequency of an LCD driver.

Table 3-3 Shift Clock Frequency

Mode No.	Shift Clock Frequency
1,2,3,4,9,10,11,12	1/4 f_{DCLK}
5,6,7,8,13	1/2 f_{DCLK}

3.4 Calculation of Data Transfer Speed

Data transfer speed means how many dots per second the LCTC can read from the memory and display on an LCD screen.

For example, the following data transfer speed is required when performing display with frame frequency of 70 Hz on an LCD screen of 640 x 200 dots:

$$640 \times 200 \times 70 = 8{,}960{,}000 \text{ (bits/sec)}$$

When the LCTC is used in wide character mode, the quantity of data read from the memory is not the same as that of data displayed on an LCD screen. This is because the LCTC transfers the same signal twice to an LCD driver in wide character mode, in which the display is doubled in width. Figure 3-3 shows this relation.

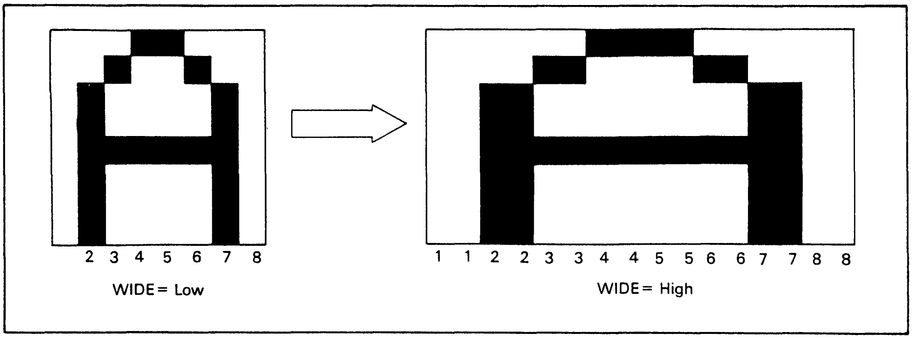


Figure 3-3 Wide Character Display

Table 3-4 shows the relation between data transfer speed and DCLK frequency.

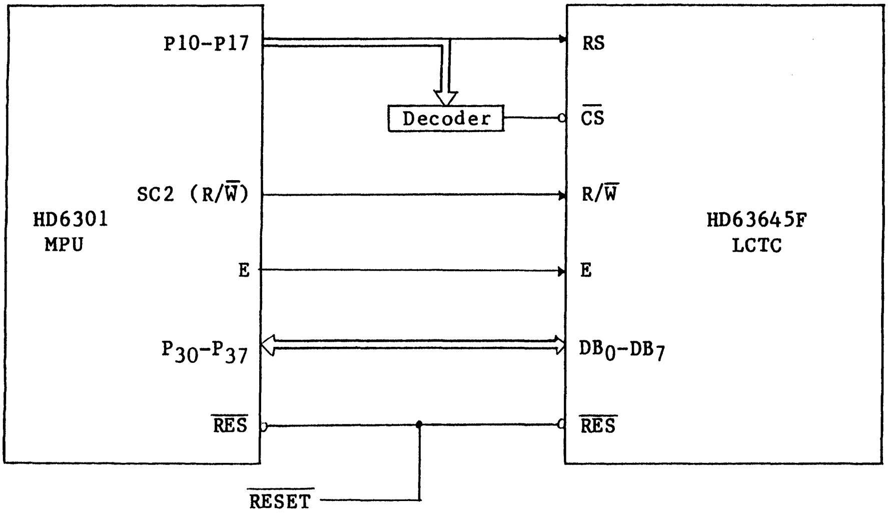
Table 3-4 Data Transfer Speed

Mode No.	Data Transfer Speed (Mbits/sec) Reading from Memory	Displaying on LCD
2,6,10	f_{DCLK}	$2 \cdot f_{DCLK}$
1,3,4,5,7,8,9,11,12	$2 \cdot f_{DCLK}$	$2 \cdot f_{DCLK}$
13	$4 \cdot f_{DCLK}$	$4 \cdot f_{DCLK}$

Note: f_{DCLK} = Input frequency of DCLK pin (MHz)

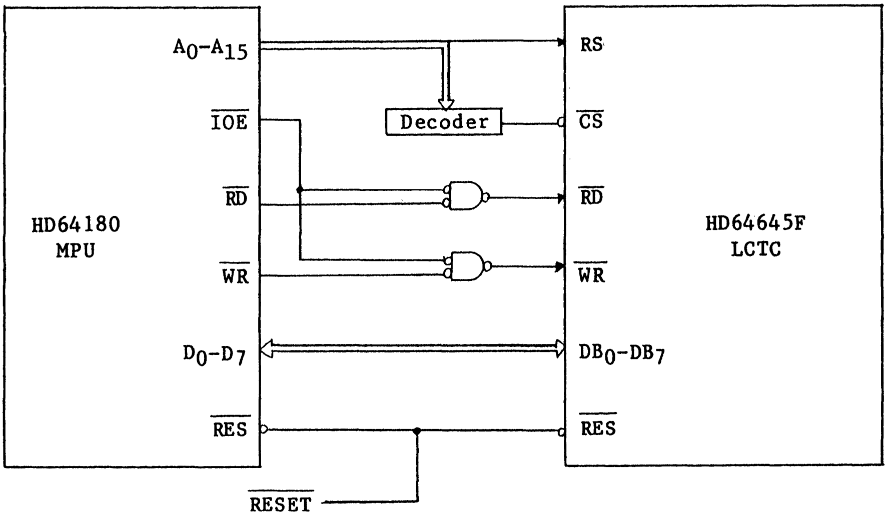
4. INTERFACE

4.1 MPU Interface



Note: HD6301 is set in mode 5. P10-P17 are used as output ports, and P_{30}-P_{37} as data buses. SC2 outputs $R/\overline{W}$ here.

(a) Interface of HD63645F to HD6301



Note: In 80-family MPUs, I/O space is separate from memory space in software. Thus the LCTC, an I/O peripheral, needs the ANDed interface signals and $\overline{IOE}$. So $\overline{IOE}$ and $\overline{RD}$, and $\overline{IOE}$ and $\overline{WR}$ should be ORed to satisfy t_{AS}, the timing of $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$.

(b) Interface of HD64645F to HD64180

Figure 4-1 Interface to MPU

4.2 How to Access Frame Buffer

4.2.1 Asynchronous frame buffer access

In an LCD system with the LCTC, the LCTC accesses a frame buffer using the memory addresses (MA0-MA15) to refresh the display periodically. The MPU also accesses the frame buffer at changing the display. The MPU accesses in 2 ways; asynchronous access and synchronous access. The former accesses regardless of the display state, and the latter accesses only during non-display time.

Figure 4-2 shows an example of asynchronous access. When the address of the MPU specifies a frame buffer in asynchronous access, the output of the address multiplexer is switched to the MPU address bus side. Thus a part of the display may then flash momentarily.

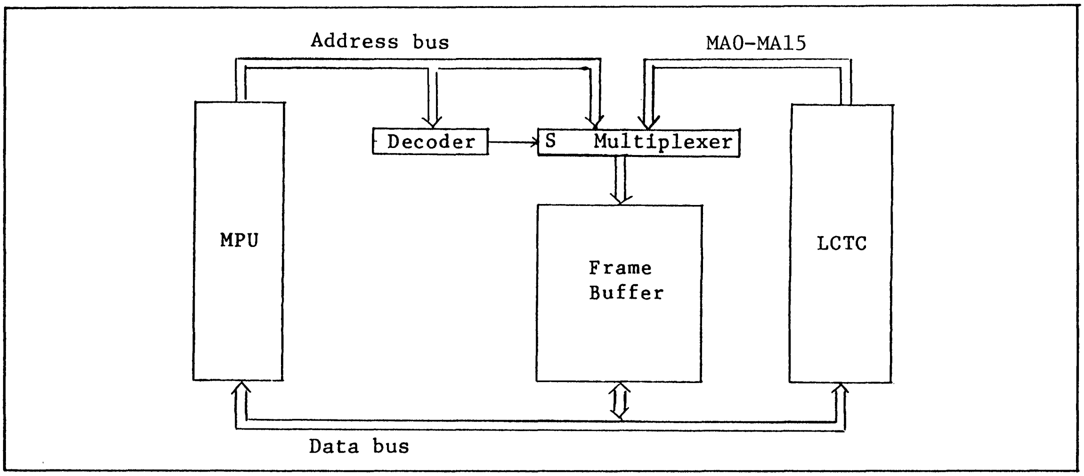


Figure 4-2 Asynchronous Frame Buffer Access

4.2.2 Synchronous frame buffer access I

Figure 4-3 shows an example of synchronous access. Here the MPU reads the DISPTMG output and accesses only while DISPTMG is low (horizontal retrace period). In synchronous access, display does not flash since the MPU access does not compete with the display access.

"5.1 Basic Application Circuit" shows a circuit example using this access method and a register setting example.

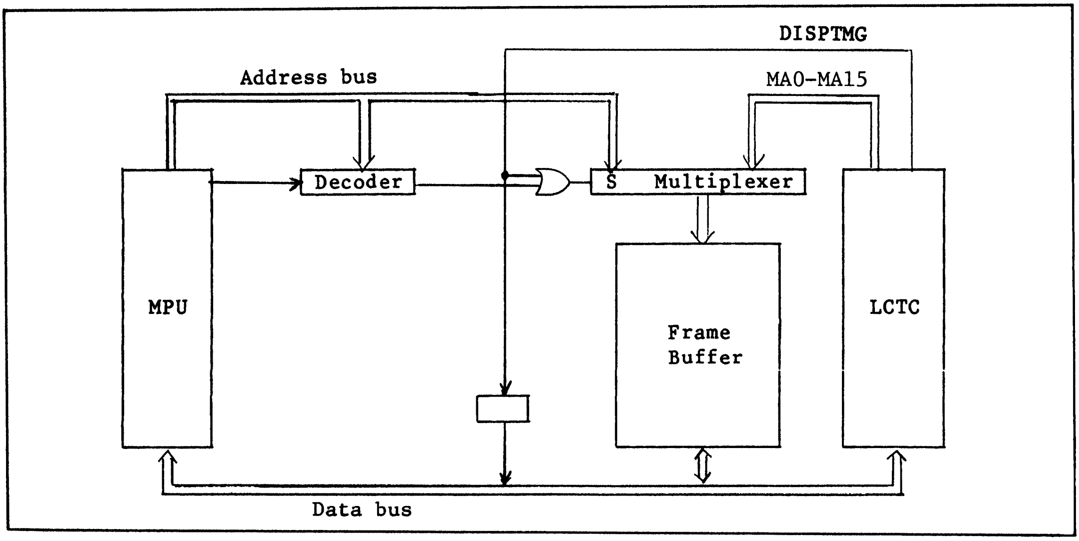


Figure 4-3 Synchronous Frame Buffer Access (1)

4.2.3 Synchronous frame buffer access II (Cycle-steal)

Figure 4-4 shows another example of synchronous access. Here a character clock time is shared between the MPU access and the display access. In the MPU access, READY signal stops E clock of the MPU, in order to give the MPU enough time to access a frame buffer. This method is called cycle-steal.

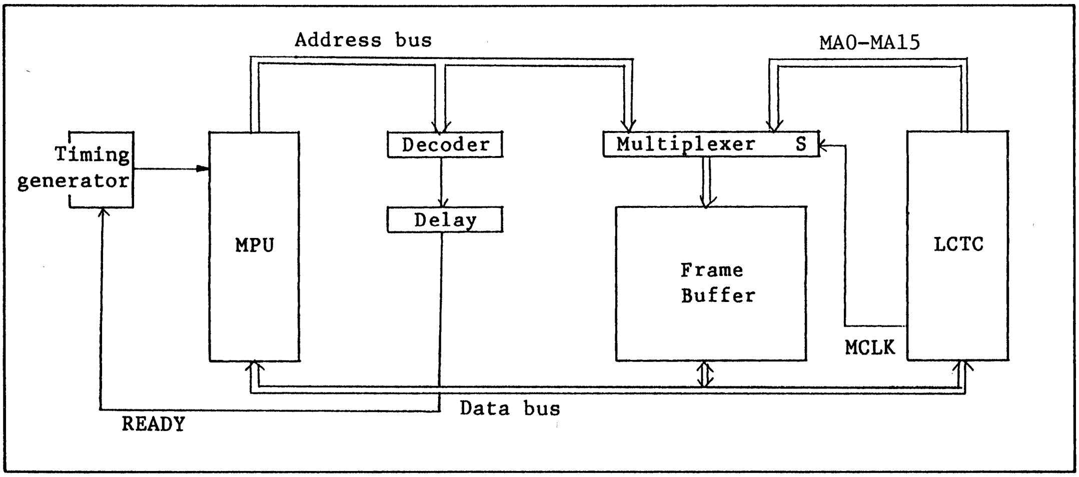
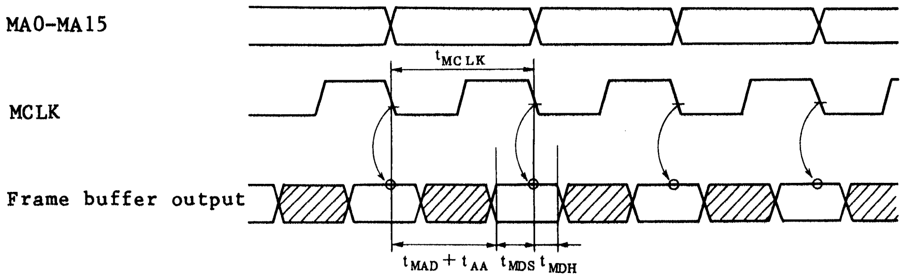


Figure 4-4 Synchronous Frame Buffer Access (2)

In this method the MPU access alternates with the display access, which causes no flashing. Besides, there is no loss of time since checking DISPTMG signal is not necessary. Therefore, this method suits a large screen of 640 x 400 dots. However, an external circuit such as a timing generator is required.

Figure 4-5 shows the timing chart in mode 5. The user needs to select the memory satisfying the following inequality.

$$t'_{LCTC} > t_{MDA} + t_{AA} + t_{MDS}$$



Note: t'_{LCTC} = time when the LCTC uses the frame buffer
t'_{MPU} = time when the MPU uses the frame buffer
t'_{MAD} = MA0-MA15 delay time of the LCTC
t'_{AA} = address access time of the memory
t'_{MDS} = MD0-MD15 setup time of the LCTC
t'_{MDH} = MD0-MD15 hold time of the LCTC

Figure 4-5 Basic Timing of Cycle-Steal

The MPU latches data in a frame buffer once and then reads it. This applies to the other modes. Refer to "2.5 Timing Charts", which shows the timing chart of MA0-MA15, MCLK, and data latch timing.

Also refer to "5.2 CRTC Compatible Board," which shows an application using cycle-steal and its timing.

5. LCTC APPLICATION CIRCUIT EXAMPLE

5.1 Basic Application Circuit

5.1.1 Circuit specifications

Figure 5-1 shows a basic application circuit using the LCTC. Figure 5-2 shows its block diagram and data flow. Table 5-1 lists its specifications.

Table 5-1 Specifications of Basic Application Circuit

Item	Specifications
Display Format	Dual screen character display (Mode 1 or Mode 2)
Character Font	8 x 8 dots
DCLK Frequency	8 MHz
Number of Displayed Characters	80 characters x 25 rows = 2,000 characters
Frame Buffer Access Mode	Synchronous access (Reading DISPTMG)
Frame Buffer	4 kbytes (SRAM HM6116 x 2)

Address Allocation	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
Frame buffer	0	0	0	1	*	*	*	*	*	*	*	*	*	*	*	*
LCTC address register	0	0	1	0	x	x	x	x	x	x	x	x	x	x	x	0
LCTC data register	0	0	1	0	x	x	x	x	x	x	x	x	x	x	x	1
DISPTMG register	0	0	1	1	x	x	x	x	x	x	x	x	x	x	x	x

x --- don't care, * --- 0 or 1

Attribute Mode		MD11	MD12	MD13	MD14	MD15
	Cursor inhibit	0	0	0	0	0
	Reverse video	1	1	0	0	0
	Blinking	0	1	0	0	0
	Display inhibit	0	1	0	1	0
	Underline	0	1	0	0	1

Note: Underline --- Lower 2 rasters (the 7th and 8th rasters) of 8 rasters constructing a character row.

5.1.2 Circuit

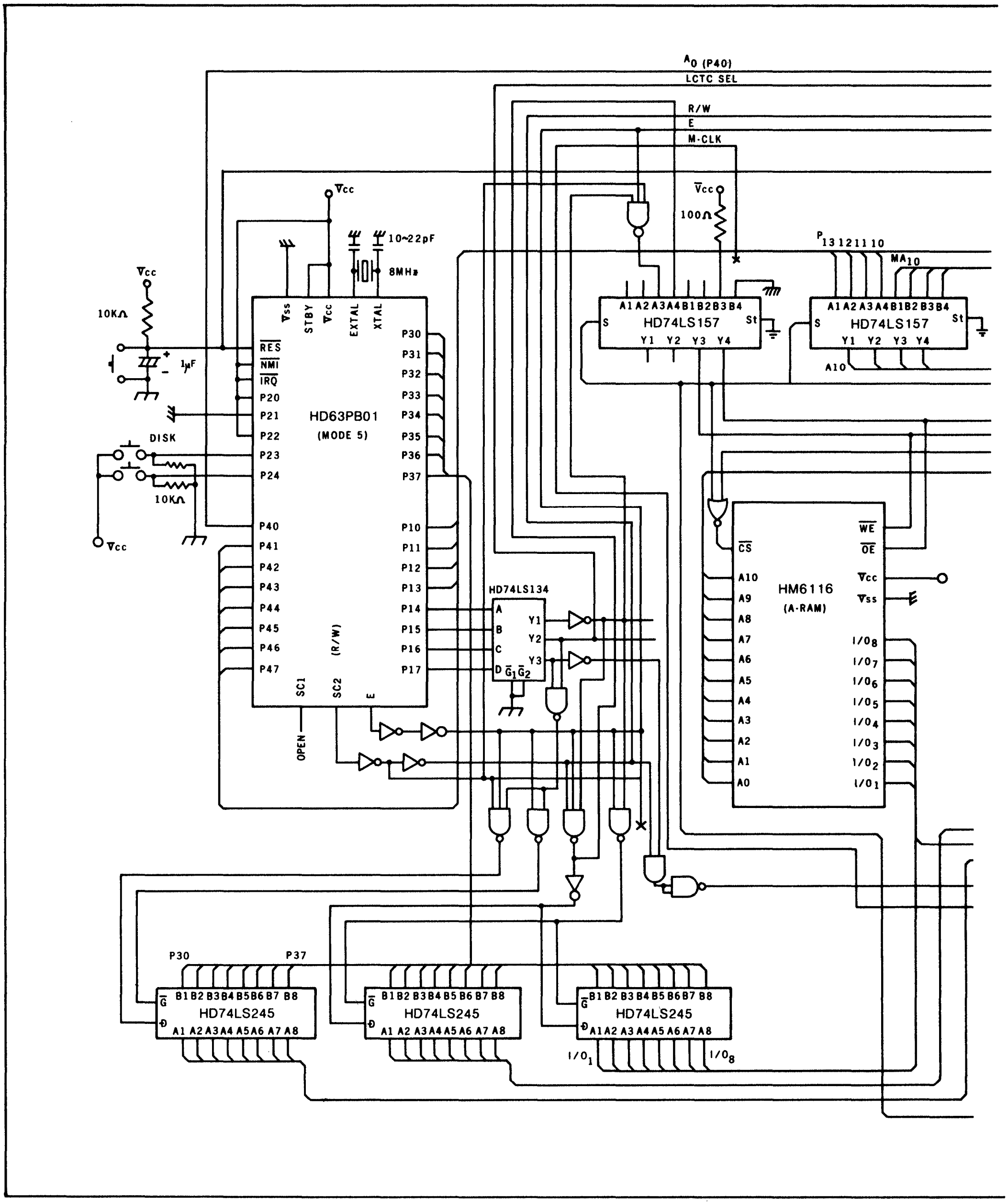
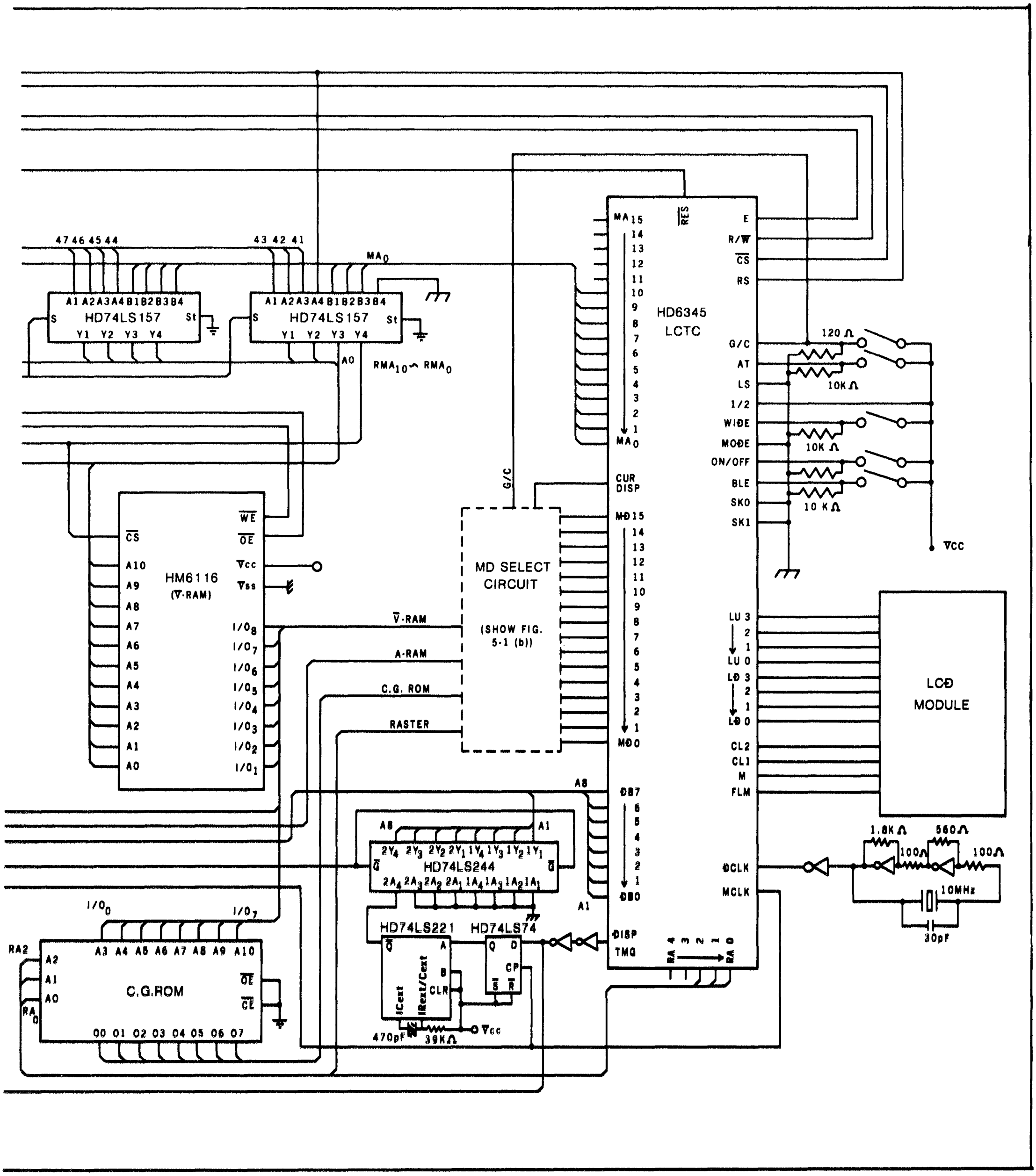


Figure 5-1 (a) Basic Application Circuit


HD74LS157
HD74LS157
A1 A2 A3 A4 B1 B2 B3 B4
Y1 Y2 Y3 Y4
S
St
47 46 45 44
43 42 41
MA0
A0
RMA10 ~ RMA0
HM6116
(V-RAM)
CS
WE
OE
Vcc
Vss
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
I/O8
I/O7
I/O6
I/O5
I/O4
I/O3
I/O2
I/O1
MD SELECT CIRCUIT
(SHOW FIG. 5-1 (b))
G/C
V-RAM
A-RAM
C.G. ROM
RASTER
HD6345
LCTC
MA15
MA0
RES
E
R/W
CS
RS
G/C
AT
LS
1/2
WIDE
MODE
ON/OFF
BLE
SK0
SK1
CUR DISP
MD15
MD0
DB7
DB0
DISP
TMG
RA4 3 2 1 RA0
LU3
LU0
LD3
LD0
CL2
CL1
M
FLM
ΦCLK
MCLK
120 Ω
10K Ω
10K Ω
10 K Ω
Vcc
LCD
MODULE
1.8K Ω
560 Ω
100 Ω
100 Ω
10MHz
30pF
A8
A1
HD74LS244
2Y4 2Y3 2Y2 2Y1 1Y4 1Y3 1Y2 1Y1
2A4 2A3 2A2 2A1 1A4 1A3 1A2 1A1
G
HD74LS221
HD74LS74
Q
A
B
CLR
Cext
Rext/Cext
D
CP
S
R
470pF
39K Ω
Vcc
I/O0
I/O7
RA2
RA0
C.G.ROM
A3 A4 A5 A6 A7 A8 A9 A10
A2
A1
A0
OE
CE
O0 O1 O2 O3 O4 O5 O6 O7

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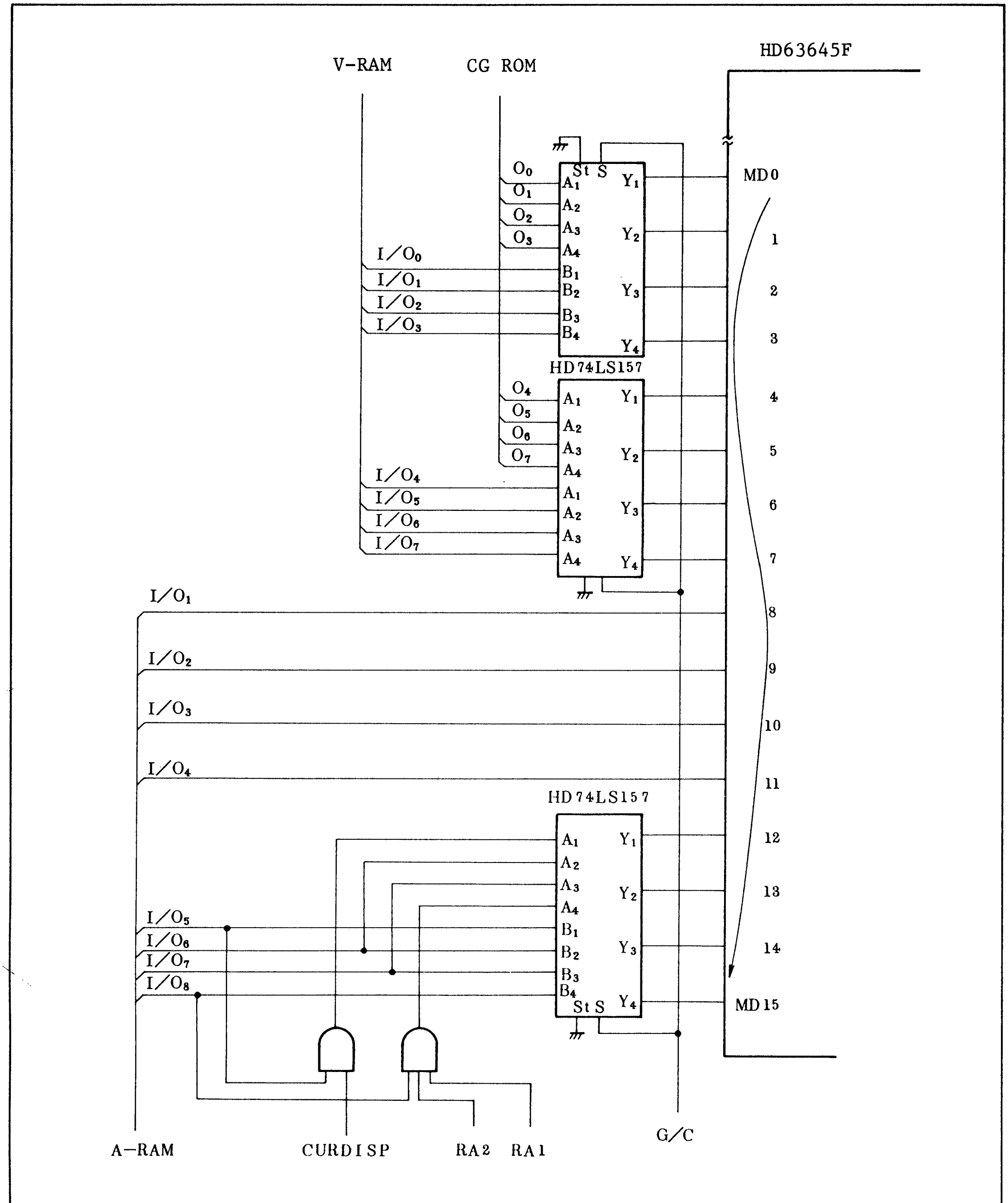


Notes: 1. STROBE pin of HD74LS157 is to be grounded.
2. A cursor is off in character mode unless MD12 (C) is high.

Figure 5-1 (b) Basic Application Circuit (MD Selector)

5.1.3 Circuit description

This circuit synchronously accesses a frame buffer using the DISPTMG signal. It is the most basic display circuit with the LCTC.

On this board, the MPU does not access a frame buffer until it has confirmed that DISPTMG signal is low and that the frame buffer is given to the MPU, by checking the DISPTMG register.

Therefore, the LCTC accesses the buffer for displaying while DISPTMG signal is high, and the MPU accesses the buffer for drawing while DISPTMG is low.

Figure 5-4 shows the timing chart of frame buffer access by the MPU. This is the timing chart when the system configuration is different from the one shown in figure 5-1 (a), which helps understanding of the synchronous access to the frame buffer using DISPTMG signal.

Figures 5-4 (a) and (b) show the timing when the DISPTMG signal of the LCTC connects directly with the DISPTMG register (HD74LS244), not through HD74LS74 and HD74LS221, which differs from the circuit shown in figure 5-1 (a). Figure 5-4 (c) is the timing chart of the same circuit as the one shown in figure 5-1 (a).

In figure 5-4 (a), the operation clock of the MPU is 4 MHz.
Here it takes 16 μs to check that DISPTMG is low and 44 μs to write the first 1-byte data into a frame buffer. Thus, it takes the MPU 60 us in total to write the first 1-byte data. But the period when DISPTMG is low, that is, when a frame buffer is given to the MPU, continues only for 35 us. Therefore, MPU write to a frame buffer overlaps with LCTC read from a frame buffer, which causes flickering of the left part of a screen.

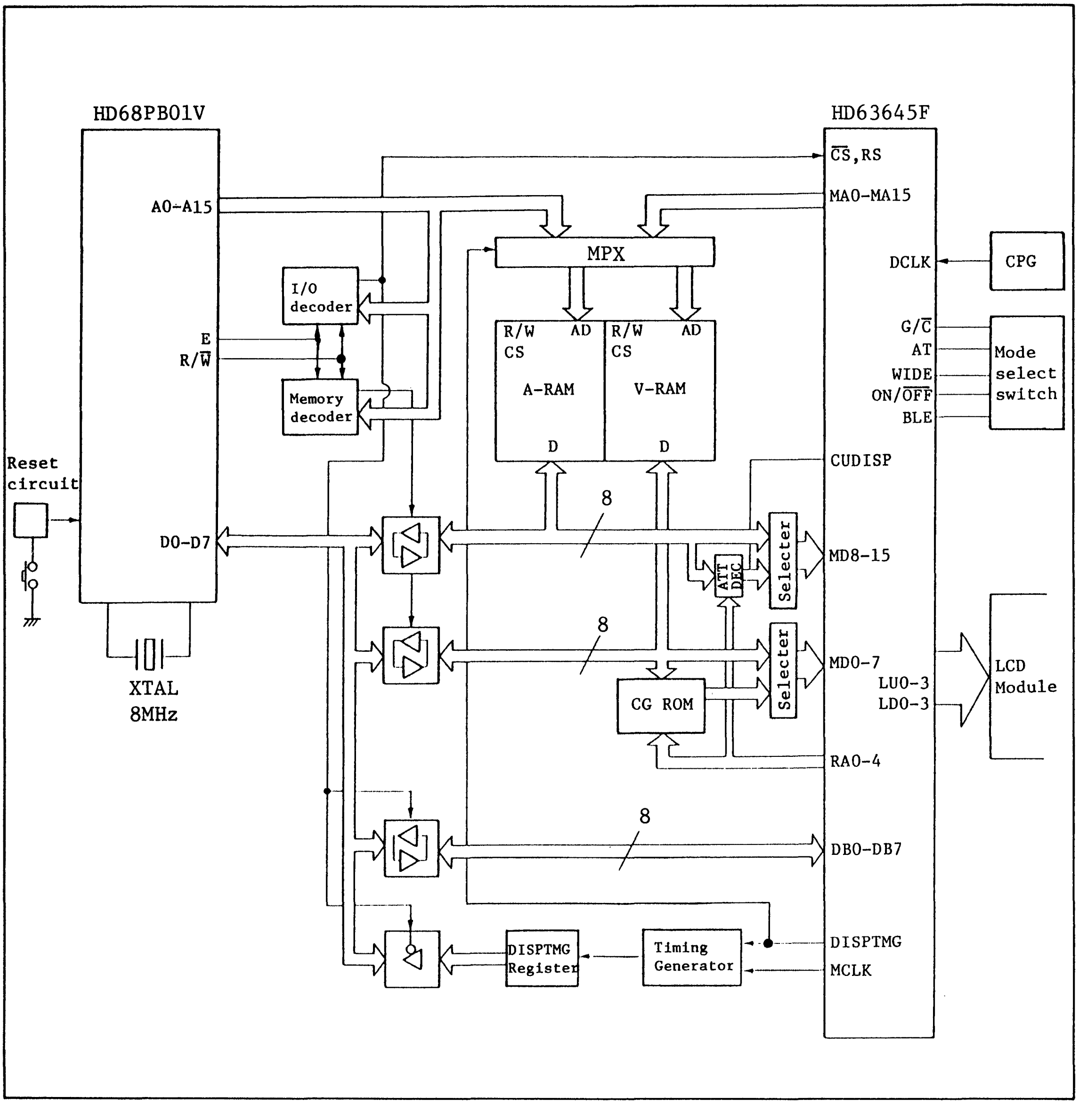


Figure 5-2 Block Diagram of Basic Application Circuit

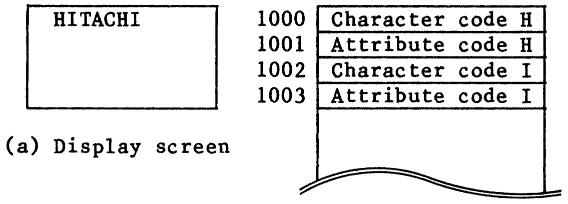
Figure 5-4 (b) shows the timing when the DISPTMG signal connects directly with HD74LS244 and the operation clock of the MPU is 8 MHz. Here it takes 30 us to check the DISPTMG register and write data to a frame buffer. Therefore, MPU finishes writing the first 1-byte data while DISPTMG is low. However, the MPU starts writing the second 1-byte data since DISPTMG continues low for 5 us after writing the first 1-byte data. So, the second MPU write overlaps with LCTC read and the left part of a screen flickers.

Figure 5-4 (c) indicates the case in which the output of HD74LS221, which generates a 13-μs-width pulse starting at the falling edge of DISPTMG, is connected with the DISPTMG register. In this case, since writing is performed just once, there are no flickering on a screen. The width of 13-μs pulse can be obtained by the following expression.

Pulse width = (time of DISPTMG = low) - (time required for MPU write)

In graphic mode, data read from a frame buffer is directly input to MD0-MD15 of the LCTC. However, memory capacity is insufficient and only Q 4-kbyte memory (e.g. 320 x 200 dots) can be displayed.

In character mode, 2 consecutive bytes of addresses are read out at the same time. The first byte is assigned to character code and the second byte to attribute code modifying the character. Figure 5-3 shows memory address assignment.



(a) Display screen

(b) Memory address

Figure 5-3 Memory Address of Basic Application Circuit (In Character Mode)

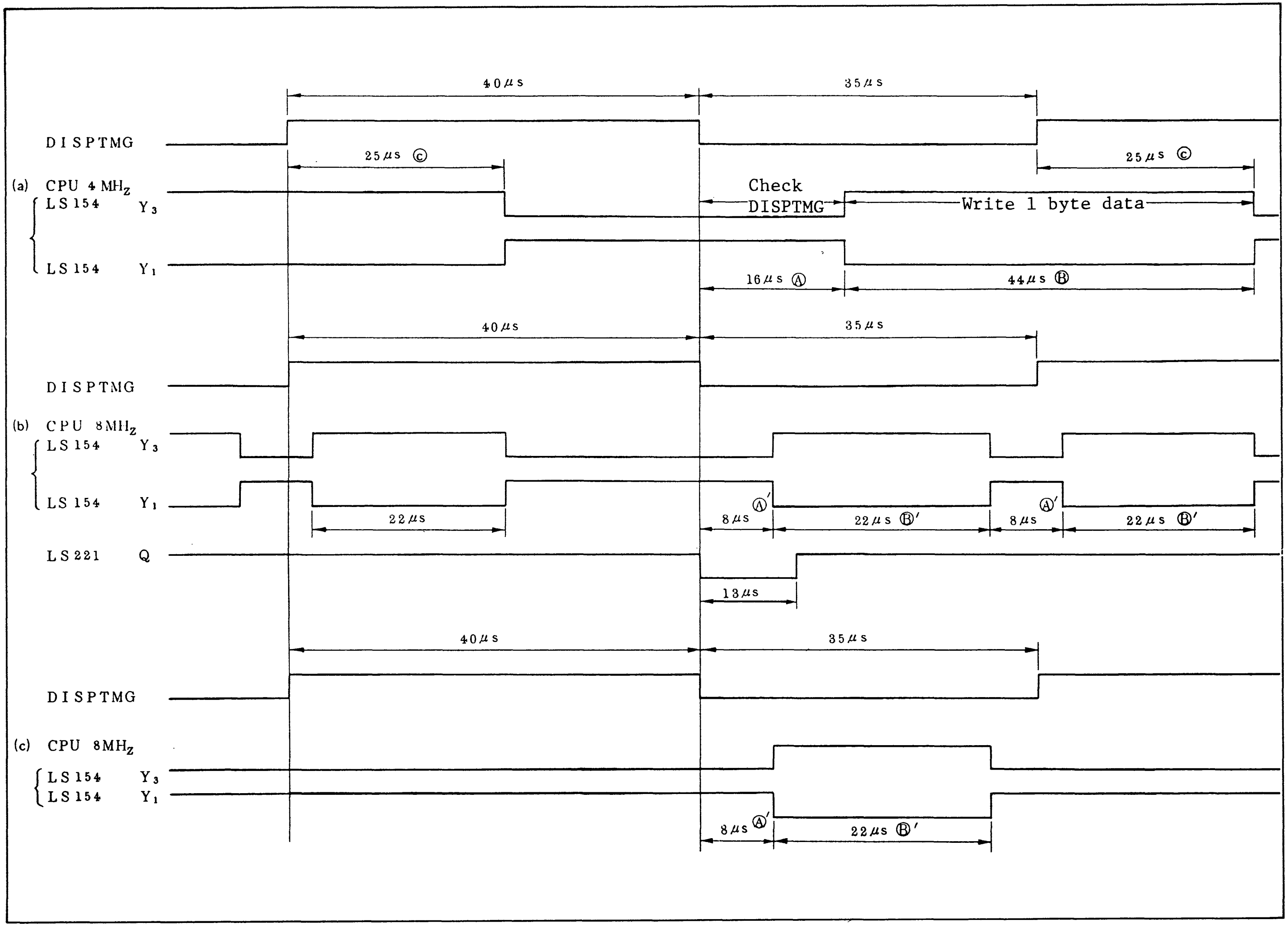


Figure 5-4 Access Timing of Frame Buffer by MPU (Basic Application Circuit)

The low-order byte (= character code) of display data is connected with addresses of character generator (= CG ROM) and is used for reading out the actual character font. Data read out of CG ROM is connected with MD0-MD7 of the LCTC. While the high-order byte (= attribute code) is connected with MD11-MD15 of the LCTC through a converter. In this way, a frame buffer can be considered to be divided into two memories in character mode; one is an attribute RAM (= ARAM) and the other a video RAM (= VRAM). Therefore, Ns expressed as the following expression should be programmed when setting the start address registers of the LCTC (R12, R13).

Ns = <memory address seen from the MPU> x 1/2

Figure 5-5 shows the specifications of attribute codes.

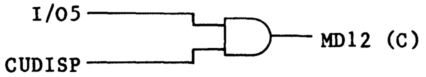
The LCTC modes (graphic/character selection, display on/off, blinking and so on) can be set by controlling the external pins of the LCTC with a toggle switch.

The LCTC can be connected both with a single and a dual screen LCD module. Up to 320 x 200 dots can be displayed in graphic mode, and up to 640 x 200 dots in character mode. When displaying a larger screen, greater RAM capacity is required. Since outputs of the LCTC on this board are connected directly with an LCD module, wires between the LCTC and a module should be short. If the user needs long wires, the outputs of the LCTC must be buffered.

On this board, since the MPU is an HD6301V, HD63645F, which has a 68-family bus interface, is adopted. When the MPU has a 80-family bus interface, HD64645F, which has 80-family bus interface, facilitates designing the system. Refer to "4.1 MPU Interface".

R: reverse video (MD11)
Directly inputs I/O4 of ARAM.

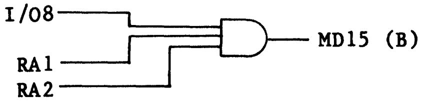
C: cursor (MD12)

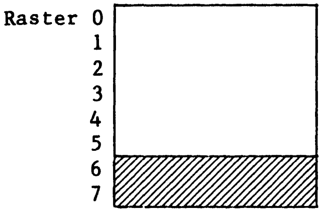


The AND of CUDISP and I/O5 of ARAM is taken. In order to display a cursor on the specified character, the fifth bit of the attribute code modifying the character should be 1.

BL: blinking (MD13)
Directly inputs I/O6 of ARAM.

B: black (MD15)





The AND of RA1, RA2, and I/O8 of ARAM is taken. When the eighth bit of the attribute code modifying the specified character is 1, the underline shown above is available.

Note: Attribute codes of the LCTC

MD0 … MD7	MD8	MD9	MD10	MD11	MD12	MD13	MD14	MD15
Character code data				R	C	BL	W	B

Figure 5-5 Attribute Codes on Basic Application Circuit

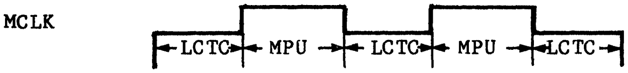
5.2 CRTC Compatible Board

5.2.1 Circuit specifications

Figure 5-6 illustrates a CRTC compatible board using the LCTC for a personal computer. Figure 5-7 illustrates its block diagram and data flow. Table 5-2 lists its specifications.

This board is software compatible with CGA (Color Graphics Adapter) of the IBM-PC.

Table 5-2 Specifications of CRTC Compatible Board

Item	Specificatoins	
Display Format	Single screen character display (Mode 5) Single screen graphic 2 display (Mode 8)	
Character Font	8 x 8 dots	
DCLK Frequency	7 MHz	
Screen Size	80 characters x 25 rows = 2,000 characters (Character display) 640 x 200 dots (Graphic display)	
Frame Buffer Access Mode	Synchronous access (Cycle-steal) 	
Frame Buffer	16 kbytes (SRAM HM6264 x 2)	
Address Allocation	Frame buffer	$A8000 to $ABFFF
	External mode register	$3D8
	MODE pin register	$3EF
	Access time register	$3EA
	LCTC address register	$3D4
	LCTC data register	$3D5

Note: IBM-PC is a trade mark of International Business Machines Corporation (USA).

5.2.2 Circuit

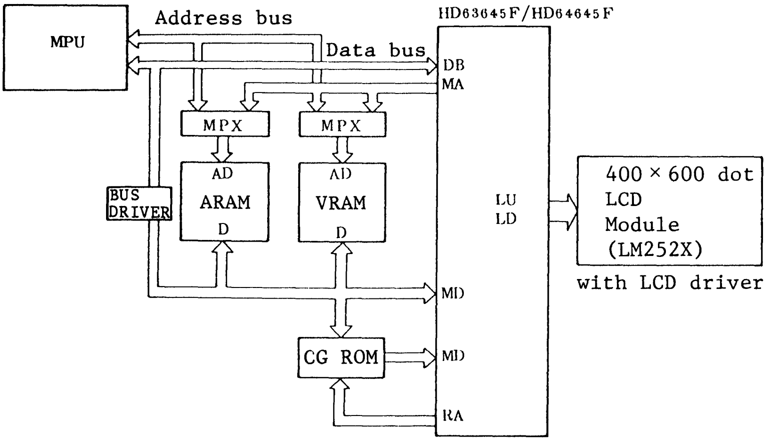


Figure 5-6 CRTC Compatible Board

For drawing, when the MPU is attempting to access a VRAM, the bus keeps the MPU wait by inserting a wait cycle into a bus cycle of the MPU if the bus is occupied by LCTC display access.

On this board, during MCLK cycle of the LCTC, LCTC display access is performed with MCLK = low, and MPU drawing access with MCLK = high.

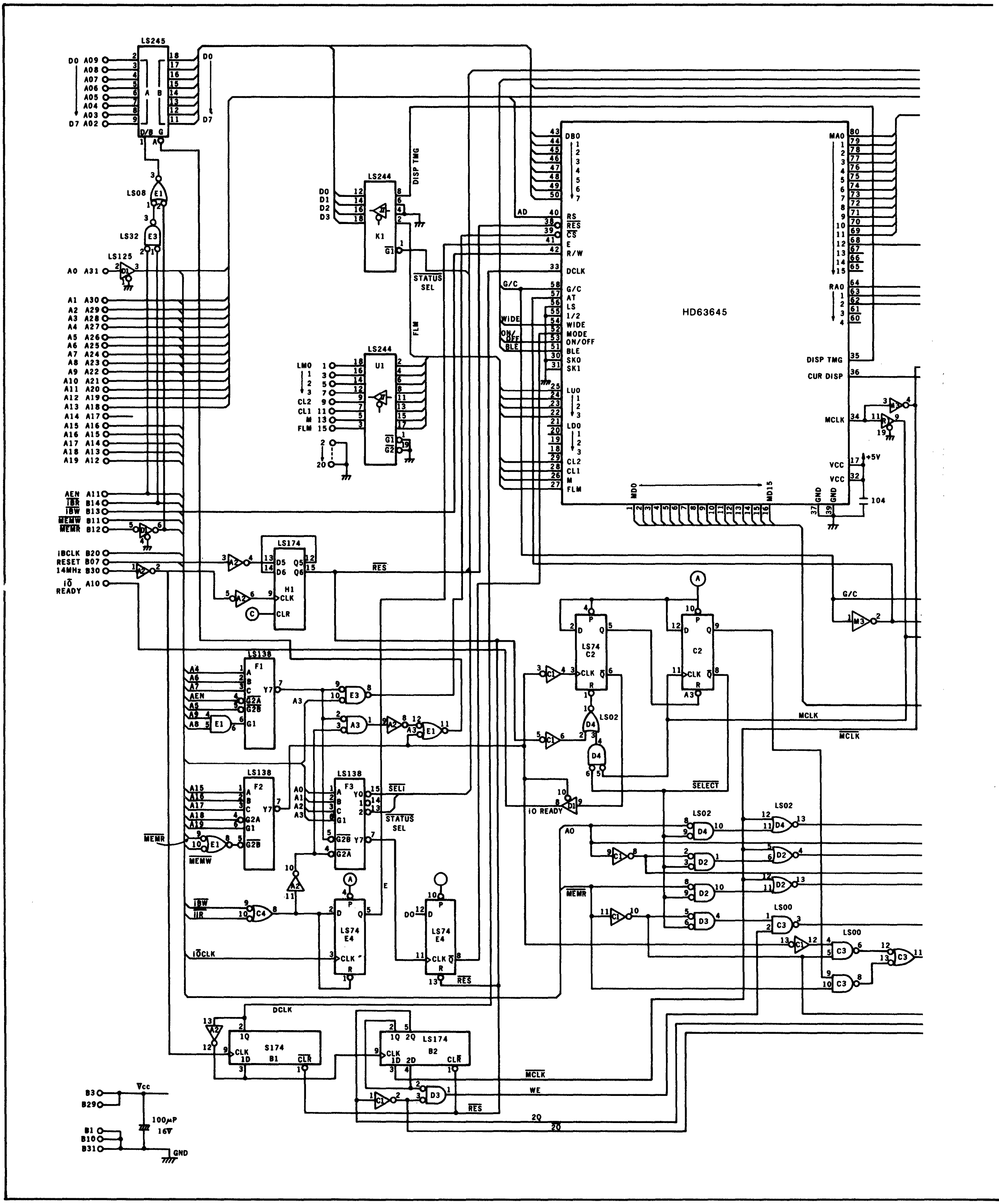
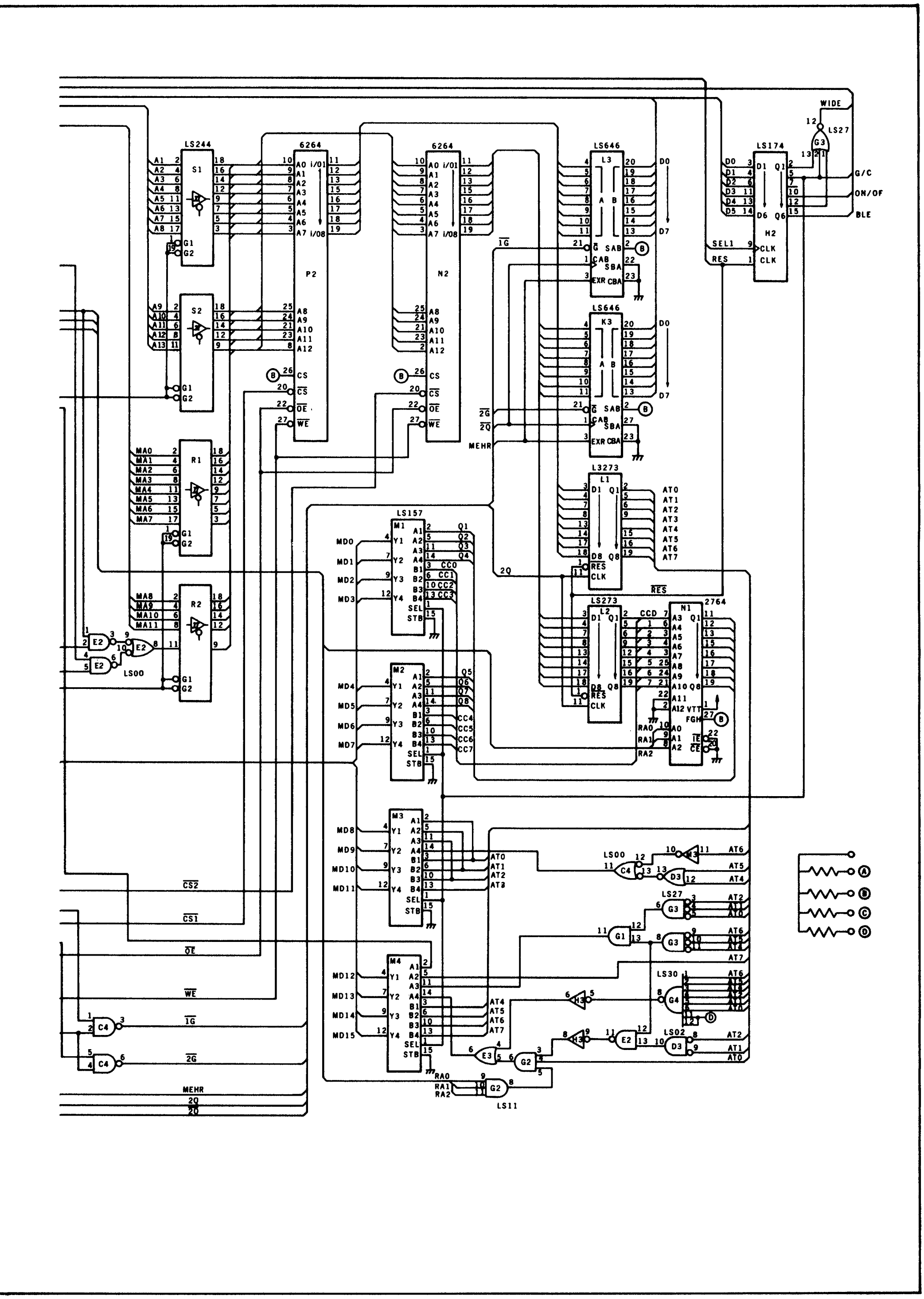


Figure 5-7 Block Diagram of CRTC Compatible Board


LS244
S1
S2
R1
R2
6264
P2
N2
LS646
L3
K3
LS174
H2
LS27
G3
WIDE
G/C
ON/OF
BLE
SEL1
RES
D0
D7
1G
2G
2Q
MEHR
L3273
L1
LS273
L2
2764
N1
AT0
AT1
AT2
AT3
AT4
AT5
AT6
AT7
CCD
RA0
RA1
RA2
LS157
M1
M2
M3
M4
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
MD8
MD9
MD10
MD11
MD12
MD13
MD14
MD15
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
CC0
CC1
CC2
CC3
CC4
CC5
CC6
CC7
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
MA9
MA10
MA11
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
E2
LS00
C4
D3
LS30
G4
G1
LS02
H3
E3
G2
LS11
CS2
CS1
OE
WE
1G
2G
MEHR
2Q
2O
A
B
C
D

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When the MPU accesses a VRAM, IOREADY is driven low and a WAIT cycle is inserted. Then, after inserting WAIT cycles from the next MCLK rising edge to falling edge, IOREADY is driven high. WAIT cycles are no longer inserted and the bus cycle is then completed.

Figures 5-8 (a) and (b) show bus timing of a VRAM. The MPU 8088, IBM-PC, operates with a 7-MHz clock. The DCLK of the LCTC inputs a 7-MHz clock as well.

At MPU write, since write data is already fixed, data does not need to be latched. $\overline{\text{WE}}$ (write enable) signal is externally generated and written.

At MPU read, since data output by memory is valid only during MCLK = high, the data should be latched during this period, and the MPU should read data at the last falling edge of T_W state after MCLK is driven low.

For display, since addresses output by the LCTC are connected with a VRAM only during MCLK = low (the first half of MCLK cycle), data output by memory should be latched during this period, and the data should be retained until data (MD) read timing of the LCTC at the second half of MCLK cycle.

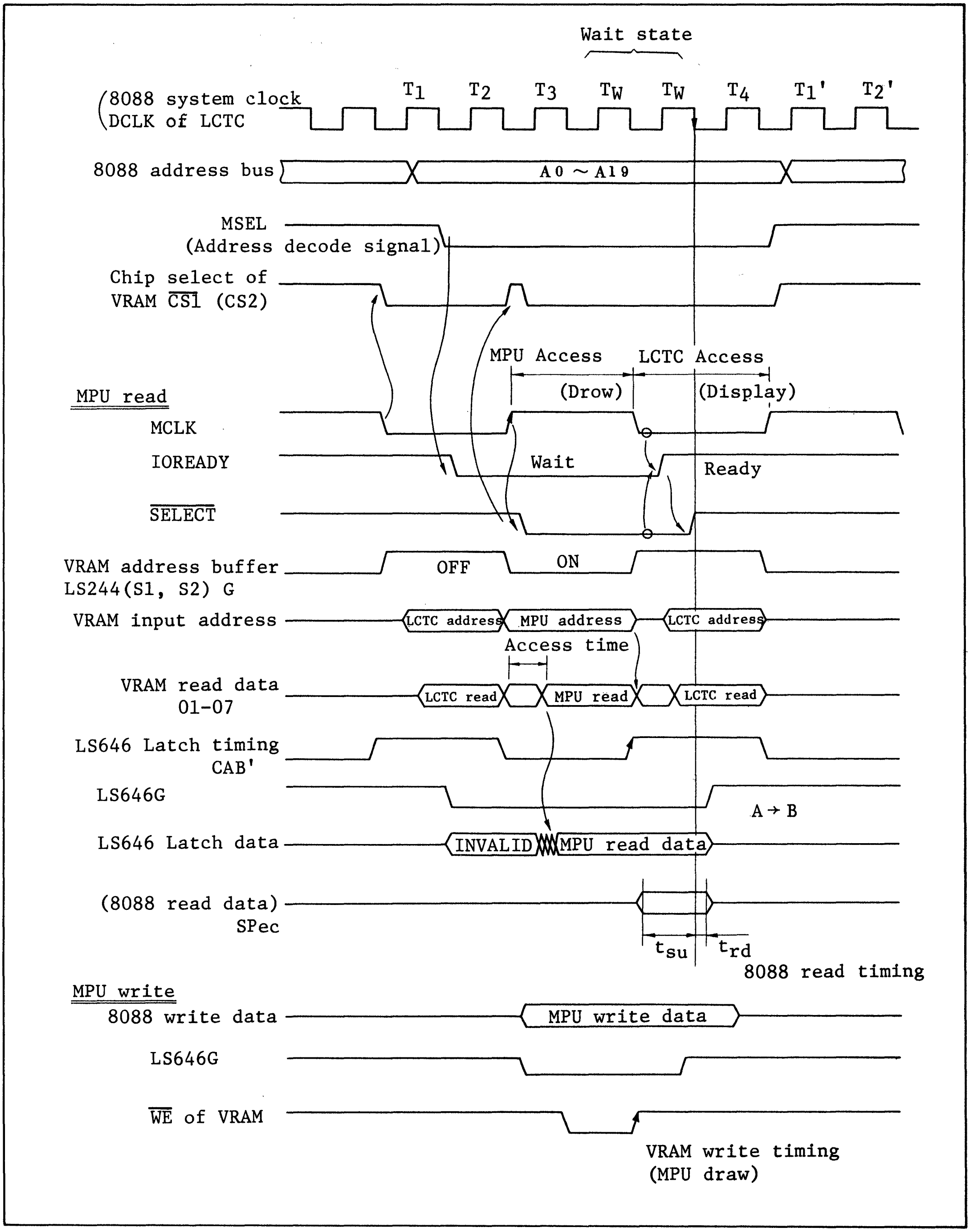


Figure 5-8 (a) VRAM Access Timing of MPU Draw

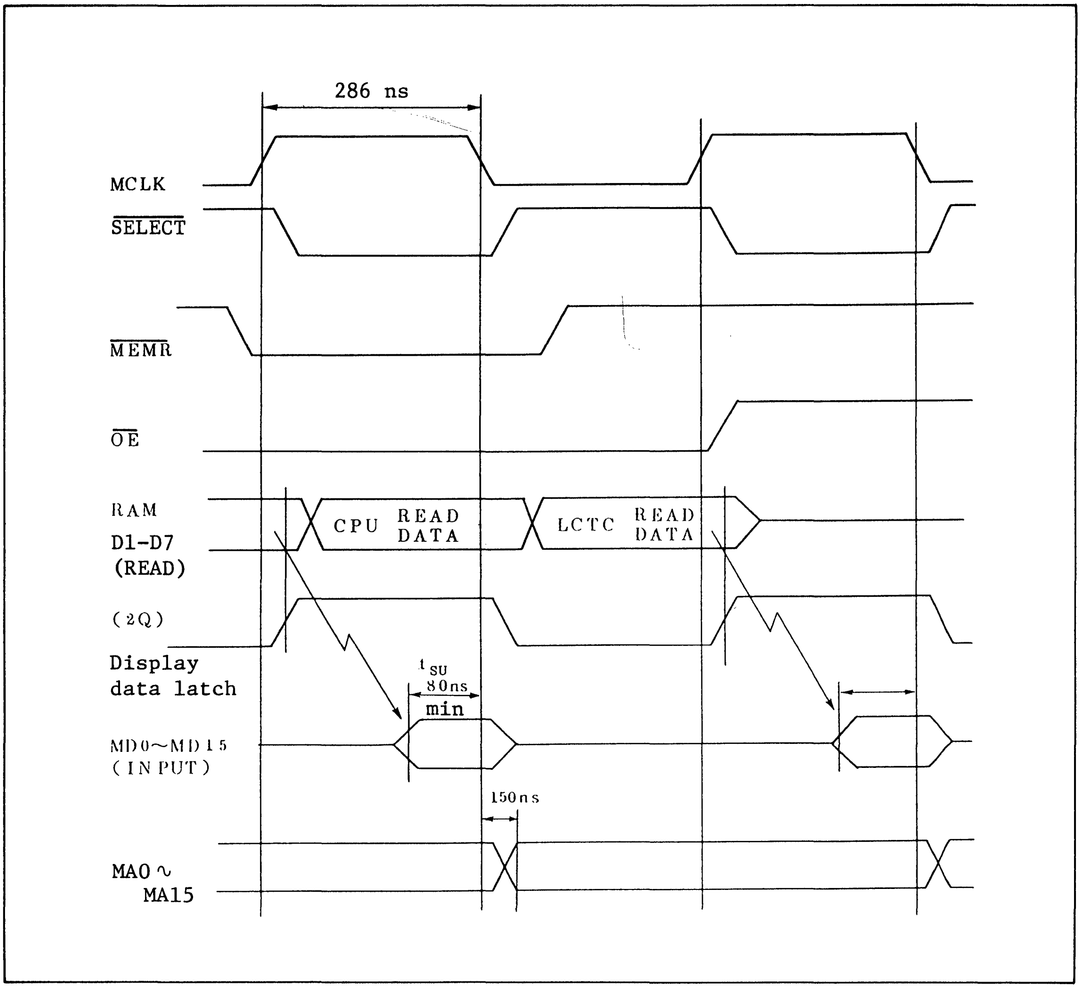


Figure 5-8 (b) VRAM Access Timing of LCTC Read

Display data read from a VRAM is directly connected with MD0-MD15 input of the LCTC in graphic mode.

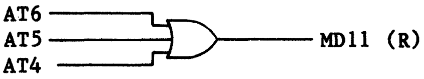
In character mode, out of 2 consecutive bytes of addresses simultaneously read, the low-order byte is assigned to a character code and the high-order byte to an attribute code modifying the character.

The low-order byte (character code) of display data is allocated to an address of the character generator (CG ROM) and is used for data read from an actual character font. Data read from CG ROM is connected to MD0-MD7 of the LCTC. The high-order byte (attribute code) is input to MD11-MD15 of LCTC attribute input after decoding according to the IBM-PC specifications. In this way, VRAM can be considered to be divided into two RAMs: ARAM (attribute RAM) and VRAM (video RAM). Figures 5-9 (a) and (b) show attribute codes specifications.

The LCTC mode (graphic/character selection, display on/off and blinking) is specified through LCTC external pins and through registers which can be written by the MPU.

	MD15	MD14	MD13	MD12	MD11	MD10	MD9	MD8	MD7	MD0
(AT = 1)	B	W	BL	C	R				Character code data	

R: reverse video (MD11)



The OR of AT6, AT5, and AT4 is taken.

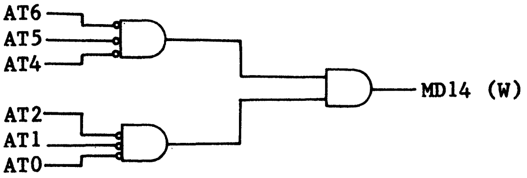
C: cursor (MD12)

Directly inputs CUDISP signal of the LCTC.

BL: blinking (MD13)

Directly inputs AT7.

W: white (MD14)



When all of AT6-AT4 and AT2-AT0 are low, nondisplay (white) is available.

B: black (MD15)

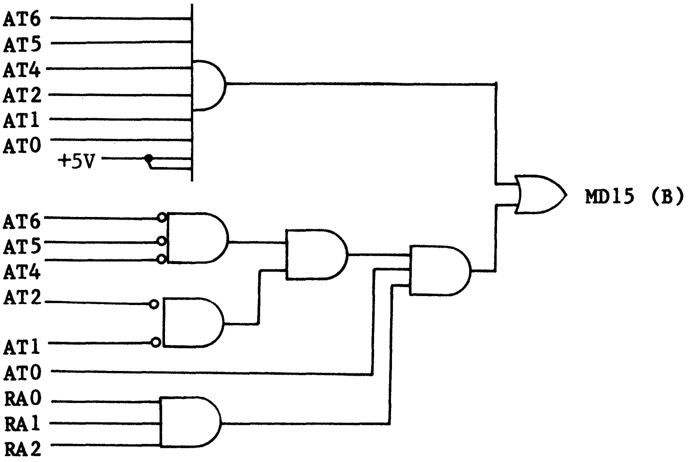


Figure 5-9 Attribute Codes Description

In character mode, this board does not support superimposition of graphics and characters (OR mode) with LCTC AT input = high (conforming to the CGA specifications). Since the black display part on an LCD differs from CRT display (white on CRT), nondisplay (black) corresponds to W (white) of the LCTC and nondisplay (white) corresponds to B (black).

Figure 5-10 shows an address map of the LCTC and VRAM on this board. Also, figure 5-11 illustrates registers on the board.

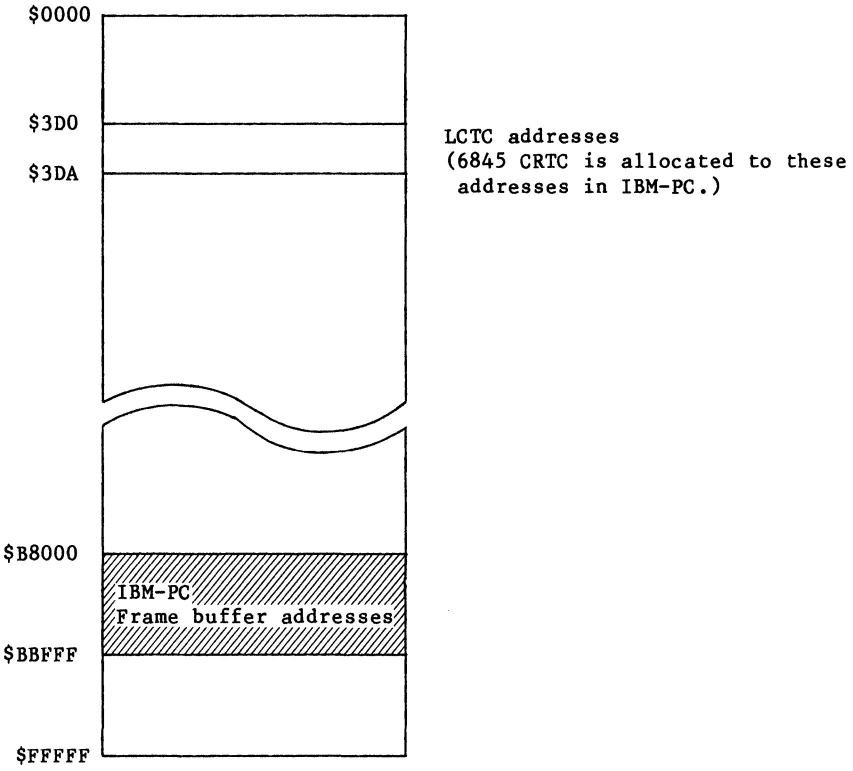
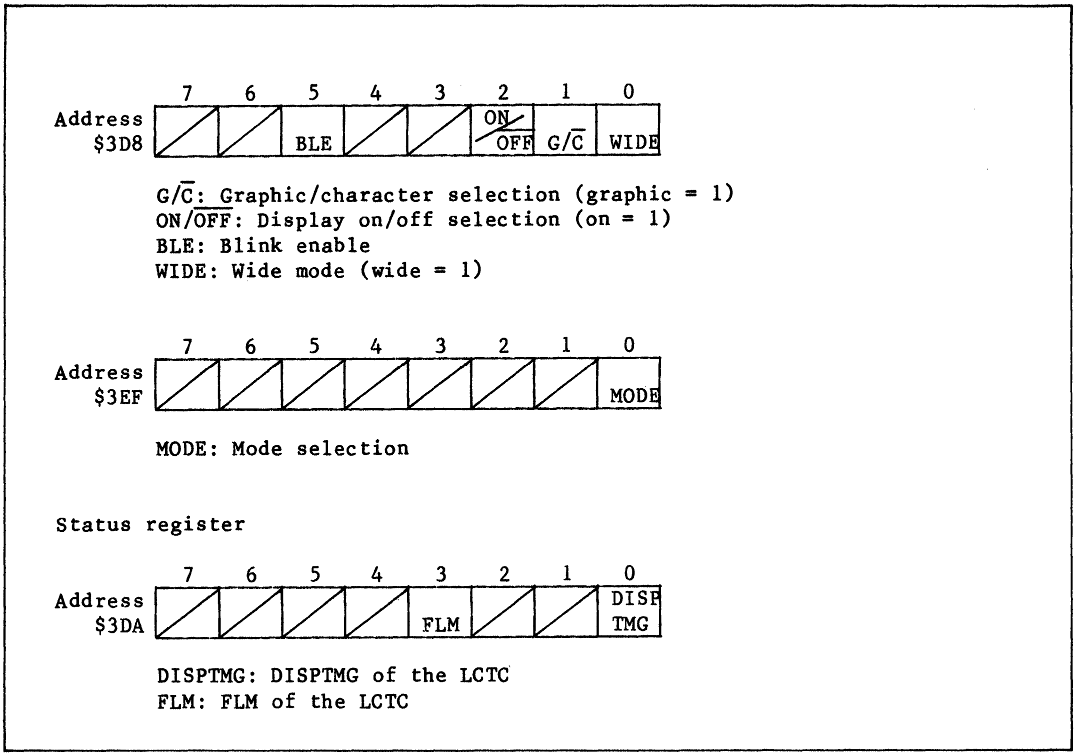


Figure 5-10 Address Map of CRTC Compatible Board



G/C: Graphic/character selection (graphic = 1)
ON/OFF: Display on/off selection (on = 1)
BLE: Blink enable
WIDE: Wide mode (wide = 1)

MODE: Mode selection

Status register

DISPTMG: DISPTMG of the LCTC
FLM: FLM of the LCTC

Figure 5-11 External Registers Description on Board

Connected LCD module has a 640 (width) dots x 200 (height) dots configuration and uses the LM250X (Hitachi), which can display alphanumerics (80 characters x 25 rows), Chinese characters and graphics. Since data is transferred to the LCD module on 4-bit basis in parallel, it uses LU0-LU3 of LCTC display data output. The LCD module can be connected simply by bufferring LCTC output.

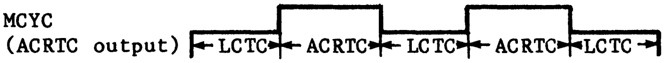
Since IBM-PC uses MPU 8088, interface can be more easily performed by using the LCTC with 80-family bus interface (HD64645F). But on this board, the LCTC with 68-family bus interface (HD63645F) is used for design convenience. Therefore, LCTC E clock is generated by using IOW and IOR signals.

5.3 Connection with ACRTC

5.3.1 Circuit specifications

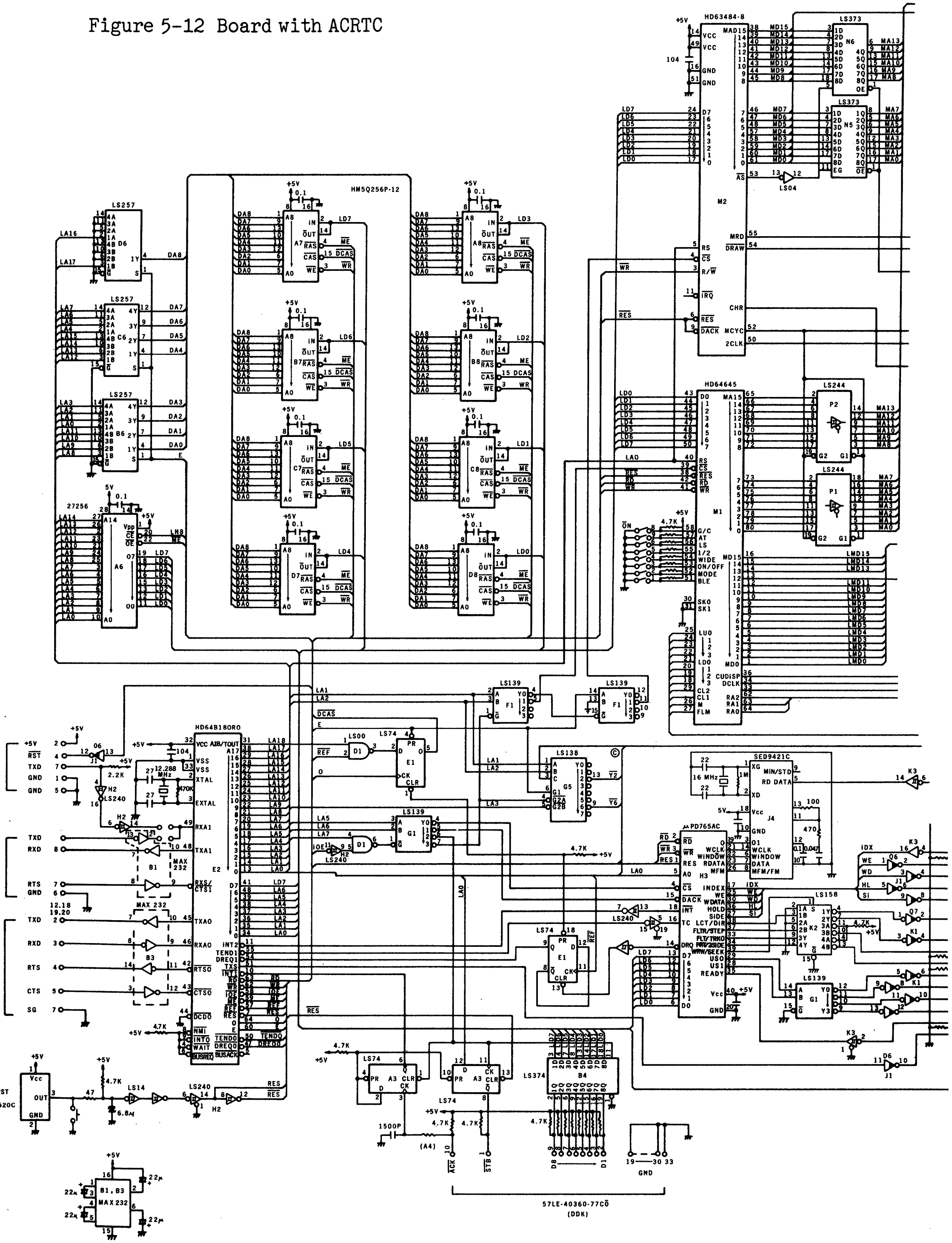
Figure 5-12 illustrates an example of display using HD63484 (ACRTC) as a drawing processor. Table 5-3 lists its specifications. Figure 5-13 shows its block diagram. As shown in the diagram, floppy discs and so on can be connected to this board, and CP/M Plus (Ver 3.0) can be used as OS. Table 5-3 shows the hardware specifications of this board.

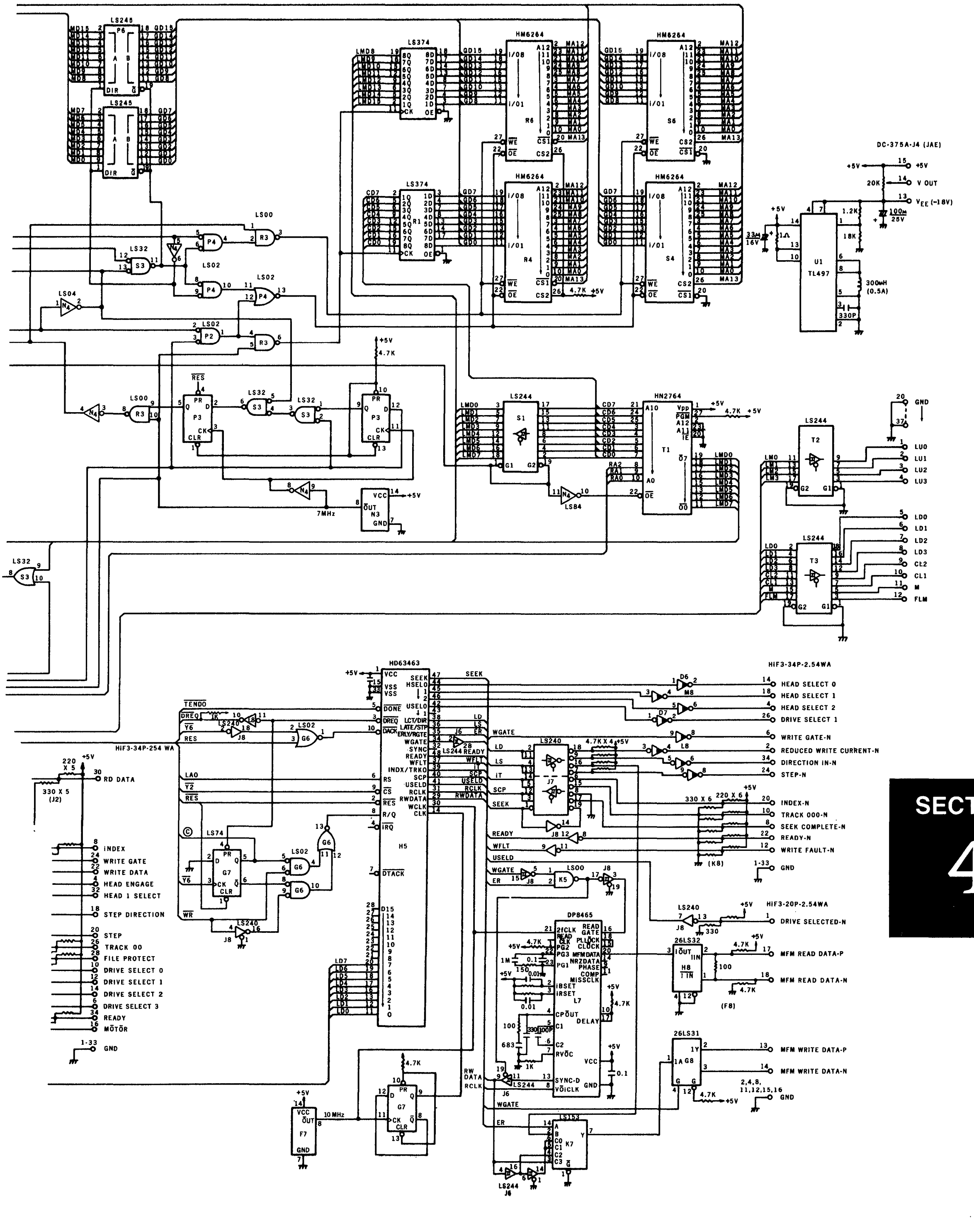
Table 5-3 Specifications of Board with ACRTC

Item	Specificatoins
Display Format	Single screen character display (Mode 5) Single screen graphic 1 display (Mode 7)
Character Font	8 x 8 dots
DCLK Frequency	7 MHz
Screen Size	80 characters x 25 rows (Character display) 640 x 200 dots (Graphic display)
Frame Buffer Access Mode	Synchronous access (Time-sharing)  MCYC (ACRTC output) LCTC ACRTC LCTC ACRTC LCTC
Frame Buffer	32 kbytes (SRAM HM6264 x 4)
Address Allocation	ACRTC address register $E0 ACRTC control register $E1 LCTC address register $E2 LCTC control register $E3

5.3.2 Circuit

Figure 5-12 Board with ACRTC




LS245
P6
LS374
R1
HM6264
R6
R4
S6
S4
DC-375A-J4 (JAE)
+5V
V OUT
V_EE (-18V)
U1
TL497
300μH (0.5A)
LS00
LS32
LS02
LS04
LS244
S1
HN2764
T1
LS84
N3
7MHz
T2
T3
LU0
LU1
LU2
LU3
LD0
LD1
LD2
LD3
CL2
CL1
M
FLM
GND
HD63463
H5
HIF3-34P-2.54WA
HEAD SELECT 0
HEAD SELECT 1
HEAD SELECT 2
DRIVE SELECT 1
WRITE GATE-N
REDUCED WRITE CURRENT-N
DIRECTION IN-N
STEP-N
INDEX-N
TRACK 000-N
SEEK COMPLETE-N
READY-N
WRITE FAULT-N
GND
HIF3-34P-254 WA
RD DATA
INDEX
WRITE GATE
WRITE DATA
HEAD ENGAGE
HEAD 1 SELECT
STEP DIRECTION
STEP
TRACK 00
FILE PROTECT
DRIVE SELECT 0
DRIVE SELECT 1
DRIVE SELECT 2
DRIVE SELECT 3
READY
MOTOR
GND
LS74
G7
G6
LS240
J8
J7
DP8465
L7
LS240
HIF3-20P-2.54WA
DRIVE SELECTED-N
26LS32
H8
MFM READ DATA-P
MFM READ DATA-N
26LS31
G8
MFM WRITE DATA-P
MFM WRITE DATA-N
F7
10MHz
LS153
K7
LS244
J6

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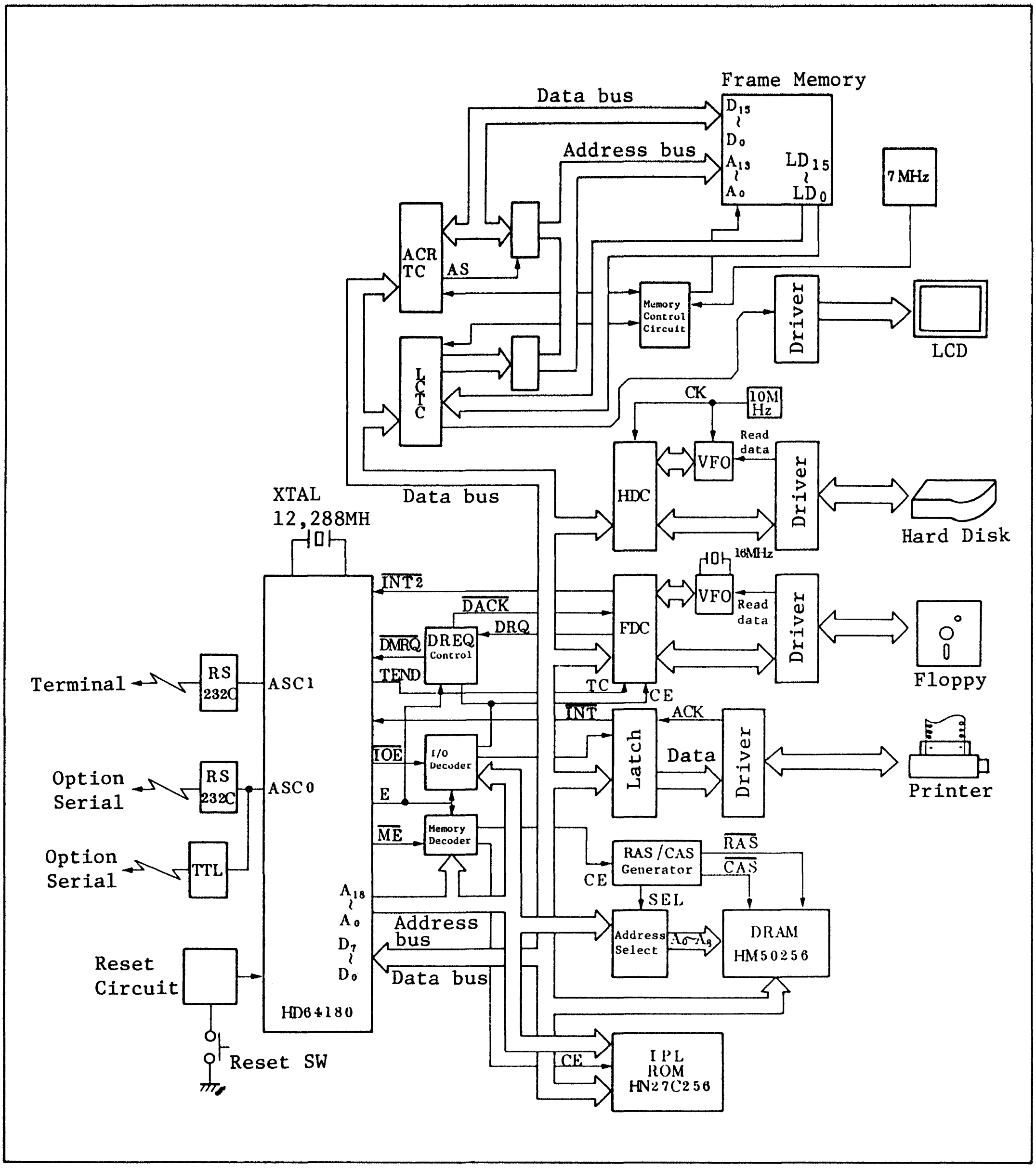


Figure 5-13 Block Diagram of Board with ACRTC

5.3.3 Circuit description

Since the LCTC is designed to be software compatible with the CRTC, it does not provide a drawing function. However, using the ACRTC as a drawing processor enables this function; the ACRTC draws on a frame buffer and then the LCTC displays the data drawn by the ACRTC on an LCD.

In this case, some of the ACRTC functions are disabled.

The following ACRTC functions are enabled.

(a) High level command language: 38 commands including graphic drawing commands such as LINE, CIRCLE, ELLIPSE, PAINT and COPY with X-Y coordinates as a parameter

(b) High speed graphic drawing: Maximum 500 ns/pixel

(c) Pattern graphic drawing: Internal 32-byte pattern RAM

(d) Drawing area detection function: Controls drawing area such as drawing inhibition outside of a specified area or detection of a particular area

The following functions are disabled.

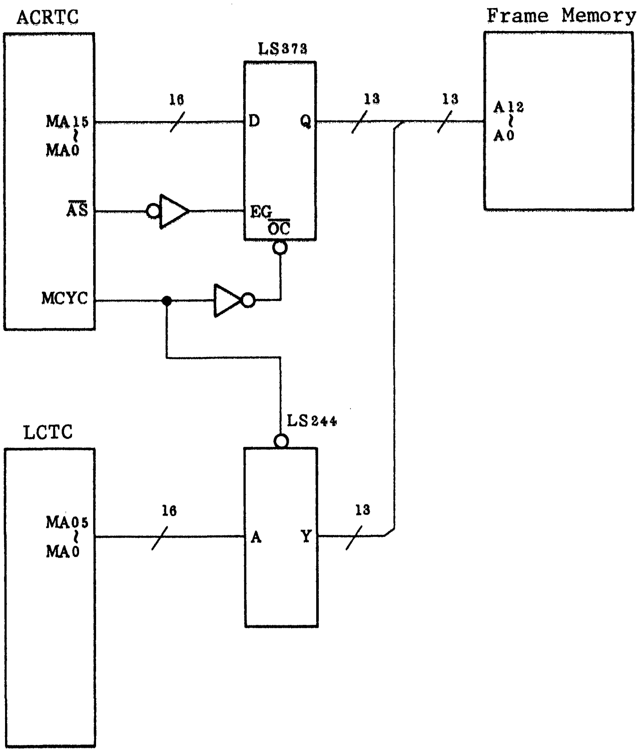
(a) Split screens
(b) Zooming
(c) Smooth scroll
(d) Screen overlaying
(e) External synchronization
(f) Programmable cursors

LCTC functions partially cover (c) and (d) of the above functions. For details of the ACRTC, refer to HD63484 ACRTC USER'S MANUAL (680-1-28-C).

Table 5-4 Hardware Specifications of Board with ACRTC

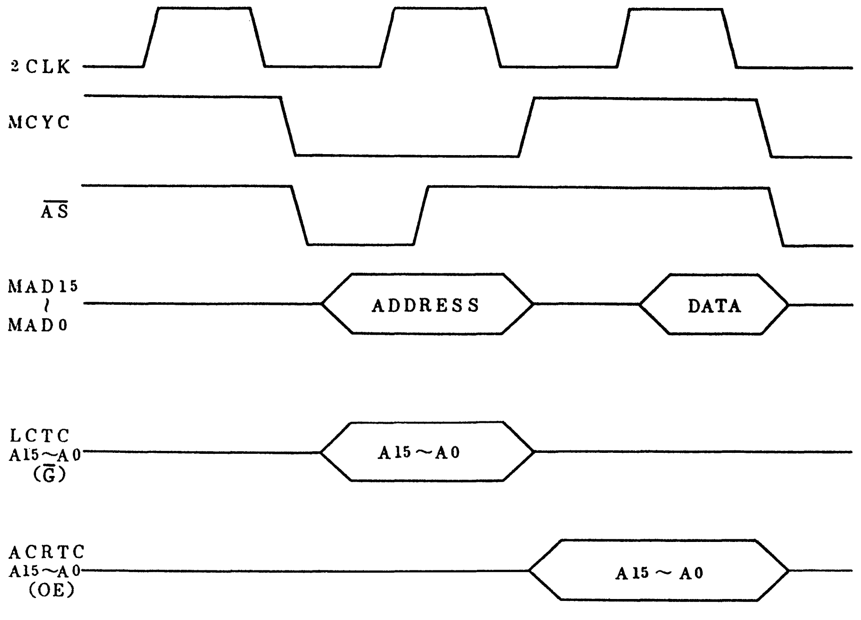
No.	Item	Specifications	Remarks
1	Processor (MPU)	HD64180, ¢ = 6.144 MHz	Uses external crystal of 12.288 MHz
2	Memory	DRAM; HM50256 x 8 (256 kbytes) ROM; HM27256 (32 kbytes)	
3	Parallel Interface	Sentronics (8-bit parallel) interface Handshake with $\overline{\text{ACK}}$ respond	
4	Serial Interface	RS-232C communication circuit x 2 channels (1 channel is only for terminals) Uses MAX232 (Maxim)	(Terminal setting) 9600 bps, 8-bit without parity, 2-bit stop
5	Floppy Disc Interface	Can select either double density or single density of 5-inch both-sided disc (FM) Up to 4 FDD's (equivalent of FD-55B TEAC)	
6	Hard Disc Interface	HDD: DK505	
7	LCD Interface	Drawing processor: HD63484 (ACRTC) Display processor: HD63645 (LCTC) DCLK = 7 MHz	DC/DC converter supplies $-V_{EE}$ of LM250, LCD module
8	Power Supply	+5 V (±5%): over 1.5 A for system	

On this board, during MCYC cycle of the ACRTC, LCTC display access is performed with MCYC = low, and ACRTC drawing access with MCYC = high. However, since the ACRTC uses pins MAD0-MAD15 as address bus and data bus, the memory address of the ACRTC should be latched. Figure 5-14 shows an address multiplexer and its timing chart.



(a) Logic

Figure 5-14 Address Multiplexer



(b) Timing Chart

Figure 5-14 Address Multiplexer (cont.)

This method requires perfect synchronization of the LCTC and the ACRTC. So, on this board, if there is any phase difference of memory cycle between the LCTC and the ACRTC, the phase is adjusted by cancelling one clock of 2CLK input of the ACRTC. Figure 5-15 shows a synchronization circuit of the LCTC and the ACRTC, and its timing chart.

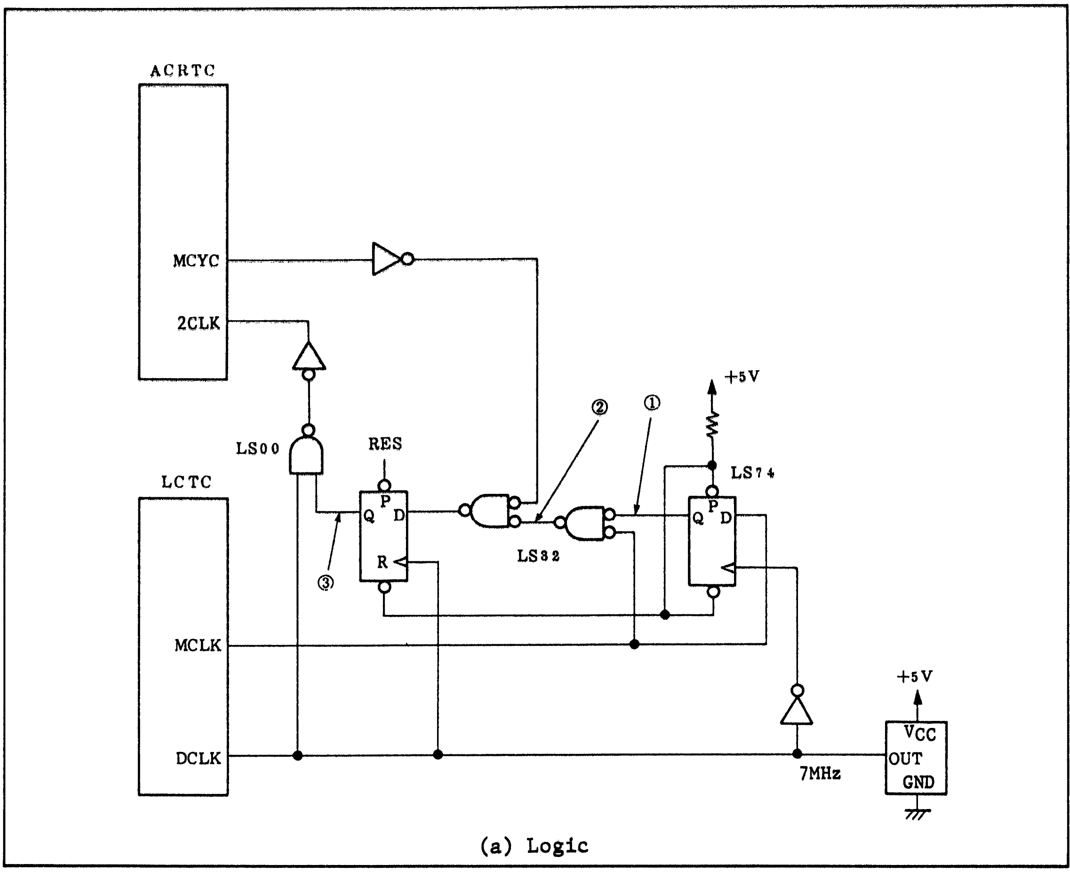


Figure 5-15 Synchronization Circuit of ACRTC and LCTC

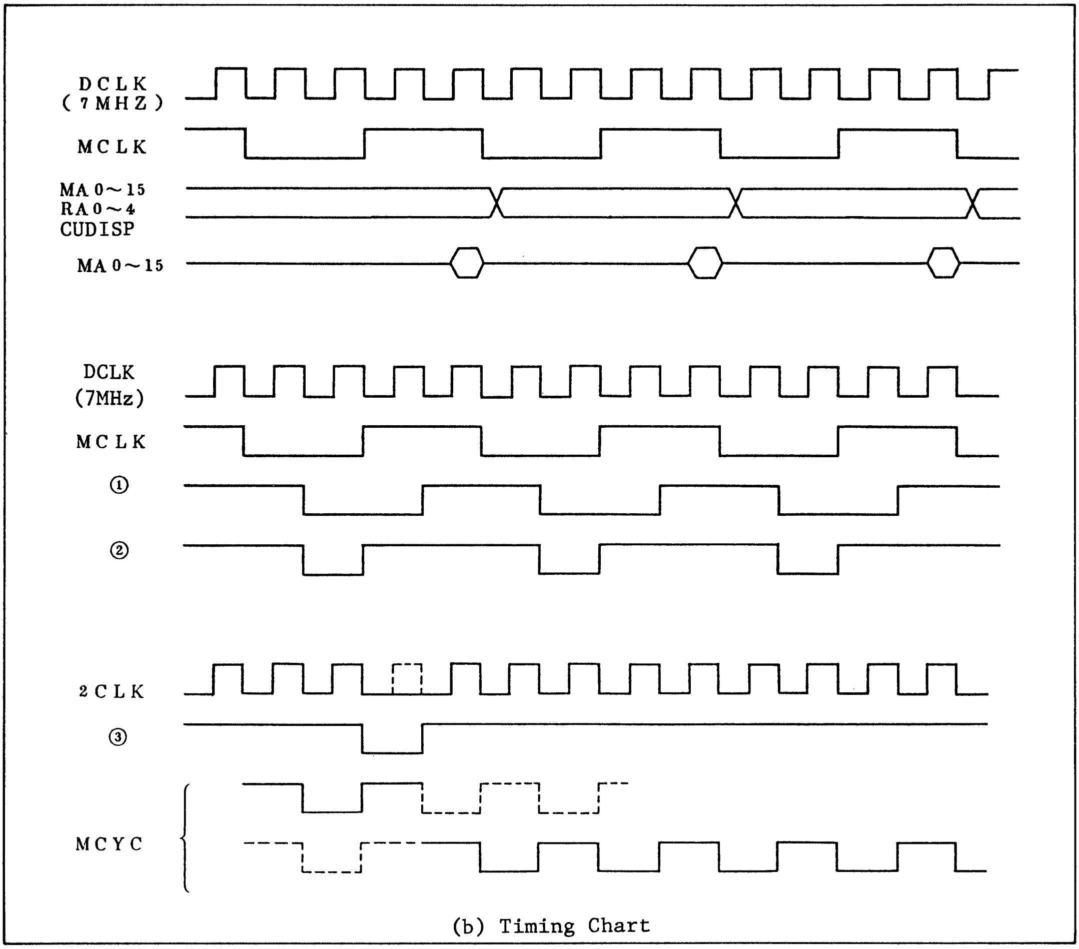


Figure 5-15 Synchronization Circuit of ACRTC and LCTC (Cont.)

Figure 5-16 shows bus timing of a frame buffer. The operation clock frequency of the ACRTC is 7 MHz. DCLK of the LCTC inputs 7-MHz clock as well.

The ACRTC writes to and read from a frame buffer while MCYC is high. Thus the LS373 latches address signal with the $\overline{\text{AS}}$ signal, and an external circuit generates the $\overline{\text{WE}}$ (write enable) signal and OE (output enable) signal for the memory, and then writes to the buffer.

During the LCTC read, the address output by the LCTC is connected with a frame buffer only while MCYC of the ACRTC is low. Therefore, the data output by the memory should be latched during this period and be retained until the late half cycle of the LCTC MCLK, when the LCTC reads data (MD).

Table 5-5 lists the I/O address map on this board, and figure 5-17 shows a physical memory map.

This board has a 256-kbit frame buffer memory, and an LCD module of up to 640 x 400 dots can be connected. It can display alphanumerics of 80 characters x 50 rows, Chinese characters, and graphics making the best use of the ACRTC.

The recommended LCD module is LX252X (Hitachi). In this module, data is transferred on a 4-bit basis in parallel with 2 buses. Thus all of LU0-LU3 of the LCTC, which output display data, are used. Since the connecting wire to an LCD module is usually long and has large capacitance, the LCTC output should be bufferred.

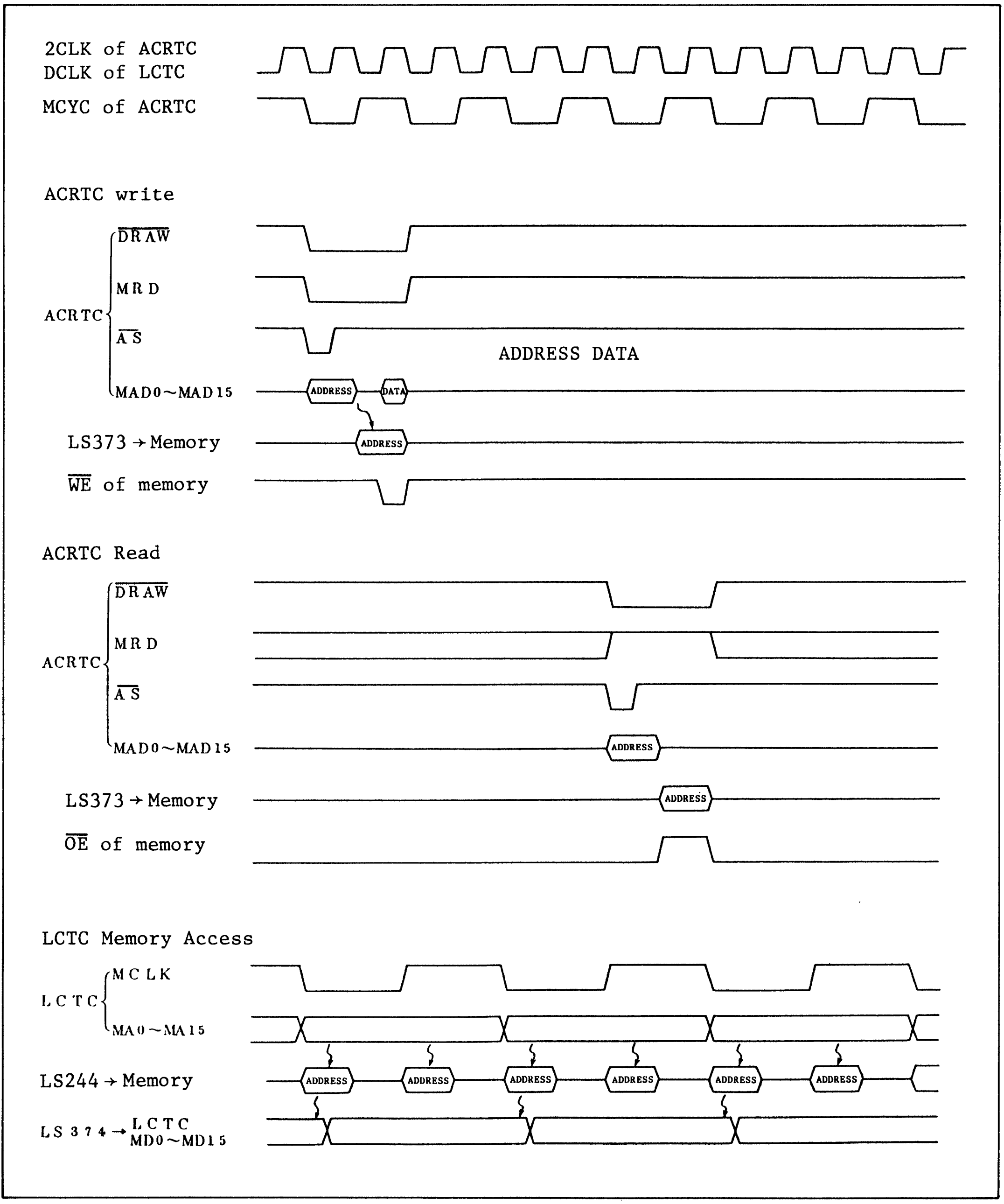


Figure 5-16 Access Timing of Frame Buffer

Table 5-5 I/O Address Map

I/O Address	Contents
80	FDC (HD63265) status
81	FDC (HD63265) data
A0	FDC (HD63265) $\overline{\text{DACK}}$ (at DMA)
C0	Output for a printer ($\overline{\text{STB}}$ = high)
C1	Output for a printer ($\overline{\text{STB}}$ = low)
E0	ACRTC (HD63484) address register
E1	ACRTC (HD63484) control register
E2	LCTC (HD63645) address register
E3	LCTC (HD63645) control register
E4	HDC (HD63463) status
E5	HDC (HD63463) data

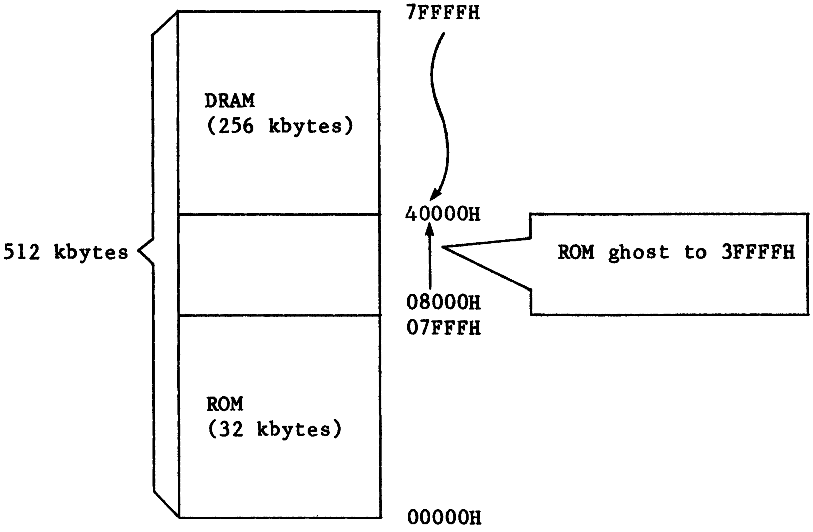


Figure 5-17 Physical Address Map

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Section Five

HD63645/ HD64645/HD64646 LCD Timing Controller (LCTC) User's Manual

Section Five

HD63645/
HD64645/HD64646
LCD Timing Controller (LCTC) User's Manual

For additional information reference:

Section 1. LCD Controller/Driver LSI Data Book
Section 2. HD66300T Horizontal Driver for TFT-Type LCD Color TV
Section 3. HD66840 Video Interface Controller (LVIC) Application Note
Section 4. HD63645F/HD64645F LCD Timing Controller (LCTC) Application Note

SECTION
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-APPENDIX-

1. OVERVIEW

1.1 General Description

The HD63645, HD64645, HD64646 (LCD Timing Controller: LCTC) is the control LSI for the large size dot matrix liquid crystal display. The LCTC is software compatible with the HD6845 (CRTC), since the programming method of internal registers and memory addresses is based on the CRTC. The display system can be easily replaced from the CRT display to the LCD.

The LCTC offers a variety of functions and performances such as vertical and horizontal scrolling, and various types of character attribute functions such as reverse video, blinking, whitening, blackening and OR function for superimposition of character display and graphic display.

The HD63645 has a 6800 family bus interface. The HD64645, HD64646 has a 80 family bus interface. The HD64646 is a modified version of the HD64645 with difference LCD interface timing.

Since the LCTC has two 4-bit data buses, the compact LCD system with a large panel is provided by connecting the LCTC with the HD61104 (column driver) and the HD61105 (common driver) and so on. And this makes the best use of the high data transfer speed of the LCTC. The power dissipation is lowered by adopting the CMOS process.

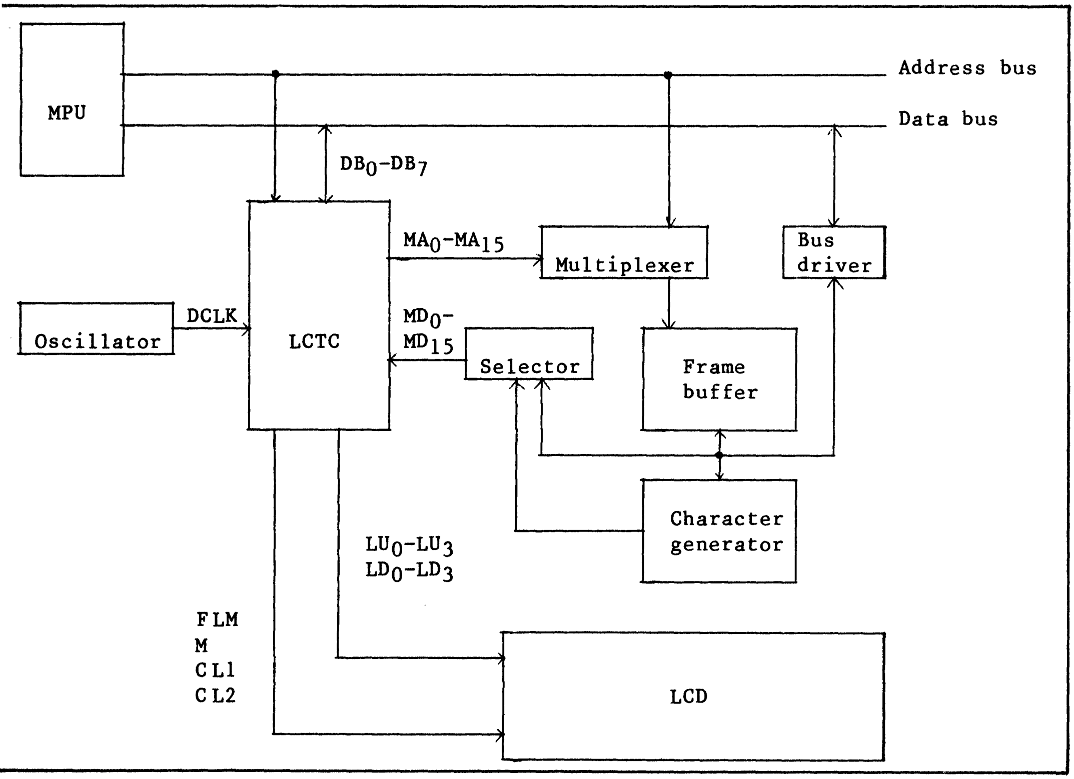


Figure 1-1 LCTC System Configuration Example

1.2 Ordering Information

Product	Bus Timing	CPU Interface	Package
HD63645	2 MHz	68 family	80-pin plastic QFP(FP-80)
HD64645	4 MHz	80 family	
HD64646	4 MHz	80 family	80-pin plastic QFP(FP-80A)

1.3 Features

- Software compatible with HD6845
- Programmable screen size: up to 1024 dots (length)
  up to 4080 dots (width)
- High speed data transfer: up to 20 MHz in the character mode
  up to 40 MHz in the graphic mode
- Selectable single or dual screen configuration
- Programmable multiplexing duty ratio: static to 1/512 duty
- Programmable character font: 1-32 dots (length)
  8 dots (width)
- Versatile character attributes: reverse video, blinking, whitening, and blackening
- OR function: superimposition of character display and graphic display
- Cursor with programmable shape, blink rate, display position and on/off switch
- Vertical smooth scrolling, vertical scrolling by character
  Horizontal scrolling by character
- Versatile display modes (*1) programmable by the mode register: display switching, graphic or character, normal or wide, attribute, and blink enable
- DRAM refresh address output
- 4- or 8-bit parallel data transfer between the LCTC and LCD driver
- Recommended LCD drivers: HD61104 (column), HD61105 (common), HD66106, and HD66107
- CPU interface: 68 family (HD63645)
  80 family (HD64645, HD64646)
- CMOS process
- Single +5 V ±10%

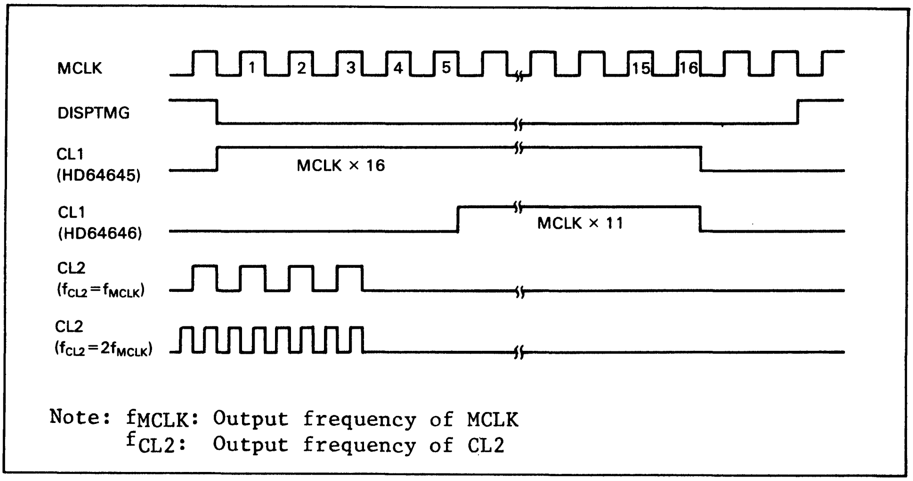
(*1) Also controlled via external pins.

1.4 Differences between HD64645 and HD64646

Figure 1-1 and figure 1-2 show the relation between display data transfer period, when display data shift clock CL2 changes and, display data latch clock CL1. Figure 1-1 is no skew, and figure 1-2 is a case with skew function.

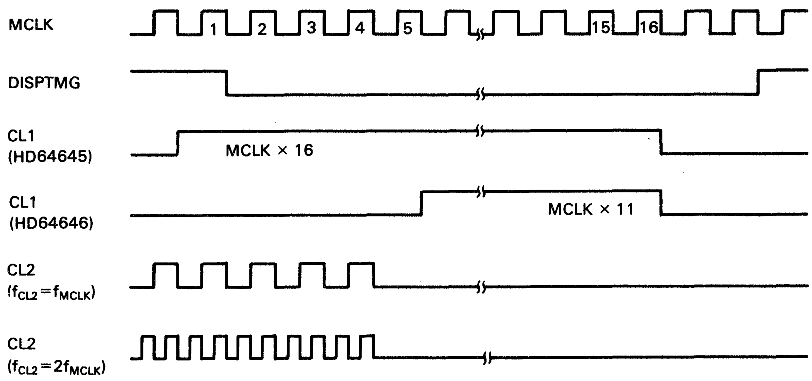
In figure 1-1 high periods of CL2 and CL1 of HD64645 overlap. HD64646 has no overlap like HD64645, and except for overlap parts HD64646 is the same as HD64645 functionally.

Besides, in case of skew function, phase relation between CL1 and CL2 changes. As figure 1-2 shows, data transfer period and CL1 "high" period of HD64646 never overlap in case of skew function.

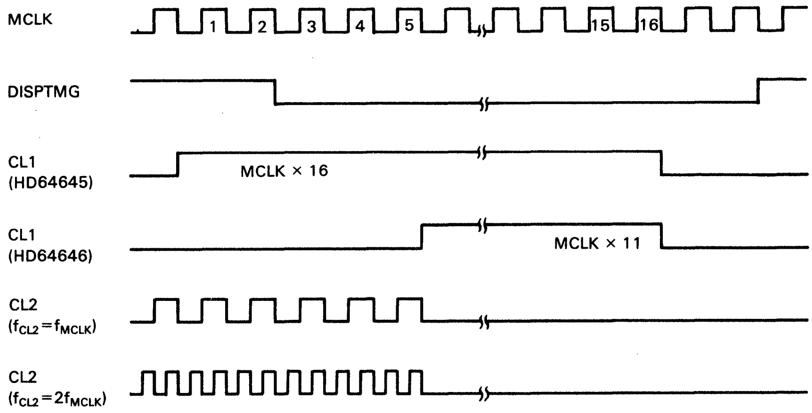


Note: f_{MCLK}: Output frequency of MCLK
f_{CL2}: Output frequency of CL2

Figure 1-1 Differences between HD64645 and HD64646 (no skew) (1)



(a) 1 character skew



(b) 2 character skew

Figure 1-2 Differences between HD64645 and HD64646 (skew) (2)

Table 1-1 LCTC Function Table

Item	Description
Display Format	Programmable horizontal scanning cycle by character clock time Programmable multiplexing duty ratio from static up to 1/512 Programmable number of displayed characters per character row Programmable number of rasters per character row (number of vertical dots of a character row + space between character rows)
Cursor Control	Programmable cursor display position, corresponding with RAM address Programmable cursor shape by setting display start/end rasters Programmable blink rate, 1/32 or 1/64 frame rate
Memory Renewal	Memory renewal time set, either by setting horizontal total characters or by pulsing MCLK
Memory Addressing	16-bit memory address and DRAM refresh address output, memories of up to 64 kbytes x 2 accessible
Paging and Scrolling	Paging and vertical scrolling by character, by renewing start address Horizontal scrolling by character, by setting horizontal virtual screen width Vertical smooth scrolling, by renewing display start raster
Character Attributes	Reverse video, blinking, whitening, and blackening attributes enable
LCTC Compatible	Facilitates system replacement of CRT display with LCD.
OR Function	Enables superimposition of character display and graphic display
LCTC Configuration	Single 5 V power supply I/O TTL compatible except $\overline{\text{RES}}$, MODE, SK0, and SK1 Bus connectable directly with HMCS6800 family (=HD63645F) CMOS process Internal logic perfect static 80-pin flat package plastic

2. LCD (LIQUID CRYSTAL DISPLAY) DESCRIPTION

2.1 How the LCD Performs

The LCD is performed through screening of external lights, while the CRT display is performed through the internal luminescence. The LCD method makes the display panel thinner and the power dissipation lower.

The following describes how the LCD performs. Without being supplied power, the external light is transmitted through the polarizers, because it is polarized at an angle of 90° by liquid crystal molecules. Then, the transmitted light is emitted in the same route by the reflector. Supplied power, the external light is not polarized, and so it cannot be transmitted through the polarizer2. Then, the screen is blackened. Basically, the LCD panel is structured as illustrated in Figure 2-1.

The LCD driver generates the potential difference to determine on or off of the screen. The LCD timing controller generates data and timing signals necessary for the driver.

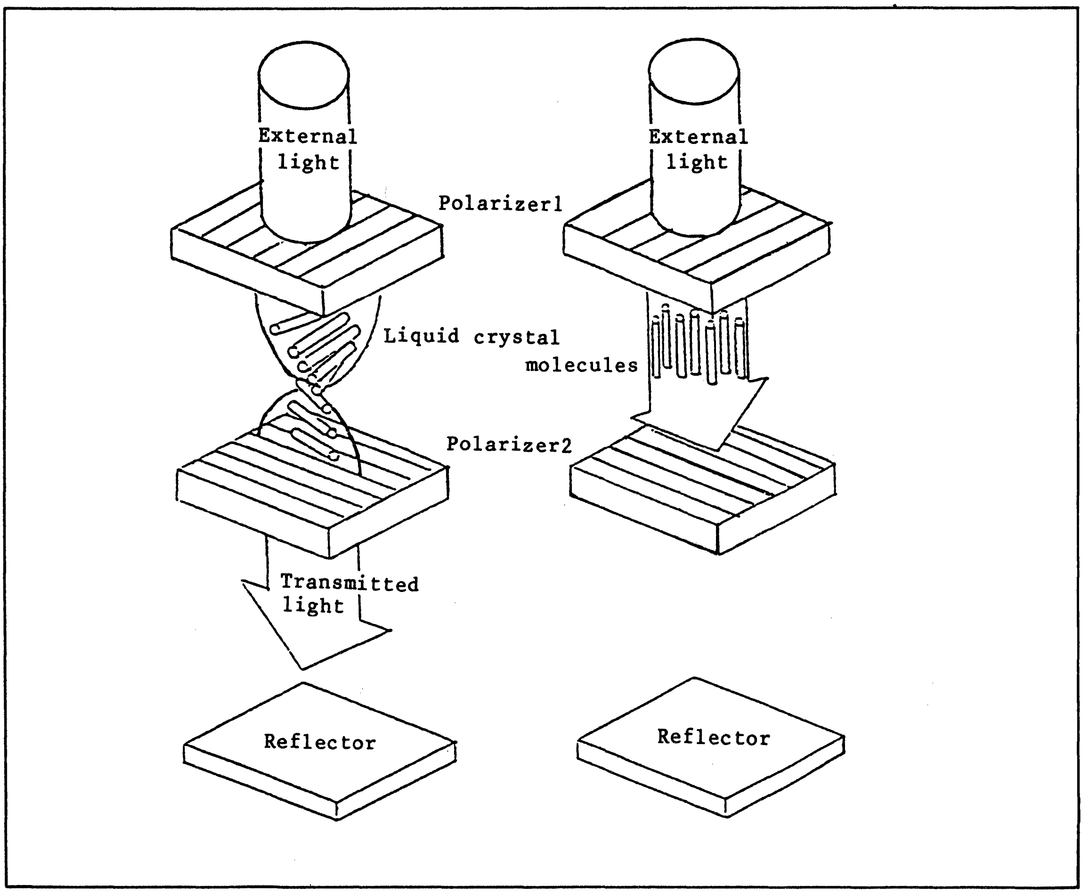


Figure 2-1 LCD Panel Structure

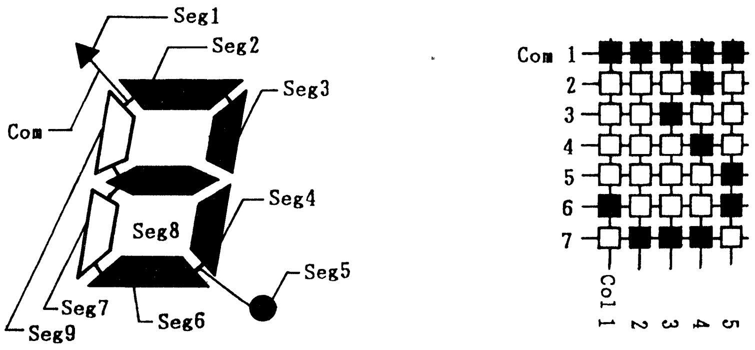
2.2 Multiplexing Drive Method

The LCD's on or off is determined by the potential difference generated by the common driver and the column driver.

For the segment type LCD shown in Figure 2-2(1), the static drive method is used. In this method, the selected level voltage is constantly supplied from the common pin. The LCD's on or off, therefore, depends on the level of the voltage supplied from the segment pins.

For the LCD screen with a large number of pixels, the multiplexing drive method is used. This method supplies the selected level voltage to each multiple common pin in turn. It scans vertically and outputs to the column pin the display data of the raster being selected at the time. The main difference between CRT and LCD is that the former scans dot by dot while the latter scans raster by raster.

This method requires a high data transfer speed for driving a large LCD because a screen must be rewritten at a speed of about 70 Hz. The LCTC offers high performance of 20 Mbits/sec (max) in the character mode and 40 Mbits/sec (max) in the graphic mode. It is most suitable to drive a large-capacity LCD.

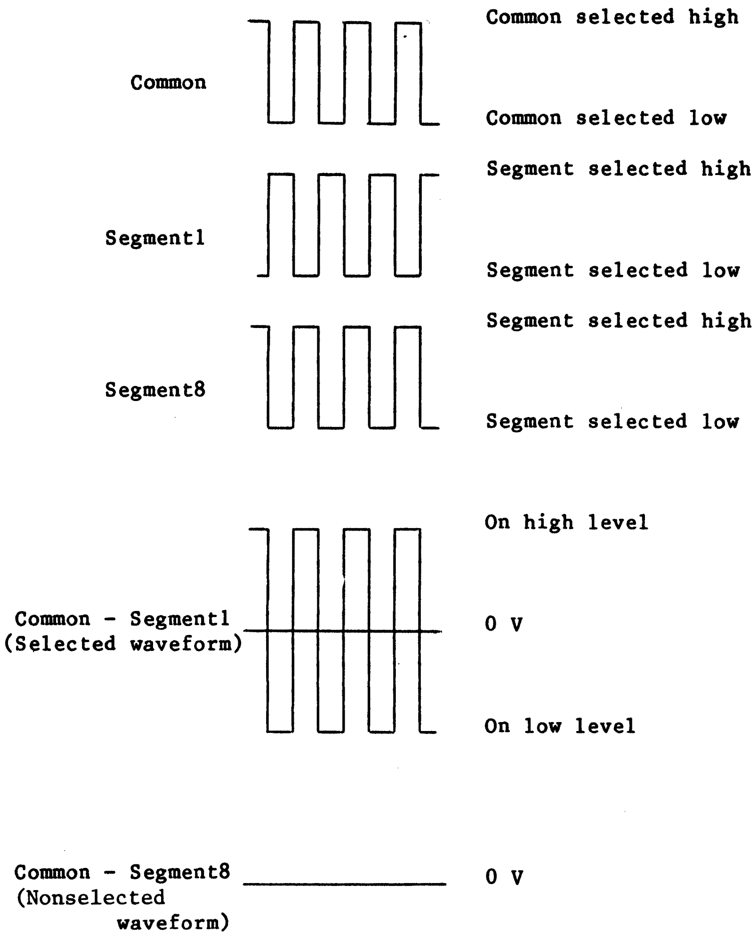


(1) Static Drive Method

(2) Multiplexing Drive Method

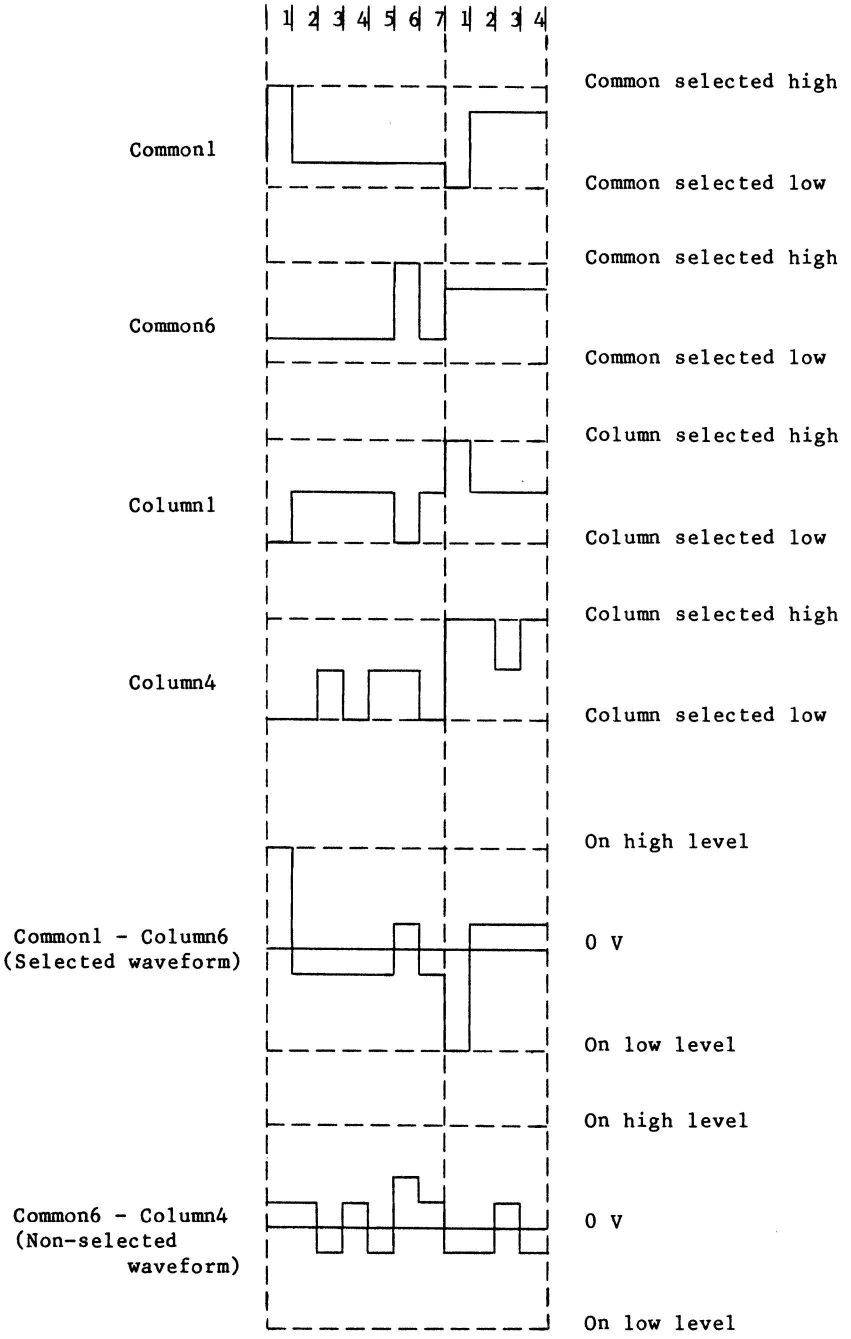
Figure 2-2 Static Drive Method and Multiplexing Drive Method

Figure 2-3 shows LCD drive waveforms. Since the DC voltage affects the liquid crystals, the drive waveforms of both the common and column pins should be alternated. The LCD driver generates the drive waveforms from the display data. For more details, refer to <u>LCD Driver LSI Data Book</u>.



(1) Static drive waveform

Figure 2-3 LCD Drive Waveforms



(2) Multiplexing drive waveform
(1/4 bias, 1/7 duty)

Figure 2-3 LCD Drive Waveforms

3. LCTC CONFIGURATION

3.1 LCTC Configuration

The HD63645F/HD64645F (LCTC) is software compatible with the HD6845 (CRTC). Therefore the display system is easily replaced from the CRT display to the LCD by using the LCTC. The LCTC supports high resolution liquid crystal display and offers versatile character attributes. It controls the large size LCD screen with a variety of display functions. The pin arrangement of the HD63645F/HD64645F is shown in Figure 3-2, and the internal block diagram in Figure 3-3.

The internal configuration of the LCTC is as follows;

(1) CRTC compatible registers (AR, R0, R1, R9-R15)

These registers are commonly equipped for CRT screen display and LCD controlled by the MPU. The display format is mostly determined by them.

(2) Registers peculiar to the LCTC (R18-R22)

These registers are specially equipped for LCD, controlled by the MPU. The extended display functions are also provided by them.

(3) Timing signal generator

This circuit generates M, FLM, CL1, CL2 (control signals for the LCD driver), RA_0-RA_4 (raster address signals), DISPTMG, and MCLK (memory access timing signals).

(4) Linear address generator

This circuit generates MA_0-MA_{15}, the frame buffer addresses. The LCTC accesses the frame buffer periodically using these address signals. It also generates DRAM refresh signals as shown in 6.5, "DRAM Refresh Address Output Function."

(5) Cursor controller

This circuit controls the cursor position, shape, and blinking.

(6) LCD data converter

This circuit converts the data transferred from the frame buffer or the character generator into 4-bit data and then outputs them to the LCD driver. It also operates the attributes such as reverse video, and OR function such as superimposition of characters and graphics.

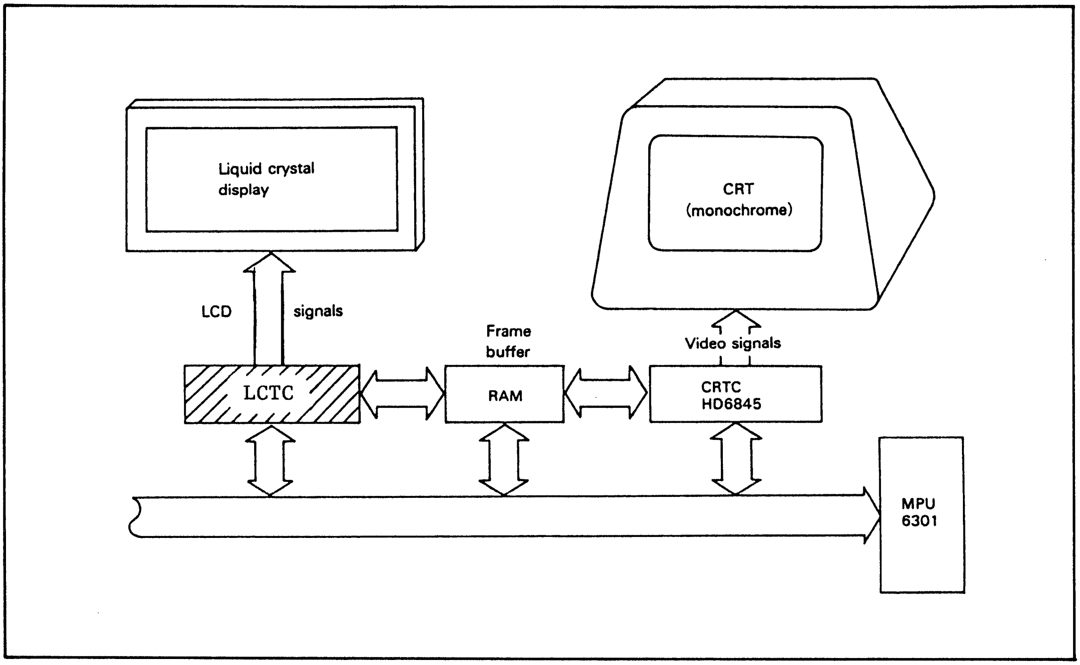
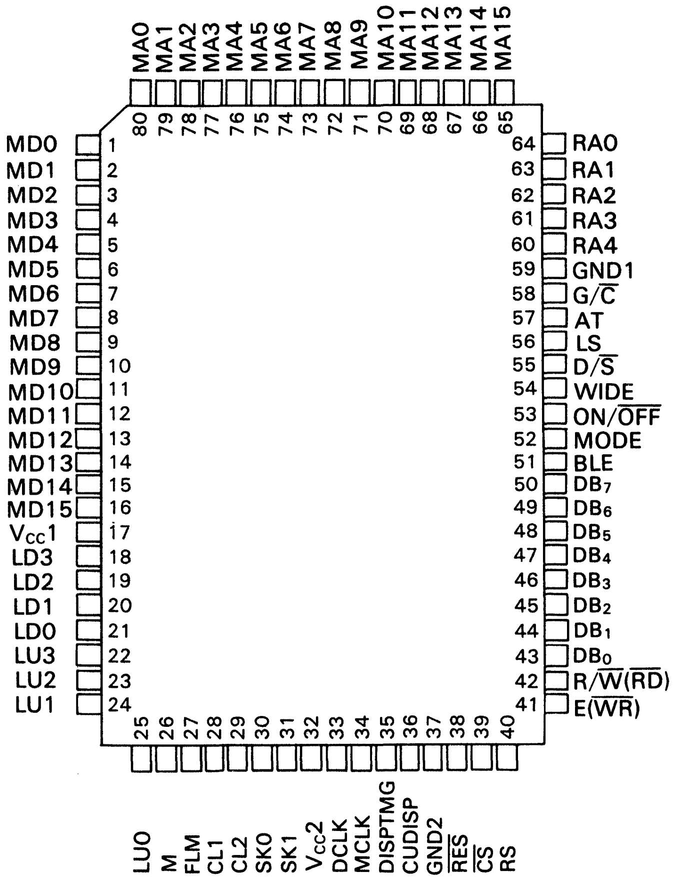


Figure 3-1 · LCD and CRT Display System

3.2 Pin Arrangement



( ) is for HD64645, HD64646

Figure 3-2 LCTC Pin Arrangement

3.3 Pin Functions

3.3.1 Pin description

Symbol	Pin Number	Name	I/O
V_{CC1}, V_{CC2}	17, 32	V_{CC}	-
GND1, GND2	37, 59	Ground	-
LU_0-LU_3	22-25	LCD up panel data 0-3	O
LD_0-LD_3	18-21	LCD down panel data 0-3	O
CL1	28	Clock 1	O
CL2	29	Clock 2	O
FLM	27	First line marker	O
M	26	M	O
MA_0-MA_{15}	65-80	Memory addresses 0-15	O
RA_0-RA_4	60-64	Raster addresses 0-4	O
MD_0-MD_7	1-8	Memory data 0-7	I
MD_8-MD_{15}	9-16	Memory data 8-15	I
DB_0-DB_7	43-50	Data buses 0-7	I/O
$\overline{CS}$	39	Chip select	I
E	41	Enable (HD63645 only)	I
$R/\overline{W}$	42	Read/write (HD63645 only)	I
$\overline{WR}$	41	Write(HD64645, HD64646 only)	I
$\overline{RD}$	42	Read(HD64645, HD64646 only)	I
RS	40	Register select	I
$\overline{RES}$	38	Reset	I
DCLK	33	D clock	I
MCLK	34	M clock	O
DISPTMG	35	Display timing	O
CUDISP	36	Cursor display	O
SK0	30	Skew 0	I
SK1	31	Skew 1	I
$ON/\overline{OFF}$	53	On/off	I
BLE	51	Blink enable	I
AT	57	Attribute	I
$G/\overline{C}$	58	Graphic/character	I
WIDE	54	Wide	I
LS	56	Large screen	I
$D/\overline{S}$	55	Dual/single	I
MODE	52	Mode	I

3.3.2 Pin functions

Power supply ($V_{CC}1$, 2, GND)

Power supply pin (+5 V): Connect V_{CC1} and V_{CC2} with +5 V power supply circuit.

Ground pin (0 V): Connect GND1 and GND2 with 0 V.

LCD interface

LCD up panel data (LU_0-LU_3), LCD down panel data (LD_0-LD_3): LU_0-LU_3 and LD_0-LD3 output LCD data as shown in Table 3-1.

Clock 1 (CL1): CL1 supplies timing clocks for display data latch.

Clock 2 (CL2): CL2 supplies timing clocks for display data shift.

First line marker (FLM): FLM supplies first line marker.

M (M): M converts liquid crystal drive output to AC.

Memory interface

Memory addresses (MA_0-MA_{15}): MA_0-MA_{15} supply the display memory address.

Raster addresses (RA_0-RA_4): RA_0-RA_4 supply the raster address.

Memory data (MD_0-MD_7): MD_0-MD_7 receive the character dot data and bitmap data.

Memory data (MD_8-MD_{15}): MD_8-MD_{15} receive attribute code data and bitmap data.

MPU interface

Data buses (DB_0-DB_7): DB_0-DB_7 send and receive data as a tristate I/O common bus.

Chip select ($\overline{CS}$): $\overline{CS}$ selects a chip. Low level enables MPU read/write of the LCTC internal registers.

Enable (E): E receives an enable clock. (HD63645 only.)

Read/write (R/$\overline{W}$): R/$\overline{W}$ enables MPU read of the LCTC internal registers when R/$\overline{W}$ is high, and MPU write when low. (HD63645 only.)

Write ($\overline{WR}$): $\overline{WR}$ receives MPU write signal. (HD64645, HD64646 only.)

Read ($\overline{RD}$): $\overline{RD}$ receives MPU read signal. (HD64645, HD64646 only.)

Register select (RS): RS selects a register. Refer to Table 4-3.

Reset ($\overline{RES}$): $\overline{RES}$ performs external reset of the LCTC. Low level of $\overline{RES}$ stops and zero-clears the LCTC internal counter. No register contents are affected.

Timing signal

D clock (DCLK): DCLK inputs the system clock.

M clock (MCLK): MCLK incicates memory cycle; DCLK is divided by four.

Display timing (DISPTMG): DISPTMG high indicates that the LCTC is reading display data.

Cursor display (CUDISP): CUDISP supplies cursor display timing; connect with MD_{12} in the character mode.

Skew 0 (SK0), skew 1 (SK1): SK0 and SK1 control skew timing. Refer to Table 3-2.

Mode select

The mode select pins ON/$\overline{OFF}$, BLE, AT, G/$\overline{C}$, and WIDE are ORed with the mode register (R22) to determine the mode.

Table 3-1 LCD Up Panel Data and LCD Down Panel Data

Pin Name	Single Screen		Dual Screen
	4-Bit Data	8-Bit Data	
LU_0-LU_3	Data output	Data output	Data output for up panel
LD0-LD3	Disconnected	Data output	Data output for down panel

On/off (ON/$\overline{\text{OFF}}$): ON/$\overline{\text{OFF}}$ switches display on and off. (High = display.)

Blink enable (BLE): BLE high level enables attribute code "blinking" (MD_{13}) and provides normal/blank blinking of specified characters for 32 frames each.

Attribute (AT): AT controls character attribute functions.

Graphic/character (G/$\overline{\text{C}}$): G/$\overline{\text{C}}$ switches between graphic and character display mode. (Graphic display when high.)

Wide (WIDE): WIDE switches between normal and wide display mode. (High = wide display, low = normal display.)

Large screen (LS): LS controls a large screen. LS high provides a data transfer speed of 40 Mbits/sec for graphic display. Also used to specify 8-bit LCD interface mode. For more details, refer to 5.4, "Mode List."

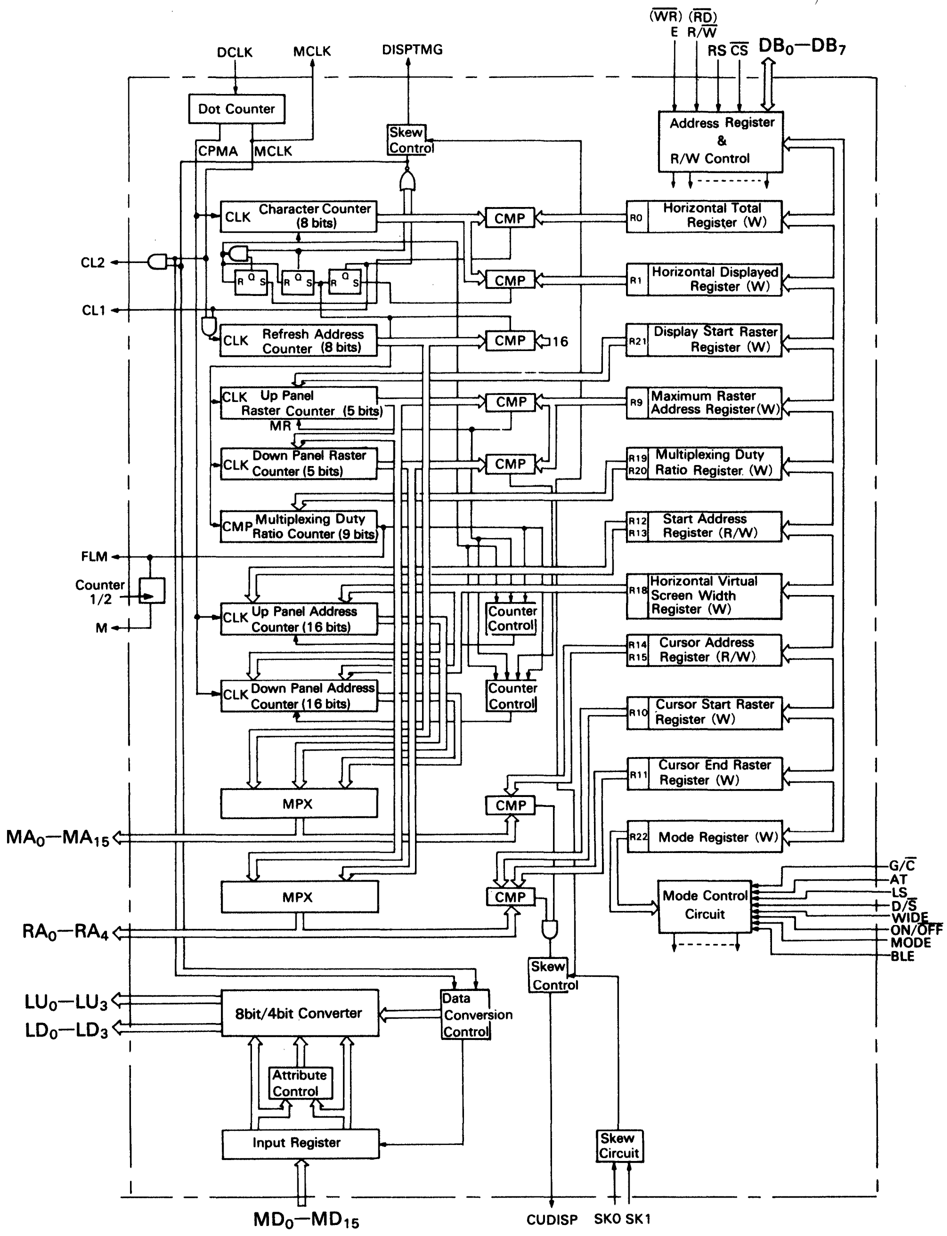
Dual/single (D/$\overline{\text{S}}$): D/$\overline{\text{S}}$ switches between single and dual screen display. (Dual screen display when high.)

Mode (MODE): MODE controls easy mode. MODE high sets duty ratio, maximum number of rasters, cursor start/end rasters, etc. Refer to Table 5-1.

Table 3-2 Skew Signals

SK0	SK1	Skew Function
0	0	No skew
1	0	1-character clock time skew
0	1	2-character clock time skew
1	1	Inhibited combination

3.4 Internal Block Diagram



(WR) (RD)
E R/W
RS CS
DB_0—DB_7
DCLK
MCLK
DISPTMG
Dot Counter
Skew Control
CPMA
MCLK
Address Register & R/W Control
Character Counter (8 bits)
CLK
CMP
R0 Horizontal Total Register (W)
CL2
CL1
R Q S
R1 Horizontal Displayed Register (W)
Refresh Address Counter (8 bits)
16
R21 Display Start Raster Register (W)
Up Panel Raster Counter (5 bits)
MR
R9 Maximum Raster Address Register (W)
Down Panel Raster Counter (5 bits)
R19 R20 Multiplexing Duty Ratio Register (W)
Multiplexing Duty Ratio Counter (9 bits)
R12 R13 Start Address Register (R/W)
FLM
Counter 1/2
M
R18 Horizontal Virtual Screen Width Register (W)
Up Panel Address Counter (16 bits)
Counter Control
R14 R15 Cursor Address Register (R/W)
Down Panel Address Counter (16 bits)
Counter Control
R10 Cursor Start Raster Register (W)
R11 Cursor End Raster Register (W)
MPX
MA_0—MA_{15}
R22 Mode Register (W)
G/C
AT
LS
D/S
WIDE
ON/OFF
MODE
BLE
Mode Control Circuit
MPX
RA_0—RA_4
Skew Control
LU_0—LU_3
LD_0—LD_3
8bit/4bit Converter
Data Conversion Control
Attribute Control
Input Register
Skew Circuit
MD_0—MD_{15}
CUDISP
SK0 SK1

( ) is for HD64645, HD64646 (80 family bus interface)

Figure 3-3 LCTC Internal Block Diagram

4. INTERNAL REGISTERS

4.1 Internal Register Comparison between LCTC and CRTC

Table 4-1 Internal Register Comparison between LCTC and CRTC

Reg. No.	LCTC		CRTC HD6845
AR	Address register	CRTC compatible registers	Address register
R0	Horizontal total characters		Horizontal total characters
R1	Horizontal displayed characters		Horizontal displayed characters
R2	---	Invalid registers	Horizontal sync position
R3	---		Sync width
R4	---		Vertical total rows
R5	---		Vertical total adjust
R6	---		Vertical displayed rows
R7	---		Vertical sync position
R8	---		Interlace mode and skew
R9	Maximum raster address	CRTC compatible registers	Maximum raster address
R10	Cursor start raster		Cursor start raster
R11	Cursor end raster		Cursor end raster
R12	Start address (H)		Start address (H)
R13	Start address (L)		Start address (L)
R14	Cursor address (H)		Cursor (H)
R15	Cursor address (L)		Cursor (L)
R16	---	Invalid registers	Light pen (H)
R17	---		Light pen (L)
R18	Horizontal virtual screen width	Additional registers	---
R19	Multiplexing duty ratio (H)		---
R20	Multiplexing duty ratio (L)		---
R21	Display start raster		---
R22	Mode register		---

The LCTC is provided with unique internal register configuration to allow display compatible in software with the CRTC.

As seen from Table 4-1, the LCTC registers are composed of "CRTC compatible registers", "invalid registers" and "additional registers". The "CRTC compatible registers" are registers required for CRT/LCD diaplay. The "invalid registers" are registers required for CRT display, not for LCD, or replaceable with another concept. The "additional registers" are indispensable for LCD or provided with functions greater than the CRTC.

The LCTC never accepts an entry of "invalid registers" No. into the address registers even if attempted.

Table 4-2 Internal Register Configuration

$\overline{CS}$	RS	Address Register 4 3 2 1 0	Reg. No.	Register Name	Program Unit	Symbol	R/W	Data Bit 7	6	5	4	3	2	1	0
1	-	- - - - - -		Invalid	-	-	-	▨	▨	▨	▨	▨	▨	▨	▨
0	0	- - - - - -	AR	Address register	-	-	W	▨	▨	▨					
0	1	0 0 0 0 0	R0	Horizontal total characters *1	Character	Nht	W								
0	1	0 0 0 0 1	R1	Horizontal displayed characters	Character	Nhd	W								
0	1	0 1 0 0 1	R9	Maximum raster address	Raster	Nr	W	▨	▨	▨					
0	1	0 1 0 1 0	R10	Cursor start raster	Raster	Ncs	W	▨	B	P					
0	1	0 1 0 1 1	R11	Cursor end raster	Raster	Nce	W	▨	▨	▨					
0	1	0 1 1 0 0	R12	Start address (H)	Memory address	-	R/W								
0	1	0 1 1 0 1	R13	Start address (L)	Memory address	-	R/W								
0	1	0 1 1 1 0	R14	Cursor address (H)	Memory address	-	R/W								
0	1	0 1 1 1 1	R15	Cursor address (L)	Memory address	-	R/W								
0	1	1 0 0 1 0	R18	Horizontal virtual screen width	Character	Nir	W								
0	1	1 0 0 1 1	R19	Multiplexing duty ratio (H)	Raster	Ndh	W	▨	▨	▨	▨	▨	▨	▨	
0	1	1 0 1 0 0	R20	Multiplexing duty ratio (L) *1	Raster	Ndl	W								
0	1	1 0 1 0 1	R21	Display start raster	Raster	Nsr	W	▨	▨	▨					
0	1	1 0 1 1 0	R22	Mode register *2		-	W	▨	▨	▨	ON/$\overline{\text{OFF}}$	G/$\overline{C}$	WIDE	BLE	AT

Notes 1) ▨: Invalid data bits.

2) R/W shows whether the CPU can only write into the register, or can both write into and read from the register.

W : Only writing into is possible.
R/W: Both writing into and reading from are possible.

3) The "value to be specified - 1" should be programmed in *1-marked registers.

4) The data bits 5 and 6 of cursor start raster register control the cursor display as shown below. (For more details, refer to 10.2.1.)

B	P	Cursor Blink Mode
0	0	Cursor on; without blinking
0	1	Cursor off
1	0	Blinking every 32-frame
1	1	Blinking every 64-frame

5) The registers R2-R8, R16, and R17 are not assigned for the LCTC. Programming these register Nos. will be ignored.

6) The OR of the MODE pin status and the register data marked with *2 determines the mode.

Table 4-3 Internal Register Description

Reg. No.	Register Name	Description
AR	Address register	Specifies the internal control registers (R0, R1, R9-R15, R18-R22) address to be accessed (5 bits).
R0	Horizontal total characters	Specifies the horizontal scanning period (8 bits).
R1	Horizontal displayed characters	Specifies the number of displayed characters per character row (8 bits).
R9	Maximum raster address	Specifies the number of rasters per character row; including the space between character rows (5 bits).
R10	Cursor start raster	Specifies the cursor start raster address and its blink mode (5 + 2 bits).
R11	Cursor end raster	Specifies the cursor end raster address (5 bits).
R12	Start address (H)	Specifies the display start address (16 bits).
R13	Start address (L)	
R14	Cursor address (H)	Specifies the cursor display address (16 bits).
R15	Cursor address (L)	
R18	Horizontal virtual screen width	Specifies the number of characters of a character row in memory space, for horizontal scrolling (8 bits).
R19	Multiplexing duty ratio (H)	Specifies the number of rasters of a screen (16 bits).
R20	Multiplexing duty ratio (L)	
R21	Display start raster	Specifies the display start raster address of the first character row, for smooth scrolling (5 bits).
R22	Mode register	Controls the display mode (5 bits).

* For more details of registers, refer to 4.4, "Internal Register Functions."

4.4 Internal Register Functions

(1) Address register (AR)

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0	—	W
-	-	-	Register address						

This register selects specified one out of 13 kinds of data registers. The address data is written into the address register through DB_0-DB_4 pins when RS = low (RS = high for data registers). If no register corresponding to a specified address number exists, the address data will be ignored.

(2) Horizontal total characters register (R0)

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0	Character	W
Nht (Total characters - 1)									

This register specifies the horizontal scanning period. The LCTC occupies a memory during the horizontal scanning period. Memory contents must be rewritten within the horizontal retrace period (horizontal total characters - horizontal displayed characters).

The unit of set value (Nht) of this register is the number of characters, not time. So the horizontal scanning period must be converted into the number of characters. How to determine the horizontal total characters will be explained in 7.4.2.

(3) Horizontal displayed characters register (R1)

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0	Character	W
Nhd (Displayed characters)									

This register specifies the number of displayed characters per character row. The horizontal character pitches are 8 dots for normal character display and 16 dots for wide character display and graphic display. Nhd should be obtained by dividing the number of horizontal dots of an LCD screen by 8 or 16 dots respectively. Note that the relation between Nht and Nhd has the restrictions shown in 4.5.

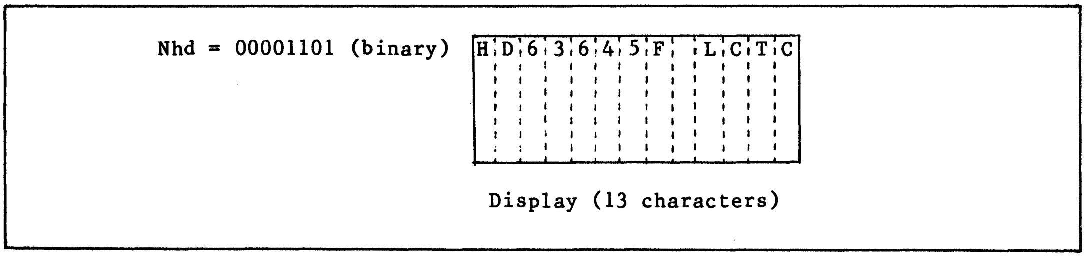


Figure 4-1 Example of Setting the Horizontal Displayed Characters for Normal Character Display

(4) Maximum raster address register (R9)

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0	Raster	W
—	—	—	Nr						

This register specifies the number of vertical dots (rasters) per character row, consisting of 5 bits. $00 (character composed of a vertical dot) up to $1F (character composed of 32 vertical dots) can be programmed in this register.

Nr should be n - 1, when the number of rasters in a character row is n.

This register is invalid when the mode is set for the graphic 1 display (mode 3, 7, 11, or 13.) However, RA0-RA4 pins operate according to the programmed value in this register.

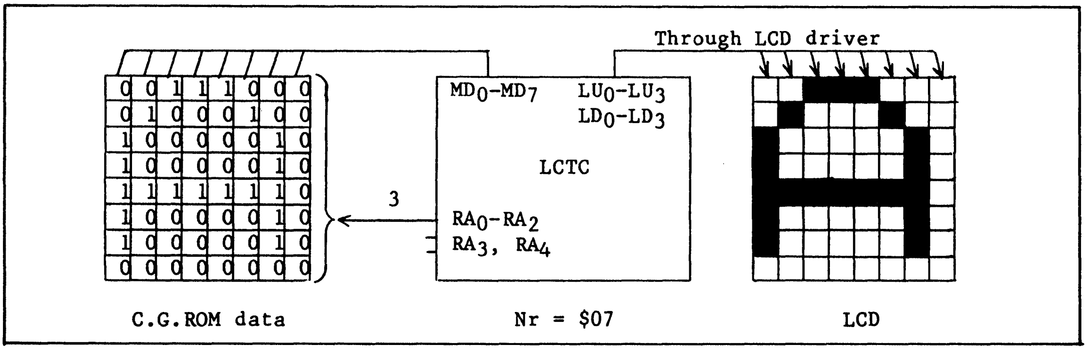


Figure 4-2 Display Example in which Maximum Raster Address is Specified 7

(5) Cursor start raster register (R10)

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0	Raster	W
-	B	P	Ncs (Raster address)						

This register specifies the cursor start raster address and its blink mode.

This register is invalid when the mode is set for the graphic display (mode 3, 4, 7, 8, 11, 12, or 13).

B	P	Cursor blink mode
0	0	Cursor on; without blinking
0	1	Cursor off
1	0	Blinking every 32-frame
1	1	Blinking every 64-frame

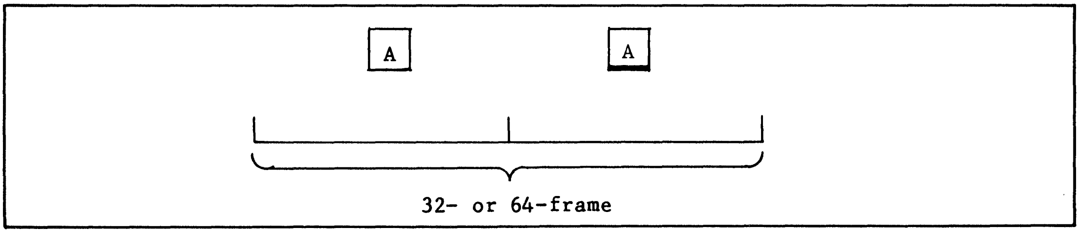


Figure 4-3 Cursor Blink Mode

(6) Cursor end raster register (R11)

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
-	-	-	Nce (Raster address)					Raster	W

This register specifies the cursor end raster address. Together with (R10), it determines the cursor display raster position and cursor height. The following condition must be satisfied in setting (R11); (R9) $\geq$ (R11) $\geq$ (R10)

This register is invalid when the mode is set for the graphic display (mode 3, 4, 7, 8, 11, 12, or 13).

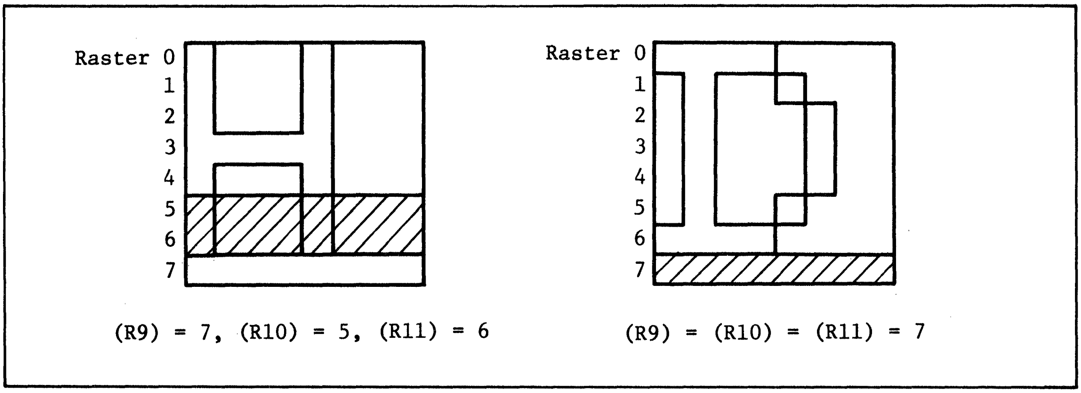


Figure 4-4 Relation among (R9), (R10), and (R11)

(7) Start address registers (H/L) (R12/R13)

Data bit								Program Unit	R/W	
7	6	5	4	3	2	1	0			
Start address (H)								Memory address	R/W	(R12)
Start address (L)										(R13)

Each register specifies the frame buffer read start address. The data read will be displayed on the upper-left end of the screen. Rewriting this register facilitates paging and scrolling. This register is composed of 16 bits of (R12) + (R13).

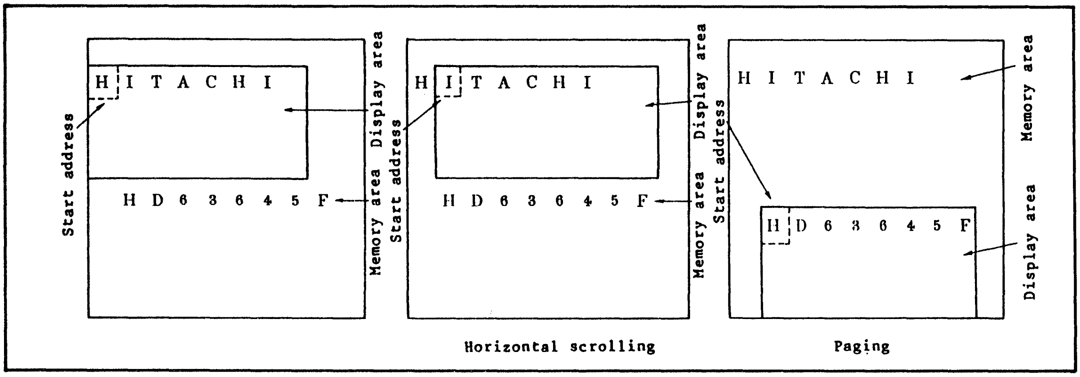


Figure 4-5 Example of Start Address Renewal (Nhd = 8, Nir = 10)

(8) Cursor address registers (H/L) (R14/R15)

Data bit								Program Unit	R/W	
7	6	5	4	3	2	1	0			
Cursor address (H)								Memory address	R/W	(R14)
Cursor address (L)										(R15)

Each register specifies the cursor display address. Cursor display requires setting of (R10) and (R11), and the CUDISP pin should be connected with MD_{12} (in the character mode). For more details of cursor control, refer to chapter 10. If no cursor address is in a space being displayed, read data from the register to make a check. This register is composed of 16 bits of (R14) + (R15).

This register is invalid when the mode is set for the graphic display (mode 3, 4, 7, 8, 11, 12 or 13).

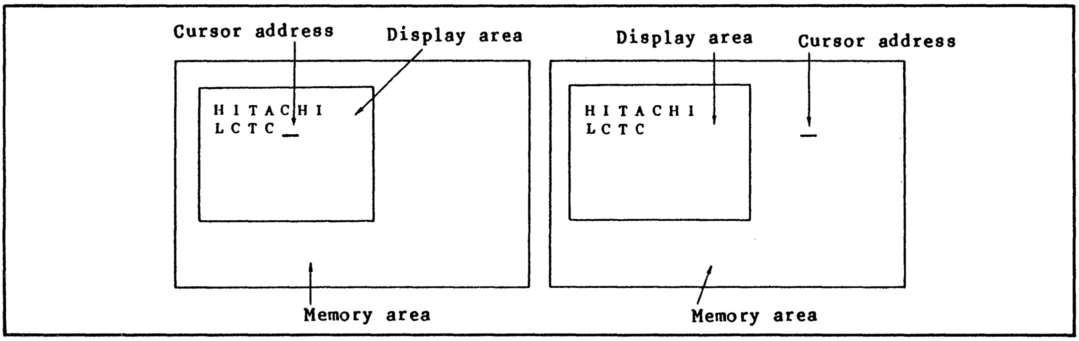


Figure 4-6 Example of Cursor Address Difference

(9) Horizontal virtual screen width register (R18)

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
Nir (No. of chars. of virtual screen width)								Character	W

This register facilitates horizontal scrolling by character by setting the memory width larger than the number of horizontal displayed characters. Conventionally, a display area has a continuous memory address configuration, as shown in Figure 4-7(1). However, this register enables the display to be a two-dimensionally wide memory space is looked in, shown in Figure 4-7(2).

When you do not use this function, write the same value as that in the horizontal displayed characters register (R1).

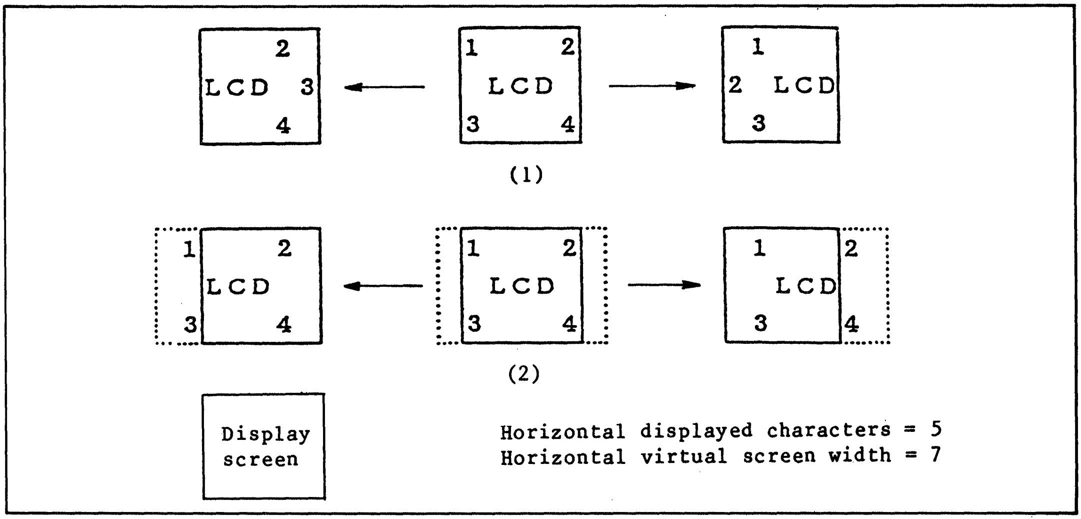

2
LCD 3
4
1 2
LCD
3 4
1
2 LCD
3
(1)
1 2
LCD
3 4
1 2
LCD
3 4
1 2
LCD
3 4
(2)
Display screen
Horizontal displayed characters = 5
Horizontal virtual screen width = 7

Figure 4-7 Display without Virtual Screen Width (1) and with Virtual Screen Width (2)

(10) Multiplexing duty ratio registers (H/L) (R19/R20)

Data Bit								Program Unit	R/W	
7	6	5	4	3	2	1	0			
-	-	-	-	-	-	-	Ndh*	Raster	W	(R19)
Ndl (Number of rasters - 1)										(R20)

*: Number of rasters - 1

This register specifies the number of common output pins required for an LCD screen by both of (R19) and (R20).

o Single LCD screen: (Register set value) = number of vertical dots - 1

o Dual LCD screen: (Register set value) = $\dfrac{\text{number of vertical dots}}{2} - 1$

Remember to keep the following conditions about the data transfer speed specified by mode setting (refer to Table 5-1);

(Number of horizontal dots) x (number of vertical dots) x (frame frequency) $\leq$ (data transfer speed)

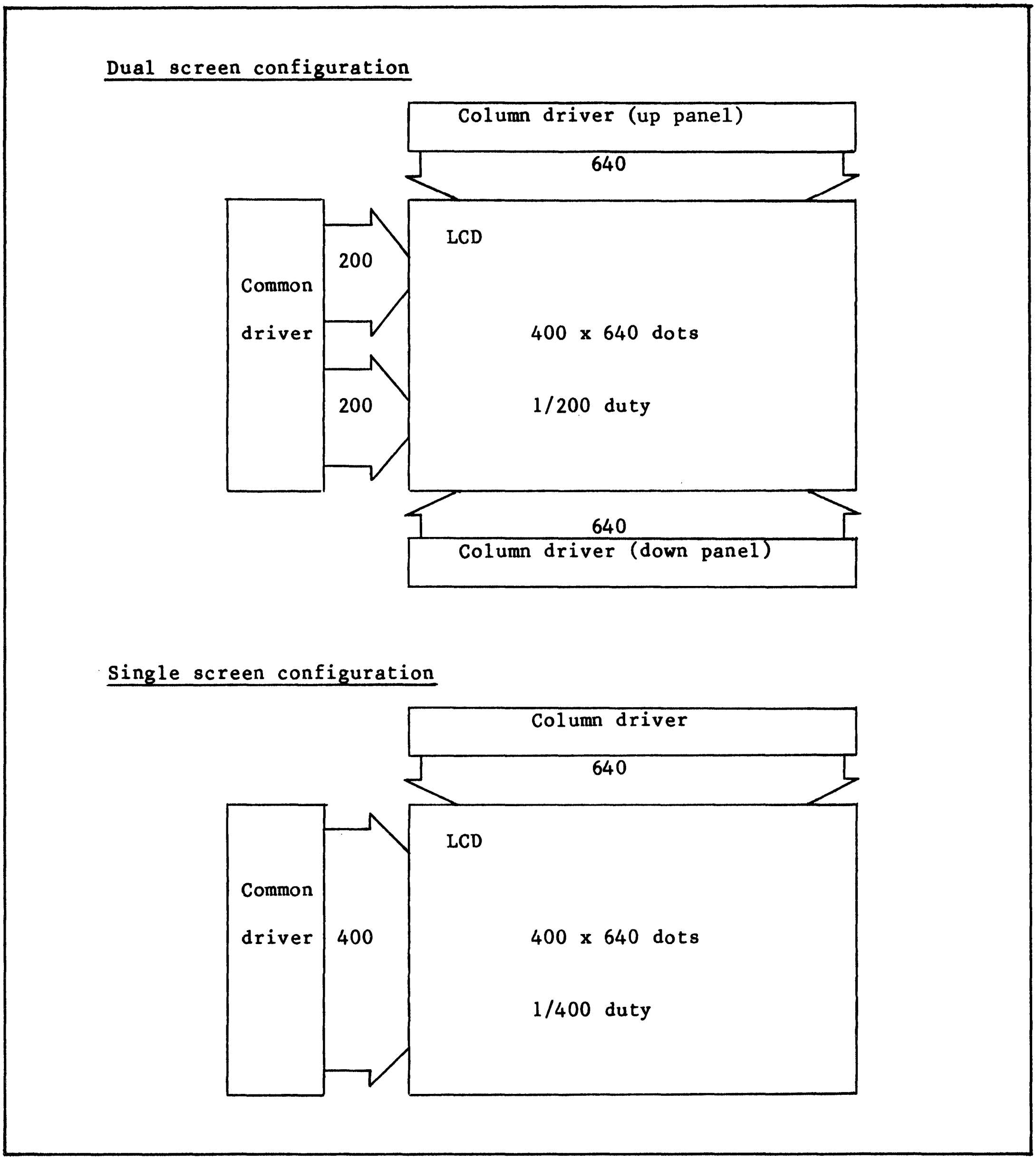


Figure 4-8 Multiplexing Duty Ratio and Screen Configurations

(11) Display start raster register (R21)

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
–	–	–	Nsr (Raster address)					Raster	W

This register specifies the start raster of the character row displayed on the top of a screen, facilitating vertical smooth scrolling. When the register is set, the display start raster should be equal or less than the maximum raster address. For the example of smooth scrolling, see Figure 4-9.

This register is invalid when the mode is set for the graphic display (mode 3, 4, 7, 8, 11, 12, or 13).

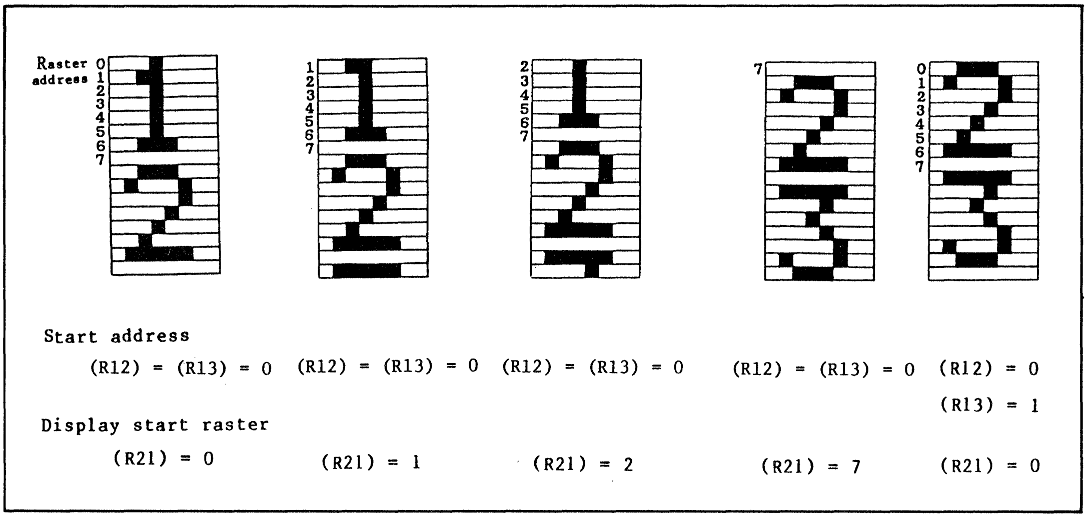


Figure 4-9 Example of Smooth Scrolling

(12) Mode register (R22)

Data Bit								Program Unit	R/W
7	6	5	4	3	2	1	0		
-	-	-	ON/$\overline{\text{OFF}}$	G/$\overline{\text{C}}$	WIDE	BLE	AT	-	W

The OR of the data bits of R22 register and the external pins of the same name determines a particular mode (Figure 4-10).

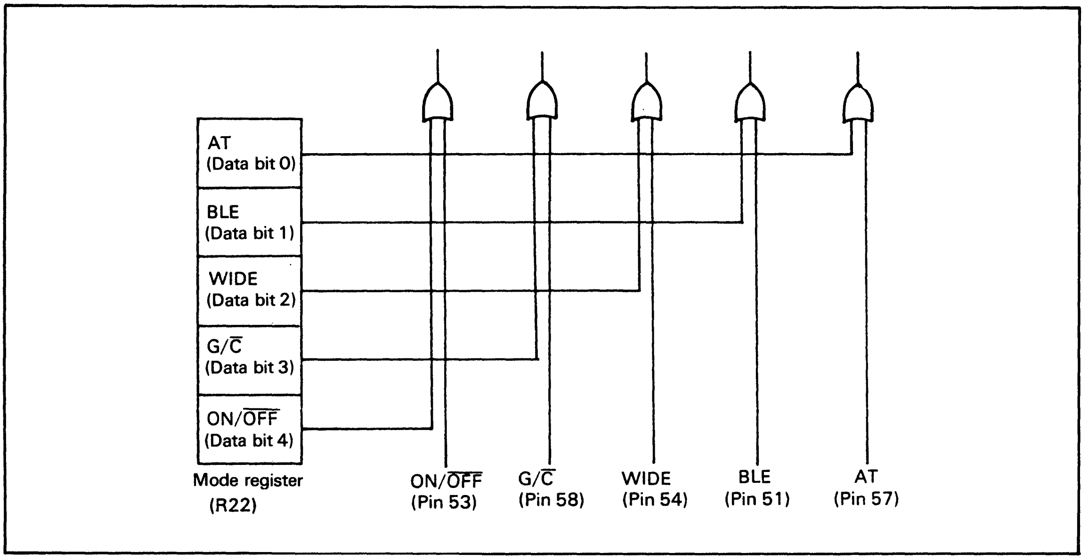

AT (Data bit 0)
BLE (Data bit 1)
WIDE (Data bit 2)
G/$\overline{\text{C}}$ (Data bit 3)
ON/$\overline{\text{OFF}}$ (Data bit 4)
Mode register (R22)
ON/$\overline{\text{OFF}}$ (Pin 53)
G/$\overline{\text{C}}$ (Pin 58)
WIDE (Pin 54)
BLE (Pin 51)
AT (Pin 57)

Figure 4-10 Correspondence between Mode Register and External Pins

Notes: 1. AT (valid only when G/$\overline{\text{C}}$ is low (character mode))
AT = high; Attribute functions enabled, OR function disabled.
AT = low; OR function enabled, attribute functions disabled.

2. BLE (valid only when G/$\overline{\text{C}}$ is low (character mode))
BLE = high; Blinking enable on the character specified by attribute RAM
BLE = low; No blinking

3. WIDE (valid only when G/$\overline{\text{C}}$ is low (character mode))
WIDE = high; Wide display enabled
WIDE = low; Normal display

4. G/$\overline{\text{C}}$
G/$\overline{\text{C}}$ = high; Graphic 1 mode display (when AT = high) or graphic 2 mode display (when AT = low)
G/$\overline{\text{C}}$ = low; Character display

5. ON/$\overline{\text{OFF}}$
ON/$\overline{\text{OFF}}$ = high; Display on state
ON/$\overline{\text{OFF}}$ = low; Display off state

4.5 Restrictions on Programming Internal Registers

Note when programming that the values you can write into the internal registers is restricted as shown in Table 4-4.

Table 4-4 Restrictions on Writing Values into the Internal Registers

Function	Restrictions	Registers
Display Format	$1 < Nhd < Nht + 1 \leq 256$ $Nhd + \frac{16}{m}$ *1 $\leq Nht + 1$	R0, R1
	(No. of vertical dots) x (no. of horizontal dots) x (frame frequency;f_{FRM}) $\leq$ (data transfer speed;V) $\{\frac{1}{2}\}$ *2 x (Nd + 1) x Nhd x $\{\frac{8}{16}\}$ *3 $f_{FRM} \leq V$	R1, R19 R20
	$Nhd \leq Nir$	R1, R18
	$0 \leq Nd \leq 511$	R19, R20
Cursor Control	$0 \leq Ncs \leq Nce$	R10, R11
	$Nce \leq Nr$	R10, R9
Smooth Scroll	$Nsr \leq Nr$	R21, R9
Memory Width Set	$0 \leq Nir \leq 255$	R18

*1 m varies according to the modes. See the following table.

Mode No.	m
5,9	1
1,6,7,8,10,11,12,13	2
2,3,4	4

*2 Set 1 when an LCD screen is a single screen, and set 2 when dual. Modes are classified as shown in the following table.

Mode No.	Value
5,6,7,8,9,10,11,12	1
1,2,3,4,13	2

*3 Set 8 when a character is constructed with 8 dots, and set 16 when with 16 dots. Modes are classified as shown in the following table.

Mode No.	Value
1,5,9	8
2,3,4,6,7,8,10,11,12,13	16

Concerning mode number, refer to Table 5-2.

4.6. Restrictions on Usage of Internal Registers

Rewriting the values in the registers from bus side asynchronously with the display operation may cause momentary flickering of the LCD. That is because the values set in the internal registers of the LSI directly control the LCD. The following registers allow you to rewrite the values during the display. (For more details, refer to "APPENDIX A."

(1) Cursor register

In writing values frequently into the cursor register for moving the cursor, write while DISPTMG is low.

(2) Start address register

In writing values frequently into the start address register for scrolling or paging, write while DISPTMG is low.

(3) Display start raster register

In writing values frequently into the display start raster register, write while DISPTMG is low.

Writing values into the other registers during the display is undesirable.

5. LCD SCREEN CONFIGURATION AND MODE SETTING

5.1 LCD System Configuration

In constructing an LCD system, you need to choose a single screen or dual screen unlike CRT.

A single screen costs less than a dual screen because of the small number of column drivers for a display and of its small mounting size. However, it has limitations considering the duty ratio, the LCD drive voltage, and the display quality of the liquid crystal. A dual screen is then necessary.

Besides, the LCTC is also capable of transferring LCD data on an 8-bit basis, which is convenient when the interval between pins supplying signals to the LCD panel is narrow. Transferring LCD data on a 4-bit basis is sufficient in using the usual LCD screens such as a single screen of 640 x 200 dots and a dual screen of 640 x 400 dots.

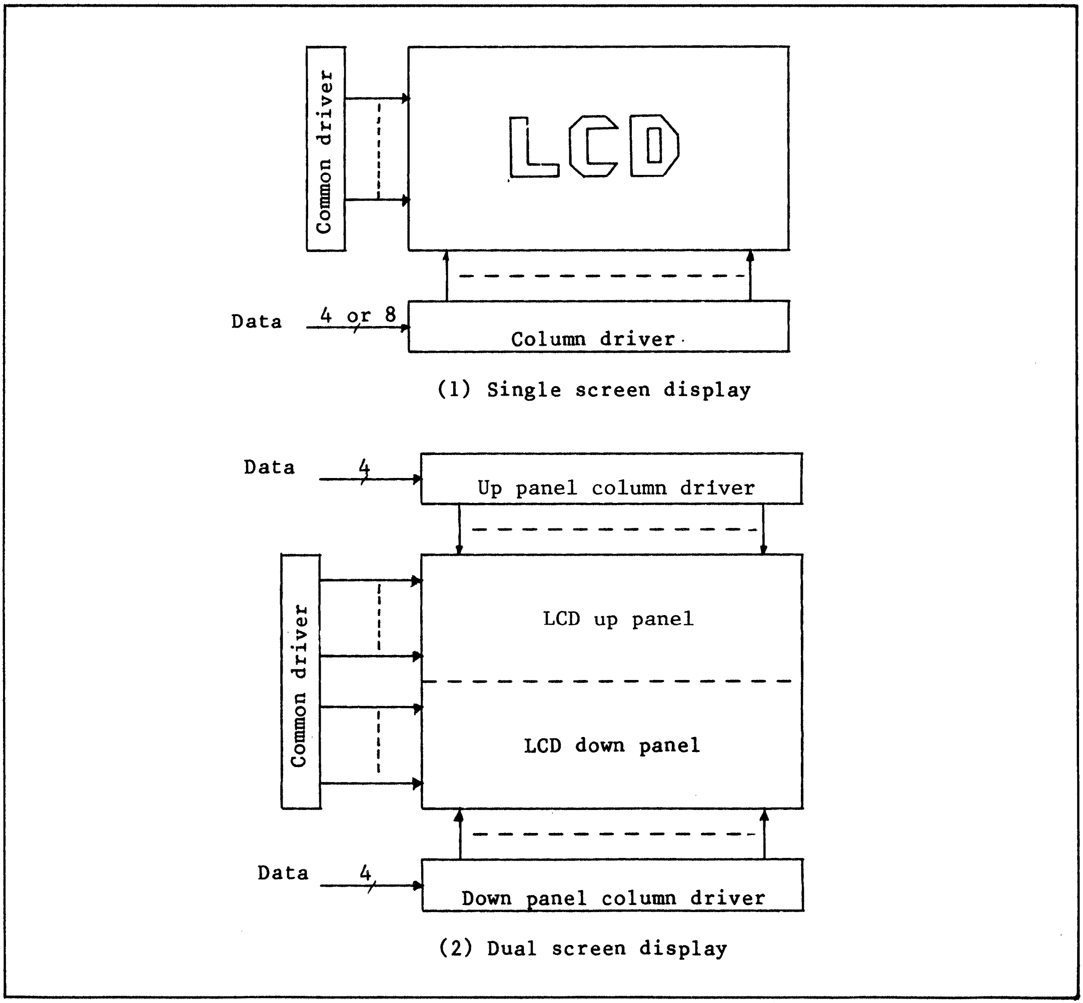


Figure 5-1 System Configuration Comparison of a Single Screen and a Dual Screen

5.2 Each System Configuration

5.2.1 Dual screen, 4-bit x 2-channel data transfer

Construct a system shown in Figure 5-2 when the mode is 1, 2, 3, 4, or 13.

The LCTC internally controls the memory addresses and the raster addresses in the character mode even when a dual screen is used. Therefore the characters spreading over the up and the down panel are displayed without a break just as when a single screen is used. Using HD61105 or so as the common driver lessens the number of drivers since it enables connecting the output pins over the two panels.

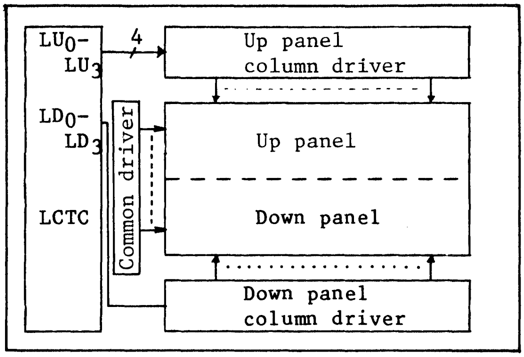


Figure 5-2
System Configuration of a Dual Screen, 4-Bit x 2-Channel Data Transfer

5.2.2 Single screen, 4-bit data transfer

Construct a system shown in Figure 5-3 when the mode is 5, 6, 7, or 8.

Display data appears at the pins LU_0-LU_3 in this system. Do not connect any wire with LD_0-LD_3 since they are not used here.

This system has limitations as to screen size depending on the drive voltage of the LCD drivers you use although it requires less number of column drivers than a dual screen does.

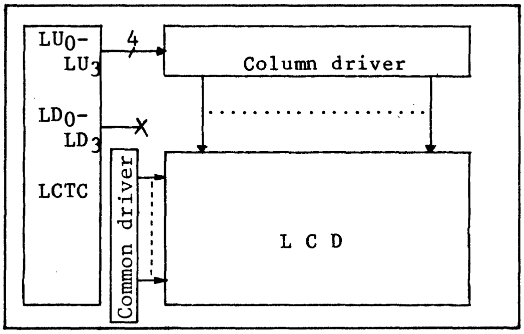


Figure 5-3
System Configuration of a Single Screen, 4-Bit Data Transfer

5.2.3 Single screen, 8-bit data transfer

Construct a system shown in Figure 5-4 when the mode is 9, 10, 11, or 12.

Data is transferred on an 8-bit basis (LU_0-LU_3 (4 bits) + LD_0-LD_3 (4 bits)) here. The data transfer capacity and other restrictions are the same as those of the modes of a single screen, 4-bit data transfer.

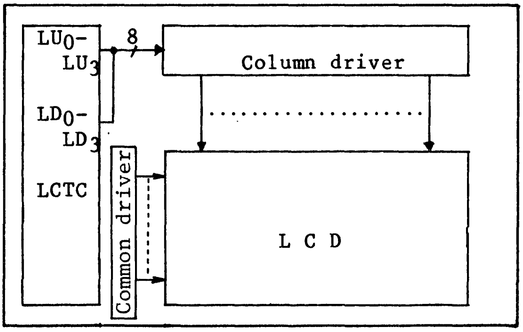


Figure 5-4
System Configuration of a Single Screen, 8-bit Data Transfer

5.3 Mode Setting

The LCTC supports the following system configurations;

(1) Single or dual screen configuration
(2) 4- or 8-bit LCD data transfer

and the following display formats;

(1) Normal or wide character display
(2) Graphic 1 mode or graphic 2 mode display

The LCTC also supports the mode for a large screen display whose data transfer speed is 40 Mbits/sec (max). (However, it supports only the display of a dual screen, graphic 1 mode.)

Table 5-1 Mode Selection

System Configuration			Display Format				
LCD Data Transfer	Screen Configuration	Screen Size	Character/Graphic	Normal/Wide	Attribute/OR	Maximum Data Transfer Speed (MBPS)	Mode No.
4-bit	Single	Normal	Character	Normal	AT OR	20	5
				Wide	AT OR	10	6
			Graphic 1			20	7
			Graphic 2			20	8
	Dual	Normal	Character	Normal	AT OR	20	1
				Wide	AT OR	10	2
			Graphic 1			20	3
			Graphic 2			20	4
		Large	Graphic 1			40	13
8-bit	Single	Normal	Character	Normal	AT OR	20	9
				Wide	AT OR	10	10
			Graphic 1			20	11
			Graphic 2			20	12

5.3.1 Screen configuration selection

The screen configuration of the LCTC display system should always be dual in the following cases;

(1) The number of the vertical dots (parallel with the common driver) of a screen exceeds 512 regardless of the number of horizontal dots (parallel with the column driver).

(2) Although the number of the vertical dots of a screen does not exceed 512, sufficient contrast is not available owing to the lack of LCD drive voltage. (Modes 5 and 9 should be switched to mode 1, modes 7 and 11 to mode 3, and modes 8 and 12 to mode 4.)

(3) The graphic display requiring the data transfer speed higher than 20 Mbits/sec is necessary. (Modes 7 and 11 should be switched to mode 13.)

5.3.2 Display format selection

The LCTC provides 4 display formats; 2 character displays (normal and wide character displays), and 2 graphic displays (graphic 1 and 2 mode displays). In using the LCTC, you need to choose one of these displays. (See Table 5-2.)

(1) Normal character display (modes 1, 5, and 9)

Normal character modes receive the data of the C.G.ROM according to the VRAM data and display the characters of 1-32 vertical dots x 8 horizontal dots (fixed). Of all the memory data, dot data is sent to the pins MD_0-MD_7 and attribute data to the pins MD_8-MD_{15}.

In these modes, the LCTC can access up to 64 kbytes of the RAM, and also the CUDISP signal appears depending on the values set in the register. (See 6.1, "Timing Charts.")

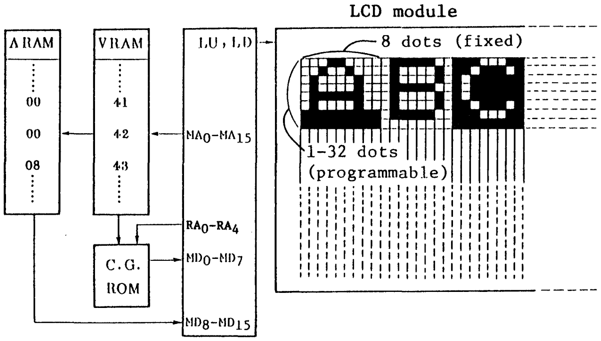
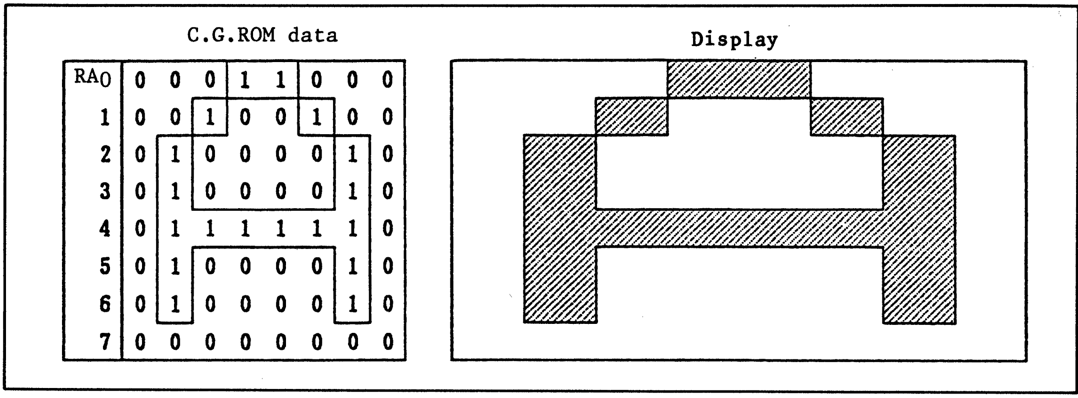


Figure 5-5 Examples of System Configuration and Display of the Normal Character Mode

(2) Wide character display (modes 2, 6, and 10)

These modes are realized with the same system configuration as that of the normal character mode. Each character is doubled in width to have 16 horizontal dots (fixed) as shown in Figure 5-6. The ARAM data is considered to be attribute data also in these modes. Conditions mentioned about the RAM access capacity and the CUDISP signal in the normal character mode applies here, too.



RA_0	0	0	0	1	1	0	0	0
1	0	0	1	0	0	1	0	0
2	0	1	0	0	0	0	1	0
3	0	1	0	0	0	0	1	0
4	0	1	1	1	1	1	1	0
5	0	1	0	0	0	0	1	0
6	0	1	0	0	0	0	1	0
7	0	0	0	0	0	0	0	0

Figure 5-6 Display Example of the Wide Character Mode

(3) Graphic 1 mode display (modes 3, 7, and 11)
These modes display the bitmap data of 2 bytes per 1 address (ARAM; 1 byte + VRAM; 1 byte). The memory addresses increase linearly in the same frame. How the raster addresses change depends on the values set in the maximum raster address register (R9).

The CUDISP signal is fixed low and attribute data is invalid.

The RAM access space is 128 kbytes (max).

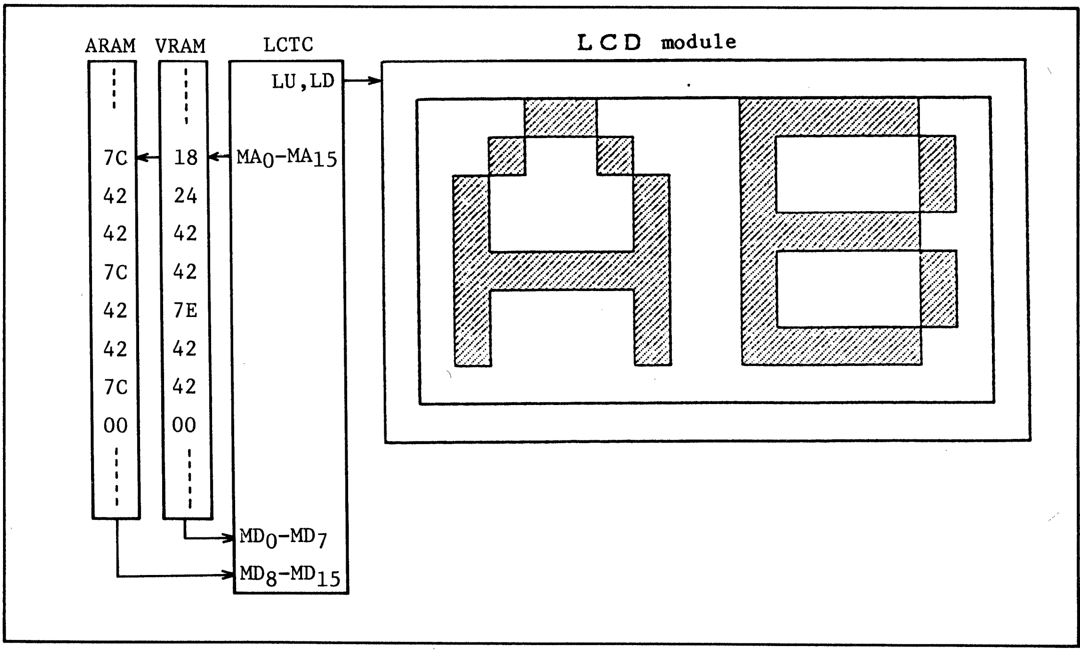
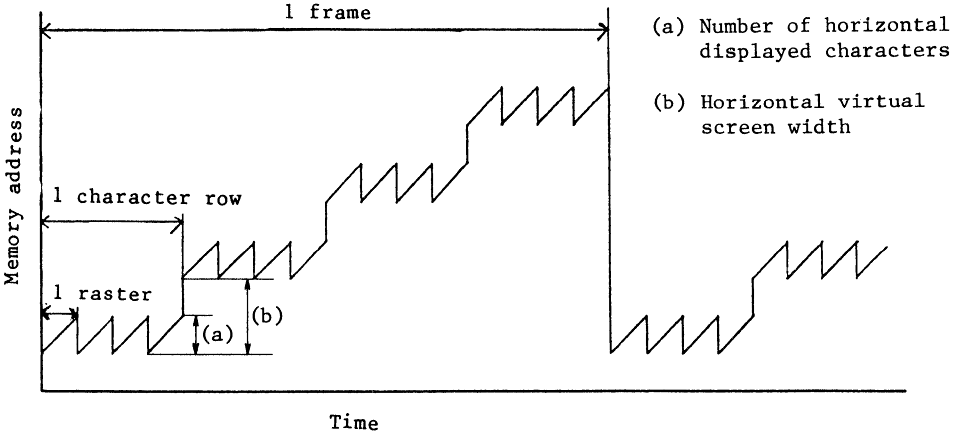


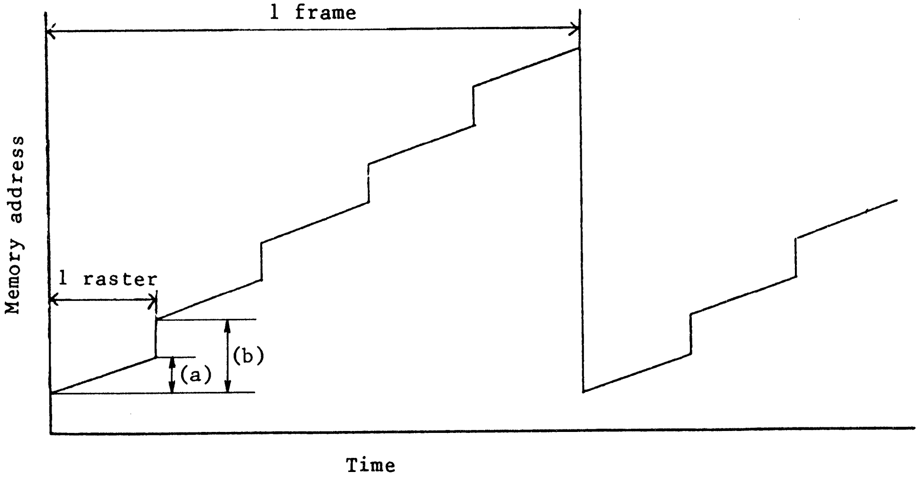
Figure 5-7 Examples of System Configuration and Display of the Graphic 1 Mode

(4) Graphic 2 mode display (modes 4, 8, and 12)

These modes are the same as the graphic 1 mode in that the LCTC displays the bitmap data of 2 bytes (ARAM + VRAM). How the memory addresses change depends on the values set in the maximum raster address register (R9) as in the character mode. (See Figure 5-8.)


1 frame
(a) Number of horizontal displayed characters
(b) Horizontal virtual screen width
Memory address
1 character row
1 raster
(a)
(b)
Time

(i) How the memory addresses change in the character mode and in the graphic 2 mode
(1 frame = 4 character rows, 1 character row = 4 rasters)



(ii) How the memory addresses change in the graphic 1 mode
(1 frame = 5 rasters)

Figure 5-8 How the Memory Addresses Change in Each Mode

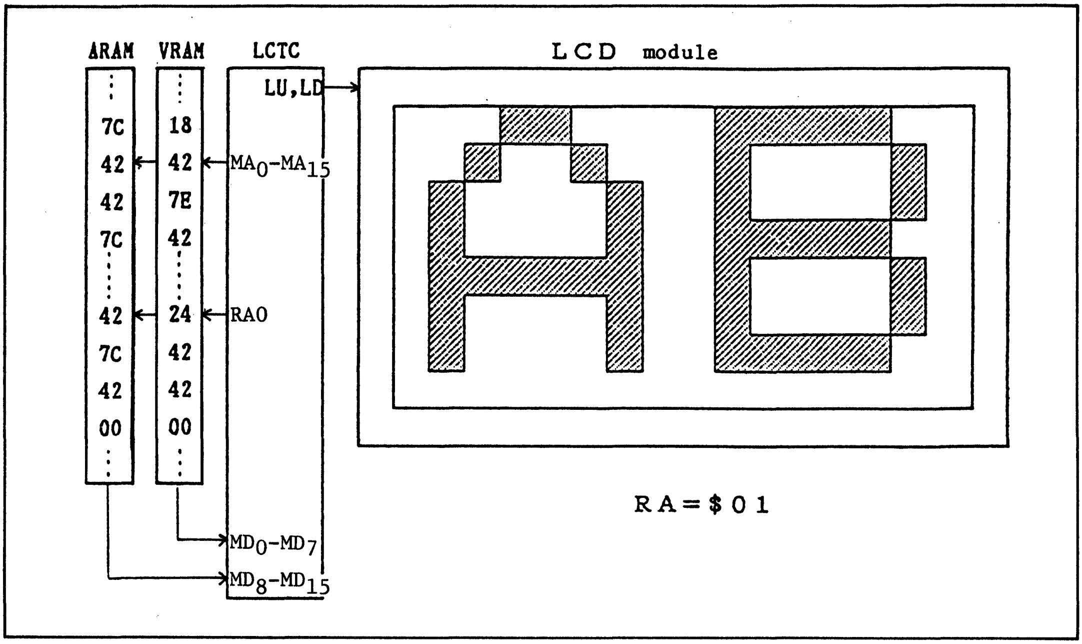


Figure 5-9 Examples of System Configuration and Display of the Graphic 2 Mode

5.4 Mode List

The LCTC provides 13 modes classified depending on the display methods and system configurations.

Table 5-2 Mode List

Item	No.	Mode Name	Pin Name D/$\overline{S}$	G/$\overline{C}$	LS	WIDE	AT	Screen Configuration	Graphic or Character	Data Transfer	Wide or Normal	Attribute	Data Transfer Speed (bits/sec) (DCLK Frequency x n)
1	1	Dual screen normal character	1	0	0	0	0	Dual	Character	4-bit x 2	Normal	OR	x 2
			1	0	0	0	1					AT	
	2	Dual screen wide character	1	0	0	1	0				Wide	OR	x 1
			1	0	0	1	1					AT	
	3	Dual screen graphic 1	1	1	0	0	1		Graphic		-	-	x 2
	4	Dual screen graphic 2	1	1	0	0	0						
2	5	Single screen normal character	0	0	0	0	0	Single	Character	4-bit	Normal	OR	
			0	0	0	0	1					AT	
	6	Single screen wide character	0	0	0	1	0				Wide	OR	x 1
			0	0	0	1	1					AT	
	7	Single screen graphic 1	0	1	0	0	1		Graphic		-	-	x 2
	8	Single screen graphic 2	0	1	0	0	0						
3	9	8-bit normal character	0	0	1	0	0		Character	8-bit	Normal	OR	
			0	0	1	0	1					AT	
	10	8-bit wide character	0	0	1	1	0				Wide	OR	x 1
			0	0	1	1	1					AT	
	11	8-bit graphic 1	0	1	1	0	1		Graphic		-	-	x 2
	12	8-bit graphic 2	0	1	1	0	0						
4	13	Large screen	1	1	1	0	1	Dual		4-bit x 2			x 4

The LCTC display mode is determined by pins D/$\overline{S}$ (pin 55), G/$\overline{C}$ (pin 58), LS (pin 56), WIDE (pin 54), and AT (pin 57). As for G/$\overline{C}$, WIDE, and AT, the OR is taken between data bits 0, 2, and 3 of the mode register (R22).

Note; The above 5 pins have 32 kinds of status combinations (1 or 0). Any combination other than the above is inhibited.

6. HD63645F/HD64645F (LCTC) PERFORMANCES

6.1 Modes and Timing Charts

6.1.1 Modes and screen size

Figure 6-1 shows the relation between the LCTC internal registers and the display screen.

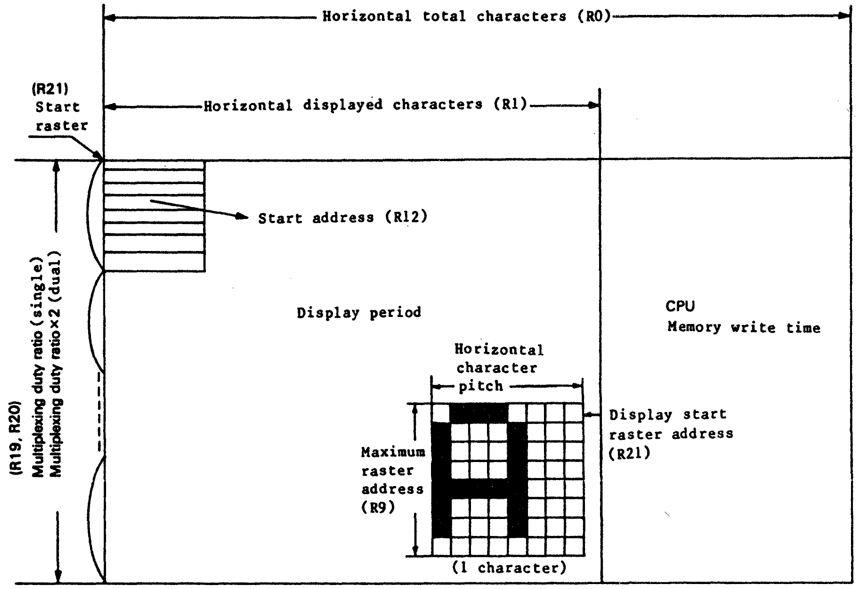


Figure 6-1 Relation between the Registers and the Display Screen

The relation between the values set in the internal register and the display screen size differs from mode to mode. See Table 6-1.

Table 6-1 Relation between the Values Set in the Internal Register and the Screen Size

No.	Modes No.	Character or Graphic	Screen Configuration	No. of Horizontal Dots of a Character	No. of Horizontal Dots of a Screen	No. of Vertical Dots of a Screen	Raster Time (μs)
1	1	Character (normal)	Dual	8	8 x Nhd	2 x Nd	$\frac{1}{f_{DCLK}} \times Nht \times 8$
2	5, 9	Character (normal)	Single	8	8 x Nhd	Nd	$\frac{1}{f_{DCLK}} \times Nht \times 16$
3	2	Character (wide)	Dual	16	16 x Nhd	2 x Nd	$\frac{1}{f_{DCLK}} \times Nht \times 16$
4	6, 10	Character (wide)	Single	16	16 x Nhd	Nd	$\frac{1}{f_{DCLK}} \times Nht \times 8$
5	3, 4, 13	Graphic	Dual	16	16 x Nhd	2 x Nd	$\frac{1}{f_{DCLK}} \times Nht \times 16$
6	7, 8, 11, 12	Graphic	Single	16	16 x Nhd	Nd	$\frac{1}{f_{DCLK}} \times Nht \times 8$

Note; Nht = horizontal total characters (R0)
Nhd = horizontal displayed characters (R1)
Nd = multiplexing duty ratio (R19, R20)
f_{DCLK} = DCLK frequency (MHz)

6.1.2 Timing charts

Figure 6-2(1)-Figure 6-2(10) show the timing charts of each mode when the values are set in the internal registers as follows;

Register No.	Register Name	Set Value
R0	Horizontal total characters	Nht
R1	Horizontal displayed characters	Nhd
R9	Maximum raster address	Nr
R10	Cursor start raster	Ncs
R11	Cursor end raster	Nce
R12	Start address (H)	-
R13	Start address (L)	-
R14	Cursor address (H)	-
R15	Cursor address (L)	-
R18	Horizontal virtual screen width	Nhd *
R19	Multiplexing duty ratio (H)	Ndh
R20	Multiplexing duty ratio (L)	Ndl
R21	Display start raster	Nsr
R22	Mode register	-

Note; The horizontal virtual screen width register does not function since Nhd is set in (R18).

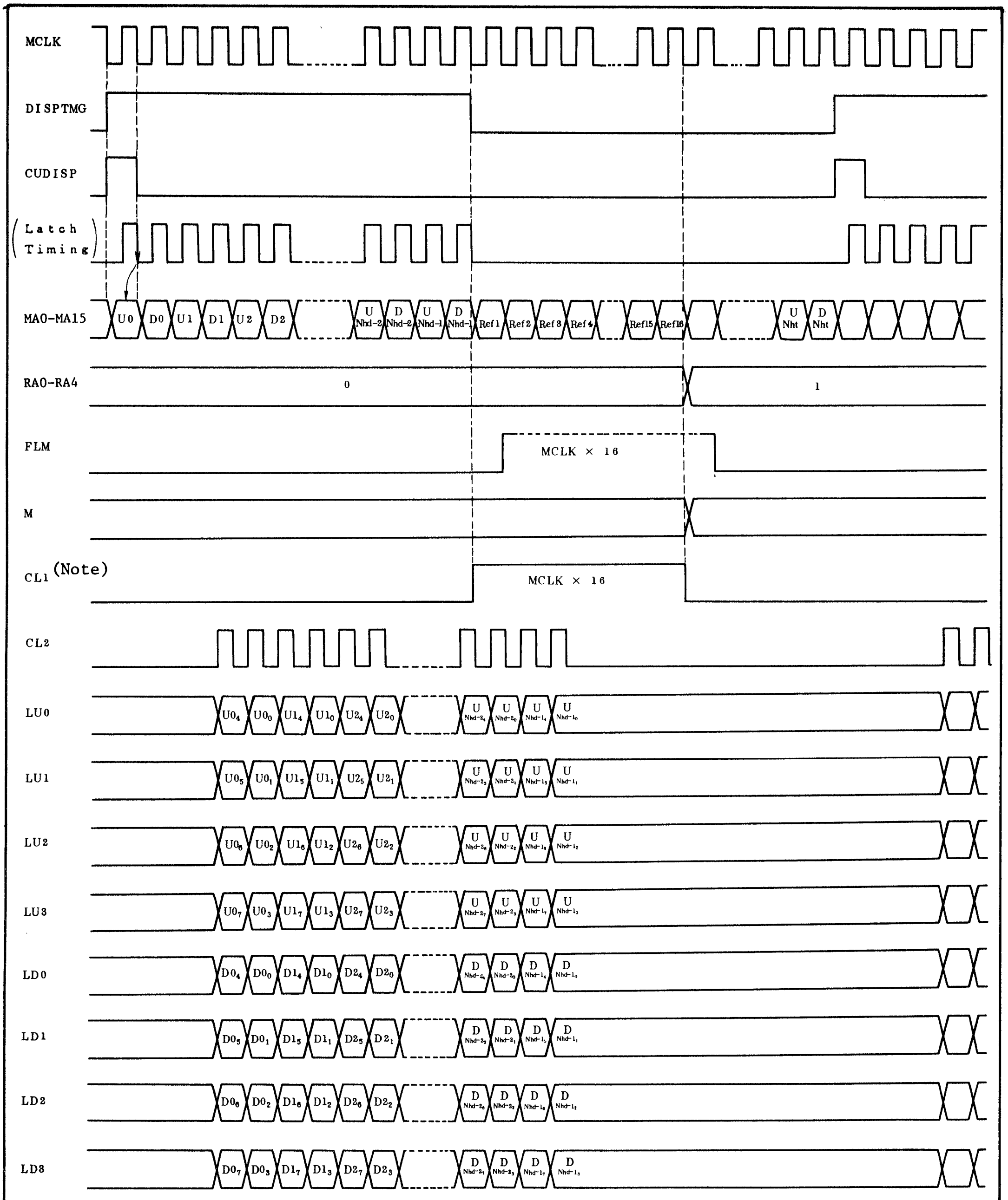
MCLK appears in a quarter period of the DCLK period in every mode, but the relation between MCLK, the MA frequency, and the CL2 frequency differs depending on the modes. Table 6-2 shows the relation. Refer to this table in choosing a memory IC and an LCD driver.

Table 6-2 Modes and the Frequency of MA and CL2

Mode No.	MA Frequency	CL2 Frequency
1, 2, 3, 4, 9	f_{MCLK}	f_{MCLK}
5, 13	f_{MCLK}	$2 \times f_{MCLK}$
6, 7, 8	$f_{MCLK}/2$	$2 \times f_{MCLK}$
10, 11, 12	$f_{MCLK}/2$	f_{MCLK}

See each timing chart about the phase relation.

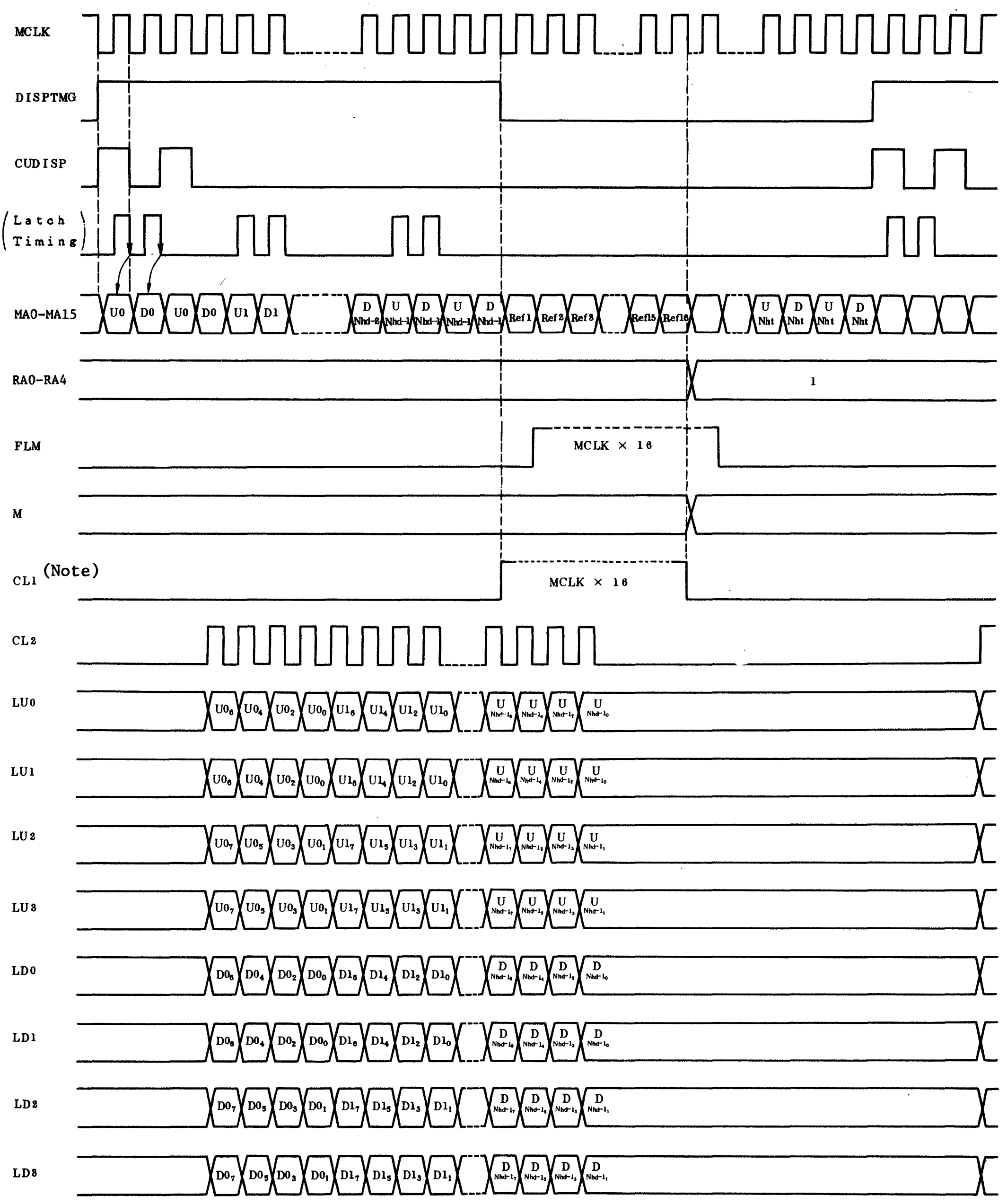
Figure 6-3 shows the timing charts of the period of a raster signal and a characrter row.



U = up panel address (data), D = down panel address (data), subscript = no. of MD pin, Nhd = horizontal displayed characters, Nht = horizontal total characters

Note: In the HD64646, the CL1 high period is 11 MCLK cycles. Therefore it doesnot overlap with CL2.
For further information, refer to the LCD interface (HD64646) in chapter 1, 1.4 Differences between HD64645 and HD64646 or chapter 14, Electrical Characteristics.

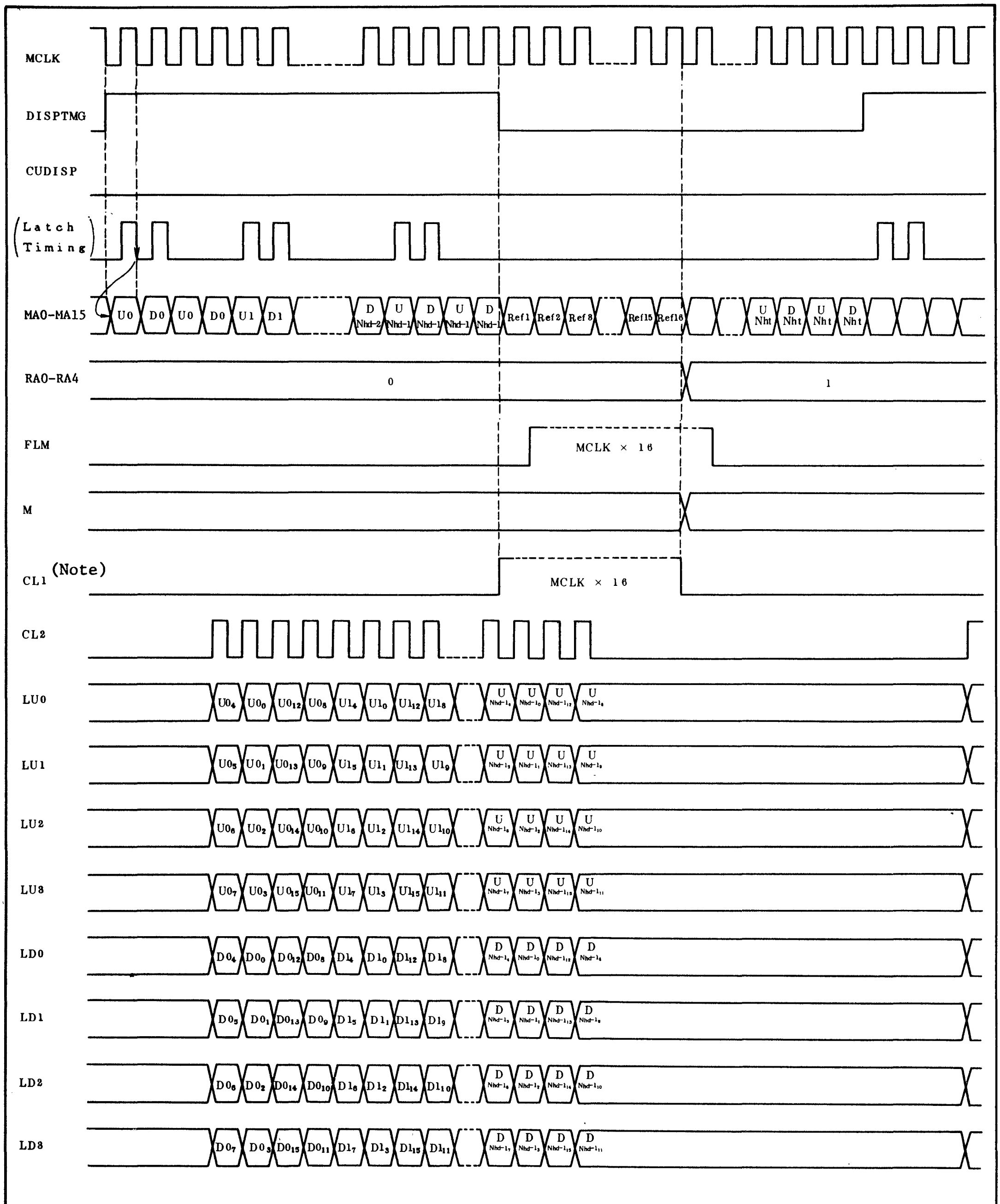
Figure 6-2 Timing Charts (1) Mode 1 (Dual screen normal character)



U = up panel address (data), D = down panel address (data), subscript = no. of MD pin,
Nhd = horizontal displayed characters, Nht = horizontal total characters

Note: In the HD64646, the CL1 high period is 11 MCLK cycles. Therefore it doesnot overlap with CL2.
For further information, refer to the LCD interface (HD64646) in chapter 1, 1.4 Differences between HD64645 and HD64646 or chapter 14, Electrical Characteristics.

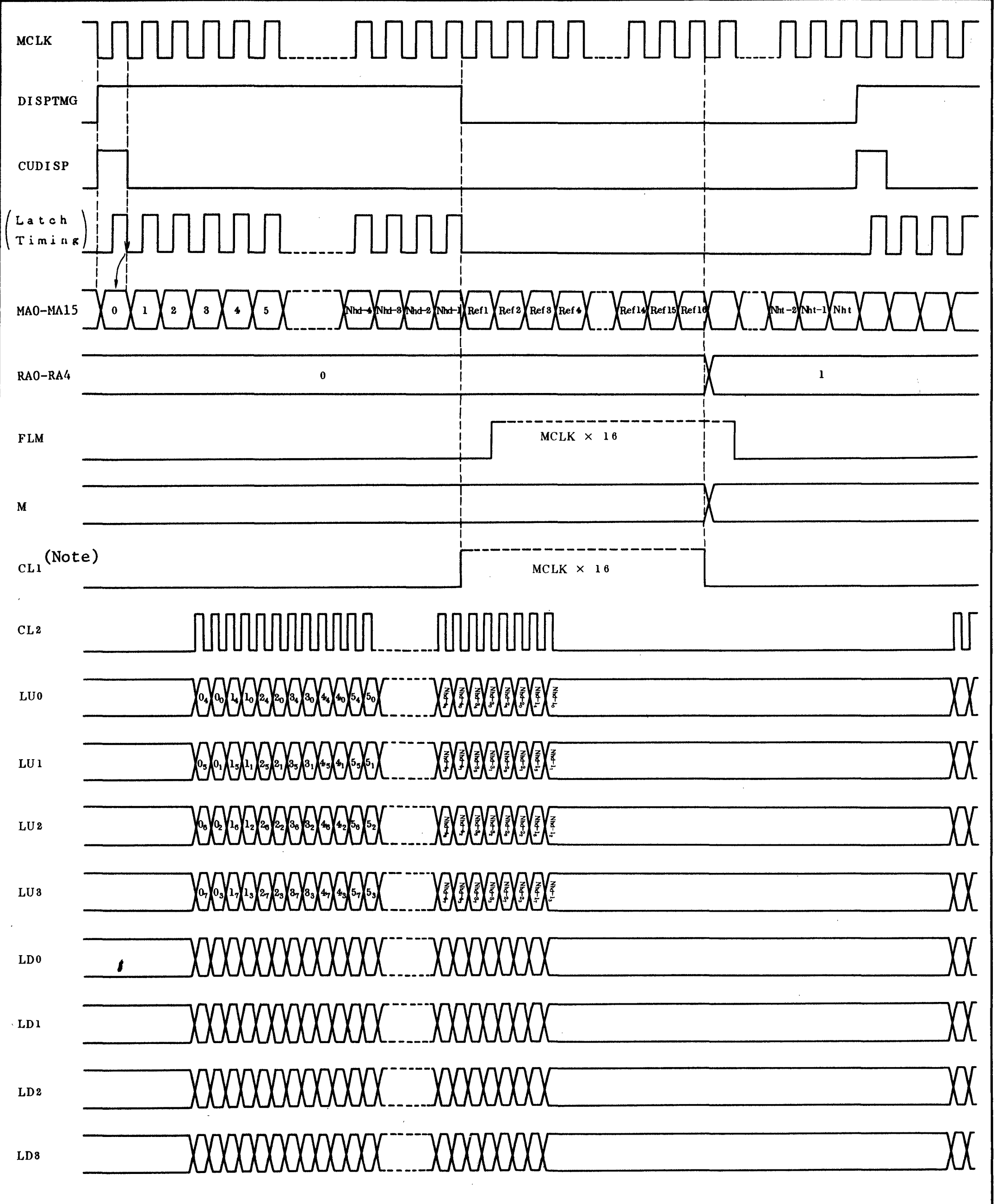
Figure 6-2 Timing Charts (2) Mode 2 (Dual screen wide character)



U = up panel address (data), D = down panel address (data), subscript = no. of MD pin, Nhd = horizontal displayed characters, Nht = horizontal total characters

Note: In the HD64646, the CL1 high period is 11 MCLK cycles. Therefore it doesnot overlap with CL2.
For further information, refer to the LCD interface (HD64646) in chapter 1, 1.4 Differences between HD64645 and HD64646 or chapter 14, Electrical Characteristics.

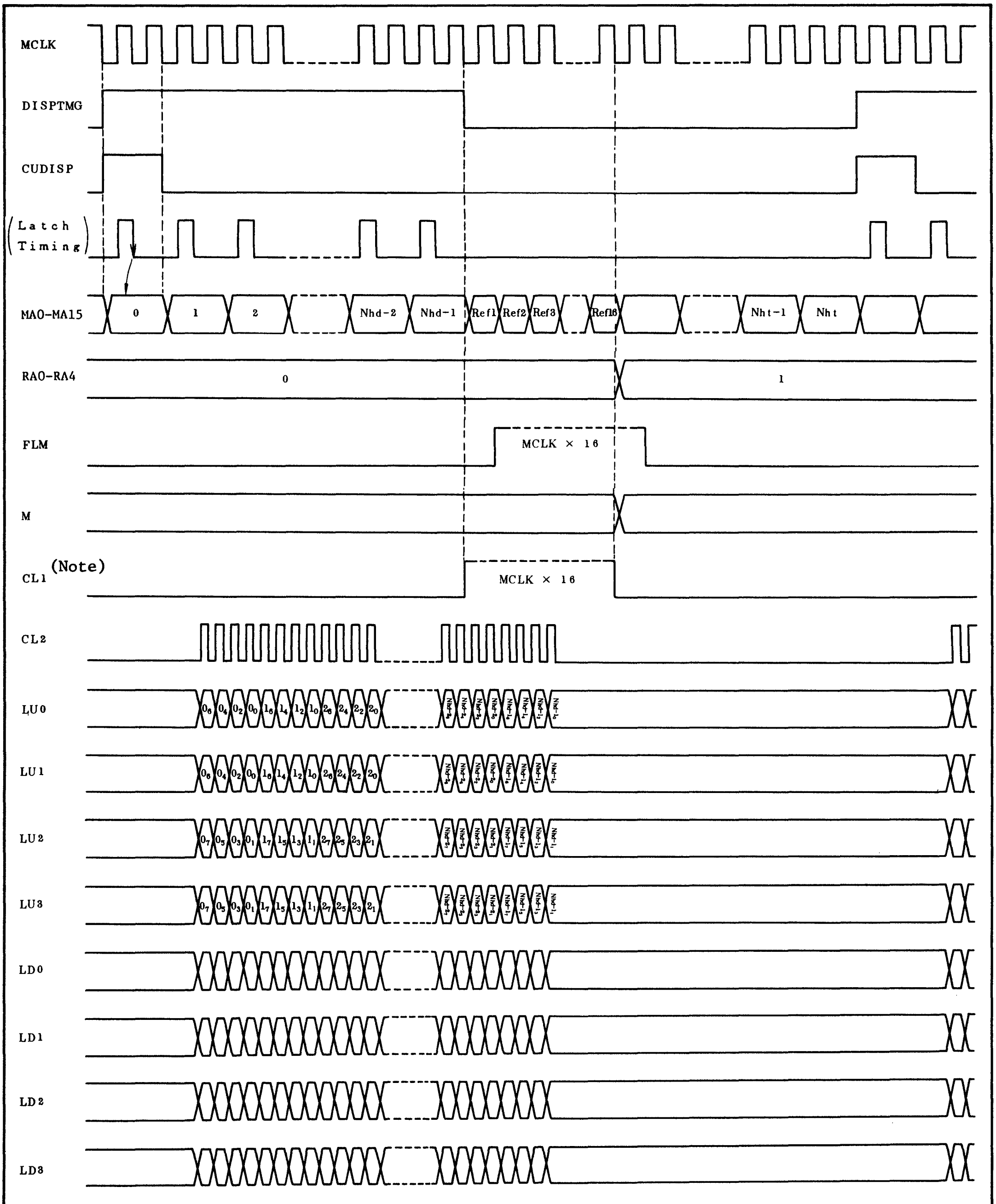
Figure 6-2 Timing Charts (3) Modes 3 and 4 (Dual screen graphic 1 and 2)



U = up panel address (data), D = down panel address (data), subscript = no. of MD pin,
Nhd = horizontal displayed characters, Nht = horizontal total characters

Note: In the HD64646, the CL1 high period is 11 MCLK cycles. Therefore it doesnot overlap with CL2.
For further information, refer to the LCD interface (HD64646) in chapter 1, 1.4 Differences between HD64645 and HD64646 or chapter 14, Electrical Characteristics.

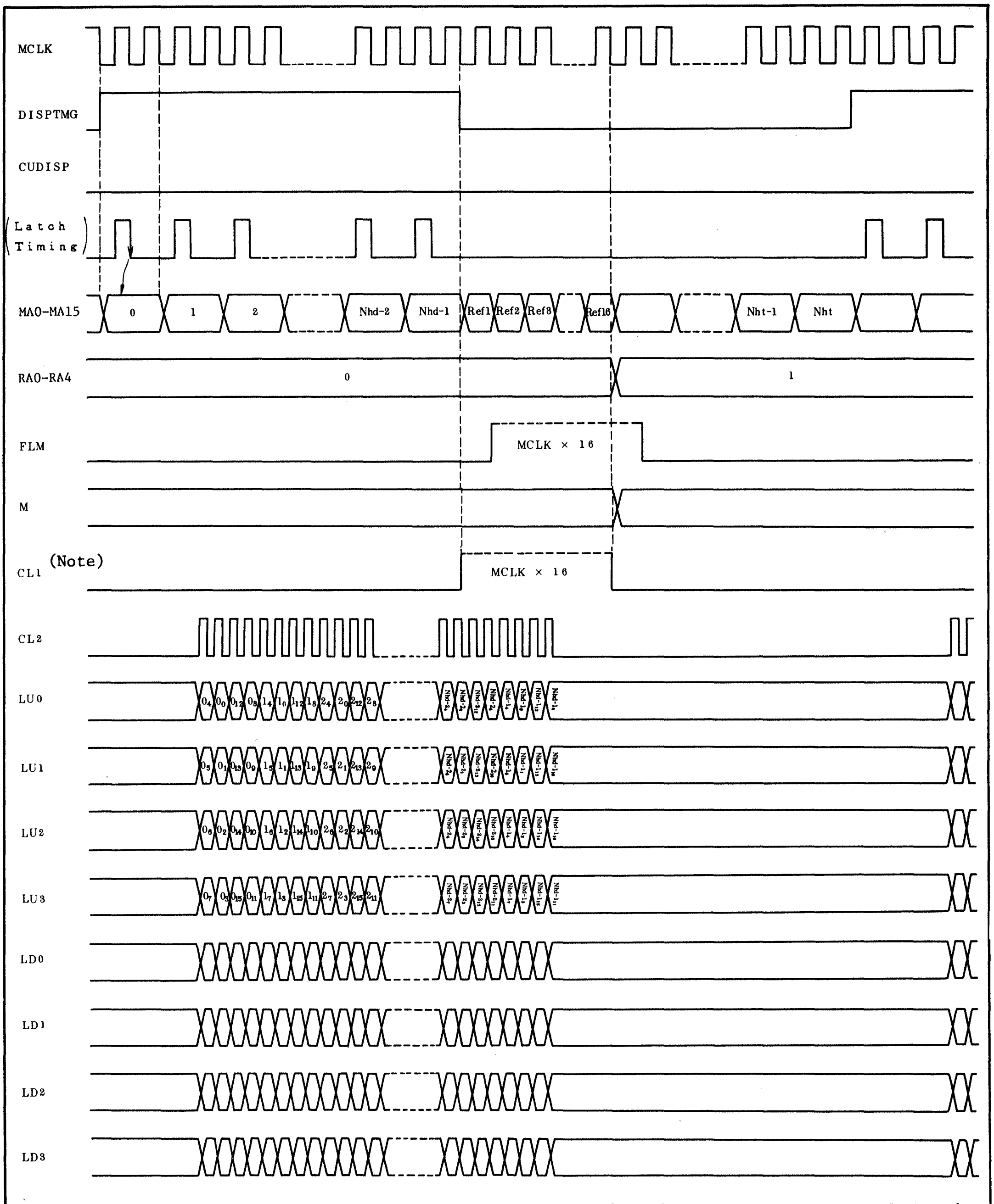
Figure 6-2 Timing Charts (4) Mode 5 (Single screen normal character)



U = up panel address (data), D = down panel address (data), subscript = no. of MD pin,
Nhd = horizontal displayed characters, Nht = horizontal total characters

Note: In the HD64646, the CL1 high period is 11 MCLK cycles. Therefore it doesnot overlap with CL2.
For further information, refer to the LCD interface (HD64646) in chapter 1, 1.4 Differences between HD64645 and HD64646 or chapter 14, Electrical Characteristics.

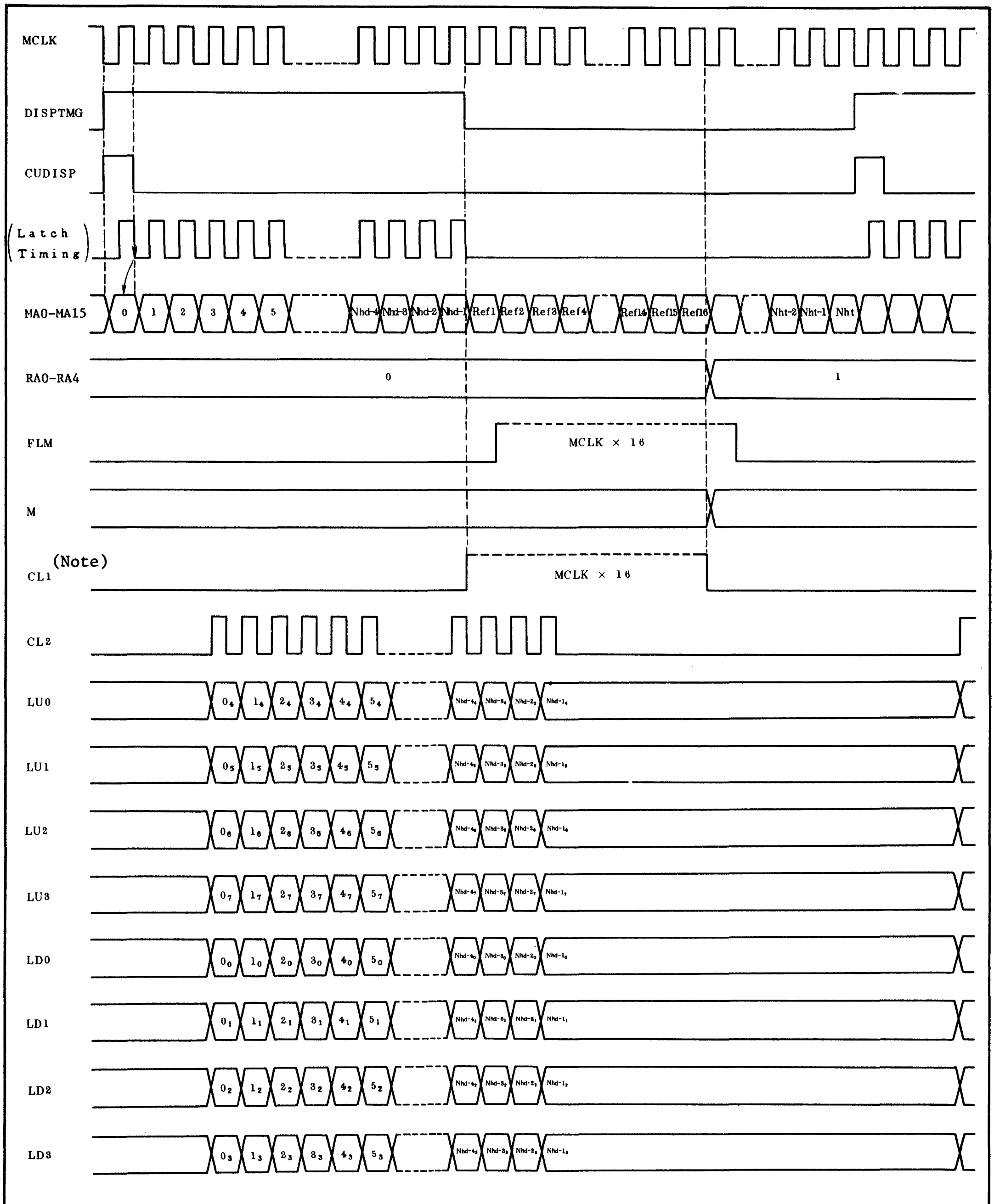
Figure 6-2 Timing Charts (5) Mode 6 (Single screen wide character)



U = up panel address (data), D = down panel address (data), subscript = no. of MD pin,
Nhd = horizontal displayed characters, Nht = horizontal total characters

Note: In the HD64646, the CL1 high period is 11 MCLK cycles. Therefore it doesnot overlap with CL2.
For further information, refer to the LCD interface (HD64646) in chapter 1, 1.4 Differences between HD64645 and HD64646 or chapter 14, Electrical Characteristics.

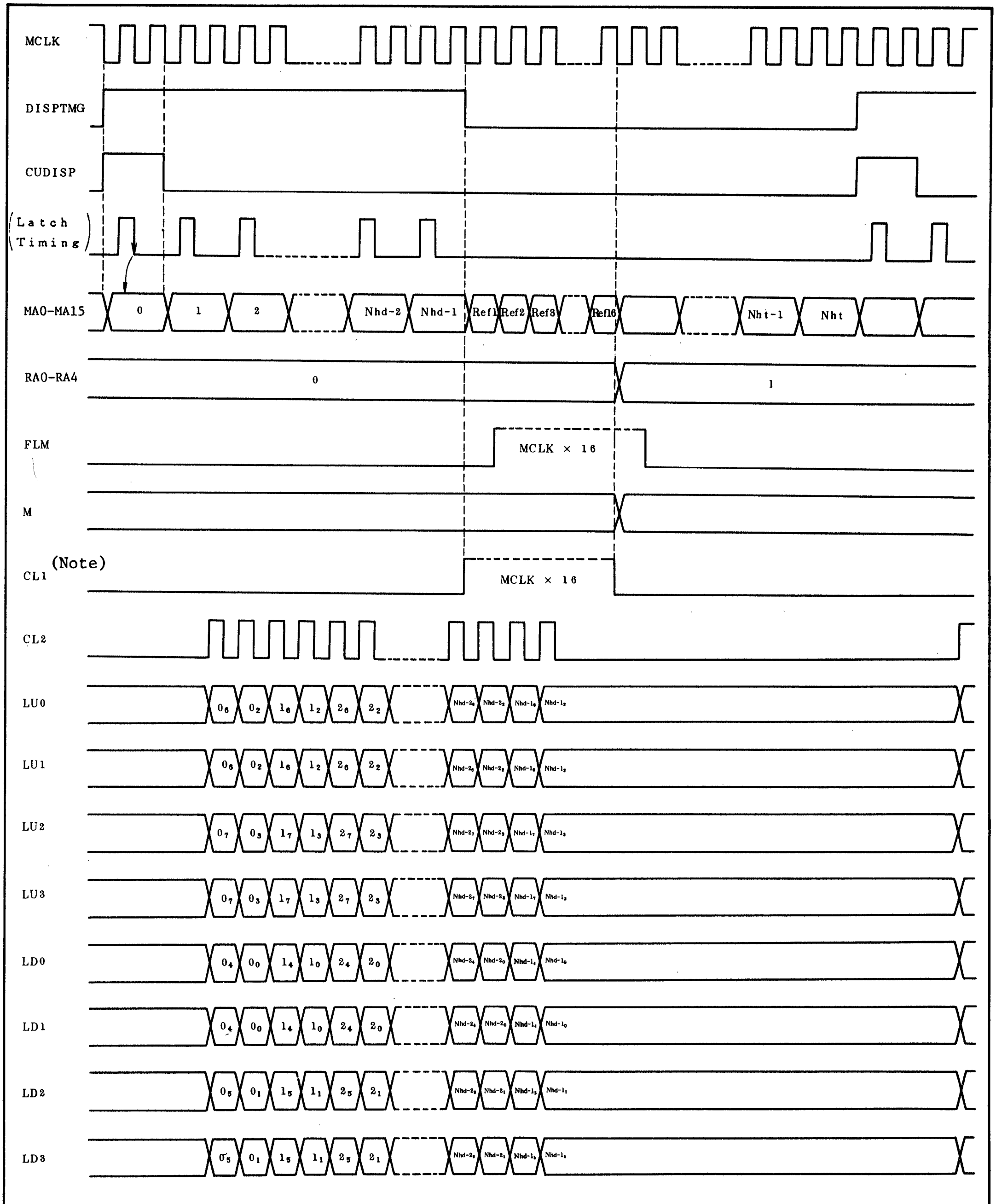
Figure 6-2 Timing Charts (6) Modes 7 and 8 (Single screen graphic 1 and 2)



U = up panel address (data), D = down panel address (data), subscript = no. of MD pin, Nhd = horizontal displayed characters, Nht = horizontal total characters

Note: In the HD64646, the CL1 high period is 11 MCLK cycles. Therefore it doesnot overlap with CL2.
For further information, refer to the LCD interface (HD64646) in chapter 1, 1.4 Differences between HD64645 and HD64646 or chapter 14, Electrical Characteristics.

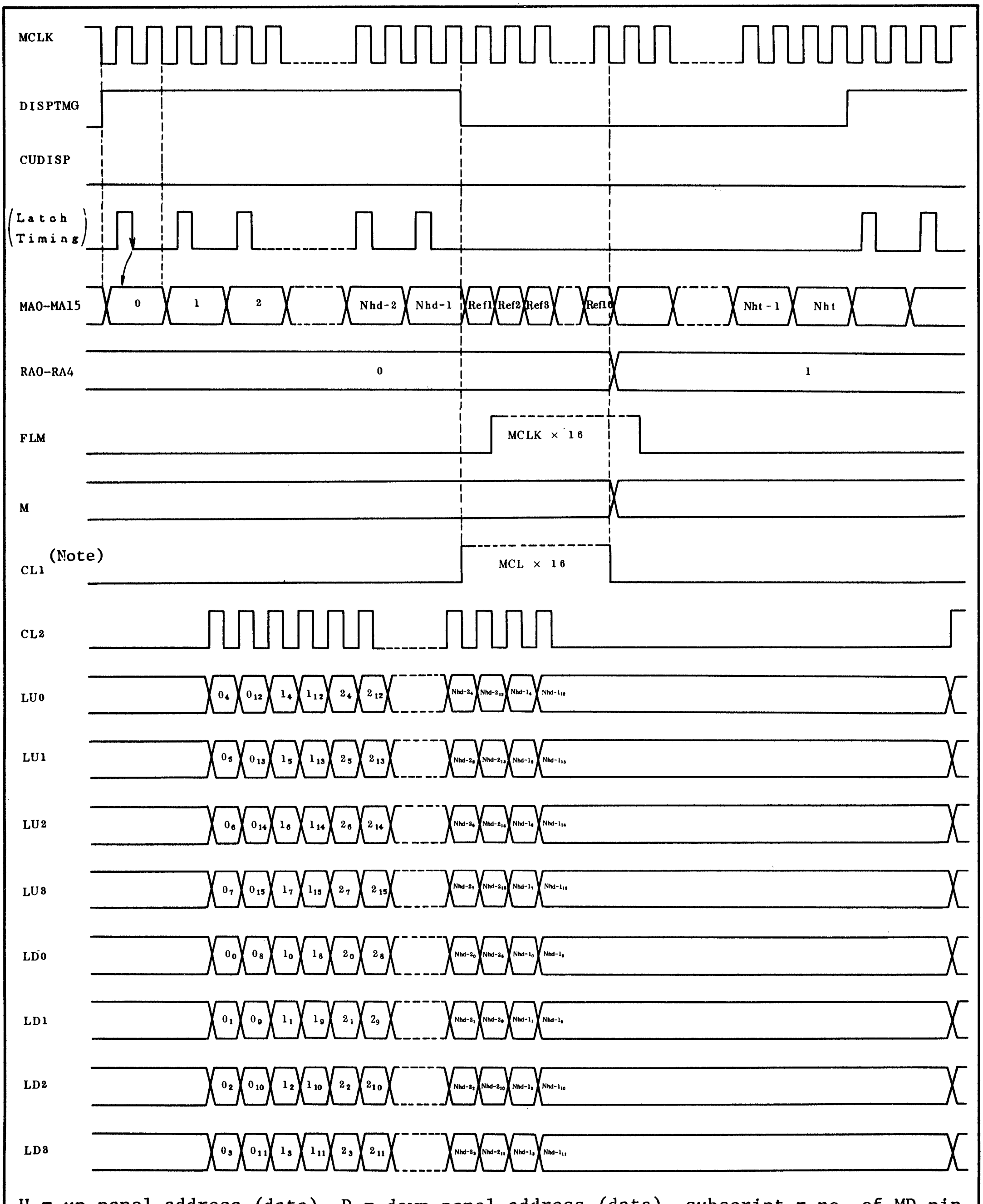
Figure 6-2 Timing Charts (7) Mode 9 (8-bit normal character)


MCLK
DISPTMG
CUDISP
Latch Timing
MA0-MA15
0
1
2
Nhd-2
Nhd-1
Ref1
Ref2
Ref3
Ref16
Nht-1
Nht
RA0-RA4
0
1
FLM
MCLK × 16
M
CL1 (Note)
MCLK × 16
CL2
LU0 0_6 0_2 1_6 1_2 2_6 2_2 Nhd-2_6 Nhd-2_2 Nhd-1_6 Nhd-1_2
LU1 0_6 0_2 1_6 1_2 2_6 2_2 Nhd-2_6 Nhd-2_2 Nhd-1_6 Nhd-1_2
LU2 0_7 0_3 1_7 1_3 2_7 2_3 Nhd-2_7 Nhd-2_3 Nhd-1_7 Nhd-1_3
LU3 0_7 0_3 1_7 1_3 2_7 2_3 Nhd-2_7 Nhd-2_3 Nhd-1_7 Nhd-1_3
LD0 0_4 0_0 1_4 1_0 2_4 2_0 Nhd-2_4 Nhd-2_0 Nhd-1_4 Nhd-1_0
LD1 0_4 0_0 1_4 1_0 2_4 2_0 Nhd-2_4 Nhd-2_0 Nhd-1_4 Nhd-1_0
LD2 0_5 0_1 1_5 1_1 2_5 2_1 Nhd-2_5 Nhd-2_1 Nhd-1_5 Nhd-1_1
LD3 0_5 0_1 1_5 1_1 2_5 2_1 Nhd-2_5 Nhd-2_1 Nhd-1_5 Nhd-1_1

U = up panel address (data), D = down panel address (data), subscript = no. of MD pin, Nhd = horizontal displayed characters, Nht = horizontal total characters

Note: In the HD64646, the CL1 high period is 11 MCLK cycles. Therefore it doesnot overlap with CL2.
For further information, refer to the LCD interface (HD64646) in chapter 1, 1.4 Differences between HD64645 and HD64646 or chapter 14, Electrical Characteristics.

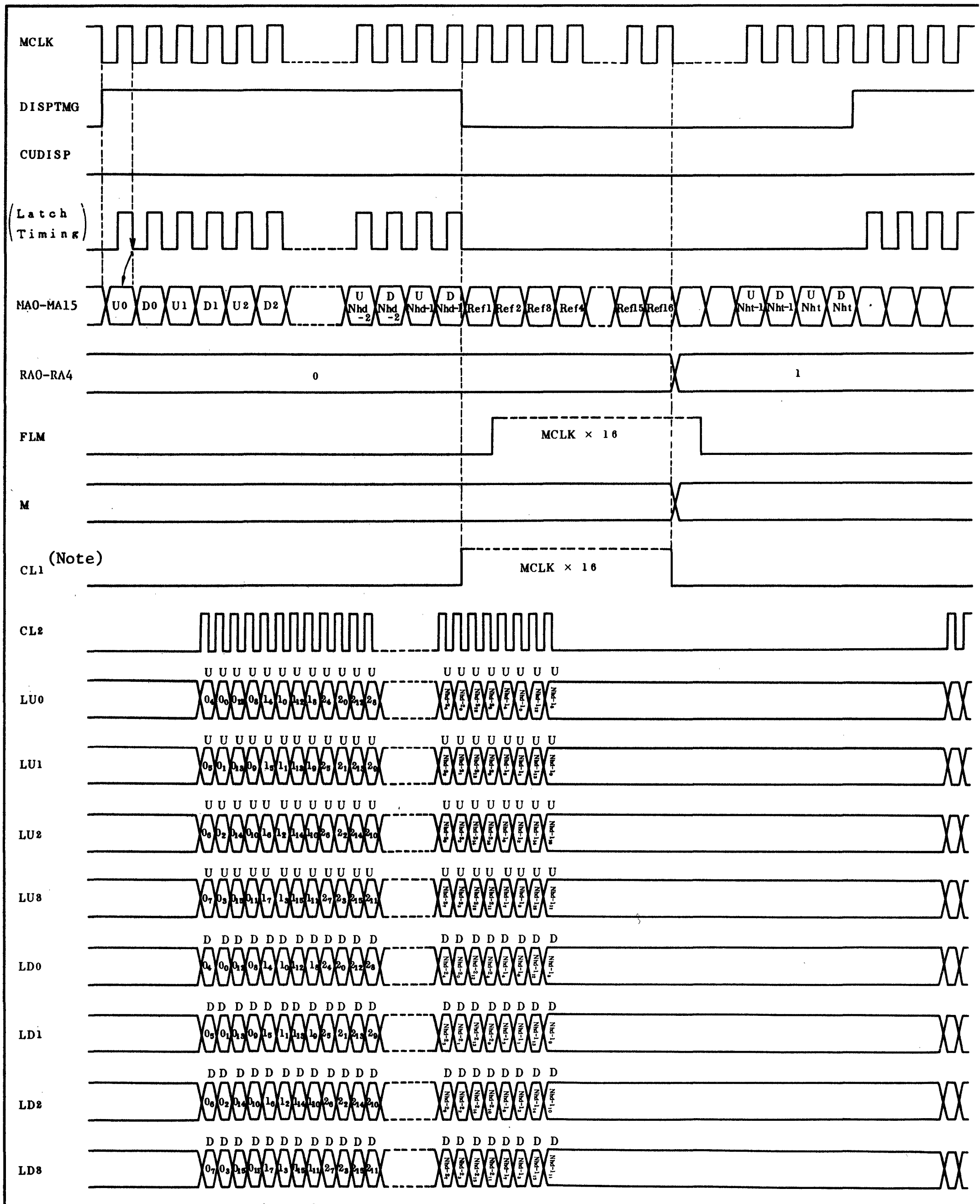
Figure 6-2 Timing Charts (8) Mode 10 (8-bit wide character)



U = up panel address (data), D = down panel address (data), subscript = no. of MD pin, Nhd = horizontal displayed characters, Nht = horizontal total characters

Note: In the HD64646, the CL1 high period is 11 MCLK cycles. Therefore it doesnot overlap with CL2.
For further information, refer to the LCD interface (HD64646) in chapter 1, 1.4 Differences between HD64645 and HD64646 or chapter 14, Electrical Characteristics.

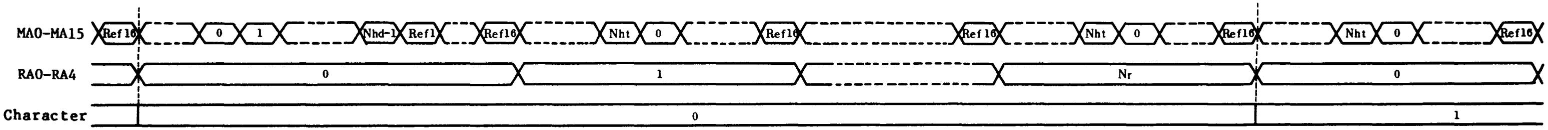
Figure 6-2 Timing Charts (9) Modes 11 and 12 (8-bit graphic 1 and 2)



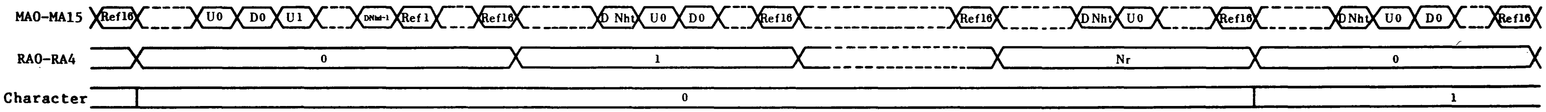
U = up panel address (data), D = down panel address (data), subscript = no. of MD pin,
Nhd = horizontal displayed characters, Nht = horizontal total characters

Note: In the HD64646, the CL1 high period is 11 MCLK cycles. Therefore it doesnot overlap with CL2.
For further information, refer to the LCD interface (HD64646) in chapter, 1, 1.4 Differences between HD64645 and HD64646 or chapter 14, Electrical Characteristics.

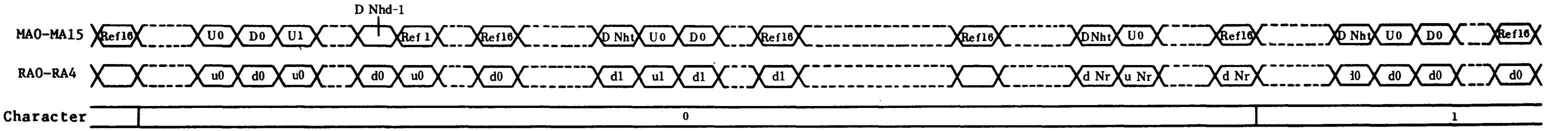
Figure 6-2 Timing Charts (10) Mode 13 (Large screen)



(1) Single screen



(2-1) Dual screen (A character row does not spread over the two panels.)



(2-2) Dual screen (A character row spreads over the two panels.)

U, u = up panel data

D, d = down panel data

Figure 6-3 Timing Charts of the Period of a Raster Signal and a Character Row

6.2 The Number of Displayed Characters and Memory Addresses

The memory addresses (MA_0-MA_{15}) of the LCTC are linear addresses beginning with the value of the start address. They increase linearly in the graphic mode and the MA pins output the same address as many times as the number of the rasters of a character row in the character mode. Thus they can be connected directly with the frame buffer in both modes.

The first address of the memory displayed on a screen can be altered freely by the start address registers (R12 and R13), and this facilitates paging and scrolling.

The LCTC can offset the memory addresses of the first characters on the adjacent character rows by the horizontal virtual screen width register (R18), and this facilitates horizontal scrolling.

It can also offset the raster addresses of the top character row of a screen by the start raster register (R21), and this facilitates vertical smooth scrolling.

Figure 6-4 shows the relation between the number of displayed characters and the memory addresses when the horizontal displayed characters (Nhd) is the same as the horizontal virtual screen width (Nir) and the start address is 0.

Although Figure 6-4 shows a case of the character mode, the address output will be the same as that of the graphic mode when Nr is set 0.

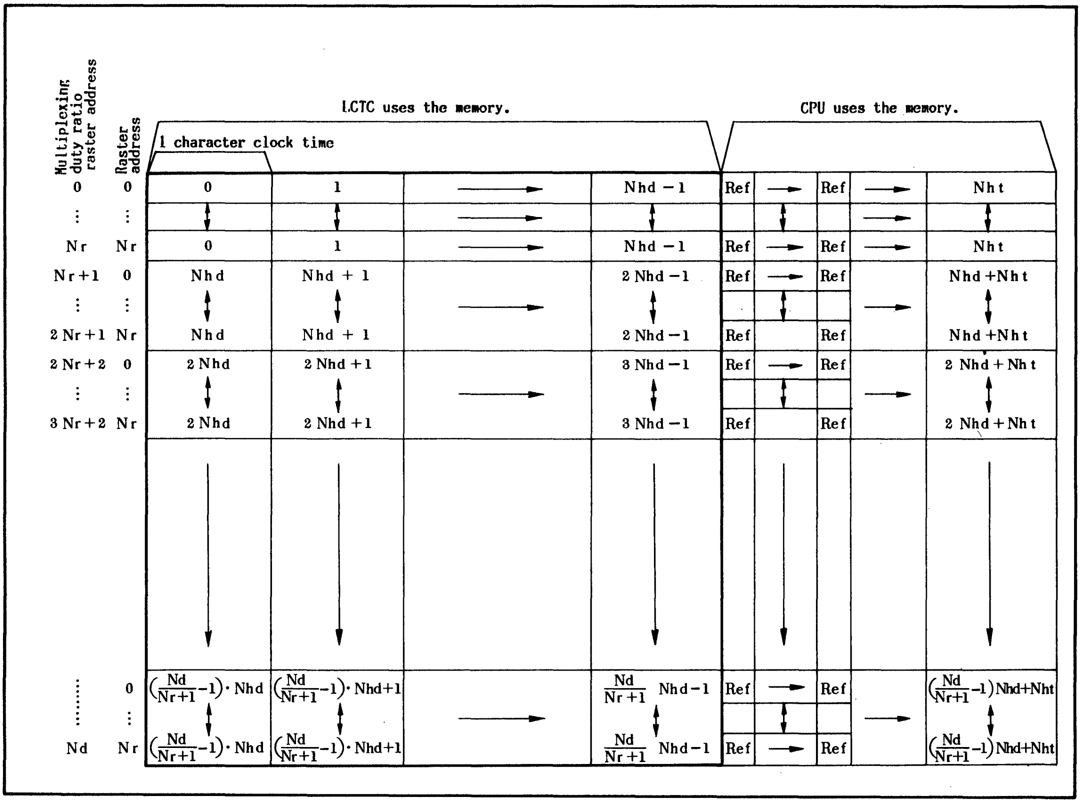


Figure 6-4 Relation between the Number of Displayed Characters and Memory Addresses when Nir = Nhd

Notes 1. ☐ indicates the display screen.

2. Ref; DRAM refresh address (See 6.5, "DRAM Refresh Address Output Function.")

3. Set values in the register corresponding to the screen in Figure 6-4

Register No.	Register Name	Set Value
R0	Horizontal total characters	Nht
R1	Horizontal displayed characters	Nhd
R9	Maximum raster address	Nr
R12, R13	Start address	0
R18	Horizontal virtual screen width	Nhd
R19, R20	Multiplexing duty ratio	Nd
R21	Display start raster	0

4. Figure 6-4 shows the screen in mode 5 (single screen, 4-bit data transfer, normal character mode).

When Nir > Nhd, an Nhd-wide "window" appears on an Nir-wide screen. Thus, although the display visible at a time is Nhd wide, one can see the whole part of an Nir-wide screen by sliding the window (= by renewing the display start address).

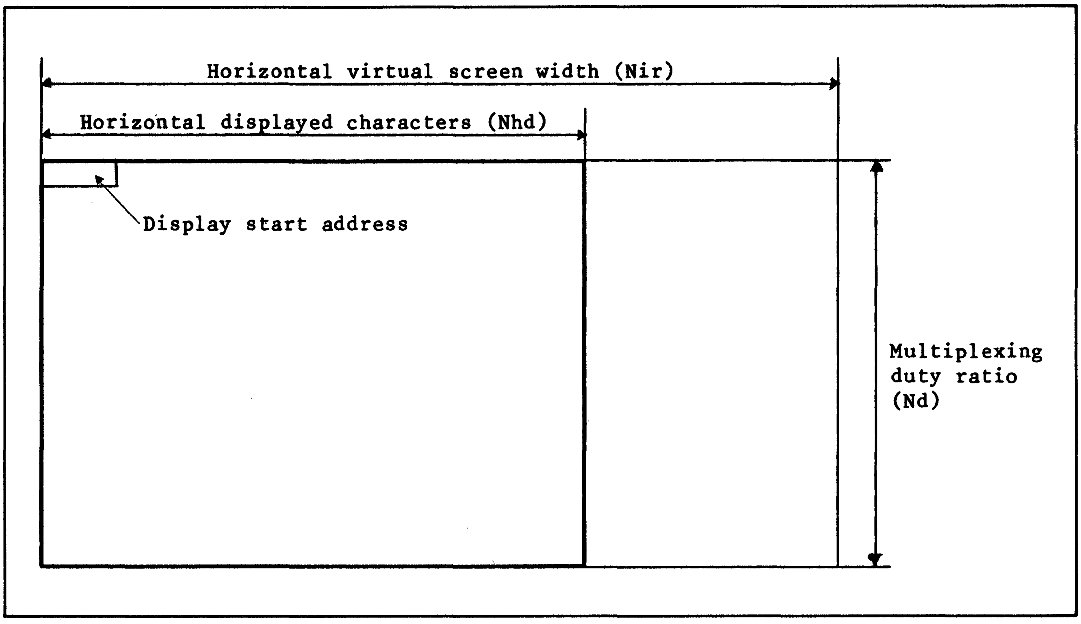

Horizontal virtual screen width (Nir)
Horizontal displayed characters (Nhd)
Display start address
Multiplexing duty ratio (Nd)

Figure 6-5 Horizontal Virtual Screen Width (= Nir)

Figure 6-6 shows the relation between the number of displayed characters and the memory addresses when Nir > Nhd. Nir defines the remainder of addresses at the end of each character row. This function facilitates horizontal scrolling. For more details, see Chapter 9, "PAGING AND SCROLLING."

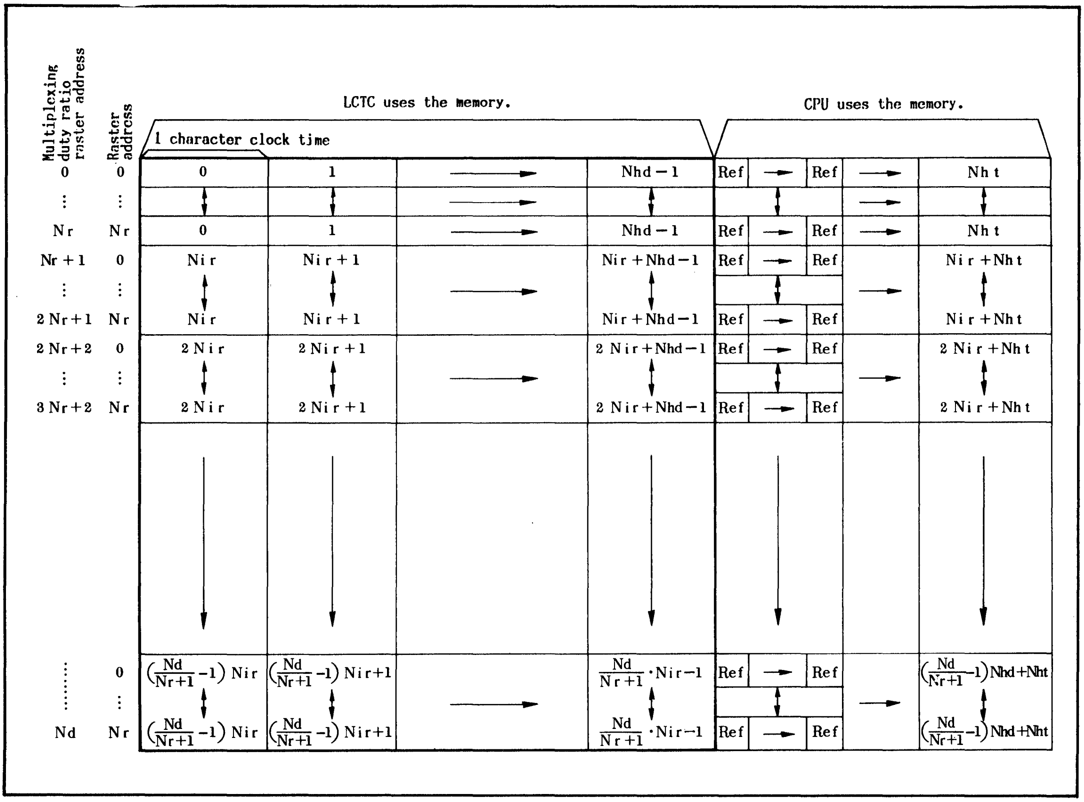


Figure 6-6 Relation between the Number of Displayed Characters and Memory Addresses when Nir > Nhd

Notes: 1. ☐ indicates the display screen.
2. Ref; DRAM refresh address (See 6.5, "DRAM Refresh Address Output Function.")
3. Set values in the register corresponding to the screen in Figure 6-6

Register No.	Register Name	Set Value
R0	Horizontal total characters	Nht
R1	Horizontal displayed characters	Nhd
R9	Maximum raster address	Nr
R12, R13	Start address	0
R18	Horizontal virtual screen width	Nir
R19, R20	Multiplexing duty ratio	Nd
R21	Display start raster	0

4. Figure 6-6 shows the screen in mode 5 (single screen, 4-bit data transfer, normal character mode).

Setting Nsr ≠ 0 (Nsr is the set value of the display start raster register (R21)) gives the offset to the first raster address of the first character row of a screen, and enables shifting the whole display vertically by the raster.

Figure 6-7 shows the relation between the number of displayed characters and the memory addresses when Nsr ≠ 0.

This function facilitates vertical smooth scrolling. For more details, see Chapter 9, "PAGING AND SCROLLING."

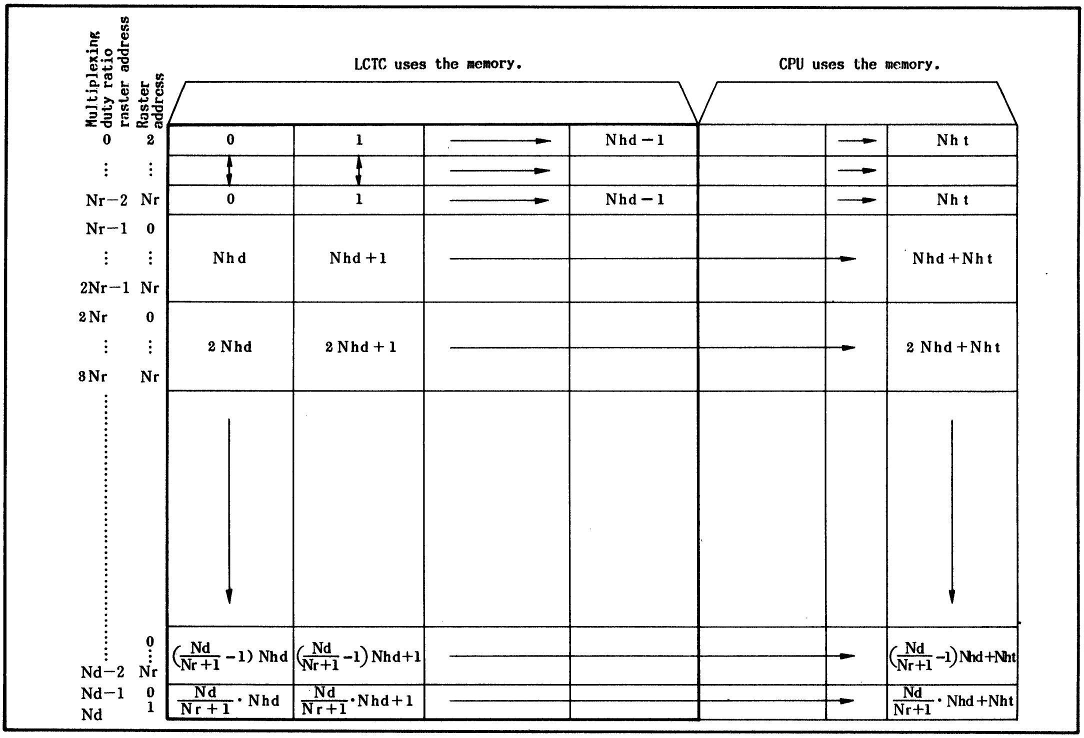


Figure 6-7 Relation between the Number of Displayed Characters and the Memory Addresses when Nsr = 2

Notes: 1. ▭ indicates the display screen.

2. Set values in the register corresponding to the screen in Figure 6-6

Register No.	Register Name	Set Value
R0	Horizontal total characters	Nht
R1	Horizontal displayed characters	Nhd
R9	Maximum raster address	Nr
R12, R13	Start address	0
R18	Horizontal virtual screen width	Nhd
R19, R20	Multiplexing duty ratio	Nd
R21	Display start raster	2

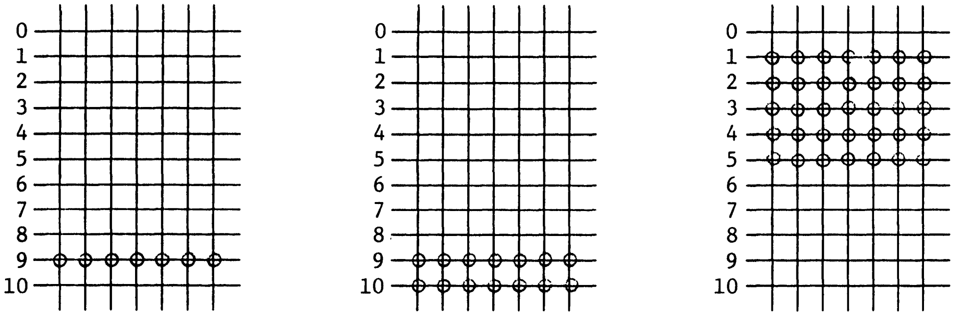
3. Figure 6-7 shows the screen in mode 5 (single screen, 4-bit data transfer, normal character mode).

6.3 Cursor Timing

Figure 6-8 shows the display patterns when values are set in the cursor start raster register and the cursor end raster register. The values to be set in these registers should satisfy the following conditions.

(Cursor start raster register) ≦ (cursor end raster register) ≦ (maximum raster address register)

Figure 6-9 shows the timing chart of the CUDISP signal.



Cursor start raster = 9
Cursor end raster = 9

Cursor start raster = 9
Cursor end raster = 10

Cursor start raster = 1
Cursor end raster = 5

Maximum raster address = 10

Figure 6-8 Cursor Control

The CUDISP output changes only in the character mode and it remains low in the graphic mode. Besides, the CUDISP output changes twice in mode 2 (dual screen, wide character mode) since the same address outputs twice. See Figure 6-2(2).

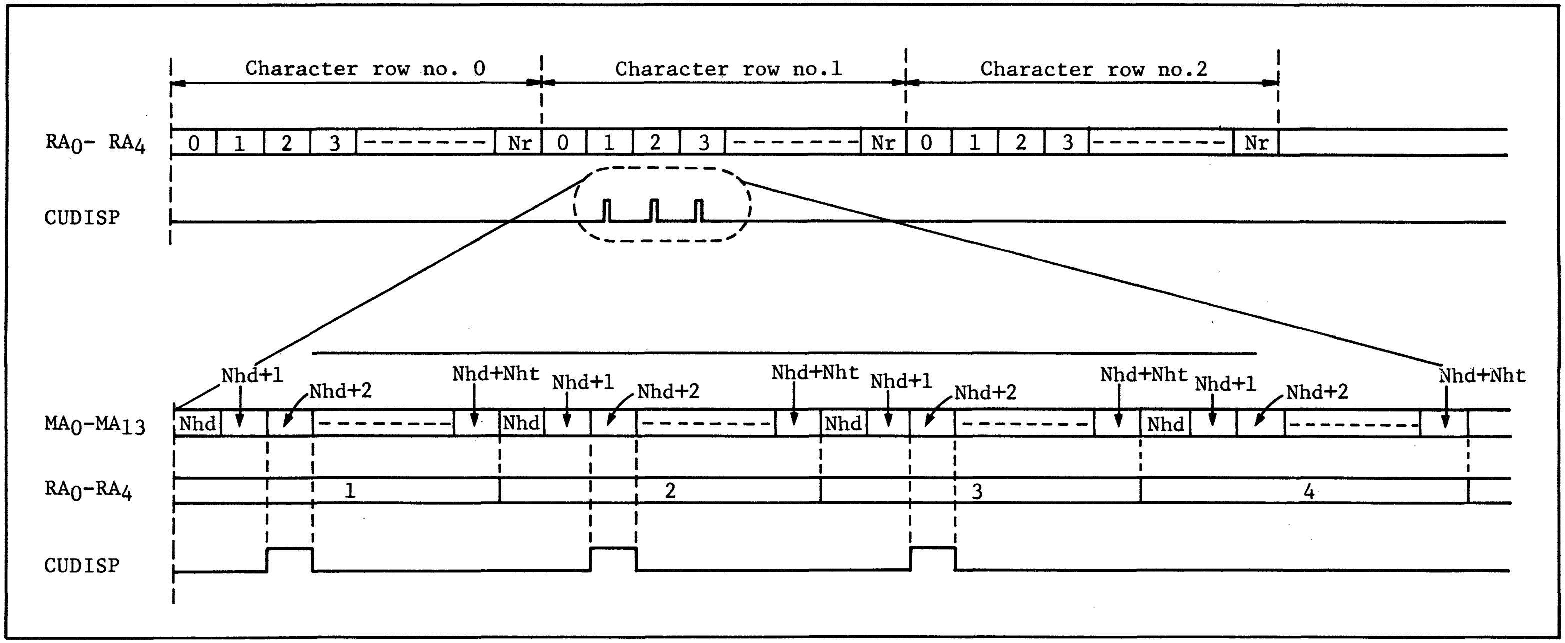
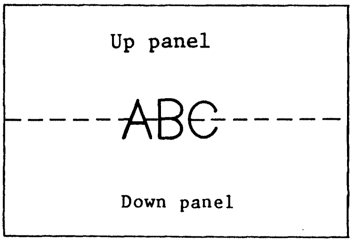


Figure 6-9 CUDISP Output Timing

Note; Cursor address register = Nhd + 2
Cursor start raster register = 1
Cursor end raster register = 3
Mode = cursor display mode
In the blink mode, a cursor goes on and off every 16th or 32nd field period.

6.4 Automatic Correction of Down Panel Raster Address

When the LCTC mode is set for character display and dual screen, memory addresses (MA) and raster addresses (RA) are output in such a way as to keep continuity of display spreading over the two panels. Therefore users can use the LCTC without considering the multiplexing duty ratio (the number of vertical dots of a screen) or the character font. (See Figure 6-10.)



Characters keep continuity in spite of the break of a screen.

Figure 6-10 Example of the Display in the Character Mode

The following explains how the LCTC performs the two cases; in one case (1) a character row does not spread over the up and down panels, and in the other case (2) it does.

(1) A character row does not spread over the up and down panels.

When the number of the vertical dots of a screen is a multiple of that of a character font, the border line of the two panels coincides with the break of characters as shown in Figure 6-11. For example, this is applicable to the case when a screen size is 640 (horizontal) x 400 (vertical) dots and a character font is 8 x 8 dots.

The further explanation will go along with the display example shown in Figure 6-11. In a dual screen, A of the up panel is transferred to the LCD driver simultaneously with L of the down panel, and B with M. However, the up panel data is latched from the memory before the down panel data. Thus the order of data latch here is A → L → B → M → ... as shown in Figure 6-12.

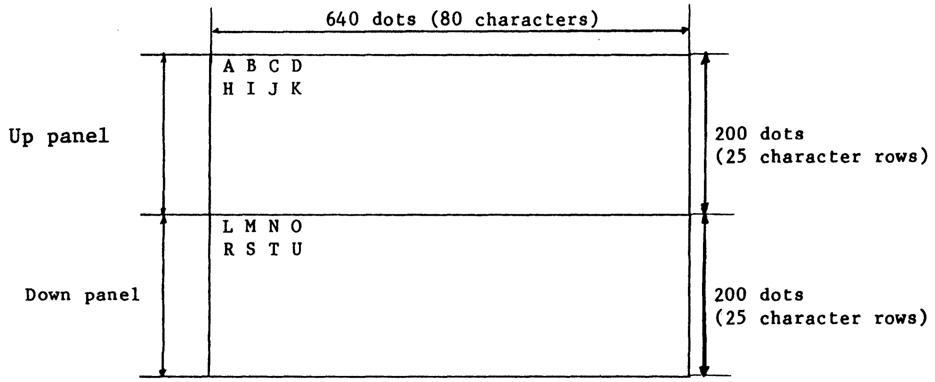


Figure 6-11 Example 1 of Dual Screen Display

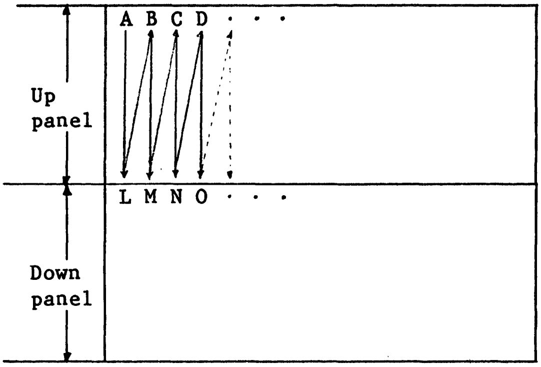


Figure 6-12 Memory Read Timing of Dual Screen Display

Therefore the relation between MA_0-MA_{15} and RA_0-RA_4 is to be as shown in Figure 6-13. However, the timing of RA_0-RA_4 is simplified to help an understanding of the figure. For more details, refer to Figure 6-3.

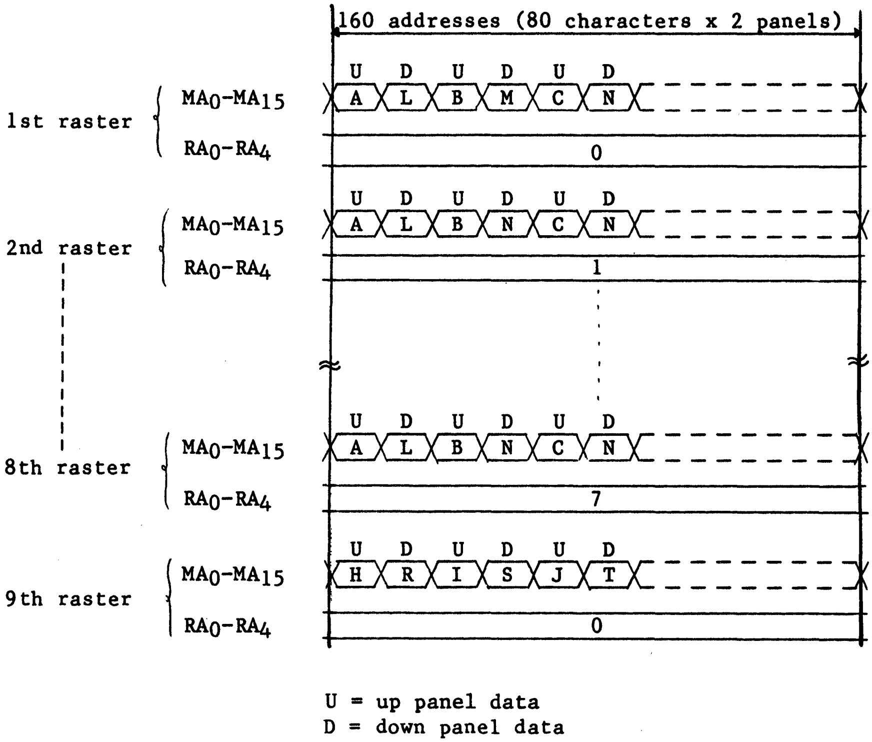


Figure 6-13 Relation between MA_0-MA_{15} and RA_0-RA_4 of the Example 1 of Dual Screen Display

(2) A character row spreads over the up and down panels.

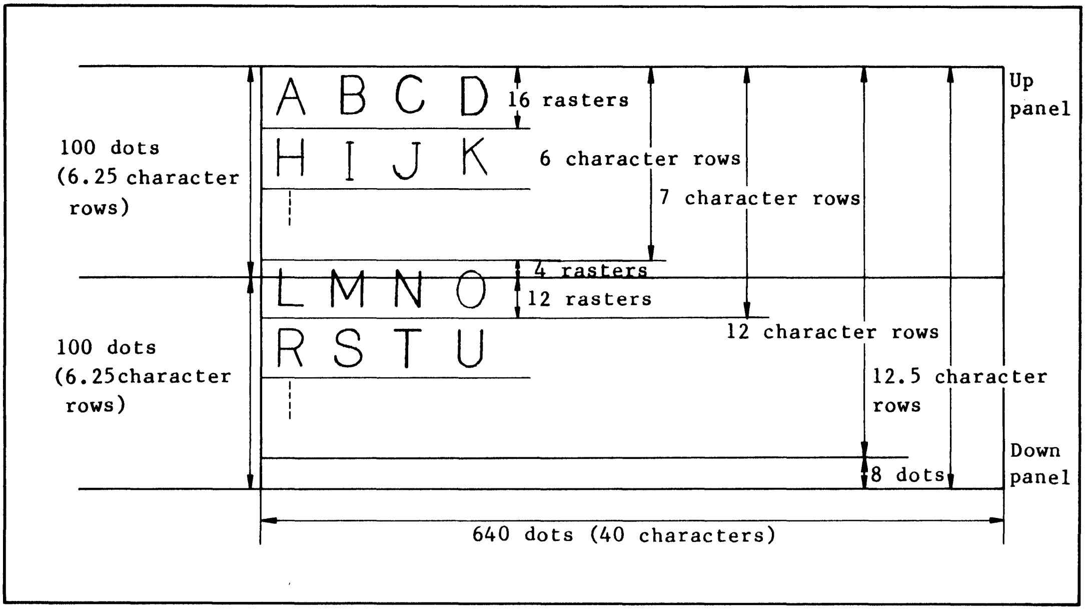


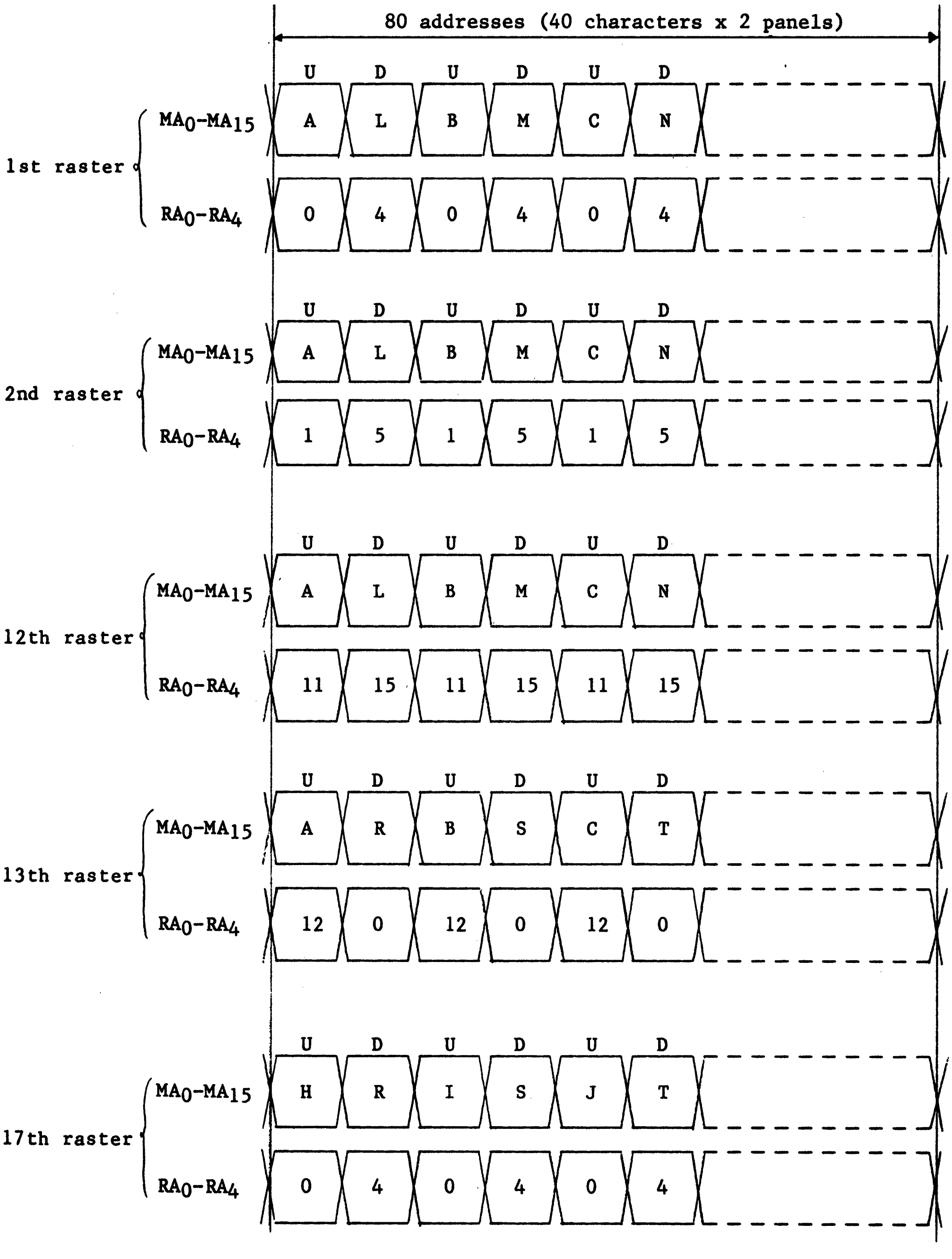
Figure 6-14 Example 2 of Dual Screen Display

As shown in Figure 6-14, when the number of the vertical dots of a screen is not a multiple of that of a character font, character row will be displayed over the two panels. For example, this is applicable to the case when a screen size is 640 (horizontal) x 200 (vertical) dots and a character font is 16 x 16 dots.

The LCTC enables continuous display since it can figure out the relationship between the number of the vertical dots of a screen (= multiplexing duty ratio) and those of the character font, and then outputs RA in a way which keeps continuity over the two panels.

However, when the screen is 200 dots long (up panel + down panel) and the character is 16 dots long, only the upper 8 dots are displayed concerning the characters on the 13th character row (= bottom row of the screen).

Figure 6-15 shows the relation between MA_0-MA_{15} and RA_0-RA_4.



U = up panel data
D = down panel data

Figure 6-15 Relation between MA_0-MA_{15} and RA_0-RA_4 of the Example 2 of Dual Screen Display

6.5 DRAM Refresh Address Output Function

6.5.1 Function

The LCTC outputs DRAM refresh addresses as shown in Figure 6-16.

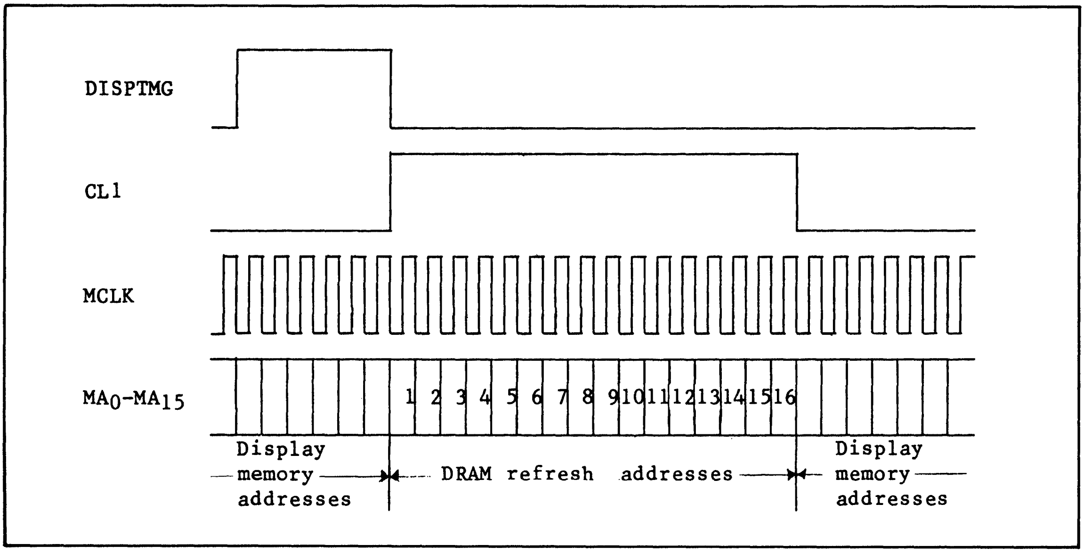


Figure 6-16 DRAM Refresh Address Output

The LCTC outputs 16 addresses for DRAM refresh every time a raster is scanned. This operation is repeated 16 times, and so it makes 256 addresses in total from \$00 to \$FF.

However, this output is not affected by the values of the horizontal total characters register (R0) or the horizontal displayed characters register (R1). (e.g. DISPTMG remains low for 16 MCLK cycles even when the horizontal total characters is the same as the horizontal displayed characters. Refer to 4.5, "Restrictions on Programming Internal Registers".)

When $\overline{\text{RES}}$ becomes low, all operations stop and the address is reset to \$00.

6.5.2 Restrictions on display screen

It restricts the screen size that the number of refresh address outputs per raster is fixed at 16.

Supposing the frame frequency is 70 Hz and the refreshing cycle of the DRAM in use is 256 cycles/4 m sec, the following relation holds true about the number of refresh cycles per second;

$$16 \times \text{multiplexing duty ratio} \times 70 > \frac{256}{0.004}$$

$$\text{Multiplexing duty ratio} > \frac{256}{16 \times 70 \times 0.004} = 57.1$$

Therefore DRAM cannot be used unless the multiplexing duty ratio of a screen is equal to, or more than 1/58 on these conditions.

6.5.3 Other Notes

It is necessary to generate the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ timing with external circuits in using this function.
In the case of HD64646, the CL1 high period does not correspond to the DRAM refresh address period. External circuits are necessary to generate the signal indicating the DRAM refresh address period.

Use the down edge of DISPTMG as the rising timing of the signal and the down edge of CL1 as the falling timing of the signal respectively.

7. INTERFACE AND PARAMETER SETTING

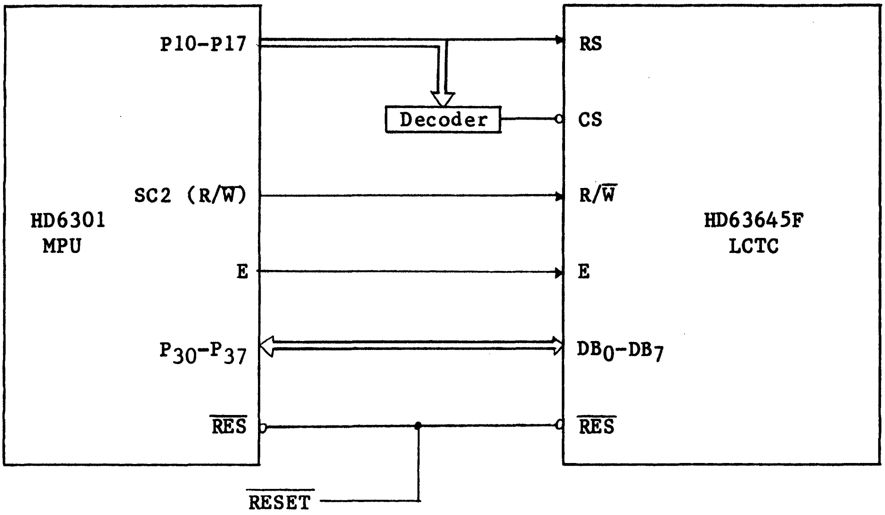
7.1 Interface to MPU

As shown in Figure 7-1, HD63645F (LCTC) and HD64645F (LCTC) are connected to the standard bus of 68 and 80 family MPU's respectively.

$\overline{\text{CS}}$ and RS signals sent from the MPU select the LCTC register. The MPU controlls the read and write of the data of HD63645F with R/$\overline{\text{W}}$ and E signals, while of HD64645F with $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals.

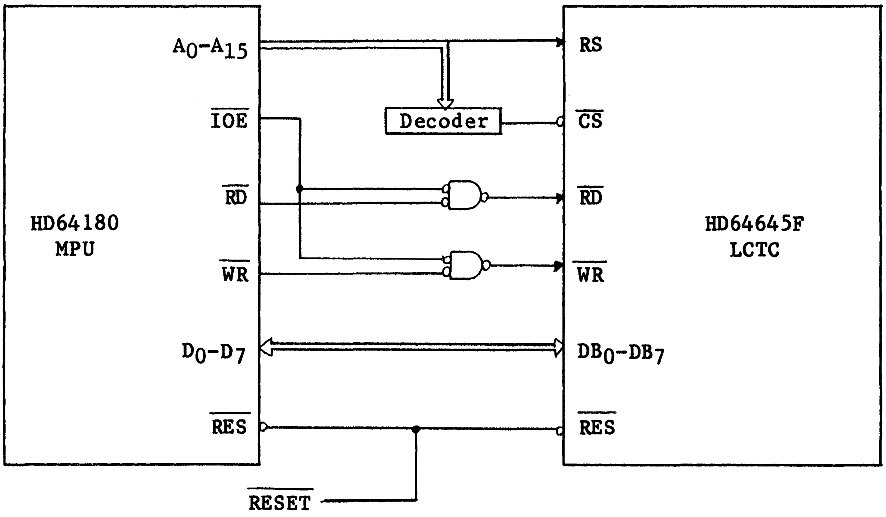
When $\overline{\text{CS}}$ and RS are low, the address register of the LCTC is selected, and when $\overline{\text{CS}}$ is low and RS is high, one of the internal data registers is selected.

$\overline{\text{RES}}$ signal resets the system. When $\overline{\text{RES}}$ is low, the internal logic circuit of the LCTC is reset. However, the internal registers R0-R22 shown in Table 4-2 are not affected by $\overline{\text{RES}}$, and retain their state prior to the reset.



Note; HD6301 is set in mode 5. P10-P17 are used as output ports, and P30-P37 as data buses. SC2 outputs R/$\overline{W}$ here.

(1) Interface between HD6301 and HD63645F



Note; Concerning 80 family MPU's, I/O space is separate from memory space in software. Thus the LCTC, a part of I/O, needs the ANDed signals of the interface signals and $\overline{IOE}$. So $\overline{IOE}$ and $\overline{RD}$, and $\overline{IOE}$ and $\overline{WR}$ should be ORed to satisfy t_{AS}, the timing of $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$.

(2) Interface between HD64180 and HD64645F

Figure 7-1 Interface to MPU

7.2 Interface to LCD System

7.2.1 Basic interface to LCD system

Figure 7-2 shows the basic interface between the LCTC and an LCD system. An LCD system can be constructed with a frame buffer, a character generator, and an LCD module.

The LCTC outputs up to 16 memory addresses (0-65535) to a frame buffer, and up to 5 raster addresses (0-31) to a character generator. The output from a character generator should be input to MD_0-MD_{15}.

The LCTC outputs FLM, M, CL2, CL1, LU_0-LU_3, and LD_0-LD_3 to an LCD module. FLM is a scan signal for a common driver, and M alternates the LCD drive signals. CL2 is a clock for shifting the data signals of a column driver, and CL1 is a clock for latching the data signals of a column driver. LU_0-LU_3, and LD_0-LD_3 are display data signals. Refer to <u>Hitachi MOS LSI Data Book LCD Driver</u> about the internal system of the LCD driver.

LCD system configuration differs from mode to mode. See chapter 5.

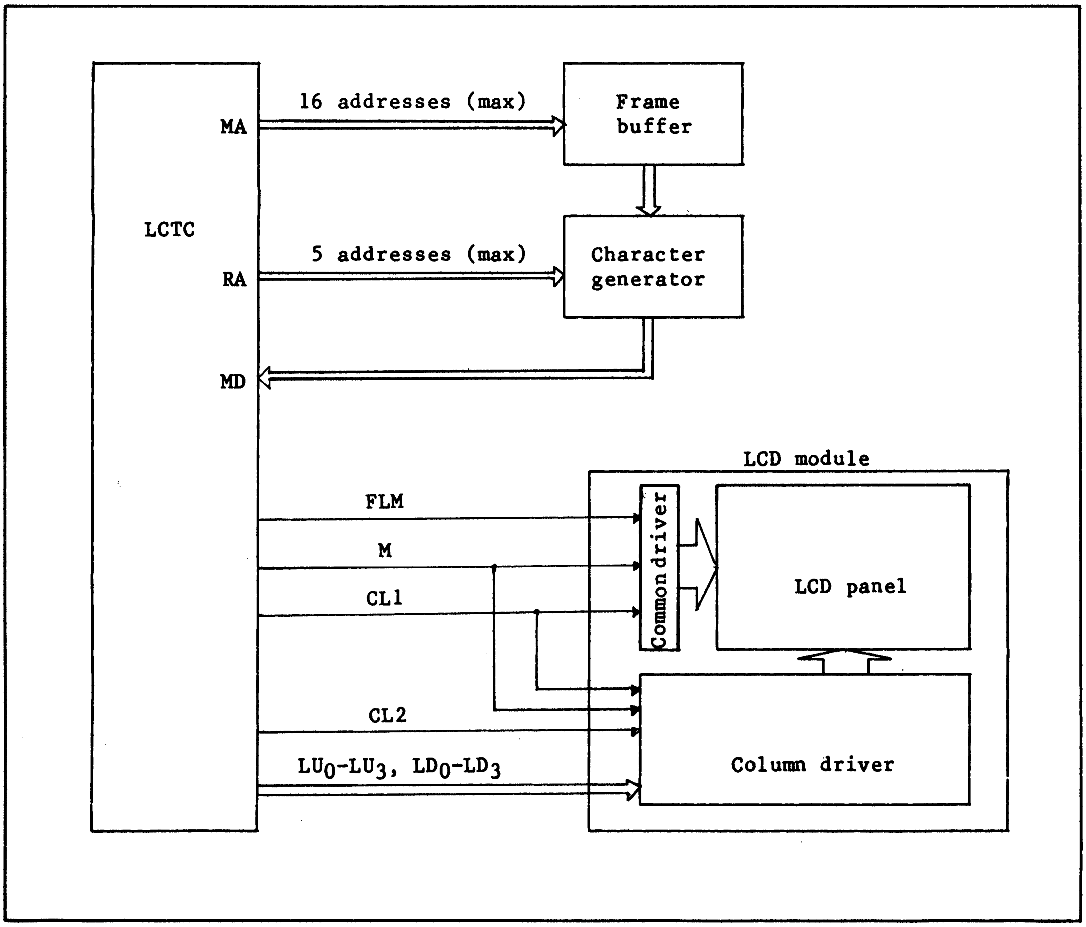


Figure 7-2 Interface to LCD System

7.2.2 Skew function

Figure 7-3 shows an example of the LCD system to access the frame buffer and the character generator simultaneously during a character clock time. Figure 7-6(i) shows its timing chart. This method is used when there are few horizontal displayed characters on a screen.

When there are many horizontal displayed characters and a character clock time is short, another method is used. In this method the outputs of the frame buffer are latched once, and the character generator is accessed at the next cycle instead that they are accessed simultaneously. Figure 7-4 shows the system configuration example, and Figure 7-6(ii) shows its timing chart. The LCTC outputs CUDISP, DISPTMG, and CL2 a character clock time behind according to the skew pins (SK0 and SK1), and latches the memory data also a character clock time behind.

In addition, when a high speed display operation is needed and when the MA delay time in a character clock time comes into question, the method shown in Figure 7-5 is used. In this method, the LCTC latches the MA outputs besides the outputs of the frame buffer. Figure 7-6(iii) shows its timing chart. Since both of the outputs of the MA and the frame buffer are latched, the character signal is delayed tow characters clock time. Therefore the LCTC again delays CUDISP, DISPTMG, CL2, and the latch timing of the memory data two characters clock time according to the skew pins, and adjusts the timing. Concerning DISPTMG, only its negative edge is delayed and positive edge remains unchanged.)

Table 7-1 shows the standards of choosing the display system configuration.

Table 7-1 Standards of Choosing the Display System Configuration

Case	Relation between t_{CH} and the Access Time of FB and CG	Block Diagram	Skew pin SK0	Skew pin SK1	Skew
1	t_{CH} > FB access time + CG access time + t_{MAD}	Figure 7-3	0	0	No skew
2	FB access time + CG access time + $t_{MAD} \geq t_{CH}$ > FB access time + t_{MAD}	Figure 7-4	0	1	1-character clock time skew
3	FB access time + $t_{MAD} \geq t_{CH}$ > FB access time	Figure 7-5	1	0	2-character clock time skew

FB; Frame buffer
CG; Character generator
t_{CH}; MA change time (character clock time)
t_{MAD}; MA delay time

Figure 7-6(i)-Figure 7-6(iii) show the examples of mode 5. Skewing is the same in all the modes.

When a character row spreads over the up and the down panels, the up panel raster address alternates with the down panel raster address synchronously with the change of the memory address because the LCTC automatically corrects the down panel raster address. Skewing does not affect raster addresses. Thus you need to synchronize the phases so as to do 1-character clock time skew by latching the raster address outputs (RA_0-RA_4). When a character row does not spread over the two panels, latching the RA outputs is not necessary because they remain unchanged for a raster time. Also, if 2-character clock time skew is used, latching is not necessary, even when a character row spreads over the two panels. The reason is as follows: RA_0-RA_4 pins output the up panel raster and the down panel raster alternately every MCLK cycle.

Therefore, if 2-character clock time skew is used, when the latch circuit applies the up panel character code, the LCTC also applies the up panel raster to it.

Similarly, when the latch circuit applies the down panel character code, the LCTC also applies the down panel raster.

Note (1) DISPTMG operation differs from that of HD6845S. For HD6845S, both the positive and negative edges of DISPTMG are delayed, while for the LCTC, only its negative edge is delayed and its positive edge remains unchanged.

(2) Skewing does not affect CL1, which generates the time when both of DISPTMG and CL1 are high during the skew. Figure 7-7 shows the relation.

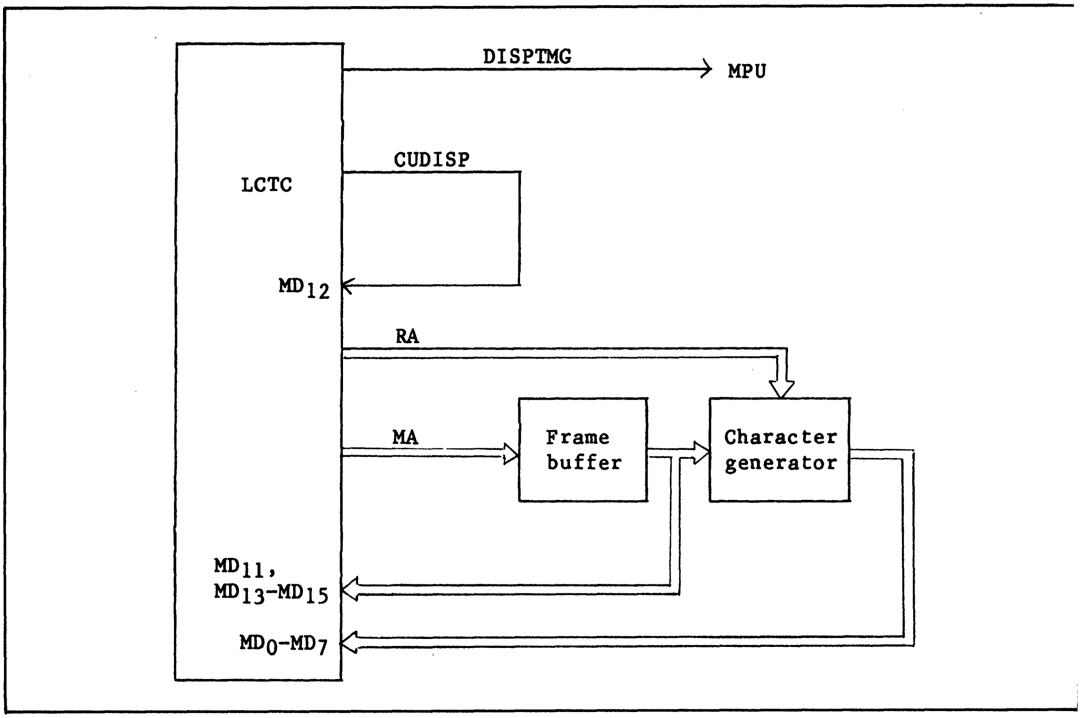


Figure 7-3 LCD System (1)

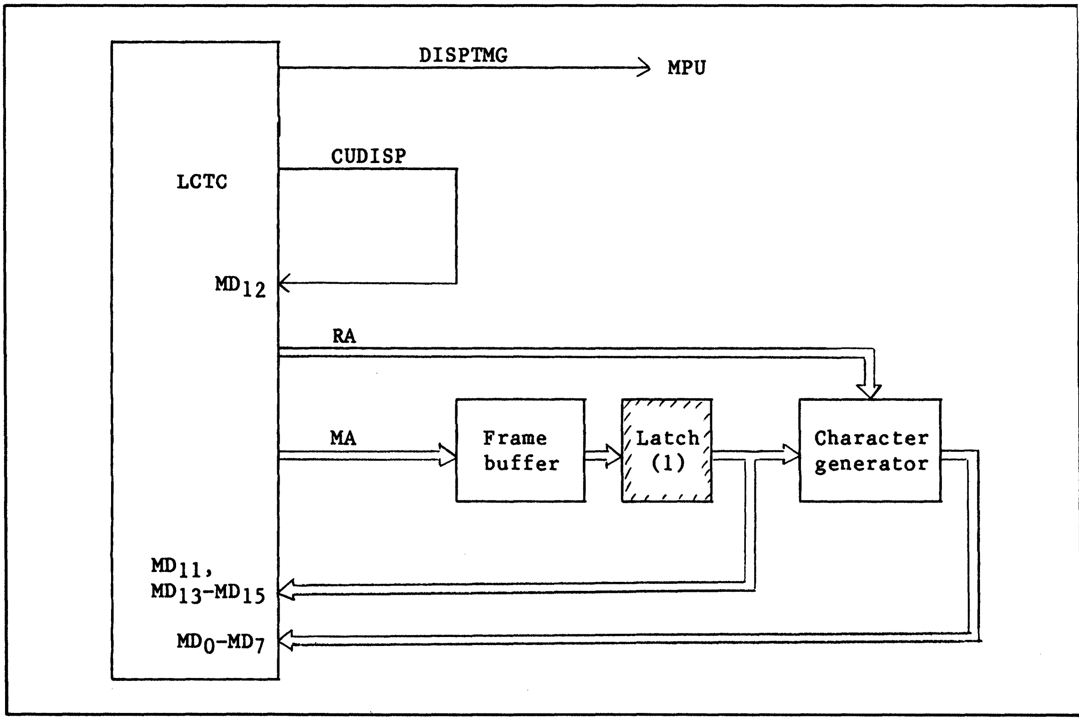


Figure 7-4 LCD System (2)

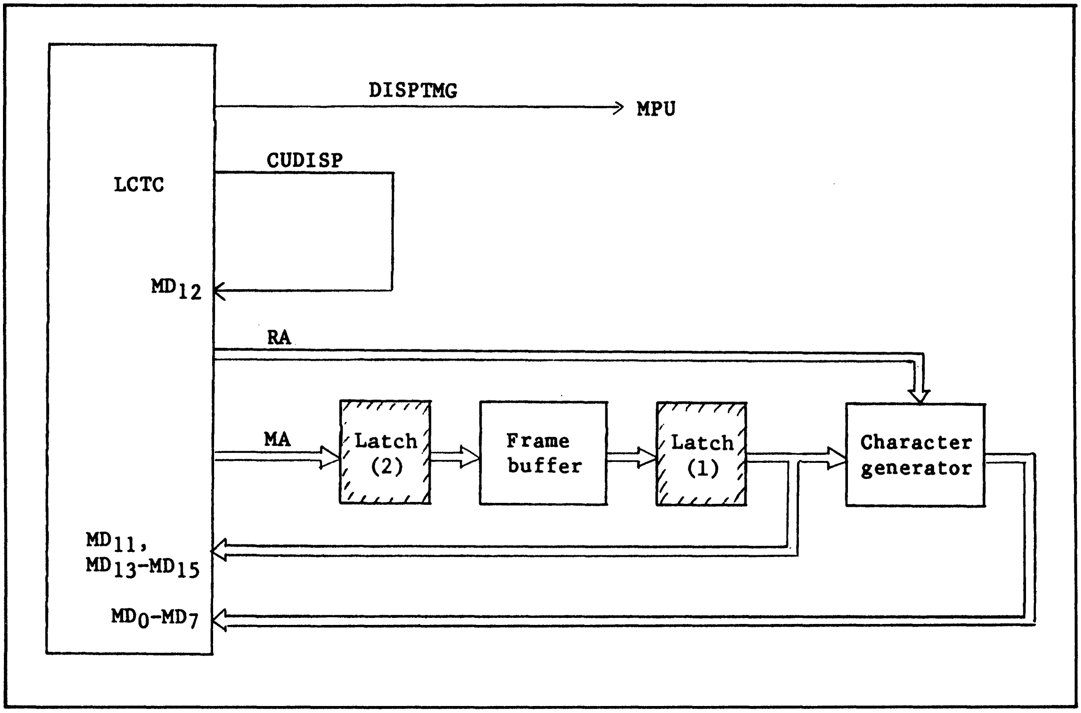
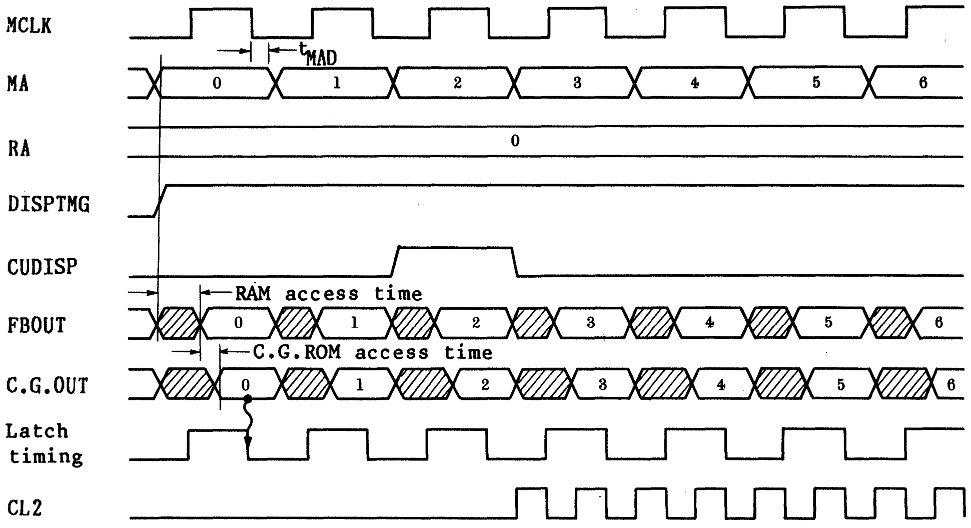
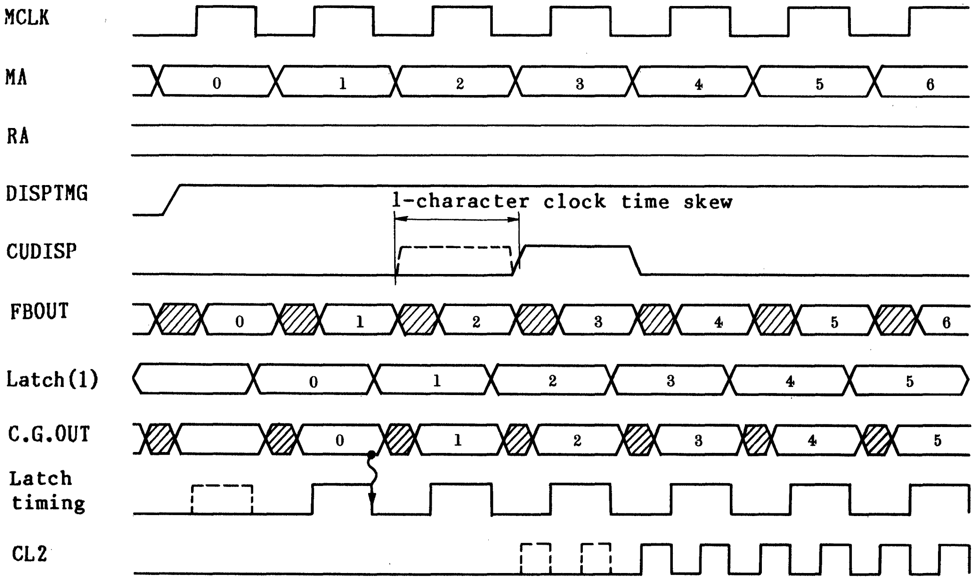


Figure 7-5 LCD System (3)

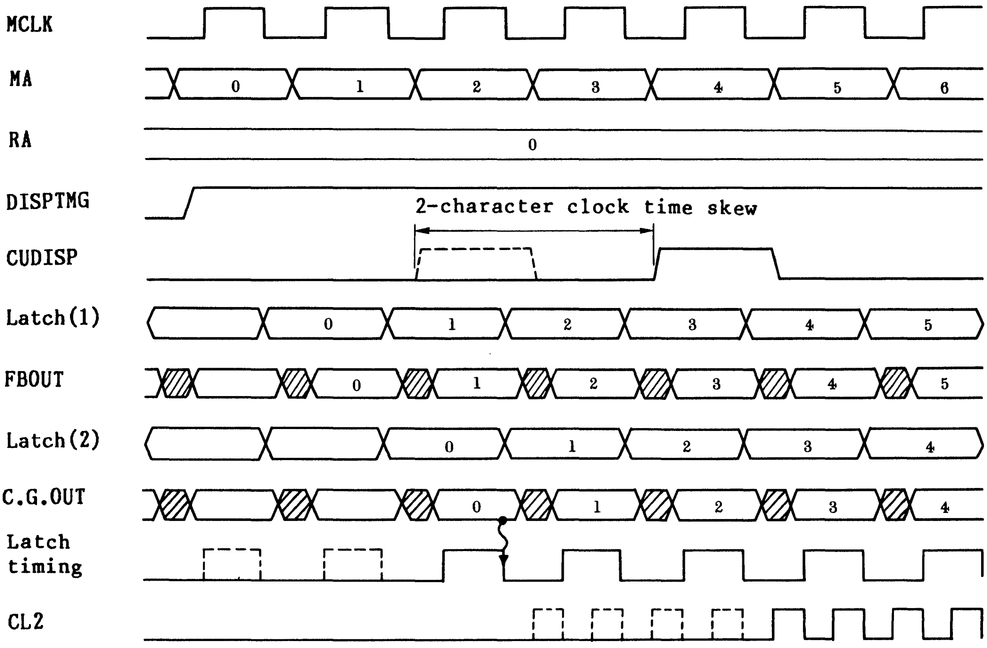


(i) Timing chart of LCD System (1)



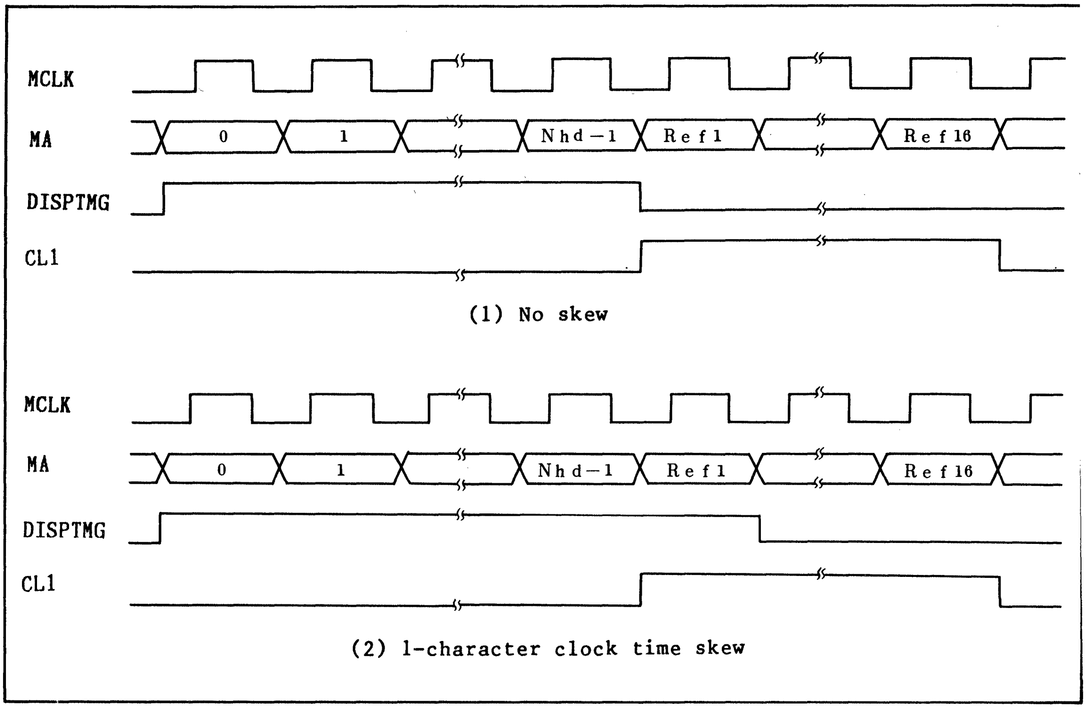
(ii) Timing chart of LCD System (2)

Figure 7-6 Skew Timing in Mode 5



(iii) Timing chart of LCD System (3)

Figure 7-6 Skew Timing in Mode 5



Note: In the HD64646, the CL1 high period is shorter than in the HD64645. Therefore it does not overlap with the DISPTMG high period. For further information, refer to "1.3 Differences between HD64645 and HD64646".

Figure 7-7 DISPTMG and CL1 in Skew Functioning

7.2.3 Relation between CL1 and CL2

CL1 and CL2 timings of the HD63465 and HD64645 are different from those of the HD64646. The CL1 high period of the HD64646 is 5 MCLK cycles shorter than that of the HD64645. The phase relations of DISPTMG, MCLK, CL1 and CL2 in the HD63645, HD64645 and HD64646 are shown below.

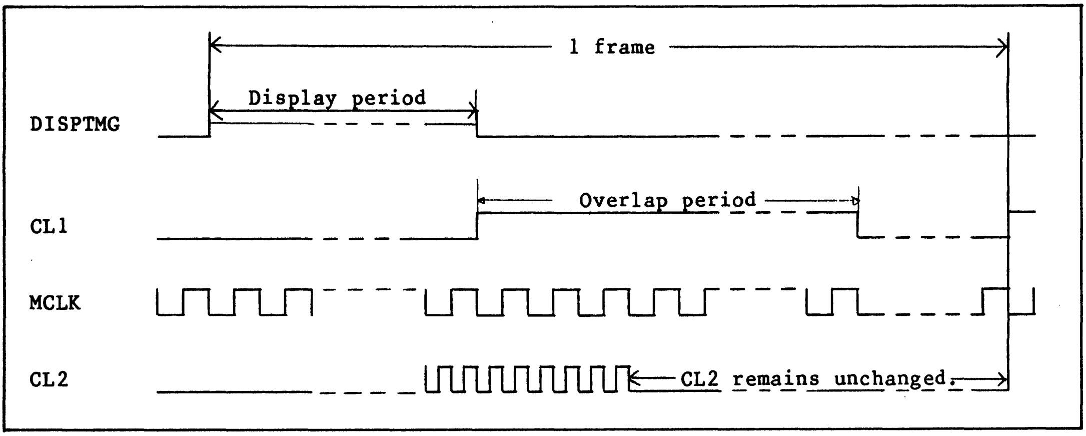


Figure 7-8 Relation between CL1 and CL2 (HD63645 and HD64645)

(1) Phase relations in the HD63645 and HD64645

Figure 7-8 shows the relation between CL1 and CL2. In the HD63645 and HD64645, CL1 is high for a long time (16 MCLK cycles) and CL2 changes during that time. Software cannot prevent this inconvenience. However, delaying CL1 with the external shift register can keep CL2 unchanged while CL1 is high. This is possible because the number of times MCLK and CL2 change while CL1 is high is fixed.

The relation between CL1 and CL2 differs from mode to mode but the relation between them and MCLK is fixed.

Table 7-2 Overlap of CL1 and CL2 in Each Mode

Mode No.	No. of CL2 Pulses during the Overlap Period	No. of MCLK Pulses during the Overlap Peiod
1, 2, 3, 4, 9, 10, 11, 12	3	3
5, 6, 7, 8, 13	6	3

Therefore delaying CL1 with the following shift register enables CL2 not to change while CL1 is high. If the period of DISPTMG = low is long, more than 4 flip-flop circuits can be connected.

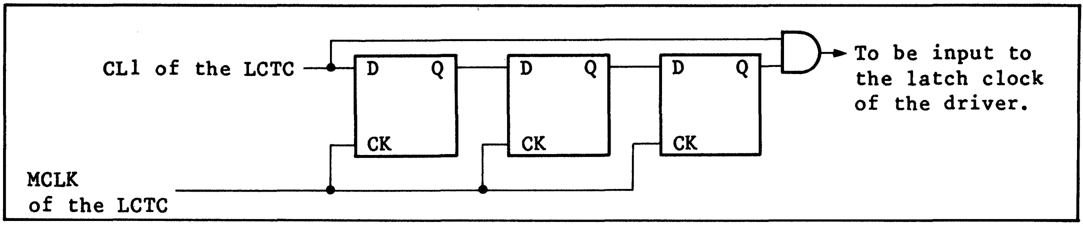


Figure 7-9 CL1 Corrector

The pulse width can be calculated from the previous information since the MCLK frequency is a quarter of the DCLK (= the operation clock input) frequency.

Make the difference great between the raster time and the display time (= the horizontal totol characters and the horizontal displayed characters) so that the periods of CL1 = high and DISPTMG = high may not overlap.

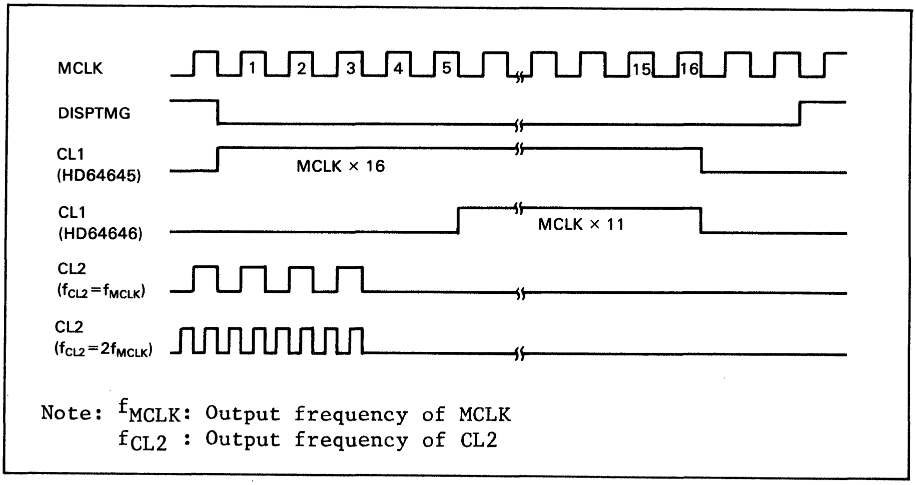
Some column drivers do not require any external circuit to correct CL1. For example, HD61104, HD66106 and HD66107 need no correction.

(2) Phase relation in the HD64646

Figure 7-10 and 7-11 shows the phase relations of DISPTMG, MCLK, CL1 and CL2 in the HD64646. The CL1 high period of the HD64646 is shorter than that of the HD64645. Figure 7-10 and 7-11 shows the timing chart without and with skew function, respectively. Figure 7-10 is no skew, and figure 7-11 is a case with skew function.

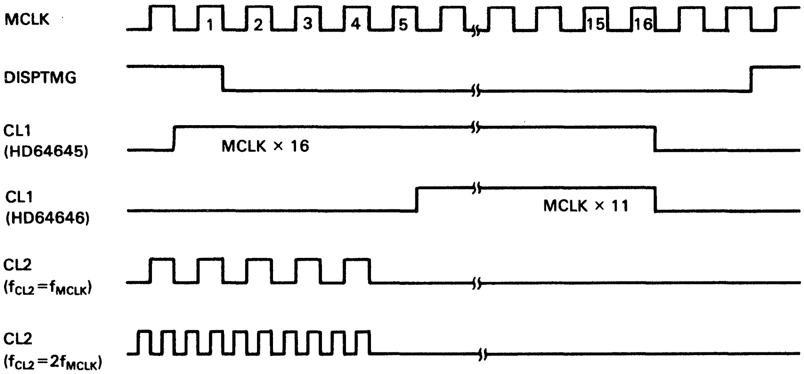
Figure 7-10 and figure 7-11 show the relation between display data transfer period, when display data shift clock CL2 changes, and display data latch clock CL1. Figure 7-10 is no skew, and figure 7-11 is a case with skew function.

For further information, refer to the LCD interface (HD64646) in chapter 14.

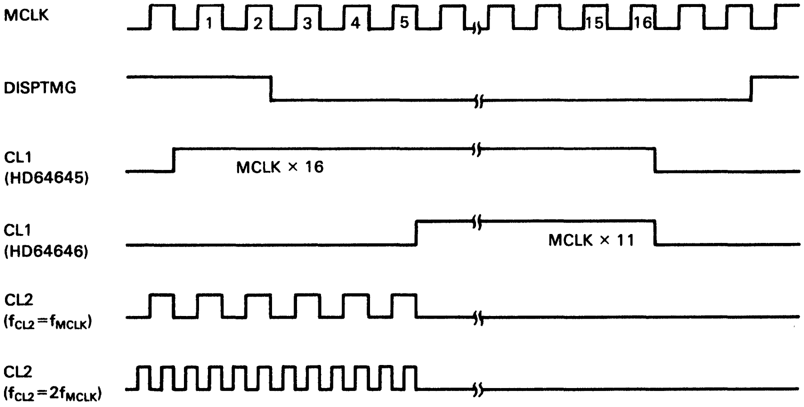


Note: f_{MCLK}: Output frequency of MCLK
f_{CL2} : Output frequency of CL2

Figure 7-10 Differences between HD64645 and HD64646 (no skew)



(a) 1 character skew



(b) 2 character skew

Figure 7-11 Differences between HD64645 and HD64646 (skew)

7.3 How to Access the Frame Buffer

As for the LCD system with the LCTC, the LCTC accesses the frame buffer, using the memory addresses (MA_0-MA_{15}) to refresh the display periodically. The MPU also accesses the frame buffer in changing the display. The MPU accesses in 2 ways; asynchronous access and synchronous access. The former is a way of accessing regardless of the display state and the latter is a way of accessing only during nondisplay time.

Figure 7-12 shows an example of the asynchronous access. When the address of the MPU specifies the frame buffer in the asynchronous access, the output of the address multiplexer is switched to the MPU address bus side. Thus a part of the display may flash momentarily then. Figure 7-13 shows the program of the asynchronous access.

Figure 7-14 shows an example of the synchronous access. Here the MPU reads the DISPTMG output and accesses only while DISPTMG = low (horizontal retrace period). In the synchronous access, display does not flash since the MPU access does not compete with the display access. Figure 7-15 shows the program of the synchronous access.

Figure 7-16 shows another example of the synchronous access. Here a character clock time is shared between the MPU access and the display access, and in the MPU access, READY signal stops ø2, the clock of the MPU, in order to give the MPU enough time to access the frame buffer. This method is called cycle-steal. Figure 7-17 shows the program then.

Since there are many ways to access the frame buffer besides the typical examples given here, it is necessary to adopt the best way according to your requirements.

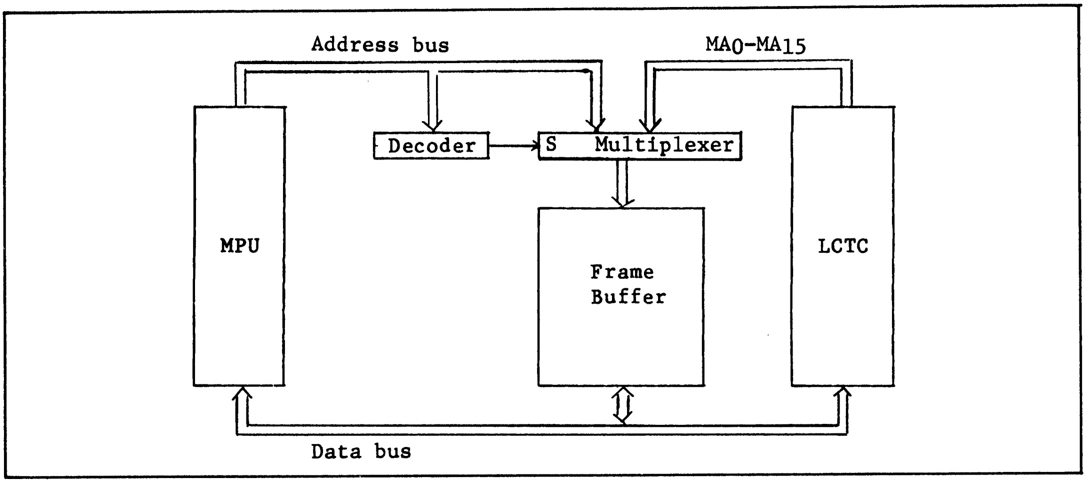


Figure 7-12 Asynchronous Access of the Frame Buffer

```
-
-
-
STA  A  FB   STORE ACCA INTO FB LOCATION
-
-
-
-
LDA  A  FB   LOAD FB LOCATION INTO ACCA
-
-
```

Figure 7-13 Program for the Asynchronous Access of the Frame Buffer

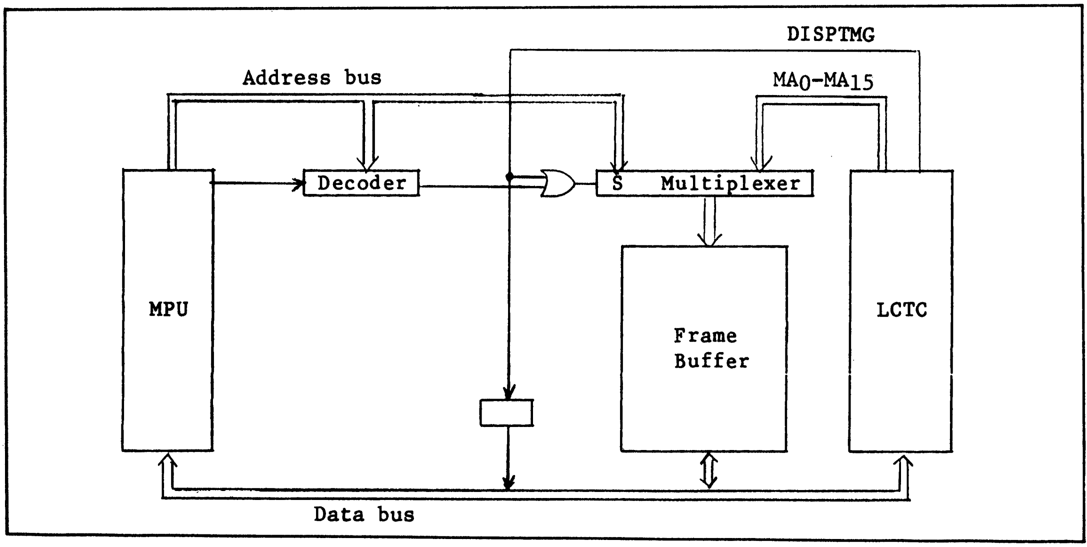


Figure 7-14 Synchronous Access of the Frame Buffer (1)

```
 -
 -
 -
LDA  A  DT   LOAD DISPTMG INTO ACCA
BIT  A  #1   BIT TEST
BGT     *-5  TRY AGAIN IF DT = 1
STA  B  FB   STORE ACCB INTO FB LOCATION
 -
 -
 -
LDA  A  DT   LOAD DISPTMG INTO ACCA
BIT  A  #1   BIT TEST
BEQ     *-5  SKIP IF ACCA = 0
LDA  B  FB   LOAD FB LOCATION INTO ACCB
```

Figure 7-15 Program for the Synchronous Access of the Frame Buffer (1)

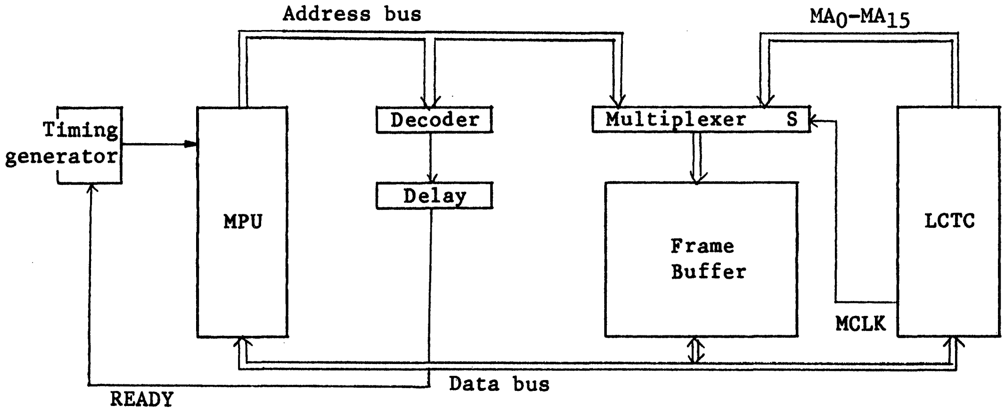


Figure 7-16 Synchronous Access of the Frame Buffer (2)

```
 -
 -
 -
STA   A  FB   STORE ACCA INTO FB LOCATION
 -
 -
 -
 -
LDA   A  FB   LOAD FB LOCATION INTO ACCA
 -
 -
```

Figure 7-17 Program for the Synchronous Access of the Frame Buffer (2)

7.4 Setting Parameters

Table 7-3 lists LCTC parameters depending on LCD control system specification, LCD screen configuration, or display functions (cursor display, scrolling display, etc.). Also shown are relevant LCTC each registers.

Table 7-3 LCTC Parameters

Parameters	LCD control system specification	LCD screen configuration	Display function	Setting method
DCLK frequency	△*	○		external circuit
Horizontal character dots		○		LCTC mode
Vertical character dots		○		R9
Total horizontal characters	○			R0
Horizontal displayed characters		○		R1
Vertical displayed dots		○		R19, R20
Skew	○			specified by pin
Cursor display mode			○	R10, R11
Start address			○	R12, R13
Cursor address			○	R14, R15
Horizontal virtual screen width		△*	○	R18
Display start raster			○	R21
Mode			○	R22, specified by pin

Note: The item marked with Δ is a secondary factor which limits the parameter.
(The item marked with ○ is a primary factor.)

7.4.1 Setting DCLK

LCTC operation clock frequency (DCLK) is specified depending on the number of dots on a screen and MPU memory access time.

DCLK frequency is obtained by the following expressions without considering MPU memory access time; that is, DISPTMG ≠ "L" and CL1 ≠ "L". DCLK frequency specification taking into account memory access time is described in the next section.

The symbols used in the following expression are:

·f_{DCLK}: DCLK frequency (Hz)
f_F: frame frequency (Hz)

Number of horizontal and vertical dots is defined as shown in Figure 7-18.

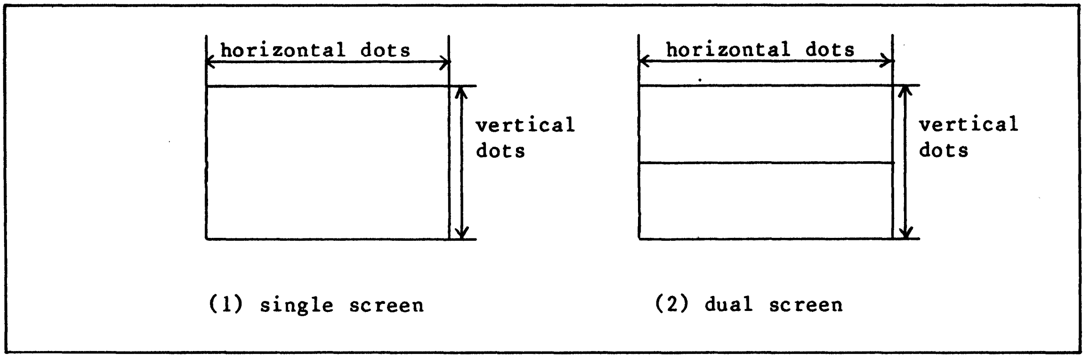
(1) All modes except mode 13

$$f_{DCLK} = \left(\frac{\text{number of horizontal dots}}{8} + \frac{16}{2*} \right) \text{x} \ \langle\text{number of vertical dots}\rangle \ \text{x} \ f_F \ \text{x} \ 4$$

* 16 is divided by 2 only in dual screen mode.

(2) Mode 13

$$f_{DCLK} = \left(\frac{\text{number of horizontal dots}}{16} + 8 \right) \text{x} \ \langle\text{number of vertical dots}\rangle \ \text{x} \ f_F \ \text{x} \ 4$$



(1) single screen

(2) dual screen

Figure 7-18 Screen Configuration and Dots

7.4.2 Setting parameters depending on memory access time

The MPU accesses a frame buffer using DISPTMG or cycle steal as shown in 7.3. This section describes how to set parameters when using DISPTMG.

LCTC timing for one display period includes a time interval for which LCTC does not accesses memory. During this period the MPU can access memory.

Figure 7-19 shows the timing diagram for 1 raster period. This period consists of the following as listed in Table 7-4.

Table 7-4 1 raster period

No.	item	DISPTMG	CL1	period
1	LCTC memory access time	High	Low	$n \cdot T_{DCLK} \cdot Nhd$
2	DRAM refresh time	Low	High	$64\ T_{DCLK}$
3	MPU memory access time	Low	Low	$n \cdot T_{DCLK}\ (Nht + 1 - Nhd) - 64\ T_{DCLK}$

*1 Nhd = number of horizontal displayed characters
Nht = total number of horizontal characters (data to be written)
T_{DCLK} = DCLK period

*2 n = constant

Relation between mode No. and constant n

Mode no.	Constant n
5, 9	4
1, 6, 7, 8, 10, 11, 13	8
2, 3, 4	16

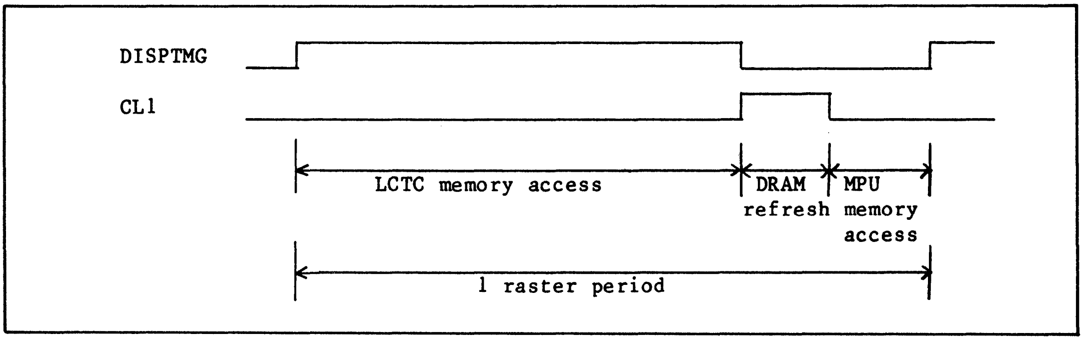


Figure 7-19 LCTC 1 raster period

As shown in Figure 7-15, the following relationship holds as to a raster period (= T_{RAS}), LCTC memory access time (= T_{LCTC}), DRAM refresh time (= T_{DRAM}), and MPU memory access time (= T_{MPU}):

$$T_{RAS} = T_{LCTC} + T_{DRAM} + T_{MPU} \qquad (7\text{-}1)$$

T_{RAS}, T_{LCTC}, and T_{DRAM} can be obtained by the following expressions:

$$T_{RAS} = n \cdot T_{DCLK} \cdot (Nht + 1) \qquad (7\text{-}2)$$

$$T_{LCTC} = n \cdot T_{DCLK} \cdot Nhd \qquad (7\text{-}3)$$

$$T_{DRAM} = 64 \cdot T_{DCLK} \qquad (7\text{-}4)$$

Thus, T_{MPU} is expressed as follows:

$$T_{MPU} = n \cdot T_{DCLK} \cdot (Nht + 1 - Nhd) - 64 \cdot T_{DCLK} \qquad (7\text{-}5)$$

While T_F is expressed as follows since it is the result of <a raster period> × <number of raster per panel (= Nd)>.

$$T_F = T_{RAS} \cdot (Nd + 1)$$

$$\therefore\ T_F = n \cdot T_{DCLK} \cdot (Ndt + 1)(Nd + 1) \qquad (7\text{-}6)$$

The following expression derives from (7-5) and (7-6):

$$T_{DCLK} = \left(\frac{T_F}{Nd + 1} - T_{MPU}\right) \cdot \frac{1}{n \cdot Nhd + 64} \qquad (7\text{-}7)$$

T_F depends on LCD characteristics and Nhd and Nd on screen configuration. The value of T_{DCLK} is, therefore, specified by T_{MPU}. DCLK frequency is a result of expression (7-7) when $T_{MPU} = 0$.

Nht, therefore, is obtained by expression (7-6) depending on applicable T_{DCLK}.

$$Nht = \frac{T_F}{n \cdot T_{DCLK} \cdot (Nd + 1)} - 1$$

Specifically, T_{MPU} can be set according to any value of (Nht - Nhd).

The user should take into account the following limitation:

(1) $T_{DCLK} \geqq 100$ ns

(2) $1 \leqq Nhd \leqq Nht + 1 \leqq 256$

(3) $Nhd + \frac{64}{n} \leqq Nht + 1$

7.4.3 Setting parameters depending on LCD screen configuration

(1) Horizontal character dots

The number of horizontal character dots basically depends on character font and space between characters as shown by the example in Figure 7-20. However, when using the LCTC, this number is either 8 or 16 depending on LCTC modes, so total of character font and space between characters should be 8 or 16 dots. Table 7-5 shows relation between mode and horizontal character dots.

Table 7-5 Relation between LCTC Modes and Number of Horizontal Character Dots

Mode No.	Number of horizontal character dots
1, 5, 9	8
2, 3, 4, 6, 7, 8, 10, 11, 12, 13	16

(2) Vertical character dots

The number of vertical character dots also depends on character font and space between characters as shown in Figure 7-20. The user should set the number of vertical character dots in the maximum raster address register (R9).

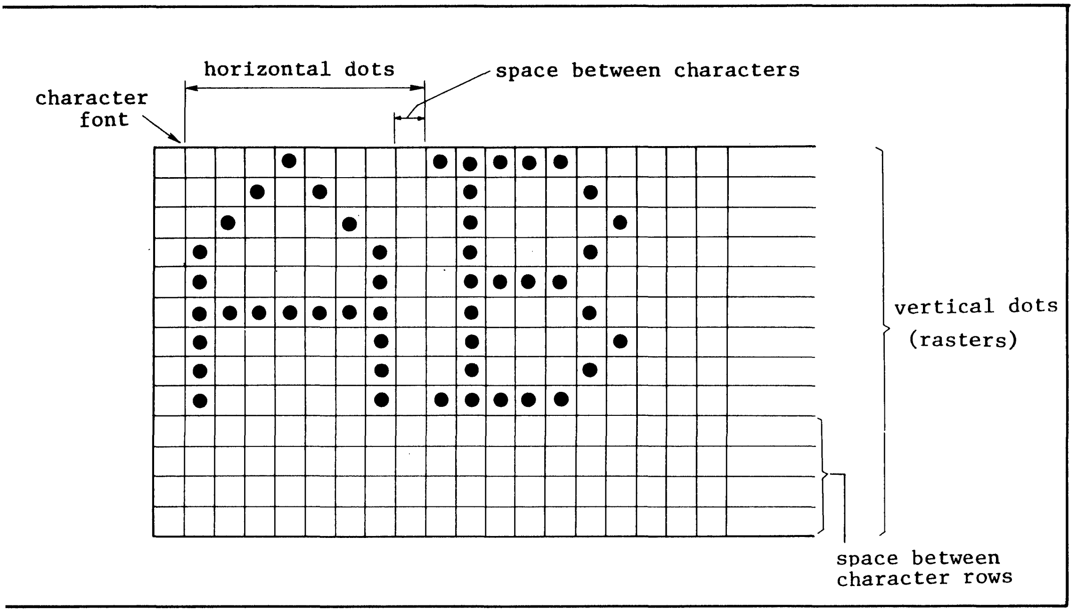


Figure 7-20 Character Dots

(3) Horizontal displayed characters

The user should set R1 to a value obtained by dividing the number of LCD horizontal dots in the specified mode by the number of horizontal character dots. In this case, the value should be rounded up to an integral number of dots.

The number of horizontal character dots depends on LCTC mode; consequently if LCTC mode is changed with screen configuration unchanged, R0 and R1 must be reinitialized.

(4) Vertical displayed rasters

The user should set R19 and R20 to the number of vertical displayed dots depending on LCD screen configuration.

In case of single screen:

$$\text{(set value)} = \langle\text{number of vertical dots}\rangle - 1$$

In case of dual screen:

$$\text{(set value)} = \frac{\langle\text{number of vertical dots}\rangle}{2} - 1$$

In single screen, even if the set value is greater than the above, LCD can still perform display, however, since picture quality is degraded in this case, it is recommended to use the value shown above.

The following describes examples of setting values for in each screen configuration. In this case, f_{DCLK} = 10 MHz and f_F = 65 to 70 MHz.

(i) 640 x 200 dots, 1/200 duty, single screen

(a) Mode 5 (character mode)

Nht = 178 (R0 set value)
Nhd = 80 (R1 set value)
Nd = 199 (R19, R20 set value)

(b) Mode 7 (graphic 1 mode)

Nht = 89 (R0 set value)
Nhd = 40 (R1 set value)
Nd = 199 (R19, R20 set value)

(ii) 640 x 400 dots, 1/200 duty, dual screen

(a) Mode 1 (character mode)

Nht = 89 (R0 set value)
Nhd = 80 (R1 set value)
Nd = 199 (R19, R20 set value)

(b) Mode 3 (graphic 1 mode)

Nht = 44 (R0 set value)
Nhd = 40 (R1 set value)
Nd = 199 (R19, R20 set value)

(c) Mode 13 (large screen graphic 1 mode)

Nht = 89 (R0 set value)
Nhd = 40 (R1 set value)
Nd = 199 (R19, R20 set value)

7.4.4 Setting parameters depending on display functions

This section describes parameters for display functions (scrolling, etc.) which is almost independent of LCD hardware (LCD control system, screen configuration, etc.).

(1) Cursor display

The LCTC can program display mode of cursor as listed in Table 10-1 and display shape of cursor as shown in Figure 10-5 with cursor start raster register (R10) and cursor end raster address (R11). Therefore, the LCTC can not only realize cursor display but also change cursor display shape according to the system. For details, see chapter 10 "CURSOR CONTROL".

(2) Start address

Start address registers (R14, R15) can provide an offset for read address of frame buffer. This function enables easy paging and scrolling. For details, see chapter 9 "PAGING AND SCROLLING".

(3) Cursor address register

Cursor display position can be programmed by cursor address registers (R14, R15). In this case, the user can program memory address of frame buffer, not X and Y addresses. For details, see chapter 10 "CURSOR CONTROL".

(4) Horizontal Virtual Screen Width

Horizontal virtual screen width register (R18) can provide an offset for start addresses of adjoining two lines. This function enables easy horizontal scrolling. For details, see chapter 9 "PAGING AND SCROLLING".

(5) Display start raster

Display start raster register (R21) can provide an offset for start raster of the first row. This function enables smooth scrolling. For details, see chapter 9 "PAGING AND SCROLLING".

(6) Mode

The LCTC controls display mode (display ON/OFF, wide display, etc.) with mode register (R22). For details, see chapter 8 "MODE REGISTER FUNCTIONS".

7.5 Easy Mode

In order to maintain software compatibility with the CRTC, easy mode is used to specify registers that the CRTC (HD6845) does not provide or which determine vertical dots in a way different from the CRTC by setting the MODE pin to high. Table 7-6 lists such registers and each fixed value. These registers determine a fixed mode and display format and allows software designed for a system using the CRTC to be displayed on an LCD without rewriting BIOS.

Table 7-6 Registers and Set Values in Easy Mode

Register No.	Registers	Fixed value (decimal)
R9	Maximum raster address register	7
R10	Cursor start raster register	6
R11	Cursor end raster register	7
R18	Horizontal virtual screen width register	same value as R1
R19	Multiplexing duty ratio register (H)	99 (in dual screen)
R20	Multiplexing duty ratio register (L)	199 (in single screen)
R21	Display start raster register	0
R22	Mode register	0

Other registers (AR, R0, R1, R12, R13, R14, R15) are independent of the status of the MODE pin, so that the user can change their contents even when MODE pin is set to high.

The following is a detailed description of the above registers in easy mode.

(1) Maximum raster address register (R9)

This register is fixed at (R9) = 00111 (binary) (= 8 rasters/row) by an internal operation in easy mode. The register state is held after the easy mode is released. In setting (R19)/(R20) again, make a rewrite after releasing the easy mode by setting the MODE pin low. (If $G/\overline{C}$ pin is high, rewriting is possible even when MODE pin is high.)

(2) Cursor start/end raster register (R10/R11)

These registers are fixed at (R10) = 00110 (binary) (= 7th raster)/(R11) = 00111 (binary) (= 8th raster) by internal operations in the easy mode. In this case, there is no blinking. After easy mode is released, the registers return to their original states.

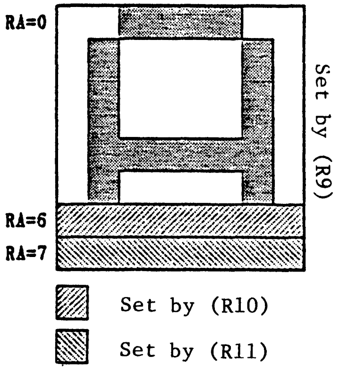


Figure 7-21 (R9)(R10)(R11) Status when MODE = High

(3) Multiplexing duty ratio register (high-order byte: R19/low-order byte: R20)

These registers are fixed at (R19) = 0 (binary)/(R20) = 01100011 (binary) (=1/100 duty) in easy mode if $D/\overline{S}$ pin is set high (dual screen) or at (R19) = 0 (binary)/(R20) = 11000111 (binary) (= 1/200 duty) if $D/\overline{S}$ pin is set low (single screen) respectively. The register state remains unchanged after easy mode is cancelled. In setting (R19)/(R20) again, rewrite these registers after cancelling easy mode by setting the MODE pin low.

(4) Display start raster register (R21)

This register is cleared and fixed at (R21) = 00000 (binary) in easy mode. Therefore, smooth scroll is impossible in easy mode. This state remains unchanged even after easy mode is cancelled. In setting the register again, cancel easy mode first.

(5) Mode register (R22)

This register is cleared and fixed at (R21) = 00000 (binary) in easy mode. However, its function can be perfectly controlled by external pin $ON/\overline{OFF}$ (pin 53), $G/\overline{C}$ (pin 58), WIDE (pin 54), BLE (pin 51), and AT (pin 57). This state remains unchanged after easy mode is cancelled. For control by register (R22), cancel the easy mode first.

(6) Horizontal virtual screen width register (R18)

This register becomes equivalent to the horizontal displayed characters register (R1) in easy mode. Since display data is stored continuously in the VRAM, horizontal scrolling is impossible. To change the set value of this register in easy mode, the contents of register (R1) must be rewritten. After easy mode is cancelled, the register returns to its original state.

8. MODE REGISTER FUNCTIONS

8.1 Mode Registers and Display Modes

Take special note that the data bits of the mode register and external pins of the same names are respectively ORed together.

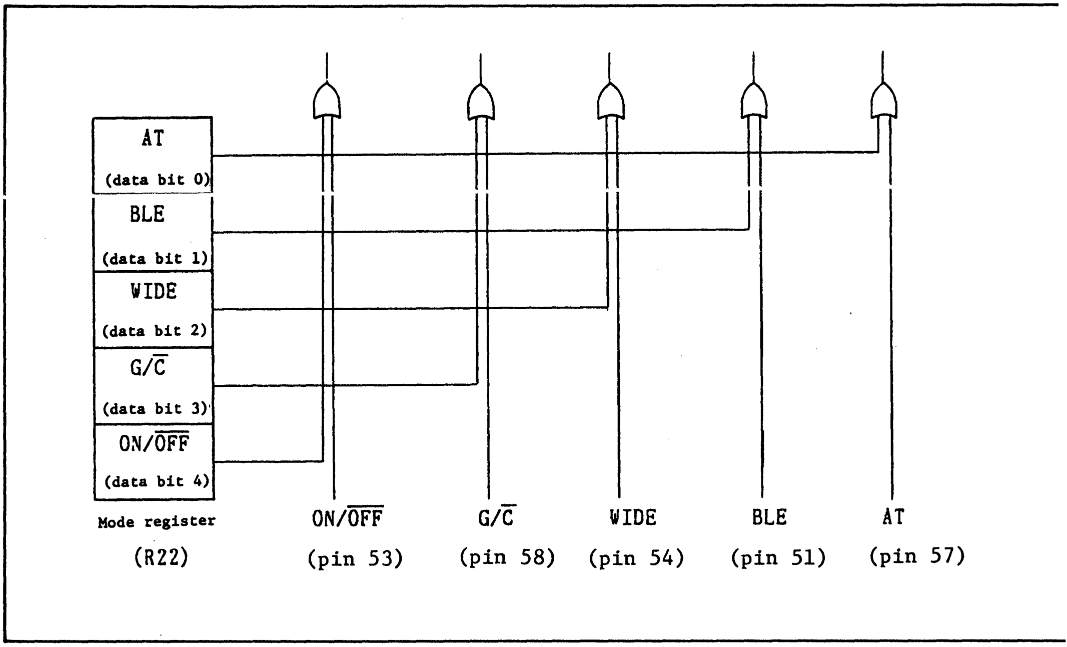


Figure 8-1 Correspondence between Mode Register and External Pin

BLE and WIDE bits are valid only in character mode.

Table 8-1 Mode Register Bits and Display Modes

	AT	BLE	WIDE	G/$\overline{C}$	ON/$\overline{OFF}$
Character mode	○	○	○	—	○
Graphic 1 mode	—	×	×	—	○
Graphic 2 mode	—	×	×	—	○

(note) ○ = valid
× = invalid
— = switching bit for display mode

8.2 Attributes (Mode Register Data Bit 0)

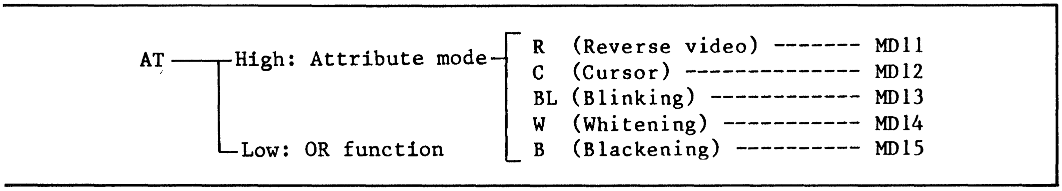

AT
High: Attribute mode
Low: OR function
R (Reverse video) ------- MD11
C (Cursor) -------------- MD12
BL (Blinking) ------------ MD13
W (Whitening) ----------- MD14
B (Blackening) ---------- MD15

Figure 8-2 Attribute Function

8.2.1 Attribute mode (AT = high)

When this bit or pin 57 is set to high, ARAM data serves as attribute data. This data operates on the character corresponding to the VRAM character code at a same address.

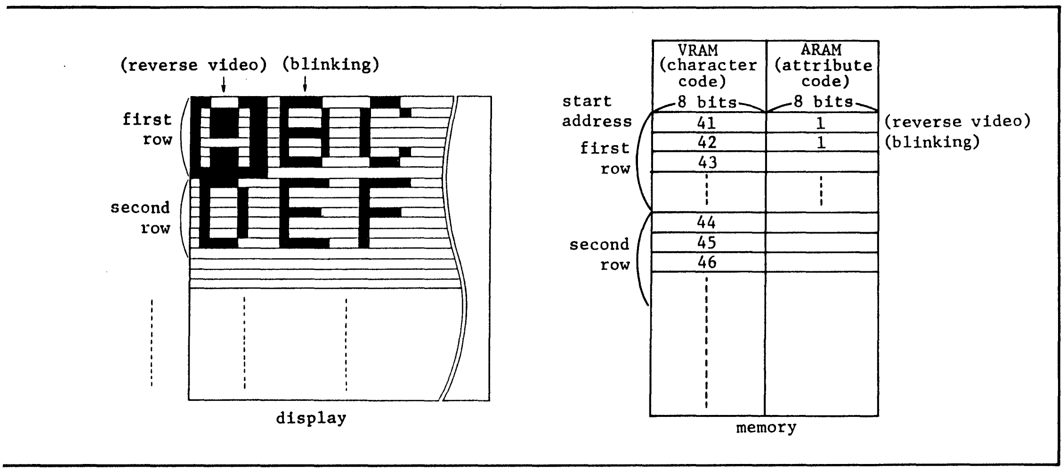


Figure 8-3 Relation between Character Display and Memory

(1) R (Reverse video): When data (ARAM data corresponding to an address specified by the MA pin) entered into MD11 pin is set to high, the data entered from MD0-MD7 is reversed (0→1, 1→0) and output from LU0-LU3 and LD0-LD3.

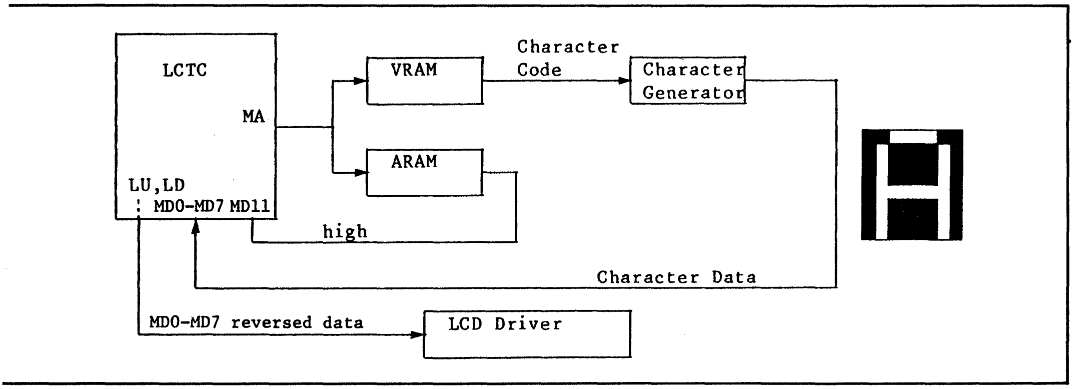
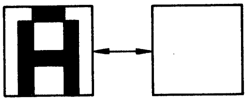


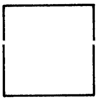
Figure 8-4 Reverse Video System

(2) C (Cursor): To display a cursor,
1. Set the cursor start/end raster register (including B and P).
2. Connect CUDISP with MD12.
For further details, refer to chapter 10 "CURSOR CONTROL".

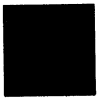
(3) BL (Character blinking): When data (ARAM data corresponding to an address specified by the MA pin) entered into MD13 pin and BLE are set to high (BLE can be controlled by external pin or data bit 2 of mode register), the specified character is blinked on for 32 frames and off for the next 32 frames. This operation is performed repeatedly.



(4) W (Whitening): When data (ARAM data corresponding to an address specified by the MA pin) entered into MD14 pin is set to high, the specified character is whitened regardless of the data entered from MD0-MD7.



(5) B (Blackening): When data (ARAM data corresponding to an address specified by the MA pin) entered into MD15 pin is set to high, the specified character is blacken regardless of the data entered from MD0-MD7.



8.2.2. Attribute data overlay

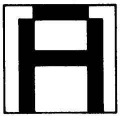
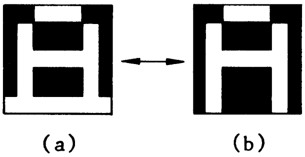
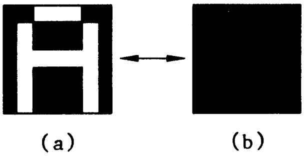
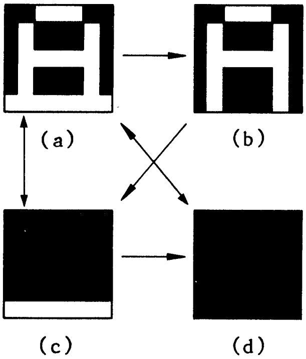
8.2.1. describes each individual attribute data function of the LCTC. This section describes attribute data overlay.

Basically, the LCTC attribute data has the following relation:

$$R > C > W > BL > B$$

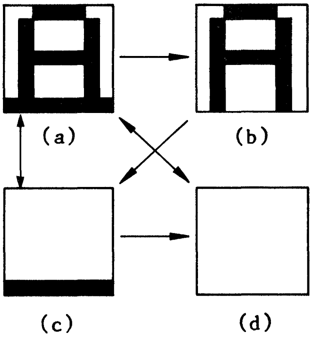
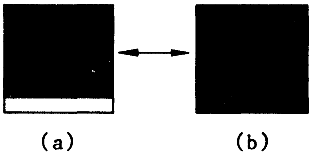
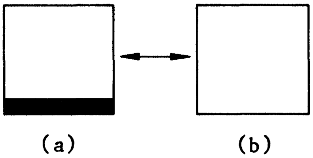
For more details, refer to Table 8-2.

Table 8-2 Attribute Data Overlay List

Attribute Data					Panel Display	Remarks
B	W	BL	C	R		
0	0	0	◎	0		Without any character attributes
0	0	0	*	1	 	(1) Repeats (a)⟷(b), with cursor blinking. (2) Keeps (a), without cursor blinking.
0	0	1	◎	1	 	Repeats (a)⟷(b) on 32 frames each.
0	0	1	*	1	 	(1) Repeats (a)⟷(c), without cursor blinking. (2) Repeats (a)⟷(d), if blink rate of cursor is the same as that of character. (3) Repeats (a)⟶(b)⟶(c)⟶(d)⟶(a), if blink rate of cursor is half that of character.

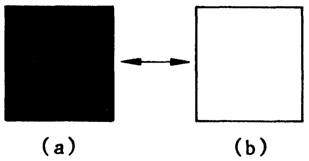
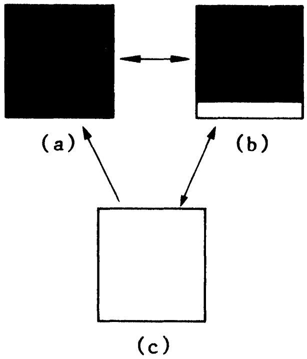
(continued)

* : CUDISP signal entry.
◎ : C (MD12 pin) fixed at low.
For more details, refer to chapter 10, "CURSOR CONTROL".

Attribute Data					Panel Display	Remarks
B	W	BL	C	R		
0	0	1	*	0		(1) Repeats (a)⟷(c), without cursor blinkin (2) Repeats (a)⟷(d), if blink rate of cursor i the same as that of character. (3) Repeats (a)⟶(b)⟶(c ⟶(d)⟶(a), if blink rate of cursor is half that of character.
0 0 1 1	1 1 1 1	0 1 0 1	* * * *	1 1 1 1		(1) Keeps (a), without cur blinking. (2) Repeats (a)⟷(b), wi cursor blinking.
0 0 1 1	1 1 1 1	0 1 0 1	* * * *	0 0 0 0		(1) Keeps (a), without cur blinking. (2) Repeats (a)⟷(b), wi cursor blinking.

(continue

* : CUDISP signal entry.
For more details, refer to chapter 10, "CURSOR CONTROL".

Attribute Data					Panel Display	Remarks
B	W	BL	C	R		
1 1	0 0	1 1	◎ ◎	1 0		Repeats (a)⟷(b) on 32 frames each.
1	0	1	*	1		(1) Repeats (a)⟷(b) on 32 frames each, without cursor blinking. (2) Repeats (b)⟷(c) on 32 frames each, if blink rate of cursor is the same as that of character. (3) Repeats (a)⟶(b)⟶(c) ⟶(a) in a cycle of 16-16-32 frame, if blink rate of cursor is half that of character.

* : CUDISP signal entry.
◎ : C (MD12 pin) fixed at low.
For more details, refer to chapter 10, "CURSOR CONTROL".

8.3 Blink Enable (BLE) (Mode Register Data Bit 1)

This data bit controls character blinking. A given character can blink only when this bit or external pin 51 and attribute data (AT = high) MD13 are set to high. 32 frames blink periodically.

8.4 Wide (WIDE) (Mode Register Data Bit 2)

This data bit controls wide character display. Normally, one character is displayed in 8-dots width. When this bit or external pin 54 is set high, one character can be displayed in 16 dots width. When normal mode is switched to wide mode, the number of horizontal dots for one character and the horizontal scanning period are doubled, and so the screen flickers. Therefore, the total number of horizontal characters and the number of horizontal displayed characters in wide mode must be half those in normal mode.

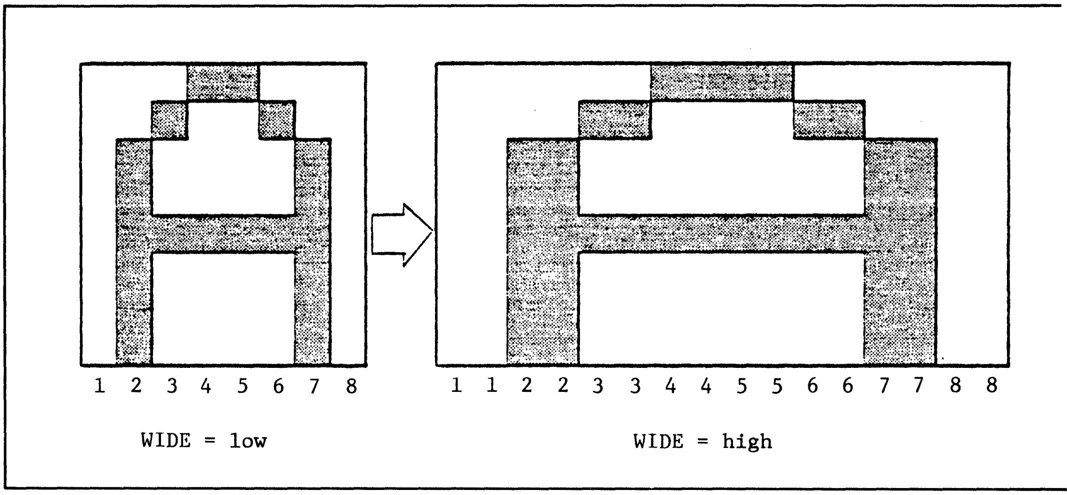


Figure 8-5 Example of Display in Wide Mode

8.5 Graphic/Character (G/$\overline{C}$) (Mode Register Data Bit 3)

This data bit determines graphic display or character display. When the bit or external pin 58 is set to high, graphic display is available. When both are set to low, character display is available. In graphic mode, one address output causes 2-byte dot data to be entered. In character mode, 1-byte dot data and 5-bit attribute data are entered. Also, the same memory address is output by a count specified by the maximum raster address register. In graphic mode, MA output increases without repetition.

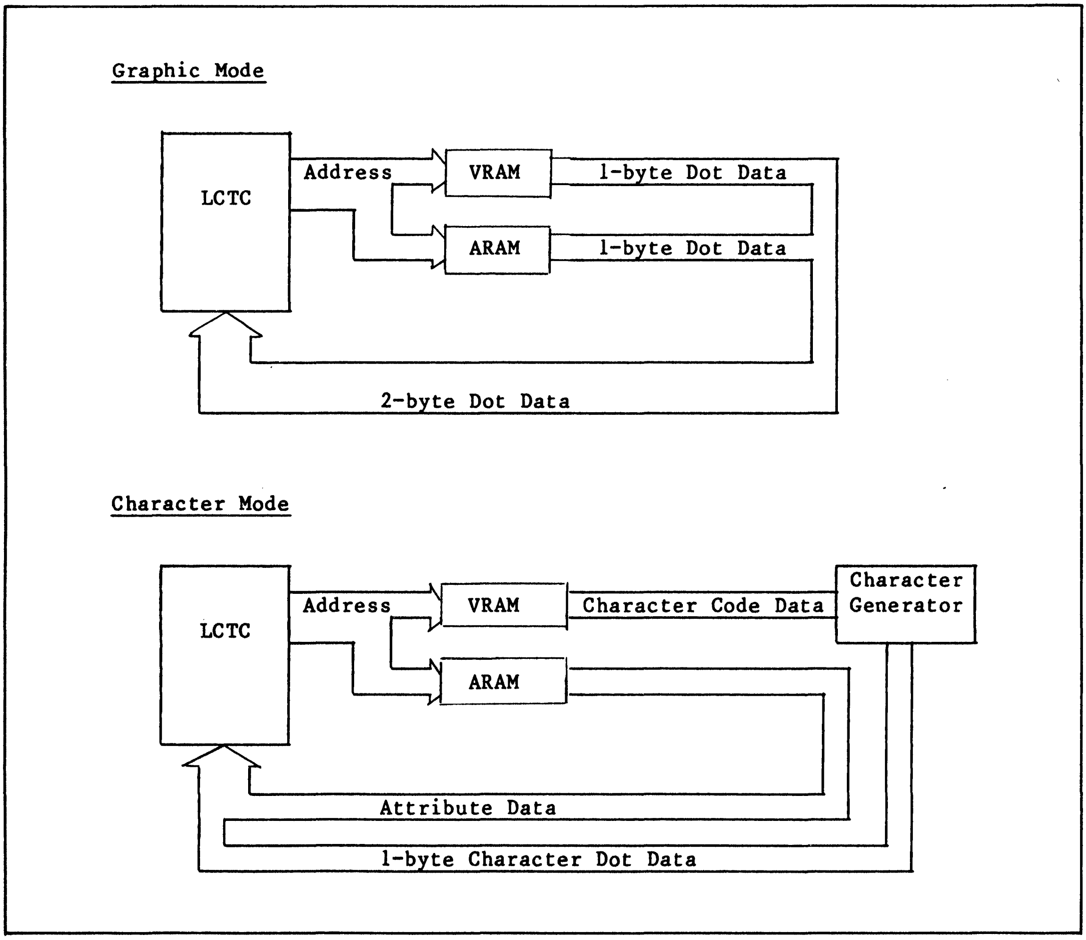
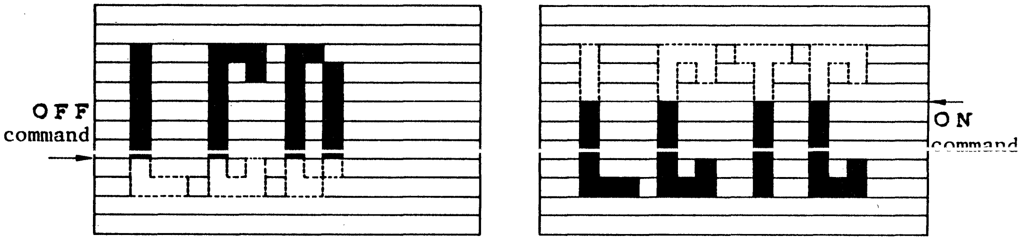


Figure 8-6 Graphic Mode and Character Mode

8.6 Display On/Off (ON/$\overline{\text{OFF}}$) (Mode Register Data Bit 4)

This data bit controls switching on/off of the whole LCD display. When this bit and external pin 53 is set to low, display data transfer is stopped. Low is output from LU0-LU3 and LD0-LD3 until either of this bit or pin 53 is set to high. When display is switched on, data transfer is restarted according to address output.



display ON → OFF
(command entered within a frame; all off by next frame)

display OFF → ON
(command entered within a frame; all on by next frame)

Figure 8-7 Example of Display On and Off

9. PAGING AND SCROLLING

The LCTC supports 8-directional scrolling by character, vertical smooth scrolling, and paging by renewing the start address registers (R12, R13), the horizontal virtual screen width register (R18) and display start raster register (R21).

For special note when often rewriting start address register for scrolling or paging, or often rewriting display start raster register for smooth scrolling, refer Appendix A "Abnormal Operation by Rewriting Registers in Display".

9.1 Horizontal Scrolling

9.1.1. Horizontal scrolling function

The horizontal virtual screen width register (R18) facilitates high-speed horizontal scrolling, compared with conventional horizontal scrolling which rewrites an entire screen. The following figure illustrates horizontal scrolling by using virtual screen width.

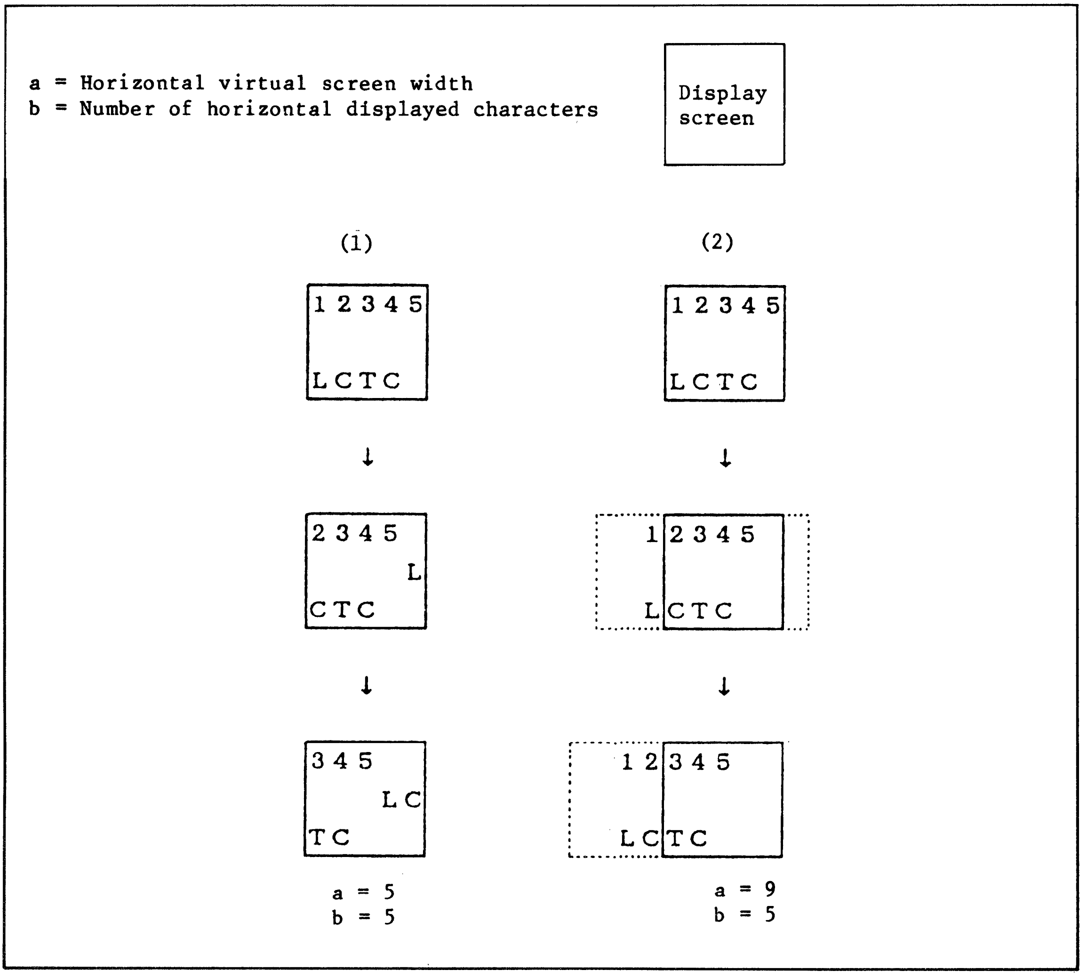


Figure 9-1 Horizontal Scrolling on Virtual Screen

Example (1) shows continuous memory addresses which are all placed in the display area; therefore, no character can be scrolled horizontally. Example (2) shows that virtual screen width facilitates high-speed horizontal character scrolling by setting start address.

9.1.2. Horizontal scrolling method

The display screen is scrolled to the left or right on a character basis by incrementing or decrementing the start address registers (R12, R13) one by one.

R12 and R13 indicate the high-order and low-order bytes of the start address respectively. If leftward scrolling starts at "(R12) = (R13) = \$00", only (R13) must be incremented by one. If it starts at "(R12) = \$01" and "(R13) = \$FF", for example, "(R12) = \$02" and "(R13) = \$00" must be set. For rightward scrolling, (R13) must be decremented by one.

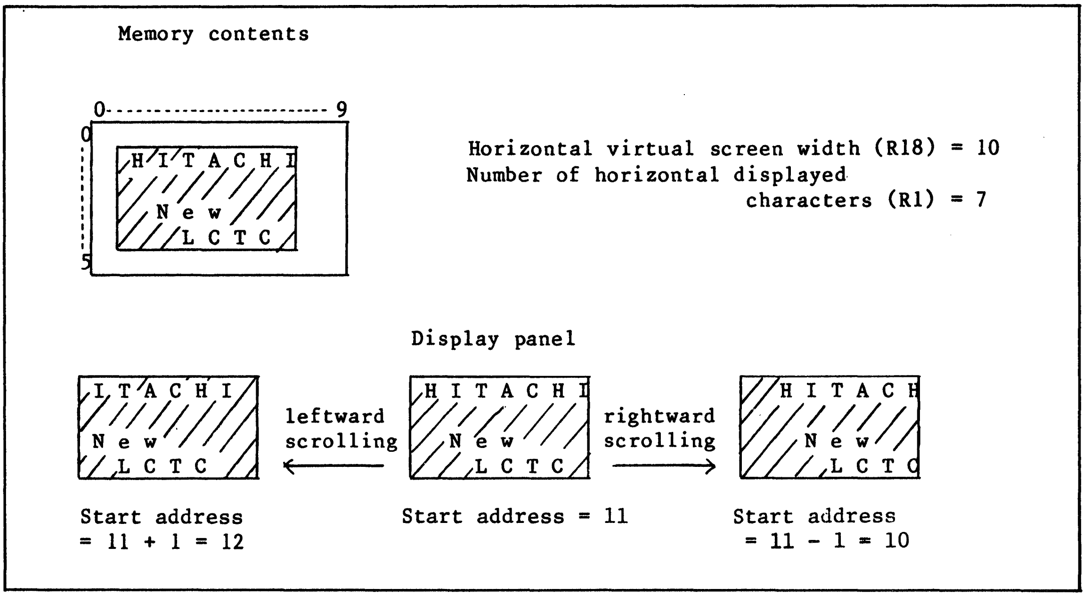


Figure 9-2 Leftward/Rightward Character Scrolling

9.2 Vertical Scrolling Function

The vertical scrolling function involves character scrolling and smooth scrolling.

9.2.1 Vertical character scrolling method

To scroll characters vertically, the user should manipulate the start address registers (R12: high-order 8 bits),(R13: low-order 8 bits) in the same manner as horizontal character scrolling. To scroll characters up and down, repeat the following procedure at fixed intervals.

Upward character scrolling: Prescroll start address + horizontal virtual screen width
Downward character scrolling: Prescroll start address - horizontal virtual screen width

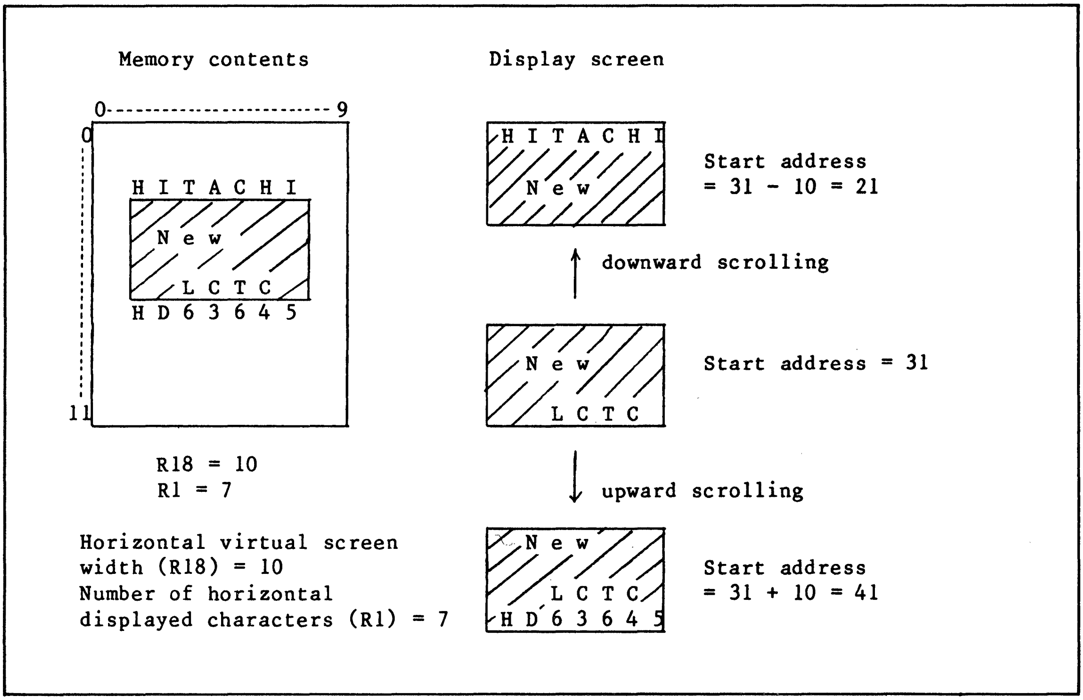


Figure 9-3 Upward/Downward Character Scrolling

9.2.2 Vertical smooth scrolling method

Vertical smooth scrolling requires the functions of display start raster register (R21) and start address registers (R12/R13). Figure 9-4 shows the vertical smooth scrolling method.

Upward smooth scrolling

(1) Enter 0 into (R12/R13) and (R21).

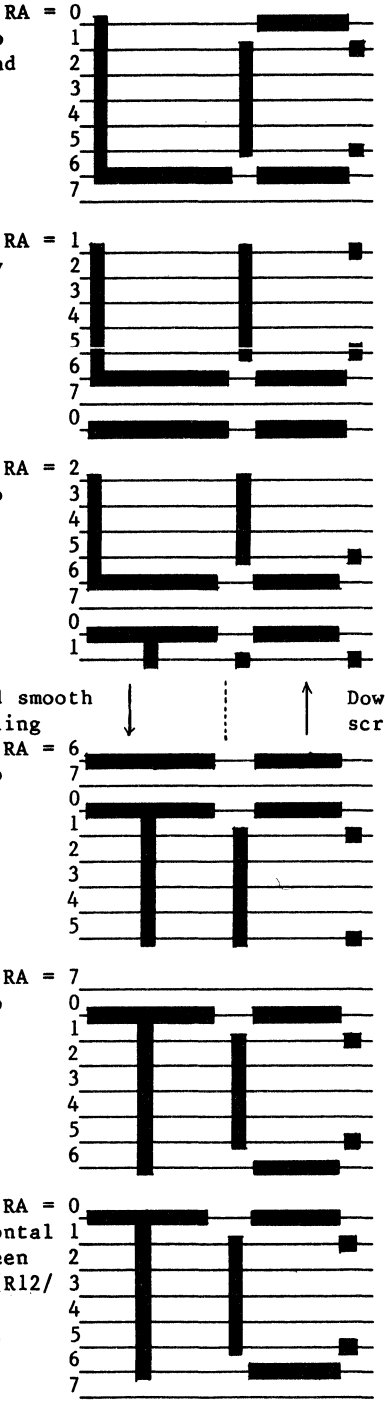
(2) Enter 1 only into (R21).

(3) Enter 2 into (R21).

(4) Enter 6 into (R21).

(5) Enter 7 into (R21).

(6) Enter horizontal virtual screen width into (R12/R13). Reset (R21).



Downward smooth scrolling

(1) Enter horizontal virtual screen width into (R12/R13) and 0 into (R21).

(2) Enter 0 into (R12/R13) and 7 into (R21).

(3) Enter 6 only into (R21).

(4) Enter 2 into (R21).

(5) Enter 1 into (R21).

(6) Enter 0 into (R21).

Repeat the above procedure at fixed intervals.

Figure 9-4 Example of Vertical Smooth Scrolling

9.2.3. Vertical character scrolling applications (multi-directional scrolling)

The following operations of the LCTC provide a variety of scrolling functions according to the relation between the start address register (R12)/(R13) and the horizontal virtual screen width register (R18).

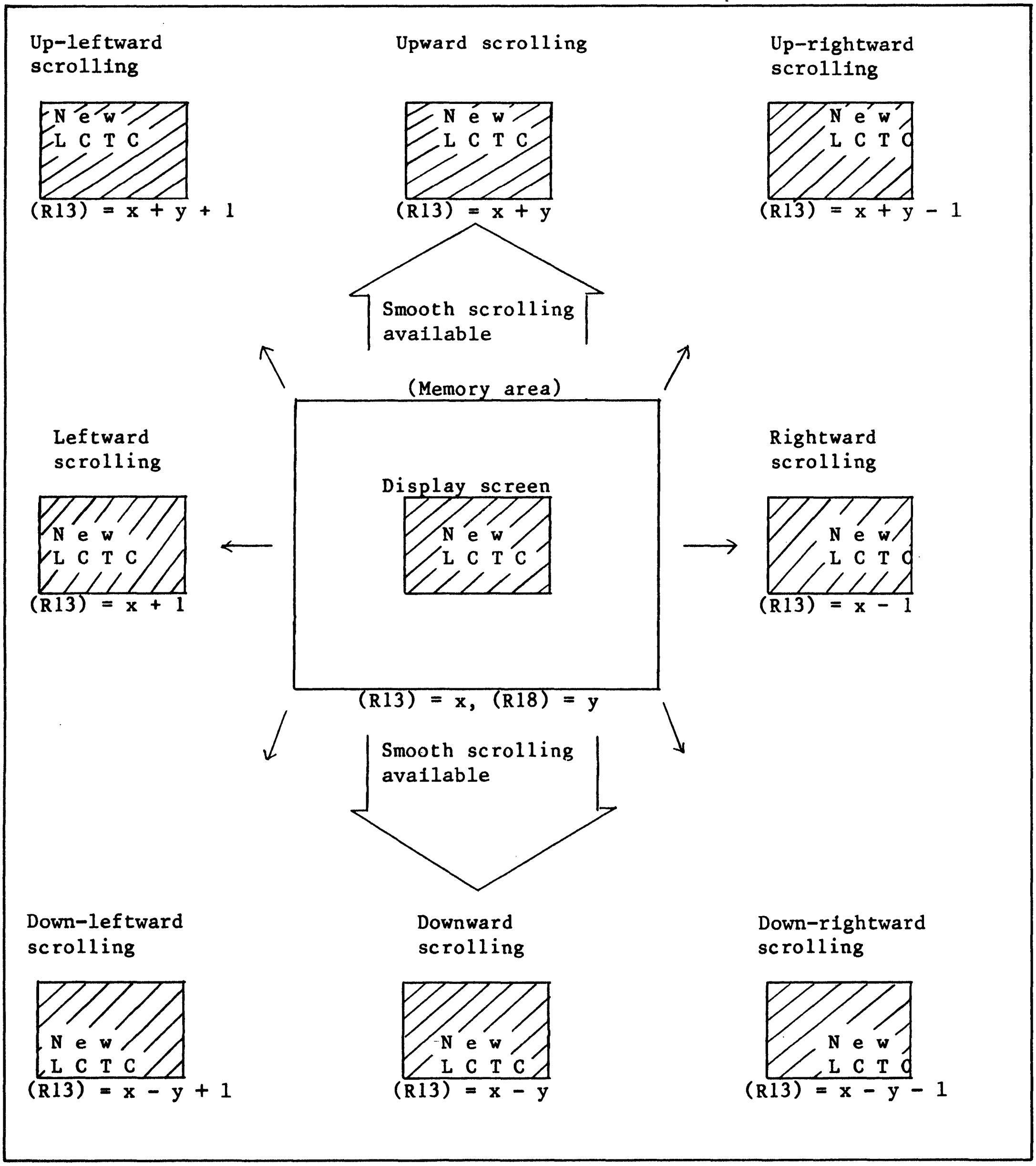


Figure 9-5 LCTC Character Scrolling

9.3 Paging Function

The LCTC is capable of accessing up to 64-kbyte VRAM. Its paging function provides display switching operation at a higher speed than the conventional one which must perform paging by rewriting RAM contents.

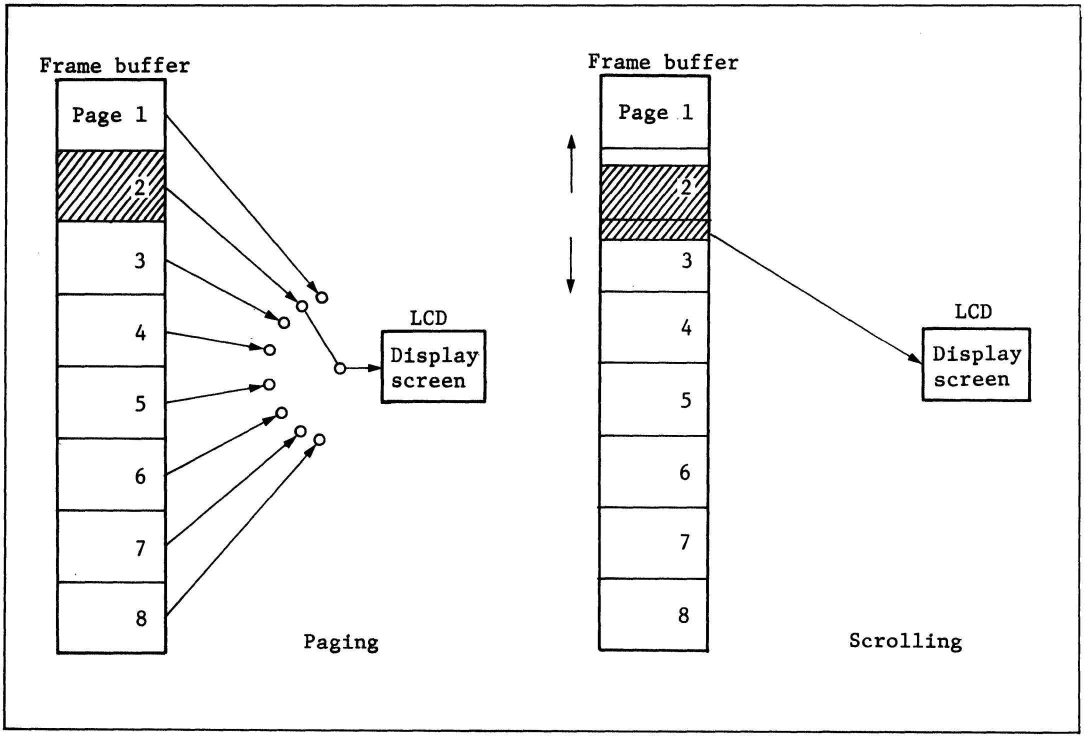


Figure 9-6 Paging and Scrolling

The LCTC uses the start address registers (R12/R13) to control paging and scrolling. Scrolling is defined as continuous change of display addresses, while paging as step-by-step change of display addresses.

10. CURSOR CONTROL

The following conditions must be satisfied to display a cursor when using the LCTC:

1. Selecting character mode and attribute function
2. Connecting CUDISP signal with MD12 pin
3. Setting cursor start/end raster register (R10,R11)
4. Setting cursor address register (R14,R15)

The LCTC can control cursor position, on/off state, blinking cycle and shape.

10.1 Cursor Position

Cursor position is specified by the cursor address registers (R14: high-order byte, R15: low-order byte). An address specified here corresponds to a buffer memory address. If a cursor address is specified outside the display screen, no cursor is displayed.

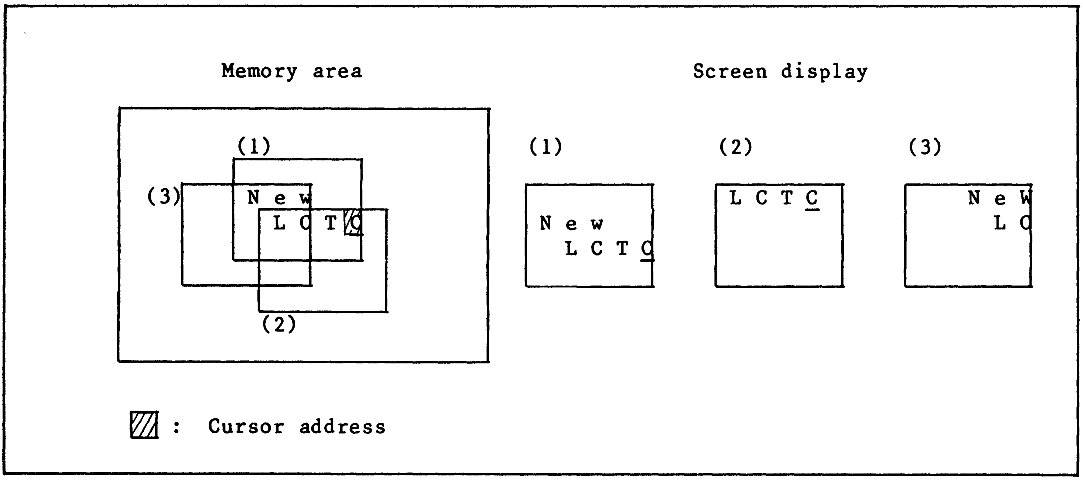


Figure 10-1 Relation between Cursor Address and Screen Display

Figure 10-1 shows the change of screen display when a start address in a memory area is changed. If the shaded part is specified as a cursor address, a cursor is displayed in (1) and (2). But no cursor is displayed in (3). Software control is required to display a cursor constantly on a display.

10.2 Cursor On/Off and Blinking Cycle

The LCTC requires an external signal to display a cursor. CUDISP signal is used as an external input via pin 36. Two kinds of methods for controlling on/off or blinking of this signal are available: one uses internal registers and the other uses an external signal to perform blinking in a desired cycle.

10.2.1 Control by CUDISP signal

The cursor on/off state and blinking cycle can be controlled by using the CUDISP signal. In this case, data bits 5 and 6 of cursor start raster register (R10) must be set according to Table 10-1 and the CUDISP pin (pin 36) must be directly connected with the MD12 pin (pin 13).

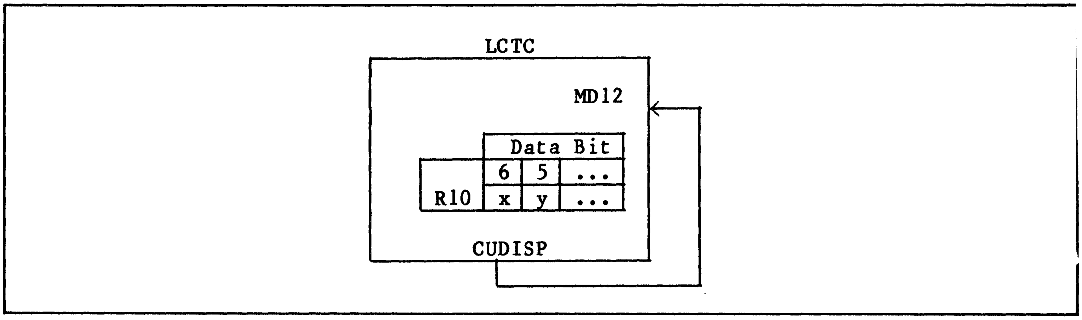


Figure 10-2 Cursor On/Off and Blinking Control by CUDISP

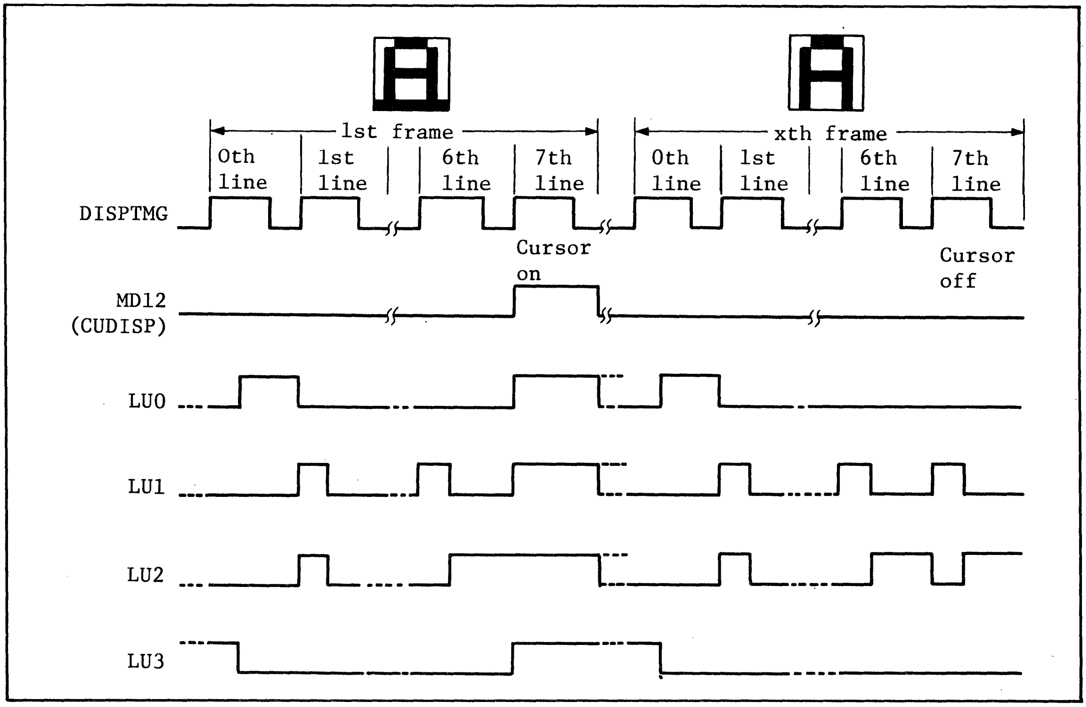


Figure 10-3 Cursor Blinking Timing

Table 10-1 Cursor Control by (R10)

R10		Cursor State
Data Bit 6	Data Bit 5	
0	0	Cursor on; without blinking
0	1	Cursor off
1	0	Cursor blinks every 32 frames
1	1	Cursor blinks every 64 frames

10.2.2 Control by external signal (Optional blinking)

This method is used to blink a cursor at any rate other than a blinking cycle specified by the cursor start raster register (R10).

In this case, data bits 5 and 6 of (R10) are set to low (cursor on, no blinking). An additional circuit shown in Figure 8-4 is necessary to generate an AND signal of an external input signal and the CUDISP signal. The result is input into the MD12 pin (pin 13).

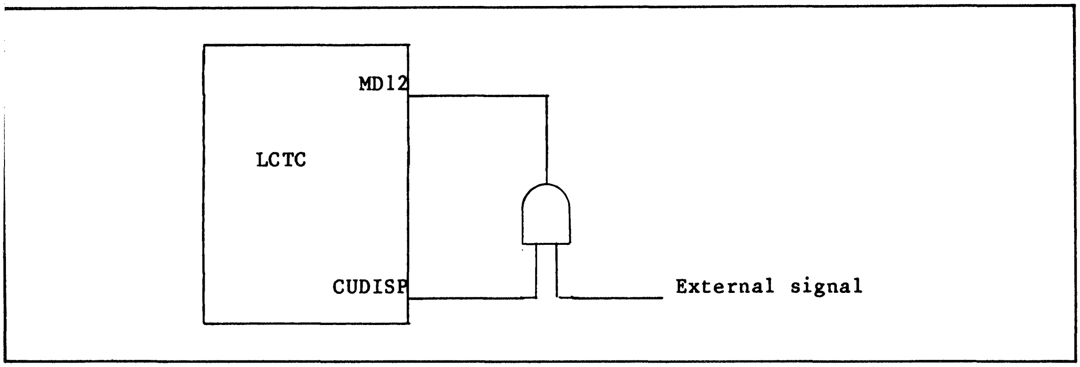
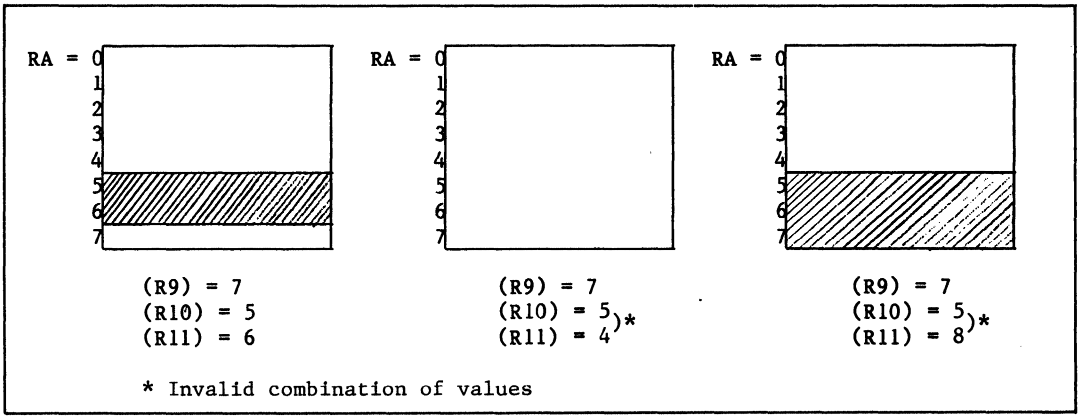


Figure 10-4 Blinking Control Circuit by External Signal

10.3 Cursor Shape

Cursor shape is determined by the cursor start/end raster register (R10; data bits 0-4)/(R11). (R10) specifies the raster number of a given cursor address where the cursor begins from the top. (R11) specifies the raster number where a cursor begins from the bottom. These two specifications determine the display position and shape of the cursor. However, if (R11) is set larger than the maximum raster address register (R9), the cursor shape is determined by (R9) and (R10). The LCTC makes such a setting invalid.



* Invalid combination of values

Figure 10-5 Cursor Shape Specified by (R9), (R10), and (R11)

11. PROGRAMMING METHODS

11.1 Read and Write of Internal Registers

The LCTC provides 14 internal registers and an address register to specify these registers, as listed in Table 4-1. The following operations are required to read or write internal registers:

STEP1: Write internal register address to the address register with a store instruction

STEP2: Read the internal register specified by the address register with a load instruction, or write data to the specified register with a store instruction

Figure 11-1 shows the process flow for reading/writing internal registers, and Figure 11-2 shows corresponding assembler language routines.

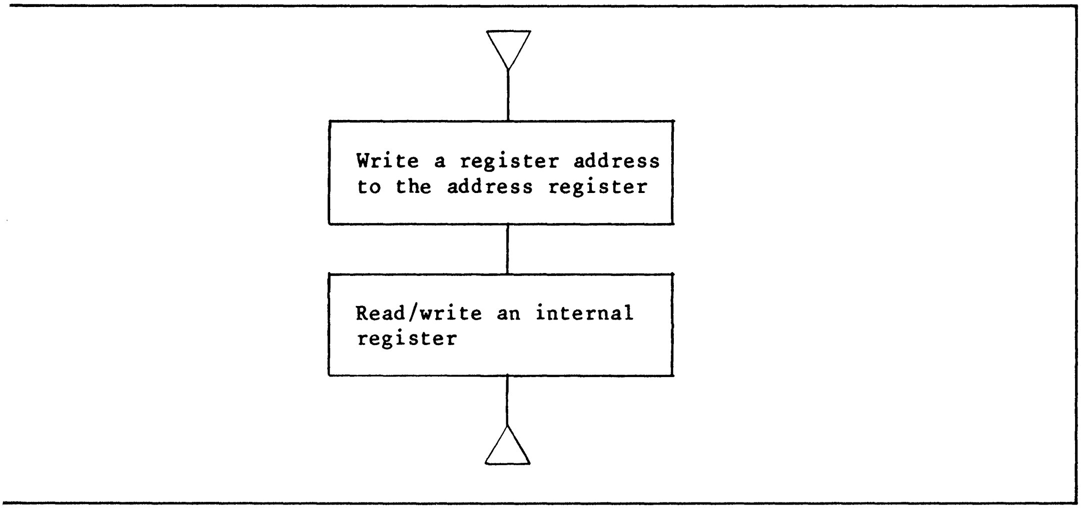

Write a register address to the address register
Read/write an internal register

Figure 11-1 Flowchart for Reading/Writing Internal Registers

```
LDA A  #15         register address ⟶ ACC      )
STA A  ADDR        ACC ⟶ address register      }   read
LDA A  ADDR + 1    cursor(L) ⟶ ACC             )
  -
LDA A  #15         register address ⟶ ACC      )
STA A  ADDR        ACC ⟶ address register      }   write
LDA A  DATA        data ⟶ ACC                  |
STA A  ADDR + 1    ACC ⟶ cursor(L)             )
  -
```

Figure 11-2 Example of Routines for Read/Write of Internal Registers

11.2 LCTC Initialization Programming

In order to enable LCTC display control functions, the user must first after power-on initialize internal registers. Without such initializing, the LCTC cannot operate correctly.

Figure 11-3 gives a flowchart for initializing LCTC registers, and Figure 11-4 shows an example of an initial program. In this case, initial data is stored in table format in register number order to set up a loop, resulting in a compact routine. Although the LCTC does not provide register Nos. 2-8 and 16-17, there is no problem if such registers are accessed.

Table 11-1 and Table 11-2 show 640 x 400 dots LCD specifications in character display and initial value of each internal register respectively. Table 11-3 and Table 11-4 show 640 x 200 dots LCD specifications in graphic display and initial register values. In this case, display page is initially 0 and cursor is in home position, so both start address and cursor address are set to 0. Note that, if the cursor address is other than an effective memory address, cursor display position is not guaranteed.

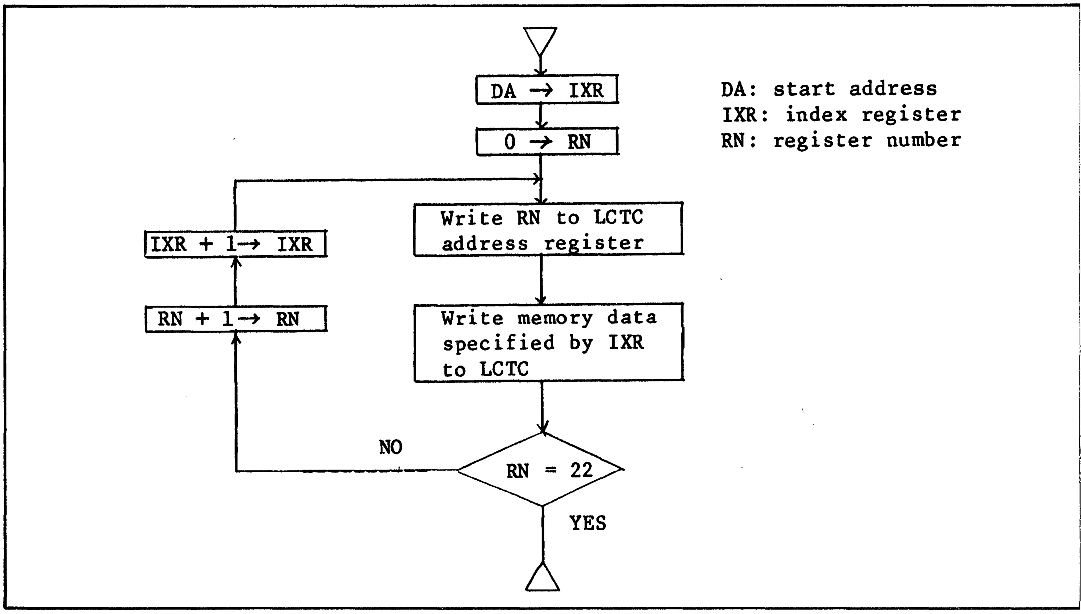


Figure 11-3 Flowchart for LCTC Initializing

```
        LDX       #DA      DA → IXR
        CLR A              0 → ACCA
ILR1    STA A     ADDR     ACCA → address register
        LDA B     0, X     DA → ACCB
        STA B     ADDR+1   ACCB → Data register
        CMP A     #22
        BEQ       ILR2     BRANCH IF ACCA = 22
        INC       A        ACCA + 1  → ACCA
        INX                XR + 1 → XR
        BRA       ILR1     BRANCH TO ILR1
ILR2    -
        -
```

Figure 11-4 LCTC Initial Program

Table 11-1 LCD Specifications (Character Display)

Item	Specification
Horizontal dots	640 dots
Vertical dots	400 dots
Multiplexing duty	1/200 duty
Character dots	8 x 8 dots (character font 5 x 7)
Displayed characters	80 characters x 50 rows
Cursor display	raster 0-7, blinking every 32 frames
Horizontal virtual screen width	80 characters (no horizontal scrolling)

Table 11-2 LCTC Initial Values (Mode 1)

Reg. No.	Register	Symbol	Hexadecimal initial value (decimal)
R0	Horizontal total characters	Nht	59 (89)
R1	Horizontal displayed characters	Nhd	50 (80)
R9	Maximum raster address	Nr	07 (7)
R10	Cursor start raster	Ncs	40
R11	Cursor end raster	Nce	07 (7)
R12	Start address (H)	-	00 (0)
R13	Start address (L)	-	00 (0)
R14	Cursor address (H)	-	00 (0)
R15	Cursor address (L)	-	00 (0)
R18	Horizontal virtual screen width	Nir	50 (80)
R19	Multiplexing duty (H)	Ndh	00 (0)
R20	Multiplexing duty (L)	Ndl	C7 (199)
R21	Display start raster	Nsr	00 (0)
R22	Mode register	-	00

Table 11-3 LCD Specifications (Graphic Display)

Item	Specification
Horizontal dots	640 dots
Vertical dots	200 dots
Multiplexing duty	1/200 duty
Character dots	16 x 1 dots (graphic)
Displayed characters	40 characters (640 dots) x 200 dots
Cursor display	—
Horizontal virtual screen width	80 characters (with horizontal scrolling)

Table 11-4 LCTC Initial Values (Mode 7)

Reg. No.	Register	Symbol	Hexadecimal initial value (decimal)
R0	Horizontal total characters	Nht	2C (44)
R1	Horizontal displayed characters	Nhd	28 (40)
R9	Maximum raster address	Nr	—
R10	Cursor start raster	Ncs	—
R11	Cursor end raster	Nce	—
R12	Start address (H)	-	00 (0)
R13	Start address (L)	-	00 (0)
R14	Cursor address (H)	-	—
R15	Cursor address (L)	-	—
R18	Horizontal virtual screen width	Nir	50 (80)
R19	Multiplexing duty (H)	Ndh	00 (0)
R20	Multiplexing duty (L)	Ndl	63 (99)
R21	Display start raster	Nsr	—
R22	Mode register	-	09

(note) —: optional value

In order to prevent display errors, it is required that MODE pin (pin 52) = V_{CC} and ON/$\overline{\text{OFF}}$ pin = GND at power-on, after which MODE pin should be set to GND just before initialization. This prevention initializes the multiplexing duty ratio register and the mode register, and switches off the LCD. When writing of display data to the frame buffer is completed after initializing, bit 4 of the mode register should be set to 1, and then the LCD is on. This procedure prevents flickering when writing data.

11.3 Paging Programming

The paging function can select a page by specifying the address of frame buffer data. Figure 11-5 shows the procedure for paging. The desired page is first specified with the page key operation, and the specified page is verified; then the start address of the corresponding frame buffer is set. The cursor address is set at the same start address to place the cursor at home position as a result of paging.

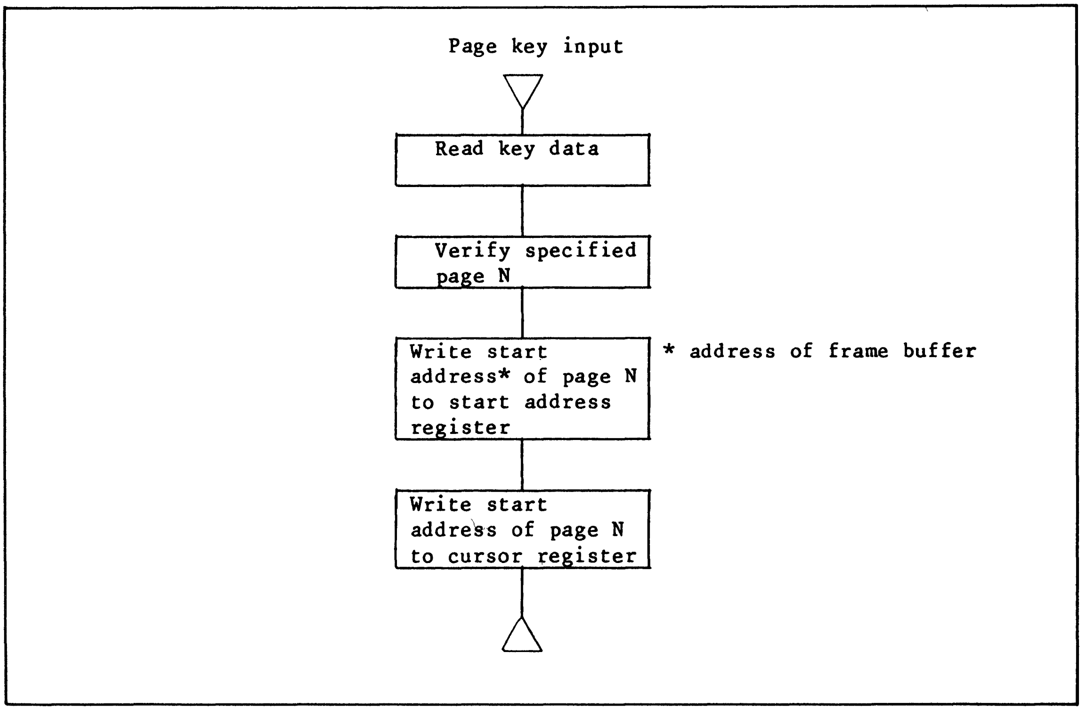

Page key input
Read key data
Verify specified page N
Write start address* of page N to start address register
* address of frame buffer
Write start address of page N to cursor register

Figure 11-5 Flowchart for Paging

11.4 Scrolling Programming

11.4.1 Vertical scrolling by character

Figure 11-6 gives the procedure for vertical scrolling by character. Scrolling up/down is controlled by a scroll key. If start address of the current page is the same as the start address of last page, scrolling up is ignored. If start address of the current page is the same as the start row of the start page, scrolling down hereafter is ignored.

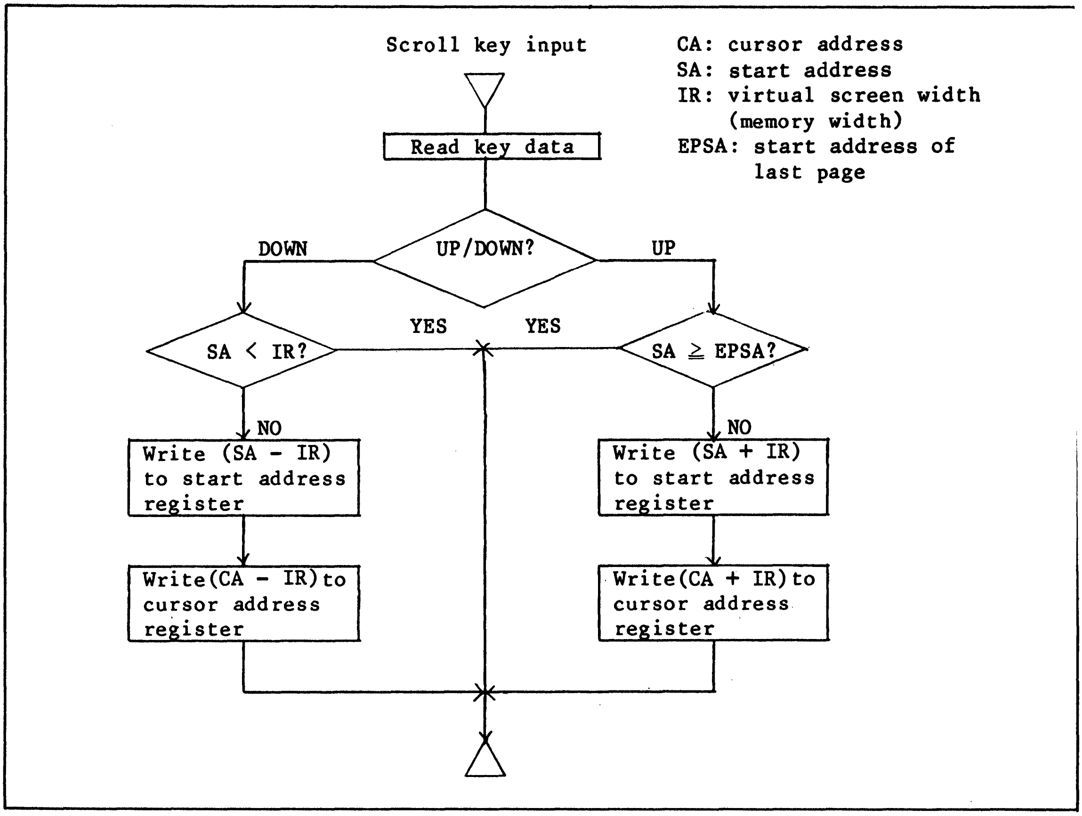

Scroll key input
CA: cursor address
SA: start address
IR: virtual screen width (memory width)
EPSA: start address of last page
Read key data
UP/DOWN?
DOWN
UP
SA < IR?
SA ≧ EPSA?
YES
YES
NO
NO
Write (SA - IR) to start address register
Write (SA + IR) to start address register
Write(CA - IR)to cursor address register
Write(CA + IR)to cursor address register

Figure 11-6 Flowchart for Vertical Scrolling by Character

11.4.2 Smooth scrolling

Figure 11-7 shows the procedure for smooth scrolling. Smooth scrolling is controlled by a scroll command. Scrolling up is caused by writing the result of incrementing the start raster to the start raster register. If the start raster is the same as the maximum number of rasters, scrolling up is performed by writing 0 to the register and writing (SA + IR) to the start address register. Scrolling down is caused by writing the result of decrementing the start raster to the start raster register. If start raster is 0, scrolling down is performed by writing the maximum number of rasters to the registers and writing (SA - IR) to the start address register.

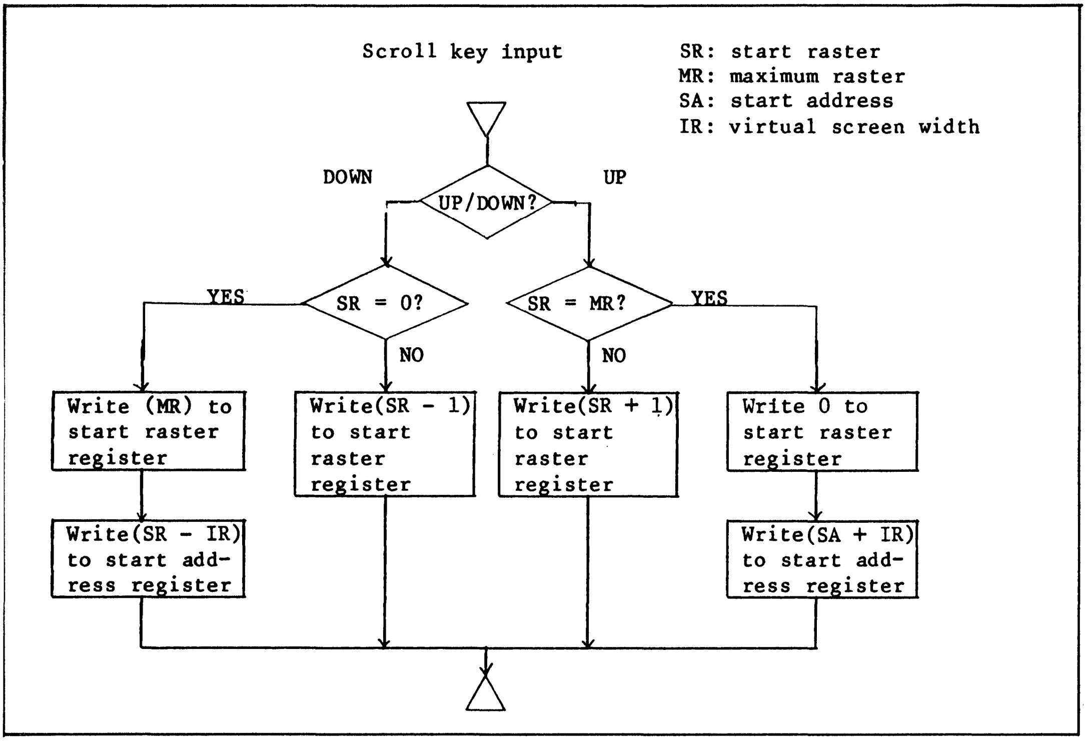

Scroll key input
SR: start raster
MR: maximum raster
SA: start address
IR: virtual screen width
DOWN
UP
UP/DOWN?
YES
SR = 0?
SR = MR?
YES
NO
NO
Write (MR) to start raster register
Write(SR - 1) to start raster register
Write(SR + 1) to start raster register
Write 0 to start raster register
Write(SR - IR) to start address register
Write(SA + IR) to start address register

Figure 11-7 Flowchart for Smooth Scrolling

11.4.3 Horizontal scrolling

Horizontal scrolling, in which virtual screen width is set larger than the number of horizontal displayed characters, is realized by controlling the start address. Figure 11-8 shows the procedure for horizontal scrolling. In this case, horizontal scroll key specifies left/right scrolling. If last address of the start row on the display is the same as the last address of memory width, left scrolling is ignored. If the start address is the same as the start address of the display page, right scrolling is ignored. Figure 11-9 gives the relation between memory width and display.

The user can specify various scrolling directions by a combination of horizontal scrolling and vertical scrolling by character.

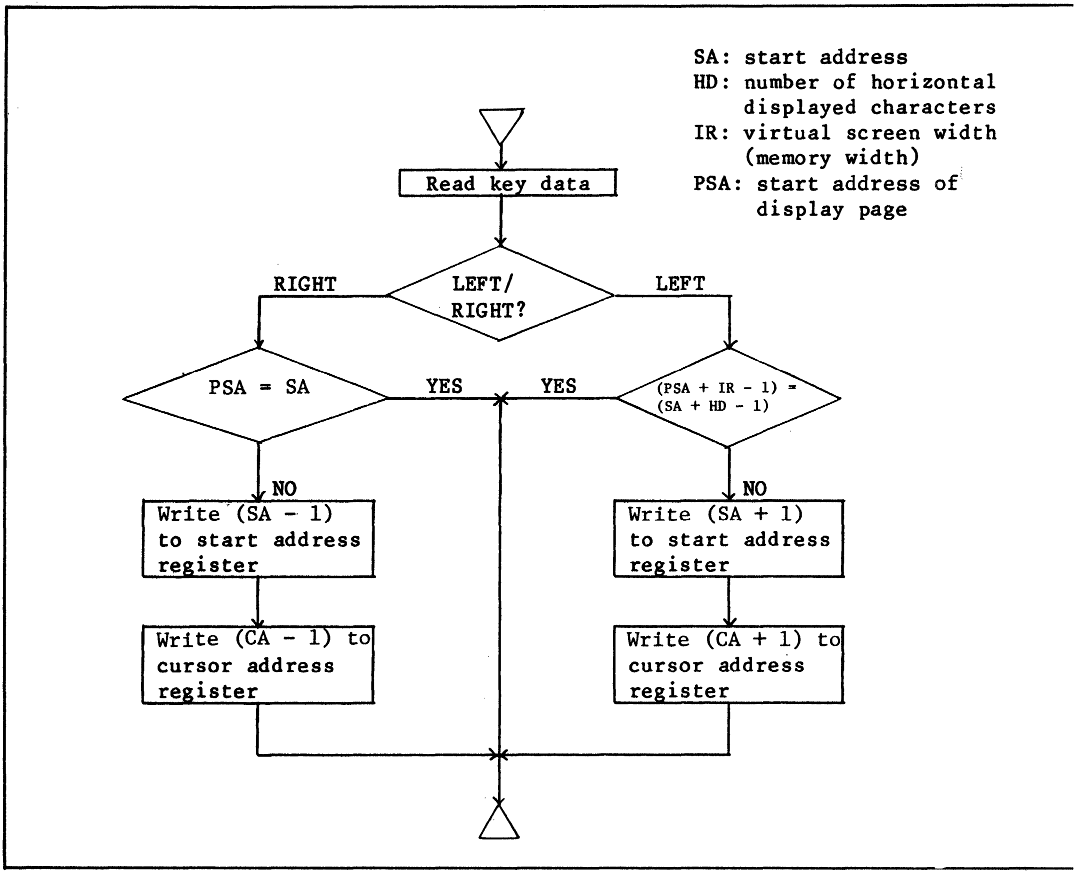

SA: start address
HD: number of horizontal displayed characters
IR: virtual screen width (memory width)
PSA: start address of display page
Read key data
LEFT/ RIGHT?
RIGHT
LEFT
PSA = SA
YES
YES
(PSA + IR - 1) = (SA + HD - 1)
NO
NO
Write (SA - 1) to start address register
Write (SA + 1) to start address register
Write (CA - 1) to cursor address register
Write (CA + 1) to cursor address register

Figure 11-8 Flowchart for Horizontal Scrolling

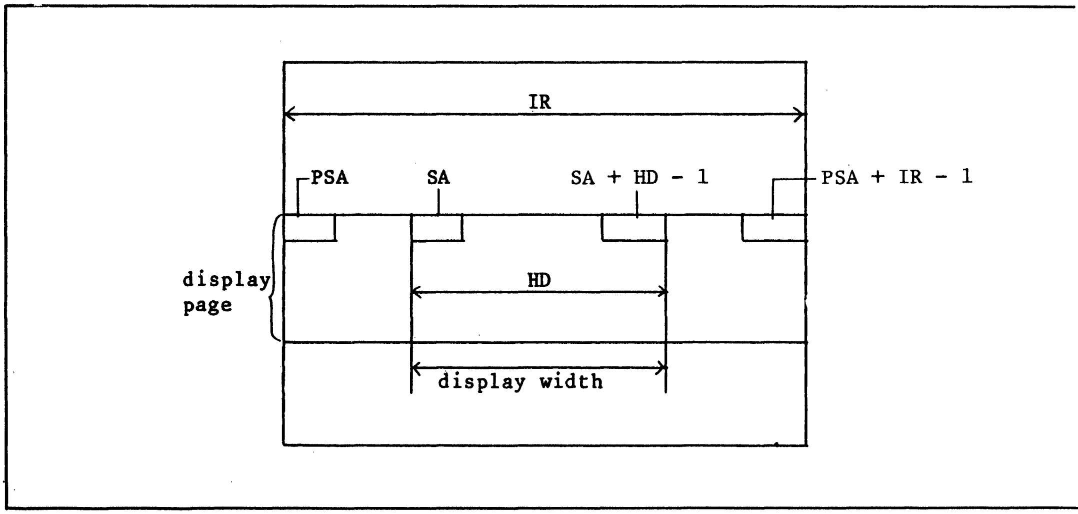


Figure 11-9 Relation Between Memory Width and Display

11.5 Cursor Control Programming

The cursor is commonly used as a pointer specifying data input position on the display. It can be placed at any position on the display and under control of cursor keys. The cursor keys are:

$\boxed{\rightarrow}$: Moves cursor right
$\boxed{\leftarrow}$: Moves cursor left
$\boxed{\downarrow}$: Moves cursor down
$\boxed{\uparrow}$: Moves cursor up
$\boxed{\text{HM}}$: Moves cursor to home position

Figure 11-10 gives an example of moving cursor right and down. When the cursor is placed at the right end of the display, key moves the cursor to the left end of the next row. When the cursor is placed at the right end of last row, key moves the cursor to the home position. And when the cursor is placed on the last row, key moves cursor to the same column of the first row. In Figure 11-10, virtual screen width (memory width) is the same as the number of horizontal displayed characters.

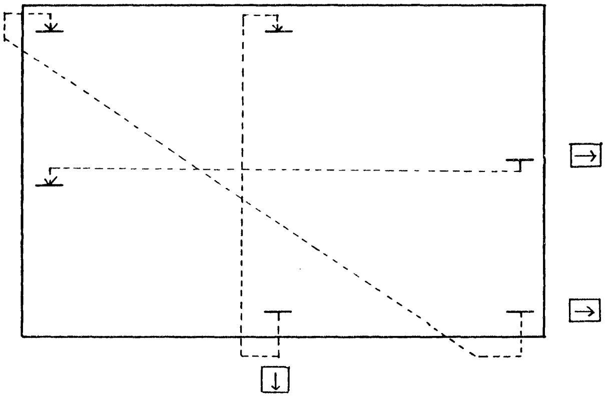


Figure 11-10 Cursor Control

Figure 11-11 and Figure 11-12 show flowcharts for control of cursor moving right and moving down, respectively.

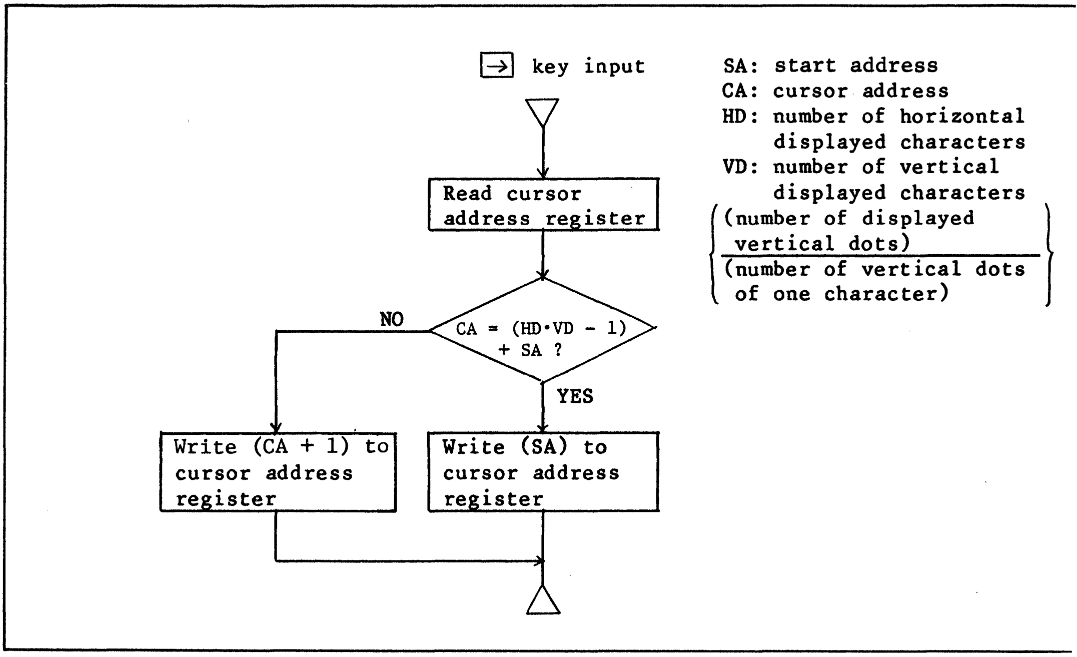

→ key input
Read cursor address register
CA = (HD•VD – 1) + SA ?
NO
YES
Write (CA + 1) to cursor address register
Write (SA) to cursor address register
SA: start address
CA: cursor address
HD: number of horizontal displayed characters
VD: number of vertical displayed characters
(number of displayed vertical dots) / (number of vertical dots of one character)

Figure 11-11 Flowchart for Moving Cursor Right

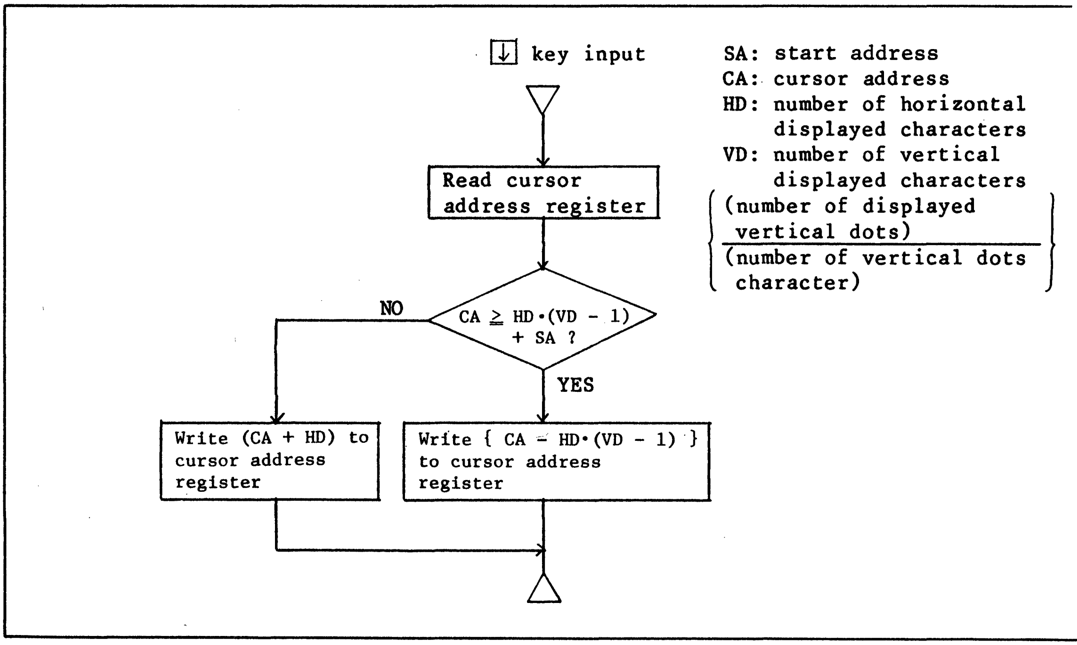

↓ key input
Read cursor address register
CA ≥ HD•(VD – 1) + SA ?
NO
YES
Write (CA + HD) to cursor address register
Write { CA – HD•(VD – 1) } to cursor address register
SA: start address
CA: cursor address
HD: number of horizontal displayed characters
VD: number of vertical displayed characters
(number of displayed vertical dots) / (number of vertical dots character)

Figure 11-12 Flowchart for Moving Cursor Down

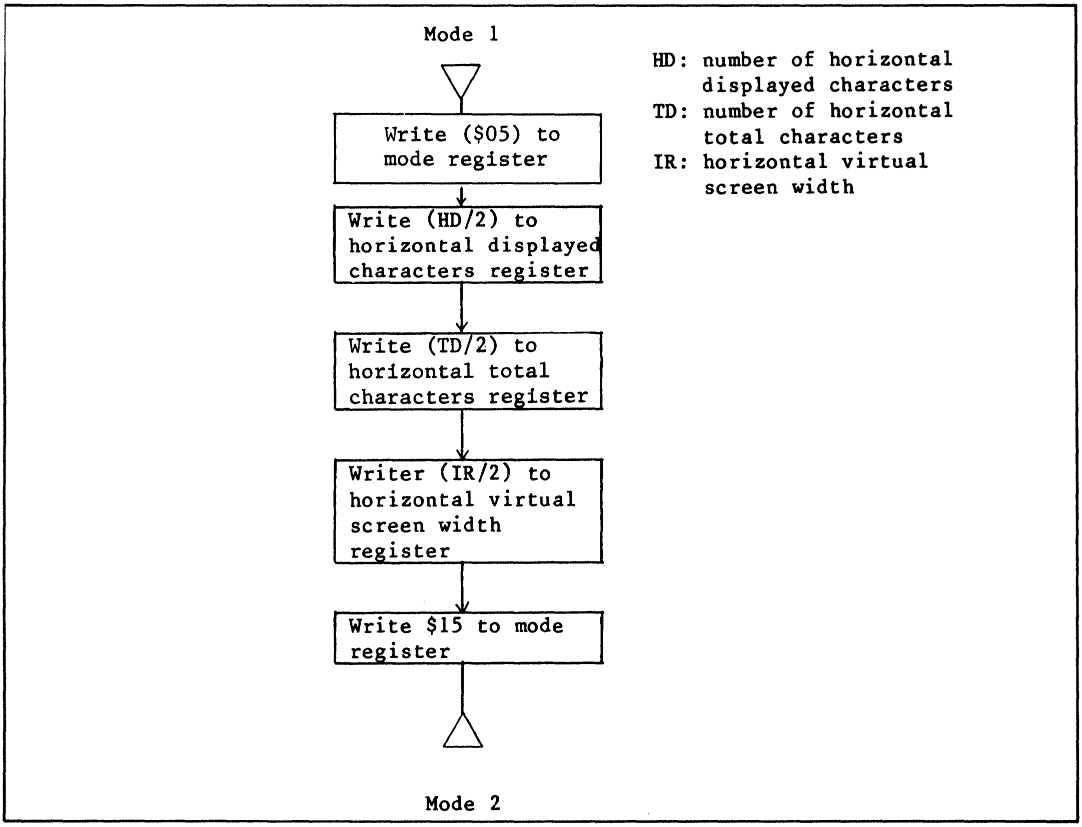
11.6 Mode Control Programming

The display mode can be changed by writing data to the mode register. In this case, it is also required to change parameters dependent on mode.

Figure 11-13 shows the procedure for switching the LCTC from mode 1 (normal character) to mode 2 (wide character). In mode 2, the number of character dots (16 horizontal dots) is twice that in mode 1, and the number of horizontal displayed characters as well as total horizontal characters and horizontal virtual screen width in mode 2 become half of those in mode 1.

Figure 11-14 shows the procedure for switching the LCTC from mode 1 (character display) to mode 3 (graphic 1 display). In mode 3, the number of horizontal dots (16 dots) is twice that in mode 1, and the number of horizontal displayed characters as well as total horizontal characters and horizontal virtual screen width in mode 3 become half of those in mode 1.

The display is off while rewriting display data in order to prevent display errors, and, after completing rewriting, the display is on.


Mode 1
Write ($05) to mode register
Write (HD/2) to horizontal displayed characters register
Write (TD/2) to horizontal total characters register
Writer (IR/2) to horizontal virtual screen width register
Write $15 to mode register
Mode 2

HD: number of horizontal displayed characters
TD: number of horizontal total characters
IR: horizontal virtual screen width

Figure 11-13 Flowchart for Changing from Mode 1 to Mode 2

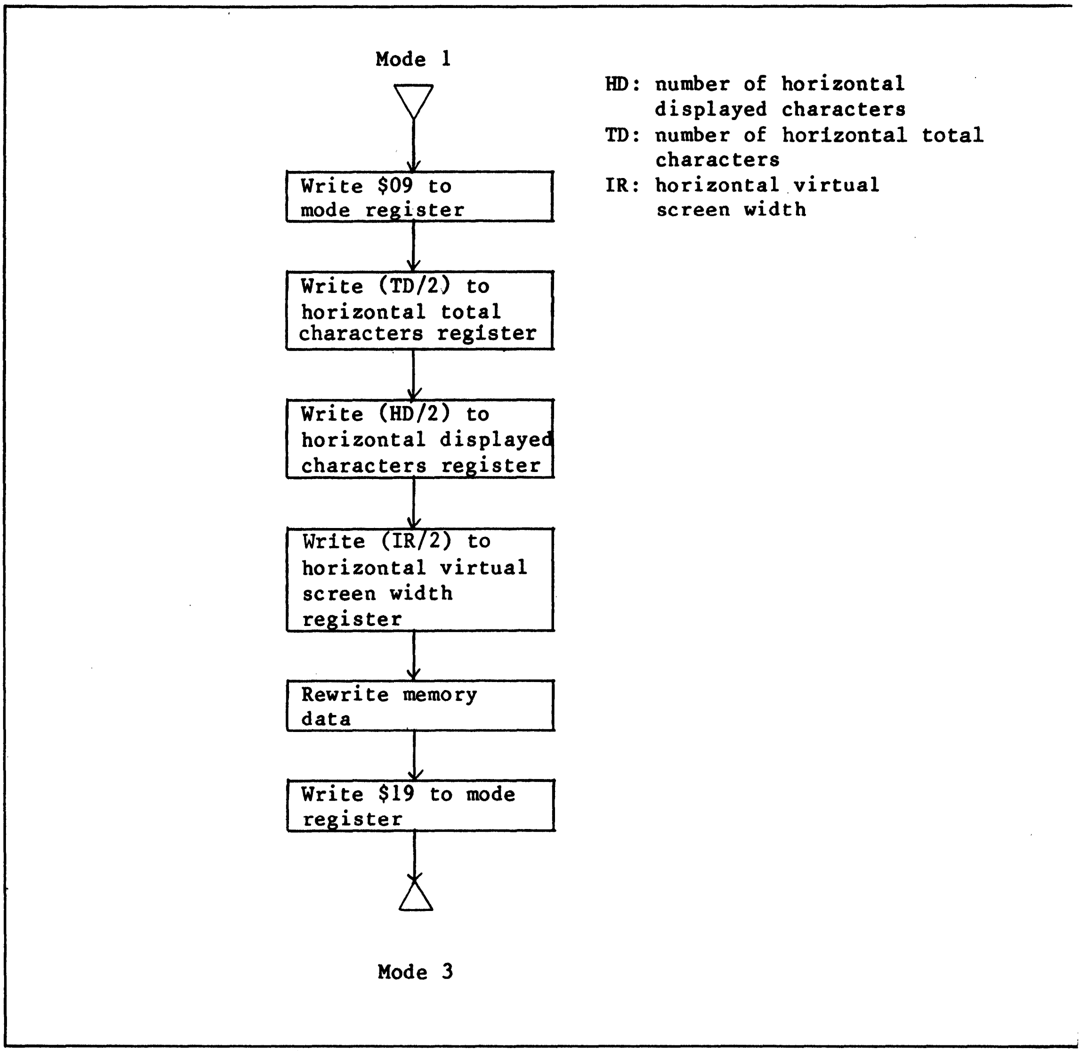

Mode 1
Write $09 to mode register
Write (TD/2) to horizontal total characters register
Write (HD/2) to horizontal displayed characters register
Write (IR/2) to horizontal virtual screen width register
Rewrite memory data
Write $19 to mode register
Mode 3
HD: number of horizontal displayed characters
TD: number of horizontal total characters
IR: horizontal virtual screen width

Figure 11-14 Flowchart for Changing from Mode 1 to Mode 3

2. DISPLAY METHODS AND SYSTEM CONFIGURATION

2.1 LCTC Display Methods and Features

he LCTC supports the following display methods.

Table 12-1 LCTC Display Methods

Display Method	Unit of Memory Data Access (Bits)	MA Output Form	Rasters per Character Row	Usage
Character mode	8	Repeats in a same character row.	1-32	Character display (graphic display also, when the no. of rasters is 1)
Graphic 1 mode	16	Increases continuously.	-	Graphic display
Graphic 2 mode	16	Repeats in a same character row.	1-32	Graphic display (for graphic software using the CRTC)
OR function	8	Repeats in a same character row.	1-32	Superimposition of characters and graphics

e; For the terms, refer to each mode explanation.

2.2 Character Mode

2.2.1 Character display description

igure 12-1 shows how the character display method works. It is necessary to can and refresh the LCD screen constantly so as to keep characters displayed on he LCD screen. Therefore the LCD system usually stores display data in a emory and refreshes the screen according to the data. Here we call the memory toring the data for displaying a "frame buffer."

here are two methods of writing data into a frame buffer from the MPU. One is bitmap method and the other is a character display method. The former irectly displays the data in a frame buffer. The latter uses character codes uch as ASCII in a frame buffer, and displays character patterns converted from haracter codes by a character generator. Figure 12-2 shows how character codes re converted into character patterns. A character generator is a ROM generating character patterns, using character codes and the scanning rasters as ddresses.

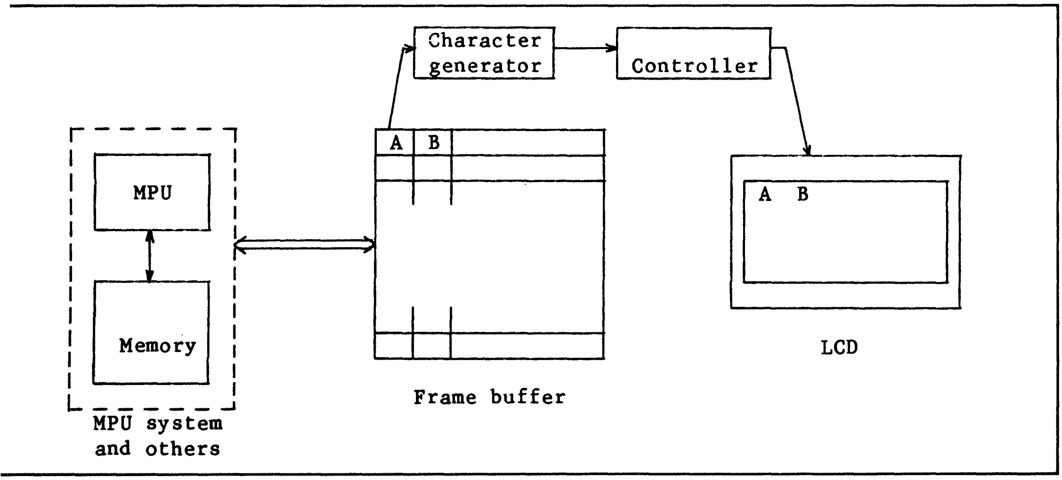


Figure 12-1 How the Character Display Method Works

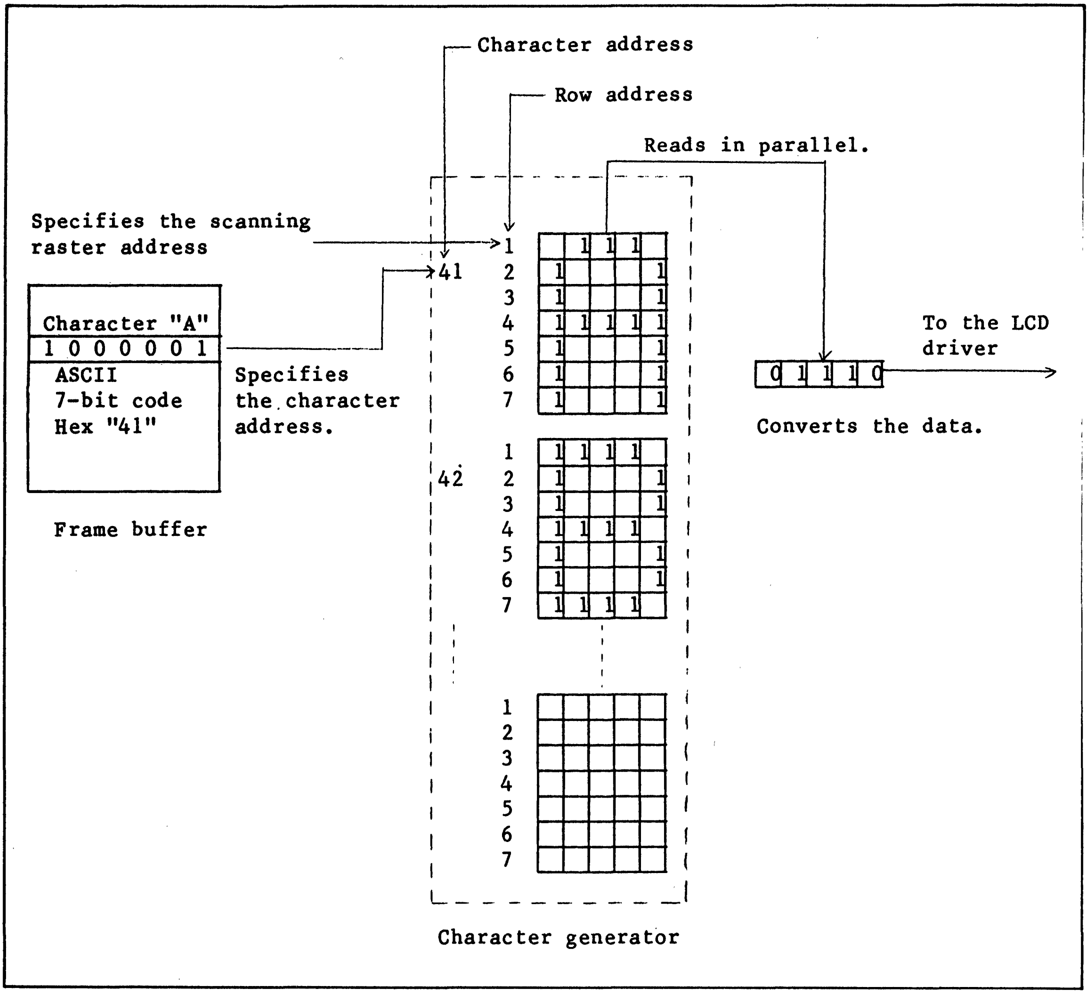


Figure 12-2 How the Character Patterns are Generated

The merit of this method is that even a small-capacity frame buffer can store plenty of character patterns because they are condensed to be character codes. However, it cannot display the characters or graphics not contained in a character generator. Thus this method is suitable for displaying only characters.

12.2.2 System configuration and memory address output

Figure 12-3 shows an example of the system configuration in the character mode. The display system is usually constructed with a character generator (C.G.ROM) and a frame buffer with ARAM and VRAM. In constructing the LCD system, no external parts are required since the LCTC can be connected directly with the LCD module. However, when the load capacitance of the LCTC exceeds the rating, noise will be produced and it may cause malfunction.

The LCTC offers the function of specifying the character attributes by character unit, such as reverse video and blink. To realize this function, the frame buffer is constructed with two types of RAM's; one stores character codes (= VRAM), and the other stores attribute codes (= ARAM). ARAM is unnecessary in case of not using the attribute function. It is possible to construct one-RAM character display system without the attribute function by setting MD_8-MD_{11}, and MD_{13}-MD_{15} low and inputting CUDISP to MD_{12}.

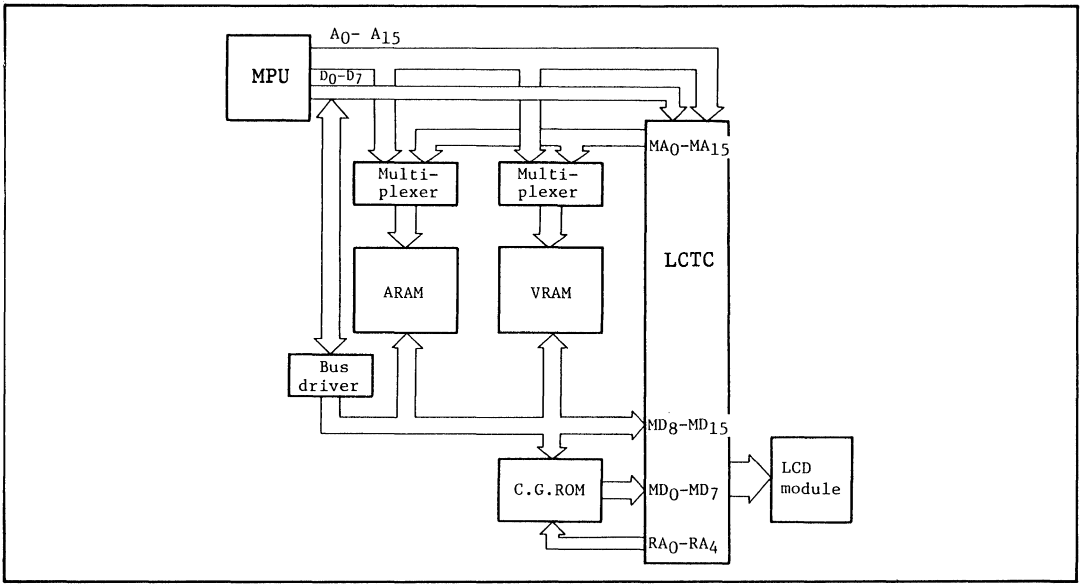


Figure 12-3 System Configuration Example in the Character Mode

As explained before, in the character mode, it is necessary to apply the same character addresses to the character generator as many times as the number of rasters constructing a character row (= set value in the maximum raster address register (R9) + 1).

Therefore the MA pins output the same addresses to the frame buffer as many times as the number of rasters constructing a character row as shown in Figure 12-4. Thus the outputs change in a saw-wave. The figure shows an examle of the screen with 3 character rows each of which is constructed with 3 rasters.

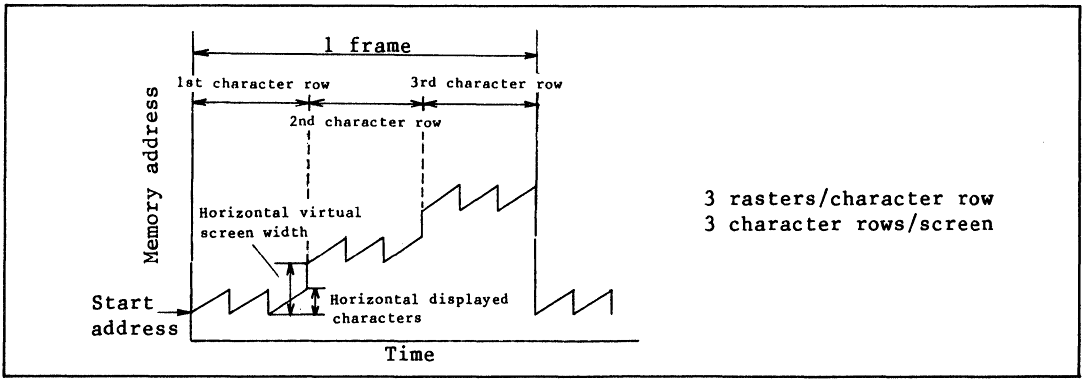


Figure 12-4 MA Outputs in the Character Mode

12.3 Graphic 1 Mode (Bitmap Display)

12.3.1 Bitmap display description

Figure 12-5 shows how the bitmap display method works. This method displays the data in the frame buffer as it is.

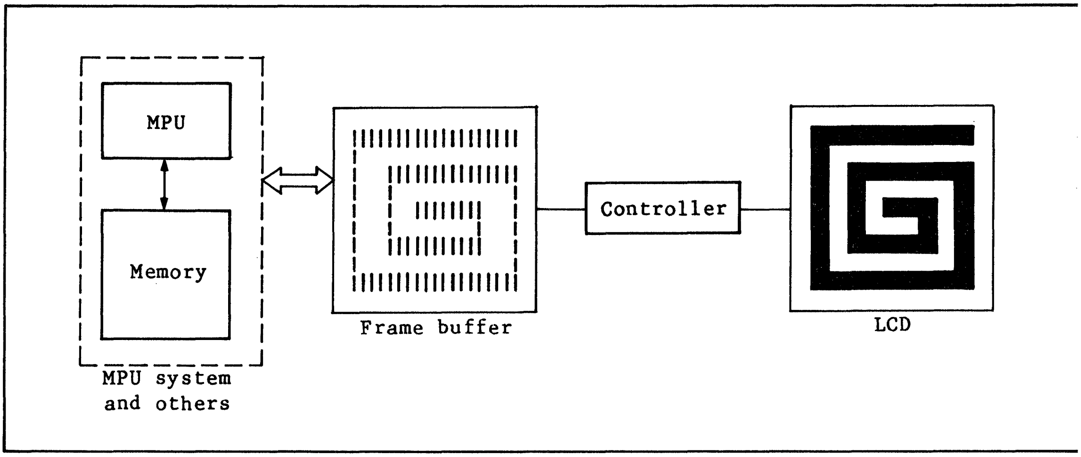


Figure 12-5 How the Bitmap Display Method Works

It requires the frame buffer whose capacity is as large as, or larger than the number of dots of a screen. However, a variety of displays are possible and it is suitable for graphic display since each bit of the frame buffer corresponds to that of the display screen.

Graphic 1 mode displays bitmap data.

12.3.2 System configuration and memory address output

Figure 12-6 shows an example of the system configuration in the graphic 1 mode. The graphic 1 mode of the LCTC displays bitmap data using the system for the character mode with the attribute function without any change. In this case, the data bypasses the C.G.ROM. Thus, the MPU accesses the memory data on 16-bit basis and at least two memories are required.

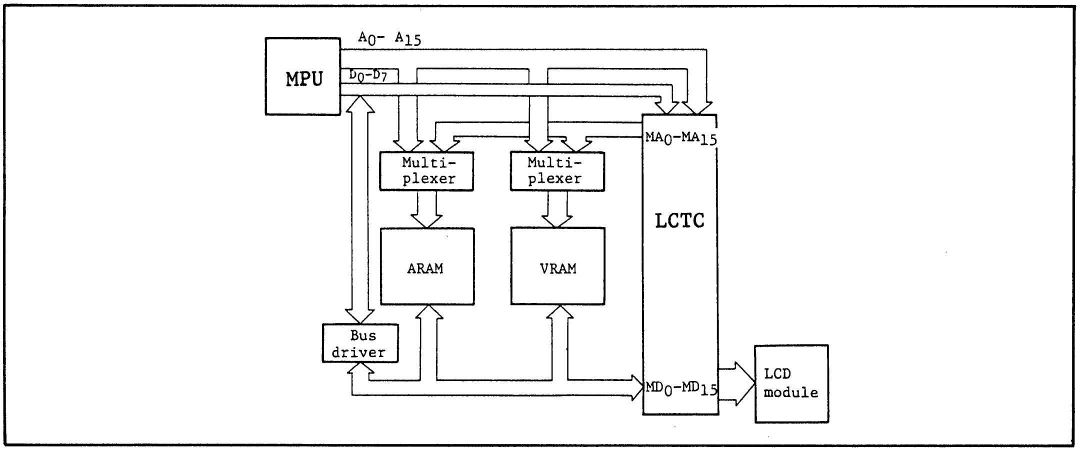


Figure 12-6 System Configuration Example in Graphic 1 Mode

The character mode can be used for bitmap display using only one RAM. For more details, refer to "13.1 1-RAM Graphic."

The MA outputs increase linearly in bitmap display as shown in Figure 12-7 since the data in the frame buffer is displayed as it is on the LCD. The figure shows an example of the screen constructed with 8 rasters.

RA outputs changes also in the graphic 1 mode, but it does not affect MA outputs unlike in the character mode. Thus the set value in the maximum raster address register (R9) is ignored.

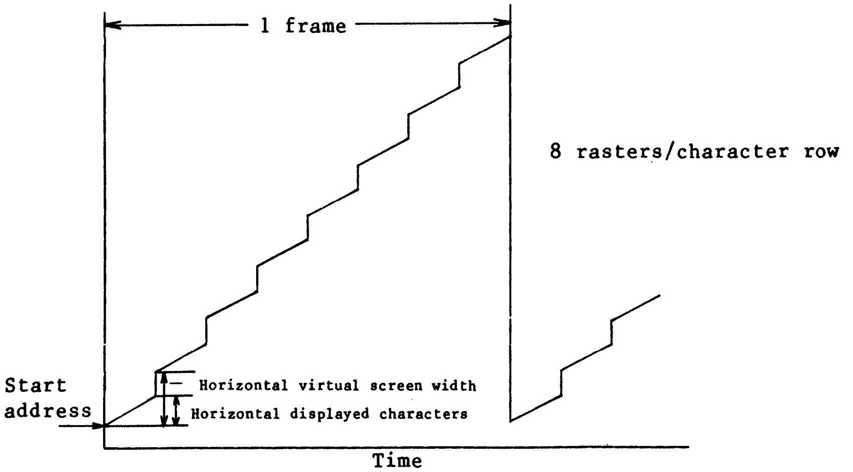


Figure 12-7 MA Outputs in the Graphic 1 Mode

12.4 Graphic 2 Mode

12.4.1 Graphic 2 mode features and usage

(1) Control of graphic software for HD6845 (CRTC)

The graphic mode is used to handle graphic display software requiring the RA output signals for memory address management.

In the LCTC graphic modes (modes 3, 7, 11, and 13), a memory address (MA) output changes continuously as shown in Figure 12-8(1). In the character modes, the character generator ROM is used. So, as shown in Figure 12-8(2), the MA output changes continuously in a raster and this operation is repeated as many times as the number of rasters in a character row.

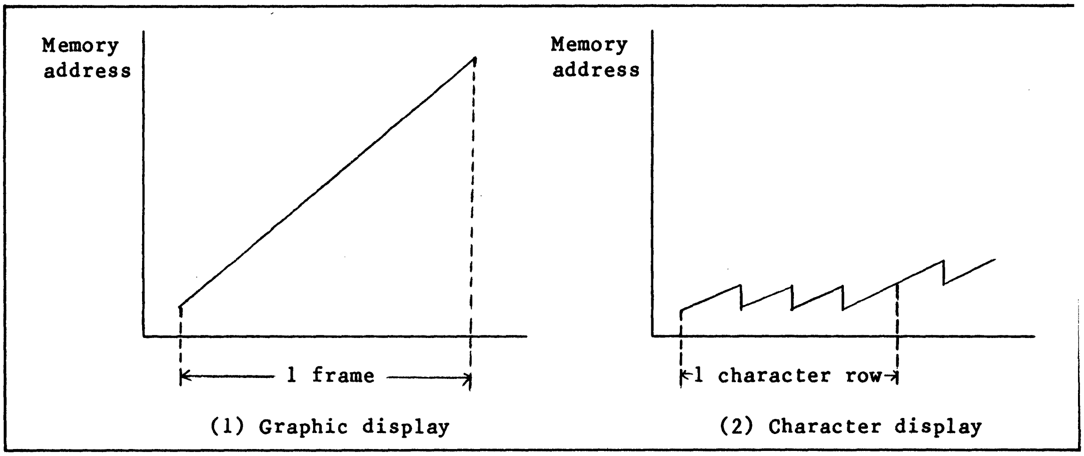


Figure 12-8 Difference in Memory Address Management between Graphic Display and Character Display

However, some graphic software for CRT display using CRTC (HD6845) use raster address (RA) output for address management as shown in Figure 12-9. Such software cannot be controlled in the graphic mode.

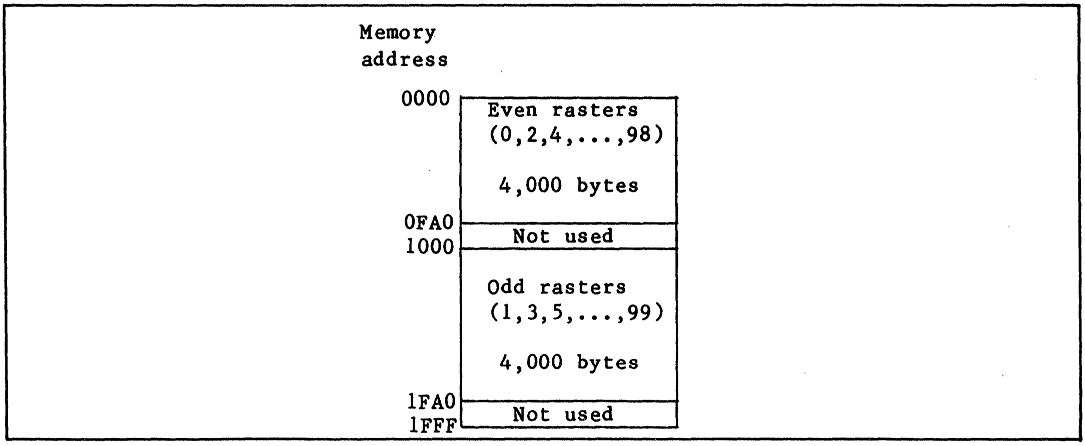


Figure 12-9 Graphic Data Management by Raster Address

In the character mode, this type of software can be controlled. However, if character mode is used to run software which uses character display and graphic display, it causes two problems. The first one is that memory control capacity for graphic display becomes half because MD_8-MD_{15} are only for attribute code. The second one is that many connections of MA output and MD input must be changed in switching character display to graphic display. Therefore a large additional circuit is required.

By using the graphic 2 mode, this type of software can be handled without these problems.

(2) Features of Graphic 2 Mode

The graphic mode has the following features:

(i) 16-bit access

A 16-bit access allows management of 128-kbyte memory. When character display is switched to graphic display, it is unnecessary to change connection of MD pins.

(ii) Same memory address management as character mode

A changeable RA output allows control of graphic display software that requires RA output signals.

12.4.2 System configuration and memory address output

As explained before, the graphic 2 mode is for managing the graphic software run by the system using HD6845 (CRTC). Therefore the basic system configuration of the graphic 2 mode should be able to switch the character mode, which is the basic mode of HD6845, to the graphic 2 mode. Figure 12-10 shows the example.

In the graphic 2 mode, a raster address must be used as a part of memory address in the graphic display. Configure hardware so that an entry into a buffer memory address can be switched from MA output to RA output according to whether it is graphic 2 mode or character mode.

Figure 12-10 shows an example of circuit configuration for controlling the graphic display software shown in Figure 12-9.

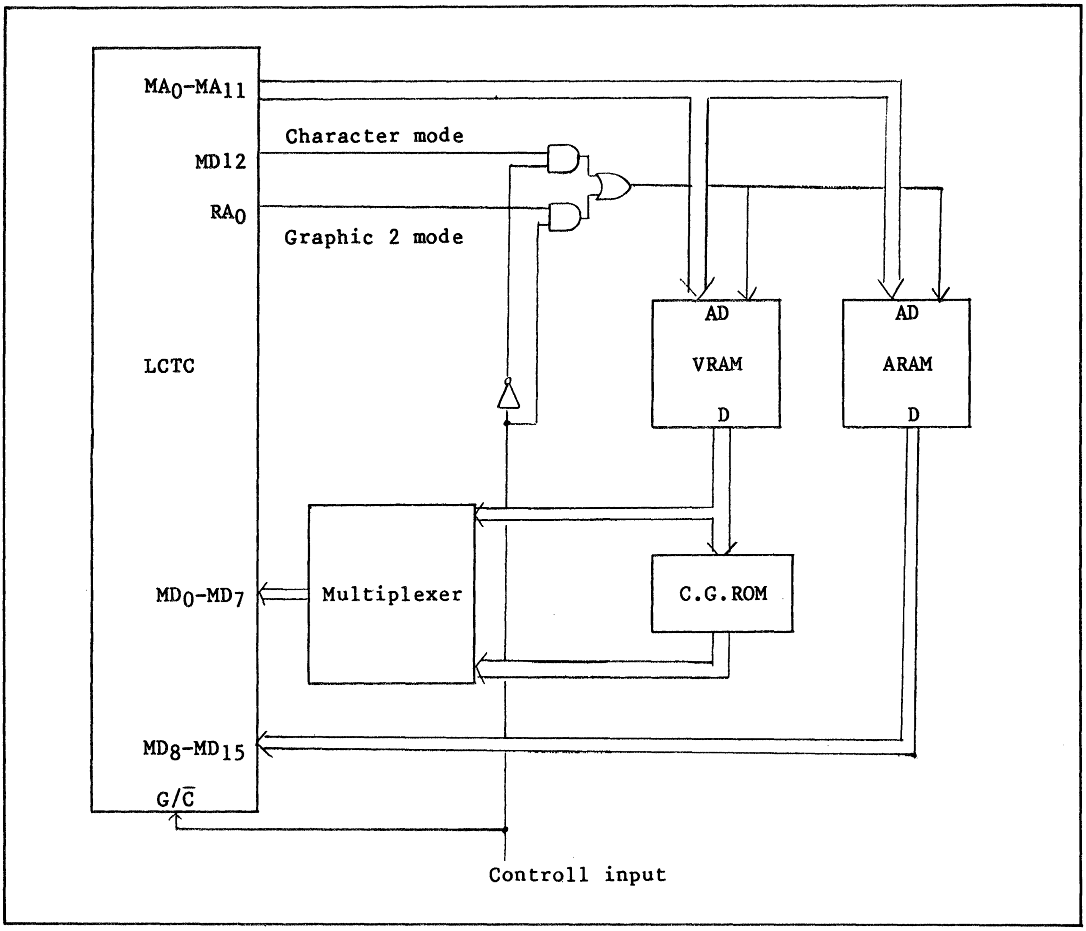


Figure 12-10 System Configuration Example in the Graphic 2 Mode

The MA outputs are exactly the same as those in the character mode. It means that the MA pins output the same addresses as many times as the number set in the maximum raster address register (R9).

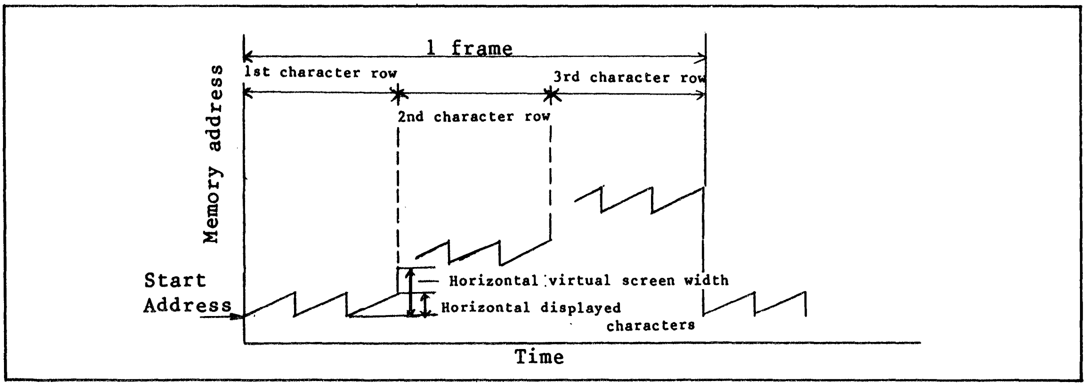


Figure 12-11 MA Outputs in the Graphic 2 Mode

12.5 OR Function

12.5.1 OR function description

The OR function is used to generate the OR of the data entered into MD_0-MD_7 (e.g. character data) and the data entered into MD_8-MD_{15} (e.g. graphic data) in the LCTC and transfer such data as 1-byte data.

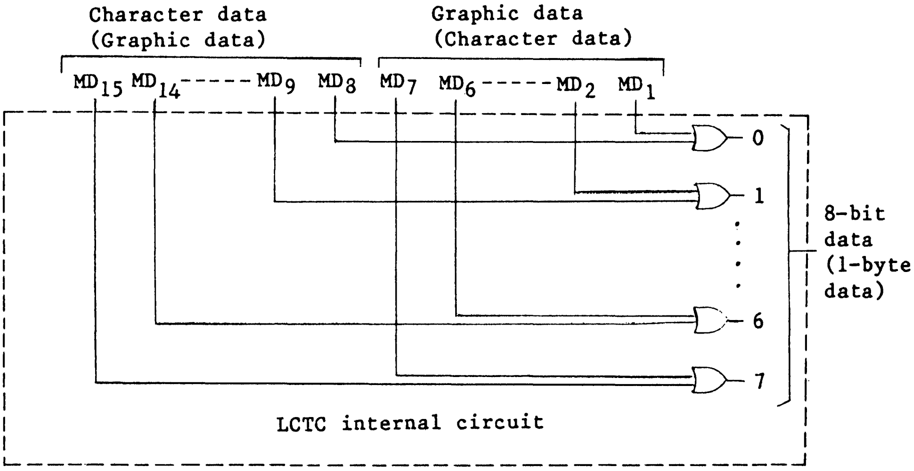


Figure 12-12 OR Function

The OR function is basically one of the functions in the character mode and should be explained in that section. However, it is preferable to explain here because this function requires modification of the external system.

The attribute function is not available when the OR function is used.

12.5.2 Superimposition of character displays

Figure 12-13 shows the system configuration example of the superimposition of character displays.

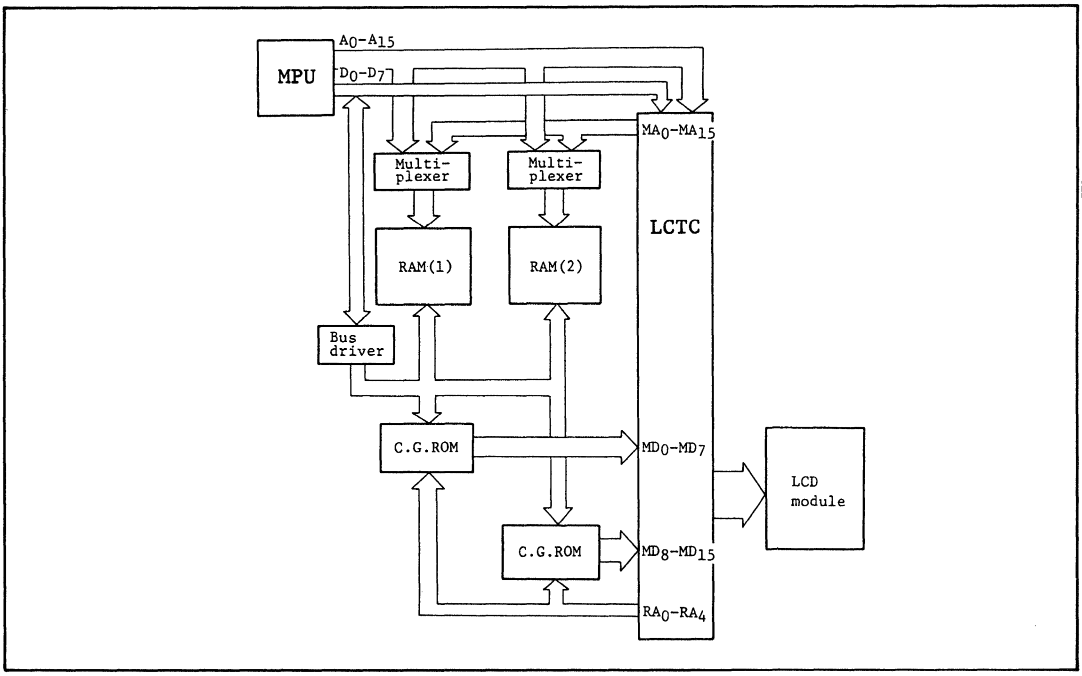


Figure 12-13 System Configuration Example of the Superimposition of Character Displays

Here the 8-bit output data of the C.G.ROM corresponding to the character codes in the RAM(1) and RAM(2) are ORed. Then the ORed 8-bit output data will be displayed. Figure 12-14 shows an example of the superimposition of character displays.

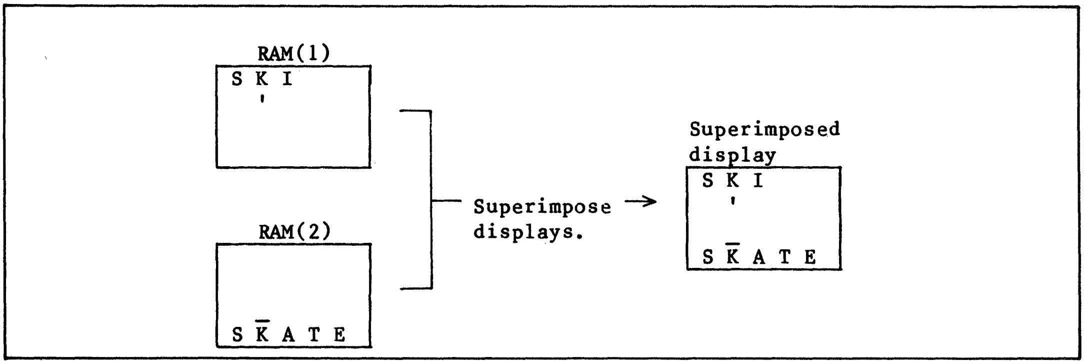


Figure 12-14 Example of the Superimposition of Character Displays

The MA and RA pins output addresses in exactly the same way as in the normal character mode.

12.5.3 Superimposition of graphic displays

Figure 12-15 shows the system configuration example of the superimposition of graphic displays. Set 0 into the maximum raster address register and connect no wire to the RA pins here.

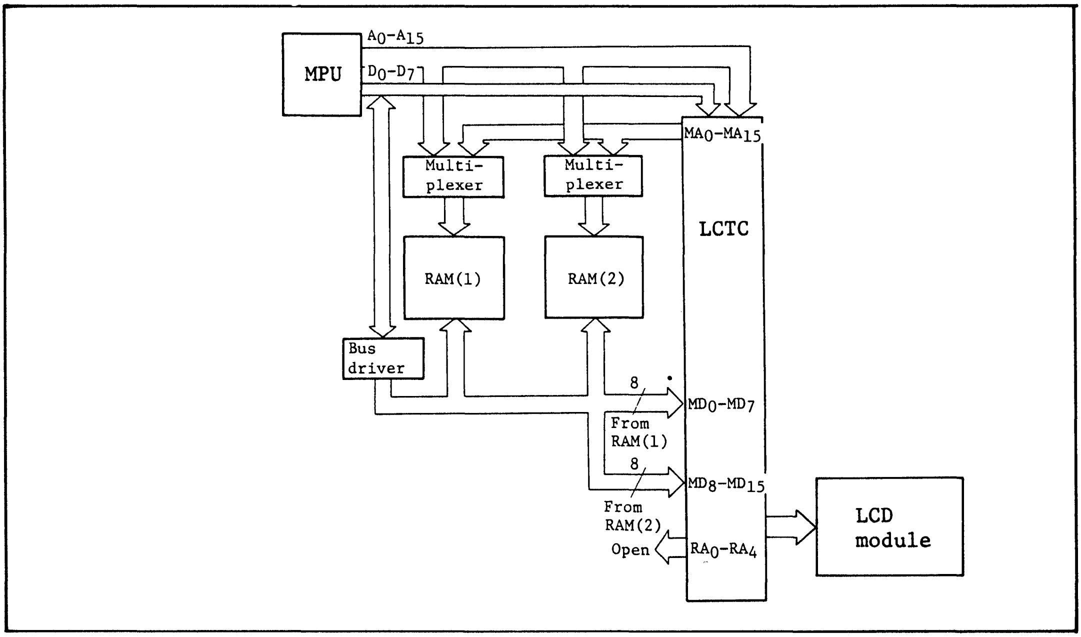


Figure 12-15 System Configuration Example of the Superimposition of Graphic Displays

Here the 8-bit graphic data of the RAM(1) and RAM(2) are ORed. And then the ORed 8-bit output data will be displayed. Figure 12-16 shows an example of the superimposition of graphic displays.

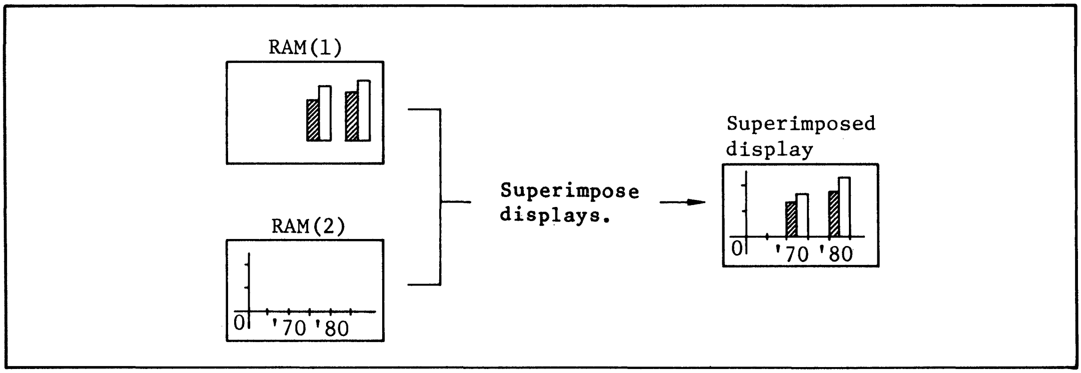


Figure 12-16 Example of the Superimposition of Graphic Displays

The MA pins output addresses in exactly the same way as in the graphic 1 mode (bitmap display).

12.5.4 Superimposition of graphic display and character display

(1) System configuration

The following operations are needed to realize the superimposition of graphics and characters: set the mode of the LCTC for character display, connect MA and RA outputs to the RAM containing graphic data, and supply the addresses increasing linearly. Thus the system configuration is to be one shown in Figure 12-17.

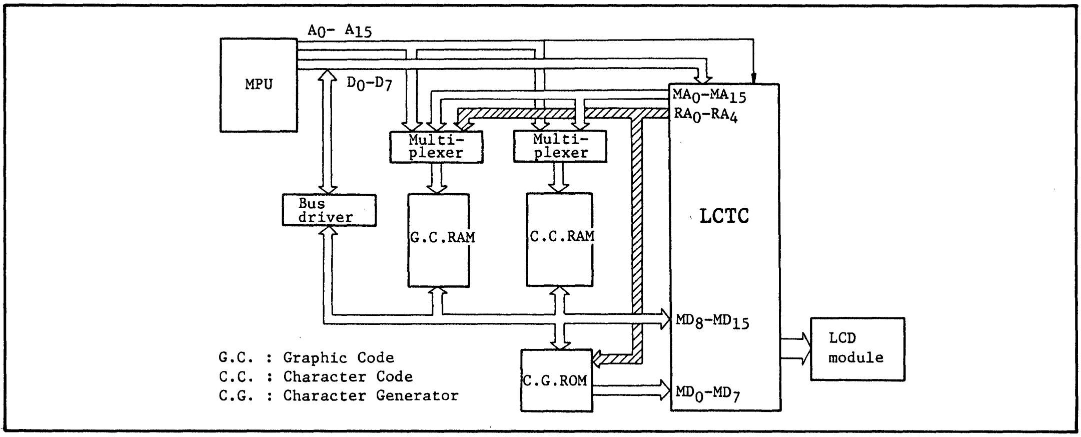


Figure 12-17 System Configuration Example of the Superimposition of Graphic Display and Character Display

(2) Display format and how to connect memory addresses

The LCTC operates in the character display mode when the system is for superimposition of graphics and characters. Thus, the connection to the C.C.RAM addresses should be the same as that of normal character display mode.

The connection to the G.C. RAM is as follows: The address of the data to be displayed on the first raster is the same in both the character display and the graphic display. Thus, the low-order bits of the MA, each of which controls the data for a raster, should be connected to the low-order bits of G.C.RAM addresses. And the RA, each of which controlls the data for a character row, should be connected to the less low-order bits of G.C.RAM addresses. Finally, the rest bits of the MA should be connected to the least low-order bits of G.C.RAM addresses.

Suppose a screen whose number of horizontal dots of a panel is D and whose number of rasters in a character row is R. As one address can specify one byte, j (= the number of low-order bits, each of which controls the data for a raster) can be calculated with the following expressions:

$$(2^3)^j \leqq D < (2^3)^{j+1}$$

$$\therefore 2^{j+3} \leqq D < 2^{j+4}$$

Then connect the RA, each of which controls the data for a character row, to the less low-order bits of G.C.RAM addresses. k (= the number of RA bits) can be calculated with the following expression:

$$2^k \leqq R < 2^{k+1}$$

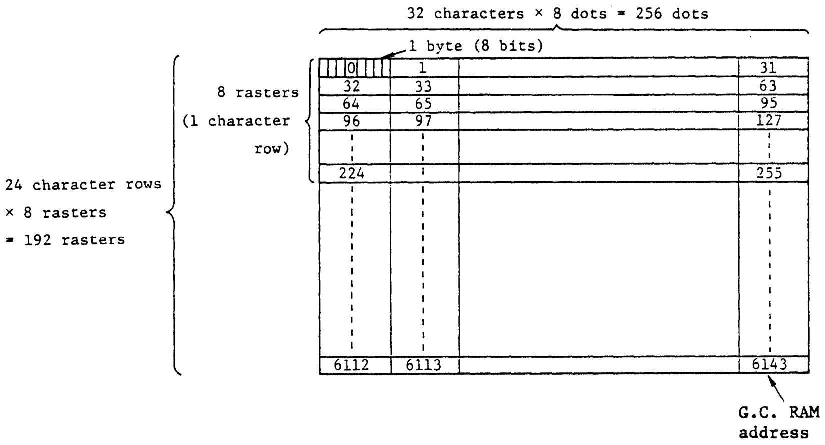
Here, connect the memory addresses as follows;

Graphic RAM Address	Connected to (of the LCTC)
ma_0-$ma_{(j-1)}$	MA_0-$MA_{(j-1)}$
ma_j-$ma_{(j+k-1)}$	RA_0-$RA_{(k-1)}$
$ma_{(j+k)}$-	MA_j-

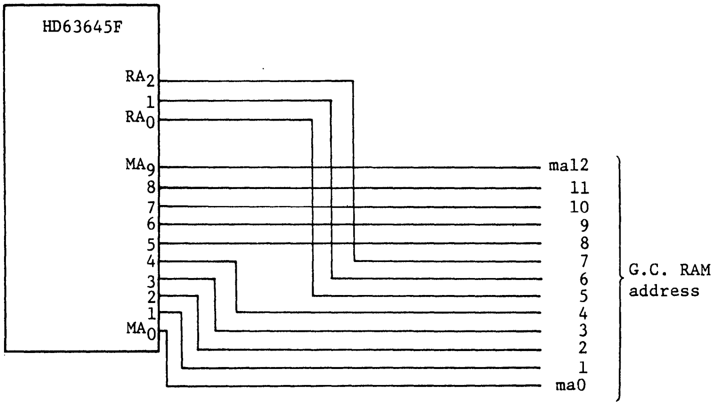
Figure 12-18(i) shows an example of the screen when D = 256 and R = 8.

$$2^5 + 3 \leqq 256 < 2^5 + 4$$
$$2^3 \leqq 8 < 2^3 + 1$$

Thus j is to be 5 and k is to be 3 since they are expressed in the above inequalities. Therefore connect MA_0-MA_4 of the LCTC to memory addresses ma_0-ma_4, RA_0-RA_2 of the LCTC to ma_5-ma_7, and MA_5- of the LCTC to ma_8-. Figure 12-18(ii) shows the connection example.



(i) Example (1) of the Graphic RAM Display



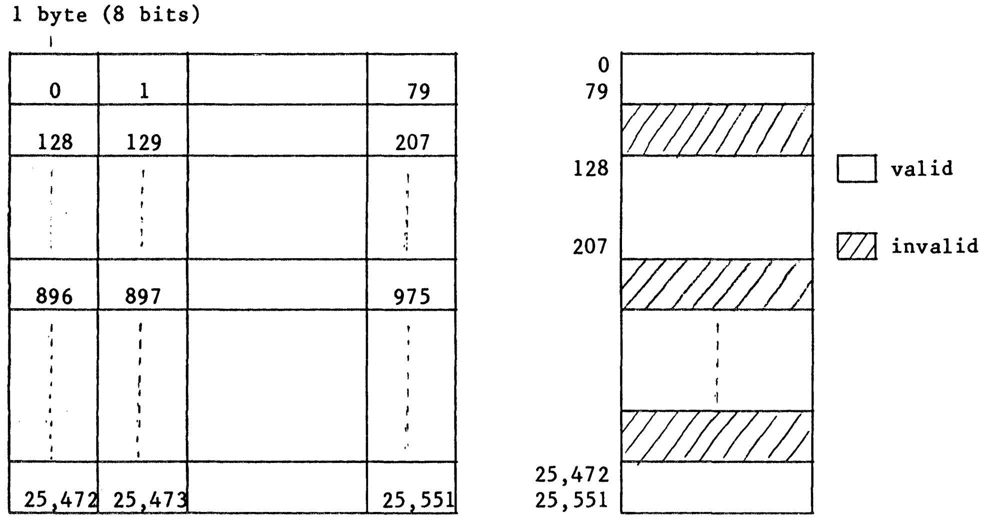
(ii) Example (1) of the Connection of the Graphic RAM and the LCTC

Figure 12-18 RAM Address Connection Example (1) in Superimposition of Graphic Display and Character Display

(3) Display format and memory address control

This method supplies continuous addresses to the graphic RAM only when D (= the number of horizontal dots of a screen) is the xth power of 2. When not, some area of the RAM will be invalid and cannot be accessed by the LCTC.

Figure 12-19(1) shows the graphic RAM address control in a screen of 640 (horizontal) x 200 (vertical) dots. Although a screen needs the data of 640 x 200 = 128,000 bits, the graphic RAM needs the capacity of 640 x (1,024/640) x 200 = 204,800 bits. When the MPU writes data into the graphic RAM, the invalid area should be taken into consideration. Figure 12-19(2) shows the relation between the invalid area of the RAM and the data display position on a screen of 640 x 200 dots.



(1) Memory address and display position on a screen

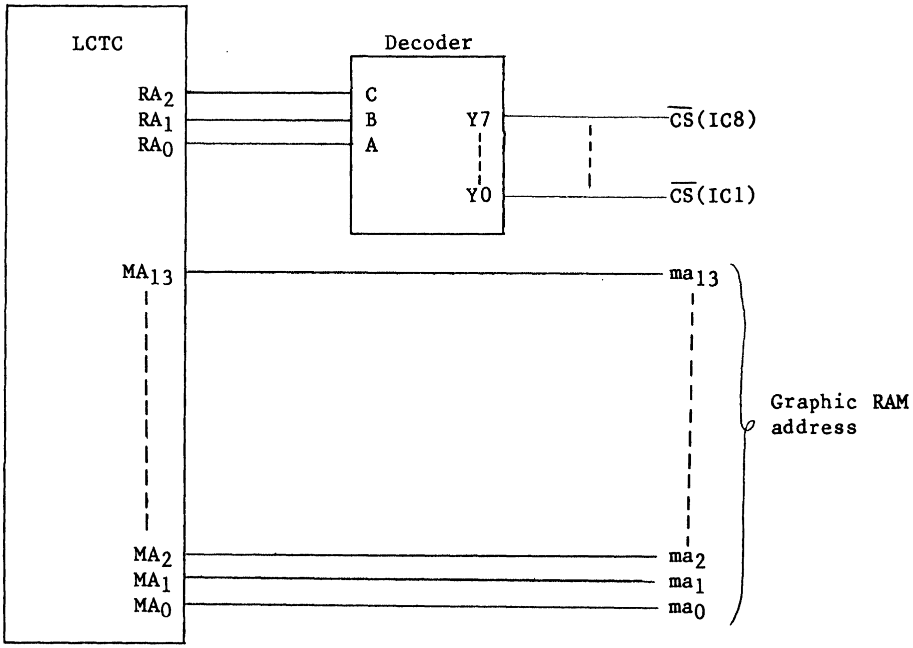
(2) Invalid area of the RAM

Figure 12-19 Graphic RAM Address Control in a Screen of 640 x 200 Dots

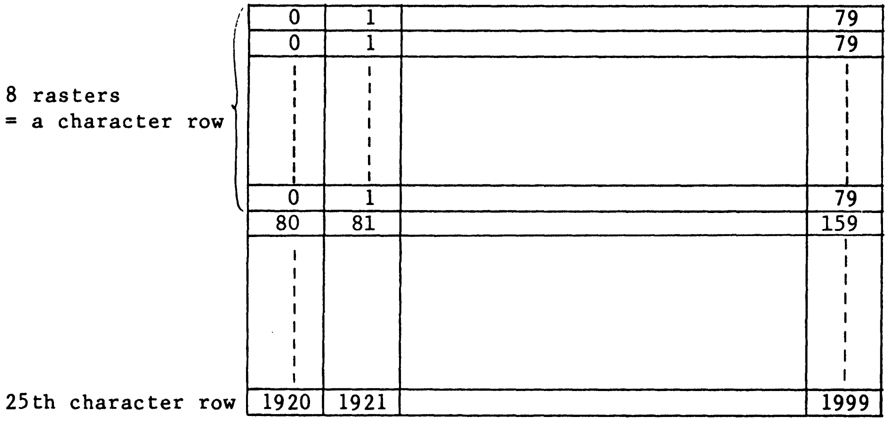
(4) Other methods for superimposition of character display and graphic display

Using a raster address signal as a chip select signal of a memory lessens the invalid area of the RAM mentioned before. Here as many memories as the number of rasters of a character row are used. The Nth raster data of each character row are placed in the Nth memory in line.

This method increases the number of external RAM's. Figure 12-20 shows an example of memory address connection when a screen size is 640 x 200 dots and a character row is constructed with 8 rasters. Since (640 x 200)/8 equals 16,000, it requires as many as 8 memories of 16 kbits. Therefore it can lessen the invalid area.



(i) Example (2) of Connection of the graphic RAM and the LCTC



(ii) Example (2) of graphic RAM display

Figure 12-20 RAM Address Connection Example (2) in Superimposing of Graphic Display and Character Display

13. LCTC APPLICATION

13.1 1 RAM Graphics

Conventionally, graphics can be performed using 2 RAMs with a small LCD. That is, the LCTC fetches 1 byte of data from V-RAM (video RAM) and 1 byte of data from A-RAM (attribute RAM), and outputs 1 byte of data in character mode, while it outputs 2 bytes of data (A-RAM + V-RAM) in graphic mode. This method, however, requires 2 RAMs to perform graphic display, and thus its system configuration cost is relatively expensive when using a small LCD. As an alternative, graphics can be performed by outputting 1 byte of data using the LCTC in character mode. Consequently, the maximum raster address must be set to 0, and then V-RAM data is input without CGROM. (See Figure 13-1.)

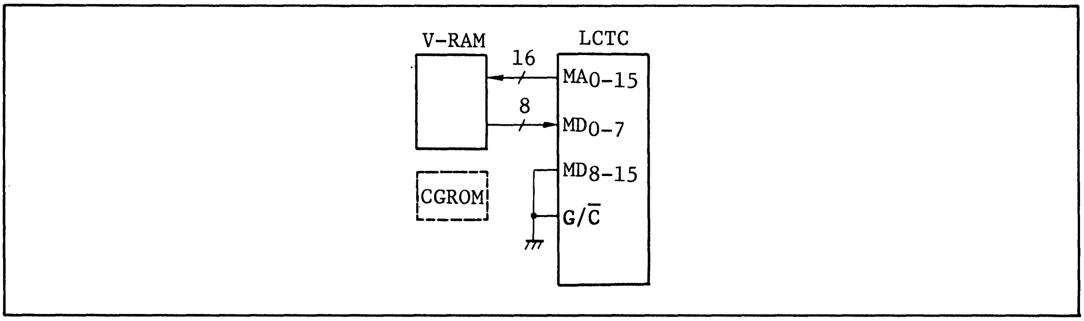


Figure 13-1 Graphic Display System Using 1 RAM

13.2 Method of Chinese Character Display

Since the LCTC is very suitable for large scale LCDs, it is very useful for display control of processors such as in compact, portable word processors whose screens are recently becoming larger.
Three methods can be used to perform Chinese character display by using the LCTC. First of all, the LCTC is used in character mode. Since one character is displayed in 1 to 32 dots (height) x 8 dots (width) with A-RAM data = 8 bits and V-RAM data = 8 bits for normal character display, only 256 characters can be provided in this method. However, since an attribute function of the LCTC requires only 4 bits, the remaining 12 bits can be used as addresses for a character generator, so that the attribute function can still be used and 4096 characters can be provided. An attribute for each Chinese character can also be specified. Because of 16 bits, a cursor cannot be used, but an underline attribute utilizing nondisplay (black) attribute can substitute. Generate the signal which becomes high while the raster is being selected on which the user want to display a cursor. Then ANDed it with the signal corresponding to nondisplay (block) in the attribute RAM to apply it to MD15.
In this case, a Chinese character generator in low scan mode with 1-set-1-chip configuration, displaying 16 x 16 dots, should be used.

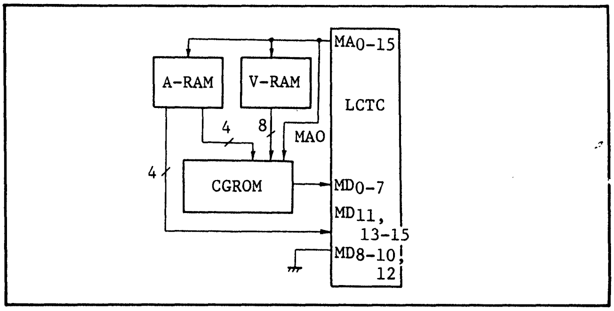


Figure 13-2 System Configuration (1) for Displaying Chinese Characters (in character mode)

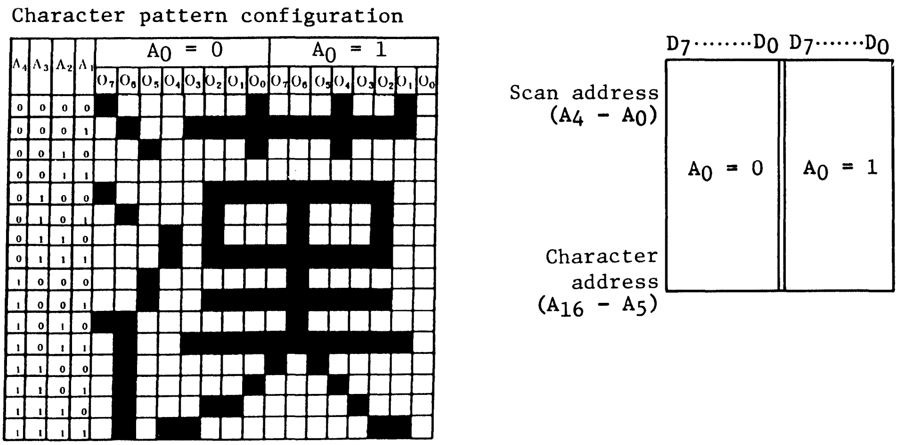


Figure 13-3 Chinese Character ROM for System Configuration (1)

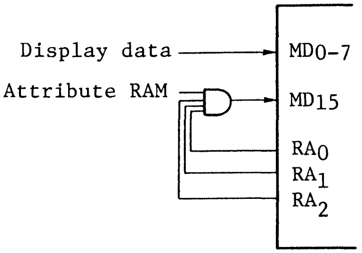


Figure 13-4 Application of Attribute Function (Underline)

In the second method, graphic 2 mode is used. Since this mode can control raster addresses and is 16-bit data fetch type, it can handle 16 x 16 dot Chinese characters as they are. As for the system configuration shown in Figure 13-5, data from CGROM is fetched into MD0 to MD15 (16 bits). In this case, an attribute function cannot be used. A Chinese character generator in low scan mode with 1-set-2-chip configuration, displaying 16 x 16 dots, should be used.

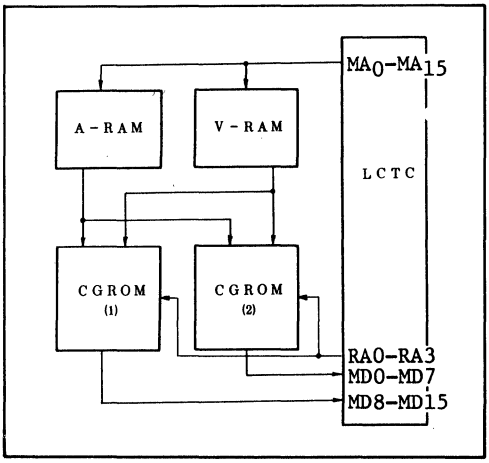


Figure 13-5 System Configuration (2) for Chinese Character Display (Graphic 2 mode)

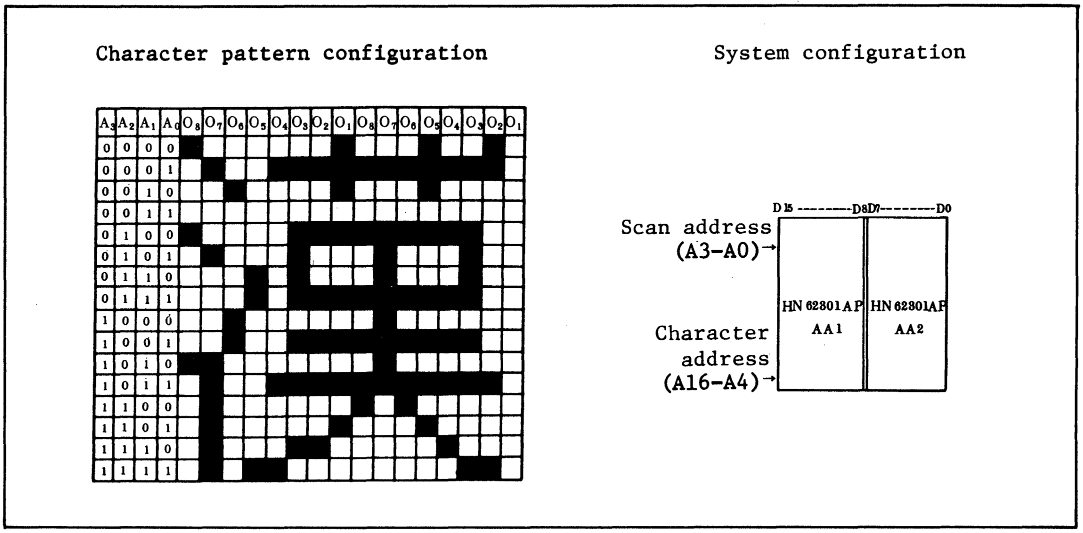

Character pattern configuration
System configuration
A3 A2 A1 A0 O8 O7 O6 O5 O4 O3 O2 O1 O8 O7 O6 O5 O4 O3 O2 O1
D15 --------D8D7--------D0
Scan address (A3-A0)
Character address (A16-A4)
HN 62301AP AA1
HN 62301AP AA2

Figure 13-6 Chinese Character ROM for System Configuration (2)

In the third method, graphic 1 mode is used. In this case, as shown in Figure 13-7, CGROM is located near the MPU and Chinese characters are written into a display buffer as a bit pattern. Through the MPU, display functions such as character variation or overlaying with figures are enhanced. Also, using this method with 1 RAM graphics (see section 13.1) enables low-cost operation.

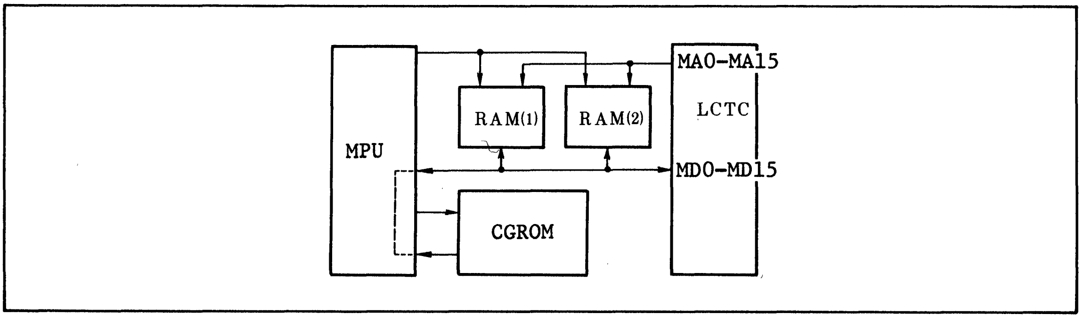


Figure 13-7 System Configuration (3) for Chinese Character Display (Graphic 1 mode)

13.3 Software Compatible with CRTC

Since LCTC internal register configuration and control method of memory address are based on CRT controller HD6845 (CRTC), conventional CRT display system software can be used; a CRT system can be easily replaced by an LCD system.

(1) System configuration

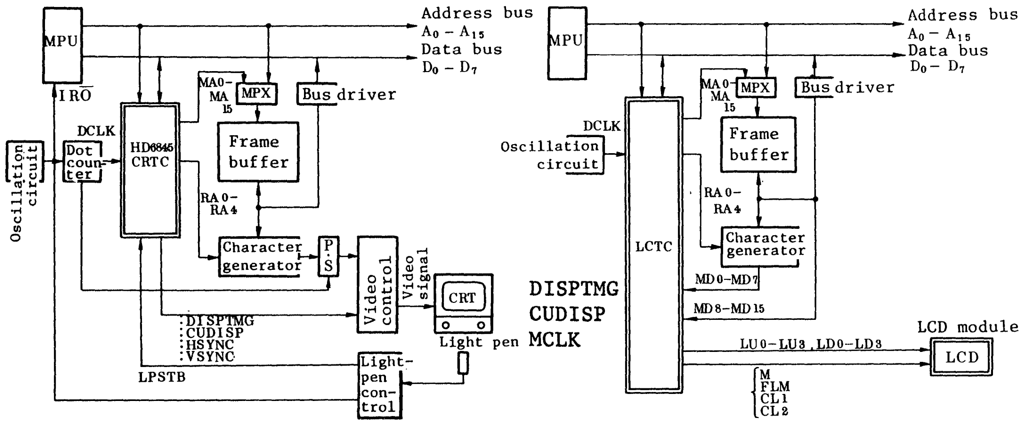
Figure 13-8 (a) shows the CRTC system and Figure 13-8 (b) shows the LCTC system.
Basic configuration (especially memory peripheral configuration important in programming) is the same. Therefore, LCD display system, which is software compatible with CRTC, is configured taking into account the points in (2) and afterwards. The circuits corresponding to dot counter, P/S converter circuit and video control circuit are incorporated, and directly connecting LCTC output to the LCD module provides an easy and compact display system configuration. Note that since a light pen cannot be used for an LCD display, the LCTC does not provide light pen control functions.

(2) Memory control

The LCTC employs the same memory control method as the CRTC. That is, use of the DISPTMG signal enables the LCTC to indicate its memory access time to the MPU, and allows for time sharing by the LCTC and MPU. A dot counter is also included and cycle steal can be easily performed by indication of MCLK signal output.
Since an LCD display does not require HSYNC signal nor VSYNC signal, the LCTC does not output these signals. However, some CRT display software utilize these signals to identify horizontal and vertical retrace period. To accommodate these software, CL1 and FLM should be used instead of HSYNC signal and VSYNC signal, respectively.

(3) Register configuration

As shown in Table 13-1, LCTC register configuration is compatible with the CRTC. The LCTC, however, does not provide registers (R2 to R7) related to horizontal and vertical synchronization unnecessary for LCD display, as well as the interlace register (R8) and registers (R16 and R17) related to light pen functions. Data written into these non-existent registers is ignored.



(a) System Configuration Using HD6845 (CRTC)

(b) System Configuration Using HD63645F/HD64645F (LCTC)

Figure 13-8 Comparison of Character Display System Between the CRTC and LCTC

Nevertheless, display information, such as number of display characters, display format of the maximum raster, and cursor and start address, can be displayed on the LCD without modifying a CRTC program.

(4) Additional registers and easy mode

R18 to R22 are newly added to the LCTC, providing functions for higher display performance than the CRTC. Therefore, since the CRTC does not provide these registers, they must be additionally specified to run a CRTC program. However, if specified in BIOS at system startup, application software does not have to be modified.
Moreover, when the screen size is 200 x 640 dots, BIOS does not have to be modified when using the easy mode function; the CRTC program is activated even if software is not modified at all. When MODE pin is set to high, easy mode is entered and register values are specified as shown in Table 13-2. *IBM-PC software can be handled by this mode.

*: IBM-PC is a registered trademark of International Business Machines, Inc.

Table 13-1 Internal Register Comparison between the LCTC and CRTC

Reg. No.	LCTC HD63645F/HD64645F	Comparison	CRTC HD6845
AR	Address Register	Equivalent to CRTC	Address Register
R0	Horizontal Total Characters		Horizontal Total Characters
R1	Horizontal Displayed Characters		Horizontal Displayed Characters
R2		Particular to CRTC; unnecessary for LCTC	Horizontal Sync Position
R3			Sync Width
R4			Vertical Total Rows
R5			Vertical Total Adjust
R6			Vertical Displayed Rows
R7			Vertical Sync Position
R8			Interlace Mode and Skew
R9	Maximum Raster Address	Equivalent to CRTC	Maximum Raster Address
R10	Cursor Start Raster		Cursor Start Raster
R11	Cursor End Raster		Cursor End Raster
R12	Start Address (H)		Start Address (H)
R13	Start Address (L)		Start Address (L)
R14	Cursor Address (H)		Cursor (H)
R15	Cursor Address (L)		Cursor (L)
R16		Particular to CRTC; unnecessary for LCTC	Light Pen (H)
R17			Light Pen (L)
R18	Horizontal Virtual Screen Width	Additional registers for LCTC	
R19	Multiplexing Duty Ratio (H)		
R20	Multiplexing Duty Ratio (L)		
R21	Display Start Raster		
R22	Mode Register		

Table 13-2 Register Values in Easy Mode

Reg. No.	Register Name	Fixed Value (decimal)
R9	Maximum raster address	7
R10	Cursor start raster	6
R11	Cursor end raster	7
R18	Horizontal virtual screen width	Same value as (R1)
R19	Multiplexing duty ratio (H)	99 (in dual screen mode)
R20	Multiplexing duty ratio (L)	199 (in single screen mode)
R21	Display start raster	0
R22	Mode register	0

13.4 How to Connect with ACRTC

Since the LCTC is designed to be software compatible with the CRTC, it does not provide a drawing function which the ACRTC has. However, using the ACRTC as a drawing processor enables a configuration in which the ACRTC gives its drawing to a display buffer, from which the LCTC can display it on the LCD.

Figure 13-9 shows a block diagram of this configuration. This allows the effective use of the ACRTC drawing function on the LCD. In this case, timing should be designed so that the LCTC and ACRTC share access of the display buffer by cycle steal.

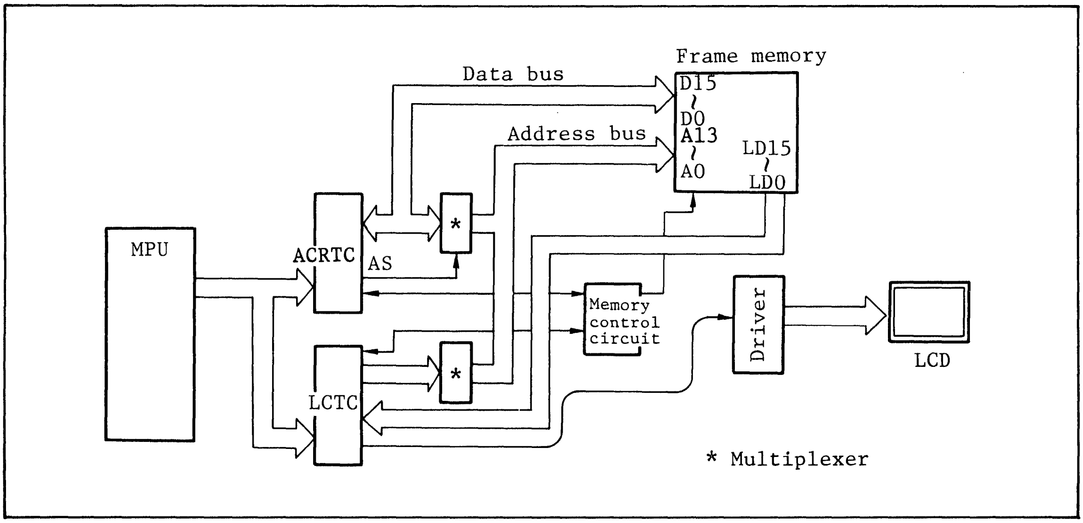


Figure 13-9 Connection with the ACRTC

As shown above, if the LCTC is configured to display, some ACRTC functions cannot be used. That is, the drawing processor within the ACRTC can be used, but not its display processor.

The following ACRTC functions can be used.

(a) High Level Command Language:	38 commands including graphic drawing commands such as LINE, CIRCLE, ELLIPSE, PAINT and COPY. With X-Y coordinates as a parameter, throughput of the system is enormously improved.
(b) High Speed Graphic Drawings:	Maximum 408 ns/pixel By unique memory storing method, the same graphic drawing is performed for both monochrome and color display.
(c) Pattern Graphic Drawing:	Using 32-byte pattern RAM, tilling can be easily performed by using color patterns.
(d) Drawing operation:	8 drawing operation modes (REPLACE, OR, AND, EOR and 4 CONDITIONAL REPLACEs) are provided. In particular, using CONDITIONAL REPLACE enables conditional color drawing such as specifications of the specific background color and drawing inhibited color, drawing of color data with priority.
(e) Drawing area detection function:	Controls drawing area such as drawing inhibition outside of a specified area or detection of a particular area
(f) DMA interface:	Control signal of DMA controller is provided, and command transfer and high speed DMA transfer between system memory and frame buffer are supported.

The following functions cannot be used.

(a) Split screens
(b) Zooming
(c) Smooth scroll
(d) Screen overlaying
(e) External synchronization
(f) Programmable cursors

LCTC functions partially cover (c) and (d) of the above functions. For details of the ACRTC, refer to "HD63484 ACRTC User's Manual".

14. ELECTRICAL CHARACTERISTICS

14.1 Absolute Maximum Ratings

Item	Symbol	Value	Note
Supply voltage	V_{CC}	−0.3 to +7.0 V	2
Terminal voltage	V_{in}	−0.3 to V_{CC} +0.3 V	2
Operating temperature	T_{opr}	−20°C to +75°C	
Storage temperature	T_{stg}	−55°C to +125°C	

Notes: 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions (V_{CC} = 5.0 V ±10%, GND = 0 V, Ta = −20°C to +75°C). If these conditions are exceeded, it could affect reliability of LSI.

2. Width respect to GROUND (GND = 0 V)

14.2 DC characteristics (V_{CC} = 5.0 V ± 10%, GND = 0 V, Ta = -20°C to +75°C, unless otherwise noted.)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high voltage	$\overline{\text{RES}}$, MODE, SK0, SK1	V_{IH}	$V_{CC}-0.5$		$V_{CC}+0.3$	V	
	DCLK, ON/$\overline{\text{OFF}}$		2.2		$V_{CC}+0.3$	V	
	All others		2.0		$V_{CC}+0.3$	V	
Input low voltage	All others	V_{IL}	−0.3		0.8	V	
Output high voltage	TTL Interface[1]	V_{OH}	2.4		—	V	$I_{OH}=-400\mu A$
	CMOS Interface[1]		$V_{CC}-0.8$		—	V	$I_{OH}=-400\mu A$
Output low voltage	TTL Interface	V_{OL}	—		0.4	V	$I_{OL}=1.6mA$
	CMOS Interface		—		0.8	V	$I_{OL}=400\mu A$
Input leakage current	All inputs except DB_0-DB_7	I_{IL}	−2.5		+2.5	μA	
Three state (off-state) leakage current	DB_0-DB_7	I_{TSL}	−10		+10	μA	
Current dissipation[2]		I_{CC}	—		10	mA	

Notes: 1. TTL Interface; MA0-MA15, RA0-RA4, DISPTMG, CUDISP, DB0-DB7, MCLK
CMOS Interface; LU0-LU3, LD0-LD3, CL1, CL2, M, FLM

2. Input/output current is excluded. When input is at the intermediate level with CMOS, excessive current flows through the input circuit to power supply. Input level must be fixed at high or low to avoid this condition.

3. If the capacity loads of LU0-LU3 and LD0-LD3 exceed the rating, noise over 0.8 V may be produced on CUDISP, DISPTMG, MCLK, FLM and M. In case the loads of LU0-LU3 and LD0-LD3 are larger than the ratings, supply signals to the LCD module through buffers.

14.3 AC Characteristics

CPU Interface (HD63645F - 68 family)

Item	Symbol	Min	Typ	Max	Unit	Figure
Enable cycle time	t_{CYCE}	500	—	—	ns	14-1
Enable pulse width (high)	P_{WEH}	220	—	—	ns	
Enable pulse width (low)	P_{WEL}	220	—	—	ns	
Enable rise time	t_{Er}	—	—	25	ns	
Enable fall time	t_{Ef}	—	—	25	ns	
$\overline{CS}$, RS, R/$\overline{W}$ setup time	t_{AS}	70	—	—	ns	
$\overline{CS}$, RS, R/$\overline{W}$ hold time	t_{AH}	10	—	—	ns	
DB_0-DB_7 setup time	t_{DS}	60	—	—	ns	
DB_0-DB_7 hold time	t_{DHW}	10	—	—	ns	
DB_0-DB_7 output delay time	t_{DDR}	—	—	150	ns	
DB_0-DB_7 output hold time	t_{DHR}	20	—	—	ns	

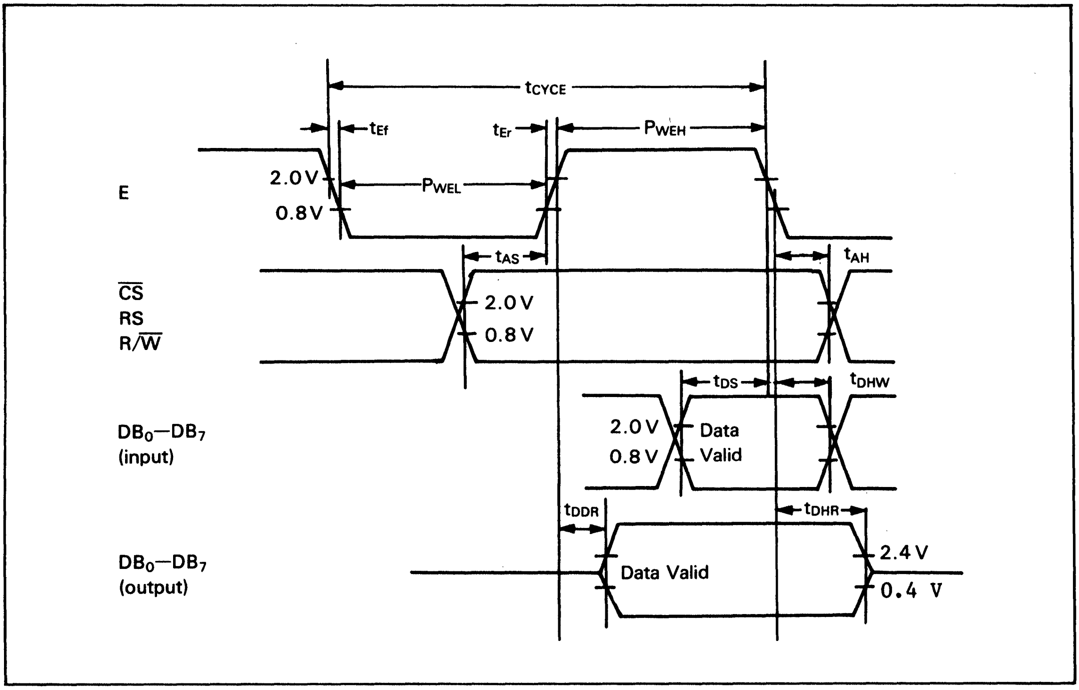


Figure 14-1 CPU Interface (HD63645F-68 family)

CPU Interface (HD64645F, HD64646F - 80 family)

Item	Symbol	Min	Typ	Max	Unit	Figure
$\overline{RD}$ high level width	t_{WRDH}	190	—	—	ns	14-2
$\overline{RD}$ low level width	t_{WRDL}	190	—	—	ns	
$\overline{WR}$ high level width	t_{WWDH}	190	—	—	ns	
$\overline{WR}$ low level width	t_{WWDL}	190	—	—	ns	
$\overline{CS}$, RS setup time	t_{AS}	0	—	—	ns	
$\overline{CS}$, RS hold time	t_{AH}	0	—	—	ns	
DB_0-DB_7 setup time	t_{DSW}	100	—	—	ns	
DB_0-DB_7 hold time	t_{DHW}	0	—	—	ns	
DB_0-DB_7 output delay time	t_{DDR}	—	—	150	ns	
DB_0-DB_7 output hold time	t_{DHR}	20	—	—	ns	

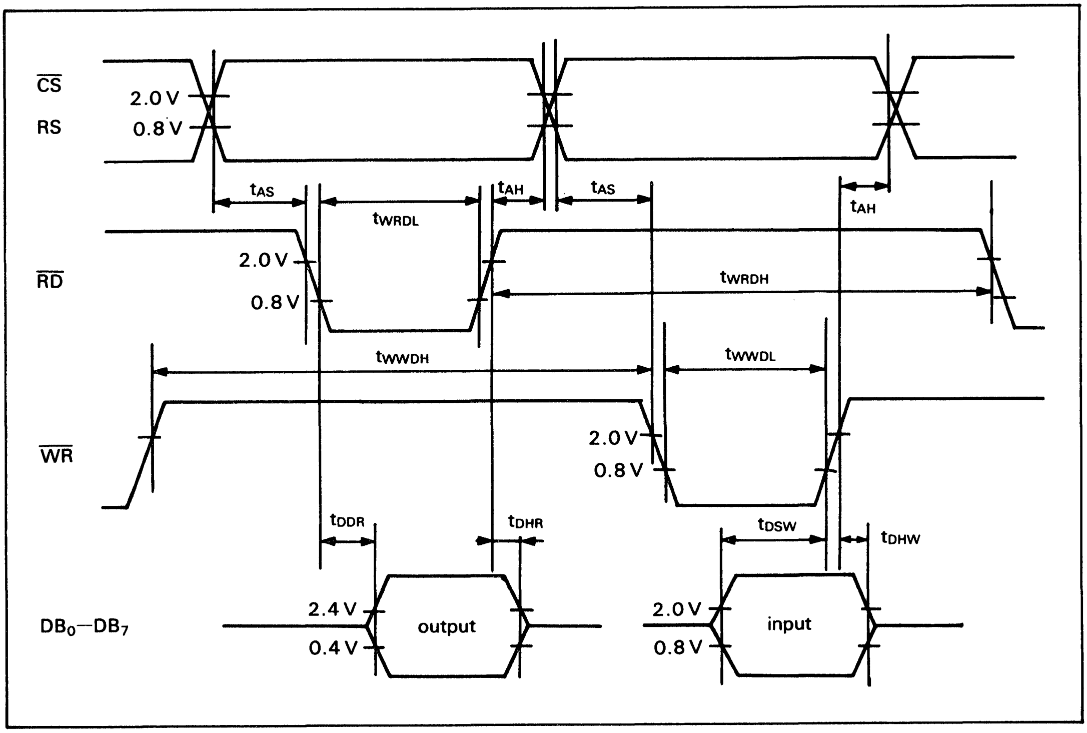


Figure 14-2 CPU Interface (HD64645F, HD64646F-80 family)

AC Characteristics (Cont)

Memory Interface

Item	Symbol	Min	Typ	Max	Unit	Figure
DCLK cycle time	t_{CYCD}	100	—	—	ns	14-3
DCLK high level width	t_{WDH}	30	—	—	ns	
DCLK low level width	t_{WDL}	30	—	—	ns	
DCLK rise time	t_{Dr}	—	—	20	ns	
DCLK fall time	t_{Df}	—	—	20	ns	
MCLK delay time	t_{DMD}	—	—	60	ns	
MCLK rise time	t_{Mr}	—	—	30	ns	
MCLK fall time	t_{Mf}	—	—	30	ns	
MA0-MA15 delay time	t_{MAD}	—	—	150	ns	
MA0-MA15 hold time	t_{MAH}	10	—	—	ns	
RA0-RA4 delay time	t_{RAD}	—	—	150	ns	
RA0-RA4 hold time	t_{RAH}	10	—	—	ns	
DISPTMG delay time	t_{DTD}	—	—	150	ns	
DISPTMG hold time	t_{DTH}	10	—	—	ns	
CUDISP delay time	t_{CDD}	—	—	150	ns	
CUDISP hold time	t_{CDH}	10	—	—	ns	
CL1 delay time	t_{CL1D}	—	—	150	ns	
CL1 hold time	t_{CL1H}	10	—	—	ns	
CL1 rise time	t_{CL1r}	—	—	50	ns	
CL1 fall time	t_{CL1f}	—	—	50	ns	
MD0-MD15 setup time	t_{MDS}	30	—	—	ns	
MD0-MD15 hold time	t_{MDH}	15	—	—	ns	

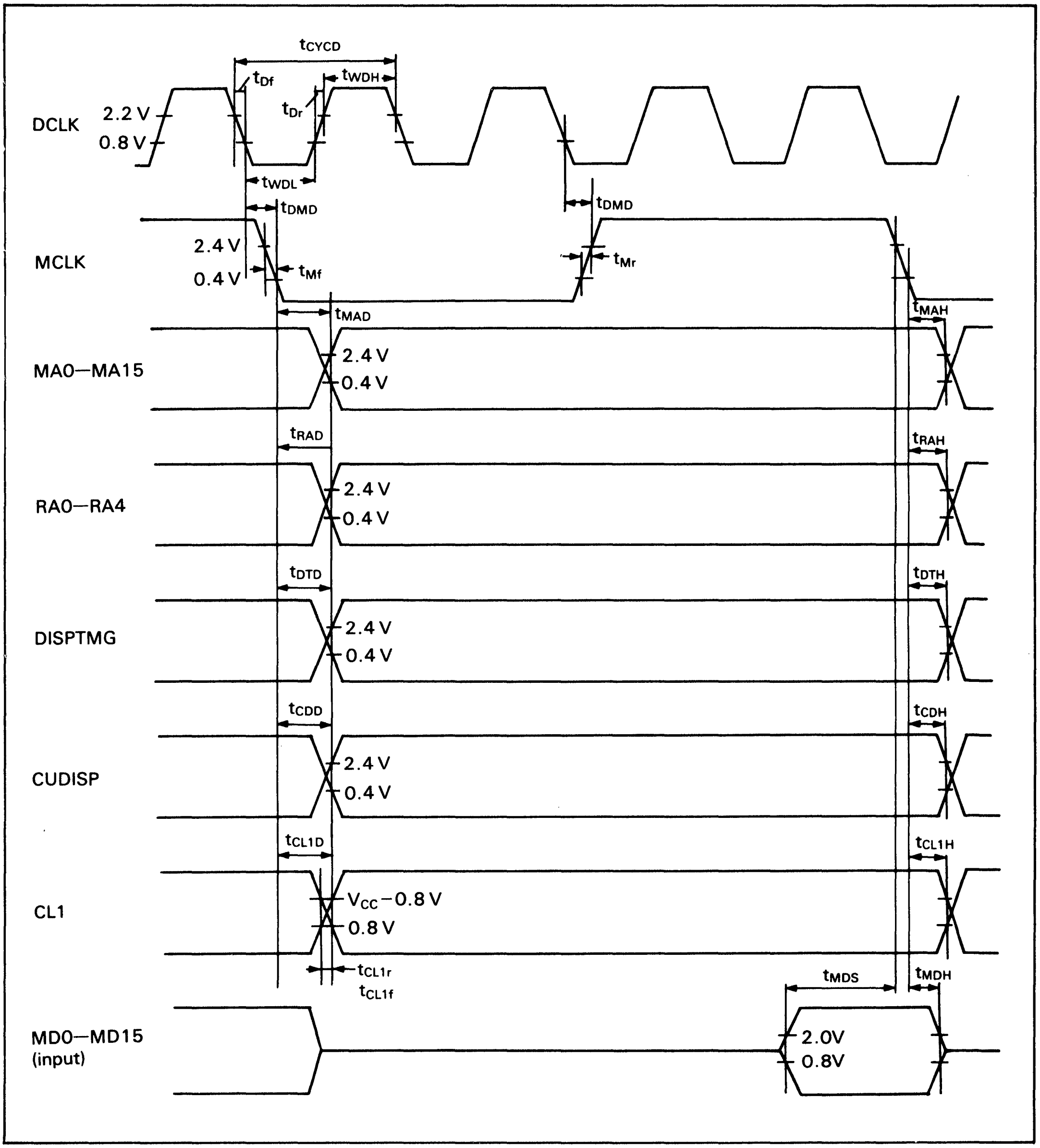


Figure 14-3 Memory Interface

AC Characteristics (Cont)

LCD Interface 1 (HD63645F, HD64645F)

Item	Symbol	Min	Typ	Max	Unit	Figure
Display data setup time	t_{LDS}	50	—	—	ns	14-4
Display data hold time	t_{LDH}	100	—	—	ns	
CL2 high level width	t_{WCL2H}	100	—	—	ns	
CL2 low level width	t_{WCL2L}	100	—	—	ns	
FLM setup time	t_{FS}	500	—	—	ns	
FLM hold time	t_{FH}	300	—	—	ns	
CL1 rise time	t_{CL1r}	—	—	50	ns	
CL1 fall time	t_{CL1f}	—	—	50	ns	
CL2 rise time	t_{CL2r}	—	—	50	ns	
CL2 fall time	t_{CL2f}	—	—	50	ns	

Note: At f_{CL2} = 3 MHz

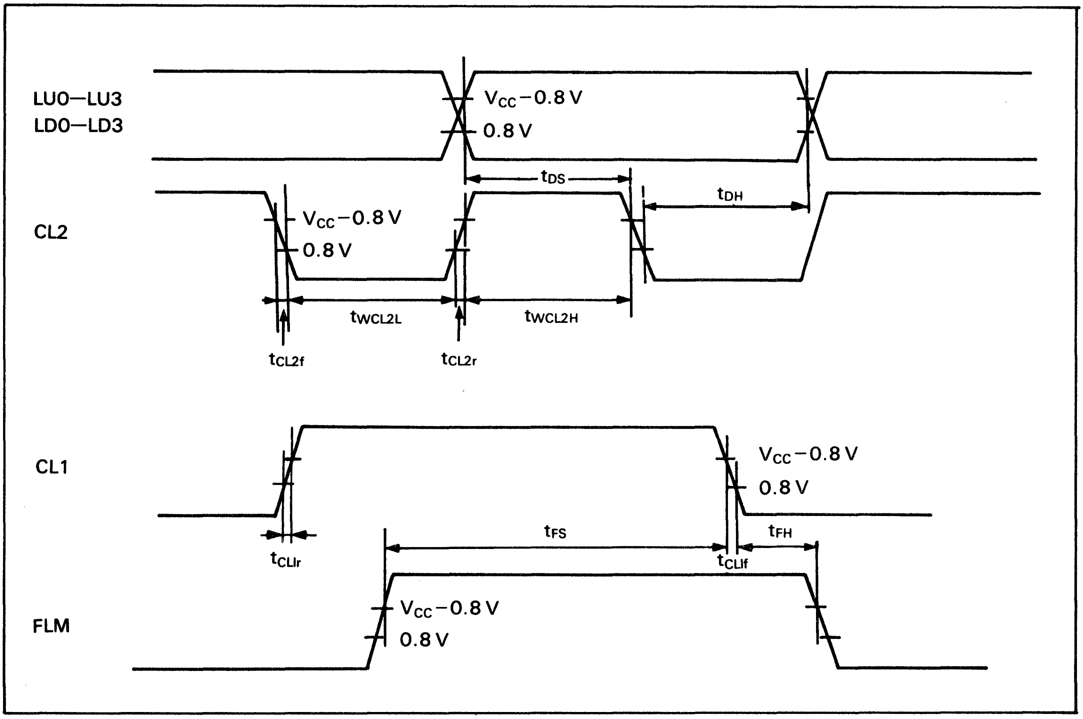


Figure 14-4 LCD Interface (HD63645F, HD64645F)

AC Characteristics (Cont)

LCD Interface 2 (HD64646F)

Item	Symbol	Min	Typ	Max	Unit	Figure
FLM setup time	t_{FS}	500	-	-	ns	Figure 14-5
FLM hold time	t_{FH}	300	-	-	ns	
M delay time	t_{DM}	-	-	200	ns	
CL1 high level width	t_{CL1H}	300	-	-	ns	
Clock setup time	t_{SCL}	500	-	-	ns	
Clock hold time	t_{HCL}	100	-	-	ns	
Phase difference 1	t_{PD1}	100	-	-	ns	
Phase Difference 2	t_{PD2}	500	-	-	ns	
CL2 high level width	t_{CL2H}	100	-	-	ns	
CL2 low level width	t_{CL2L}	100	-	-	ns	
CL2 rise time	t_{CL2r}	-	-	50	ns	
CL2 fall time	t_{CL2f}	-	-	50	ns	
Display data setup time	t_{LDS}	80	-	-	ns	
Display data hold time	t_{LDH}	100	-	-	ns	
Display data deley time	t_{LDD}	-	-	30	ns	

Note: At f_{CL2} = 3 MHz

LCD Interface 3

Item	Symbol	Min	Typ	Max	Unit	Figure
FLM setup time	t_{FS}	500	-	-	ns	Figure 14-5
FLM hold time	t_{FH}	200	-	-	ns	
M delay time	t_{DM}	-	-	200	ns	
CL1 high level width	t_{CL1H}	300	-	-	ns	
Clock setup time	t_{SCL}	500	-	-	ns	
Clock hold time	t_{HCL}	100	-	-	ns	
Phase difference 1	t_{PD1}	70	-	-	ns	
Phase difference 2	t_{PD2}	500	-	-	ns	
CL2 high level width	t_{CL2H}	50	-	-	ns	
CL2 low level width	t_{CL2L}	50	-	-	ns	
CL2 rise time	t_{CL2r}	-	-	50	ns	
CL2 fall time	t_{CL2f}	-	-	50	ns	
Display data setup time	t_{LDS}	30	-	-	ns	
Display data hold time	t_{LDH}	30	-	-	ns	
Display data delay time	t_{LDD}	-	-	30	ns	

Note: At f_{CL2} = 5 MHz

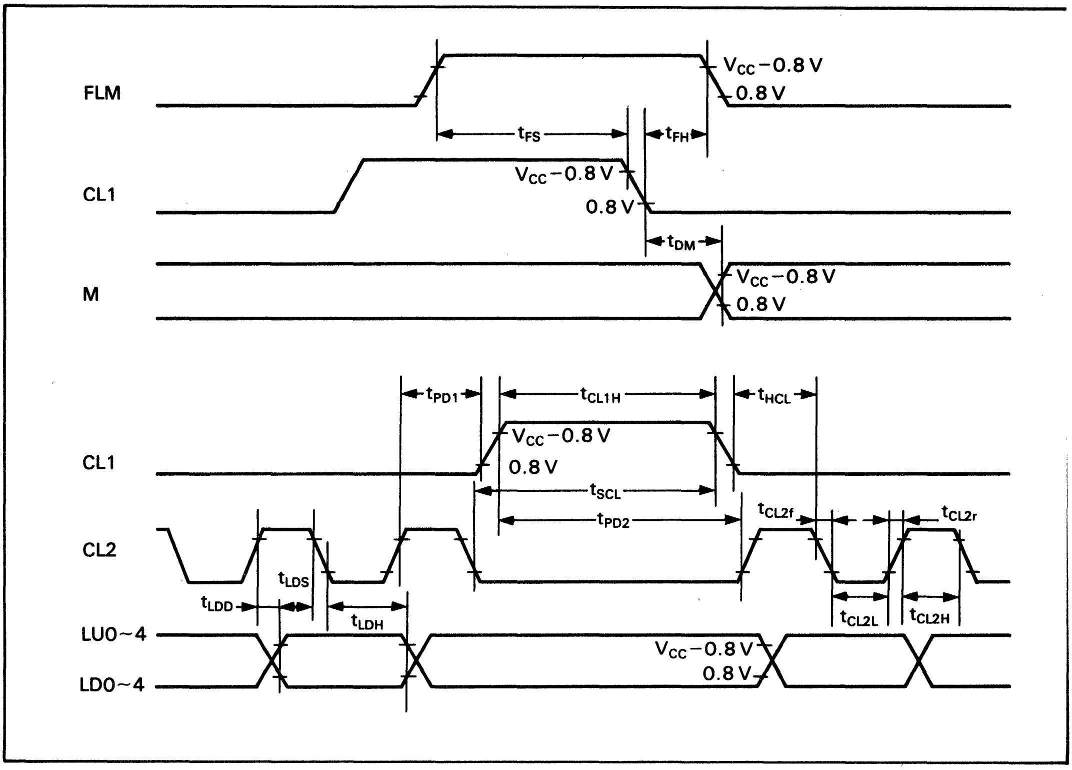
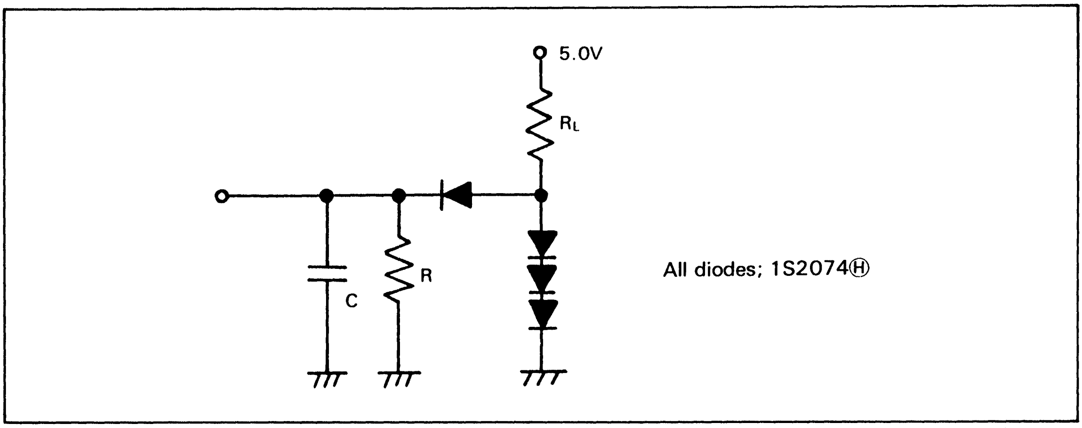


Figure 14-5 LCD Interface (HD64646F)

AC Characteristics

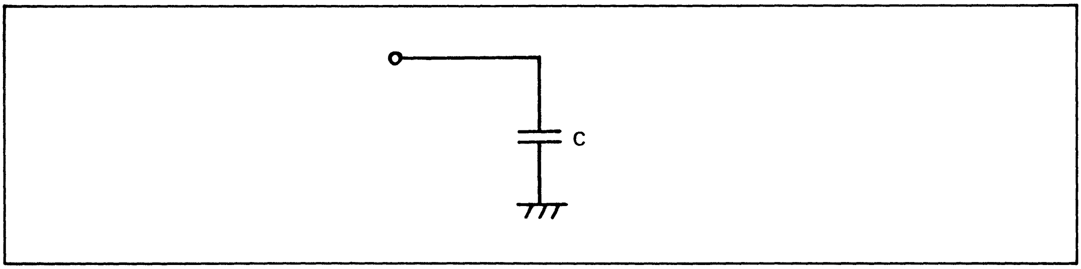
TTL Load

Pin	R_L	R	C	Remarks
DB_0-DB_7	2.4 kΩ	11 kΩ	130 pF	tr, tf: Not specified
MA0-MA15, RA0-RA4, DISPTMG, CUDISP	2.4 kΩ	11kΩ	40 pF	
MCLK	2.4 kΩ	11 kΩ	30 pF	tr, tf: Specified



Capacity Load

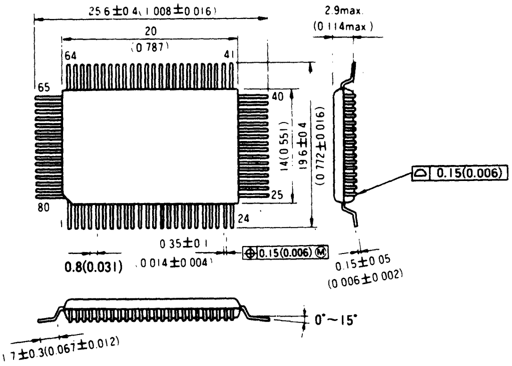
Pin	C	Remarks
CL2	150 pF	tr, tf: Specified
CL1	200 pF	
LU0-LU3, LD0-LD3, M	150 pF	tr, tf: Not specified
FLM	50 pF	

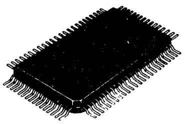


15. PACKAGE DIMENSION

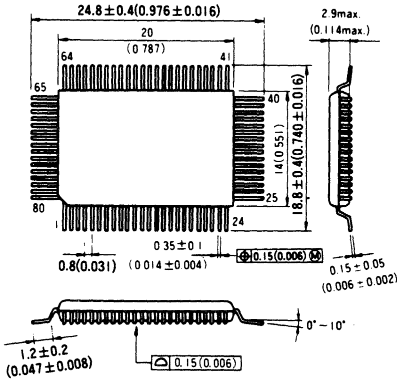
Scale: 3/
(Unit: mm (inch)

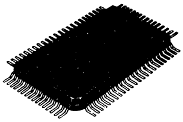
FP-80





FP-80B





-APPENDIX-

A. Abnormal Operation by Rewriting Registers during Display*

Reg. No.	Register Name	Abnormal Operation by Rewriting Registers and Countermeasure	Rewritable or not **
R0	Horizontal Total Characters	The horizontal scanning period goes out of order.	×
R1	Horizontal Displayed Characters	DISPTMG width may be shorter than the specified value, because the number of horizontal display characters is mistakenly obtained in rewriting registers only for 1 raster period.	○
R9	Maximum Raster Address	The number of rasters in one row might be temporarily different from the specified value by rewriting. Rewriting should be performed during DISPTMG low.	△
R10	Cursor Start Raster	Cursor raster may not be correctly displayed. Also, blinking cycle may be shorter temporarily. Rewriting should be performed during DISPTMG low.	△
R11	Cursor End Raster		△
R12	Start Address (H)	R12 and R13 are used during the last raster period of 1 field. Except for this period, rewriting is possible. Rewriting R12 and R13 in respective fields allows temporary display by start address dynamically determined in rewriting.	○
R13	Start Address (L)		○
R14	Cursor Address (H)	Rewriting in display period may temporarily cause cursor to be displayed at an address different from that specified. Rewriting should be performed during DISPTMG low.	○
R15	Cursor Address (L)	Rewriting R12 and R13 in respective fields allows cursor to be displayed temporarily at dynamic address in rewriting.	○
R18	Horizontal Virtual Screen Width	R18 is used during the last MCLK cycle of raster period. Rewriting during this period may cause displaying at an address different from that specified.	△
R19	Multiplexing Duty Ratio (H)	Rewriting in the last raster period of one field may cause the vertical scanning period to go out of order. Except for this period, rewriting is possible.	△
R20	Multiplexing Duty Ratio (L)		△
R21	Display Start Raster	R21 is used in the last raster period of one field. Except for this period, rewriting is possible.	○
R22	Mode Register	Rewriting during display period may temporarily cause distortion on the screen. Rewriting should be performed during DISPTMG low.	△

*: Temporarily occurs in rewriting an internal register during display. Usually after rewriting, the LSI performs display operation from the next field. (As operations in this table fall outside of the guaranteed range, they are shown just for reference.)

**: ○ --- The register can be rewritten without affecting display screen.
△ --- The register can be rewritten under certain conditions. If the conditions are not met, flickers temporarily occur.
× --- Rewriting may cause flickers temporarily.

B. Programming Precautions

Since internal register data to be written has the following limitations as shown in Table 1 , extra care should be taken in programming.

Table 1 Limitations of Register Data to Be Written

Function	Limitation	Applicable registers
Screen Configuration	$1 < Nhd < Nht + 1 \leq 256$ $Nhd + \frac{16}{m}{}^{*1} \leq Nht + 1$	R0, R1
	(Number of vertical dots) x (Number of horizontal dots) x (Frame frequency; f_{FRM}) $\leq$ (Data transfer speed; V) $\begin{Bmatrix}1\\2\end{Bmatrix}^{*2} \times (Nd + 1) \times Nhd \times \begin{Bmatrix}8\\16\end{Bmatrix}^{*3} \times f_{FRM} \leq V$	R1, R19 R20
	$Nhd \leq Nir$	R1, R18
	$0 \leq Nd \leq 511$	R19, R20
Cursor Control	$0 \leq Ncs \leq Nce$	R10, R11
	$Nce \leq Nr$	R10, R9
Smooth Scroll	$Nsr \leq Nr$	R21, R9
Memory Width	$0 \leq Nir \leq 255$	R18

*1: The value of m depends on the mode, as shown in the following table.

mode No.	m
5, 9	1
1, 6, 7, 8, 10, 11, 12, 13	2
2, 3, 4	4

*2: Set to 1 if the LCD screen has 1 panel and single screen configuration and to 2 if the LCD screen has 2 panels and single screen configuration. Refer to the following table.

mode No.	Set value
5, 6, 7, 8, 9, 10, 11, 12	1
1, 2, 3, 4, 13	2

*3: Set to 8 if one character consists of 8 dots and to 16 if one character consists of 16 dots, as shown below.

mode No.	Set value
1, 5, 9	8
2, 3, 4, 6, 7, 8, 10, 11, 12, 13	16

C. Reset Sequence

$\overline{\text{RES}}$ pin determines the internal state of LSI counters and the like. This pin neither affect register contents nor control output pins basically.

Reset is defined as follows (Figure C-1):

- ° At reset: the time when $\overline{\text{RES}}$ goes low
- ° During reset: the period while $\overline{\text{RES}}$ remains low
- ° After reset: the period on and after $\overline{\text{RES}}$ transition from low to high

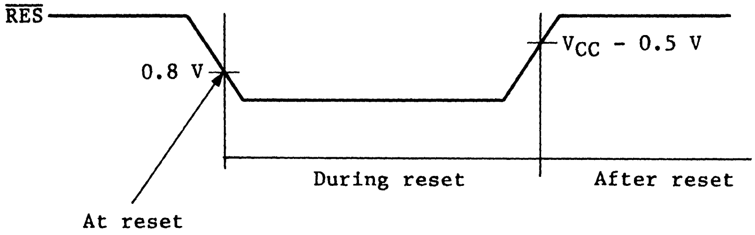


Figure C-1 Reset Definition

$\overline{\text{RES}}$ pin should be pulled high by users during operation.

C.1 Reset State

(1) Reset State of Pins

RES pin does not basically control output pins. It also operates independently of other input pins. Reset state of each pin is shown below.

Pin No.	Symbol	Name	I/O	Description
1 - 16	MD0 - MD15	MEMORY DATA 0 - 15	I	Unaffected
17	V_{CC1}	V_{CC}	-	—
18 - 21	LD3 - LD0	LCD DOWN DATA 3 - 0	O	Preserves states before reset
22 - 25	LU3 - LU0	LCD UP DATA 3 - 0	O	Preserves states before reset
26	M	M	O	Preserves state before reset
27	FLM	FIRST LINE MARKER	O	Preserves state before reset
28	CL1	CLOCK1	O	Preserves state before reset
29	CL2	CLOCK2	O	Depends on mode*
30, 31	SK0, SK1	SKEW0, 1	I	Unaffected
32	V_{CC2}	V_{CC}	-	—
33	DCLK	D CLOCK	I	Unaffected
34	MCLK	M CLOCK	O	Fixed at high level
35	DISPTMG	DISPLAY TIMING	O	Preserves state before reset
36	CUDISP	CURSOR DISPLAY	O	Preserves state before reset
37	GND2	GROUND	-	—
38	RES	RESET	I	—
39	CS	CHIP SELECT	I	Unaffected
40	RS	REGISTER SELECT	I	Unaffected
41	E	ENABLE	I	Unaffected
42	R/W	READ/WRITE	I	Unaffected
43 - 50	DB0 - DB7	DATA BUS 0 - 7	I/O	Unaffected
51	BLE	BLINK ENABLE	I	Unaffected
52	MODE	MODE	I	Unaffected
53	ON/OFF	ON/OFF	I	Unaffected
54	WIDE	WIDE	I	Unaffected
55	D/S	DUAL/SINGLE	I	Unaffected
56	LS	LARGE SCREEN	I	Unaffected
57	AT	ATTRIBUTE	I	Unaffected
58	G/C	GRAPHIC/CHARACTER	I	Unaffected
59	GND1	GROUND	-	—
60 - 64	RA0 - RA4	RASTER ADDRESS 0 - 4	O	Preserves states before reset
65 - 80	MA0 - MA15	MEMORY ADDRESS 0 - 4	O	Preserves states before reset

*1: The reset state of CL2 depends on the mode as follows.

mode No.	Reset state
5, 6, 7, 8, 13	Fixed at low level
1, 2, 3, 4, 9, 10, 11, 12	① Fixed at high level with RES state in data transfer ② Fixed at low level with RES state except in data transfer

(2) Reset State of Registers

RES pin does not affect register contents. Therefore, registers can be read and written even during reset state. Their contents will be preserved regardless of reset until they are rewritten.

C.2 Display Sequence after Reset

The LCTC starts display operation immediately after reset. Take extra care since in the first field after reset, its display operation is different from normal operation.

The differences between normal operation and that after reset are as follows:

(1) After reset, memory address (MA) starts from 0 in the first field, and from the set value in the start address register (R12, R13) after that field.

(2) After reset, raster address (RA) starts from 0 in the first field, and from the set value in the display start raster register (R21).

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