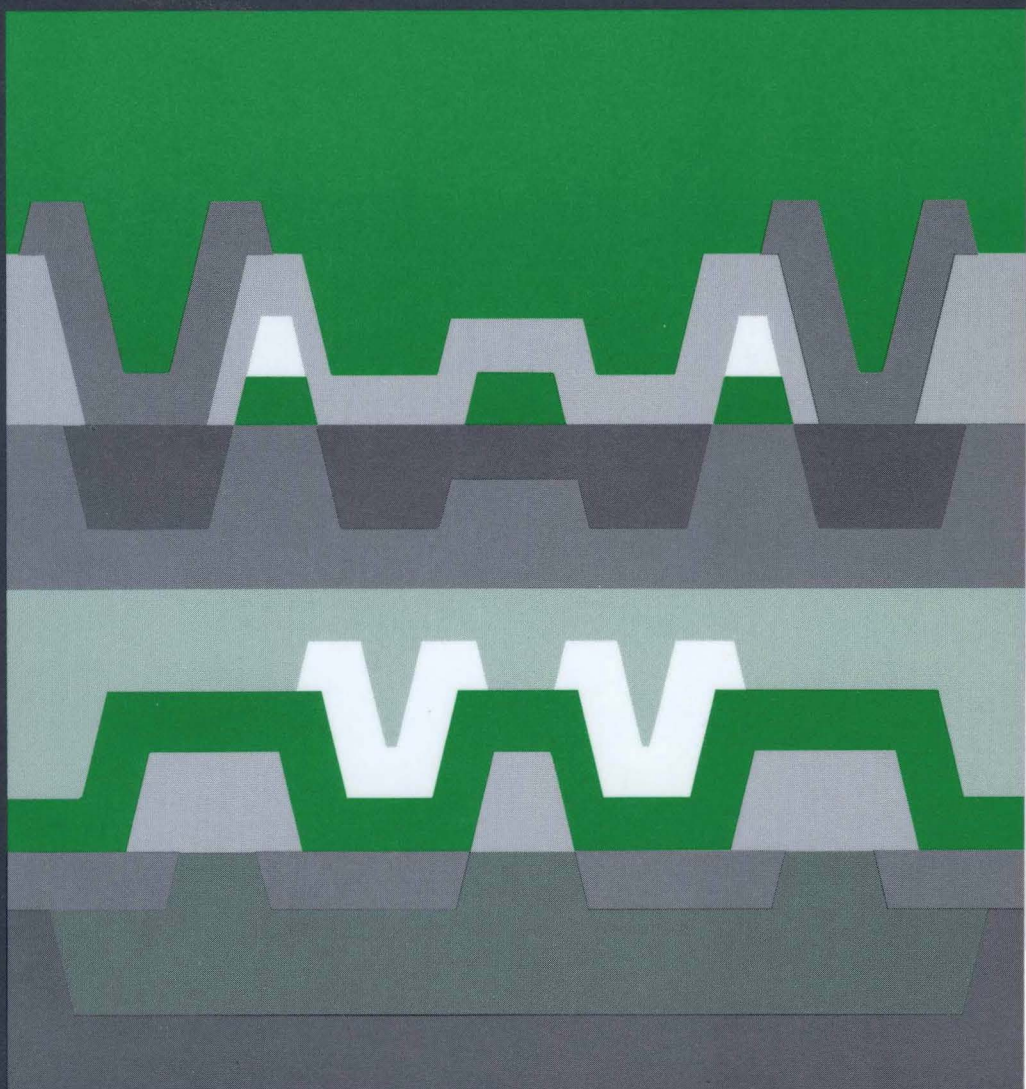
HITACHI

IC MEMORIES DATA BOOK



#M11

HITACHI

IC MEMORIES DATA BOOK

#M11

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■QUICK REFERENCE GUIDE TO HITACHI IC MEMORIES

■MOS RAM

Mode	Total Bit	Type No.	Process	Organization (word × bit)	Access Time (ns)max	Cycle Time (ns)min	Supply Voltage (V)	Power Dissipation (W)	Package† Pin No.	CG	G	P	FP	SP	Page
Static	16k-bit	HM6116-2	CMOS	2048×8	120	120	+5	0.1m/0.2	24	●	●	●	●		65
		HM6116-3			150	150		0.1m/0.18		●	●	●	●		65
		HM6116-4			200	200				●	●	●	●		65
		HM6116L-2			120	120		20μ△/0.18			●	●	●		80
		HM6116L-3			150	150		20μ△/0.16			●	●	●		80
		HM6116L-4			200	200					●	●	●		80
		HM6116A-12			120	120		0.1m/15m				●		●	98
		HM6116A-15			150	159						●		●	98
		HM6116A-20			200	200						●		●	98
		HM6116AL-12			120	120		5μ/10m				●		●	102
		HM6116AL-15			150	150						●		●	102
		HM6116AL-20			200	200						●		●	102
		HM6117-3			150	150		0.1m/0.2				●	●		106
		HM6117-4			200	200						●	●		106
		HM6117L-3			150	150		10μ/0.18				●	●		116
		HM6117L-4			200	200						●	●		116
		HM6168H-45		4096×4	45	45		0.1m/0.25	20		●	●			128
		HM6168H-55			55	55					●	●			128
		HM6168H-70			70	70					●	●			128
		HM6168HL-45			45	45		5μ/0.25				●			132
		HM6168HL-55			55	55						●			132
		HM6168HL-70			70	70						●			132
		HM6167		16384×1	70	70		0.1m/0.15	20		●	●			137
		HM6167-6			85	85					●	●			137
		HM6167-8			100	100					●	●			137
		HM6167L			70	70		5μ/0.15				●			143
		HM6167L-6			85	85						●			143
		HM6167L-8			100	100						●			143
		HM6167H-45			45	45		0.1m/0.2		●	●	●			147
		HM6167H-55			55	55				●	●	●			147
		HM6167HL-45			45	45		5μ/0.2				●			158
		HM6167HL-55			55	55						●			158
		HM6267-35**			35	35		0.1m/0.25				●			162
		HM6267-45**			45	45						●			162

(continued)

Mode	Total Bit	Type No.	Process	Organization (Word × bit)	Access Time (ns)max	Cycle Time (ns)min	Supply Voltage (V)	Power Dissipation (W)	Package*						Page
									Pin No.	CG	G	P	FP	SP	
Static	64k-bit	HM6264-10	CMOS	8192×8	100	100	+5	0.1m/0.2	28			●			166
		HM6264-12			120	120						●	●		166
		HM6264-15			150	150						●	●		166
		HM6264L-10			100	100		10μ/0.2				●			176
		HM6264L-12			120	120						●	●		176
		HM6264L-15			150	150						●	●		176
		HM6287-55*		65536×1	55	55		0.1m/0.3	22	●		●			188
		HM6287-70*			70	70				●		●			188
		HM6287L-55*			55	55		10μ/0.3				●			189
		HM6287L-70*			70	70						●			189
Psude Static	256k-bit	HM65256-15*	CMOS	32768×8	150	150	+5	7m/0.3	28			●			190
		HM65256-20*			200	200						●			190
Dynamic	64k-bit	HM48416A-12	NMOS	16384×4	120	230	+5	20m/0.3	18			●			192
		HM48416A-15			150	260						●			192
		HM48416A-20			200	330						●			192
		HM4864-2		65536×1	150	270		20m/0.33	16		●	●			199
		HM4864-3			200	335					●	●			199
		HM4864A-12			120	220		20m/0.25		●	●	●			209
		HM4864A-15			150	260				●	●	●			209
		HM4864A-20			200	330				●	●	●			209
	256k-bit	HM50256-12		262144×1	120	220		20m/0.35			●	●			219
		HM50256-15			150	260					●	●			219
		HM50256-20			200	330					●	●			219
		HM50257-12			120	220		20m/0.35			●	●			226
		HM50257-15			150	260					●	●			226
		HM50257-20			200	330					●	●			226

• Under development •• Preliminary △HM6116LP／LFP Series : 10μW

† The package codes of CG, G, P, FP and SP are applied to the package materials as follows.
CG : Glass-sealed Caramic Leadless Chip Carrier, G : Cerdip, P : Plastic DIP,
FP : Flat Plastic Package (SOP), SP : Skinny Type Plastic DIP

■MOS ROM

Mode	Total Bit	Type No.	Process	Organization (Word × bit)	Access Time (ns)max	Supply Voltage (V)	Power Dissipation (W)	Package † Pin No.	C	G	P	FP	Page
Mask	64k-bit	HN61364	CMOS	8192×8	250	+5	5μ/50m	28			●	●	234
		HN61364H**			200						●		236
		HN61365			250			24			●		237
		HN61366			250						●		239
	128k-bit	HN613128		16384×8	250		5μ/50m	28			●	●	241
		HN613128H**			200						●		243
	256k-bit	HN61256		32768×4 or 65536×4	3500		5μ/7.5m				●	●	244
		HN613256		32768×8	250		5μ/50m				●	●	246
		HN613256H**			200						●		248
	1M-bit	HN62301**		131072×8	350		2m/75m				●		249
U. V. Erasablce & Electrically	32k-bit	HN482732A-20	NMOS	4096×8	200	+5	0.18/0.8	24		●			254
		HN482732A-25			250					●			254
		HN482732A-30			300					●			254
	64k-bit	HN482764		8192×8	250		0.18/0.55	28		●			258
		HN482764-2			200					●			258
		HN482764-3			300					●			258
		HN27C64-15	CMOS		150		0.55m/0.17			●			267
		HN27C64-20			200					●			267
		HN27C64-25			250					●			267
		HN27C64-30			300					●			267
	128k-bit	HN4827128-25	NMOS	16384×8	250		0.18/0.53			●			272
		HN4827128-30			300					●			272
		HN4827128-45			450					●			272
	256k-bit	HN27256-25**		32768×8	250		0.22/0.55			●			280
		HN27256-30**			300					●			280
One Time Electrically	64k-bit	HN482764-3	NMOS	8192×8	300	+5	0,18/0.55	28			●		263
	128k-bit	HN4827128-30**		16384×8	300		0.18/0.53				●		276
Electrically Erasable & Programmable	64k-bit	HN58064-25**	NMOS	8192×8	250	+5	0.22/0.55	28			●		284
		HN58064-30**			300						●		284
		HN58064-45**			450						●		284

• Under development ** Preliminary

† The packade codes of G, P and FP are applied to the packge material as follows.
G : Cerdip, P : Plastic DIP, FP : Plastic Flat Package

■BIPOLAR RAM

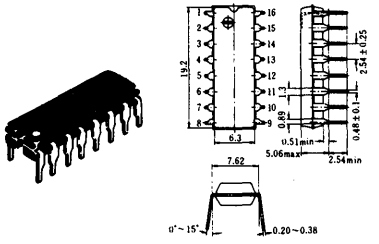
Level	Total Bit	Type No.	Organization (word×bit)	Output	Access Time (ns)max	Supply Voltage (V)	Power Dissipation (mW/bit)	Package† Pin No.	F	G	CC	Replacement	Page
ECL 10K	256	HM10414	256×1	Open Emitter	10	−5.2	2.8	16		●		F10414	290
		HM10414-1			8					●			290
	1K	HM2110	1024×1		35		0.5			●		F10415	294
		HM2110-1			25					●		F10415A	294
		HM2112			10		0.8			●			298
		HM2112-1			8					●			298
		HM10422	256×4		10		0.8	24		●		F10422	303
		HM10422-7			7		1.0			●			308
	4K	HM10470	4096×1		25		0.2	18		●		F10470	311
		HM10470-1			15					●			311
		HM10470-20			20		0.25			●			316
		HM2142			10		0.3	20		●			319
		HM10474	1024×4		25		0.2	24		●		F10474	322
		HM10474-8•			8		0.3			●			327
		HM10474-10•			10					●			327
	16K	HM10480	16384×1		25		0.05	20	●	●		F10480	330
		HM10480-15•			15		0.06			●			333
		HM10480-20•			20					●			333
		HM10484-15•	4096×4		15		0.06	28		●			336
		HM10484-20*			20					●			336
ECL 100K	1K	HM100415	1024×1		10	−4.5	0.6	16		●	●	F100415	339
		HM100422	256×4		10		0.8	24	●	●	●	F100422	342
	4K	HM100470	4096×1		25		0.2	18		●		F100470	345
		HM100474	1024×4		25		0.2	24	●	●		F100474	348
	16K	HM100480	16384×1		25		0.05	20	●	●		F100480	353
		HM100480-15*			15		0.06			●			356
		HM100480-20*			20					●			356
		HM100484-15*	4096×4		15		0.06	28		●			359
		HM100484-20*			20					●			359

• Under development
† The package codes of F,G and CC are applied to the packge materials as follows.
F : Flat Package, G : Cerdip, CC : Ceramic Leadless Chip Carrier

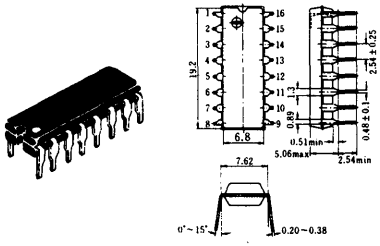
■ PACKAGE INFORMATION (Dimensions in mm)

● Dual-in-line Plastic

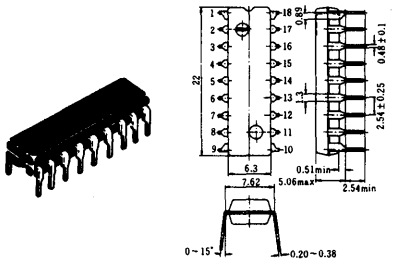
● DP-16



● DP-16A



● DP-18



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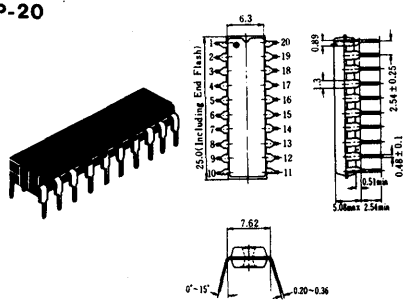
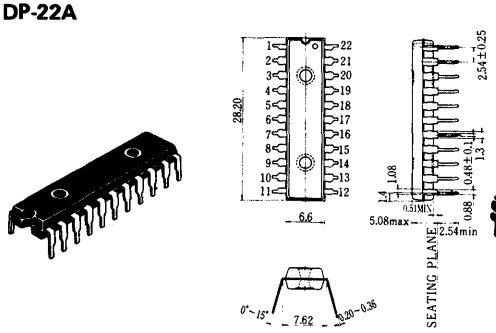
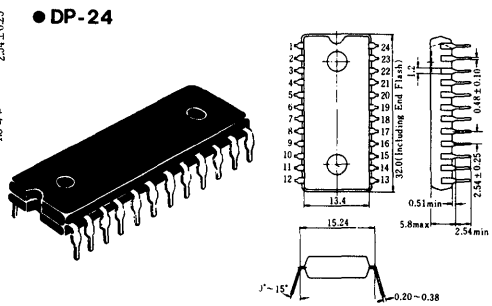


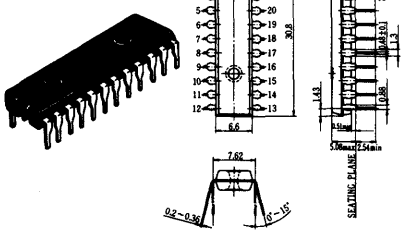
● DP-22A



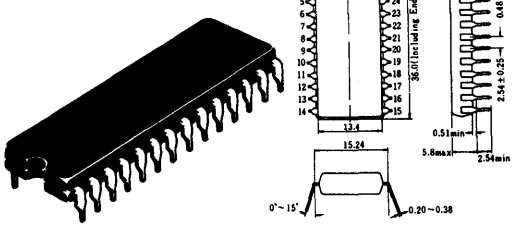
● DP-24



● DP-24A



● DP-28

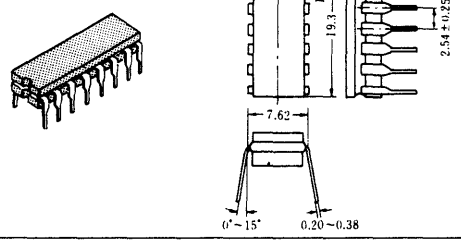


Applicable ICs

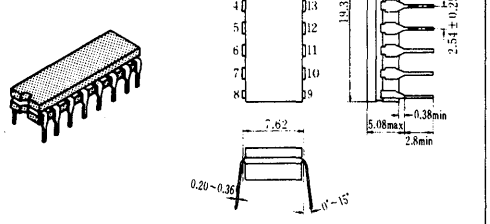
DP-16	HM4864P-2, HM4864P-3, HM4864AP-12, HM4864AP-15, HM4864AP-20
DP-16A	HM50256P-12, HM50256P-15, HM50256P-20, HM50257P-12, HM50257P-15, HM50257P-20
DP-18	HM6148HP-35, HM6148HP-45, HM6148HP-55, HM6148HLP-35, HM6148HLP-45, HM6148HLP-55, HM6147HP-35, HM6147HP-45,HM6147HP-55,HM6147HLP-35,HM6147HLP-45,HM6147HLP-55,HM48416AP-12,HM48416AP-15,HM48416AP-20
DP-20	HM6168HP-45, HM6168HP-55, HM6168HP-70, HM6168HLP-45, HM6168HLP-55, HM6168HLP-70, HM6167P, HM6167P-6, HM6167P-8, HM6167LP, HM6167LP-6, HM6167LP-8, HM6167HP-45, HM6167HP-55, HM6167HLP-45, HM6167HLP-55, HM6267P-35, HM6267P-45
DP-22A	HM6287P-55, HM6287P-70, HM6287LP-55, HM6287LP-70
DP-24	HM6116P-2, HM6116P-3, HM6116P-4, HM6116LP-2, HM6116LP-3, HM6116LP-4, HM6116AP-12, HM6116AP-15, HM6116AP-20, HM6116ALP-12, HM6116ALP-15, HM6116ALP-20, HM6117P-3, HM6117P-4, HM6117LP-3, HM6117LP-4, HN61365P, HN61366P
DP-24A	HM6116ASP-12, HM6116ASP-15, HM6116ASP-20, HM6116ALSP-12, HM6116ALSP-15, HM6116ALSP-20
DP-28	HM6264P-10, HM6264P-12, HM6264P-15, HM6264LP-10, HM6264LP-12, HM6264LP-15, HM65256P-15, HM65256P-20, HN61364P, HN61364HP, HN613128P, HN613128HP, HN61256P, HN613256P, HN613256HP, HN62301P, HN482764P-3, HN4827128P-30, HN58064P-25, HN58064P-30, HN58064P-45

● **CERDIP**

● **DG-16**



● **DG-16A**



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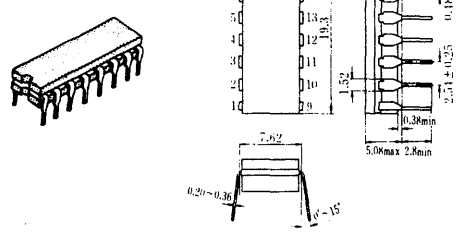
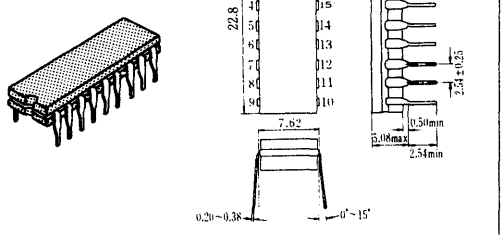
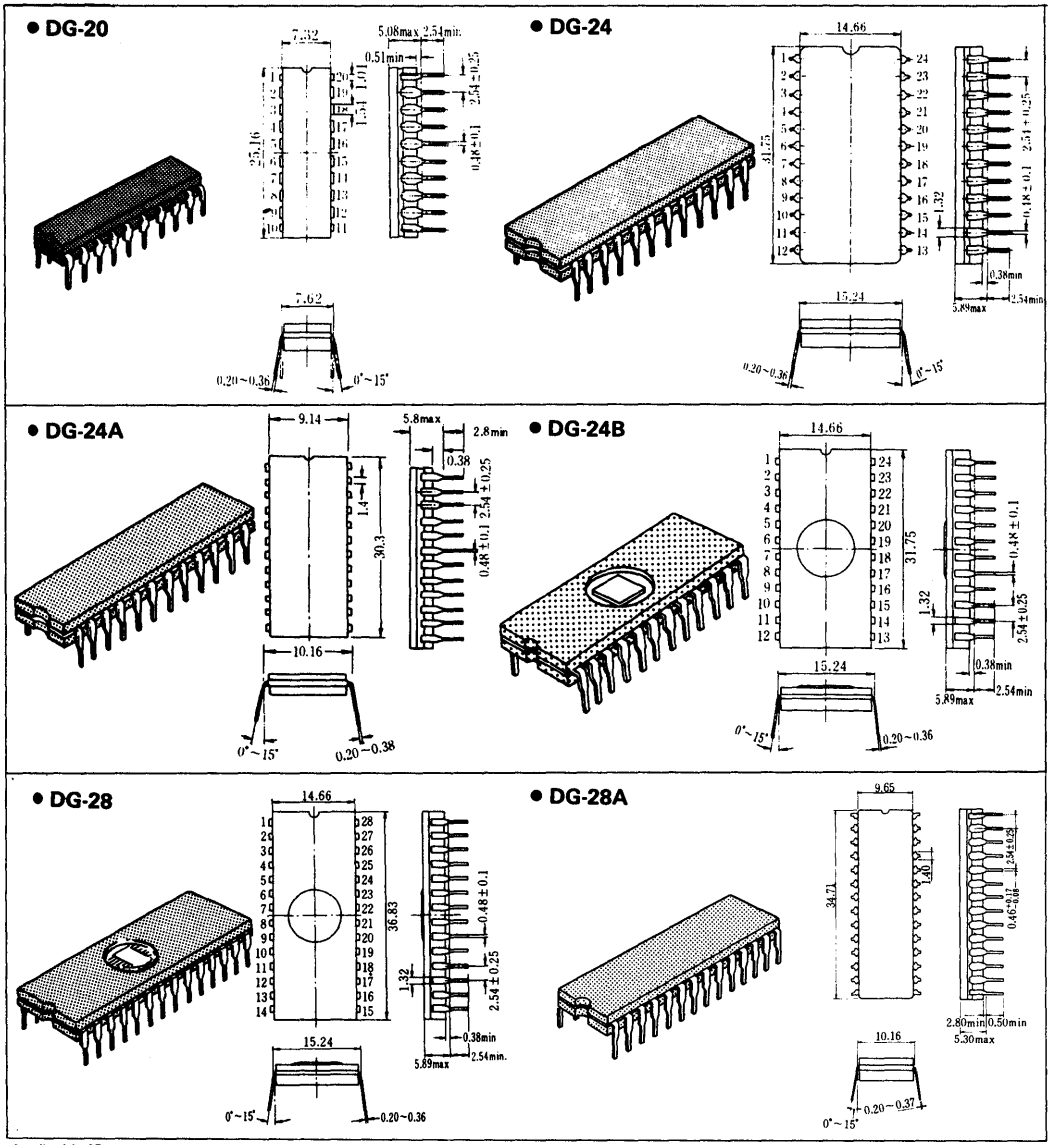


● **DG-18**



(to be continued)

Package Information

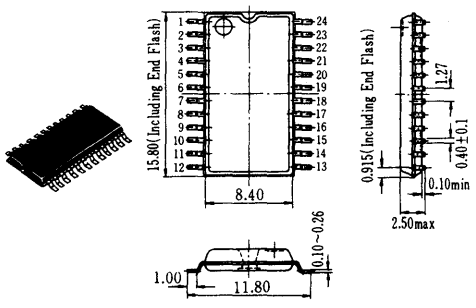


Applicable ICs

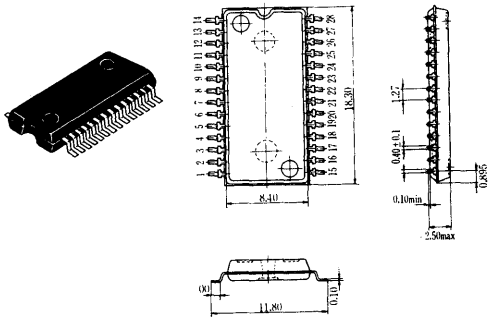
DG-16	HM10414, HM10414-1
DG-16A	HM2110, HM2110-1, HM2112, HM2112-1, HM100415
DG-16B	HM4864-2, HM4864-3, HM4864A-12, HM4864A-15, HM4864A-20, HM50256-12, HM50256-15, HM50256-20, HM50257-12, HM50257-15, HM50257-20
DG-18	HM6148H-35, HM6148H-45, HM6148H-55, HM6147H-35, HM6147H-45, HM6147H-55, HM10470, HM10470-1, HM10470-15, HM100470
DG-20	HM6168H-45, HM6168H-55, HM6168H-70, HM6167, HM6167-6, HM6167-8, HM6167H-45, HM6167H-55, HM2142, HM10480, HM10480-15, HM10480-20, HM100480, HM100480-15, HM100480-20
DG-24	HM6116-2, HM6116-3, HM6116-4, HM6116L-2, HM6116-3, HM6116L-4
DG-24A	HM10422, HM10422-7, HM10474, HM10474-8, HM10474-10, HM100422, HM100474,
DG-24B	HN482732AG-20, HN482732AG-25, HN482732AG-30
DG-28	HN482764G, HN482764G-2, HN482764G-3, HN27C64G-15, HN27C64G-20, HN27C64G-25, HN27C64G-30, HN482718G-25, HN4827128G-30, HN4827128G-45, HN27256G-25, HN27256G-30
DG-28A	HM10484-15, HM10484-20, HM100484-15, HM100484-20

● Surface Mount Packages

● FP-24



● FP-28



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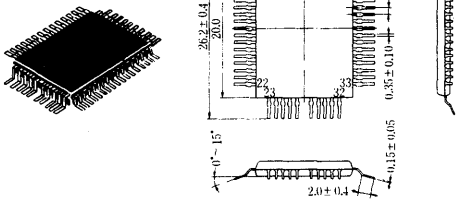
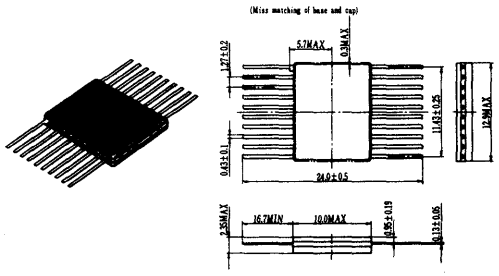
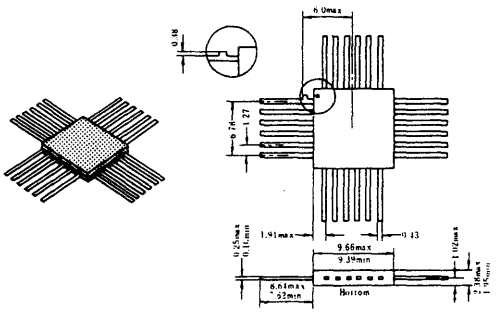


● FG-20



● FG-24

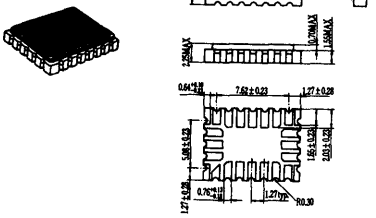


● Applicable ICs

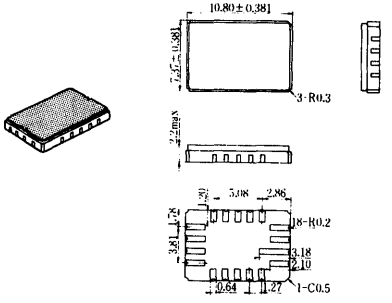
FP-24	HM6116FP-2, HM6116FP-3, HM6116FP-4, HM6116LFP-2, HM6116LFP-3, HM6116LFP-4, HM6117FP-3, HM6117FP-4, HM6117LFP-3, HM6117LFP-4
FP-54	HN61364FP, HN613128FP, HN61256FP, HN613256FP
FG-20	HM10480F, HM100480F
FG-24	HM100422F, HM100474F,

● Surface Mount Packages

● CC-24



● CG-18



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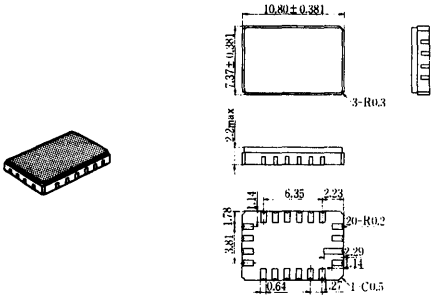
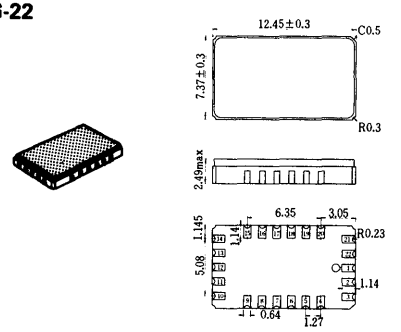
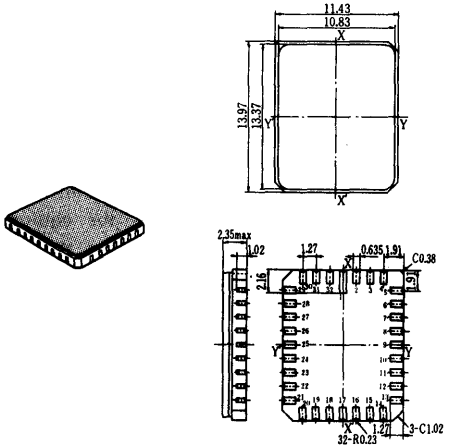


● CG-22



● CG-32



● Applicable ICs

CC-24	HM100415CC, HM100422CC
CG-18	HM4864ACG-12, HM4864ACG-15 HM4864ACG-20
CG-20	HM6167HCG-45, HM6167HCG-55
CG-22	HM6287CG-55, HM6287CG-70
CG-32	HM6116CG-2, HM6116CG-55 HM6116CG-4

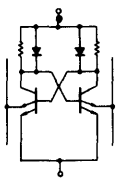
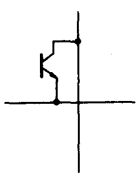
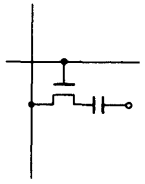
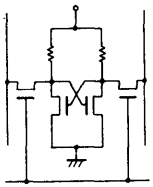
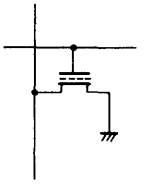
■ RELIABILITY OF HITACHI IC MEMORIES

1. STRUCTURE

IC memories are classified into Bipolar and MOS structural types, with unique, respective characteristics. Bipolar characteristics are high speed and small capacity, while MOS features large capacity.

Produced with the most advanced semiconductor manufacturing technologies, the LSI memory is integrated in high density by unit patterns called "cells." Despite differences in circuit design, pattern layout, and degree of integration, stable product reliability is achieved in the manufacturing process by incorporating past achievements in single cell design, and the proven reliability of each respective technology. Unified production standards are applied in design, manufacture, and inspection stages, and reliability is guaranteed by using TEG (Test Element Group) evaluation. Examples of Bipolar and MOS memory cell circuits are shown in Table 1.

● **Table 1 Examples of Basic Cell Circuit of IC Memories**

Classification	Bipolar memory (RAM)	Bipolar memory (PROM)	NMOS memory (Dynamic RAM)	NMOS, CMOS memories (Static RAM)	NMOS memory (PROM)
Application	Buffer memory, control memory of high-speed computer	Microcomputer control use	Main memory of computer, microcomputer memory		For microcomputer control
Example of basic cell circuit					

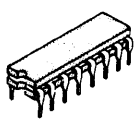
IC memory chips are produced in Ceramic, Cerdip, and Plastic packages. Leadless Chip Carriers (LCC's) for high package density, and Small Outline (SO) packages are currently being developed.

Hermetically sealed Ceramic and Cerdip packaging is suitable for high reliability equipment. Plastic, the leading semiconductor package, is used in a wide variety of applications. Hitachi's improved Plastic package provides a reliability level nearly that of the hermetically sealed Ceramic and Cerdip packages. Table 2 shows examples of IC memory package outlines.

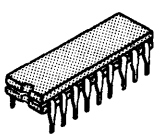
● **Table 2 Examples of IC Memory Package Outlines**

■ Cerdip

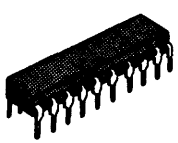
● 16 pin



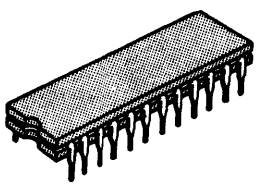
● 18 Pin



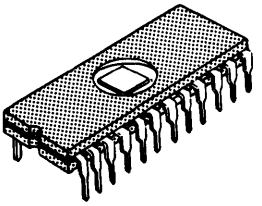
● 20 Pin



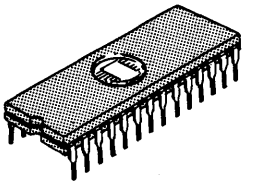
● 24 Pin



- 24 Pin with Lid

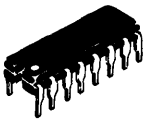


- 28 Pin with Lid

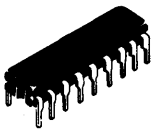


■ Plastic DIP

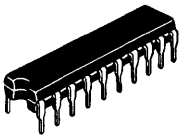
- 16 Pin



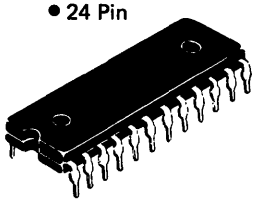
- 18 Pin



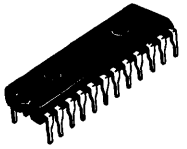
- 20 Pin



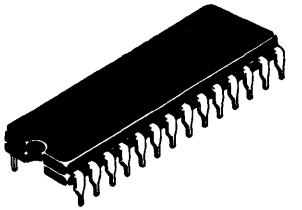
- 24 Pin



- 24 Pin



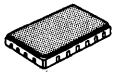
- 28 Pin



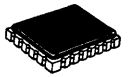
■ Leadless Chip Carrier

- 18 Pin

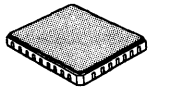
- 20 Pin



- 24 Pin

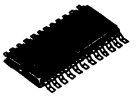


- 32 Pin

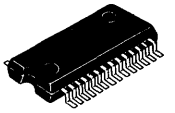


■ SOP

- 24 Pin



- 28 Pin



2. RELIABILITY DATA

2.1 Reliability test data on Bipolar memories

Reliability test data is shown in Tables 3 and 4. Since unified design and quality control standards are applied in the manufacturing process, reliability is assured in all device types. Results have further indicated that the greater the device capacity, the higher the reliability per bit.

• Table 3 Results on Bipolar Memory Reliability Tests (1)

Test item	Test condition	HM10470 Cerdip				HM100422 (Chip Carrier)			
		Samples	Total component hours	Failures	Failure rate*	Samples	Total component hours	Failures	Failure rate*
High-temperature (Operating)	T_a = 125°C V_{EE} = −5.2V (HM10470)	125	C.H. 4.0×10^5	0	l/hr 2.3×10^{-6}	–	–	–	–
	T_a = 150°C V_{EE} = −5.2V (HM10470) V_{CC} = −5.0V (HM100422)	80	2.7×10^5	0	3.4×10^{-6}	40	4×10^4	0	2.3×10^{-5}
High-temperature storage	T_a = 200°C	27	2.7×10^4	0	3.4×10^{-5}	40	4×10^4	0	2.3×10^{-5}
	T_a = 295°C	20	2.0×10^4	0	4.6×10^{-5}	40	4×10^4	0	2.3×10^{-5}

* Estimated failure rate with confidence level 60%.

• Table 4 Result on Bipolar Memory Reliability Tests (2)

Test item	Test condition	HM10470 (Cerdip)		HM100422 (Chip carrier)	
		Samples	Failures	Samples	Failures
Temperature cycling	−65°C ~ +150°C, 10 cycles	120	0	40	0
Soldering heat	260°C, 10 seconds	22	0	–	–
Thermal shock	0°C ~ +100°C, 10 cycles	36	0	20	0
Mechanical shock	1500G, 0.5ms, Three times each for X, Y and Z	30	0	60	0
Variable frequency	100 ~ 2000Hz, 20G Three times each for X, Y and Z	40	0	60	0
Constant-acceleration	20000G, 1 minute, each for X, Y and Z	40	0	60	0

2.2 Reliability test data on MOS Memories

Tables 5, 6 and 7 depict reliability test data on a representative group of MOS memory types—HM50256 256K DRAM, HM4864AP 64K DRAM, HM6264P 64K SRAM, HM6116/FP 16K SRAM, HN4827128 128K EPROM, and leadless chip carrier devices in the 64K DRAM and 4K/16K SRAM product lines.

• Table 5 Results on MOS Memory Reliability Test (1)

Test item	Test Condition	HM50256 (Ceramic)				HN4827128G (Cerdip)				Remarks
		Samples	Total component hours	Failures	Failure rate*	Samples	Total component hours	Failures	Failure rate*	
High-temperature dynamic operation	T_a = 125°C V_{CC} = 5.5V t_{cyc} = 3μs	–	–	–	l/hr –	100	1.0×10^5	0	l/hr 9.2×10^{-6}	
	T_a = 150°C V_{CC}=8V/7V t_{cyc} = 3μs	723	1.44×10^6	7	5.8×10^{-6}	–	–	–	–	Oxide failure x 7
	T_a = 125°C V_{CC}=8V/7V t_{cyc} = 3μs	2920	1.12×10^6	2	2.8×10^{-6}	–	–	–	–	Oxide failure x 2

*** Estimated failure rate with confidence level 60%.**

● **Table 6 Results on MOS Memory Reliability Tests (2)**

Test item	Test condition	HM4864AP (Plastic)				HM6264P (Plastic)				Remarks
		Samples	Total component hours	Failures	Failure rate*	Samples	Total component hours	Failures	Failure rate*	
					l/hr				l/hr	
High-temperature dynamic operation	T_a = 150°C V_{CC} = 7V t_{cyc} = 3μs	173	1.73×10^5	0	1.3×10^{-6}	–	–	–	–	
	T_a = 125°C V_{CC} = 7V t_{cyc} = 3μs	173	1.73×10^5	0	1.3×10^{-6}	774	8.4×10^5	2	3.7×10^{-6}	Isolation failure x 1 Defective crystal x 1
High-temperature and high-humidity bias	T_a = 85°C RH = 85% V_{CC} = 5.5V	177	1.77×10^5	0	5.2×10^{-6}	304	3×10^5	0	3×10^{-6}	
Pressure cooker	T_a = 121°C RH = 85% storage	22	1.1×10^4	0	8.4×10^{-5}	55	2.2×10^4	0	4.2×10^{-5}	

* Estimated failure rate with confidence level 60%.

● **Table 7 Results on MOS Memory Reliability Tests (3)**

Test item	Test condition	HM50256 (cerdip)		EPROM (Cerdip)		HM6116P		HM6116FP		LCC		Remarks
		Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	
Temperature cycling	−55°C~+150°C 10 cycles	386	0	775	0	5462	0	1838	0	860	0	
Temperature cycling	−55°C~+150°C 1000 cycles	116	0	250	0	100	0	90	0*	445	0	*500 cycles
Thermal shock	−65°C~+150°C 15 cycles	145	0	146	0	38	0	38	0	498	0	
Soldering heat	260°C 10 seconds	50	0	90	0	22	0	297	0	82	0	
Mechanical shock	1500G 0.5ms	38	0	90	0	–	–	–	–	82	0	
Variable frequency	20Hz~2000Hz 20G	38	0	90	0	–	–	–	–	82	0	
Constant-acceleration	20,000G	38	0	90	0*	–	–	–	–	82	0	*6000G

2.3 Reliability of IC memory electrical characteristics

Internal elements of IC memory device types are designed to assure stability of electrical characteristics.

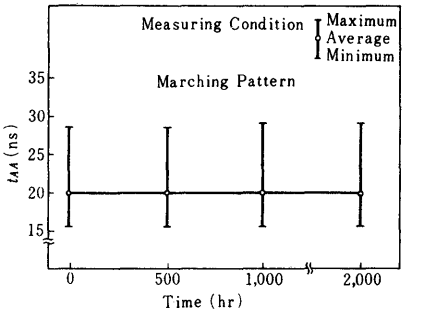
Bipolar access time test data is given in Fig. 1. Dynamic operation test data on 64K DRAM is shown in Fig. 2 and 3.

Fig. 1 Example of Change in Bipolar Memory Characteristics

Example	
Device name	HM10470
Test condition	Ta=125°C, V_{EE}=−5.2V
Failure criteria	t_{AA}=25ns
Failure mechanism	Surface degradation

Results:
Access time (t_{AA}) is stabilized and is within the failure criteria.

Example of time change in access time for Bipolar memory



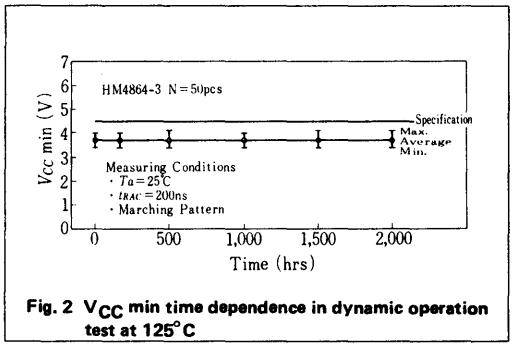


Fig. 2 V_{CC} min time dependence in dynamic operation test at 125°C

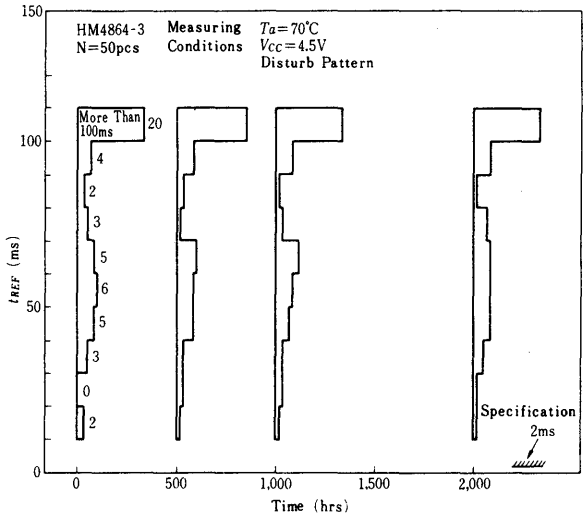


Fig. 3 Time dependence in refresh time (t_{REF}) in dynamic operation test at 125°C

2.4 Classification of failure modes

Examples of field failures are shown in Fig. 4 and 5. Hitachi eliminates latent defects such as pinholes, foreign materials, etc., in each respective stage of production. Process data and field failure data is continuously analyzed, and high temperature burn-in screening is executed to further improve design, manufacture, and reliability.

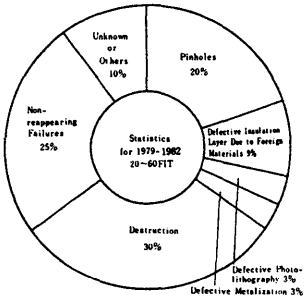


Fig. 4 Classification of Failure Modes of Bipolar Memory in the field

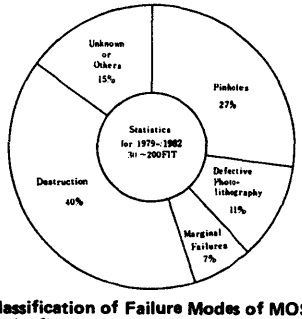


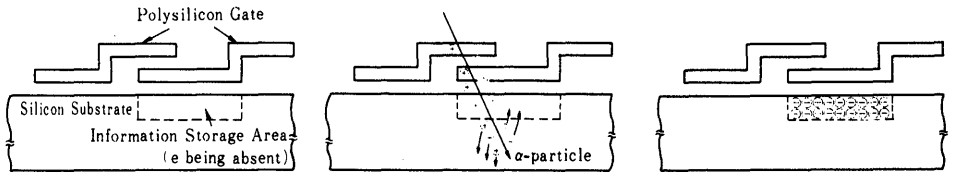
Fig. 5 Classification of Failure Modes of MOS Memory in the field

3. SOFT ERROR

3.1 Soft Error

Miniaturization of IC memories has reduced horizontal and vertical plane dimensions, signal level, and stored charge. One obstacle to further scaling is soft errors—"transitory failures in which normal memory operation can be recovered by reprogramming data." Soft errors are caused by alpha particles emitted from Uranium and Thorium contained in the packaging materials. When memory chips are exposed to alpha particles, many electron-hole pairs are induced in the Si substrate, causing memory data reversion. Fig. 6 shows the mechanism of data reversion in NMOS DRAMs. Negative voltage is applied to the Si substrate. Positive holes are drawn by the substrate, and only electrons cause information reversion (from data "1" to "0") in the memory cell.

Fig. 6 shows a misoperation defined as "Memory cell mode of soft errors," as distinguished from "Bit line mode of soft errors" shown in Fig. 7. As information in a memory cell is read out on the bit line, the bit line potential changes depending on the memory cell data. The change is small (several hundred mV), and compared with standard potential (potential read out from a dummy cell), it is amplified by the sense amplifier. If the bit line is exposed to alpha particles during the short period between read-out from the memory cell and amplification by the sense amplifier, the bit line potential decreases. As the potential becomes less than standard, misoperation occurs from "0" to "1." Both are called "Bit line mode" since errors appear at irradiation of alpha particles. Soft error dependence on cycle time is shown in Fig. 8.

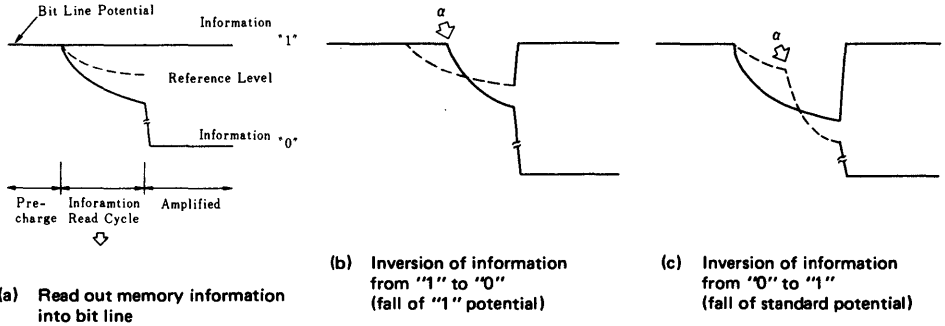


(a) Memory information at "1" (Electrons are absent) (1 Transistor type memory cell)

(b) Incident α-particle generate a large quantity of electron-hole pairs. Generated electrons enter the information storage area and holes are drawn to the substrate power supply.

(c) Inversion of memory information from "1" (electrons "absent") to "0" (electrons "filled")

Fig. 6 Misoperation in Memory Cell



(a) Read out memory information into bit line

(b) Inversion of information from "1" to "0" (fall of "1" potential)

(c) Inversion of information from "0" to "1" (fall of standard potential)

Fig. 7 Misoperation on Bit Line

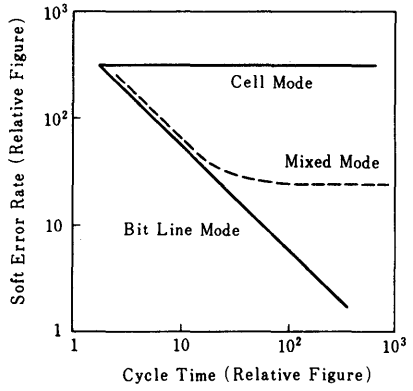


Fig. 8 Soft Error Rate's Dependence on Cycle Time

Actual products will have three types of failure modes—cell mode, bit line mode, and a mixture of both modes. Soft error mechanisms in static MOS and Bipolar memories are different from the above-mentioned mechanisms in dynamic MOS memories.

In static memory, current always flows through the cell to retain data in the flip-flop. When partial current induced by alpha particles exceeds the retention current, misoperation occurs due to reversion of the flip-flop.

3.2 Examples of soft error preventive measures

In 64K DRAM development, accelerated irradiation test data indicated a higher soft error rate than the expected design rate. Hitachi performed the following soft error preventive measures:

(1) Selection of packaging materials which emit minimal alpha particles
(2) Application of chip coating technology to prevent alpha particles from reaching the chip surface.
(3) Use of circuitry and layout technology with inherent ability to resist alpha particles.

As a result of these measures, soft errors in 64K DRAM have reached acceptable levels (Fig. 9). These preventive measures also are applied to other device types, such as the 16K DRAM, single power supply 5V family of products.

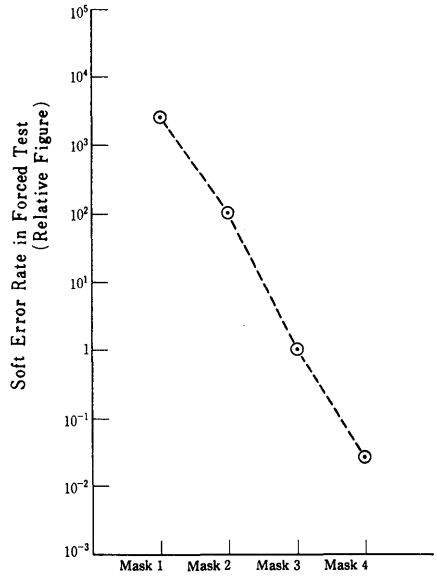


Fig. 9 Example of Soft Error Improvement on 64K-bit Dynamic RAM

3.3 System-level preventive measures

Hitachi's effort to reduce soft errors has resulted in almost trouble-free memories. System-level reliability can be further improved by supplying functions such as ECC for large memory systems, and a parity bit for small systems.

4. RELIABILITY CLASSIFICATION

In designing IC memories, Hitachi classifies memory reliability by the particular device application, and can control the flow of design, production and testing to suit that application.

Reliability can be classified according to the following general applications:

(1) Large scale computers and electronic exchanges
(2) Automotive applications
(3) General communication-industrial use.

When using our memories in any special equipment, please do not hesitate to consult our sales engineering staff regarding reliability in that application.

Precautions given below for handling IC memories will assist the designer in achieving optimum circuit designs, and prevent device malfunction.

1. BIPOLAR IC MEMORY

1.1 Prevention of static electricity

Bipolar memories are considered to have higher resistance to damage by static electricity than MOS ICs. However, presently available high-speed Bipolar memory ICs must be handled with suitable static electricity preventive measures. Since their diffused junctions have become thinner than conventional types in order to perform at high speed, the following measures are recommended:

(1) Keep all device terminals in a conductive mat to maintain equi-potential during transportation and storage. A conductive mat called "MOSPAK" is commercially available. Unless otherwise specified, all Hitachi IC memories are shipped in conductive mats. Memories should be stored in these mats.

(2) When handling IC memories for inspection or connection, grounding must be provided as shown in Fig. 1. The 1M ohm resistor protects the handler from electric shock.

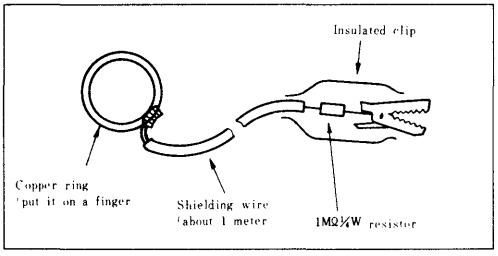


Fig. 1

(3) Control the ambient relative humidity at about 50 per cent.

(4) Wear cotton clothes instead of synthetic fabrics.

(5) Ground all soldering iron tips.

(6) Pack IC memories mounted on circuit boards in conductive mats.

1.2 Prevention of Reverse Insertion

Marking of No. 1 pin is clearly stamped on the device package to prevent incorrect insertion of ICs.

1.3 Mounting and Removal of ICs with Voltage Applied

If ICs are inserted or removed from a board when voltage is applied, the voltage induced at current on/off can destroy the ICs. Mount and remove ICs with power removed. The same precaution is necessary in measurements using a tester.

1.4 Prevention of Oscillation

ECL Bipolar memory has a high transistor cutoff frequency. Sometimes oscillation is caused by the external circuit, and IC misoperation occurs. In such cases, a high frequency capacitor (0.1μF) is recommended between the IC's ground and voltage supply line.

1.5 Precaution on Simple "H" Level of ECL Memories

If an IC's input is grounded to fix input level at "H," misoperation sometimes occurs due to the internal circuit composition. "H" and "L" input levels are specified $V_{IL(min)}$ and $V_{IH(max)}$, respectively. Please refer to these specifications to properly utilize ICs.

1.6 Cooling

The power dissipation of Bipolar memories is 400mW to 1000mW, depending on the device. When many Bipolar memories are mounted on a board, forced air cooling may be required. In addition, cooling will improve reliability as shown in Fig. 2. We recommend the junction temperature be kept lower than 85°C to achieve high reliability.

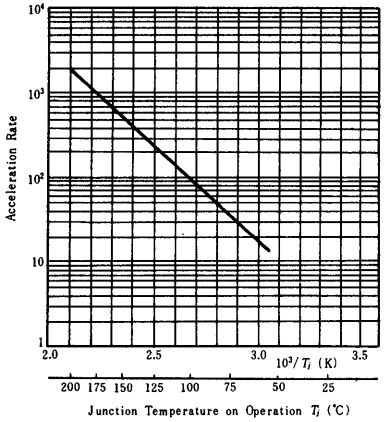


Fig. 2 Example of derating of ECL

1.7 Other Precautions

(1) Deforming of magazine and carrier:
Plastic magazine and carrier material for ECL flat packages is usually thermo-plastic, which deforms at temperatures higher than 40 to 50°C. If burn-in occurs in the field, use an aluminum magazine or other metal type fixture.

(2) Shock in transportation:
Normal handling tests and drop tests (JIS-C7021 A-8) on individual glass-sealed devices indicate no damage. However, strong shock received during transportation or loading of devices packed in magazines may cause damage. Even after devices are board-mounted, IC packages may be damaged if the board strength is insufficient to withstand strong deforming stress. Please contact Hitachi or its representatives regarding handling and transportation of Hitachi devices.

2. MOS IC MEMORY

2.1 Prevention of Static Electricity

The preventive measures referred to in Paragraph 1.1 should also be followed for MOS memories.

2.2 Reducing Power Source Noise

Current spikes can create a power source noise in dynamic memories. Since MOS memories are accessed while being refreshed, use of large capacitors is recommended (a 10μF capacitor for every 9 pieces of 64K-bit HM4864P, as well as an 0.1μF high-frequency capacitor for each memory).

2.3 Assessing Memory System Designs

When evaluating system designs, power margin curves (shmoo plots) can be obtained by observing V_{BB} and V_{DD} power levels as they are gradually varied vs. system timing margin. Optimum curves are those which are closest to the margin shown for the memory device itself.

2.4 Parity Bit

Application of MOS static memories to microcomputers has increased because MOS static memory operates from a single 5V power source, without refresh. In some circuit design applications, all bits are used as information bits without a parity bit. However, we recommend adding a parity bit to thoroughly avoid memory error.

2.5 Use with High Voltage

Avoid system operation failure caused by high electrical fields by shielding MOS IC memories from the high voltage source.

1. VIEWS ON QUALITY AND RELIABILITY

Basic views on quality at Hitachi are to meet the individual uers' required quality level and maintain a general quality level equal to or above that of the general market. The quality required by the user may be specified by contract, or may be indefinite. In either case, efforts are made to assure reliable performance in actual operating circumstances. Quality control during the manufacturing process, and quality awareness from design through production lead to product quality and customer satisfaction. Our quality assurance technique consists basically of the following steps:

(1) Build in reliability at the design stage of new product development.
(2) Build in quality at all steps in the manufacturing process.
(3) Execute stringent inspection and reliability confirmation of final products.
(4) Enhance quality levels through field data feed back.
(5) Cooperate with research laboratories for higher quality and reliability.

With the views and methods mentioned above, utmost efforts are made to meet users' requirements.

2. RELIABILITY DESIGN OF SEMICONDUCTOR DEVICES

2.1 Reliability Targets

The reliability target is an important factor in sales, manufacturing, performance, and price. It is not adequate to set a reliability target based on a single set of common test conditions. The reliability target is set based on many factors:

(1) End use of semiconductor device.
(2) End use of equipment in which device is used.
(3) Device manufacturing process.
(4) End user manufacturing techniques.
(5) Quality control and screening test methods.
(6) Reliability target of system.

2.2 Reliability Design

The following steps are taken to meet the reliability targets:

(1) Design Standardization
As for design rules, critical items pertaining to quality and reliability are always studied at circuit design, device design, layout design, etc. Therefore, as long as standardized processing and materials are used the reliability risk is extremely small even in the case of new development devices, with the exception of special requirements imposed by functional needs.

(2) Device Design
It is important for the device design to consider total balance of process, structure, circuit, and layout design, especially in the case where new processes and/or new materials are employed. Rigorous technical studies are conducted prior to device development.

(3) Reliability Evaluation by Functional Test
Functional Testing is a useful method for design and process reliability evaluation of IC's and LSI devices which have complicated functions.

The objectives of Functional Test are:
- Determining the fundamental failure mode.
- Analysis of relation between failure mode and manufacturing process.
- Analysis of failure mechanism.
- Establishment of QC points in manufacturing process.

2.3 Design Review

Design Review is an organized method to confirm that a design satisfies the performance required and meets design specifications. In addition, design review helps to insure quality and reliability of the finished products. At Hitachi, design review is performed from the planning stage to production for new products, and also for design changes on existing products. Items discussed and considered at design review are:

(1) Description of the products based on design documents.
(2) From the standpoint of each participant, design documents are studied, and for points needing clarification, further investigation will be carried out.
(3) Specify quality control and test methods based on design documents and drawings.
(4) Check process and ability of manufacturing line to achieve design goal.
(5) Preparation for production.
(6) Planning and execution of sub-programs for design changes proposed by individual specialists,

for test, experiments, and calculations to confirm the design changes.

(7) Analysis of past failures with similar devices, discussion of methods to prevent them, and planning and execution of test programs to confirm success.

3. QUALITY ASSURANCE SYSTEM

3.1 Activity of Quality Assurance

General views of overall quality assurance in Hitachi are as follows:

(1) Problems in each individual process should be solved in the process. Therefore, at the finished product stage the potential failure factors have been removed.

(2) Feedback of information is used to insure a satisfactory level of ability process.

3.2 Quality Approval

To insure quality and reliability, quality approval is carried out at the preproduction stage of device design, as described in section 2. Our views on quality approval are:

(1) A third party executes approval objectively from the standpoint of the customer.

(2) Full consideration is given to past failures and information from the field.

(3) No design change or process change without QA approval.

(4) Parts, materials, and processes are closely monitored.

(5) Control points are established in mass production after studying the process abilities and variables.

3.3 Quality and Reliability Control at Mass Production

Quality control is accomplished through division of functions in manufacturing, quality assurance, and other related departments. The total function flow is shown in Fig. 2. The main points are described below.

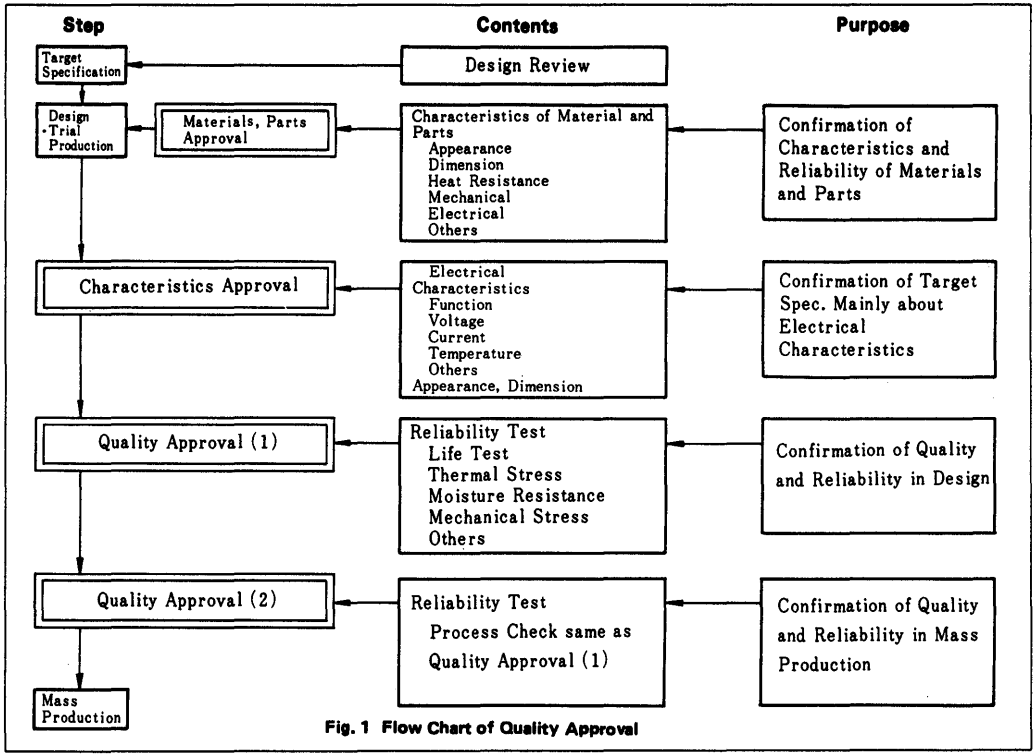


Fig. 1 Flow Chart of Quality Approval

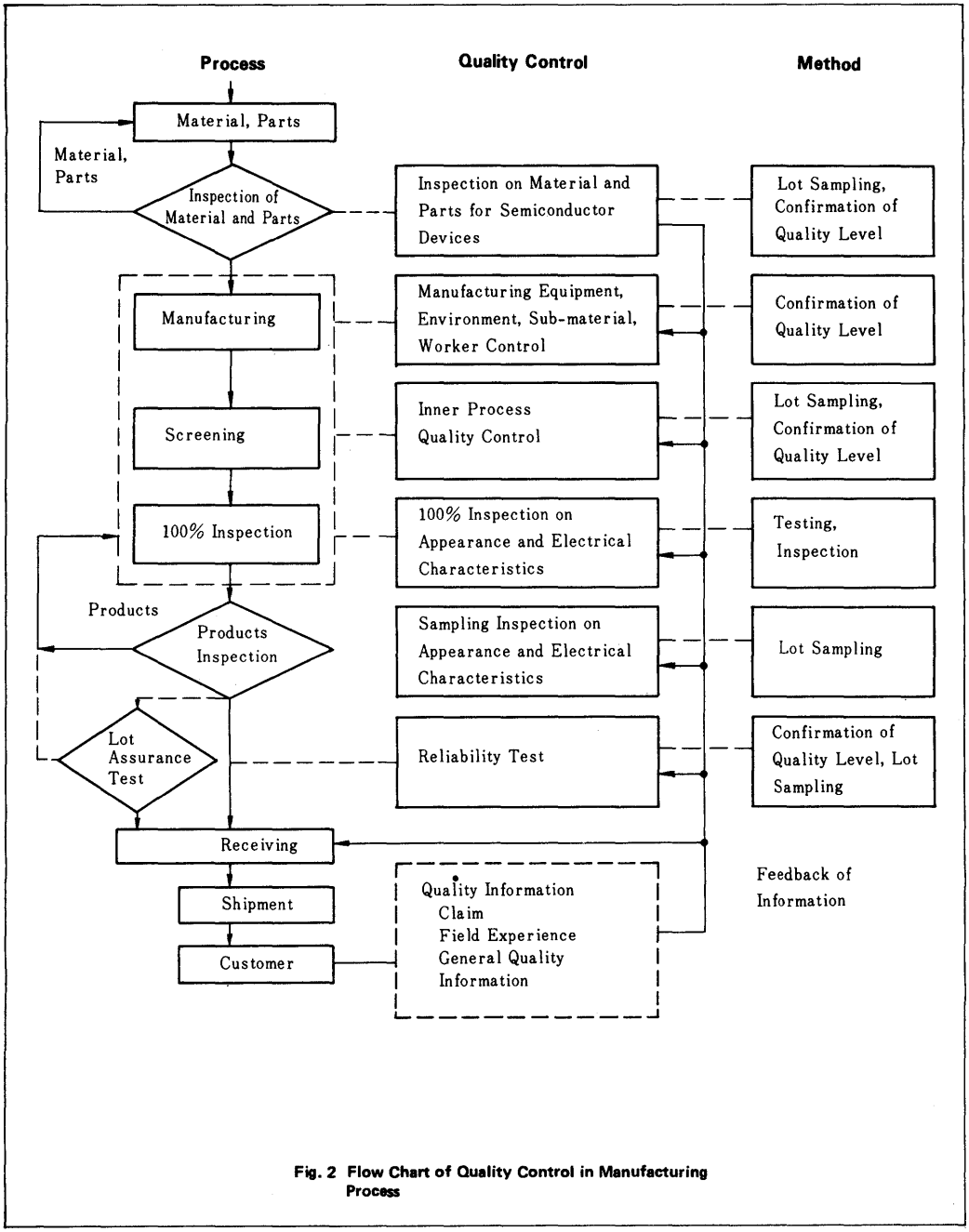


Fig. 2 Flow Chart of Quality Control in Manufacturing Process

3.3.1 Quality Control of Parts and Materials

As semiconductor devices tend towards higher performance and higher reliability, the importance of quality control of parts and materials becomes paramount. Items such as crystals, lead frames, fine wire for wire bonding, packages, and materials needed in manufacturing processes such as masks and chemicals, are all subject to rigorous inspection and control. Incoming inspection is performed based on the purchase specification and drawing. The sampling is executed based mainly on MIL-STD-105D.

The other activities of quality assurance are as follows:

(1) Outside vendor technical information meeting.
(2) Approval and guidance of outside vendors.
(3) Chemical analysis and test.

The typical check points of parts and materials are shown in Table 1.

• Table 1 Quality Control Check Points of Material and Parts (Example)

Material, Parts	Important Control Items	Point for Check
Wafer	Appearance	Damage and Contamination on Surface
	Dimension	Flatness
	Sheet Resistance	Resistance
	Defect Density	Defect Numbers
	Crystal Axis	
Mask	Appearance	Defect Numbers, Scratch
	Dimension	Dimension Level
	Resistoration	
	Gradation	Uniformity of Gradation
Fine Wire for Wire Bonding	Appearance	Contamination, Scratch, Bend, Twist
	Dimension	
	Purity	Purity Level
	Elongation Ratio	Mechanical Strength
Frame	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Processing Accuracy	
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
Ceramic Package	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Leak Resistance	Airtightness
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
	Electrical Characteristics	
	Mechanical Strength	Mechanical Strength
Plastic	Composition	Characteristics of Plastic Material
	Electrical Characteristics	
	Thermal Characteristics	
	Molding Performance	Molding Performance
	Mounting Characteristics	Mounting Characteristics

3.3.2 Inner Process Quality Control

Inner Process Quality Control performs very important functions in quality assurance of semiconductor devices. The manufacturing Inner Process Quality Control is shown in Fig. 3.

(1) Quality Control of Semi-final Products and Final Products

Potential failure factors of semiconductor devices are removed in the manufacturing process. To achieve this, check points are set-up in each process and products which have potential failure factors are not moved to the next process step. Manufacturing lines are rigidly selected and tight inner process quality controls are executed—rigid checks in each process and each lot, 100% inspection to remove failure factors caused by manufacturing variables and high temperature aging and temperature cycling. Elements of inner process quality control are as follows:

- Condition control of equipment and workers environment and random sampling of semi-final products.
- Suggestion system for improvement of work.
- Education of workers.
- Maintenance and improvement of yield.
- Determining quality problems, and implementing countermeasures.
- Transfer of quality information.

(2) Quality Control of Manufacturing Facilities and Measuring Equipment

Manufacturing equipment is improving as higher performance devices are needed. At Hitachi, the automation of manufacturing equipment is encouraged. Maintenance Systems maintain operation of high performance equipment. There are daily inspections which are performed based on related specifications. Inspection points are listed in the specification and are checked one by one to prevent any omission. As for adjustment and maintenance of measuring equipment, specifications are checked one by one to maintain and improve quality.

(3) Quality Control of Manufacturing Circumstances and Sub-Materials

The quality and reliability of semiconductor devices are highly affected by the manufacturing process. Therefore, controls of manufacturing circum-

stances such as temperature, humidity and dust, and the control of submaterials, like gas, and pure water used in a manufacturing process, are intensively executed.

Dust control is essential to realize higher integration and higher reliability of devices. At Hitachi, maintenance and improvement of cleanliness at manufacturing sites is accomplished through attention to buildings, facilities, air conditioning systems, delivered materials, clothes, work environment, and periodic inspection of floating dust concentration.

3.3.3 Final Product Inspection and Reliability Assurance

(1) Final Product Inspection

Lot inspection is done by the quality assurance

Process	Control Point		Purpose of Control
▽Purchase of Material			
Wafer	Wafer	Characteristics, Appearance	Scratch, Removal of Crystal Defect Wafer
○Surface Oxidation	Oxidation		Assurance of Resistance
□Inspection on Surface Oxidation		Appearance, Thickness of Oxide Film	Pinhole, Scratch
○Photo Resist	Photo Resist		
□Inspection on Photo Resist		Dimension, Appearance	Dimension Level
◇PQC Level Check			Check of Photo Resist
○Diffusion	Diffusion	Diffusion Depth, Sheet Resistance	Diffusion Status
□Inspection on Diffusion		Gate Width	Control of Basic Parameters (V_{TH}, etc)
◇PQC Level Check		Characteristics of Oxide Film Breakdown Voltage	Cleaness of surface, Prior Check of V_{IH} Breakdown Voltage Check
○Evaporation	Evaporation	Thickness of Vapor Film, Scratch, Contamination	Assurance of Standard Thickness
□Inspection on Evaporation			
◇PQC Level Check			
□Wafer Inspection	Wafer	Thickness, V_{TH} Characteristics	Prevention of Crack, Quality Assurance of Scribe
□Inspection on Chip Electrical Characteristics	Chip	Electrical Characteristics	
○Chip Scribe		Appearance of Chip	
□Inspection on Chip Appearance			
◇PQC Lot Judgement			
Frame			
○Assembling	Assembling	Appearance after Chip Bonding	Quality Check of Chip Bonding
		Appearance after Wire Bonding	Quality Check of Wire Bonding
◇PQC Level Check		Pull Strength, Compresion Width, Shear Strength	Prevention of Open and Short
□Inspection after Assembling		Appearance after Assembling	
◇PQC Lot Judgement			
Package			
○Sealing	Sealing	Appearance after Sealing Outline, Dimension	Guarantee of Appearance and Dimension
◇PQC Level Check	Marking	Marking Strength	
○Final Electrical Inspection			
◇Failure Analysis		Analysis of Failures, Failure Mode, Mechanism	Feedback of Analysis Information
□Appearance Inspection			
△Sampling Inspection on Products			
○Receiving			
↓Shipment			

Fig. 3 Example of Inner Process Quality Control

department for products which were judged good in 100% test . . . the final process in manufacturing. Though 100% yield is expected, sampling inspection is executed to prevent mixture of bad product by mistake. The inspection is executed not only to confirm that the products have met the users' requirements but also to consider potential quality factors. Lot inspection is executed based on MIL-STD-105D.

(2) Reliability Assurance Tests
To assure the reliability of semiconductor devices, reliability tests and tests on individual manufacturing lots that are required by the user, are periodically performed.

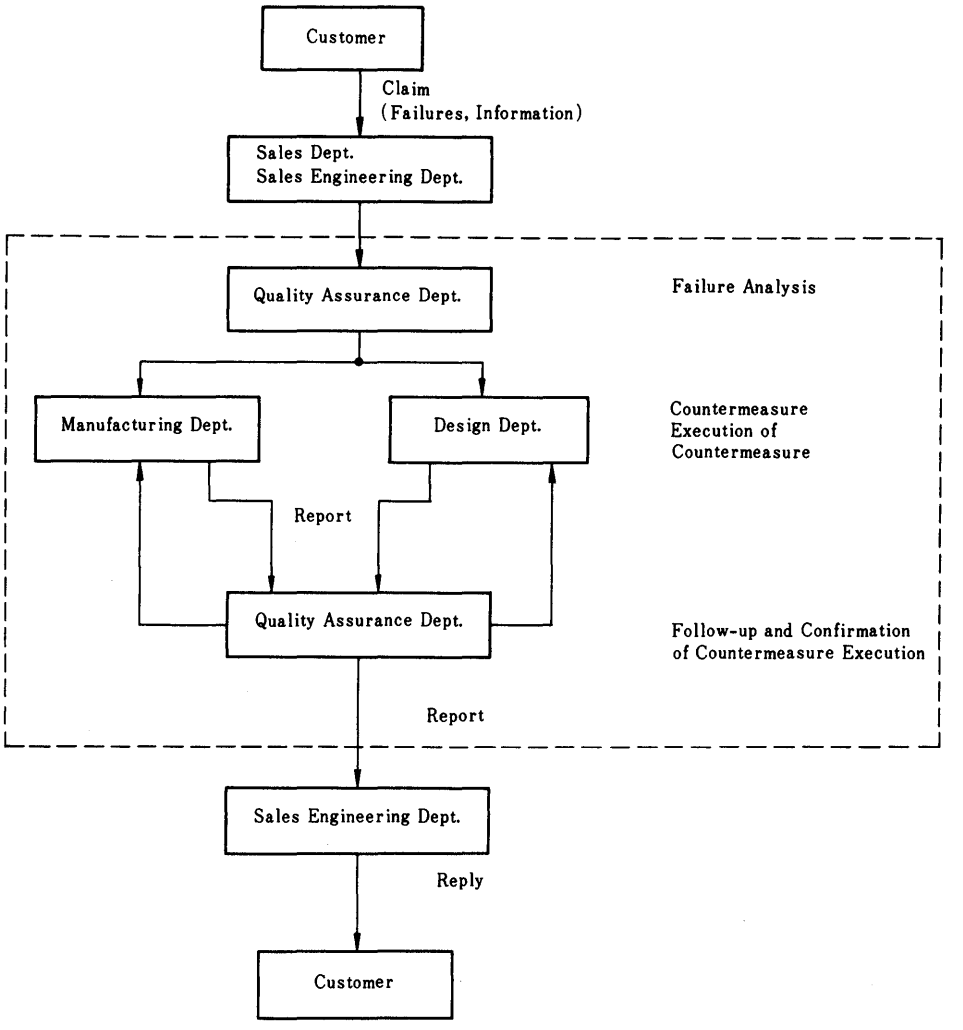


Fig. 4 Process Flow Chart of Field Failure

1. Inspection Methods

Compared to conventional core memories, all peripheral circuits such as decoder, write, and read circuits are contained within an IC memory.

A function test for TTL gates can be performed by a simple DC parameter facility.

IC memory quality cannot be determined by inspecting DC characteristics only, because the number of transistors relating to the DC pin characteristics only amount to 1/1000 of all elements. Systematic electrical inspection of IC memories requires a memory tester which generates an inspection pattern for the IC memory at high speed. When the address input becomes multiplexed, as in 16K memory, even generating the function test pattern becomes a serious problem. The following address patterns are representative of those used to determine whether internal circuits are functioning properly:

(1) All "Low," all "High"
(2) Checker flag
(3) Stripe pattern
(4) Marching
(5) Galloping
(6) Walking
(7) Ping-pong

From many possible address patterns, we have listed a group of patterns convenient for checking the mutual interference of bits, including some with maximum power dissipation. (1) to (4) are N patterns, capable of checking IC memories of N bits with several sequences of N against the IC memory of N bits. (5) to (7) are N^2 patterns which require several sequences of N^2.

A serious problem arises in using the N^2 patterns in large capacity memory. For example, a period of about 30 minutes is required to inspect 16K memory with a galloping pattern. Patterns (1) to (3) are comparatively simple and effective methods, but do not guarantee protection against a failure in the decoder. The simplest pattern for inspecting the necessary memory function is a Marching pattern.

2. Marching Pattern

As its name indicates, this is a pattern in which "1" marches into all bits written "0". The addressing method is explained in the following example for a simple 16-bit memory:

(1) Write "0" for all bits (Fig. 1a).
(2) Read "0" of 0th address and check that read data is "0". Hereafter, "Read" = "checking and judging the data."
(3) Write "1" in the 0th address (Fig. 1b).
(4) Read "0" of 1st address.
(5) Write "1" in 1st address.
(6) Read "0" of nth address.
(7) Write "1" in nth address (Fig. 1c).
(8) Repeat above procedures (6) and (7) up to the last. Finally all data will become "1."
(9) Since all data is "1" in this condition, replace "0" and "1" after procedure (2), and repeat once more up to procedure (8).

It is understood that 5N address patterns are necessary for the N bit memory in this method.

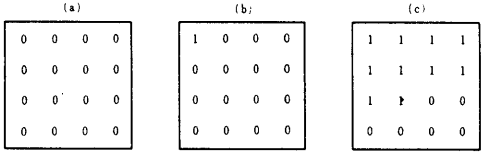


Fig. 1 Addressing method for 16 bits memory in the Marching pattern

3. Generation of Marching Pattern

A method of generating the marching pattern and displaying failed bits on the Braun tube is shown below. Fig. 2 shows the block diagram, with the address pattern generated by four synchronous 4-bit counters. All address patterns are shown in Fig. 4—an example of 16K bit memory. It can be seen that A14, which has half the frequency of the maximum address input A13, is the same as the data input. The A15 signal together with the HD74161 carrier signal is used to determine the sequence termination.

In the read and write cycles shown in Fig. 2, after clearing all bits, addressing is twice the period of clearing. This switching is performed at the binary gate, following the reference pulse generating circuit.

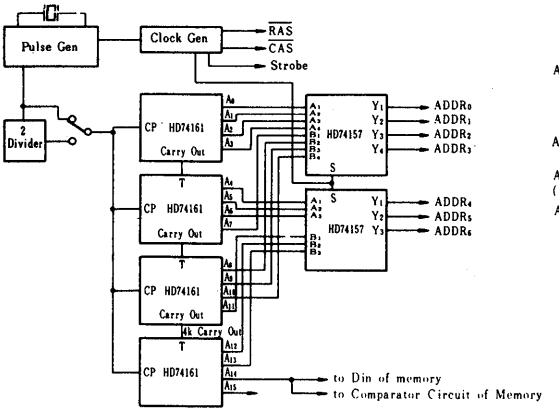


Fig. 2 Marching Pattern Generating Circuit

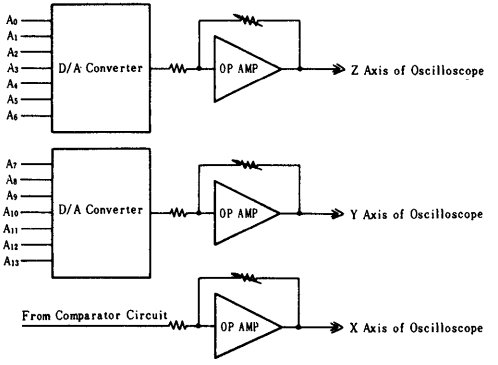


Fig. 3 Fail Bit Map Display Circuit

The output of the HD74161 is input to the D/A converter, and the output of D/A converter is connected to the oscilloscope to display A X-Y matrix. The output of the comparator circuit is connected to the Z axis and performs luminous intensity modulation. In this way, the bit map can be displayed on the CRT.

Fig. 5 shows an example of a voltage margin check. By changing V_{BB}, the increase and decrease of failed bits can be seen. The complicated operation of the memory can be seen dynamically by CRT display, rather than by pulse waveform observed with an ordi-

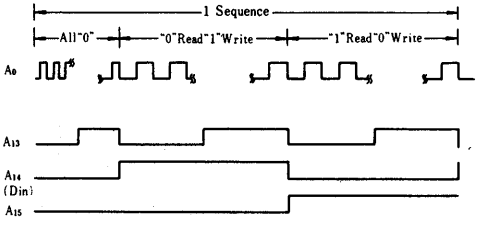
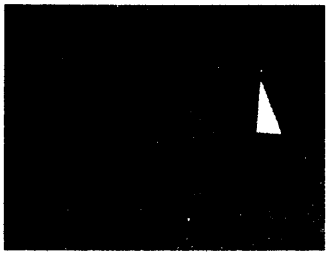
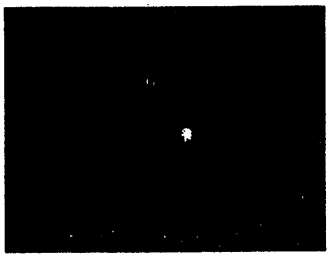


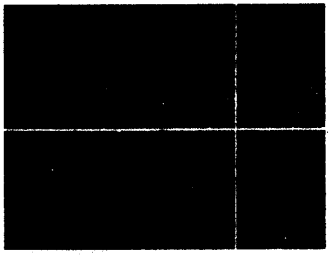
Fig. 4 Entire Pulse Relations



(A)

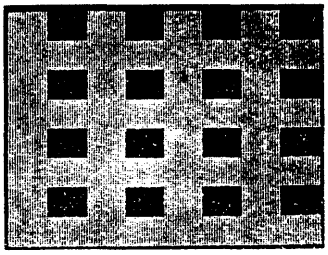


(B)



(C)

Fig. 6 Example of 1 bit solid fail



(D)

Fig. 5 Example of 1 bit solid fail

nary oscilloscope. The bit map as shown in Fig. 5 is extremely useful in observing IC memory operation.

4. Failure Mode

70~90% of failure at user end is called a solid failure—a mode which has no relation to access time, voltage margin and timing. In this failure mode, the memory is not capable of reading from or writing to certain specified bits, which are fixed at "0" or "1". An example of single bit solid failure is shown in Fig. 6. The convenient tester previously described can detect such failures. Except for special cases, it is rarely necessary to perform high-precision measurements such as those made by IC memory manufacturers.

Full inspection of IC memories under adverse conditions, performed by Hitachi, guarantees voltage and timing conditions listed in the data sheet.

An extremely accurate memory tester is required for performing high-precision inspection with 1ns accuracy. Hitachi is developing testers to supply newer high-efficiency memories with excellent characteristics and quality.

1. Power On

When power is applied to a semiconductor memory, power-on current varies with V_{CC} and clock conditions, as shown in Fig. 1. If the rise time of V_{CC} is in the 10μs range, the RAM does not operate dynamically, causing a surge of I_{CC} current. This I_{CC} current surge may be avoided by insuring that V_{CC} rise time is longer than 100μs.

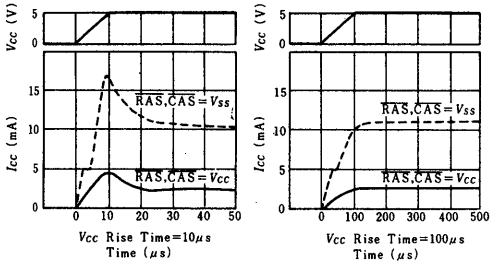


Fig. 1 Relationship between standard value of I_{CC} and V_{CC} during power-up

2. Operation Modes (See Fig. 2)

(1) Read-Cycle:
First decide the X address of the memory cell chosen, and start with trailing of $\overline{RAS}$. When the X address is held by the internal circuitry, change to Y address. Then trail $\overline{CAS}$ to take in the Y address. If the $\overline{WE}$ pin is at high, the output will appear on the Dout pin.

(2) Write Cycle:
The input at Din is written in the memory cell when $\overline{WE}$ turns to low before $\overline{CAS}$.

(3) Read/Modify/Write Cycle:
During this cycle, $\overline{CAS}$ and $\overline{WE}$ are trailed down to low, so that data is read out from, and written in, the same address in the same memory cycle.

(4) Page Mode Cycle:
In this cycle, $\overline{CAS}$ is cyclically moved after taking in the X address through $\overline{RAS}$, to scan only the Y address. This permits reading out and writing in only one column of data at high speed.

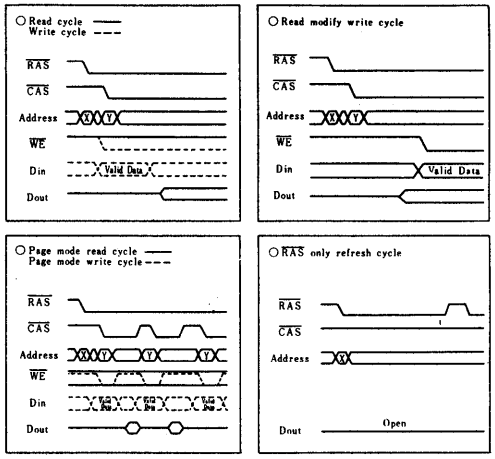


Fig. 2 Operating modes of Dynamic RAMs

2. Data Output

Dout is a TTL-compatible, three-state output with two TTL-load fan out. The output is controlled by the $\overline{CAS}$ signals. In the early write cycle, the output reaches high impedance to permit use as a common I/O terminal.

3. Refresh Cycle

Refresh is a process of periodical rewriting to offset the leakage of charge in the cell, and is implemented in the $\overline{RAS}$ only refresh cycle, and ordinary read cycle. Whether 16K- or 64K-bit, all bits can be refreshed by giving a 128-cycle scanning to only the X addresses between A0 and A6. Each cycle refreshes 128 bits for the 16K-bit DRAM, and 512 bits for the 64K-bit RAM.

The $\overline{RAS}$ only refresh cycle permits a power-efficient refresh that calls for approximately 75% of current consumed by the read cycle. With $\overline{CAS}$ fixed at high, the output reaches high impedance.

The HM4816A has a special function called hidden refresh which allows holding the output by turning $\overline{CAS}$ to low during $\overline{RAS}$ only refresh.

There are two methods of refreshing:
(1) Concentrated—giving a 128-cycle refresh after

operating the memory for a period of 2ms maximum.

(2) Deconcentrated—which repeats a refresh cycle every 16μs, following the initial 16μ memory operation (=2ms/128).

4. Operating Current in Dynamic RAMs

Fig. 3 shows the waveforms of current applied in various operating modes for HM4864. The mean operating current in each mode equals the value obtained by dividing the integrated result of each waveform by the cycle time. The first peak in each mode appears during memory access. On the other hand, the peak during standby appears due to the precharging operation in each circuit.

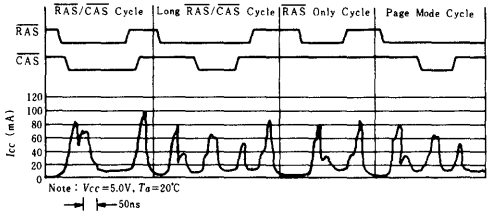


Fig. 3 Power supply voltage (HM4864)

DRAMs show different current peaks, depending upon $\overline{RAS}$ and $\overline{CAS}$ timing. The largest peak appears when both X and Y operate simultaneously. The maximum current peak for HM4864 is approximately 100mA. Current consumed during standby is expressed as a function of cycle time dependency in Fig. 4. During standby, with a once-in-every16μs refresh, HM4864 consumes approximately 3mA current.

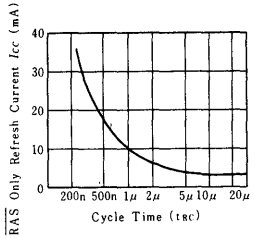


Fig. 4 Cycle time dependence of $\overline{RAS}$ only refresh current (HM4864)

5. Noise

Noise can be classified into power source noise, and input signal noise. The power source noise can be further classified as low- or high-frequency noise as shown in Fig. 5. To assure stable memory operation, peak-to-peak power supply voltage, in the presence of low- or high-frequency noise, should be held below 10% of standard level. To prevent power source noise, we recommend a condenser of 0.1μF for each one or two devices.

Input signal noise can be classified overshoot or undershoot. Overshoot should be held below the highest input level specified. To prevent input-undershoot-induced parasitic transistor effects, a −5V V_{BB} is used (three supply designs) or a built-in V_{BB} bias circuit is included on chip.

Design should provide that the input undershoot does not exceed the minimum specified for V_{IL}. Overshoot and undershoot in DRAMS can be reduced by inserting a damping resistance of several tens of ohms.

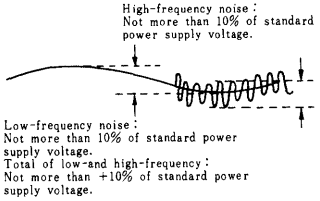


Fig. 5 Power source noise

1. PROGRAMMING AND ERASING EPROMs

1.1 Programming

Information is programmed into the memory cell of an EPROM by applying a high voltage to its drain and gate (Fig. 1 and 2). High voltage at the drain increases the energy of the electrons in the channel area, which become "hot electrons" capable of jumping across the oxide film. Pulled by high voltage at the gate, the hot electrons are admitted into the floating gate. The charge entering the floating gate changes the threshold voltage in the memory element, thereby storing new information.

When reading out, voltage is applied as in Fig. 3, and "1" and "0" are identified by checking whether or not current flows. Since the drain voltage for read-out is set at 3V, no erroneous writing takes place.

When shipped, all EPROM bits are held at logic "1" with all charge released (no programmed data). In changing "1" to "0" by applying the specified waveform and voltage, data is programmed. The higher the V_{PP} voltage, and the longer the program pulse width t_pW, the greater the quantity of electrons programmed in, as shown in Fig. 4.

If V_{PP} exceeds the rated value, as in overshoot, the memory's p-n junction may yield to permanent breakdown. To avoid this, check V_{PP} overshoot of the PROM programmer. Also check negative-voltage-induced noise at other terminals, which can create a parasitic transistor effect and reduce apparent yield.

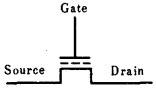


Fig. 1 Memory transistor circuit symbols

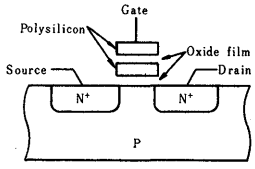


Fig. 2 Cross section of memory transistor

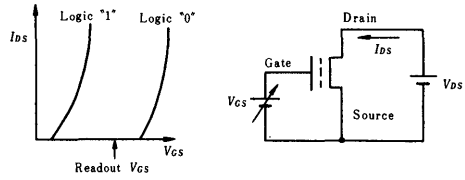
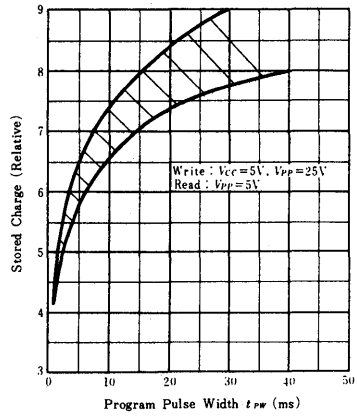


Fig. 3 Reading out stored information



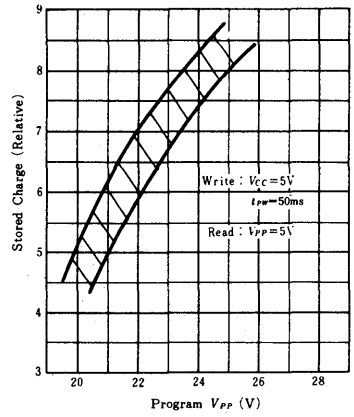


Fig. 4 Typical Programming Characteristics of EPROMs.

1.2 Erasing

Hitachi's EPROMs are usually capable of being written and erased more than 100 times. Data stored in the EPROM is erased by exposing the chip to ultraviolet light, which releases the electric charge from the floating gate. Electrons in the floating gate receive ultraviolet energy, become hot electrons again and jump into the control gate or substrate. This process erases the stored data.

Wavelength and minimum exposure of ultraviolet light are specified as 2,537Å, and 15W sec/cm² respectively. Erasure occurs by exposing a device to an ultraviolet lamp of 12,000μW/cm² at a distance of 1.2~3cm for approximately 20 minutes. The ultraviolet light transmission rate of the transparent lid is about 70%. Contamination or foreign material on the surface—which lowers transmission and prolongs erase time—should be eliminated by the use of alcohol or other solvent that will not damage the package. Fig. 5 shows typical EPROM erasure characteristics.

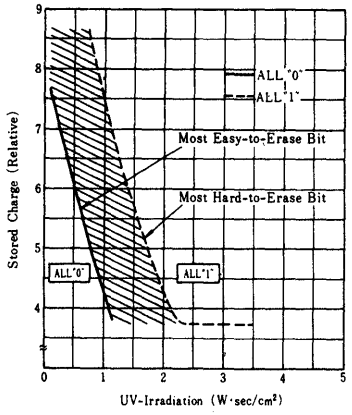


Fig. 5 Typical Erasing Characteristics

1.3 Data Retention

As a result of writing in, approximately 0.5 to 2.0 x 10^{-13} coulomb of electrons are accumulated at the floating gate. With the elapse of time, these electrons decrease, which can result in inversion of stored data. The mechanisms of electron dissipation are explained as follows:

(1) Data Dissipation by Heat
The accumulation of electrons at the floating gate is an unbalanced state, so the dissipation of thermally excited electrons is unavoidable. Data holding time is closely related to temperature. Fig. 6 shows typical data retention characteristics.

(2) Data Dissipation by Ultraviolet Light
Ultraviolet rays at a wavelength of not greater than 3,000~4,000Å will release the charge stored in EPROMs. Prolonged exposure to fluorescent light and sunlight, which contain some ultraviolet rays, can cause data corruption. Fig. 7 shows examples of data retention time using ultraviolet, sunlight, and fluorescent light sources.

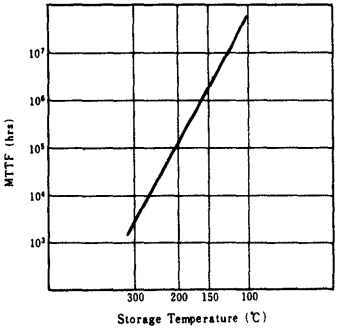


Fig. 6 Typical Data Retention Characteristics

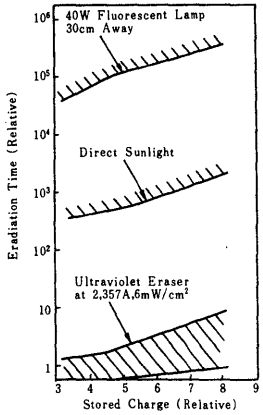


Fig. 7 EPROM's data retention time

(3) Data dissipation by voltage
This type of dissipation occurs while information is being written in. High voltage at other memory cells lying on the same word or data line as the cell being programmed, can cause dissipation of stored electric charge. Such defects are eliminated by inspection at the factory. The programing voltage and pulse width should always be kept within specified limits.

1.4 EPROM Programmer

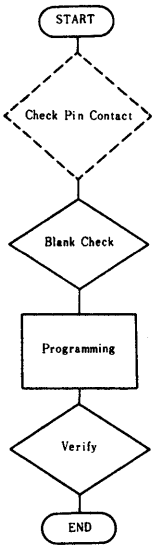
An EPROM Programmer stores program data from a source in its internal RAM, and writes the program data into an EPROM. A minimum of 3 functions are necessary to accomplish this: the Blank check function prior to programming, the Programming function, and the Verify function. As shown in the drawing, programmers also are provided with a reverse insertion checking function, or pin contact checking function, prior to the Blank Check. The diagram is outlined as follows:

(a) Pin contact check
Checking is performed by detecting the forward current of each EPROM pin. This forward biased resistance differs between product manufacturers.

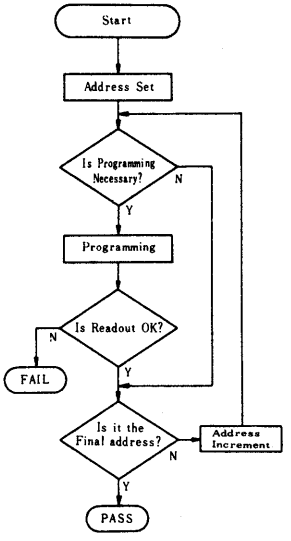
(b) Reverse insertion check
This check detects reverse insertion of the device, places the equipment in reset mode, and protects the device and equipment.

(c) Blank Check
This function is performed prior to programming to determine whether the EPROM is erased, or to prevent EPROM reprogramming. With output data in the erased condition at "1" (high), check whether or not data in the EPROM is also at "1." It will failstop, if any "0" is detected. Normally, a lamp or buzzer provides warning.

(d) Programming
Normal programming flow is shown below. An EPROM data word will be read out prior to programming, and compared with programming data. If they coincide, programming will be skipped; and if they differ, programming will be performed. Read out will be again compared with programming data, and if they coincide, it will progress to the next address.



(e) Verify
This function after programming completion, checks that the programming is correct when compared with data in the internal RAM of the programmer. It performs fail-stop when data does not coincide, lighting the fail lamp, and displaying the address and data.



(f) How to input the program
The following methods are given to input program data to the internal RAM of the programmer. Paper tape input and teletypewriter input are usually options.

Method	Content
Copy input	Input by copying the master ROM.
Manual input	Input by the keyswitch of the front panel. Used for correction or revision of program
Paper tape input	Read the paper tape furnished from the host system with the tape reader
Teletypewriter input	Input with the teletypewriter. Preparation, correction and list preparation of the program can be made.

1.5 Handling EPROMs

Contact with a charged human body, plastics, or dry cloth causes the glass window of an EPROM to generate static electricity which could cause device malfunction. Typical malfunctions are faulty blanking and write margin setting, which give the impression that information has been correctly written in. This malfunction is due to prolonged retention of electric charge on the glass window, resulting from the static electricity. It can be eliminated by neutralizing the charges through short exposure to ultraviolet rays—a procedure recommended before reprogramming, as it also reduces charges in the floating gate. To prevent charging of the window, use the following methods:

(1) Use a grounding system for the operator handling EPROMs, and avoid use of gloves that may develop a static charge.
(2) Refrain from rubbing the glass window with plastics and other substances that may develop a charge.
(3) Avoid use of coolant sprays which contain ions.
(4) Use shielding labels with conductive substances that can evenly distribute the established charge.

1.6 Shielding Labels

When using EPROMs in environments where ultraviolet exposure can occur, put a shield label over the glass window to absorb ultraviolet light. Specially prepared labels are marketed, and metal-loaded types are particularly effective. Few shielding labels meet all environmental requirements established for EPROMs. A suitable label must be chosen for each application by considering the following label characteristics:

(1) Adhesive Strength
Avoid repeated attaching and dusting which may reduce adhesive strength. Ultraviolet erasure and reprogramming are recommended after stripping off an attached label. If labels must be changed, attach the new label over the old, since peeling may develop a static charge.
(2) Temperature Range
Use a shielding label in an environment where temperature falls within the specified allowable range. Beyond this range, label paste may harden, or remain on the window glass even after the label is removed.
(3) Humidity Range
Use a shielding label where humidity does not exceed the specified allowable range.

■MASK ROM PROGRAMMING INSTRUCTION

The writing of custom program codes into mask ROMs is performed by the CAD system, using a large scale computer. ROM code data should conform to specifications given below, using either paper tape, EPROM, or magnetic tape. Additional instructions, such as chip select and customer part number, should be given in the "ROM Specification Identification Sheet."

1. Specification of EPROM

1.1 Submit three sets of EPROM stored Data. In the case of two or four EPROMs, specify the address of the EPROM.

1.2 The ROM Code data is input from the start address to the Final Address in the EPROM.

1.3 Type of EPROM

HN462716 (2K-word x 8-bit, 2716 Compatible)
HN462532 (4K-word x 8-bit, TMS2532 Compatible)
HN462732 (4K-word x 8-bit, 2732 Compatible)
HN482764 (8K-word x 8-bit, 2764 Compatible)
HN4827128 (16K-word x 8-bit, 27128 Compatible)

2. Specification of Magnetic Tape

2.1 The following type of magnetic tape is specified, which can be entered in a magnetic tape device compatible with the IBM magnetic tape device:

(1) Length . 2,400 feet, 1,200 feet, or 600 feet.
(2) Width . . . . . $^1/_2$ inch
(3) Channel . . . . . .9 channels
(4) Bit Density . . . . . .800 BPI or 1,600 BPI
(clearly state bit density in the "ROM Specification Identification Sheet.")

2.2 Use EBCDIC code.

2.3 Follow the format for magnetic tape described as follows:

(1) No leading tape mark
(2) No label
(3) Record size _____ 80 byte/1 record
(4) Block size _____ 10 records/1 block
(5) Indicate end of the file with 2 successive tape marks (TM).

2.4 Ensure that magnetic tapes represent one roll for each chip. Extending the single-chip portion over several rolls is unacceptable.

2.5 Data Mode

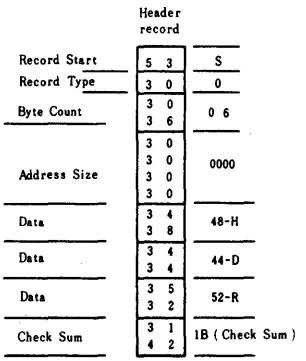
2.5.1 HMCS6800 Load Module Mode

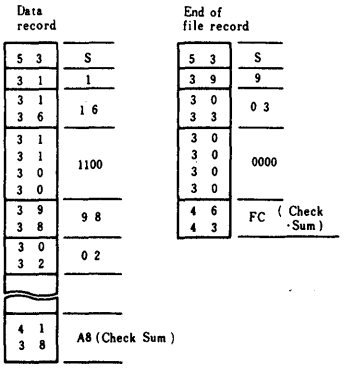
This mode is the object mode output from the HMCS6800 assembler.

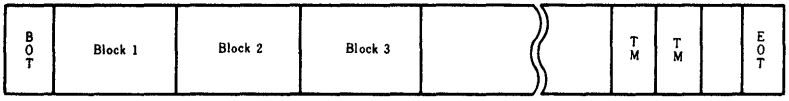
(1) Divide the 8-bit code into the upper and lower 4-bit codes, and convert each into hexadecimal notations. Example: The code of 1100 0110 is as follows under binary notation:

(Upper 4 bits) $D_7\ D_6\ D_5\ D_4$	(Lower 4 bits) $D_3\ D_2\ D_1\ D_0$	Bit weight (ROM output equivalence)
1 1 0 0	0 1 1 0	

(2) The actual load module mode is shown as follows:







S0 indicates the head of the file, and S9 indicates the end of the file. The actual data enters following S1 or from the address (hexadecimal) indicated in the address size. The address of the data recorder address is compared with the next data recorder address, by counting in 1-byte increments, and checking whether or not it is sequential. Where the address is skipped, 00 or FF data enters hexadecimally. A printed example on paper tape for the HMCS6800 load module mode is as follows:

Example

```
Header Record →S00B000058204558414D504CB5
Data Record   →S113F0007EF5587EF7897EFAA77EF9C07EF9C47E24
Data Record   →S112F010FA657EFA8B7EFAA07EF9DC7EFA247E06
End of
File Record   →S9030000FC
```

(3) In case the address is skipped, it should be entered into the "ROM Specification Identification Sheet" that the skipped address and data (00 or FF) entered into the skipped address by hexadecimal notation.

2.5.2 BNPF Mode

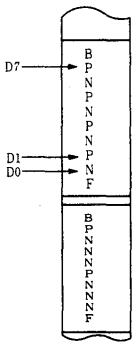
(1) One word is symbolized by the word start mark B, the bit content represented by 8 characters of P and N, and the BNPF slice composed of successive 10 characters of the word end mark F.

(2) The contents from F of one BNPF slice up to B of the next BNPF slice are ignored. The code of AA by hexadecimal notation is symbolized in the example shown below.

2.5.3 The bit pattern (PNPF slice) must be designated on all ROM addresses. Therefore, the ROM head address is 0 on the "ROM Specification Identification Sheet."

B . . . . . .Indicates starts of 1 word.
N. . . . . .Indicates "0" of 1 bit data.
P. . . . . .Indicates "1" of 1 bit data.
F. . . . . .Indicates end of 1 word.

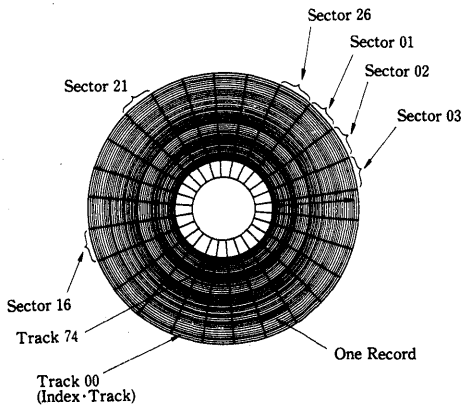
Example



3. Specification of Floppy Disk

3.1 Use the following type of Floppy Disk

(1) Type . 8 Inch Single Sided and Single Density.
(2) Number of Sector 26
(3) Number of Track 77



3.2 Use the EBCDIC code as the use code.

3.3 Make the format of the floppy disk as described below.

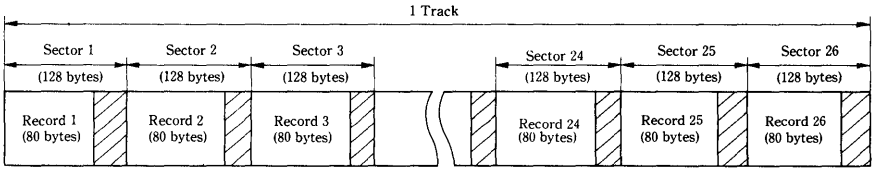
(1) Composition

No.	Item	Location	
		Track	Sector
1	Standard Volume Label	00	07
2	Standard Head Label	00	08 ~ 26
3	Data Area	01 ~ 73	01 ~ 26
4	Alternal Track	75, 76	01 ~ 26
5	Spare Track	00 74	01 ~ 06 01 ~ 26

(2) Record size . . . . . 80 byte/1 record
(3) Use the sector as below. Use one sector for one record, that is 80 bytes out of 128 bytes used for one record.

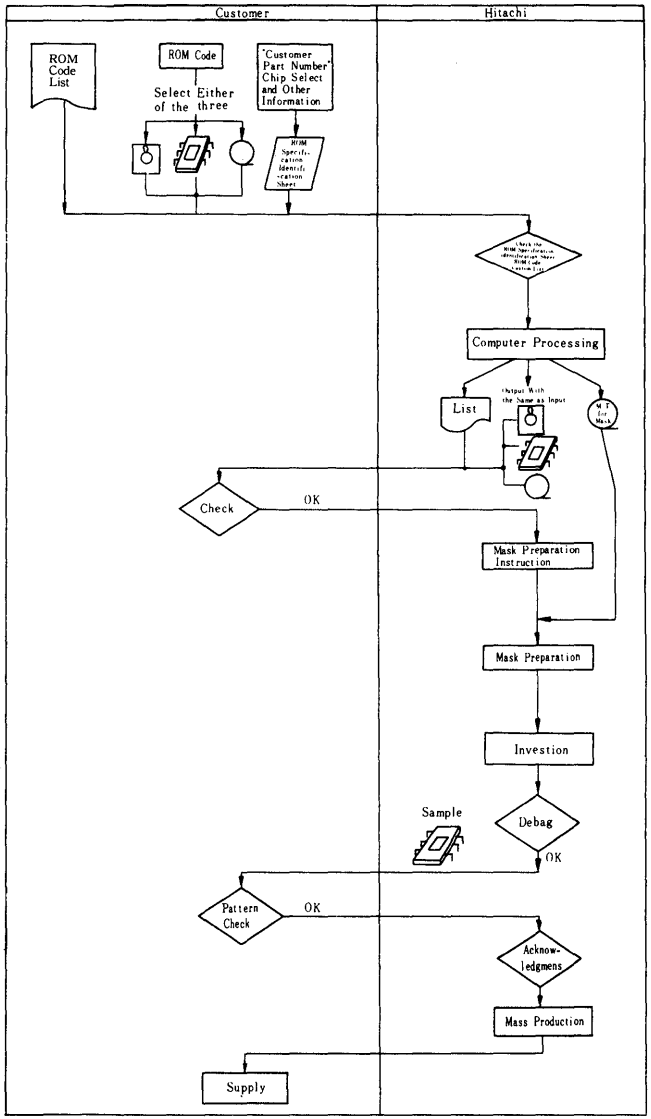
3.4 Data Mode

See 2.5



: unuse

Mask ROM Development Flowchart



DATA SHEETS

MOS STATIC RAM

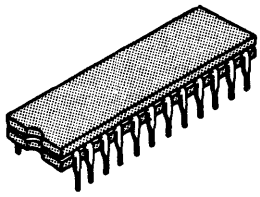
HM6116-2, HM6116-3, HM6116-4
HM6116P-2, HM6116P-3, HM6116P-4

2048-word×8-bit High Speed Static CMOS RAM

■FEATURES

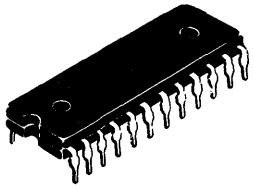
- Single 5V Supply and High Density 24 Pin Package
- High speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation Standby: 100μW (typ.) Operation: 180mW (typ.)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

HM6116-2, HM6116-3, HM6116-4



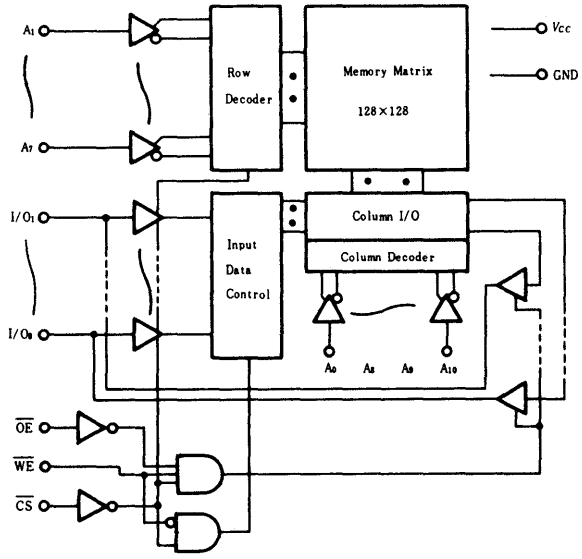
(DG-24)

HM6116P-2, HM6116P-3, HM6116P-4

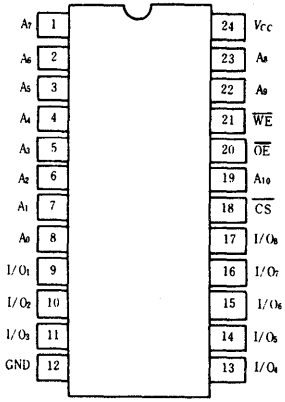


(DP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns : −3.5V

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−3.0*	—	0.8	V

* Pulse Width : 50ns, DC : V_{IL} min=−0.3V

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test Conditions	HM6116/P-2			HM6116/P-3/-4			Unit
			min	typ*	max	min	typ*	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	—	—	10	—	—	10	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH}, $V_{I/O}$=GND to V_{CC}	—	—	10	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	—	40	80	—	35	70	mA
	I_{CC1}**	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	—	35	—	—	30	—	mA
Average Operating Current	I_{CC2}	Min. cycle, duty=100%	—	40	80	—	35	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	—	5	15	—	5	15	mA
	I_{SB1}	$\overline{CS}$≧V_{CC}−0.2V, V_{in}≧V_{CC}−0.2V or V_{in}≦0.2V	—	0.02	2	—	0.02	2	mA
Output Voltage	V_{OL}	I_{OL}=4mA	—	—	0.4	—	—	—	V
		I_{OL}=2.1mA	—	—	—	—	—	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	V

* V_{CC}=5V, Ta=25°C
** Reference Only

■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C)

●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

●READ CYCLE

Item	Symbol	HM6116/P-2		HM6116/P-3		HM6116/P-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

● WRITE CYCLE

Item	Symbol	HM6116/P-2		HM6116/P-3		HM6116/P-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

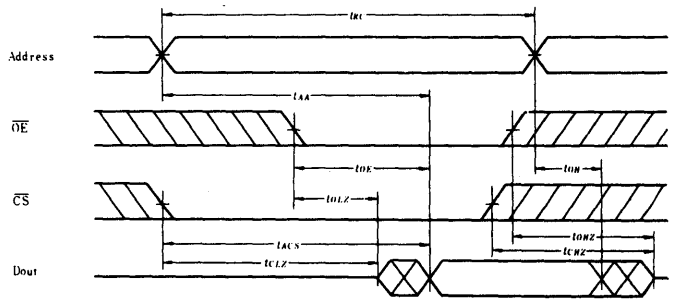
■ CAPACITANCE (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

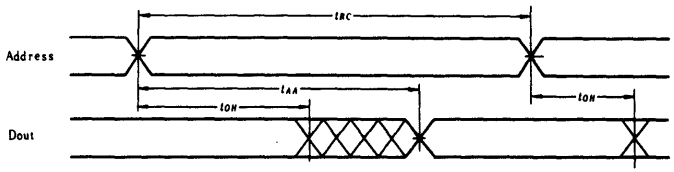
Note) This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

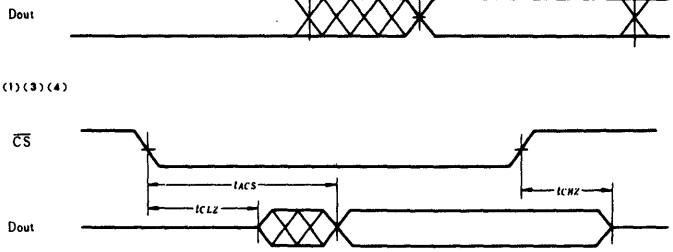
● READ CYCLE (1)[1]



● READ CYCLE (2)[1][2][4]

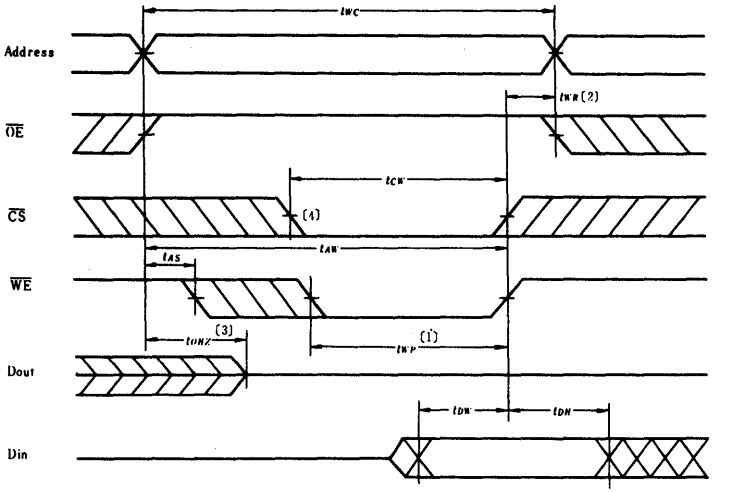


● READ CYCLE (3)[1][3][4]

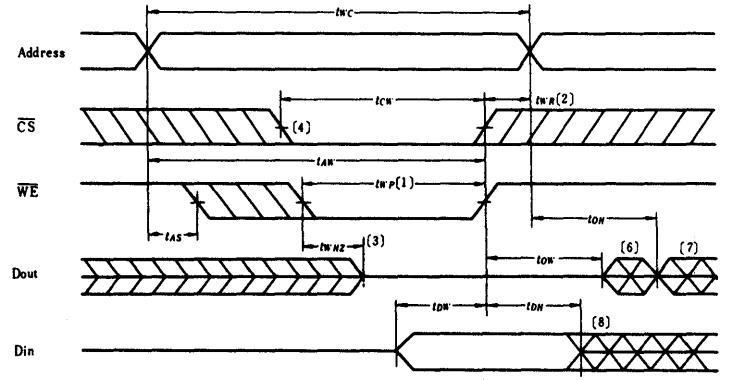


NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE}$ = V_{IL}.

WRITE CYCLE (1)

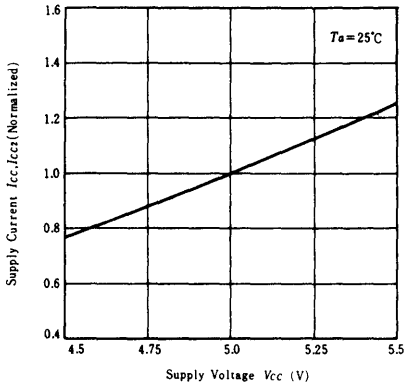


● WRITE CYCLE (2) [5]

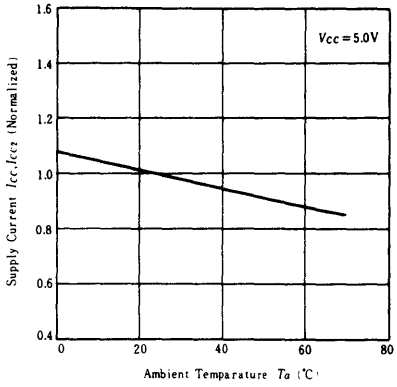


NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

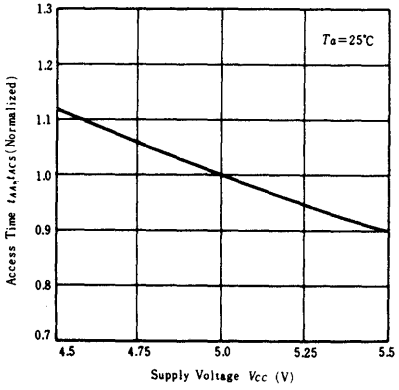
SUPPLY CURRENT vs. SUPPLY VOLTAGE



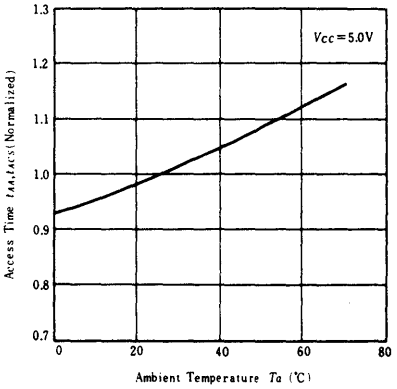
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



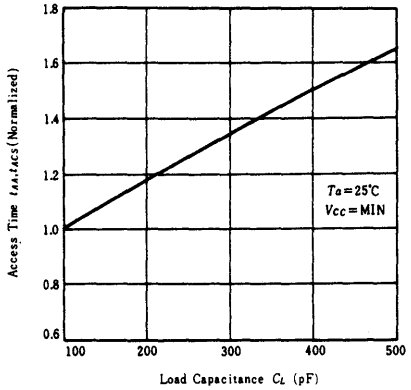
ACCESS TIME vs. SUPPLY VOLTAGE



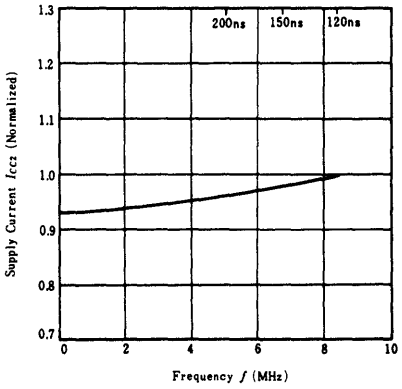
ACCESS TIME vs. AMBIENT TEMPERATURE



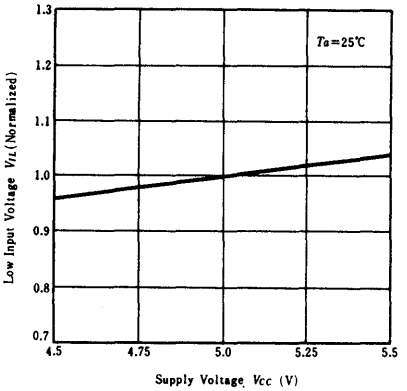
ACCESS TIME vs. LOAD CAPACITANCE



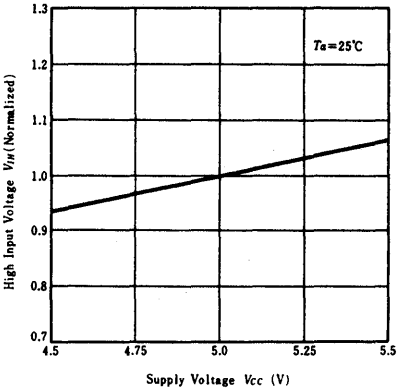
SUPPLY CURRENT vs. FREQUENCY



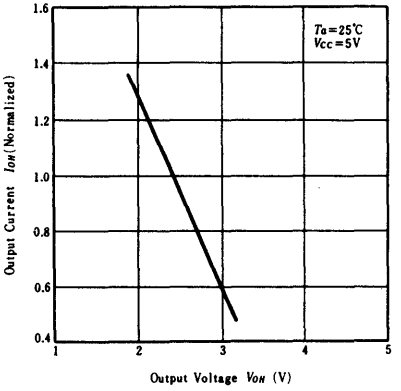
LOW INPUT VOLTAGE vs. SUPPLY VOLTAGE



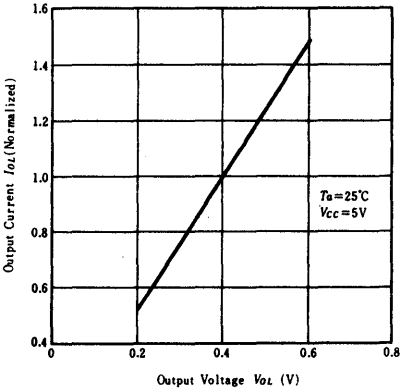
HIGH INPUT VOLTAGE vs. SUPPLY VOLTAGE



OUTPUT CURRENT vs. OUTPUT VOLTAGE



OUTPUT CURRENT vs. OUTPUT VOLTAGE

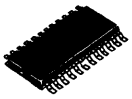


HM6116FP-2, HM6116FP-3, HM6116FP-4

2048-word×8-bit High Speed Static CMOS RAM

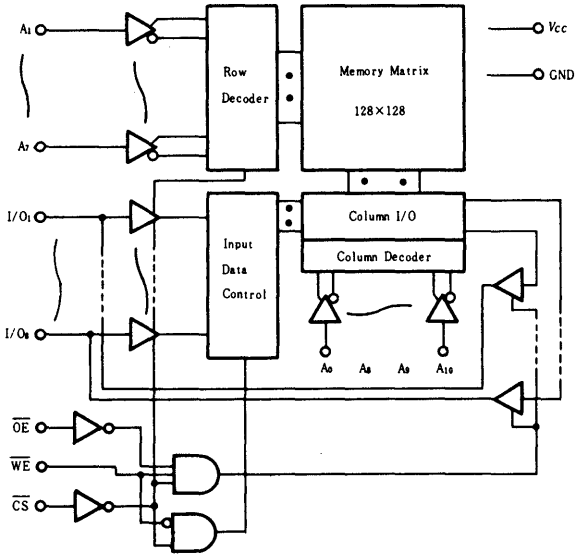
■FEATURES

- High Density Small-Sized Package
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply
- High Speed: Fast Access Time — 120ns/150ns/200ns (max.)
- Low Power Standby — Standby: 100μW (typ.)
- Low Power Operation; — Operation: 180mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time

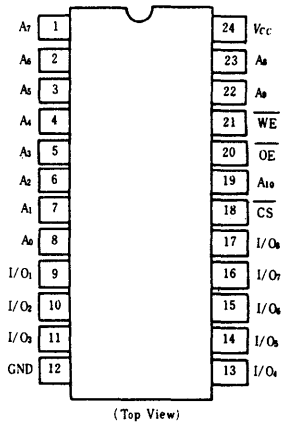


(FP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

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Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns: −3.5V

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle(1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle(1)
L	L	L	Write	I_{CC}	Din	Write Cycle(2)

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−3.0*	—	0.8	V

* Pulse Width : 50ns, DC : V_{IL} min=−0.3V

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test Conditions	HM6116FP-2			HM6116FP-3/-4			Unit
			min	typ*	max	min	typ*	max	
Input Leakage Current	I_{LI}	V_{CC}=5.5V, V_{in}=GND to V_{CC}	—	—	10	—	—	10	μA
Output Leakage Current	I_{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ $V_{I/O}$=GND to V_{CC}	—	—	10	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA	—	40	80	—	35	70	mA
	I_{CCI}**	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	—	35	—	—	30	—	mA
Average Operating Current	I_{CC2}	Min. cycle, duty=100%	—	40	80	—	35	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	5	15	—	5	15	mA
	I_{SB1}	$\overline{CS}\geq V_{CC}-0.2V$, $V_{in}\geq V_{CC}$ −0.2V or $V_{in}\leq 0.2V$	—	0.02	2	—	0.02	2	mA
Output Voltage	V_{OL}	I_{OL}=4mA	—	—	0.4	—	—	—	V
		I_{OL}=2.1mA	—	—	—	—	—	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	V

* V_{CC}=5V, Ta=25°C
** Reference Only

■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C)

●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

●READ CYCLE

Item	Symbol	HM6116FP-2		HM6116FP-3		HM6116FP-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

● WRITE CYCLE

Item	Symbol	HM6116FP-2		HM6116FP-3		HM6116FP-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

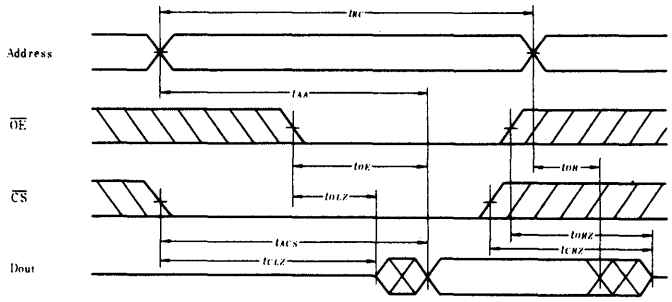
■ CAPACITANCE (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

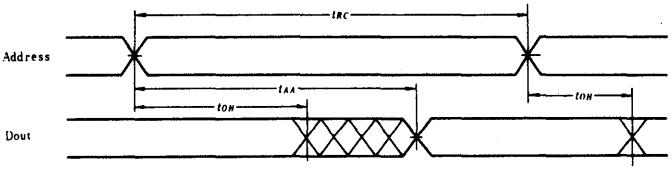
Note) This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

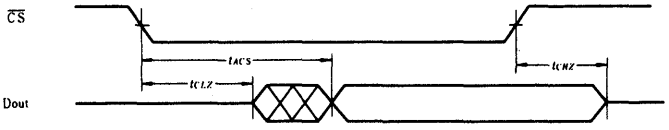
● READ CYCLE (1)[1]



● READ CYCLE (2)[1][2][4]



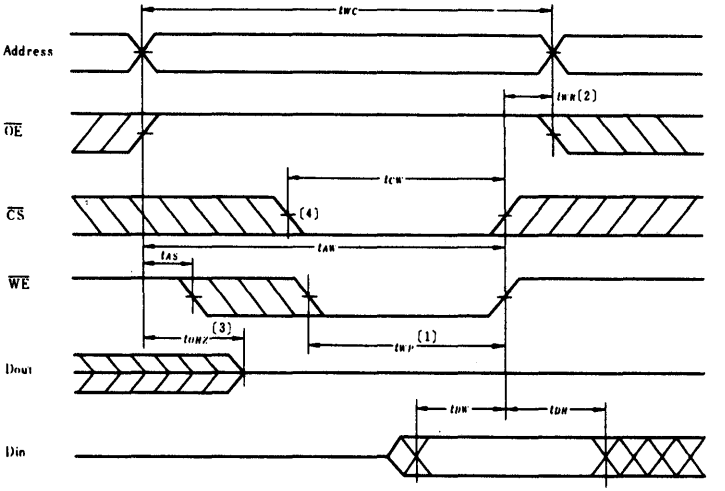
● READ CYCLE (3)[1][3][4]



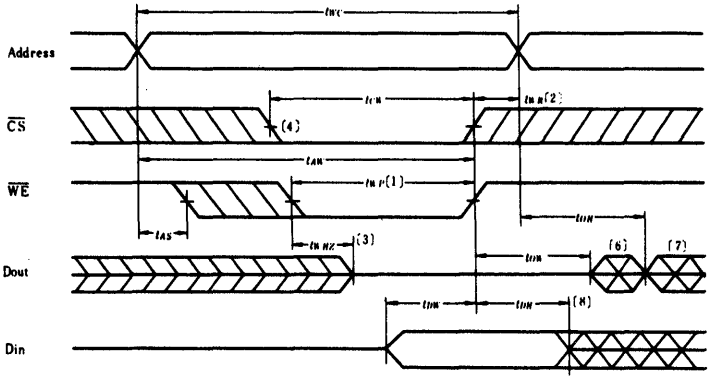
NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE}$ = V_{IL}.

■TIMING WAVEFORM

●WRITE CYCLE (1)[1]

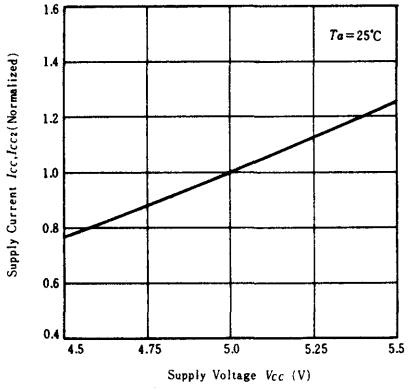


●WRITE CYCLE (2)[5]

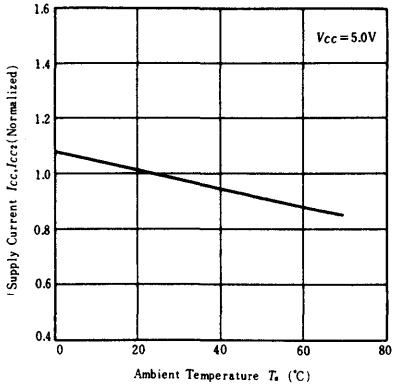


NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

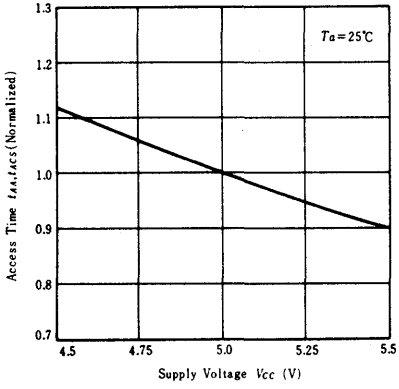
SUPPLY CURRENT vs. SUPPLY VOLTAGE



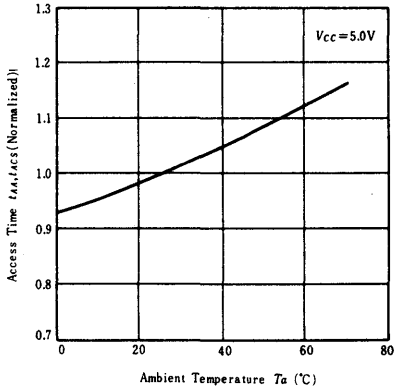
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



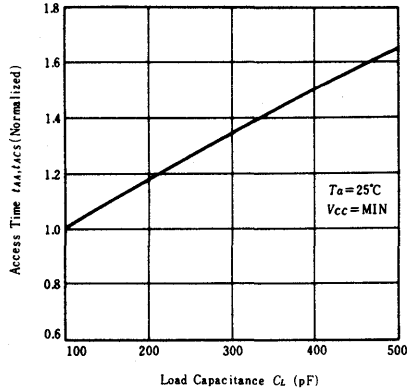
ACCESS TIME vs. SUPPLY VOLTAGE



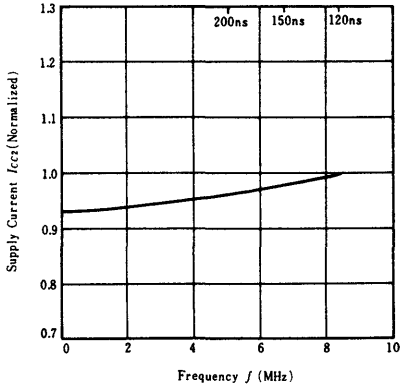
ACCESS TIME vs. AMBIENT TEMPERATURE



ACCESS TIME vs. LOAD CAPACITANCE



SUPPLY CURRENT vs. FREQUENCY

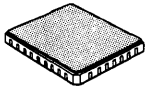


HM6116CG-2, HM6116CG-3, HM6116CG-4

2048-word×8-bit High Speed Static CMOS RAM

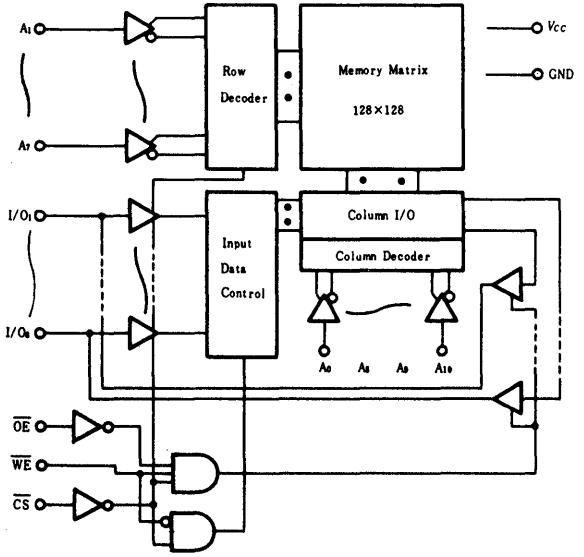
■FEATURES

- Single 5V Supply and High Density 32 pin-Leadless-Chip Carrier
- High speed. Fast Access Time — 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation — Standby: 100μW (typ.), Operation: 180mW (typ.)
- Completely Static RAM: No Clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time

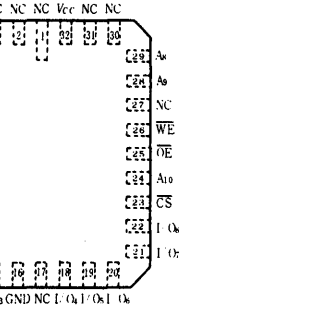


(CG-32)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Temperature Under Bias	T_{bias}	−10 to 85	°C
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns : −3.5V

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−3.0*	—	0.8	V

* Pulse Width : 50ns, DC : V_{IL} min=−0.3V

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test Conditions	HM6116CG-2			HM6116CG-3/-4			Unit
			min	typ*	max	min	typ*	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	—	—	10	—	—	10	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, $V_{I/O}$=GND to V_{CC}	—	—	10	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA	—	40	80	—	35	70	mA
	I_{CC1}**	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	—	35	—	—	30	—	mA
Average Operating Current	I_{CC2}	Min. cycle, duty=100%	—	40	80	—	35	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	5	15	—	5	15	mA
	I_{SB1}	$\overline{CS}\geqq V_{CC}-0.2V$, $V_{in}\geqq V_{CC}-0.2V$ or $V_{in}\leqq 0.2V$	—	0.02	2	—	0.02	2	mA
Output Voltage	V_{OL}	I_{OL}=4mA	—	—	0.4	—	—	—	V
		I_{OL}=2.1mA	—	—	—	—	—	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	V

* V_{CC}=5V, Ta=25°C
** Reference Only

■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C)

●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

●READ CYCLE

Item	Symbol	HM6116CG-2		HM6116CG-3		HM6116CG-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

● WRITE CYCLE

Item	Symbol	HM6116CG-2		HM6116CG-3		HM6116CG-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

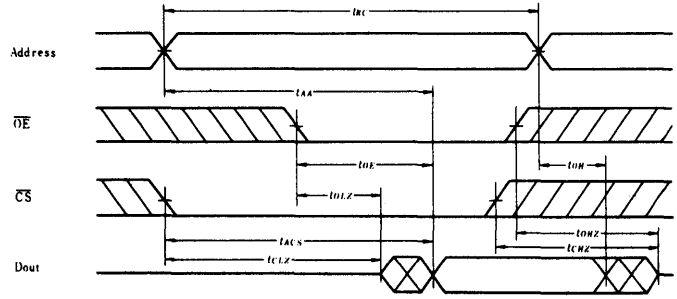
■ CAPACITANCE (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

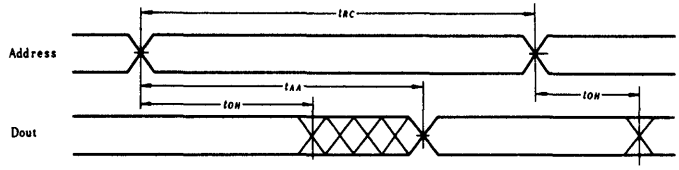
Note) This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

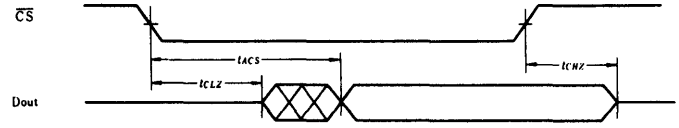
● READ CYCLE (1)[1]



● READ CYCLE (2)[1][2][4]

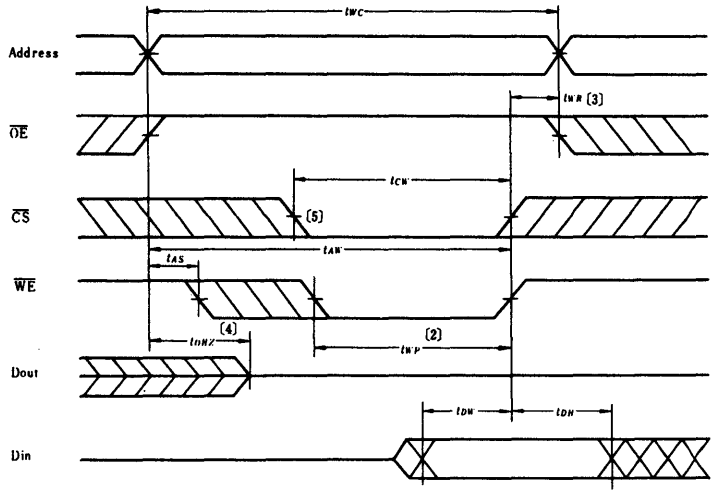


● READ CYCLE (3)[1][3][4]

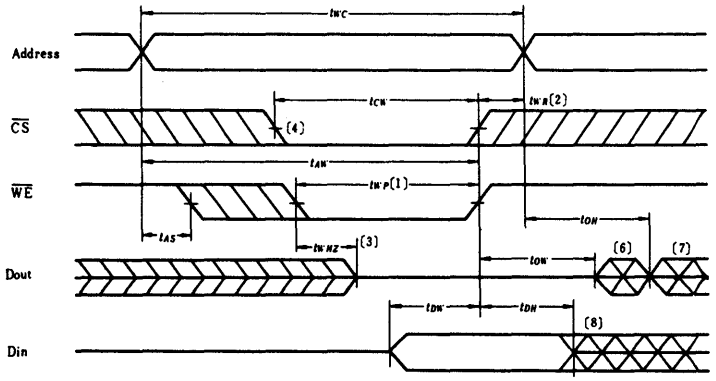


NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE}$ = V_{IL}.

WRITE CYCLE (1) [1]



● WRITE CYCLE (2) [5]



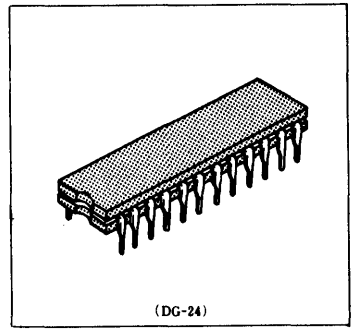
NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

HM6116L-2, HM6116L-3, HM6116L-4

2048-word×8-bit High Speed Static CMOS RAM

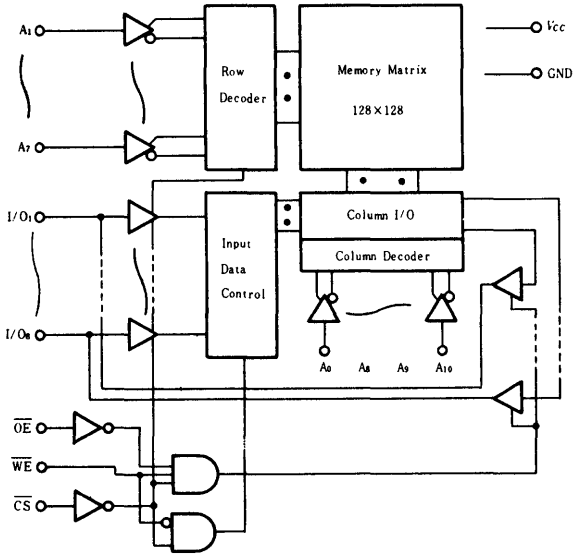
■ FEATURES

- Single 5V Supply and High Density 24 Pin Package
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Standby: 20μW (typ.)
- Low Power Operation; Operation: 160mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

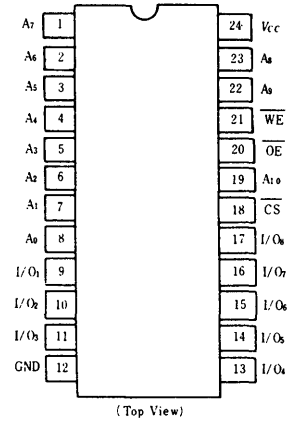


(DG-24)

■ FUNCTIONAL BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns : −3.5V

■ TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−3.0*	—	0.8	V

* Pulse Width: 50ns, DC: V_{IL} min = −0.3V

■ DC AND OPERATING CHARACTERISTICS (V_{CC}=5V ±10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test Conditions	HM6116L-2			HM6116L-3/-4			Unit
			min	typ*	max	min	typ*	max	
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	—	—	2	—	—	2	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, $V_{I/O}$=GND to V_{CC}	—	—	2	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA	—	35	70	—	30	60	mA
	I_{CC1}**	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	—	30	—	—	25	—	mA
Average Operating Current	I_{CC2}	min. cycle, duty=100%	—	35	70	—	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	4	12	—	4	12	mA
	I_{SB1}	$\overline{CS} \geq V_{CC}-0.2V$, $V_{in} \geq V_{CC}-0.2V$ or $V_{in} \leq 0.2V$	—	4	100	—	4	100	μA
Output Voltage	V_{OL}	I_{OL}=4mA	—	—	0.4	—	—	—	V
		I_{OL}=2.1mA	—	—	—	—	—	0.4	
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	V

* : V_{CC}=5V, Ta=25°C
** : Reference Only

■ AC CHARACTERISTICS (V_{CC}=5V ±10%, Ta=0 to +70°C)

● AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

● READ CYCLE

Item	Symbol	HM6116L-2		HM6116L-3		HM6116L-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

● WRITE CYCLE

Item	Symbol	HM6116L-2		HM6116L-3		HM6116L-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

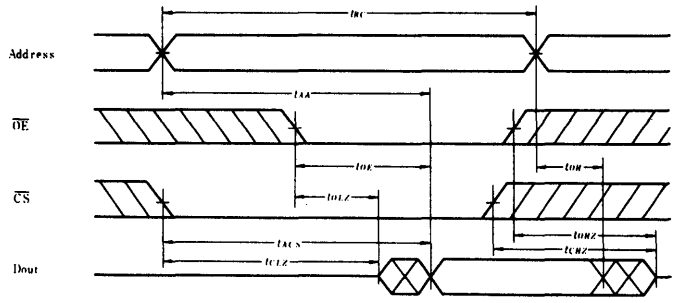
■ CAPACITANCE (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

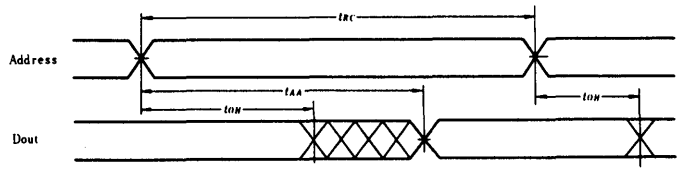
Note) This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

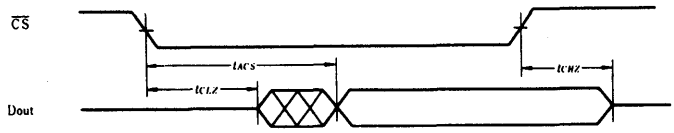
● Read Cycle (1) (1)



● Read Cycle (2) (1), (2), (4)

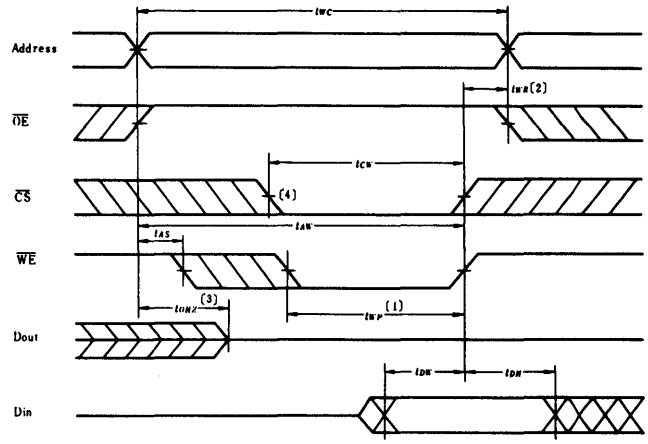


● Read Cycle (3) (1), (3), (4)

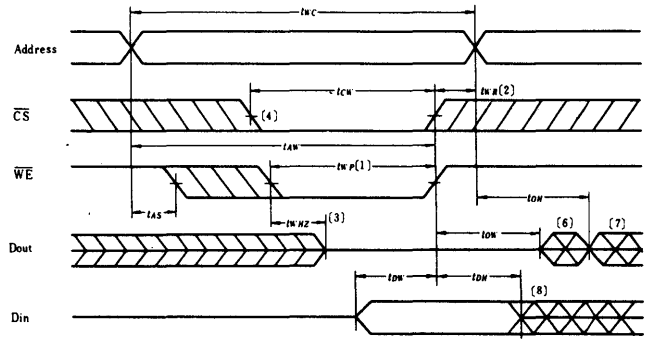


NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE}$ = V_{IL}.

● **Write Cycle (1)**



● **Write Cycle (2)** (5)



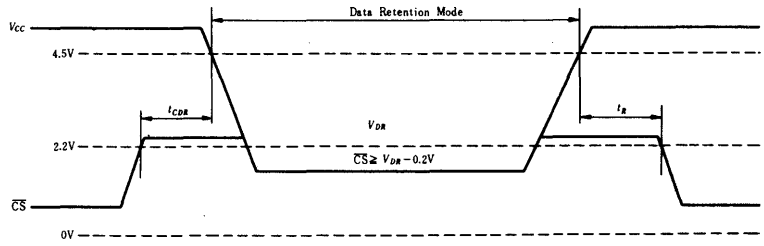
NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL})
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■ LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=0 to +70°C)

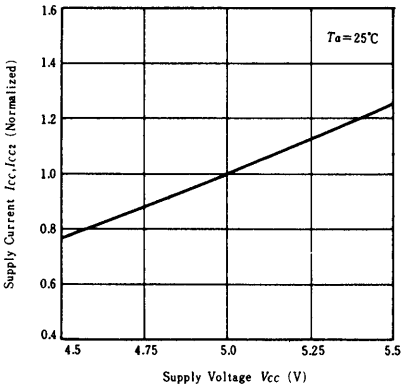
Item	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$ −0.2V, $V_{in} \geq V_{CC}$ −0.2V or $V_{in} \leq$0.2V	2.0	—	—	V
Data Retention Current	I_{CCDR}*	V_{CC}=3.0V, $\overline{CS} \geq$2.8V, $V_{in} \geq$2.8V or $V_{in} \leq$0.2V	—	—	50	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}**	—	—	ns

* V_{IL}=−0.3V min.
** t_{RC}=Read Cycle Time.

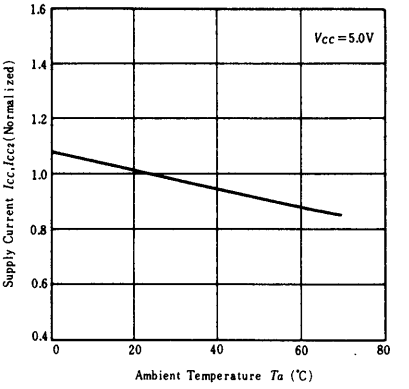
● **Low Vcc Data Retention Waveform**



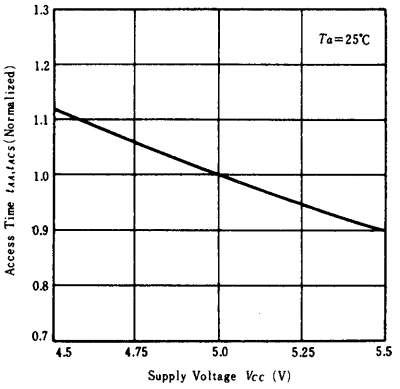
SUPPLY CURRENT vs. SUPPLY VOLTAGE



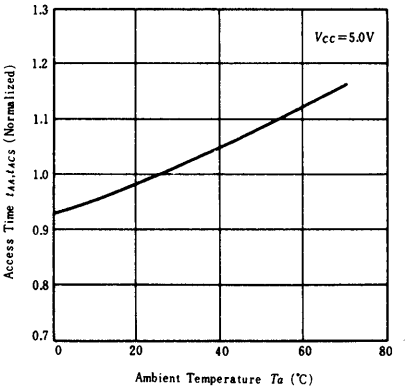
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



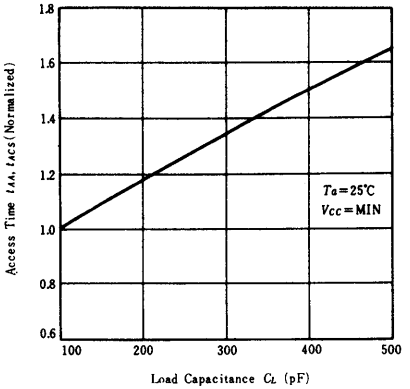
ACCESS TIME vs. SUPPLY VOLTAGE



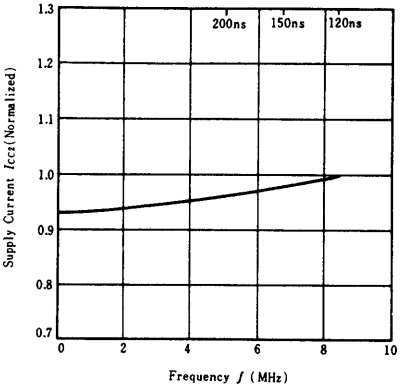
ACCESS TIME vs. AMBIENT TEMPERATURE



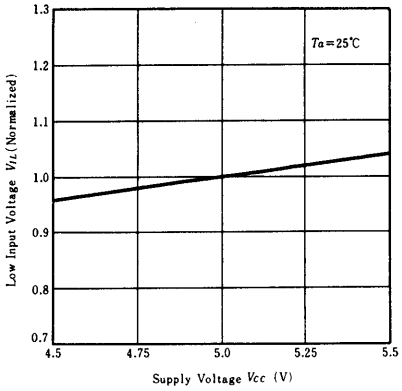
ACCESS TIME vs. LOAD CAPACITANCE



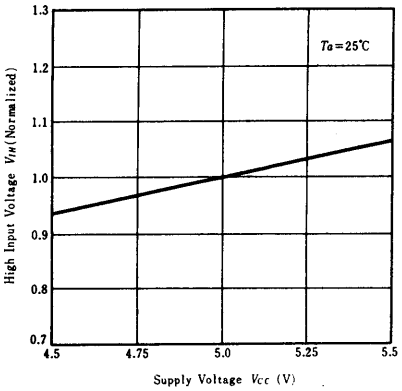
SUPPLY CURRENT vs. FREQUENCY



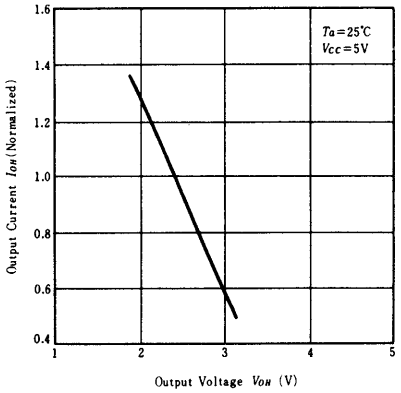
LOW INPUT VOLTAGE vs. SUPPLY VOLTAGE



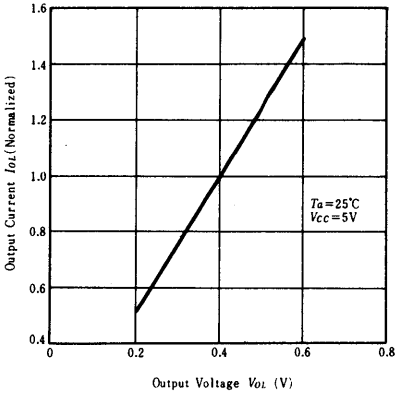
HIGH INPUT VOLTAGE vs. SUPPLY VOLTAGE



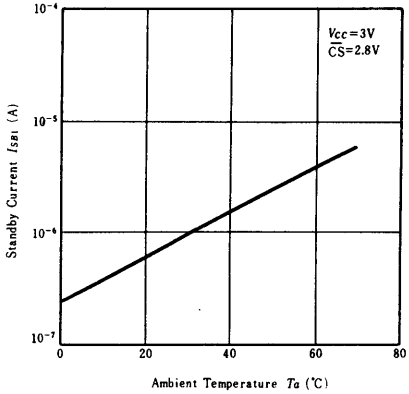
OUTPUT CURRENT vs. OUTPUT VOLTAGE



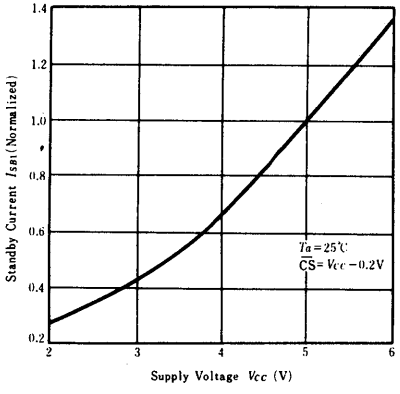
OUTPUT CURRENT vs. OUTPUT VOLTAGE



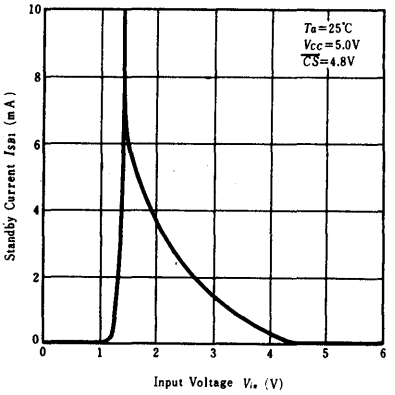
STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE



STANDBY CURRENT vs. INPUT VOLTAGE

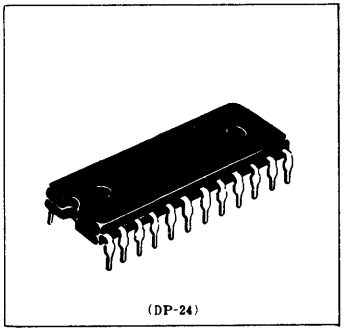


HM6116LP-2, HM6116LP-3, HM6116LP-4

2048-word×8-bit High Speed Static CMOS RAM

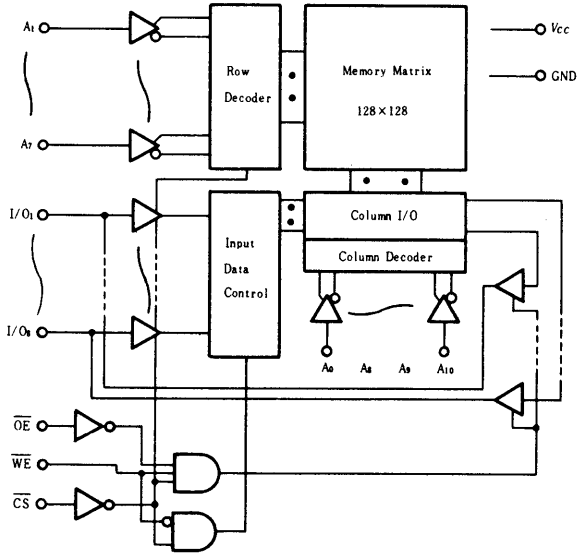
■FEATURES

- Single 5V Supply and High Density 24 Pin Package
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation; Standby: 10μW (typ.) Operation: 160mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

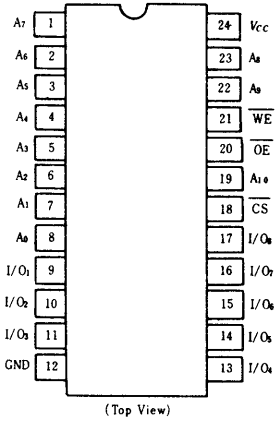


(DP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns : −3.5V

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−3.0*	—	0.8	V

* Pulse Width : 50ns, DC : V_{IL} min = −0.3V

■ DC AND OPERATING CHARACTERISTICS (V_{CC}=5V ±10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test Conditions	HM6116LP-2			HM6116LP-3/-4			Unit
			min	typ*	max	min	typ*	max	
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	—	—	2	—	—	2	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, $V_{I/O}$=GND to V_{CC}	—	—	2	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA	—	35	70	—	30	60	mA
	I_{CC1}**	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	—	30	—	—	25	—	mA
Average Operating Current	I_{CC2}	min. cycle, duty=100%	—	35	70	—	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	4	12	—	4	12	mA
	I_{SB1}	$\overline{CS} \geqq V_{CC}-0.2V$, $V_{in} \geqq V_{CC}-0.2V$ or $V_{in} \leqq 0.2V$	—	2	50	—	2	50	μA
Output Voltage	V_{OL}	I_{OL}=4mA	—	—	0.4	—	—	—	V
		I_{OL}=2.1mA	—	—	—	—	—	0.4	
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	V

* : V_{CC}=5V, Ta=25°C
** : Reference Only

■ AC CHARACTERISTICS (V_{CC}=5V ±10%, Ta=0 to +70°C)

● AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

● READ CYCLE

Item	Symbol	HM6116LP-2		HM6116LP-3		HM6116LP-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

● WRITE CYCLE

Item	Symbol	HM6116LP-2		HM6116LP-3		HM6116LP-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

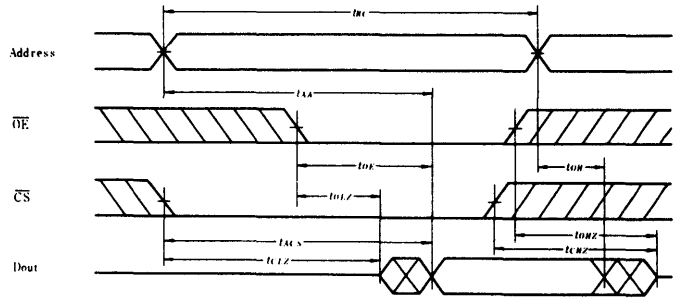
■ CAPACITANCE (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

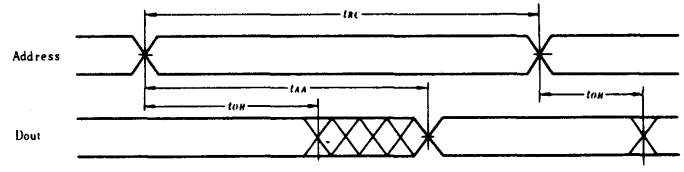
Note) This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

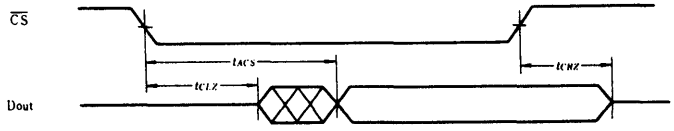
● Read Cycle (1) (1)



● Read Cycle (2) (1), (2), (4)

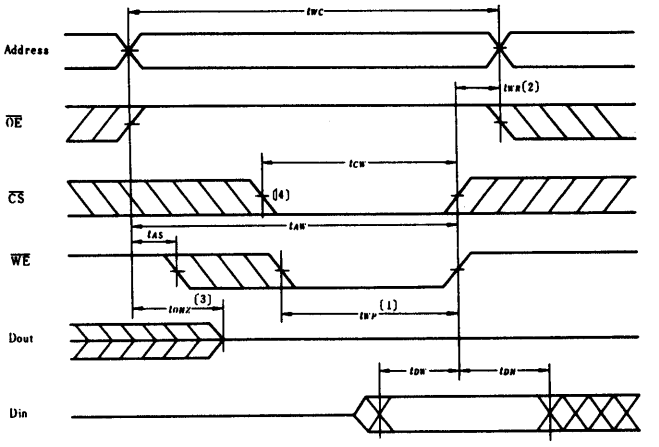


● Read Cycle (3) (1), (3), (4)

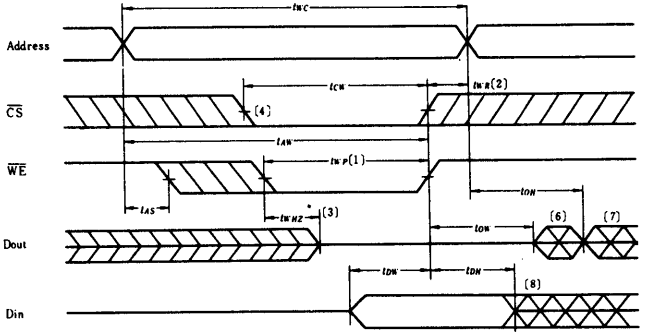


NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE}$ = V_{IL}.

● **Write Cycle (1)**



● **Write Cycle (2)** (5)



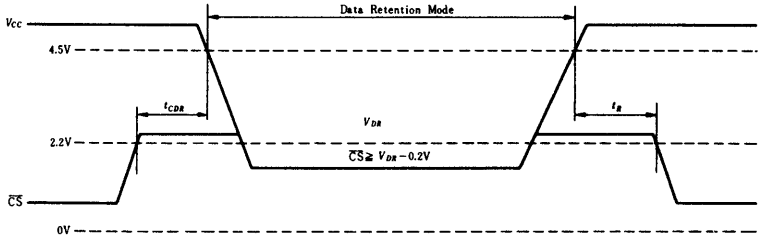
NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=0 to +70°C)

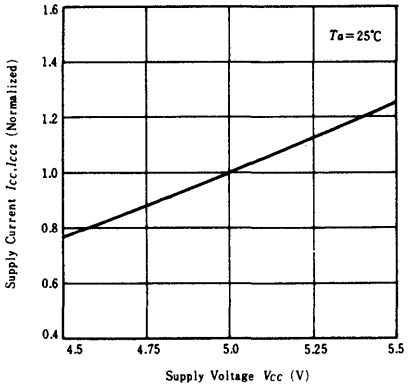
Item	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$ −0.2V, $V_{in} \geq V_{CC}$ −0.2V or $V_{in} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}*	V_{CC}=3.0V, $\overline{CS} \geq 2.8V$, $V_{in} \geq 2.8V$ or $V_{in} \leq 0.2V$	—	—	30	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}**	—	—	ns

* 10 μA max at Ta=0°C to +40°C, V_{IL} min = −0.3V
** t_{RC} = Read Cycle Time.

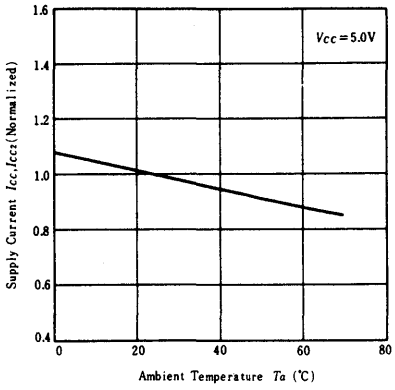
● **Low Vcc Data Retention Waveform**



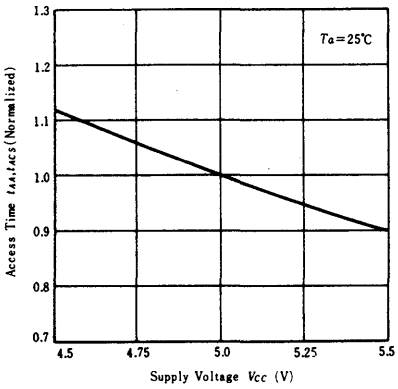
SUPPLY CURRENT vs. SUPPLY VOLTAGE



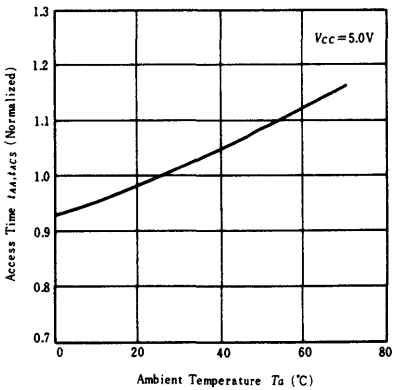
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



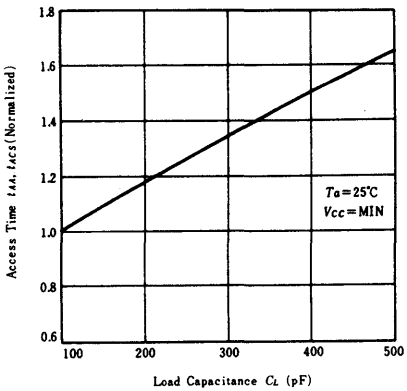
ACCESS TIME vs. SUPPLY VOLTAGE



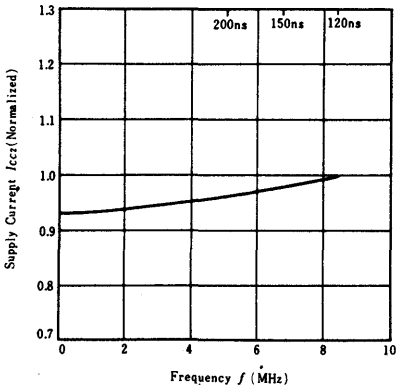
ACCESS TIME vs. AMBIENT TEMPERATURE



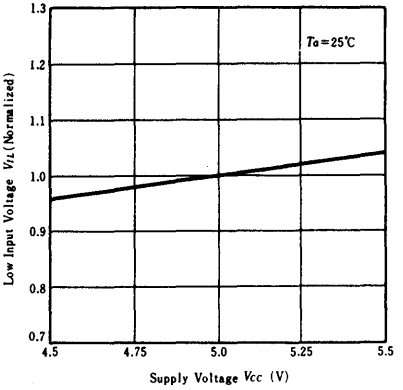
ACCESS TIME vs. LOAD CAPACITANCE



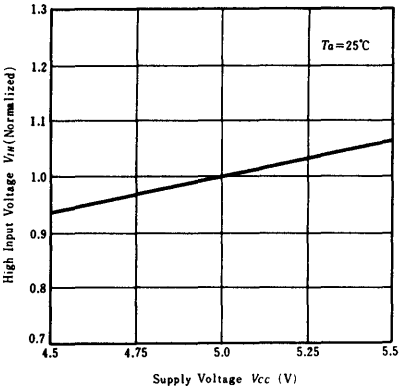
SUPPLY CURRENT vs. FREQUENCY



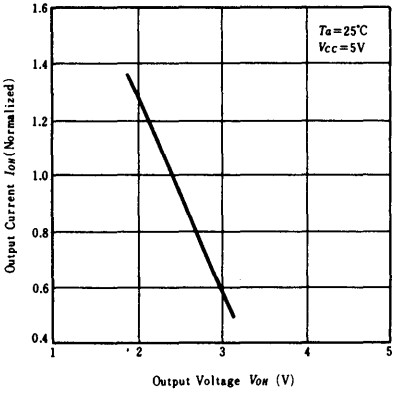
LOW INPUT VOLTAGE vs. SUPPLY VOLTAGE



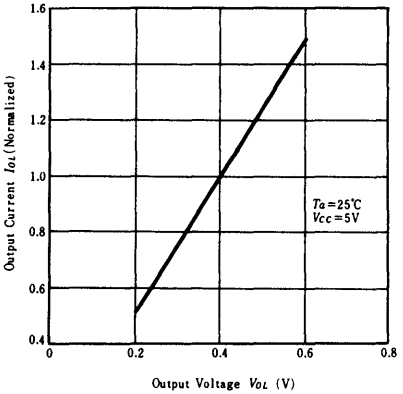
HIGH INPUT VOLTAGE vs. SUPPLY VOLTAGE



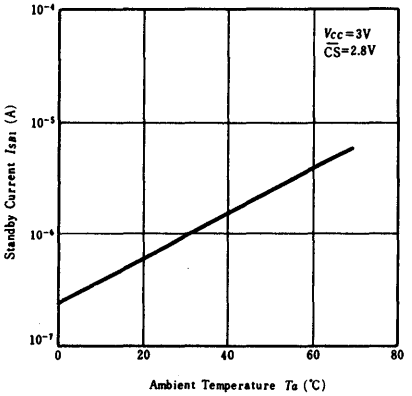
OUTPUT CURRENT vs. OUTPUT VOLTAGE



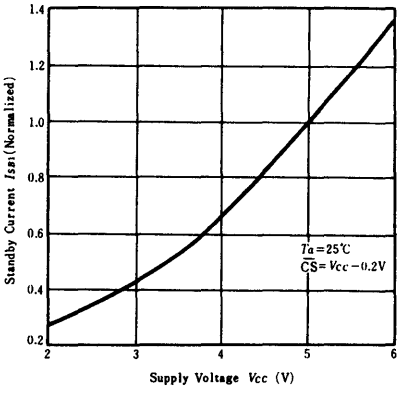
OUTPUT CURRENT vs. OUTPUT VOLTAGE



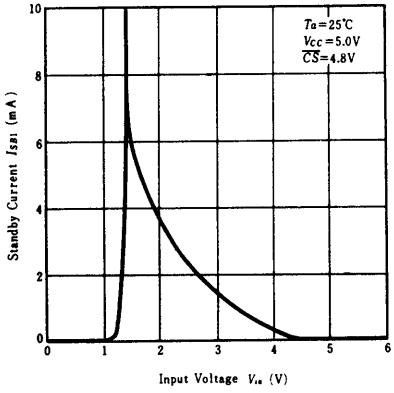
STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE



STANDBY CURRENT vs. INPUT VOLTAGE

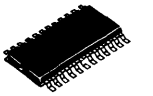


HM6116LFP-2, HM6116LFP-3, HM6116LFP-4

2048-word×8-bit High Speed Static CMOS RAM

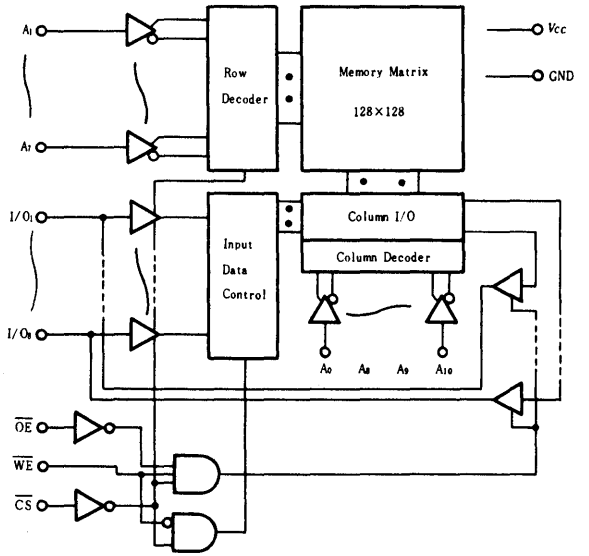
■FEATURES

- High Density Small-sized Package
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply
- High Speed: Fast Access Time — 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation; — Standby: 10μW (typ.) Operation: 160mW (typ.)
- Completely Static RAM: No Clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

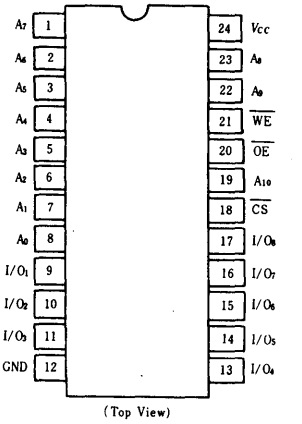


(FP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

*Pulse width 50ns: −3.5V

HITACHI

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−3.0*	—	0.8	V

* Pulse Width : 50ns, DC : V_{IL} min=−0.3V.

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test Conditions	HM6116LFP-2			HM6116LFP-3/-4			Unit
			min	typ*	max	min	typ*	max	
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	—	—	2	—	—	2	μA
Output Leakage Currnnt	$\lvert I_{LO} \rvert$	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, $V_{I/O}$=GND to V_{CC}	—	—	2	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA	—	35	70	—	30	60	mA
	I_{CC1}**	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	—	30	—	—	25	—	mA
Average Operating Current	I_{CC2}	Min cycle, duty=100%	—	35	70	—	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	4	12	—	4	12	mA
	I_{SB1}	$\overline{CS}\geq V_{CC}-0.2V$, $V_{in}\geq V_{CC}-0.2V$ or $V_{in}\leq 0.2V$	—	2	50	—	2	50	μA
Output Voltage	V_{OL}	I_{OL}=4mA	—	—	0.4	—	—	—	V
		I_{OL}=2.1mA	—	—	—	—	—	0.4	
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	V

* : V_{CC}=5V, Ta=25°C
** : Reference Only

■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C)

●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

●READ CYCLE

Item	Symbol	HM6116LFP-2		HM6116LFP-3		HM6116LFP-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

●WRITE CYCLE

Item	Symbol	HM6116LFP-2		HM6116LFP-3		HM6116LFP-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

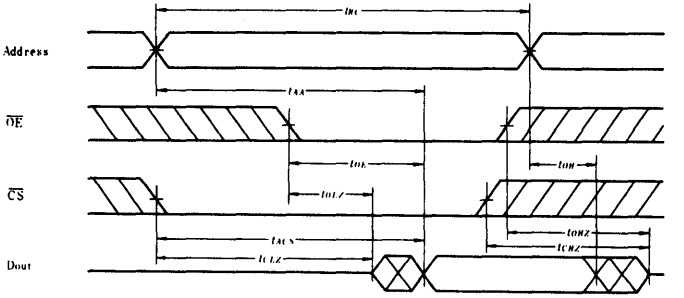
■CAPACITANCE (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	Cin	Vin=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

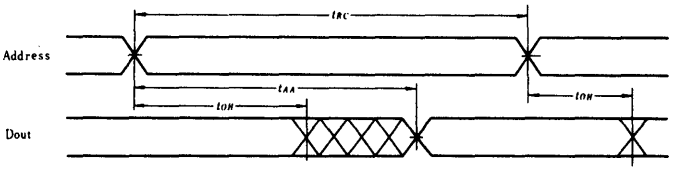
Note) This parameter is sampled and not 100% tested.

■TIMING WAVEFORM

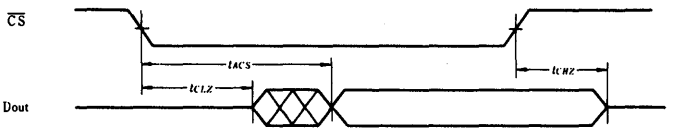
●READ CYCLE (1)[1]



●READ CYCLE (2)[1][2][4]

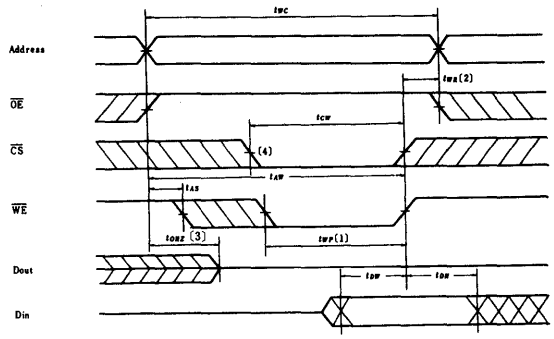


●READ CYCLE (3)[1][3][4]

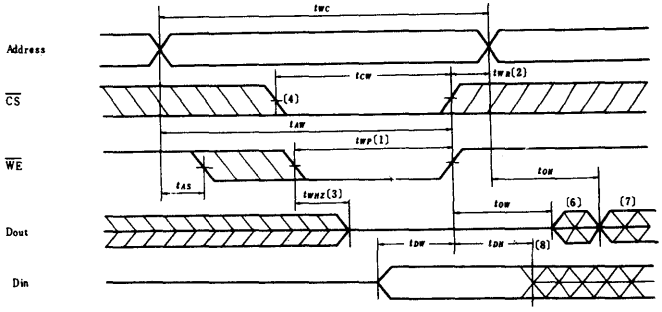


NOTES: 1. $\overline{WE}$ is High for Read Cycle
2. Device is continuously selected, $\overline{CS}$ = V_{IL}
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE}$ = V_{IL}.

●WRITE CYCLE (1)



●WRITE CYCLE (2)[5]



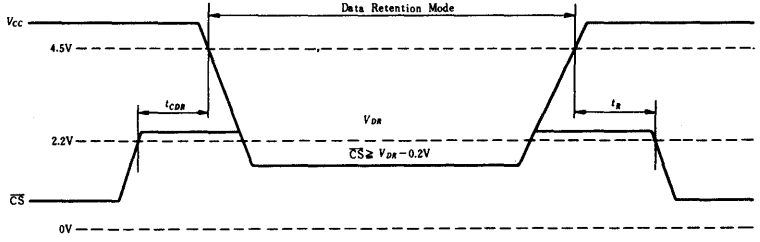
NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■LOW V_{CC} DATA RETENTION CHARACTERISTICS (Ta=0 to +70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC}-0.2V$ $V_{IN} \geqq V_{CC}-0.2V$ or $V_{IN} \leqq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}*	V_{CC}=3.0V, $\overline{CS} \geqq 2.8V$ $V_{IN} \geqq 2.8V$ or $V_{IN} \leqq 0.2V$	—	—	30	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		**t_{RC}	—	—	ns

* V_{IL} min=−0.3V, 10 μA max (at Ta=0 to +40°C)
** t_{RC}=Read Cycle Time.

●Low V_{CC} DATA RETENTION WAVEFORM



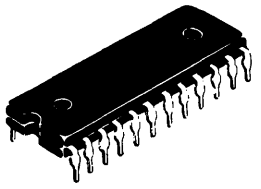
HM6116AP-12, HM6116AP-15, HM6116AP-20, HM6116ASP-12, HM6116ASP-15, HM6116ASP-20

2048-word × 8-bit High Speed Static CMOS RAM

■ FURTURES

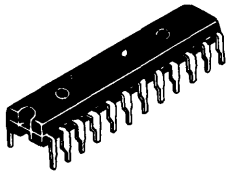
- High speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation — Standby: 100μW (typ.); Operation: 15mW (typ.) (f = 1MHz)
- Single 5V Supply and High Density 24 Pin Package
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

HM6116AP Series



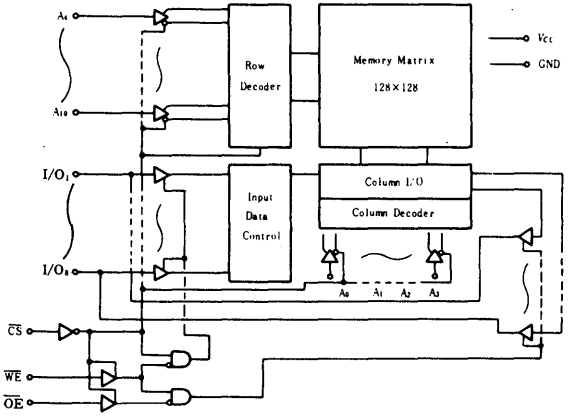
(DP-24)

HM6116ASP Series

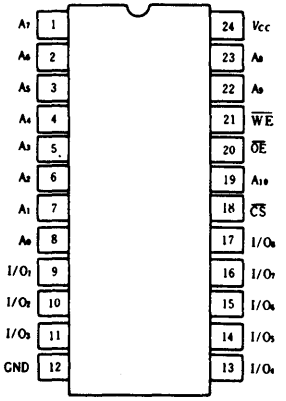


(DP-24A)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns : −3.5V

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−3.0*	—	0.8	V

* Pulse Width : 50ns, DC : V_{IL} min = −0.3V

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ±10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	HM6116AP/ASP-12			HM6116AP/ASP-15			HM6116AP/ASP-20			Unit
			min	typ*	max	min	typ*	max	min	typ*	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	—	—	2	—	—	2	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	CS=V_{IH} or OE=V_{IH}, $V_{I/O}$=GND to V_{CC}	—	—	2	—	—	2	—	—	2	μA
Operating Power Supply Current	I_{CC}	CS=V_{IL}, $I_{I/O}$=0mA V_{in}=V_{IH} or V_{IL}	—	5	15	—	5	15	—	5	15	mA
	I_{CC1}	V_{IH}=V_{CC}, V_{IL}=0V, CS=V_{IL}, $I_{I/O}$=0mA, f=1MHz	—	3	6	—	3	6	—	3	6	mA
Average Operating Current	I_{CC2}	min. cycle, duty = 100%	—	35	60	—	25	45	—	20	35	mA
Standby Power Supply Current	I_{SB}	CS=V_{IH}	—	1	4	—	1	4	—	1	4	mA
	I_{SB1}	CS≧V_{CC} −0.2V	—	0.02	2	—	0.02	2	—	0.02	2	mA
Output Voltage	V_{OL}	I_{OL}=4mA	—	—	0.4	—	—	0.4	—	—	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	2.4	—	—	V

* V_{CC}=5V, T_a=25°C

■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C)

●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

● READ CYCLE

Item	Symbol	HM6116AP/ASP-12		HM6116AP/ASP-15		HM6116AP/ASP-20		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	10	—	10	—	ns
Output Enable to Output Valid	t_{OE}	—	55	—	60	—	70	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	10	—	10	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	20	—	ns

● WRITE CYCLE

Item	Symbol	HM6116AP/ ASP-12		HM6116AP/ ASP-15		HM6116AP/ ASP-20		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	–	150	–	200	–	ns
Chip Selection to End of Write	t_{CW}	70	–	90	–	120	–	ns
Address Valid to End of Write	t_{AW}	105	–	120	–	140	–	ns
Address Set Up Time	t_{AS}	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	70	–	80	–	100	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	35	–	40	–	50	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	ns
Output Active from End of Write	t_{OW}	10	–	10	–	10	–	ns

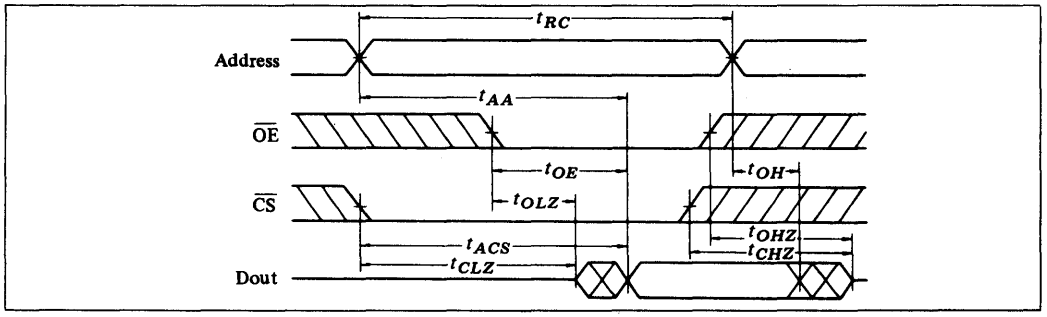
■CAPACITANCE (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

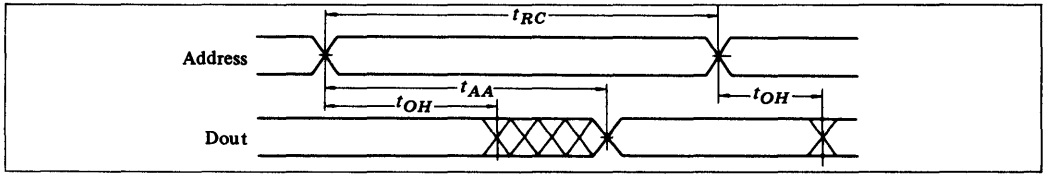
Note) This parameter is sampled and not 100% tested.

■TIMING WAVEFORM

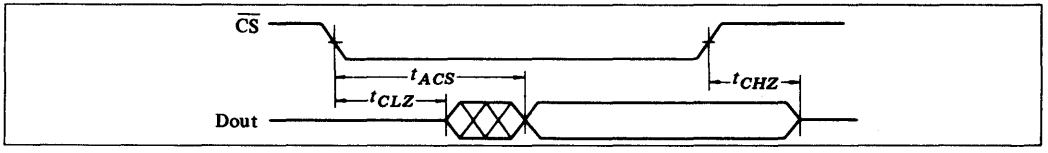
●READ CYCLE (1)[1]



●READ CYCLE (2)[1][2][4]

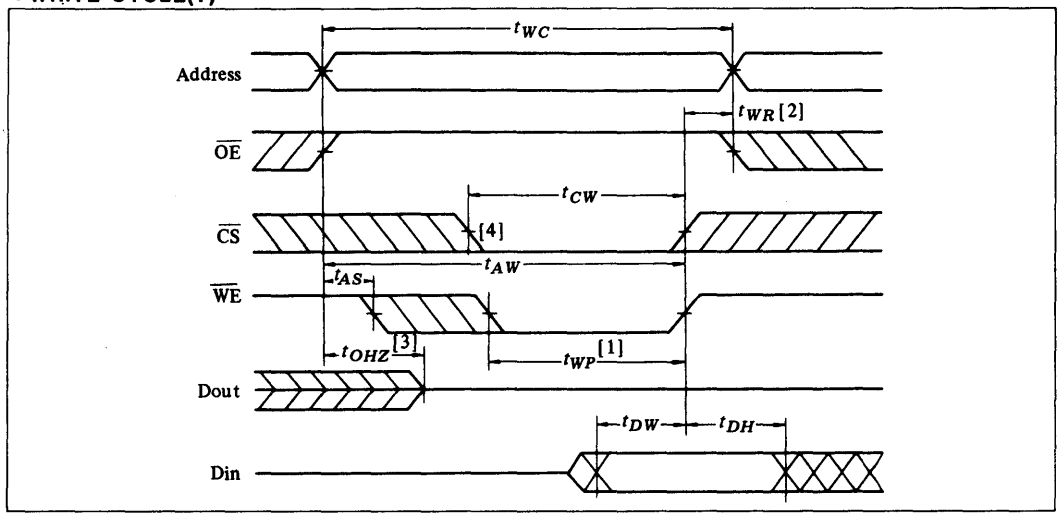


●READ CYCLE (3)[1][3][4]

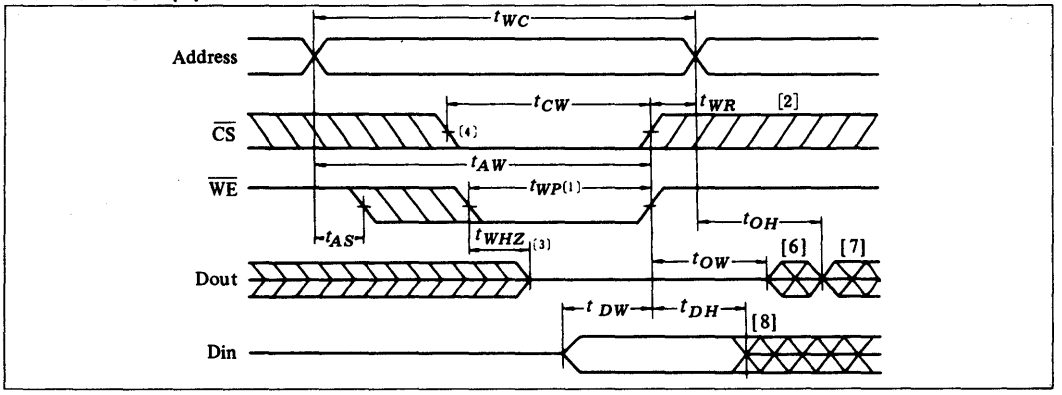


NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE}$ = V_{IL}.

●WRITE CYCLE(1)



●WRITE CYCLE(2)[5]



NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL})
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

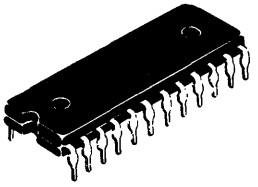
HM6116ALP-12, HM6116ALP-15, HM6116ALP-20, HM6116ALSP-12, HM6116ALSP-15, HM6116ALSP-20

2048-word × 8-bit High Speed Static CMOS RAM

■ FEATURES

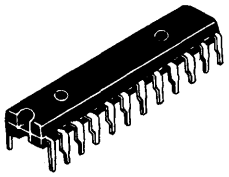
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation; Standby: 5μW (typ.) Operation: 10mW (typ.) (f = 1MHz)
- Capability of Battery Back up Operation
- Single 5V Supply and High Density 24 Pin Package
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

HM6116ALP Series



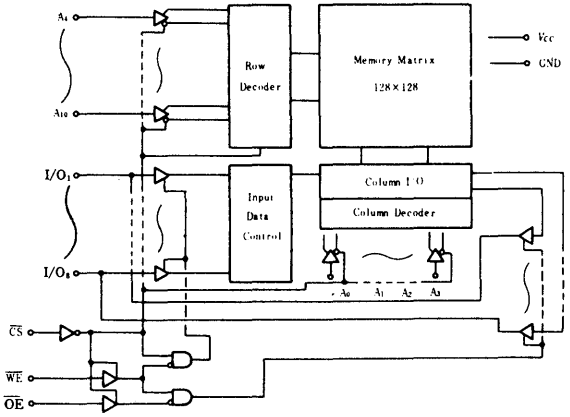
(DP-24)

HM6116ALSP Series

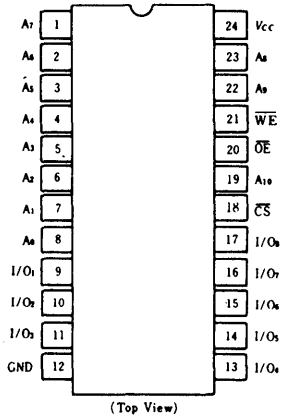


(DP-24A)

■ FUNCTIONAL BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns : −3.5V

■ TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−3.0*	—	0.8	V

* Pulse Width: 50ns, DC: V_{IL} min = −0.3V

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	HM6116ALP/ ALSP-12			HM6116ALP/ ALSP-15			HM6116ALP/ ALSP-20			Unit
			min	typ*	max	min	typ*	max	min	typ*	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	—	—	2	—	—	2	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	CS=V_{IH} or OE=V_{IH}, $V_{I/O}$=GND to V_{CC}	—	—	2	—	—	2	—	—	2	μA
Operating Power Supply Current	I_{CC}	CS=V_{IL}, $I_{I/O}$=0mA V_{in}=V_{IH} or V_{IL}	—	4	12	—	4	12	—	4	12	mA
	I_{CC1}	V_{IH}=V_{CC}, V_{IL}=0V CS=V_{IL}, $I_{I/O}$=0mA, f=1MHz	—	2	5	—	2	5	—	2	5	mA
Average Operating Current	I_{CC2}	min. cycle, duty = 100%	—	30	50	—	20	40	—	15	30	mA
Standby Power Supply Current	I_{SB}	CS=V_{IH}	—	0.5	3	—	0.5	3	—	0.5	3	mA
	I_{SB1}	CS≧V_{CC} −0.2V	—	1	50	—	1	50	—	1	50	μA
Output Voltage	V_{OL}	I_{OL}=4mA	—	—	0.4	—	—	0.4	—	—	0.4	V
	V_{OH}	I_{OH}= −1.0mA	2.4	—	—	2.4	—	—	2.4	—	—	V

* V_{CC}=5V, T_a=25°C

■ AC CHARACTERISTICS (V_{CC}=5V ±10%, Ta=0 to +70°C)

● AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

● READ CYCLE

Item	Symbol	HM6116ALP/ ALSP-12		HM6116ALP/ ALSP-15		HM6116ALP/ ALSP-20		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	10	—	10	—	ns
Output Enable to Output Valid	t_{OE}	—	55	—	60	—	70	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	10	—	10	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	20	—	ns

● WRITE CYCLE

Item	Symbol	HM6116ALP/ ALSP-12		HM6116ALP/ ALSP-15		HM6116ALP/ ALSP-20		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	–	150	–	200	–	ns
Chip Selection to End of Write	t_{CW}	70	–	90	–	120	–	ns
Address Valid to End of Write	t_{AW}	105	–	120	–	140	–	ns
Address Set Up Time	t_{AS}	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	70	–	80	–	100	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WOH}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	35	–	40	–	50	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	ns
Output Active from End of Write	t_{OW}	10	–	10	–	10	–	ns

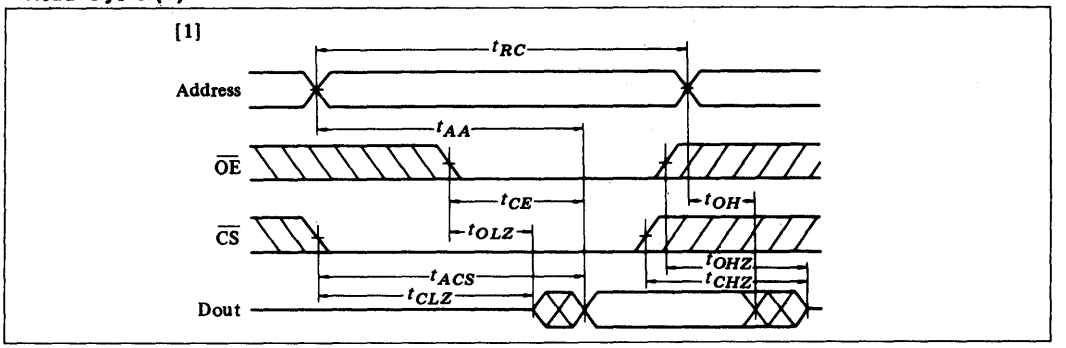
■ CAPACITANCE (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

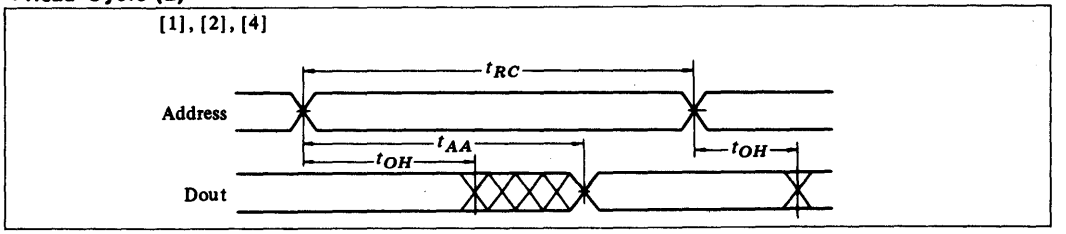
Note) This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

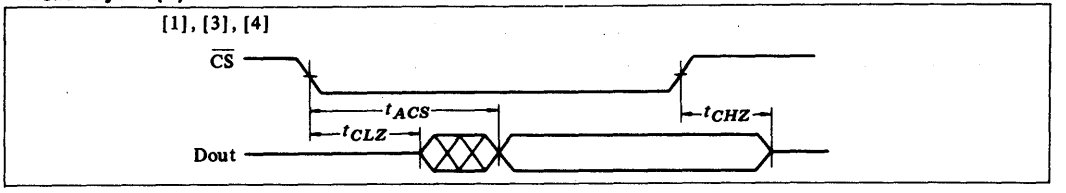
● Read Cycle (1)



● Read Cycle (2)

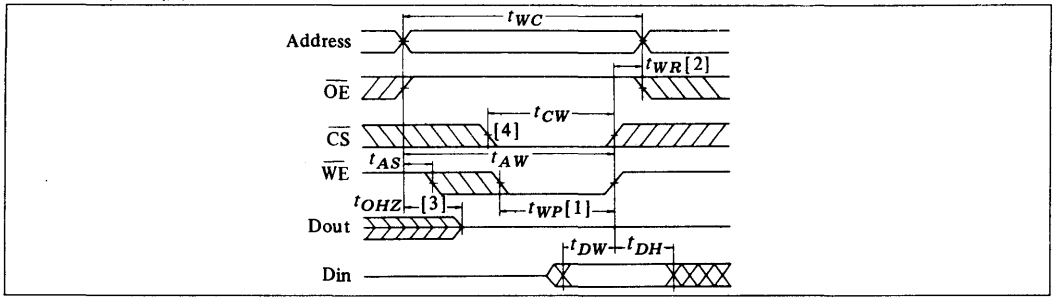


● Read Cycle (3)

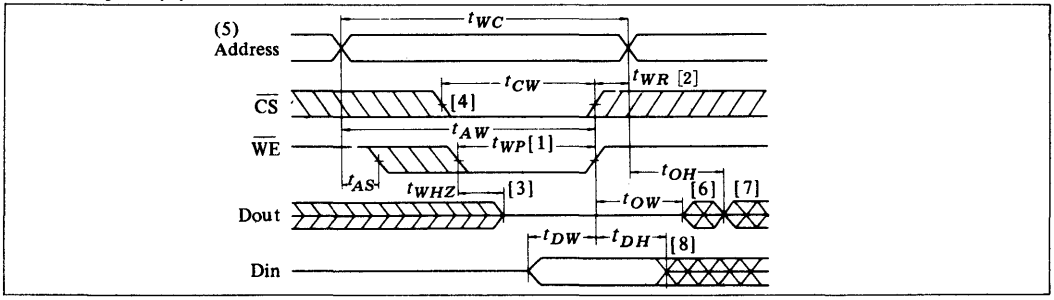


NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE}$ = V_{IL}.

● **Write Cycle (1)**



● **Write Cycle (2)**



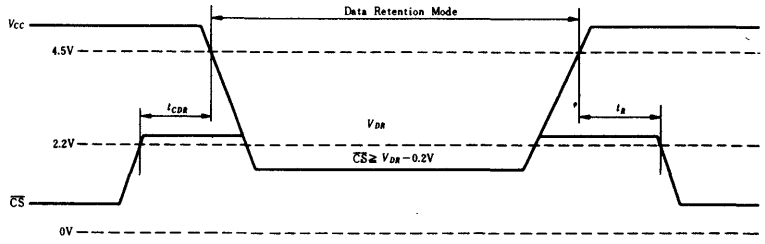
NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL})
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■ LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=0 to +70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$ −0.2V	2.0	—	—	V
Data Retention Current	I_{CCDR}*	V_{CC}=3.0V, $\overline{CS} \geq$2.8V	—	—	30	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}**	—	—	ns

* 10 μA max at Ta=0°C to +40°C, V_{IL} min = −0.3V
** t_{RC} = Read Cycle Time.

● **Low Vcc Data Retention Waveform**

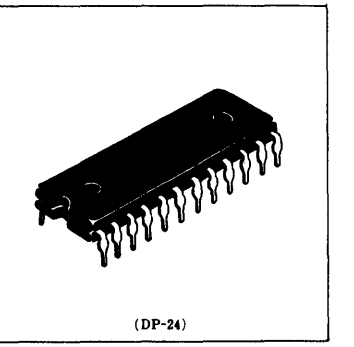


HM6117P-3, HM6117P-4

2048-word×8-bit High Speed Static CMOS RAM

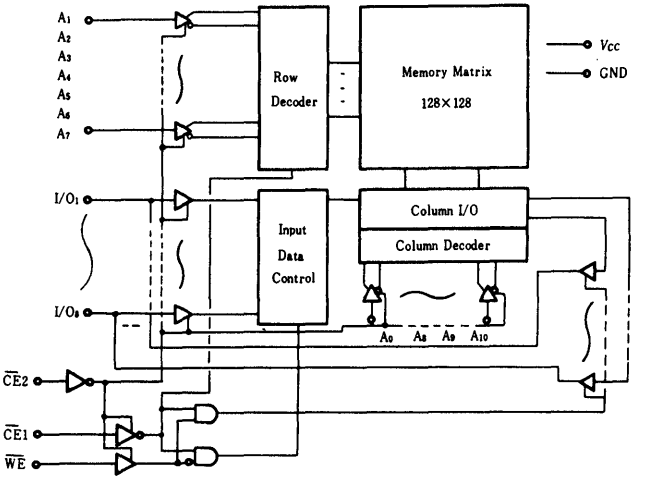
■FEATURES

- Single 5V Supply and High Density 24 pin Package.
- High Speed: Fast Access Time 150ns/200ns (max.)
- Low Power Standby and Low Power Operation: Standby: 100μW (typ.) Operation: 200mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time

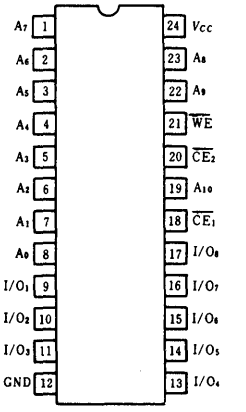


(DP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	*−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

* Pulse width 50ns : −3.5V

■TRUTH TABLE

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin
H	×	×	Not Selected	I_{CCL1}	High Z
×	H	×	Not Selected	I_{CCL2}	High Z
L	L	H	Read	I_{CC}	Dout
L	L	L	Write	I_{CC}	Din

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0°C to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	3.5	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−3.0*	—	0.8	V

* Pulse width : 50ns, DC : $V_{IL_{min}}$ = −0.3V

■DC AND OPERATING CHARACTERISTICS (Ta=0℃ to +70℃, V_{CC}=5V±10%, GND=0V)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{IN}=GND to V_{CC}	—	—	10	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CE}_1 = V_{IH}$ or $\overline{CE}_2 = V_{IH}$ $V_{I/O}$=GND to V_{CC}	—	—	10	μA
Operating Power Supply Current : DC	I_{CC}	$\overline{CE}_1 = \overline{CE}_2 = V_{IL}$, $I_{I/O}$=0mA	—	40	80	mA
Average Operating Current	I_{CC1}	Min cycle, duty=100% $\overline{CE}_1 = V_{IL}$, $\overline{CE}_2 = V_{IL}$	—	40	80	mA
Standby Power Supply Current (1) : DC	I_{CCL1}*	$\overline{CE}_1 \geq V_{CC}-0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	—	0.02	2	mA
Standby Power Supply Current (2) : DC	I_{CCL2}*	$\overline{CE}_2 \geq V_{CC}-0.2V$	—	0.02	2	mA
Output low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	V

Notes : 1) Typical limits are at V_{CC}=5.0V, Ta=+25°C
2) * : $V_{IL_{min}}$ = −0.3V

■CAPACITANCE (Ta=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (Ta=0℃ to +70℃, V_{CC}=5V±10% unless otherwise noted)

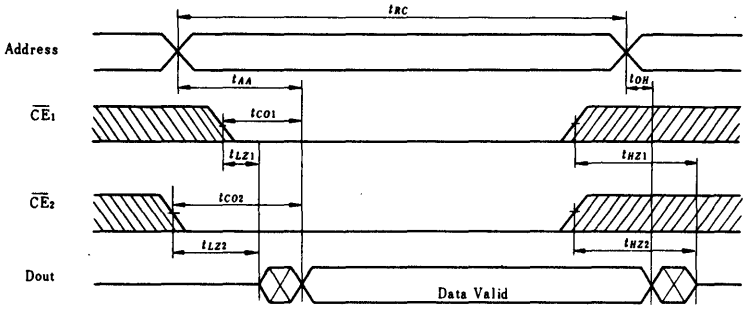
●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1 TTL Gate and C_L=100pF (including scope and jig)

●READ CYCLE

Item	Symbol	HM6117P-3		HM6117P-4		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	150	—	200	—	ns
Address Access Time	t_{AA}	—	150	—	200	ns
Chip Enable ($\overline{CE}_1$) to Output	t_{CO1}	—	150	—	200	ns
Chip Enable ($\overline{CE}_2$) to Output	t_{CO2}	—	150	—	200	ns
Chip Enable ($\overline{CE}_1$) to Output in Low Z	t_{LZ1}	10	—	10	—	ns
Chip Enable ($\overline{CE}_2$) to Output in Low Z	t_{LZ2}	10	—	10	—	ns
Chip Disable ($\overline{CE}_1$) to Output in High Z	t_{HZ1}	0	70	0	80	ns
Chip Disable ($\overline{CE}_2$) to Output in High Z	t_{HZ2}	0	70	0	80	ns
Output Hold from Address Change	t_{OH}	15	—	15	—	ns

● TIMING WAVEFORM OF READ CYCLE (Notes 1)

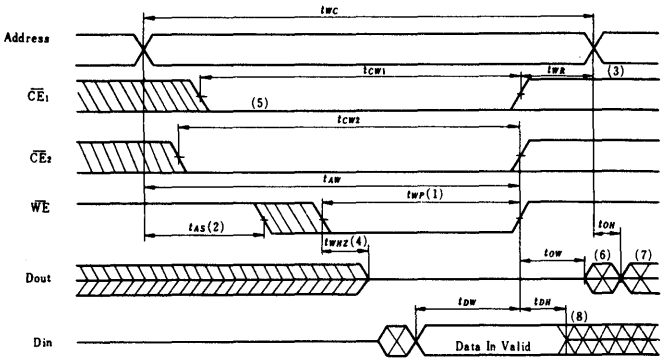


NOTES: 1. $\overline{WE}$ is High for Read Cycle.

● WRITE CYCLE

Item	Symbol	HM6117P-3		HM6117P-4		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	150	—	200	—	ns
Chip Enable ($\overline{CE}_1$) to End of Write	t_{CW1}	100	—	120	—	ns
Chip Enable ($\overline{CE}_2$) to End of Write	t_{CW2}	110	—	130	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	ns
Address Valid to End of Write	t_{AW}	130	—	150	—	ns
Write Pulse Width	t_{WP}	100	—	120	—	ns
Write Recovery Time	t_{WR}	15	—	15	—	ns
Write to Output in High Z	t_{WHZ}	0	60	0	70	ns
Data to Write Time Overlap	t_{DW}	50	—	60	—	ns
Data Hold from Write Time	t_{DH}	20	—	20	—	ns
Output Active from End of Write	t_{OW}	10	—	10	—	ns

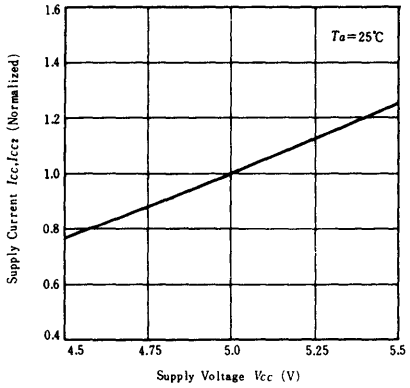
● TIMING WAVEFORM OF WRITE CYCLE



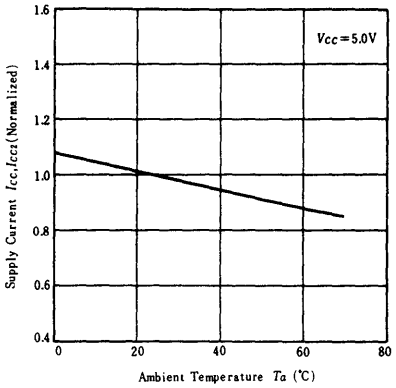
NOTES: 1 A write occurs during the overlap (t_{WP}) of low $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{WE}$.

2. t_{AS} is measured from the address changes to the biginning of the write.
3. t_{WR} is measured from the earlier of $\overline{CE}_1$, $\overline{CE}_2$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE}_1$ or $\overline{CE}_2$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transitions, output remain in a high impedance state.
6. Dout is the same phase of write data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CE}_1$ and $\overline{CE}_2$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

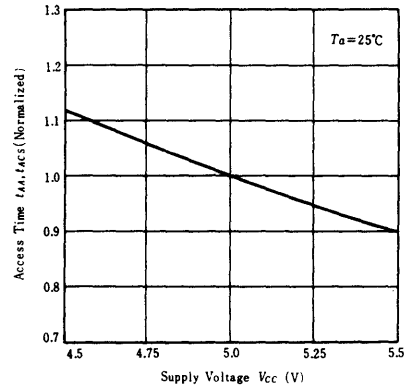
SUPPLY CURRENT vs. SUPPLY VOLTAGE



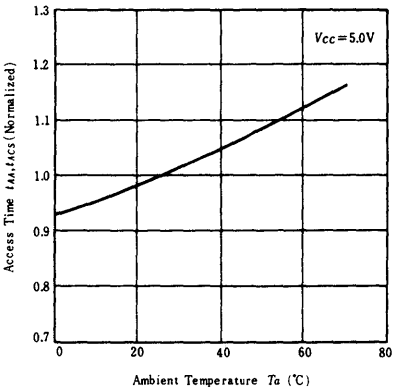
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



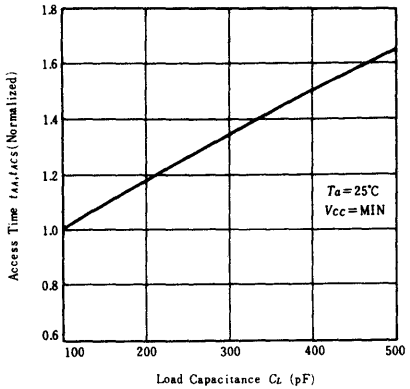
ACCESS TIME vs. SUPPLY VOLTAGE



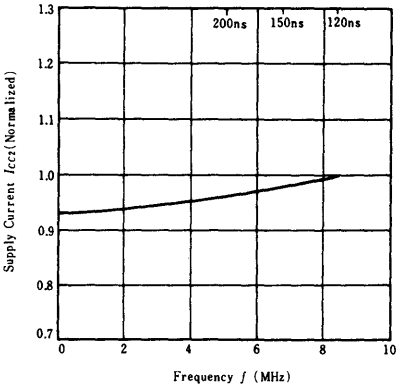
ACCESS TIME vs. AMBIENT TEMPERATURE



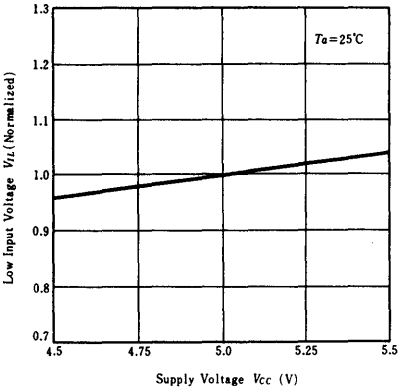
ACCESS TIME vs. LOAD CAPACITANCE



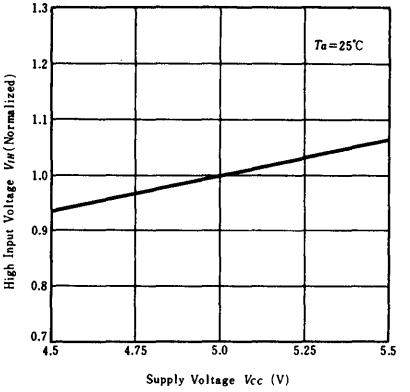
SUPPLY CURRENT vs. FREQUENCY



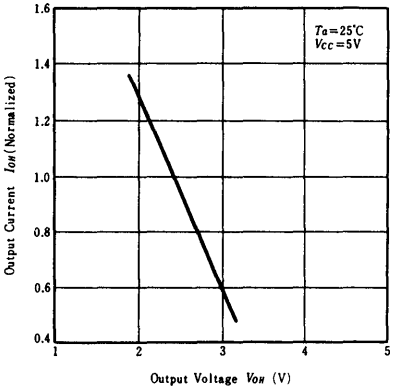
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



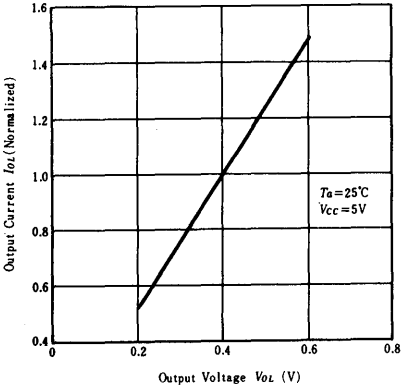
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE

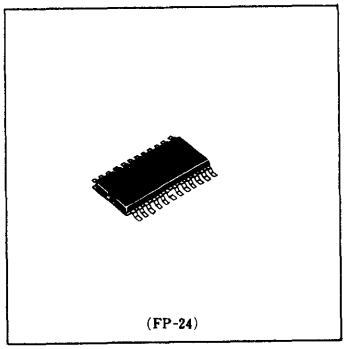


HM6117FP-3, HM6117FP-4

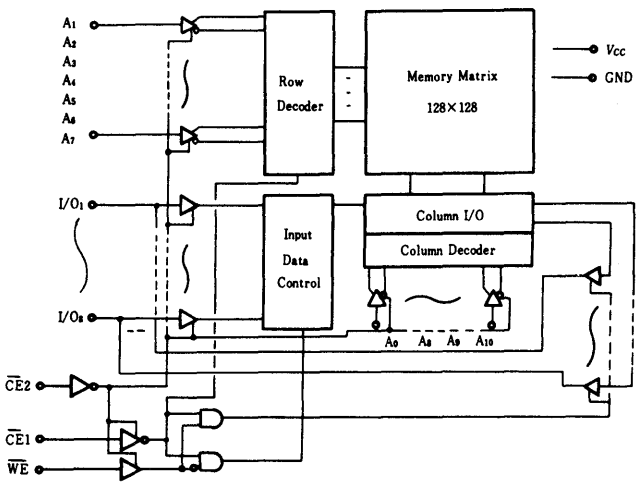
2048-word×8-bit High Speed Static CMOS RAM

■FEATURES

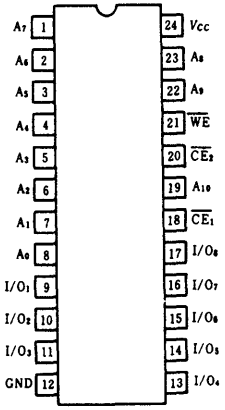
- High Density Small Sized Package
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply and High Density 24 pin Package.
- High Speed: Fast Access Time 150ns/200ns (max.)
- Low Power Standby and Low Power Operation: Standby: 100μW (typ.) Operation: 200mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time



■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	*−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

* Pulse width 50ns : −3.5V

■TRUTH TABLE

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin
H	×	×	Not Selected	I_{CCL1}	High Z
×	H	×	Not Selected	I_{CCL2}	High Z
L	L	H	Read	I_{CC}	Dout
L	L	L	Write	I_{CC}	Din

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0°C to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	3.5	6.0	V
Input low (logic 0) Voltage	V_{IL}	−3.0*	—	0.8	V

* Pulse width : 50ns, DC : $V_{IL_{min}}$ = −0.3V

■DC AND OPERATING CHARACTERISTICS (Ta=0℃ to +70℃, V_{CC}=5V±10%, GND=0V)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{IN}=GND to V_{CC}	—	—	10	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CE_1}=V_{IH}$ or $\overline{CE_2}=V_{IH}$ $V_{I/O}$=GND to V_{CC}	—	—	10	μA
Operating Power Supply Current : DC	I_{CC}	$\overline{CE_1}=\overline{CE_2}=V_{IL}$, $I_{I/O}$=0mA	—	40	80	mA
Average Operating Current	I_{CC1}	Min cycle, duty=100% $\overline{CE_1}=V_{IL}$, $\overline{CE_2}=V_{IL}$	—	40	80	mA
Standby Power Supply Current (1) : DC	I_{CCL1}*	$\overline{CE_1}\geqq V_{CC}-0.2V$, $V_{IN}\geqq V_{CC}-0.2V$ or $V_{IN}\leqq 0.2V$	—	0.02	2	mA
Standby Power Supply Current (2) : DC	I_{CCL2}*	$\overline{CE_2}\geqq V_{CC}-0.2V$	—	0.02	2	mA
Output low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	V

Notes : 1) Typical limits are at V_{CC}=5.0V, Ta=+25°C
2) * : $V_{IL_{min}}$ = −0.3V

■CAPACITANCE (Ta=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (Ta=0℃ to +70℃, V_{CC}=5V±10% unless otherwise noted)

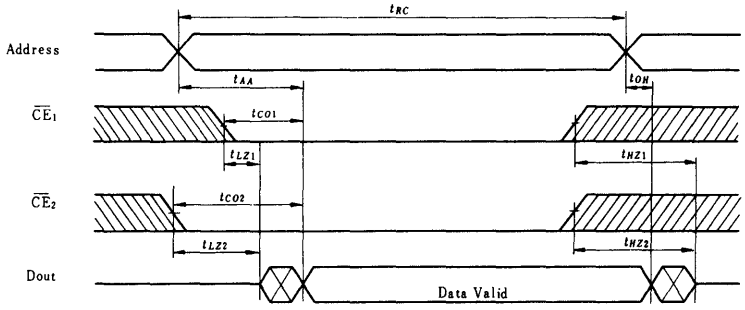
●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

●READ CYCLE

Item	Symbol	HM6117P-3		HM6117P-4		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	150	—	200	—	ns
Address Access Time	t_{AA}	—	150	—	200	ns
Chip Enable ($\overline{CE_1}$) to Output	t_{CO1}	—	150	—	200	ns
Chip Enable ($\overline{CE_2}$) to Output	t_{CO2}	—	150	—	200	ns
Chip Enable ($\overline{CE_1}$) to Output in Low Z	t_{LZ1}	10	—	10	—	ns
Chip Enable ($\overline{CE_2}$) to Output in Low Z	t_{LZ2}	10	—	10	—	ns
Chip Disable ($\overline{CE_1}$) to Output in High Z	t_{HZ1}	0	70	0	80	ns
Chip Disable ($\overline{CE_2}$) to Output in High Z	t_{HZ2}	0	70	0	80	ns
Output Hold from Address Change	t_{OH}	15	—	15	—	ns

● TIMING WAVEFORM OF READ CYCLE (Notes 1)

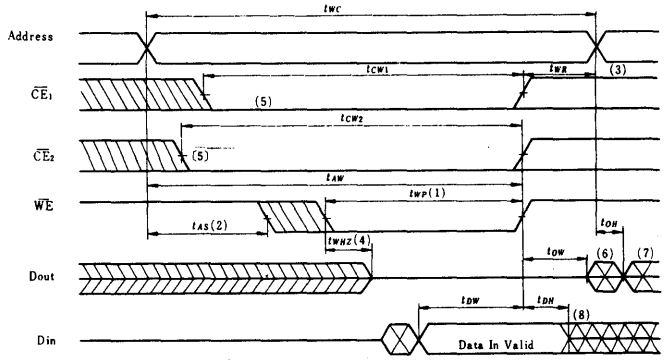


NOTES: 1. $\overline{WE}$ is High for Read Cycle.

● WRITE CYCLE

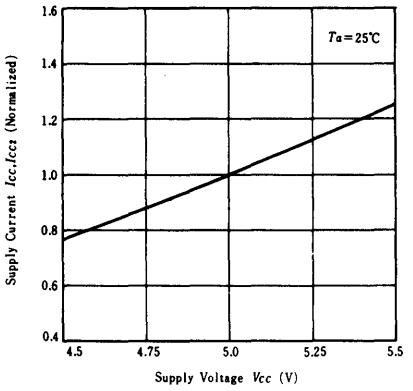
Item	Symbol	HM6117P-3		HM6117P-4		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	150	—	200	—	ns
Chip Enable ($\overline{CE}_1$) to End of Write	t_{CW1}	100	—	120	—	ns
Chip Enable ($\overline{CE}_2$) to End of Write	t_{CW2}	110	—	130	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	ns
Address Valid to End of Write	t_{AW}	130	—	150	—	ns
Write Pulse Width	t_{WP}	100	—	120	—	ns
Write Recovery Time	t_{WR}	15	—	15	—	ns
Write to Output in High Z	t_{WHZ}	0	60	0	70	ns
Data to Write Time Overlap	t_{DW}	50	—	60	—	ns
Data Hold from Write Time	t_{DH}	20	—	20	—	ns
Output Active from End of Write	t_{OW}	10	—	10	—	ns

● TIMING WAVEFORM OF WRITE CYCLE

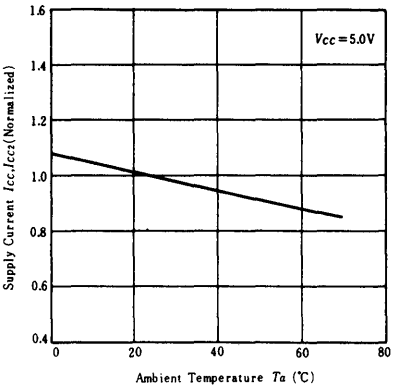


NOTES:
1. A write occurs during the overlap (t_{WP}) of low $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{WE}$.
2. t_{AS} is measured from the address changes to the biginning of the write.
3. t_{WR} is measured from the earlier of $\overline{CE}_1$, $\overline{CE}_2$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE}_1$ or $\overline{CE}_2$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transitions, output remain in a high impedance state.
6. Dout is the same phase of write data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CE}_1$ and $\overline{CE}_2$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

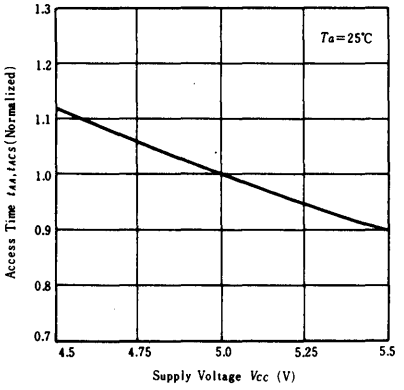
SUPPLY CURRENT vs. SUPPLY VOLTAGE



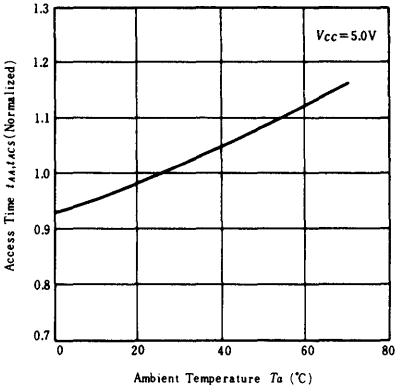
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



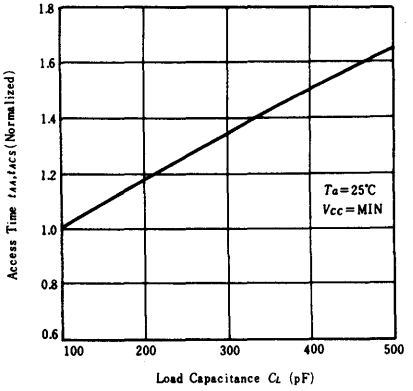
ACCESS TIME vs. SUPPLY VOLTAGE



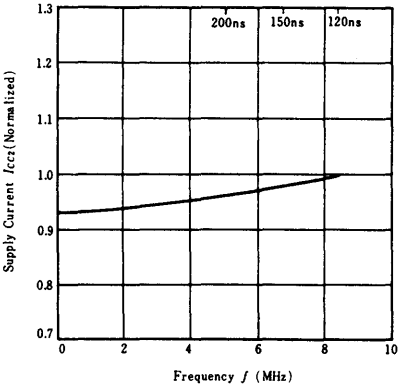
ACCESS TIME vs. AMBIENT TEMPERATURE



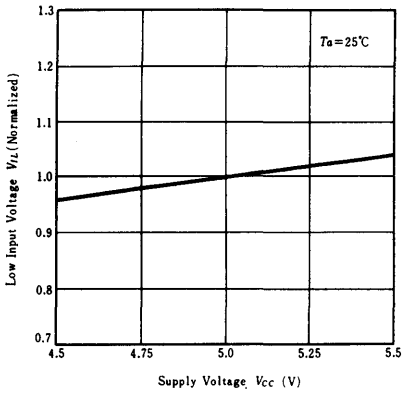
ACCESS TIME vs. LOAD CAPACITANCE



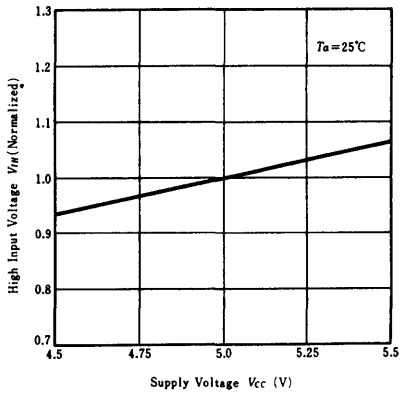
SUPPLY CURRENT vs. FREQUENCY



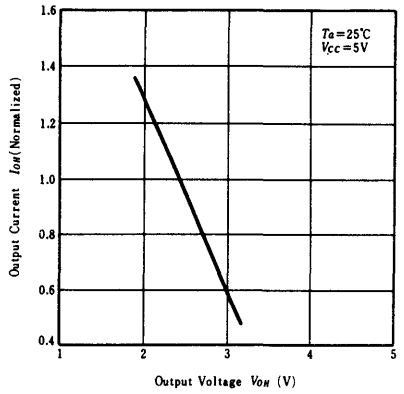
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



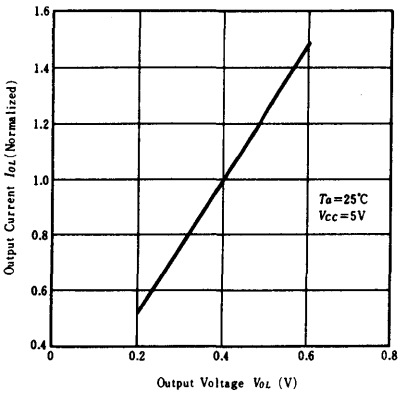
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE

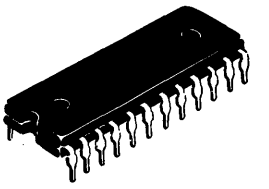


HM6117LP-3, HM6117LP-4

2048-word×8-bit High Speed Static CMOS RAM

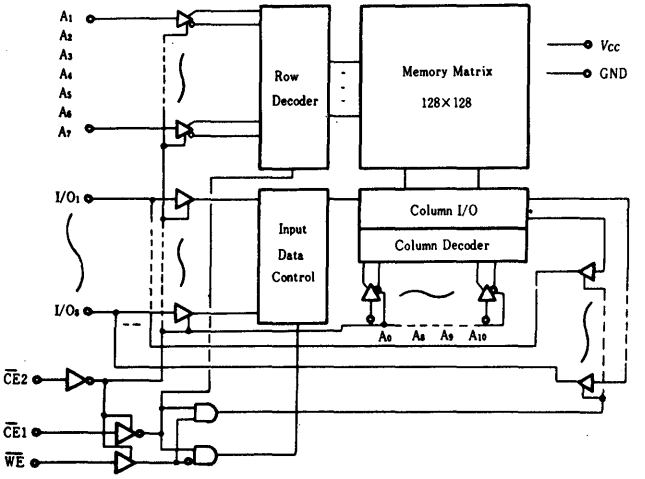
■FEATURES

- Single 5V Supply and High Density 24 Pin Package.
- High Speed: Fast Access Time 150ns/200ns max.
- Low Power Standby and Low Power Operation;
  Standby: 10μW (typ.) Two Chip Enable Input for Battery Back up
  Operation: 180mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

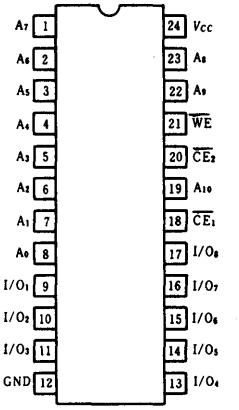


(DP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	*−0.5 to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse width 50ns: −3.5V

■TRUTH TABLE

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin
H	×	×	Not Selected	I_{CCL1}	High Z
×	H	×	Not Selected	I_{CCL2}	High Z
L	L	H	Read	I_{CC}	Dout
L	L	L	Write	I_{CC}	Din

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0°C to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	3.5	6.0	V
Input low (logic 0) Voltage	V_{IL}	−3.0*	—	0.8	V

* Pulse Width : 50ns, DC : $V_{IL_{min}}$ = −0.3V.

■DC AND OPERATING CHARACTERISTICS (Ta=0°C to +70°C, V_{CC}=5V±10%, GND=0V)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{IN}=GND to V_{CC}	—	—	2	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CE_1}=V_{IH}$ or $\overline{CE_2}=V_{IH}$ $V_{I/O}$=GND to V_{CC}	—	—	2	μA
Operating Power Supply Current : DC	I_{CC}	$\overline{CE_1}=\overline{CE_2}=V_{IL}$, $I_{I/O}$=0mA	—	35	70	mA
Average Operating Current	I_{CC1}	Min cycle, duty=100% $\overline{CE_1}=V_{IL}$, $\overline{CE_2}=V_{IL}$	—	35	70	mA
Standby Power Supply Current (1) : DC	I_{CCL1}*	$\overline{CE_1} \geqq V_{CC}-0.2V$ $V_{IN} \geqq V_{CC}-0.2V$ or $V_{IN} \leqq 0.2V$	—	2	50	μA
Standby Power Supply Current (2) : DC	I_{CCL2}*	$\overline{CE_2} \geqq V_{CC}-0.2V$	—	2	50	μA
Output low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	V

Notes : 1) Typical limits are at V_{CC}=5.0V, Ta=+25°C
2) * : $V_{IL_{min}}$ = −0.3V

■CAPACITANCE (Ta=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

Note : 1) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (Ta=0°C to +70°C, V_{CC}=5V±10% unless otherwise noted)

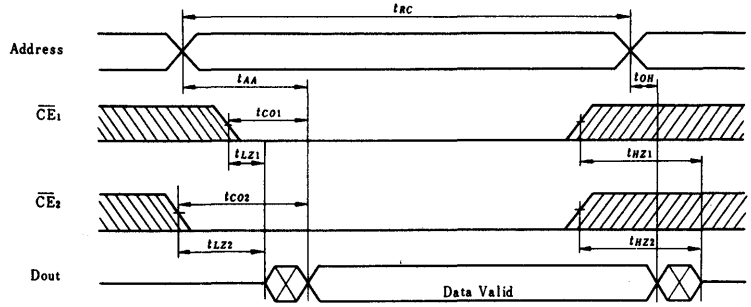
●AC TEST CONDITIONS

Input Pulse Levels ..... 0.8V to 2.4V
Input Rise and Fall Times 10ns
Input and Output Timing Reference Levels ... 1.5V
Output Load ..... 1 TTL Gate and C_L = 100pF (Including Scope & Jig)

●READ CYCLE

Item	Symbol	HM6117LP-3		HM6117LP-4		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	150	—	200	—	ns
Address Access Time	t_{AA}	—	150	—	200	ns
Chip Enable ($\overline{CE_1}$) to Output	t_{CO1}	—	150	—	200	ns
Chip Enable ($\overline{CE_2}$) to Output	t_{CO2}	—	150	—	200	ns
Chip Enable ($\overline{CE_1}$) to Output in Low Z	t_{LZ1}	10	—	10	—	ns
Chip Enable ($\overline{CE_2}$) to Output in Low Z	t_{LZ2}	10	—	10	—	ns
Chip Disable ($\overline{CE_1}$) to Output in High Z	t_{HZ1}	0	70	0	80	ns
Chip Disable ($\overline{CE_2}$) to Output in High Z	t_{HZ2}	0	70	0	80	ns
Output Hold from Address Change	t_{OH}	15	—	15	—	ns

● TIMING WAVEFORM OF READ CYCLE (Notes 1)

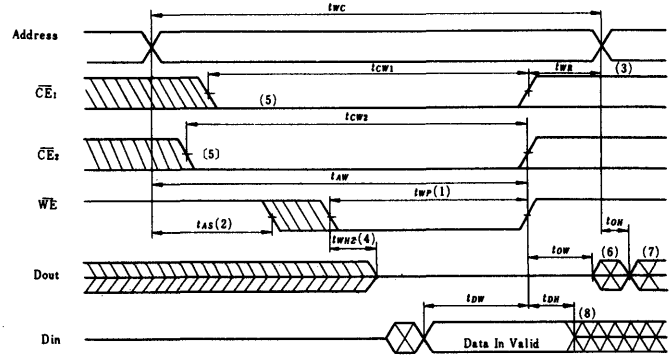


NOTES: 1. $\overline{WE}$ is High for Read Cycle.

● WRITE CYCLE

Item	Symbol	HM6117LP-3		HM6117LP-4		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	150	—	200	—	ns
Chip Enable ($\overline{CE}_1$) to End of Write	t_{CW1}	100	—	120	—	ns
Chip Enable ($\overline{CE}_2$) to End of Write	t_{CW2}	110	—	130	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	ns
Address Valid to End of Write	t_{AW}	130	—	150	—	ns
Write Pulse Width	t_{WP}	100	—	120	—	ns
Write Recovery Time	t_{WR}	15	—	15	—	ns
Write to Output in High Z	t_{WHZ}	0	60	0	70	ns
Data to Write Time Overlap	t_{DW}	50	—	60	—	ns
Data Hold from Write Time	t_{DH}	20	—	20	—	ns
Output Active from End of Write	t_{OW}	10	—	10	—	ns

● TIMING WAVEFORM OF WRITE CYCLE



NOTES: 1 A write occurs during the overlap (t_{WP}) of low $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{WE}$.

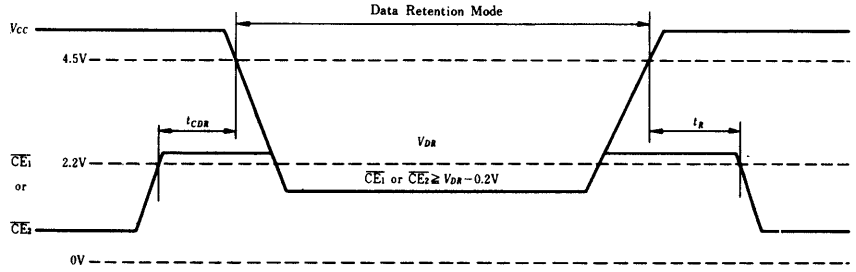
2. t_{AS} is measured from the address changes to the biginning of the write.
3. t_{WR} is measured from the earlier of $\overline{CE}_1$, $\overline{CE}_2$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE}_1$ or $\overline{CE}_2$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transitions, output remain in a high impedance state.
6. Dout is the same phase of write data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CE}_1$ and $\overline{CE}_2$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■LOW V_{CC} DATA RETENTION CHARACTERISTICS (Ta=0°C to +70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR1}	$\overline{CE_1} \geqq V_{CC}-0.2V$, $V_{IN} \geqq V_{CC}-0.2V$ or $V_{IN} \leqq 0.2V$	2.0	—	—	V
V_{CC} for Data Retention	V_{DR2}	$\overline{CE_2} \geqq V_{CC}-0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR1}	V_{CC}=3.0V, $\overline{CE_1} \geqq 2.8V$, $V_{IN} \geqq 2.8V$ or $V_{IN} \leqq 0.2V$	—	—	30*	μA
Data Retention Current	I_{CCDR2}	V_{CC}=3.0V, $\overline{CE_2} \geqq V_{CC}-0.2V$	—	—	30*	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}**	—	—	ns

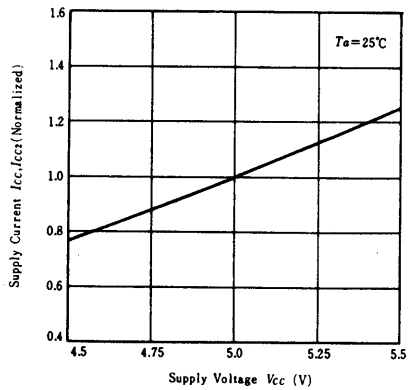
* 10μA max at Ta=0°C to +40°C, V_{IL} min=−0.3V
** t_{RC}=Read Cycle Time

●LOW V_{CC} DATA RETENTION WAVEFORM

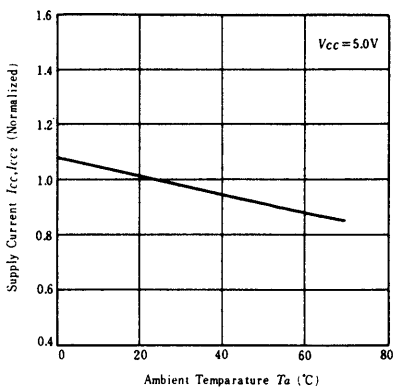


NOTE: 1. $\overline{CE_2}$ controls Address buffer, $\overline{WE}$ buffer, $\overline{CE_1}$ buffer and D_{IN} buffer. If $\overline{CE_2}$ controls data retention mode, V_{IN} level (address, $\overline{WE}$, $\overline{CE_1}$, $D_{I/O}$) can be in the high impedance state. If $\overline{CE_1}$ controls data retention mode, V_{IN} level (address, $\overline{WE}$, $\overline{DE_2}$, $D_{I/O}$) must be $V_{IN} \geqq V_{CC}-0.2V$ or $V_{IN} \leqq 0.2V$.

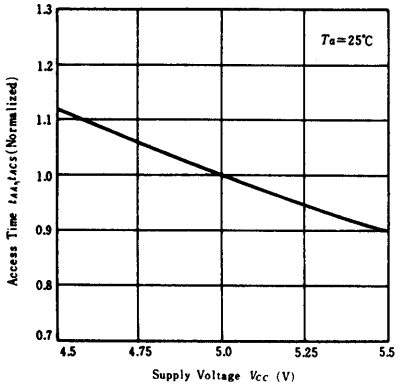
SUPPLY CURRENT vs. SUPPLY VOLTAGE



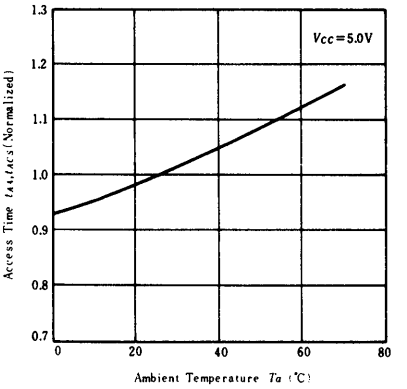
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



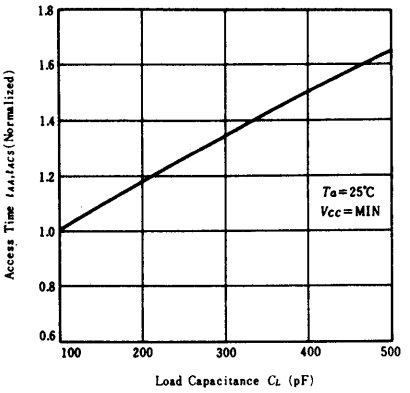
ACCESS TIME vs. SUPPLY VOLTAGE



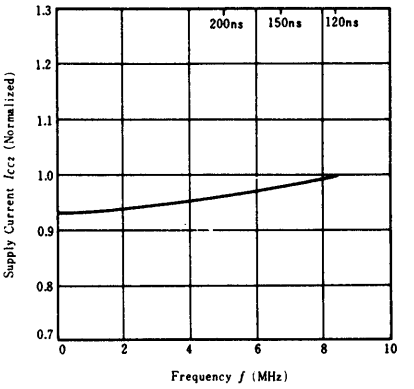
ACCESS TIME vs. AMBIENT TEMPERATURE



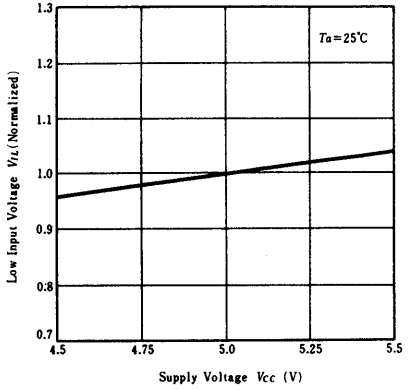
ACCESS TIME vs. LOAD CAPACITANCE



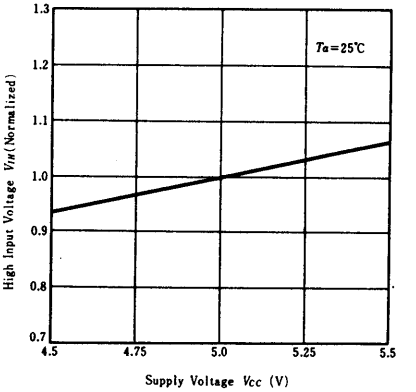
SUPPLY CURRENT vs. FREQUENCY



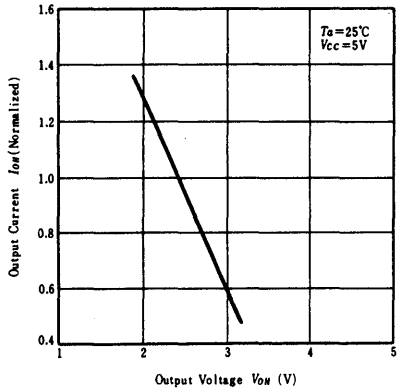
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



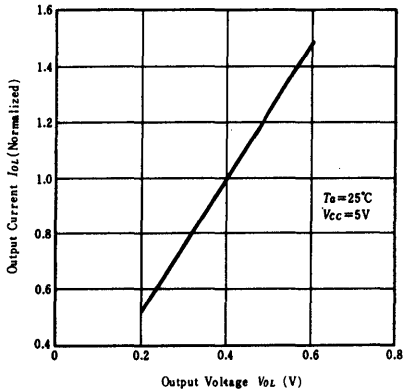
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



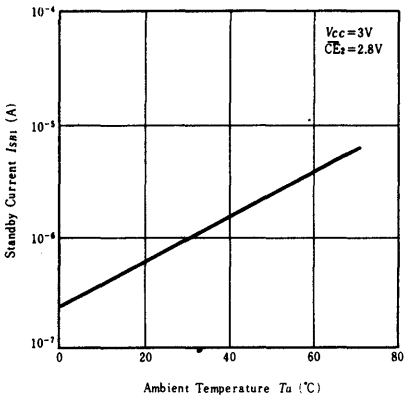
OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



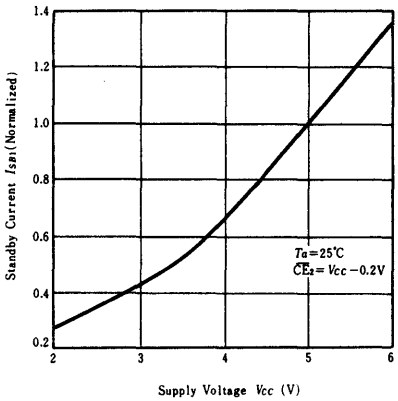
OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE



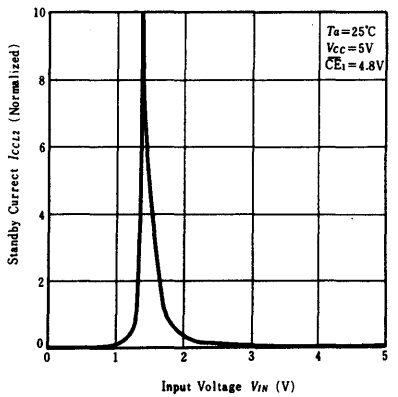
STAND-BY CURRENT vs. AMBIENT TEMPERATURE



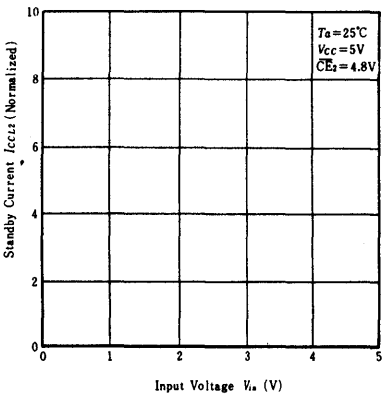
STAND-BY CURRENT vs. SUPPLY VOLTAGE



STAND-BY CURRENT vs. INPUT VOLTAGE



STAND-BY CURRENT vs. INPUT VOLTAGE

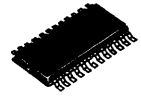


HM6117LFP-3, HM6117LFP-4

2048-word×8-bit High Speed Static CMOS RAM

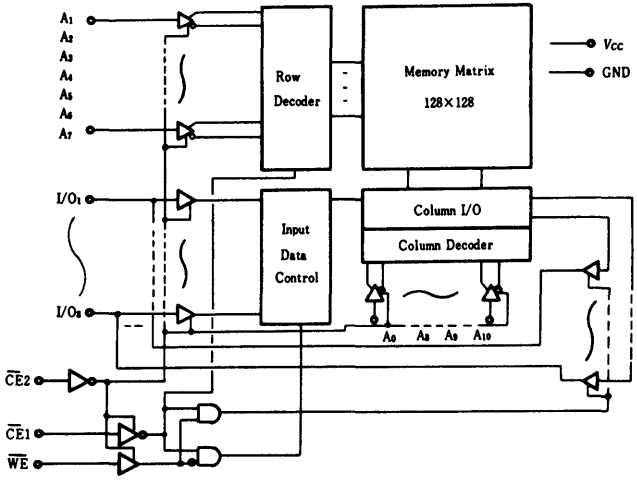
■FEATURES

- High Density Small-sized Packaged
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply
- High Speed: Fast Access Time 150ns/200ns max.
- Low Power Standby and Low Power Operation;
  Standby: 10μW (typ.) Two Chip Enable Input for Battery Back up
  Operation: 180mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

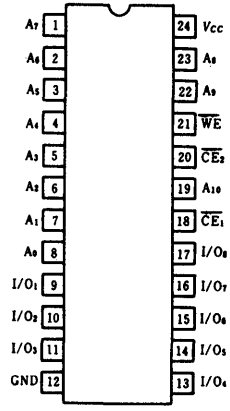


(FP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	*−0.5 to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse width 50ns : −3.5V

■TRUTH TABLE

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin
H	×	×	Not Selected	I_{CCL1}	High Z
×	H	×	Not Selected	I_{CCL2}	High Z
L	L	H	Read	I_{CC}	Dout
L	L	L	Write	I_{CC}	Din

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0℃ to +70℃)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	3.5	6.0	V
Input low (logic 0) Voltage	V_{IL}	−3.0*	—	0.8	V

* Pulse Width : 50ns, DC : $V_{IL_{min}}$ = −0.3V.

■DC AND OPERATING CHARACTERISTICS (Ta=0℃ to +70℃, V_{CC}=5V±10%, GND=0V)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{IN}=GND to V_{CC}	—	—	2	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CE_1}=V_{IH}$ or $\overline{CE_2}=V_{IH}$ $V_{I/O}$=GND to V_{CC}	—	—	2	μA
Operating Power Supply Current : DC	I_{CC}	$\overline{CE_1}=\overline{CE_2}=V_{IL}$, $I_{I/O}$=0mA	—	35	70	mA
Average Operating Current	I_{CC1}	Min cycle, duty=100% $\overline{CE_1}=V_{IL}$, $\overline{CE_2}=V_{IL}$	—	35	70	mA
Standby Power Supply Current (1) : DC	I_{CCL1}*	$\overline{CE_1}\geqq V_{CC}-0.2V$ $V_{IN}\geqq V_{CC}-0.2V$ or $V_{IN}\leqq 0.2V$	—	2	50	μA
Standby Power Supply Current (2) : DC	I_{CCL2}*	$\overline{CE_2}\geqq V_{CC}-0.2V$	—	2	50	μA
Output low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	V

Notes : 1) Typical limits are at V_{CC}=5.0V, Ta=+25℃
2) * : $V_{IL_{min}}$=−0.3V

■CAPACITANCE (Ta=25℃, f=1.0MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

Note : 1) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (Ta=0℃ to +70℃, V_{CC}=5V±10% unless otherwise noted)

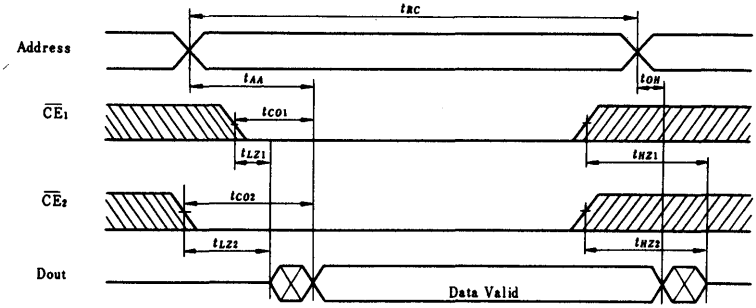
●AC TEST CONDITIONS

Input Pulse Levels ..... 0.8V to 2.4V
Input Rise and Fall Times 10ns
Input and Output Timing Reference Levels ... 1.5V
Output Load ..... 1 TTL Gate and C_L = 100pF (Including Scope & Jig)

●READ CYCLE

Item	Symbol	HM6117LFP-3		HM6117LFP-4		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	150	—	200	—	ns
Address Access Time	t_{AA}	—	150	—	200	ns
Chip Enable ($\overline{CE_1}$) to Output	t_{CO1}	—	150	—	200	ns
Chip Enable ($\overline{CE_2}$) to Output	t_{CO2}	—	150	—	200	ns
Chip Enable ($\overline{CE_1}$) to Output in Low Z	t_{LZ1}	10	—	10	—	ns
Chip Enable ($\overline{CE_2}$) to Output in Low Z	t_{LZ2}	10	—	10	—	ns
Chip Disable ($\overline{CE_1}$) to Output in High Z	t_{HZ1}	0	70	0	80	ns
Chip Disable ($\overline{CE_2}$) to Output in High Z	t_{HZ2}	0	70	0	80	ns
Output Hold from Address Change	t_{OH}	15	—	15	—	ns

● TIMING WAVEFORM OF READ CYCLE (Notes 1)

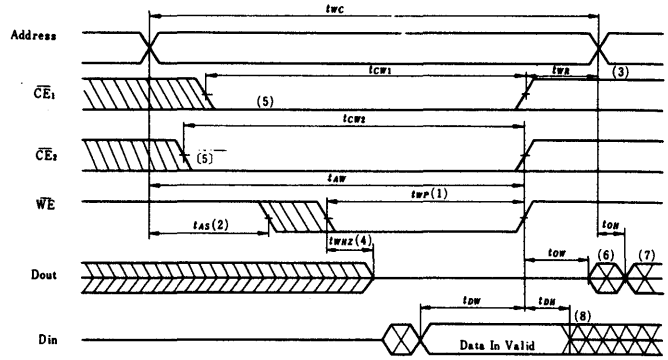


NOTES: 1. $\overline{WE}$ is High for Read Cycle.

● WRITE CYCLE

Item	Symbol	HM6117LFP-3		HM6117LFP-4		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	150	—	200	—	ns
Chip Enable ($\overline{CE}_1$) to End of Write	t_{CW1}	100	—	120	—	ns
Chip Enable ($\overline{CE}_2$) to End of Write	t_{CW2}	110	—	130	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	ns
Address Valid to End of Write	t_{AW}	130	—	150	—	ns
Write Pulse Width	t_{WP}	100	—	120	—	ns
Write Recovery Time	t_{WR}	15	—	15	—	ns
Write to Output in High Z	t_{WHZ}	0	60	0	70	ns
Data to Write Time Overlap	t_{DW}	50	—	60	—	ns
Data Hold from Write Time	t_{DH}	20	—	20	—	ns
Output Active from End of Write	t_{OW}	10	—	10	—	ns

● TIMING WAVEFORM OF WRITE CYCLE



NOTES: 1 A write occurs during the overlap (t_{WP}) of low $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{WE}$.

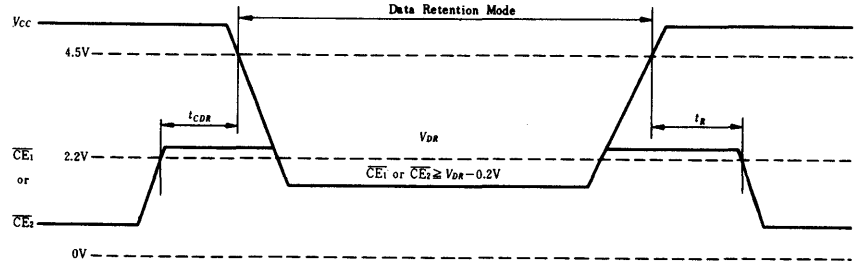
2. t_{AS} is measured from the address changes to the biginning of the write.
3. t_{WR} is measured from the earlier of $\overline{CE}_1$, $\overline{CE}_2$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE}_1$ or $\overline{CE}_2$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transitions, output remain in a high impedance state.
6. Dout is the same phase of write data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CE}_1$ and $\overline{CE}_2$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■LOW V_{CC} DATA RETENTION CHARACTERISTICS (Ta=0°C to +70°C)

Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR1}	$\overline{CE_1} \geqq V_{CC}-0.2V$, $V_{IN} \geqq V_{CC}-0.2V$ or $V_{IN} \leqq 0.2V$	2.0	—	—	V
V_{CC} for Data Retention	V_{DR2}	$\overline{CE_2} \geqq V_{CC}-0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR1}	V_{CC}=3.0V, $\overline{CE_1} \geqq 2.8V$, $V_{IN} \geqq 2.8V$ or $V_{IN} \leqq 0.2V$	—	—	30*	μA
Data Retention Current	I_{CCDR2}	V_{CC}=3.0V, $\overline{CE_2} \geqq V_{CC}-0.2V$	—	—	30*	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}**	—	—	ns

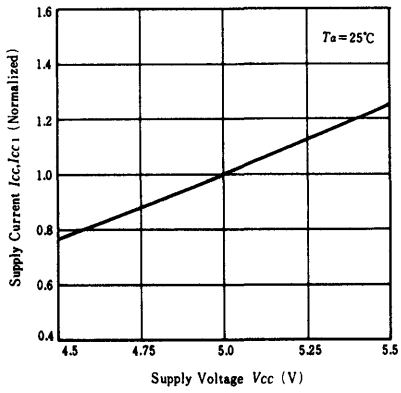
* 10μA max at Ta=0°C to +40°C, V_{IL} min=−0.3V
** t_{RC}=Read Cycle Time

●LOW V_{CC} DATA RETENTION WAVEFORM

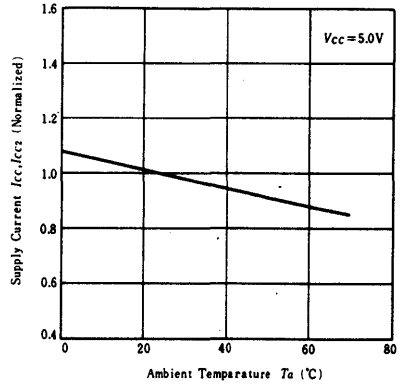


NOTE: 1. $\overline{CE_2}$ controls Address buffer, $\overline{WE}$ buffer, $\overline{CE_1}$ buffer and D_{IN} buffer. If $\overline{CE_2}$ controls data retention mode, V_{IN} level (address, $\overline{WE}$, $\overline{CE_1}$, $D_{I/O}$) can be in the high impedance state. If $\overline{CE_1}$ controls data retention mode, V_{IN} level (address, $\overline{WE}$, $\overline{CE_2}$, $D_{I/O}$) must be $V_{IN} \geqq V_{CC}-0.2V$ or $V_{IN} \leqq 0.2V$.

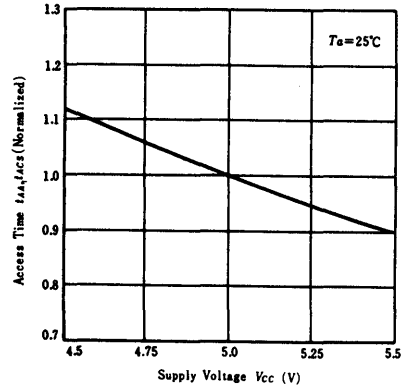
SUPPLY CURRENT vs. SUPPLY VOLTAGE



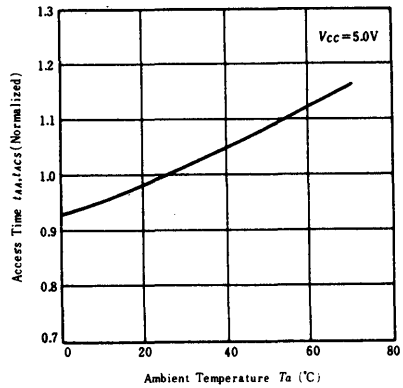
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



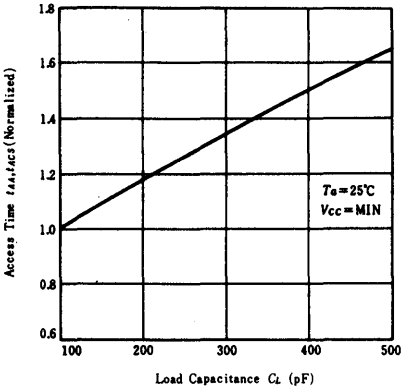
ACCESS TIME vs. SUPPLY VOLTAGE



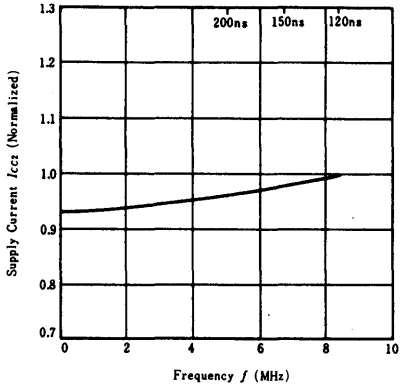
ACCESS TIME vs. AMBIENT TEMPERATURE



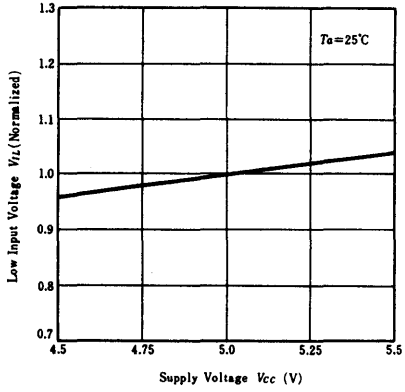
ACCESS TIME vs. LOAD CAPACITANCE



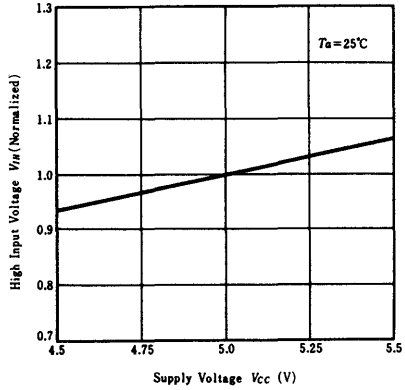
SUPPLY CURRENT vs. FREQUENCY



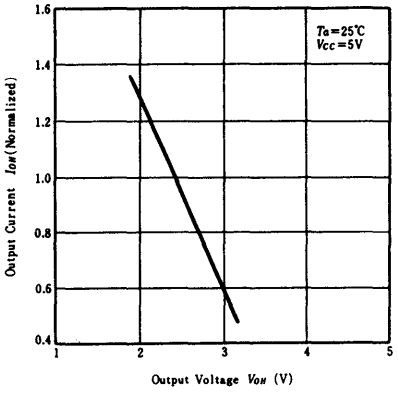
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



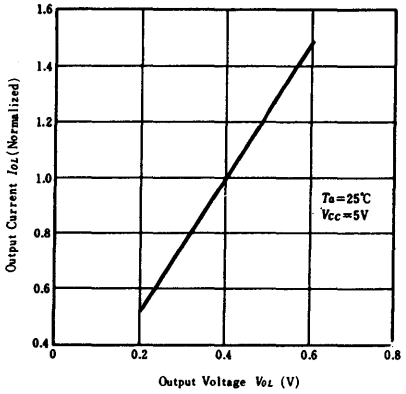
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



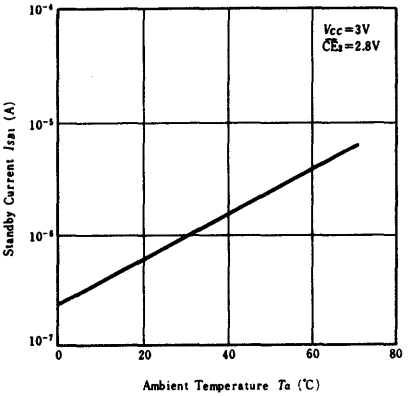
OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



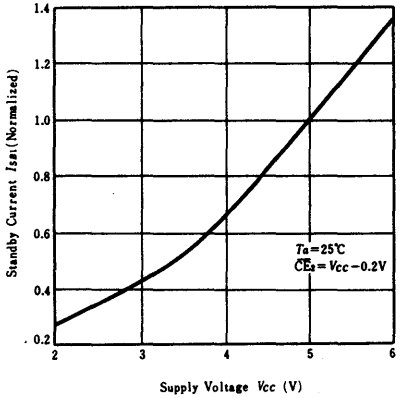
OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE



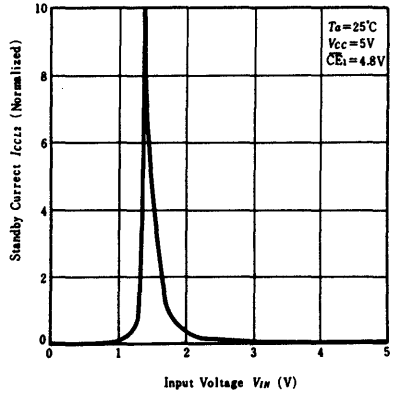
STAND-BY CURRENT vs. AMBIENT TEMPERATURE



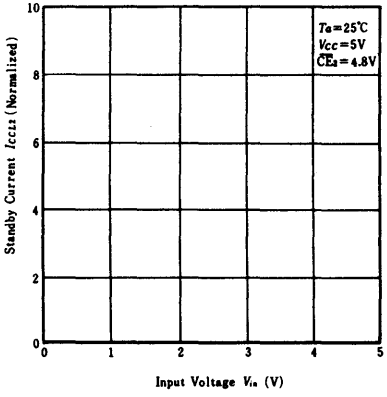
STAND-BY CURRENT vs. SUPPLY VOLTAGE



STAND-BY CURRENT vs. INPUT VOLTAGE



STAND-BY CURRENT vs. INPUT VOLTAGE



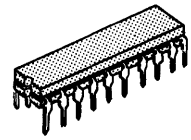
HM6168H-45, HM6168H-55, HM6168H-70, HM6168HP-45, HM6168HP-55, HM6168HP-70

4096-word×4-bit High Speed Static CMOS RAM

■FEATURES

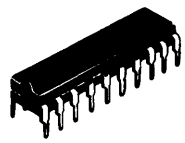
- High Speed: Fast Access Time 45/55/70 ns (max.)
- Single +5V Supply and High Density 20 Pin Package
- Low Power Standby and Low Power Operation;
  100μW typ. (Standby), 200mW typ. (Operation)
- Completely Static Memory
  No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible — All Inputs and Outputs

HM6168H-45/55/70



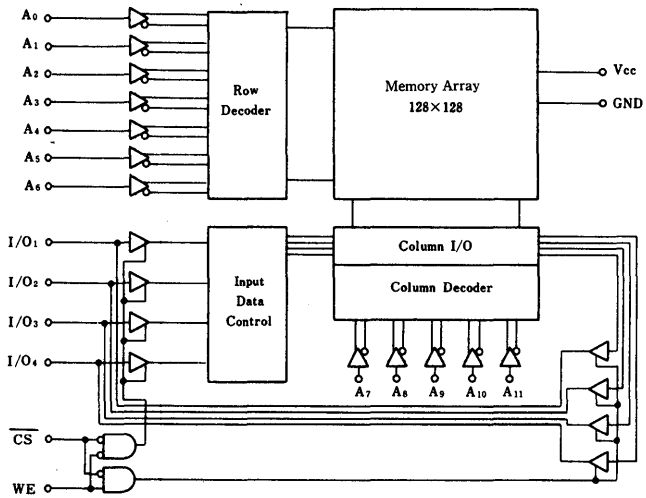
(DG-20)

HM6168HP-45/55/70

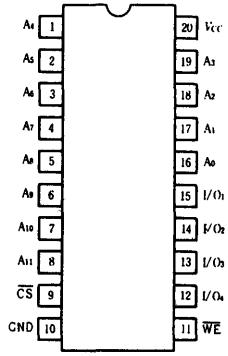


(DP-20)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_{IN}	−3.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

* Pulse Width 20ns, DC=−0.5V

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	X	Not selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle 1, 2
L	L	Write	I_{CC}	Din	Write Cycle 1, 2

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to + 70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*	–	0.8	V

* −3.0V (Pulse width 20ns)

■ DC AND OPERATING CHARACTERISTICS (V_{CC}=5V ±10%, GND=0V, Ta=0 to + 70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Imput Leakage Current	$\lvert I_{LI} \rvert$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}$=V_{IH}, $V_{I/O}$=GND to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	–	40	90	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	–	15	25	mA
Standby Power Supply Current(1)	I_{SB1}	$\overline{CS}$=V_{CC}−0.2V, V_{IN}≦0.2V or V_{IN}≧V_{CC}−0.2V	–	0.02	2.0	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4mA	2.4	–	–	V

Note: Typical limits are at V_{CC}=5.0V, Ta=25°C and specified loading.

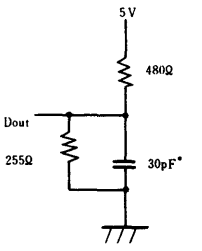
■ CAPACITANCE (Ta=25°C, f=1MHz)

Item	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{in}	V_{IN}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	8	pF

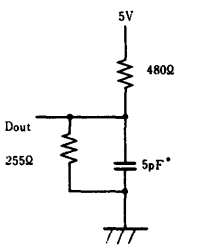
■ AC CHARACTERISTICS (V_{CC}=5V ±10%, Ta=0 to + 70°C, unless otherwise noted.)

• AC TEST CONDITION

- Input pulse levels: GND to 3.0V
- Input rise and fall times: 5ns
- Input and Output timing reference levels: 1.5V
- Output load: See Figure



Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW})

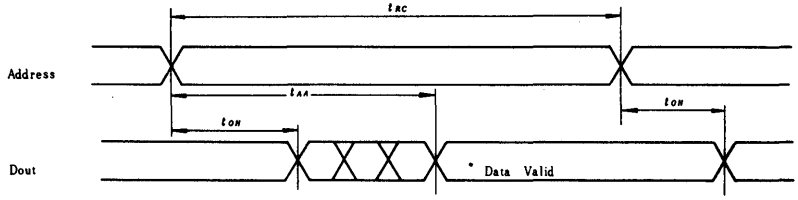
* Including scope and jig.

• READ CYCLE

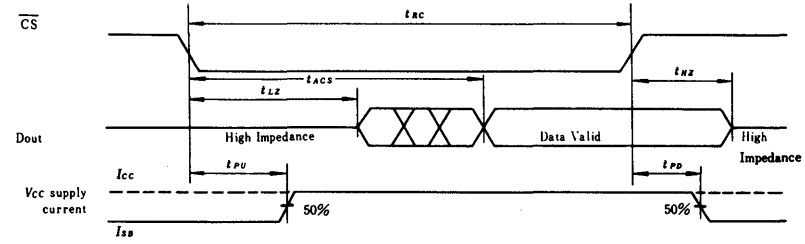
Item	Symbol	HM6168H/P-45		HM6168H/P-55		HM6168H/P-70		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	45	–	55	–	70	–	ns
Address Access Time	t_{AA}	–	45	–	55	–	70	ns
Chip Select Access Time	t_{ACS}	–	45	–	55	–	70	ns
Output Hold from Address Change	t_{OH}	5	–	5	–	5	–	ns
Chip Selection to Output in Low Z*	t_{LZ}	20	–	20	–	20	–	ns
Chip Deselection to Output in High Z*	t_{HZ}	0	20	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	0	–	ns
Chip Deselection to Power Down Time	t_{PD}	–	30	–	30	–	30	ns

* Transition is measured ±500mV for high impedance voltage with Load (B).
This parameter is sampled and not 100% tested.

• TIMING WAVEFORM OF READ CYCLE NO. 1[(1), (2)]



• TIMING WAVEFORM OF READ CYCLE NO. 2[(1), (3)]



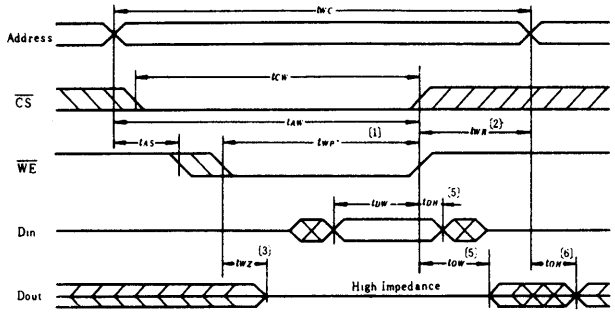
Notes) 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

• WRITE CYCLE

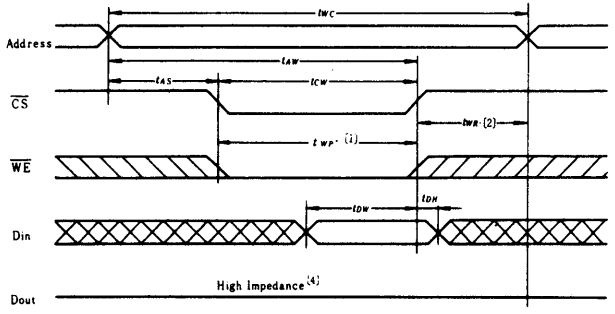
Item	Symbol	HM6168H/P-45		HM6168H/P-55		HM6168H/P-70		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	45	–	55	–	70	–	ns
Chip Selection to End of Write	t_{CW}	40	–	50	–	60	–	ns
Address Valid to End of Write	t_{AW}	40	–	50	–	60	–	ns
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	35	–	45	–	55	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns
Data Valid to End of Write	t_{DW}	20	–	25	–	30	–	ns
Data Hold Time	t_{DH}	0	–	0	–	0	–	ns
Write Enabled to Output in High Z*	t_{WZ}	0	15	0	20	0	25	ns
Output Active from End of Write*	t_{OW}	0	–	0	–	0	–	ns

* Thansition is measured ±500mV from high impedance voltage with Load (B).
This parameter is sampled and not 100% tested.

• TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)



• TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ Controlled)



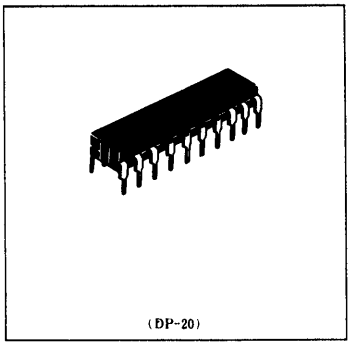
Notes) 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$, (t_{WP})
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffer buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of Write data of this write cycle.

HM6168HLP-45, HM6168HLP-55, HM6168HLP-70

4096-word×4-bit High Speed Static CMOS RAM

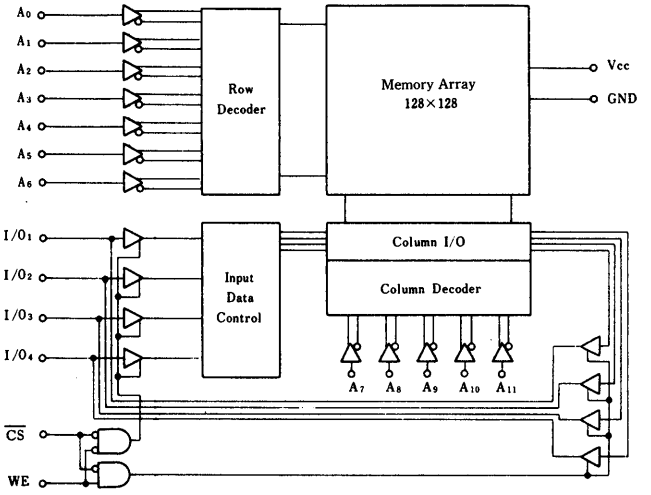
■FEATURES

- High Speed: Fast Access Time 45/55/70ns (max.)
- Single +5V Supply and High Density 20 Pin Package
- Low Power Standby and Low Power Operation;
  5μW typ. (Standby), 200mW typ. (Operation)
- Completely Static Memory
  No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible—All Inputs and Outputs
- Capable of Battery back up Operation

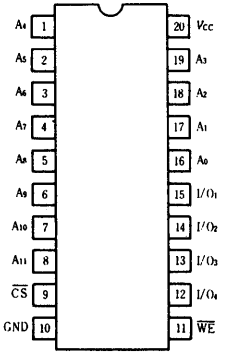


(DP-20)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_{IN}	−3.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

* Pulse Width 20ns, DC = −0.5V

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	X	Not selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle 1, 2
L	L	Write	I_{CC}	Din	Write Cycle 1, 2

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to + 70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*	–	0.8	V

* −3.0V (Pulse width 20ns)

■ DC AND OPERATING CHARACTERISTICS (V_{CC}=5V ±10%, GND=0V, Ta=0 to + 70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Imput Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, $V_{I/O}$=GND to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	–	40	90	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	–	15	25	mA
Standby Power Supply Current(1)	I_{SB1}	$\overline{CS}$=V_{CC}-0.2V, V_{IN}≦0.2V or V_{IN}≧V_{CC}-0.2V	–	1	50	μA
Output Low Voltage	V_{OL}	I_{OL}=8mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4.0mA	2.4	–	–	V

Note: Typical limits are at V_{CC}=5.0V, Ta=25°C and specified loading.

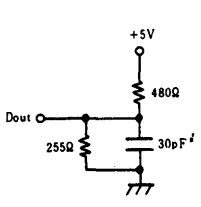
■ CAPACITANCE (Ta=25°C f=1MHz)

Item	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{in}	V_{IN}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	8	pF

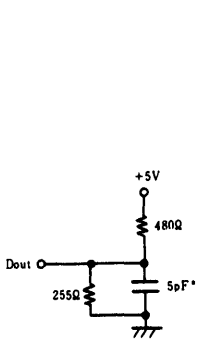
■ AC CHARACTERISTICS (V_{CC}=5V ±10%, Ta=0 to + 70°C, unless otherwise noted)

● AC TEST CONDITIONS

Input pulse levels: GND to 3.0V
Input rise and fall times: 5 ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure



Output Load (A) * Including scope and jig.



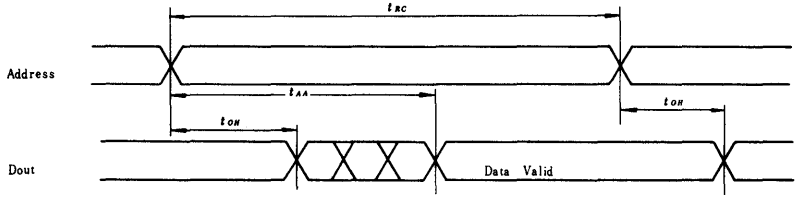
Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW})

• READ CYCLE

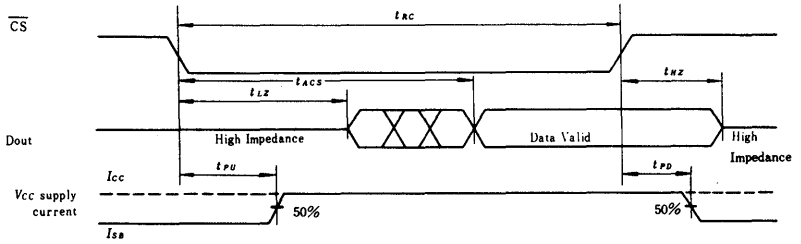
Item	Symbol	HM6168HLP-45		HM6168HLP-55		HM6168HLP-70		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	45	–	55	–	70	–	ns
Address Access Time	t_{AA}	–	45	–	55	–	70	ns
Chip Select Access Time	t_{ACS}	–	45	–	55	–	70	ns
Output Hold from Address Change	t_{OH}	5	–	5	–	5	–	ns
Chip Selection to Output in Low Z*	t_{LZ}	20	–	20	–	20	–	ns
Chip Deselection to Output in High Z*	t_{HZ}	0	20	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	0	–	ns
Chip Deselection to Power Down Time	t_{PD}	–	30	–	30	–	30	ns

* Transition is measured ±500mV for high impedance voltage with Load (B).
This parameter is sampled and not 100% tested.

• TIMING WAVEFORM OF READ CYCLE NO. 2(1), (2)



• TIMING WAVEFORM OF READ CYCLE NO. 2(1), (3)



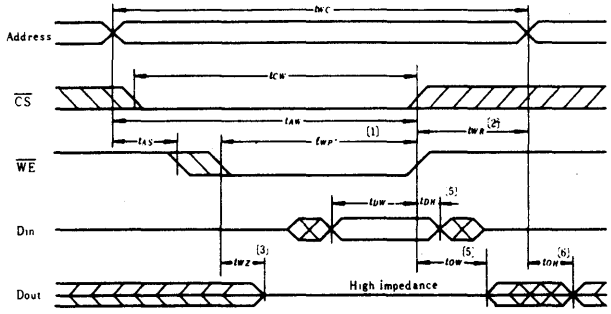
Notes) 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

• WRITE CYCLE

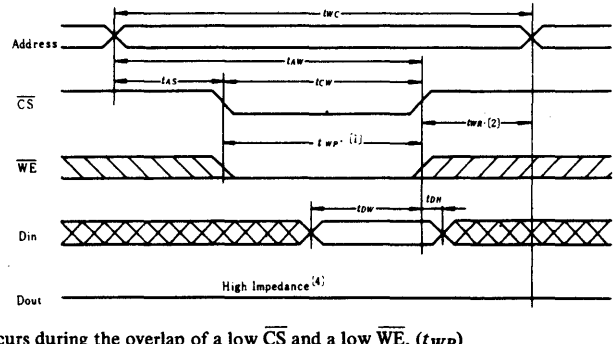
Item	Symbol	HM6168HLP-45		HM6168HLP-55		HM6168HLP-70		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	45	–	55	–	70	–	ns
Chip Selection to End of Write	t_{CW}	40	–	50	–	60	–	ns
Address Valid to End of Write	t_{AW}	40	–	50	–	60	–	ns
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	35	–	45	–	55	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns
Data Valid to End of Write	t_{DW}	20	–	25	–	30	–	ns
Data Hold Time	t_{DH}	0	–	0	–	0	–	ns
Write Enabled to Output in High Z*	t_{WZ}	0	15	0	20	0	25	ns
Output Active from End of Write*	t_{OW}	0	–	0	–	0	–	ns

* Thansition is measured ±500mV from high impedance voltage with Load (B).
This parameter is sampled and not 100% tested.

• TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)



• TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ Controlled)



Notes) 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$, (t_{WP})
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffer buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of Write data of this write cycle.

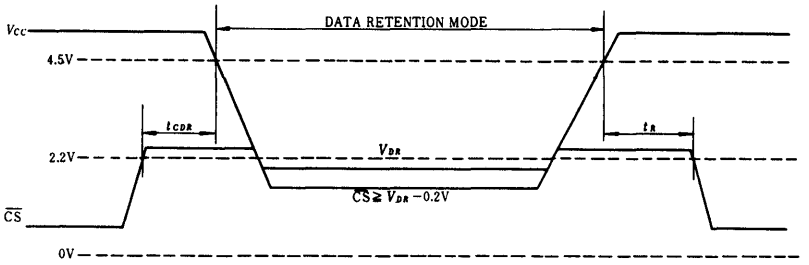
■LOW V_{CC} DATA RETENTION CHARACTERISTICS ($0℃ \leqq Ta \leqq 70℃$)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC}-0.2V$ $V_{in} \geqq V_{CC}-0.2V$ or $0V \leqq V_{in} \leqq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}		—	—	30* 20**	μA
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		t_{RC} (1)	—	—	ns

Note: 1. t_{RC} = Read Cycle Time.

* V_{CC} = 3.0V
** V_{CC} = 2.0V

●LOW V_{CC} DATA RETENTION WAVEFORM



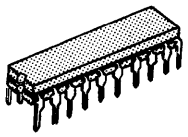
HM6167,HM6167-6,HM6167-8,
HM6167P,HM6167P-6,HM6167P-8

16384-word×1-bit High Speed Static CMOS RAM

■FEATURES

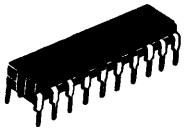
- Single +5V Supply and High Density 20 Pin Package
- Fast Access Time — 70ns/85ns/100ns
- Low Power Stand-by and Low Power Operation
  Stand-by 25mW Typ. and Operating 150mW Typ.
- Completely Static Memory . . . . . No Clock nor Refresh Required
- Fully TTL Compatible — All Inputs and Output
- Separate Data Input and Output . . . . . Three State Output
- Pin-Out Compatible with Intel 2167 Series

HM6167, HM6167-6, HM6167-8



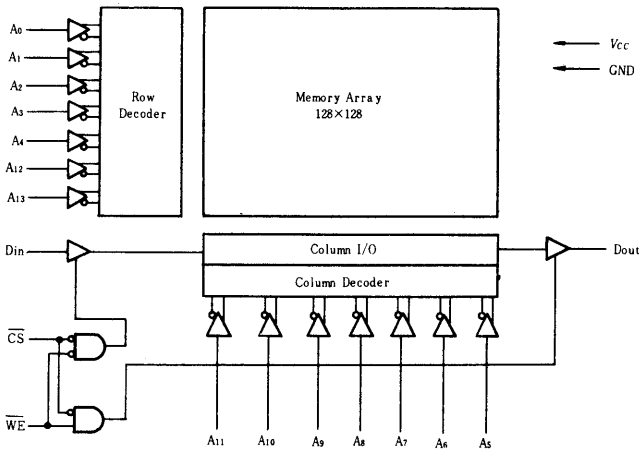
(DG-20)

HM6167P, HM6167P-6, HM6167P-8

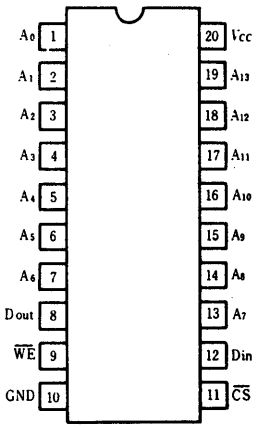


(DP-20)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to GND	V_T	−0.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	°C
Storage Temperature**	$T_{stg(bias)}$	−10 to +85	°C

* Pulse width 20ns : −3.5V **under bias

■RECOMMENDED DC OPERATING CONDITIONS

(0°C ≦ Ta ≦ 70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	−3.0*	—	0.8	V

* Pulse width 20ns, DC : V_{IL} min = −0.3V

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin	Reference Cycle
H	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle 1, 2
L	L	Write	I_{CC}	High Z	Write Cycle 1, 2

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, Ta=0℃ to +70℃)

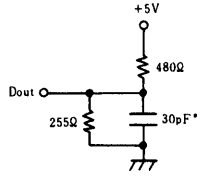
Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{IN}=0V~V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, V_{OUT}=0V~V_{CC}	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, Output Open	—	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	—	5	20	mA
	I_{SB1}	$\overline{CS}$=V_{CC}−0.2V V_{IN}≦0.2V or V_{IN}≧V_{CC}−0.2V	—	0.02	2	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4mA	2.4	—	—	V

Note) Typical limits are at V_{CC}=5.0V, Ta=25℃ and specified loading.

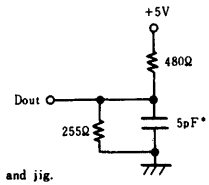
■AC TEST CONDITIONS

Input pulse levels: GND to 3.0V
Input rise and fall times: 5 ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure

Output Load A



Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



* Including scope and jig.

■CAPACITANCE (Ta=25℃, f=1.0MHz)

Item	Symbol	max	Unit	Conditions
Input Capacitance	C_{IN}	5	pF	V_{IN}=0V
Output Capacitance	C_{OUT}	6	pF	V_{OUT}=0V

Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0℃ to 70℃, unless otherwise noted.)

●READ CYCLE

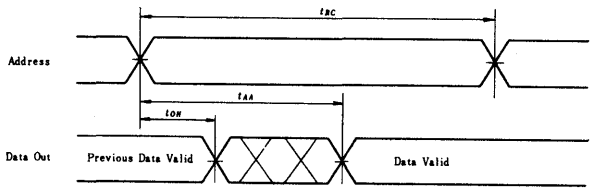
Item	Symbol	HM6167, HM6167P		HM6167-6, HM6167P-6		HM6167-8, HM6167P-8		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	70	—	85	—	100	—	ns
Address Access Time	t_{AA}	—	70	—	85	—	100	ns
Chip Select Access Time	t_{ACS}	—	70	—	85	—	100	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	5	—	ns
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	40	0	40	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	35	—	40	—	45	ns

● WRITE CYCLE

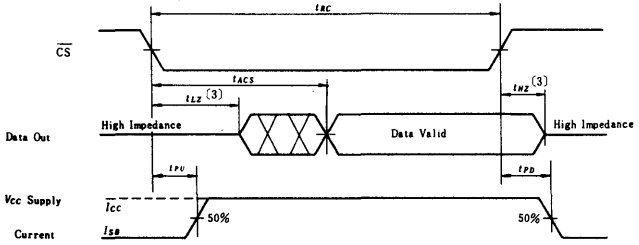
Item	Symbol	HM6167, HM6167P		HM6167-6, HM6167P-6		HM6167-8, HM6167P-8		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	70	—	85	—	100	—	ns	2
Chip Selection to End of Write	t_{CW}	55	—	65	—	80	—	ns	
Address Valid to End of Write	t_{AW}	55	—	65	—	80	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	
Write Pulse Width	t_{WP}	40	—	45	—	55	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	
Data Valid to End of Write	t_{DW}	30	—	35	—	40	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	
Write Enable to Output in High Z	t_{WZ}	0	30	0	40	0	40	ns	3, 4
Output Active from End of Write	t_{OW}	0	—	0	—	0	—	ns	3, 4

Notes) 1. If $\overline{CS}$ goes high simultaneouly with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF READ CYCLE NO. 1 [1), 2)]

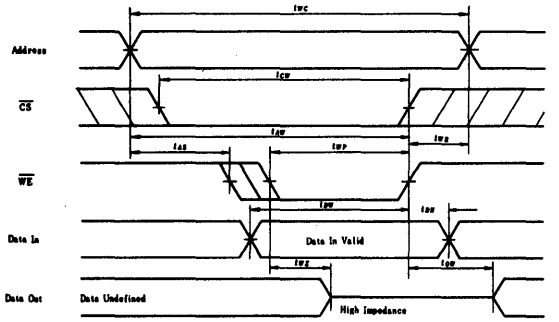


● TIMING WAVEFORM OF READ CYCLE NO. 2 [1), 3)]



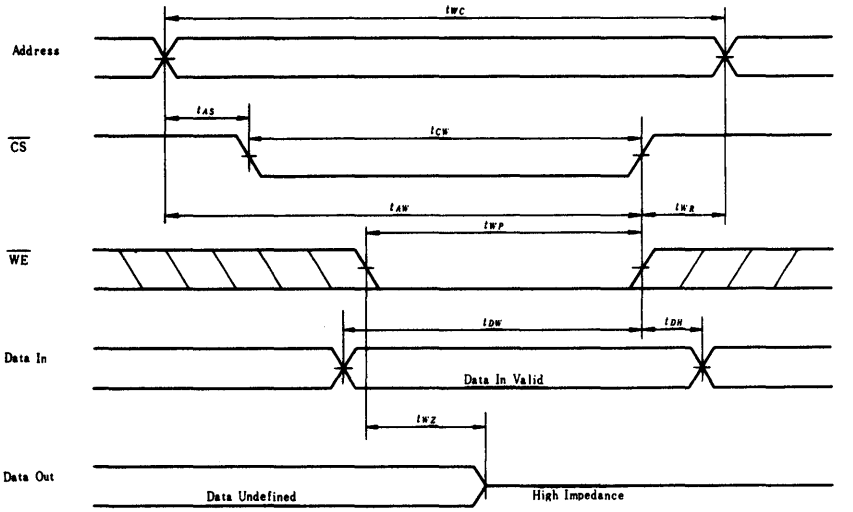
NOTES: 1. $\overline{WE}$ is high and $\overline{CS}$ is low for READ cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.

● TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)



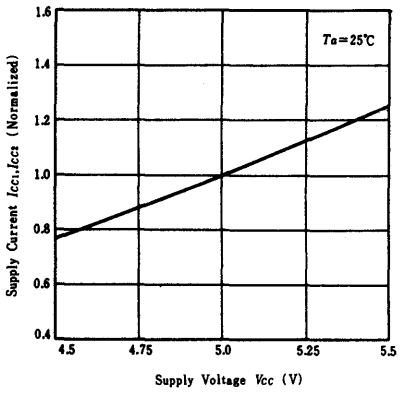
NOTE: 1. Transition is measured ±500mV from steady state voltage with specified loading in Load B.

● TIMING WAVEFORM OF WRITE CYCLE No. 2 ($\overline{CS}$ Controlled)

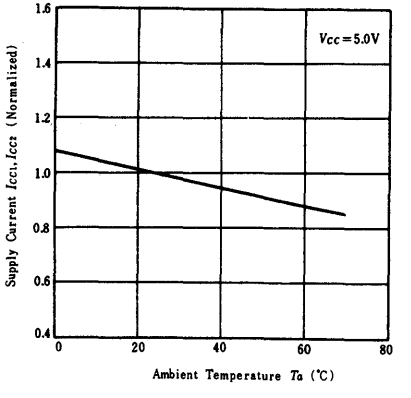


Note) Transition is measured ±500mV from steady state voltage with specified loading in Load B.

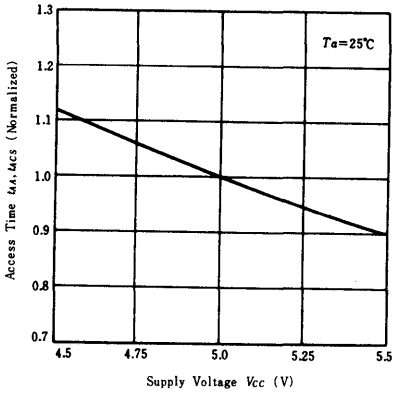
SUPPLY CURRENT vs. SUPPLY VOLTAGE



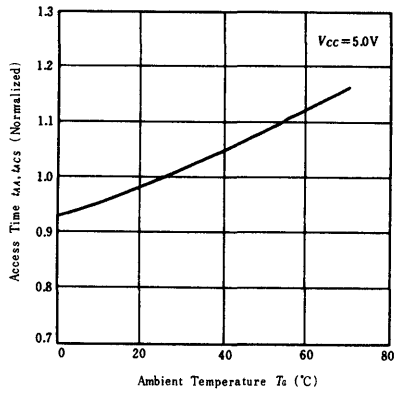
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



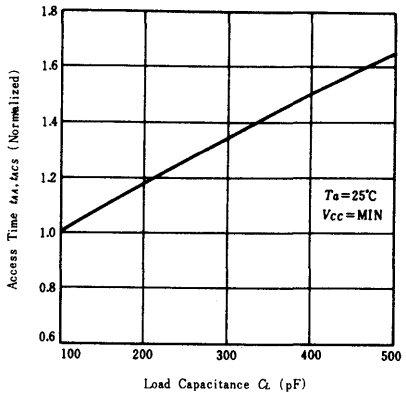
ACCESS TIME vs. SUPPLY VOLTAGE



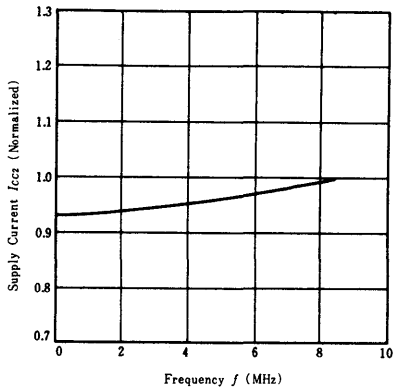
ACCESS TIME vs. AMBIENT TEMPERATURE



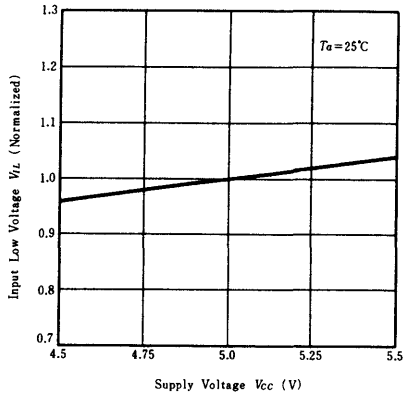
ACCESS TIME vs. LOAD CAPACITANCE



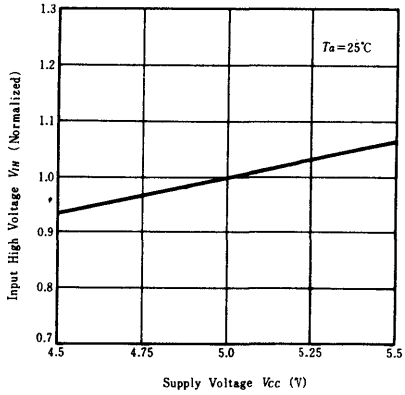
SUPPLY CURRENT vs. FREQUENCY



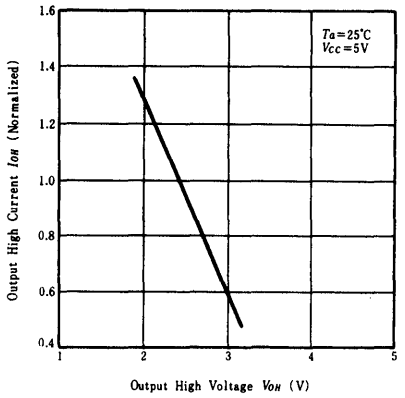
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



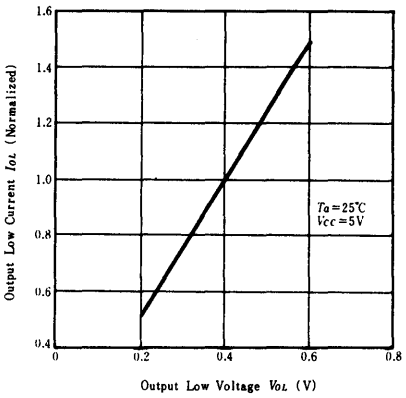
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



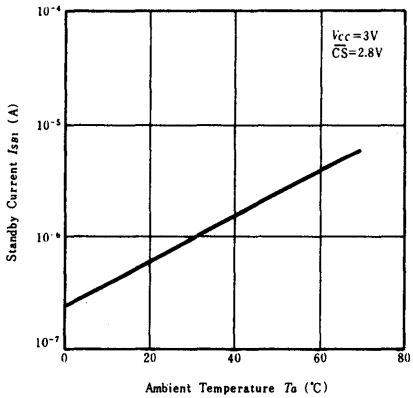
OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



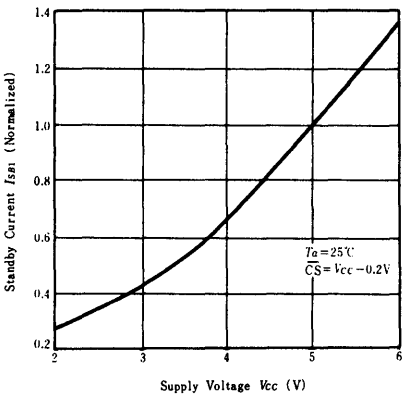
OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE



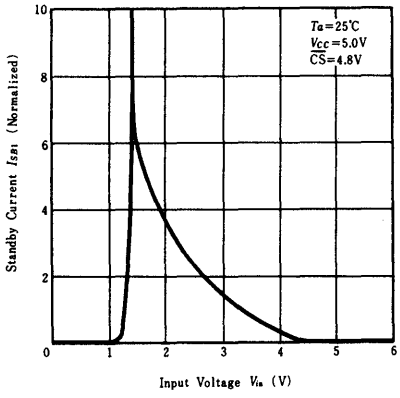
STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE



STANDBY CURRENT vs. INPUT VOLTAGE

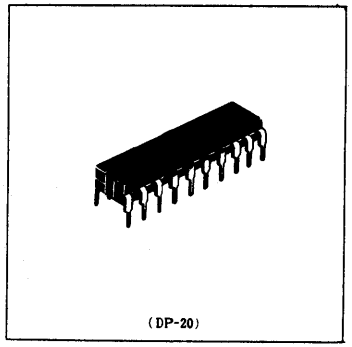


HM6167LP, HM6167LP-6, HM6167LP-8

16384-word×1-bit High Speed Static CMOS RAM

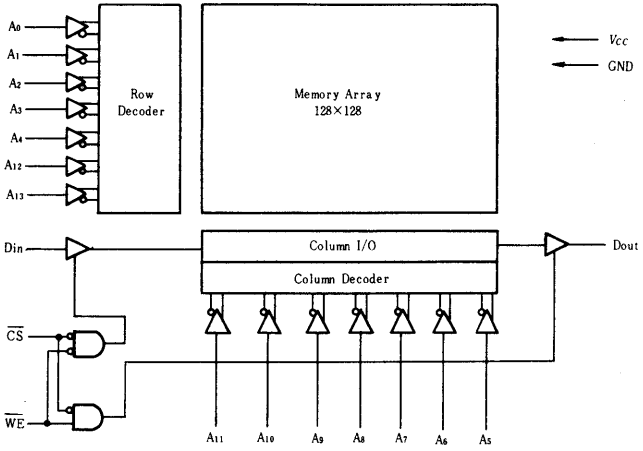
■FEATURES

- Single +5V Supply and High Density 20 Pin Package
- Fast Access Time 70ns/85ns/100ns
- Low Power Stand-by and Low Power Operation
  Stand-by 5μW (typ) and Operating 150mW (typ.)
- Completely Static Memory. . . . . .No Clock or Refresh Required
- Fully TTL Compatible. . . . . .All Inputs and Output
- Separate Data Input and Output . . . . . .Three State Output
- Capable of Battery Back up Operation

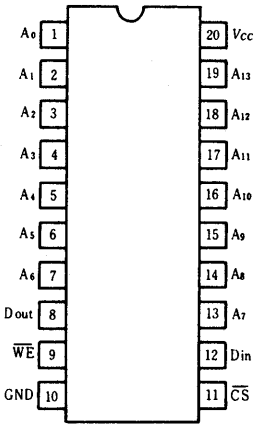


(DP-20)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to GND	V_T	−0.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature**	$T_{stg(bias)}$	−10 to +85	°C

* Pulse width 20ns −3.5V ** under bias

■RECOMMENDED DC OPERATING CONDITIONS (0 °C ≦ Ta ≦ 70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	−3.0*	—	0.8	V

* Pulse width 20ns, DC; V_{IL} min = −0.3V

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin	Reference Cycle
H	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle 1, 2
L	L	Write	I_{CC}	High Z	Write Cycle 1, 2

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, Ta=0~+70°C)

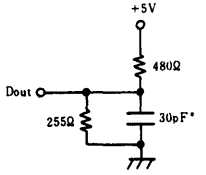
Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V V_{IN}=0V~V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, V_{out}=0V~V_{CC}	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, Output Open	—	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	—	5	20	mA
	I_{SB1}	$\overline{CS}$=V_{CC}−0.2V V_{IN}≦0.2V or V_{IN}≧V_{CC}−0.2V	—	1	50	μA
Output Low Voltage	V_{OL}	I_{OL}=8mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4mA	2.4	—	—	V

Note) Typical limits are at V_{CC}=5.0V, Ta=25°C and specified loading.

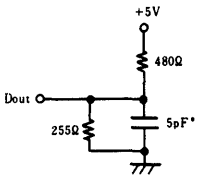
■AC TEST CONDITIONS

Input pulse levels: GND to 3.0V
Input rise and fall times: 5 ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure

Output Load A



Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



* Including scope and jig.

■CAPACITANCE (Ta=25°C, f=1.0MHz)

Item	Symbol	max	Unit	Conditions
Input Capacitance	C_{IN}	5	pF	V_{IN}=0V
Output Capacitance	C_{OUT}	6	pF	V_{OUT}=0V

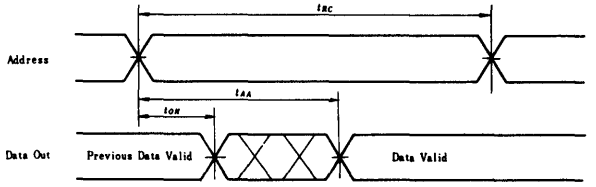
Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (Ta=0°C to +70°C, V_{CC}=5V±10%, unless otherwise noted.)

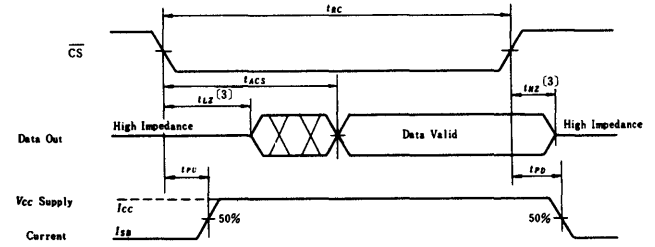
●READ CYCLE

Item	Symbol	HM6167LP		HM6167LP-6		HM6167LP-8		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	70	—	85	—	100	—	ns
Address Access Time	t_{AA}	—	70	—	85	—	100	ns
Chip Select Access Time	t_{ACS}	—	70	—	85	—	100	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	5	—	ns
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	40	0	40	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	35	—	40	—	45	ns

● TIMING WAVEFORM OF READ CYCLE NO.1 [1), 2)]



● TIMING WAVEFORM OF READ CYCLE NO.2 [1), 3)]



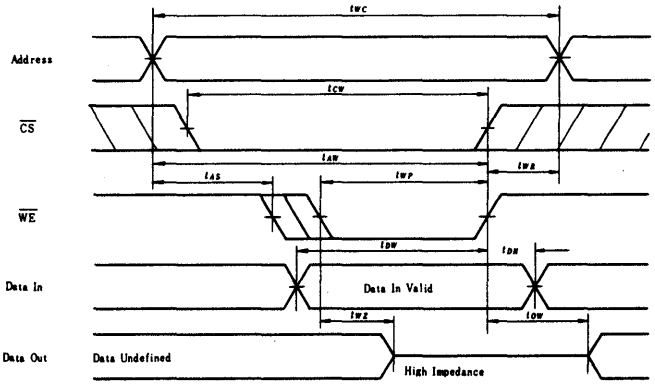
NOTES: 1. $\overline{WE}$ is high and $\overline{CS}$ is low for READ Cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading B.

● WRITE CYCLE

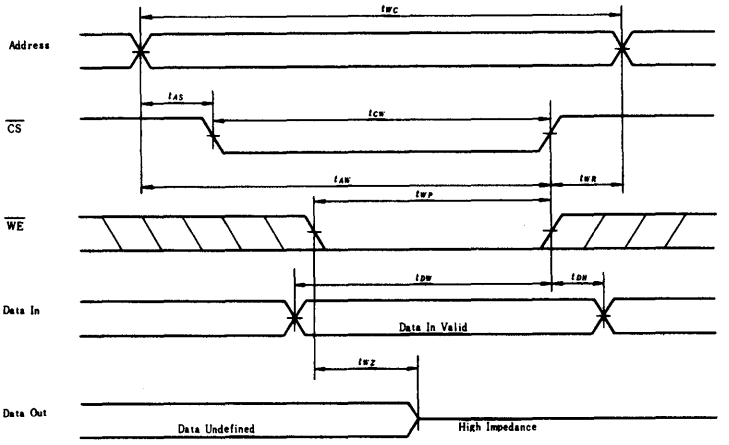
Item	Symbol	HM6167LP		HM6167LP-6		HM6167LP-8		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	70	—	85	—	100	—	ns	2
Chip Selection to End of Write	t_{CW}	55	—	65	—	80	—	ns	
Address Valid to End of Write	t_{AW}	55	—	65	—	80	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	
Write Pulse Width	t_{WP}	40	—	45	—	55	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	
Data Valid to End of Write	t_{DW}	30	—	35	—	40	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	
Write Enable to Output in High Z	t_{WZ}	0	30	0	40	0	40	ns	3, 4
Output Active from End of Write	t_{OW}	0	—	0	—	0	—	ns	3, 4

Notes) 1. If $\overline{CS}$ goes high simultaneouly with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ Controlled)



● TIMING WAVEFORM OF WRITE CYCLE No. 2 ($\overline{CS}$ Controlled)



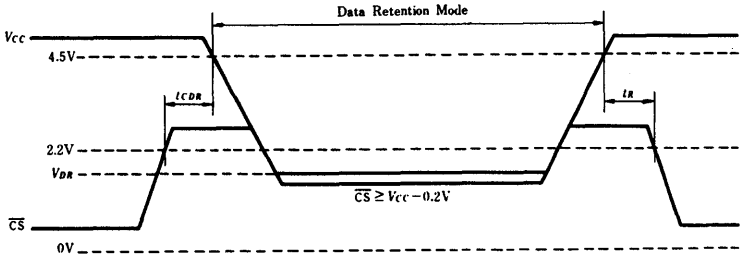
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (Ta=0°C to 70°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}-0.2V$ $V_{in} \geq V_{CC}-0.2V$ or $0V \leq V_{in} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}		—	—	20*	μA
			—	—	30**	
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		t_{RC}△	—	—	ns

△ t_{RC}=Read Cycle Time

* V_{CC}=2.0V
** V_{CC}=3.0V

■ LOW V_{CC} DATA RETENTION WAVEFORM



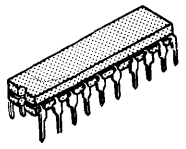
HM6167H-45, HM6167H-55, HM6167HP-45, HM6167HP-55

16384-word x 1-bit High Speed Static CMOS RAM

■ FEATURES

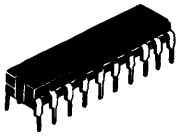
- Fast Access Time. . . . . .HM6167H/P-45 45ns (max)
  HM6167H/P-55 55ns (max)
- Low Power Standby and Low Power Operation
  Standby 100μW (typ), Operating 200mW (typ)
- Single +5V Supply and High Density 20 Pin Package
- Completely Static Memory . . . .No Clock nor Refresh Required
- Fully TTL Compatible . . . . . .All Inputs and Output
- Separate Data Input and Output. . . . . .Three State Output

HM6167H-45, HM6167H-55



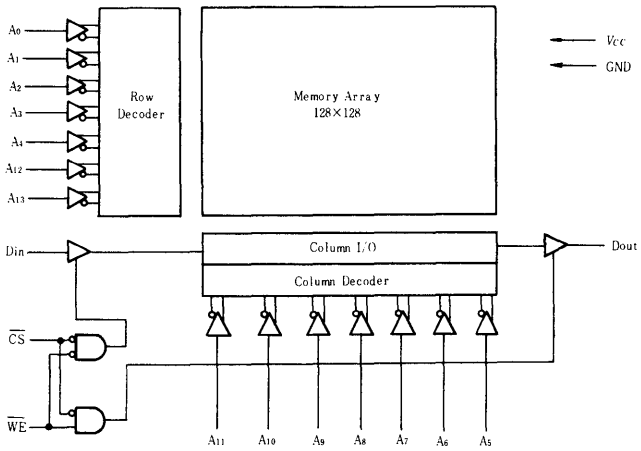
(DG-20)

HM6167HP-45, HM6167HP-55

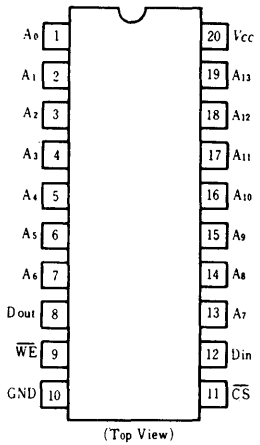


(DP-20)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with respect to GND	V_T	−3.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	°C
Storage Temperature (under bias)	T_{bias}	−10 to +85	°C

* Pulse Width 20ns, DC: −0.5V

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−3.0*	–	0.8	V

* Pulse Width: 20ns, DC: V_{IL} (min) = −0.5V

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, Ta=0℃ to +70℃)

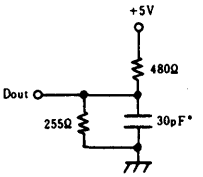
Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{IN}=0V~V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, V_{OUT}=0V~V_{CC}	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, Output Open	—	40	80	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	—	10	20	mA
	I_{SB1}	$\overline{CS}$≧V_{CC}−0.2V V_{IN}≦0.2V or V_{IN}≧V_{CC}−0.2V	—	0.02	2	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4mA	2.4	—	—	V

Note) Typical limits are at V_{CC}=5.0V, Ta=25℃ and specified loading.

■AC TEST CONDITIONS

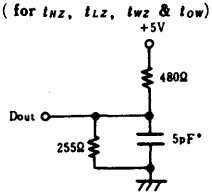
Input pulse levels: GND to 3.0V
Input rise and fall times: 5 ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure

Output Load A



* Including scope and jig.

Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



* Including scope and jig.

■CAPACITANCE (Ta=25℃, f=1.0MHz)

Item	Symbol	typ	max	Unit	Conditions
Input Capacitance	C_{IN}	3	5	pF	V_{IN}=0V
Output Capacitance	C_{OUT}	5	7	pF	V_{OUT}=0V

Note) This parameter is sampled and not 100% tested.

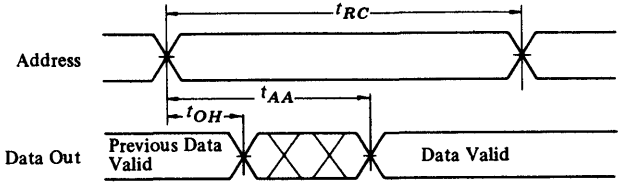
■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0°C to 70°C, unless otherwise noted.)

●READ CYCLE

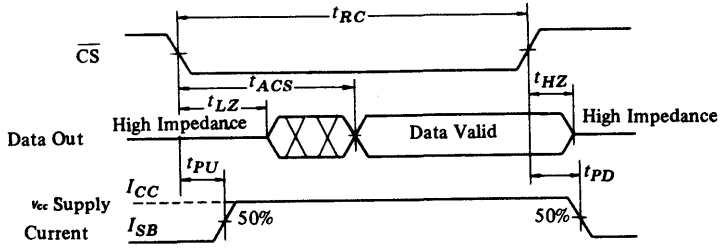
Item	Symbol	HM6167H/P-45		HM6167HP-55		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	45	–	55	–	ns	(1)
Address Access Time	t_{AA}	–	45	–	55	ns	
Chip Select Access Time	t_{ACS}	–	45	–	55	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	ns	(2) (3) (7)
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	ns	(2) (3) (7)
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns	
Chip Deselection to Power Down Time	t_{PD}	–	30	–	30	ns	

NOTES: 1. All Read Cycle timing are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is High for READ cycle.
5. Device is continuously selected, $\overline{CS}$ = V_{IL}.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

●TIMING WAVEFORM OF READ CYCLE NO.1 [4), 5)]



●TIMING WAVEFORM OF READ CYCLE NO.2 [4), 6)]

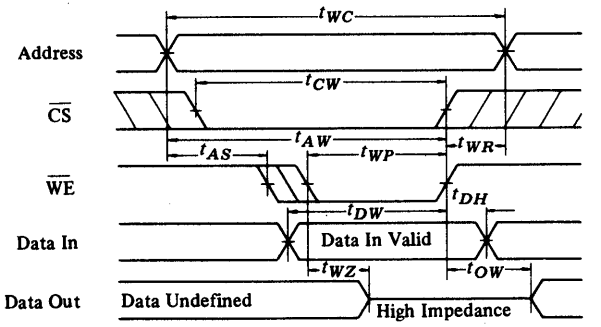


• WRITE CYCLE

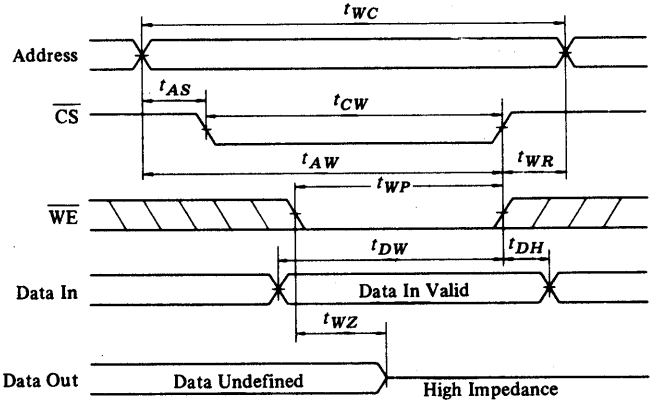
Item	Symbol	HM6167H/P-45		HM6167H/P-55		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	45	–	55	–	ns	(2)
Chip Selection to End of Write	t_{CW}	40	–	50	–	ns	
Address Valid to End of Write	t_{AW}	40	–	50	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Write Pulse Width	t_{WP}	25	–	35	–	ns	
Write Recovery Time	t_{WR}	0	–	0	–	ns	
Data Valid to End of Write	t_{DW}	25	–	25	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	25	0	25	ns	(3) (4)
Output Active from End of Write	t_{OW}	0	–	0	–	ns	(3) (4)

NOTES: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
2. All write cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

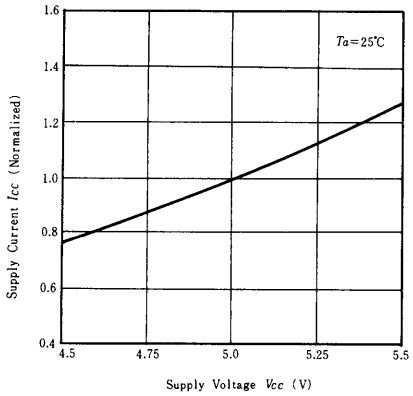
• TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



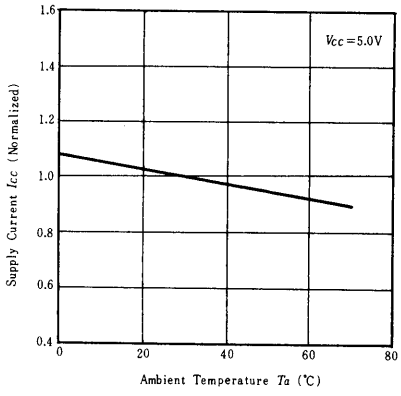
• TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



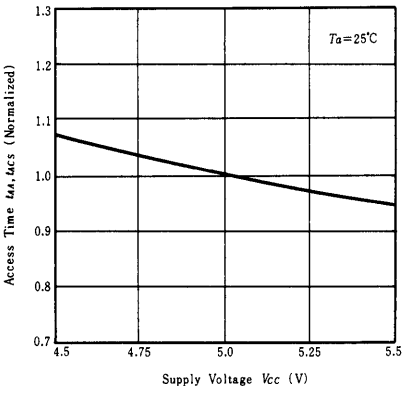
SUPPLY CURRENT vs. SUPPLY VOLTAGE



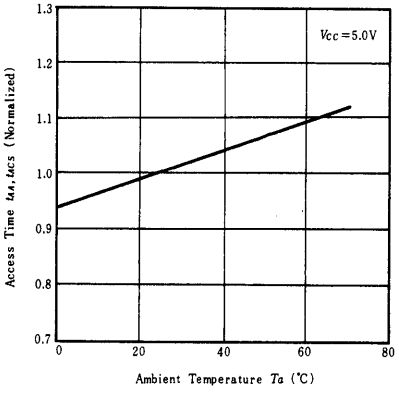
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



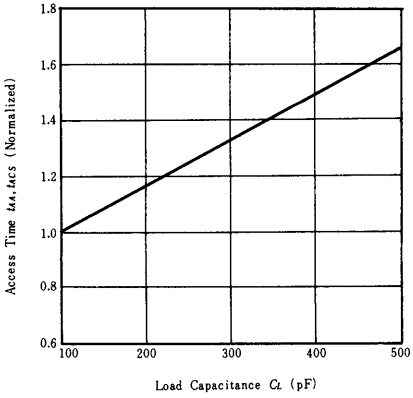
ACCESS TIME vs. SUPPLY VOLTAGE



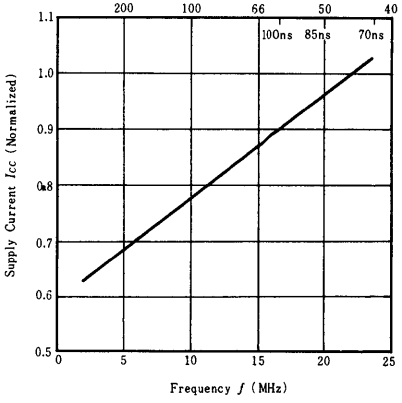
ACCESS TIME vs. AMBIENT TEMPERATURE



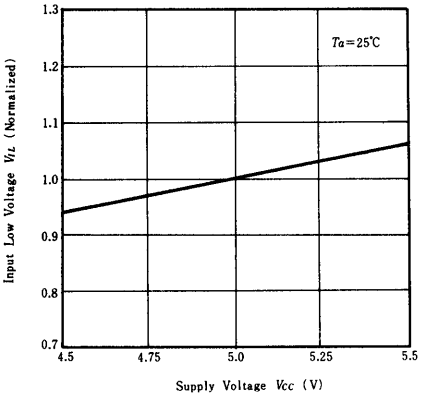
ACCESS TIME vs. LOAD CAPACITANCE



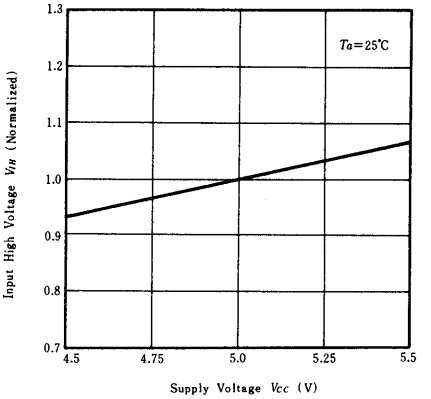
SUPPLY CURRENT vs. FREQUENCY



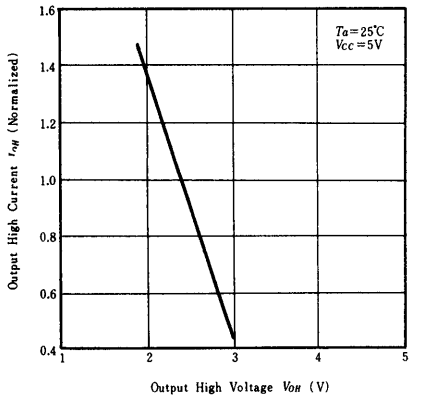
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



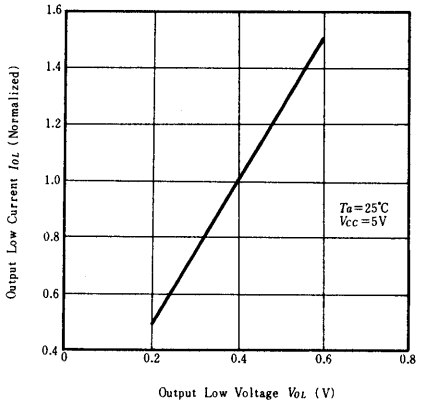
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



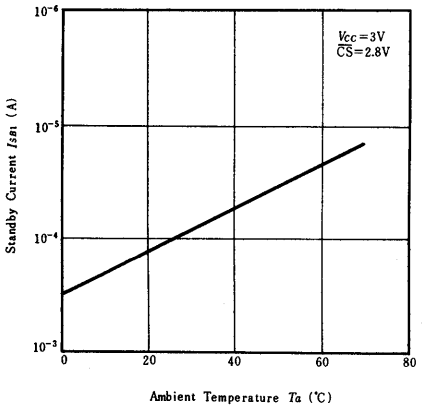
OUTPUT CURRENT vs. OUTPUT VOLTAGE



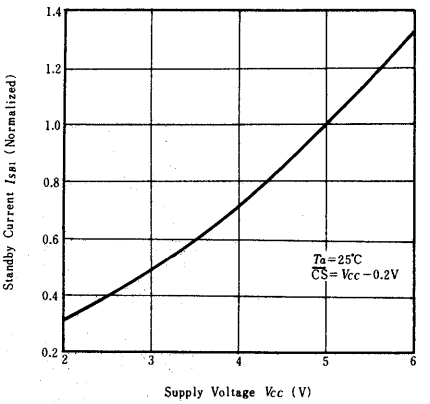
OUTPUT CURRENT vs. OUTPUT VOLTAGE



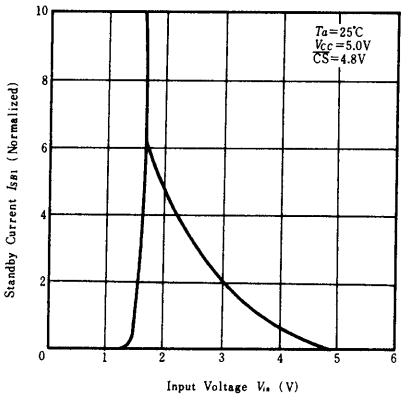
STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE



STANDBY CURRENT vs. INPUT VOLTAGE

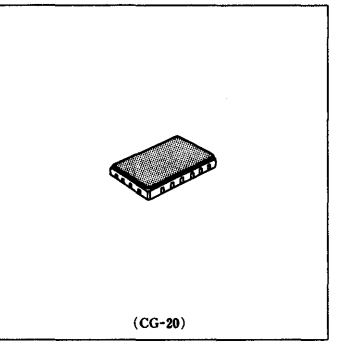


HM6167HCG-45,HM6167HCG-55

16384-word×1-bit High Speed Static CMOS RAM

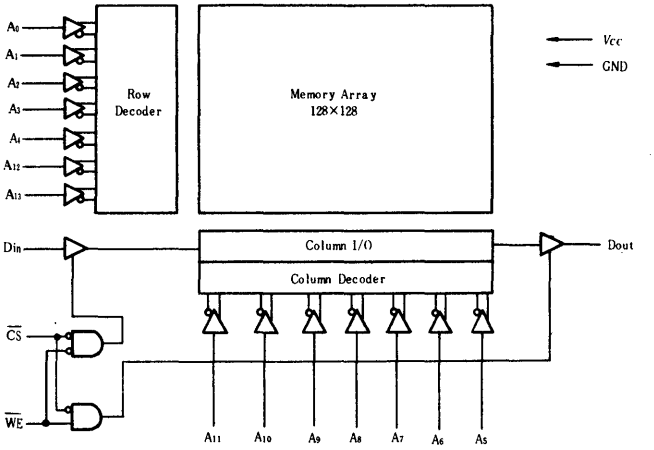
■FEATURES

- High Density 20 pin Leadless Chip Carrier
- High Speed: Fast Access Time 45/55ns Max.
- Low Power Standby and Low Power Operation
  Standby: 100μW typ., Operation: 200mW typ.
- Completely Static Memory;
  No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible; All Inputs and Output

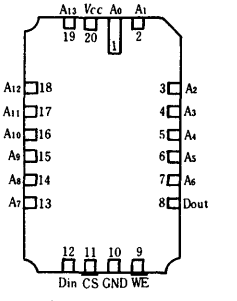


(CG-20)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Bottom View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin*	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

* with respect to GND. V_{IN} min = −3.5V (Pulse width 20ns)

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	−0.5*	—	0.8	V

* −3.0V (Pulse width 20ns)

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V ±10%, Ta=0 to +70°C)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC}=5.5V, V_{IN}=0V to V_{CC}	—	—	2	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}=V_{IH}$, V_{OUT}=0V to V_{CC}	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, Output Open	—	40	80	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	10	20	mA
	I_{SB1}	$\overline{CS} \geq V_{CC}-0.2V$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}-0.2V$	—	20	2000	μA
Output Voltage	V_{OL}	I_{OL}=8mA	—	—	0.4	V
	V_{OH}	I_{OH}=−4mA	2.4	—	—	V

Note) * : Typical limits are at V_{CC}=5.0V, Ta=25°C and specified loading.

■CAPACITANCE (Ta=25°C, f=1MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	3	5	pF
Output Capacitance	C_{out}	V_{out}=0V	5	7	pF

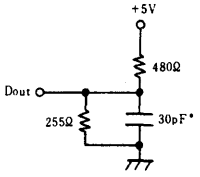
Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (V_{CC}=5V ±10%, Ta=0 to +70°C)

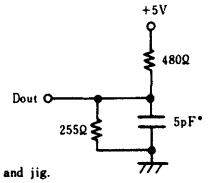
●AC TEST CONDITIONS

Input Pulse Levels: GND to 3.0V
Input Rise and Fall Times: 5 ns
Output Reference Levels: 1.5V

Output Load A



Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



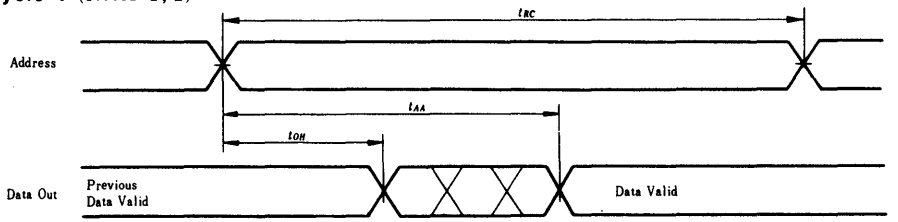
* Including scope and jig.

●READ CYCLE

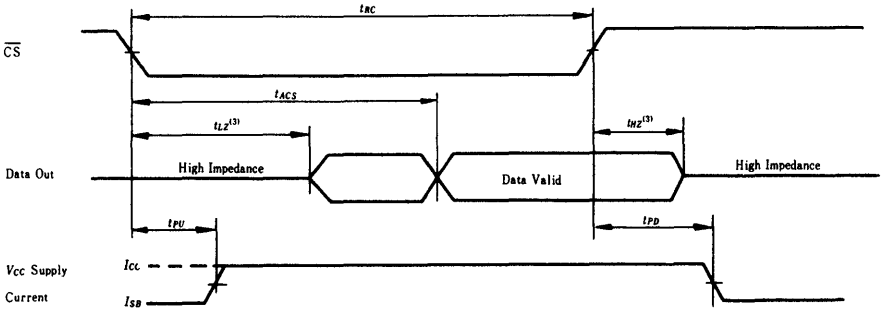
Item	Symbol	HM6167HCG-45		HM6167HCG-55		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	45	—	55	—	ns	1
Address Access Time	t_{AA}	—	45	—	55	ns	
Chip Select Access Time	t_{ACS}	—	45	—	55	ns	
Output Hold from Address Change	t_{OH}	5	—	5	—	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	ns	2, 3, 4
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	ns	2, 3, 4
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns	
Chip Deselection to Power Down Time	t_{PD}	—	30	—	30	ns	

Notes) 1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

●Read Cycle-1 (Notes 1, 2)



●Read Cycle-2 (Notes 1, 3)



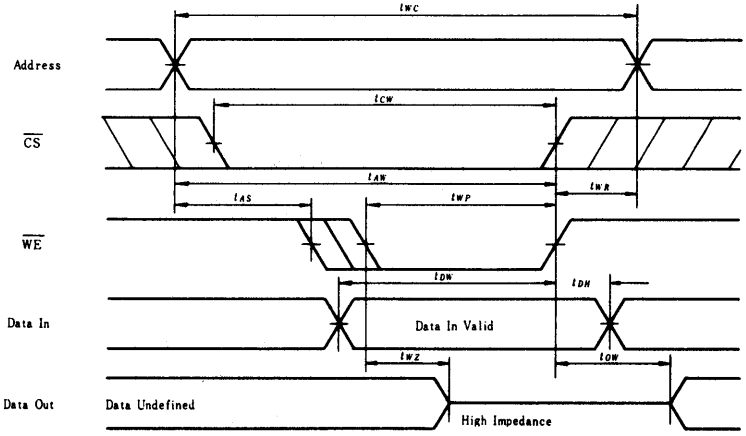
Notes) 1. $\overline{WE}$ is high for Read Cycle.
2. Address valid prior to or coincident with $\overline{CS}$ transjtion low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.

●WRITE CYCLE

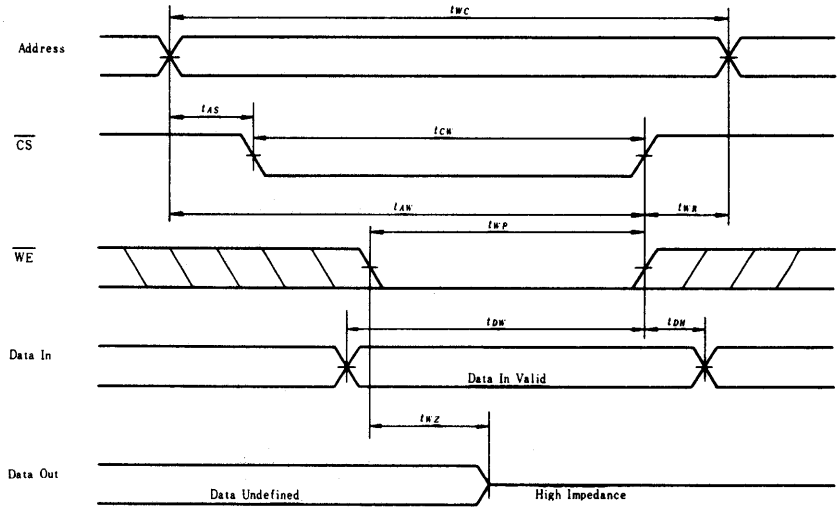
Item	Symbol	HM6167HCG-45		HM6167HCG-55		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	45	—	55	—	ns	2
Chip Selection to End of Write	t_{CW}	40	—	50	—	ns	
Address Valid to End of Write	t_{AW}	40	—	50	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	ns	
Write Pulse Width	t_{WP}	25	—	35	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	ns	
Data Valid to End of Write	t_{DW}	25	—	25	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	ns	
Write Enable to Output in High Z	t_{WZ}	0	25	0	25	ns	3, 4
Output Active from End of Write	t_{OW}	0	—	0	—	ns	3, 4

Notes) 1. If $\overline{CS}$ goes high simultaneouly with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

●Write Cycle-1 ($\overline{WE}$ Controlled)



●Write Cycle-2 ($\overline{CS}$ Controlled)

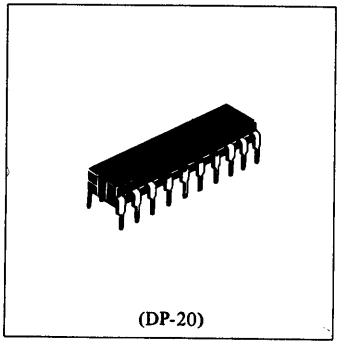


HM6167HLP-45, HM6167HLP-55

16384-word x 1-bit High Speed Static CMOS RAM

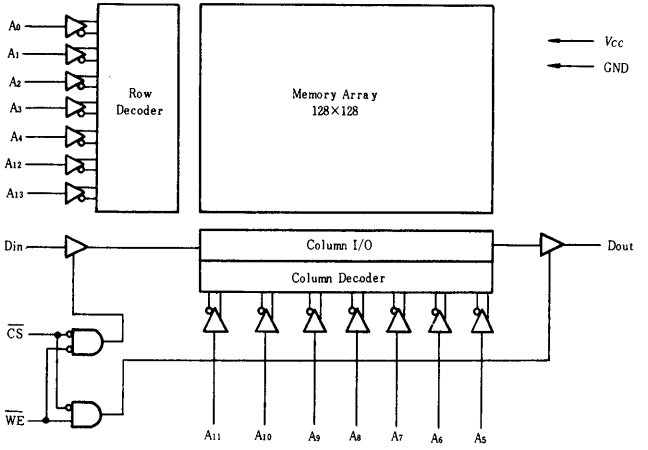
■ FEATURES

- Fast Access Time. . . . . .HM6167HLP-45 45ns (max)
  HM6167HLP-55 55ns (max)
- Low Power Standby and Low Power Operation
  Standby 5μW (typ) and Operating 200mW (typ)
- Capable of Battery Back-up Operation
- Single +5V Supply and High Density 20 Pin Package
- Completely static Memory
  No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible . . . . .All Inputs and Output

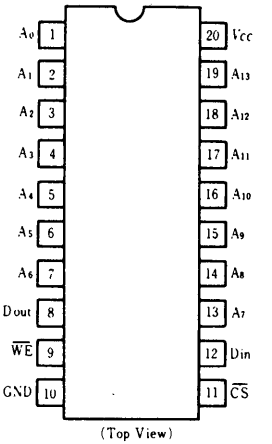


(DP-20)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with respect to GND	V_T	−3.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

* Pulse Width 20ns, DC: −0.5V

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−3.0*	–	0.8	V

* Pulse Width 20ns, DC: V_{IL} min = −0.5V

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

■ DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, Ta=0~+70°C)

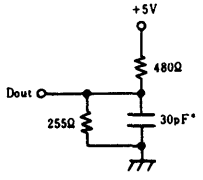
Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V V_{IN}=0V~V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, $V_{I/O}$=0V~V_{CC}	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, Output Open	—	40	80	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	—	10	20	mA
	I_{SB1}	$\overline{CS}$=V_{CC}−0.2V V_{IN}≦0.2V or V_{IN}≧V_{CC}−0.2V	—	1	50	μA
Output Low Voltage	V_{OL}	I_{OL}=8mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4mA	2.4	—	—	V

Note) Typical limits are at V_{CC}=5.0V, Ta=25°C and specified loading.

■ AC TEST CONDITIONS

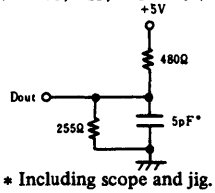
Input pulse levels: GND to 3.0V
Input rise and fall times: 5 ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure

Output Load A



* Including scope and jig.

Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



* Including scope and jig.

■ CAPACITANCE (Ta=25°C, f=1MHz)

Item	Symbol	typ.	max	Unit	Conditions
Input Capacitance	C_{IN}	3	5	pF	V_{IN}=0V
Output Capacitance	C_{OUT}	5	7	pF	V_{OUT}=0V

Note) This parameter is sampled and not 100% tested.

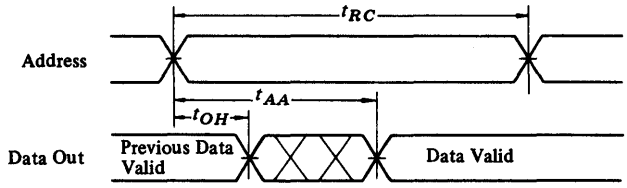
■ AC CHARACTERISTICS (Ta=0°C to +70°C, V_{CC}=5V±10%, unless otherwise noted.)

●READ CYCLE

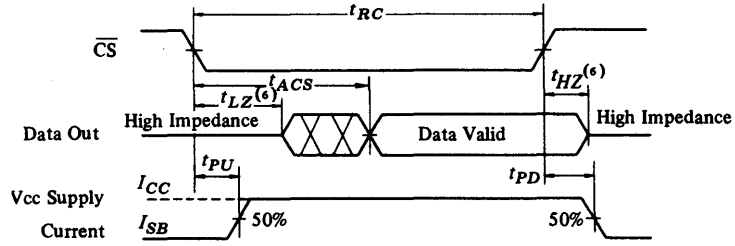
Item	Symbol	HM6167HLP-45		HM6167HLP-55		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	45	–	55	–	ns	(1)
Address Access Time	t_{AA}	–	45	–	55	ns	
Chip Select Access Time	t_{ACS}	–	45	–	55	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	ns	(2)(3)(7)
Chip Selection to Output in High Z	t_{HZ}	0	30	0	30	ns	(2)(3)(7)
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns	
Chip Deselection to Power Down Time	t_{PD}	–	30	–	30	ns	

NOTES:
1. All Read Cylce timing are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is High for READ cycle.
5. Device is continuously selected, $\overline{CS}$ = V_{IL}.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF READ CYCLE NO. 1 [4) 5)]



● TIMING WAVEFORM OF READ CYCLE NO. 2 [4) 6)]

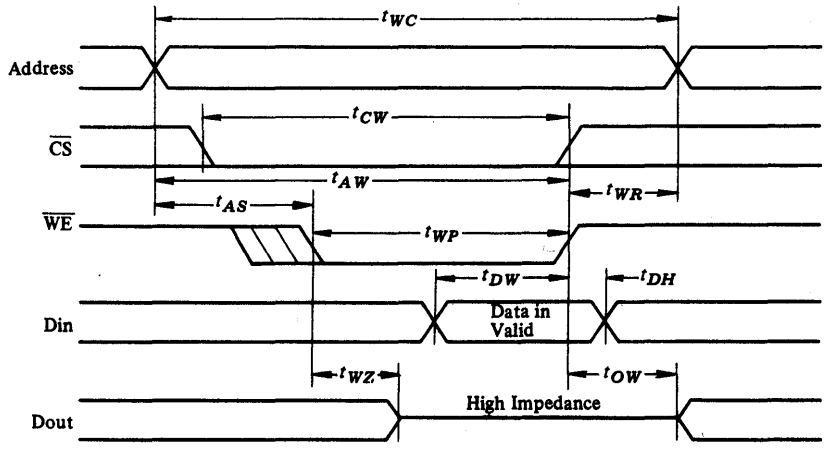


● WRITE CYCLE

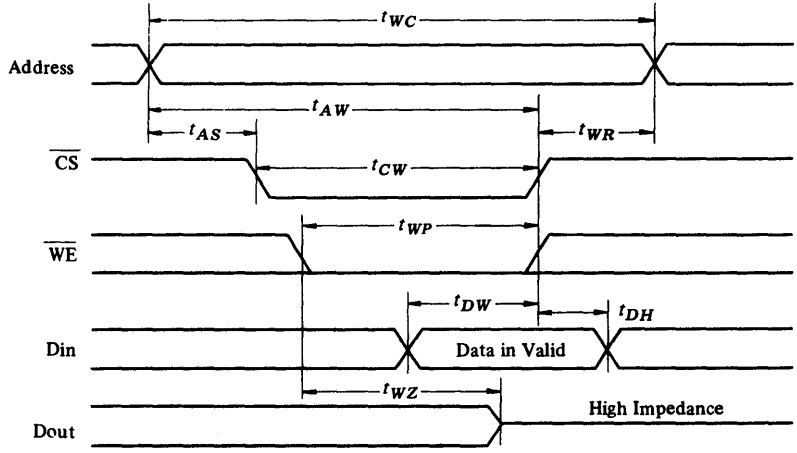
Item	Symbol	HM6167HLP-45		HM6167HLP-55		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	45	–	55	–	ns	(2)
Chip Selection to End of Write	t_{CW}	40	–	50	–	ns	
Address Valid to End of Write	t_{AW}	40	–	50	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Write Pulse Width	t_{WP}	25	–	35	–	ns	
Write Recovery Time	t_{WR}	0	–	0	–	ns	
Data Valid to End of Write	t_{DW}	25	–	25	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	25	0	25	ns	(3) (4)
Output Active from End of Write	t_{OW}	0	–	0	–	ns	(3) (4)

NOTES: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
2. All Write Cycle timings are referenced from the last valid address to the first transitions address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)



● TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ Controlled)



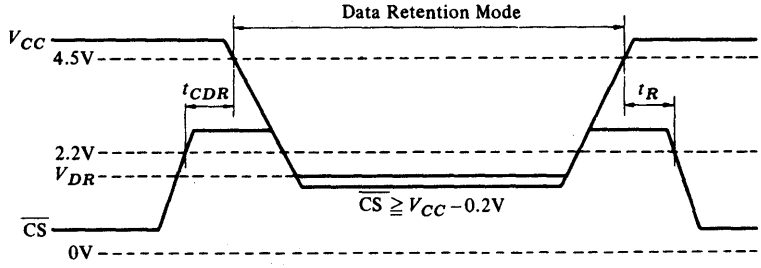
■LOW V_{CC} DATA RETENTION CHARACTERISTICS (Ta=0°C to 70°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}-0.2V$ $V_{in} \geq V_{CC}-0.2V$ or $0V \leq V_{in} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}		—	—	20*	μA
			—	—	30**	
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		t_{RC}△	—	—	ns

△ t_{RC} = Read Cycle Time

* V_{CC}=2.0V
** V_{CC}=3.0V

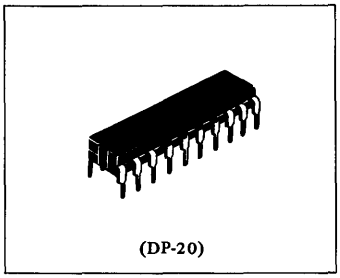
●LOW V_{CC} DATA RETENTION WAVEFORM



HM6267P-35,HM6267P-45

Preliminary

16384-word x 1-bit High Speed Static CMOS RAM

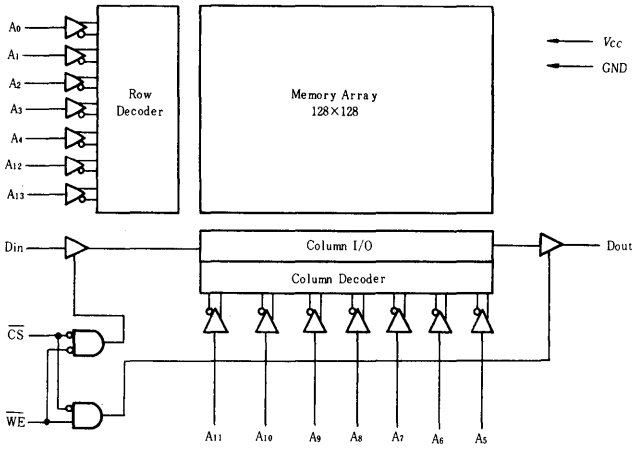


(DP-20)

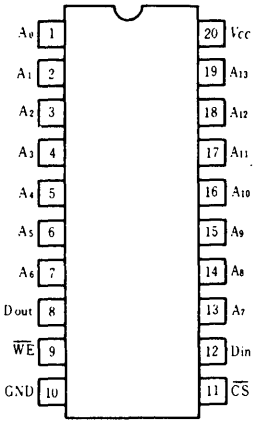
■ FEATURES

- High Speed: Fast Access Time 35/45ns (max.)
- Low Power Standby and Low Power Operation
  Standby: 0.1mW (typ.), Operation: 200mW (typ.)
- Single 5V Supply and High Density 20 Pin Package
- Completely Static Memory ..... No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Input and Output

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin*	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

* with respect to GND. V_T min = −3.5V (Pulse width 20ns)

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−3.0*	–	0.8	V

* Pulse Width 20ns, DC: V_{IL} min = −0.5V

Note: The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

■ DC AND OPERATING CHARACTERISTICS[1] (V_{CC} = 5V ±10%[2], GND = 0V, T_a = 0 to +70°C)

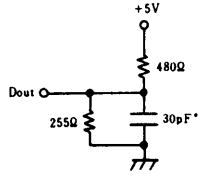
Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC} = 5.5V, V_{in} = GND to V_{CC}	–	–	10	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}$ = V_{IH}, V_{out} = GND to V_{CC}	–	–	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, Output Open	–	40	80[3]	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}	–	10	20	mA
	I_{SB1}	$\overline{CS} \geqq V_{CC}-0.2V$, $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC}-0.2V$	–	0.02	2	mA
Output Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	V
	V_{OH}	I_{OH} = –4mA	2.4	–	–	V

Notes) 1. Typical limits are at V_{CC} = 5V, T_a = 25°C and specified loading.
2. V_{CC} = 5V±5% for 35ns version.
3. 100mA max. for 35ns version.

■ AC TEST CONDITIONS

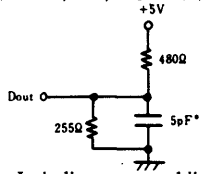
Input pulse levels: GND to 3.0V
Input rise and fall times: 5ns
Input and Output timing reference levels: 1.5V
Output load: See Figure

Output Load A



* Including scope and jig.

Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



* Including scope and jig.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	typ.	max	Unit	Conditions
Input Capacitance	C_{IN}	3	5	pF	V_{IN}=0V
Output Capacitance	C_{OUT}	5	7	pF	V_{OUT}=0V

Note) This parameter is sampled and not 100% tested.

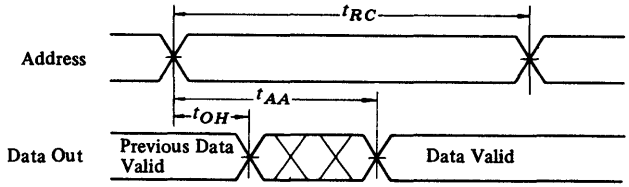
■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%*, T_a = 0 to 70°C, unless otherwise noted.)

● READ CYCLE

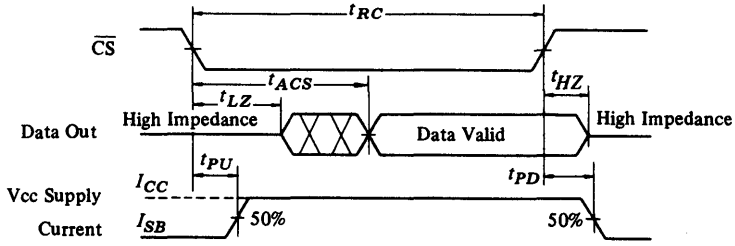
Item	Symbol	HM6267P-35		HM6267P-45		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	35	–	45	–	ns	1
Address Access Time	t_{AA}	–	35	–	45	ns	
Chip Select Access Time	t_{ACS}	–	35	–	45	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	ns	2, 3, 7
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	ns	2, 3, 7
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns	
Chip Deselection to Power Down Time	t_{PD}	–	20	–	30	ns	

* V_{CC} = 5V ± 5% for 35ns version.

● TIMING WAVEFORM OF READ CYCLE NO. 1 [4) 5)]



● TIMING WAVEFORM OF READ CYCLE NO. 2 [4) 6)]

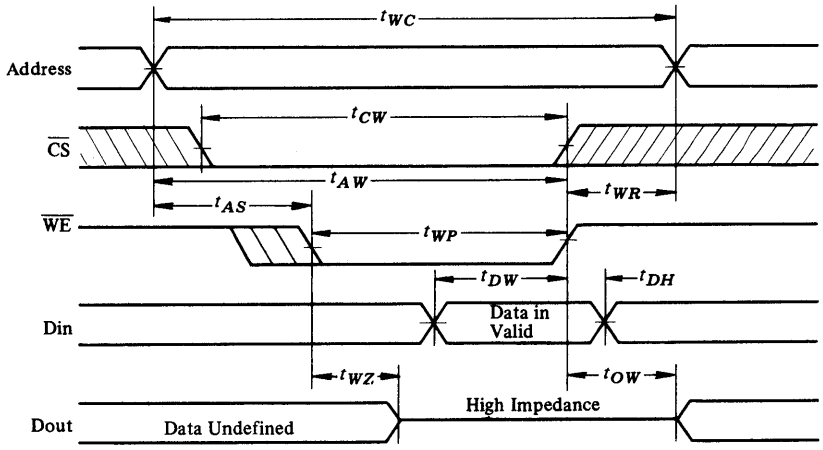


NOTES:
1. All Read Cylce timing are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is High for READ cycle.
5. Device is continuously selected, $\overline{CS}$ = V_{IL}.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

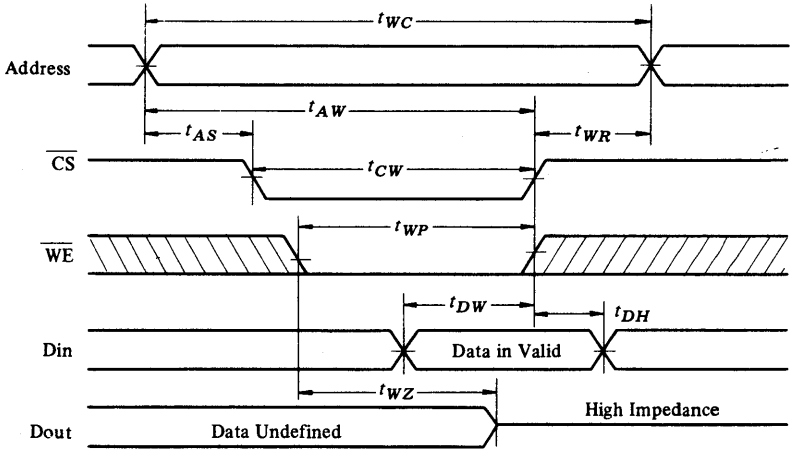
● WRITE CYCLE

Item	Symbol	HM6267P-35		HM6267P-45		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	35	–	45	–	ns	2
Chip Selection to End of Write	t_{CW}	30	–	40	–	ns	
Address Valid to End of Write	t_{AW}	30	–	40	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Write Pulse Width	t_{WP}	20	–	25	–	ns	
Write Recovery Time	t_{WR}	0	–	0	–	ns	
Data Valid to End of Write	t_{DW}	20	–	25	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Write Enabled to Output in High Z	t_{WZ}	0	20	0	25	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

- **TIMING WAVEFORM OF WRITE CYCLE NO. 1** ($\overline{WE}$ Controlled)



- **TIMING WAVEFORM OF WRITE CYCLE NO. 2** ($\overline{CS}$ Controlled)



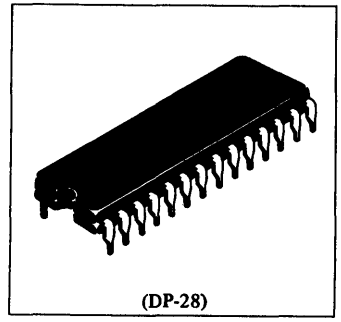
NOTES: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
2. All Write Cycle timings are referenced from the last valid address to the first transitions address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

HM6264P-10, HM6264P-12, HM6264P-15

8192-word x 8-bit High Speed Static CMOS RAM

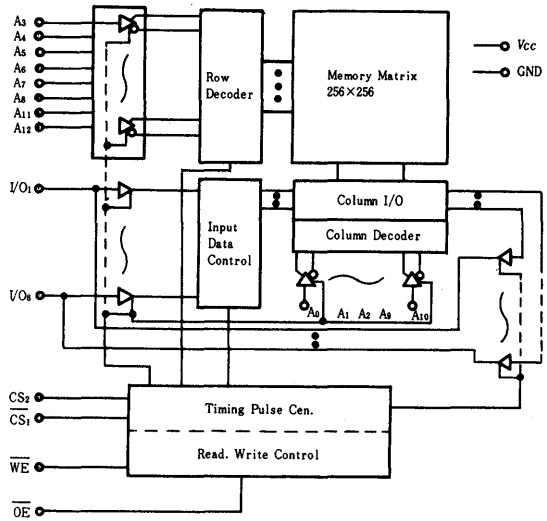
■ FEATURES

- Fast access Time — 100ns/120ns/150ns (max.)
- Low Power Standby — Standby: 0.1mW (typ.)
  Low Power Operation — Operating: 200mW (typ.)
- Single +5V Supply
- Completely Static Memory..... No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764

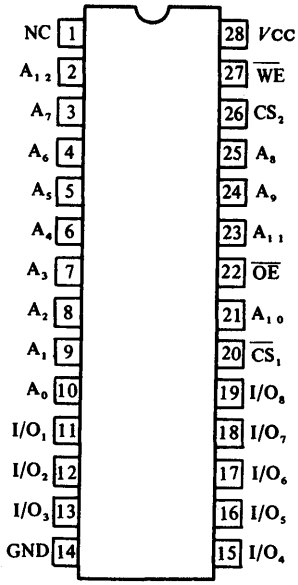


(DP-28)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	−0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

* With respect to GND. ** Pulse width 50ns: −3.0V

■ TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

X: H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.3*	–	0.8	V

* Pulse Width 50ns: −3.0V

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V±10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{in}=GND to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=GND to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS1}$=V_{IL}, CS2=V_{IH}, $I_{I/O}$=0mA	–	40	80	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $I_{I/O}$=0mA	–	60	110	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$=V_{IH} or CS2=V_{IL}	–	1	3	mA
	I_{SB1}**	$\overline{CS1}$≧V_{CC}−0.2V, CS2≧V_{CC}−0.2V or CS2≦0.2V	–	0.02	2	mA
	I_{SB2}**	CS2≦0.2V	–	0.02	2	mA
Output Voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	–	–	V

* Typical limits are at V_{CC}=5.0V, T_a=25°C and specified loading.
** V_{IL} min=−0.3V

■ CAPACITANCE (f = 1MHz, T_a = 25°C)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	8	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V±10%, Ta = 0 to +70°C)

• AC TEST CONDITIONS

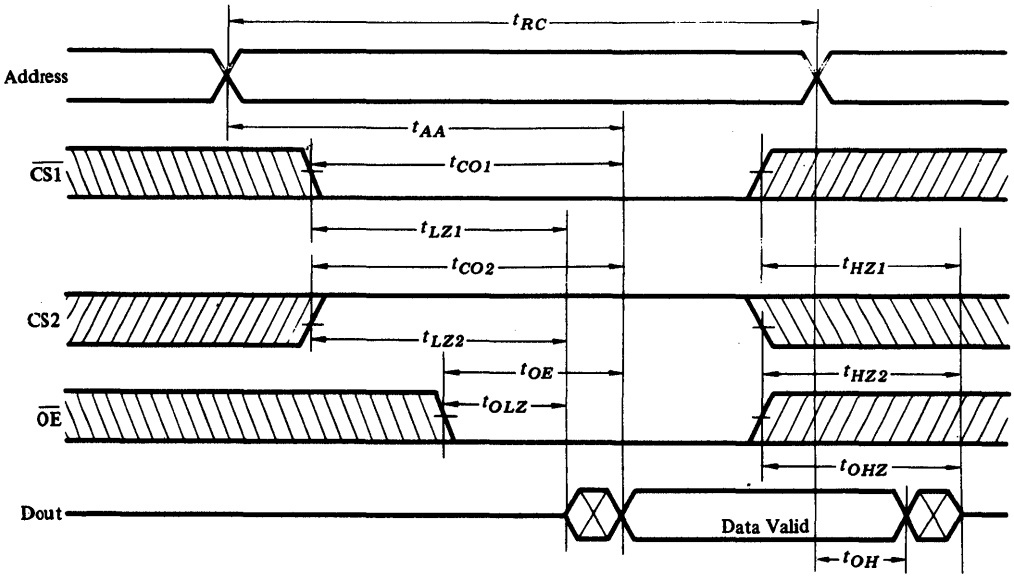
Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10ns
Input and Output Timing Reference Level: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

• READ CYCLE

Item		Symbol	HM6264P-10		HM6264P-12		HM6264P-15		Unit
			min	max	min	max	min	max	
Read Cycle Time		t_{RC}	100	–	120	–	150	–	ns
Address Access Time		t_{AA}	–	100	–	120	–	150	ns
Chip Selection to Output	$\overline{CS1}$	t_{CO1}	–	100	–	120	–	150	ns
	CS2	t_{CO2}	–	100	–	120	–	150	ns
Output Enable to Output Valid		t_{OE}	–	50	–	60	–	70	ns
Chip Selection to Output in Low Z	$\overline{CS1}$	t_{LZ1}	10	–	10	–	15	–	ns
	CS2	t_{LZ2}	10	–	10	–	15	–	ns
Output Enable to Output in Low Z		t_{OLZ}	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	$\overline{CS1}$	t_{HZ1}	0	35	0	40	0	50	ns
	CS2	t_{HZ2}	0	35	0	40	0	50	ns
Output Disable to Output in High Z		t_{OHZ}	0	35	0	40	0	50	ns
Output Hold from Address Change		t_{OH}	10	–	10	–	15	–	ns

NOTES: 1 t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
2 At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

• **READ CYCLE**

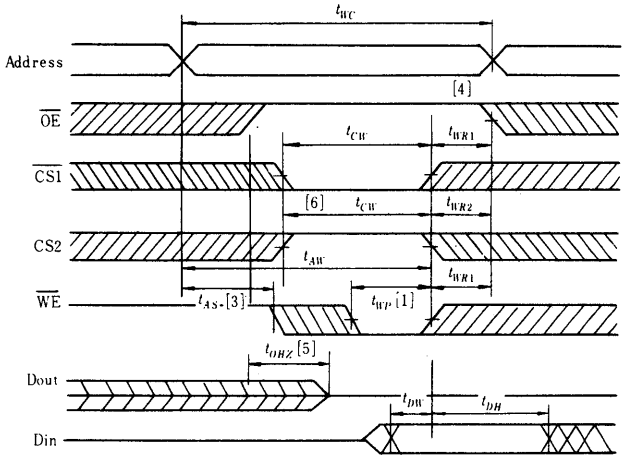


NOTE: 1) $\overline{WE}$ is high for Read Cycle

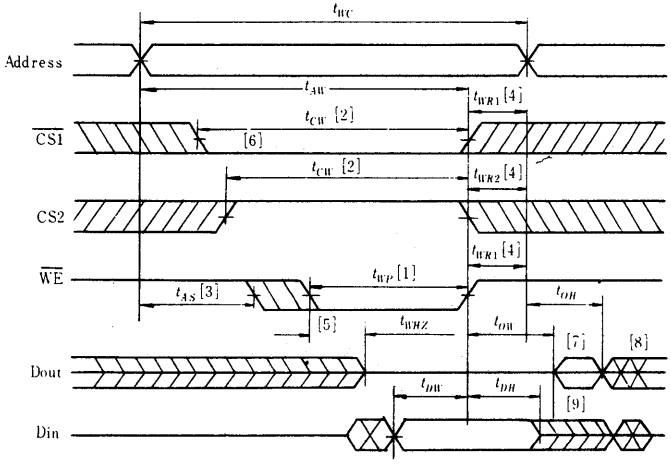
• **WRITE CYCLE**

Item		Symbol	HM6264P-10		HM6264P-12		HM6264P-15		Unit
			min	max	min	max	min	max	
Write Cycle Time		t_{WC}	100	–	120	–	150	–	ns
Chip Selection to End of Write		t_{CW}	80	–	85	–	100	–	ns
Address Setup Time		t_{AS}	0	–	0	–	0	–	ns
Address Valid to End of Write		t_{AW}	80	–	85	–	100	–	ns
Write Pulse Width		t_{WP}	60	–	70	–	90	–	ns
Write Recovery Time	$\overline{CS1}$, $\overline{WE}$	t_{WR1}	5	–	5	–	10	–	ns
	CS2	t_{WR2}	15	–	15	–	15	–	ns
Write to Output in High Z		t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap		t_{DW}	40	–	50	–	60	–	ns
Data Hold from Write Time		t_{DH}	0	–	0	–	0	–	ns
$\overline{OE}$ to Output in High Z		t_{OHZ}	0	35	0	40	0	50	ns
Output Active from End of Write		t_{OW}	5	–	5	–	10	–	ns

• **WRITE CYCLE (1) ($\overline{OE}$ clock)**

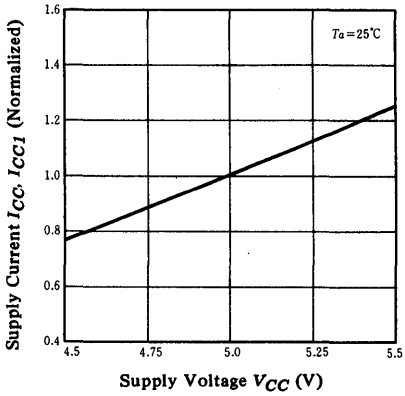


• **WRITE CYCLE (2) ($\overline{OE}$ Low Fix)**

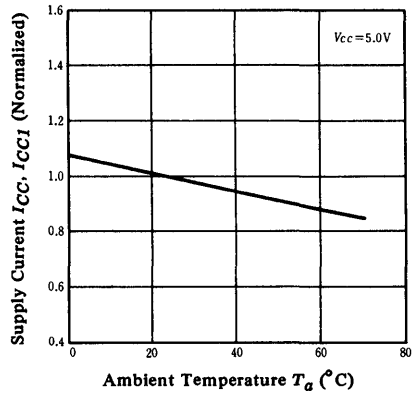


NOTES: 1) A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginninng of write to the end of write.
2) t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3) t_{AS} is measured from the address valid to the beginning of write.
4) t_{WR} is measured from the end of write to the address change.
t_{WR1} applies in case a write ends at $\overline{CS1}$ or $\overline{WE}$ going high.
t_{WR2} applies in case a write ends at CS2 going low.
5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6) If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7) Dout is the same phase of the latest written data in this write cycle.
8) Dout is the read data of next address.
9) If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

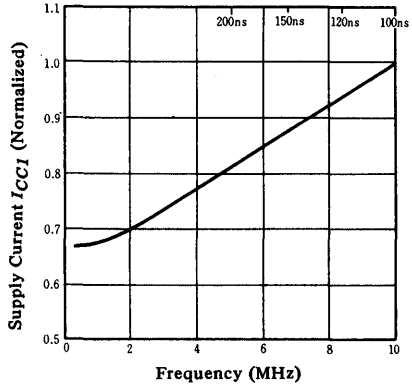
SUPPLY CURRENT vs. SUPPLY VOLTAGE



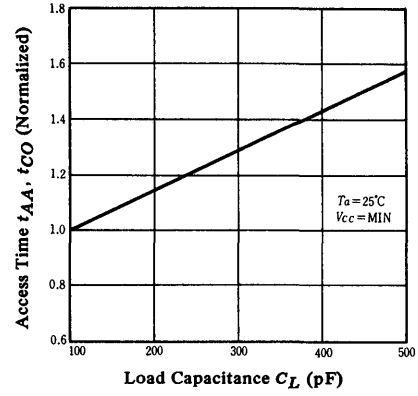
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



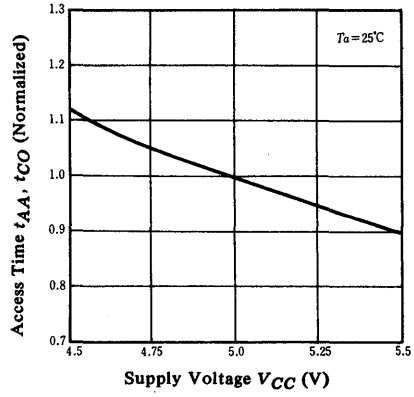
SUPPLY CURRENT vs. FREQUENCY



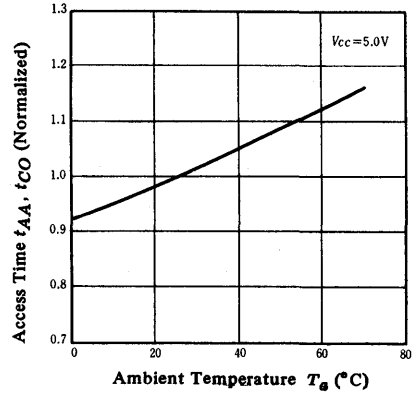
ACCESS TIME vs. LOAD CAPACITANCE



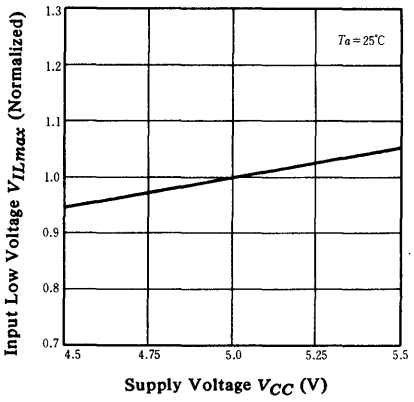
ACCESS TIME vs. SUPPLY VOLTAGE



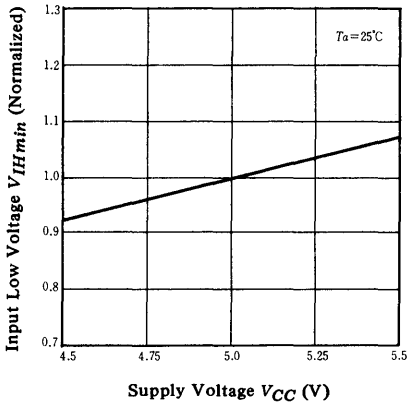
ACCESS TIME vs. AMBIENT TEMPERATURE



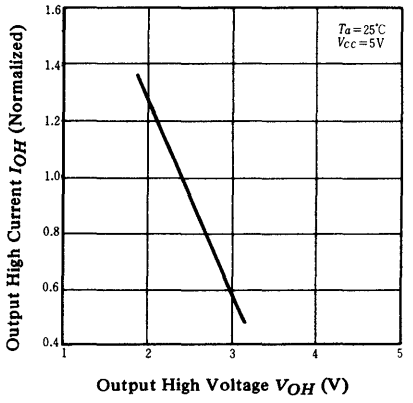
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



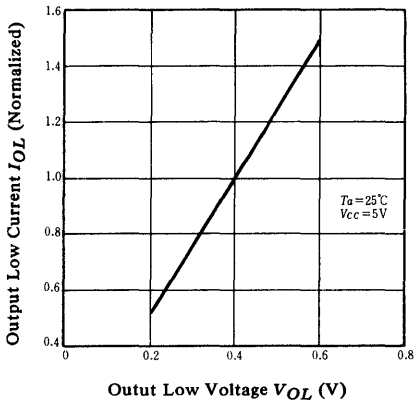
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



OUTPUT CURRENT vs. OUTPUT VOLTAGE



OUTPUT CURRENT vs. OUTPUT VOLTAGE

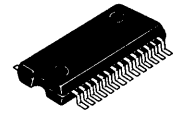


HM6264FP-12,HM6264FP-15

8192-word x 8-bit High Speed Static CMOS RAM

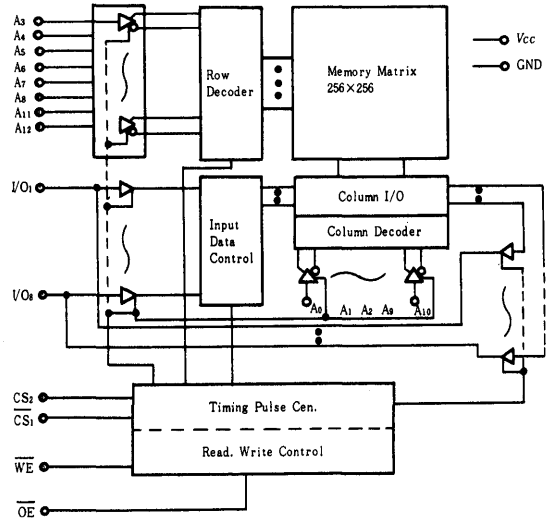
■ FEATURES

- High Density Small-sized Packaged
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- High Speed: Fast Access Time 120/150ns (max)
- Single 5V Supply
- Low Power Standby and Low Power Operation
  Standby: 0.1mW (typ.), Operation: 200mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time

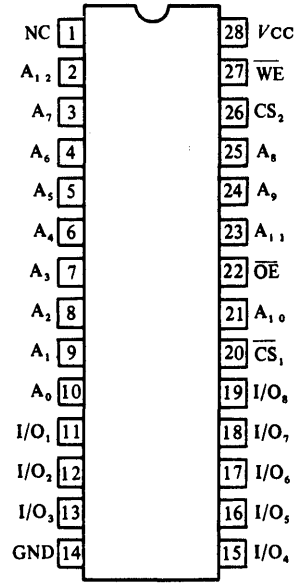


(FP-28)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	−0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

* With respect to GND. ** Pulse width 50ns: −3.0V

■ TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

X: H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.3*	–	0.8	V

* Pulse Width 50ns: −3.0V

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V±10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{in}=GND to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=GND to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS1}$=V_{IL}, CS2=V_{IH}, $I_{I/O}$=0mA	–	40	80	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $I_{I/O}$=0mA	–	60	110	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$=V_{IH} or CS2=V_{IL}	–	1	3	mA
	I_{SB1}**	$\overline{CS1}$≧V_{CC}−0.2V, CS2≧V_{CC}−0.2V or CS2≦0.2V	–	0.02	2	mA
	I_{SB2}**	CS2≦0.2V	–	0.02	2	mA
Output Voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	–	–	V

* Typical limits are at V_{CC}=5.0V, T_a=25°C and specified loading.
** V_{IL} min=−0.3V

■ CAPACITANCE (f = 1MHz, T_a = 25°C)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	8	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V±10%, Ta = 0 to +70°C)

• AC TEST CONDITIONS

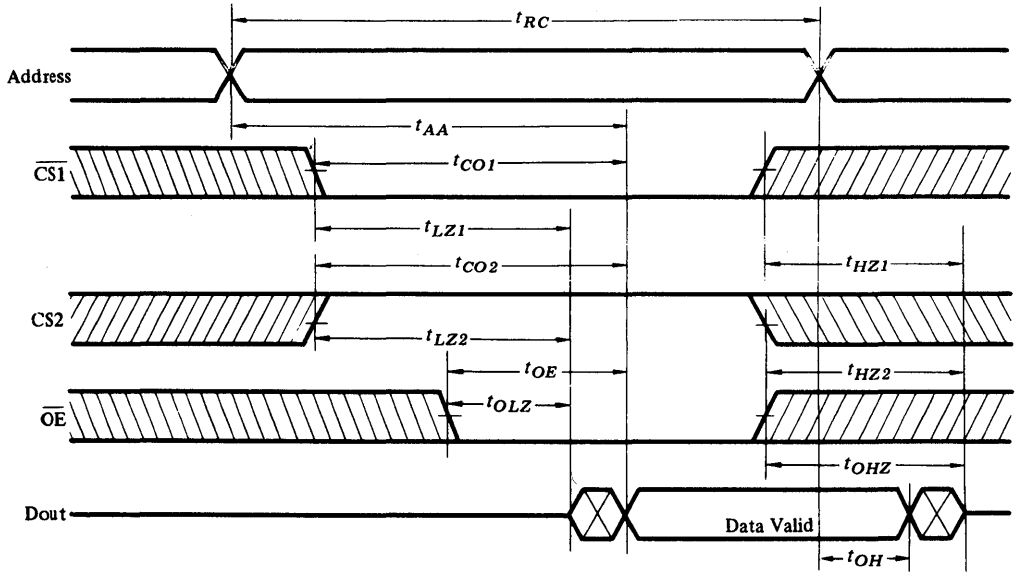
Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10ns
Input and Output Timing Reference Level: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

• READ CYCLE

Item		Symbol	HM6264FP-12		HM6264FP-15		Unit
			min	max	min	max	
Read Cycle Time		t_{RC}	120	–	150	–	ns
Address Access Time		t_{AA}	–	120	–	150	ns
Chip Selection to Output	$\overline{CS1}$	t_{CO1}	–	120	–	150	ns
	CS2	t_{CO2}	–	120	–	150	ns
Output Enable to Output Valid		t_{OE}	–	60	–	70	ns
Chip Selection to Output in Low Z	$\overline{CS1}$	t_{LZ1}	10	–	15	–	ns
	CS2	t_{LZ2}	10	–	15	–	ns
Output Enable to Output in Low Z		t_{OLZ}	5	–	5	–	ns
Chip Deselection to Output in High Z	$\overline{CS1}$	t_{HZ1}	0	40	0	50	ns
	CS2	t_{HZ2}	0	40	0	50	ns
Output Disable to Output in High Z		t_{OHZ}	0	40	0	50	ns
Output Hold from Address Change		t_{OH}	10	–	15	–	ns

NOTES: 1 t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
2 At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

• READ CYCLE

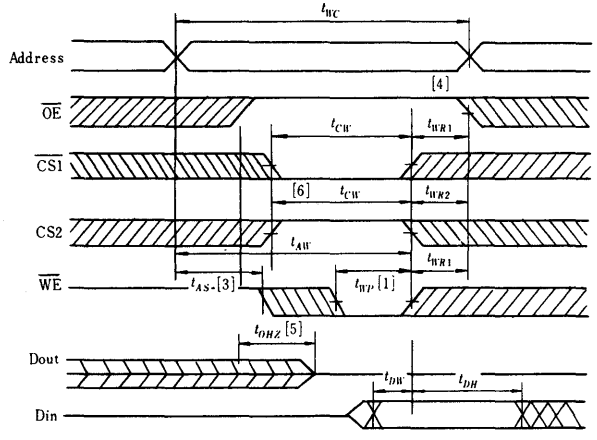


NOTE: 1) $\overline{WE}$ is high for Read Cycle

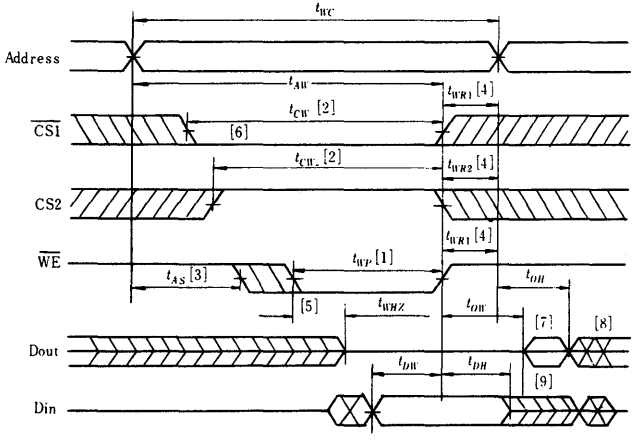
• WRITE CYCLE

Item		Symbol	HM6264FP-12		HM6264FP-15		Unit
			min	max	min	max	
Write Cycle Time		t_{WC}	120	–	150	–	ns
Chip Selection to End of Write		t_{CW}	85	–	100	–	ns
Address Setup Time		t_{AS}	0	–	0	–	ns
Address Valid to End of Write		t_{AW}	85	–	100	–	ns
Write Pulse Width		t_{WP}	70	–	90	–	ns
Write Recovery Time	$\overline{CS1}$, $\overline{WE}$	t_{WR1}	55	–	10	–	ns
	CS2	t_{WR2}	15	–	15	–	ns
Write to Outputiin High Z		t_{WHZ}	0	40	0	50	ns
Data to Write Time Overlap		t_{DW}	50	–	60	–	ns
Data Hold from Write Time		t_{DH}	0	–	0	–	ns
OE to Output in High Z		t_{OHZ}	0	40	0	50	ns
Output Active from End of Write		t_{OW}	5	–	10	–	ns

• **WRITE CYCLE (1) ($\overline{OE}$ clock)**



• **WRITE CYCLE (2) ($\overline{OE}$ Low Fix)**



NOTES: 1) A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginninng of write to the end of write.

2) t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.

3) t_{AS} is measured from the address valid to the beginning of write.

4) t_{WR} is measured from the end of write to the address change.
t_{WR1} applies in case a write ends at $\overline{CS1}$ or $\overline{WE}$ going high.
t_{WR2} applies in case a write ends at CS2 going low.

5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

6) If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.

7) Dout is the same phase of the latest written data in this write cycle.

8) Dout is the read data of next address.

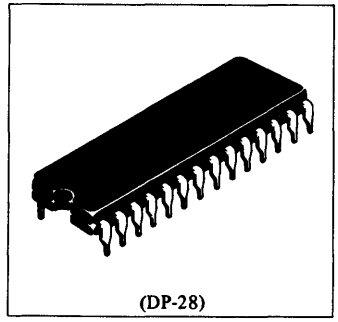
9) If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

HM6264LP-10, HM6264LP-12
HM6264LP-15

8192-word x 8-bit High Speed Static CMOS RAM

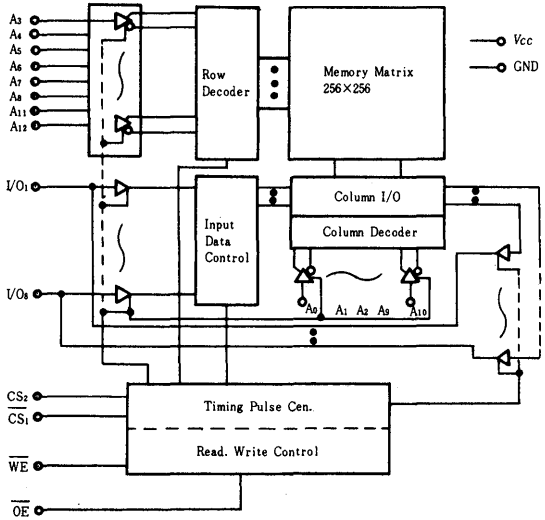
■ FEATURES

- Fast access Time — 100ns/120ns/150ns (max.)
- Low Power Standby — Standby: 0.01mW (typ.)
  Low Power Operation — Operating: 200mW (typ.)
- Capability of Battery Back-up Operation
- Single +5V Supply
- Completely Static Memory. . . . . No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764

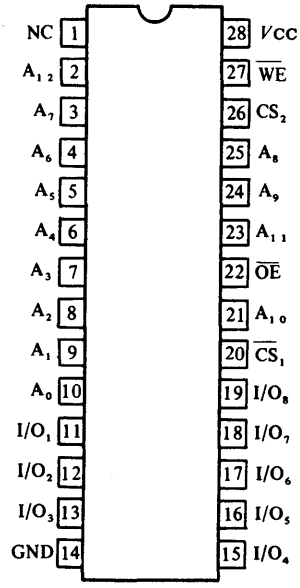


(DP-28)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	−0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

* With respect to GND. ** Pulse width 50ns: −3.0V

■ TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

X: H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.3*	–	0.8	V

* Pulse Width 50ns: −3.0V

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V±10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{in}=GND to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=GND to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS1}$=V_{IL}, CS2=V_{IH}, $I_{I/O}$=0mA	–	40	80	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $I_{I/O}$=0mA	–	60	110	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$=V_{IH} or CS2=V_{IL}	–	1	3	mA
	I_{SB1}**	$\overline{CS1}$≧V_{CC}−0.2V, CS2≧V_{CC}−0.2V or CS2≦0.2V	–	2	100	μA
	I_{SB2}**	CS2≦0.2V	–	2	100	μA
Output Voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	–	–	V

* Typical limits are at V_{CC}=5.0V, T_a=25°C and specified loading.
** V_{IL} min=−0.3V

■ CAPACITANCE (f= 1MHz, T_a = 25°C)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	8	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V±10%, Ta = 0 to +70°C)

• AC TEST CONDITIONS

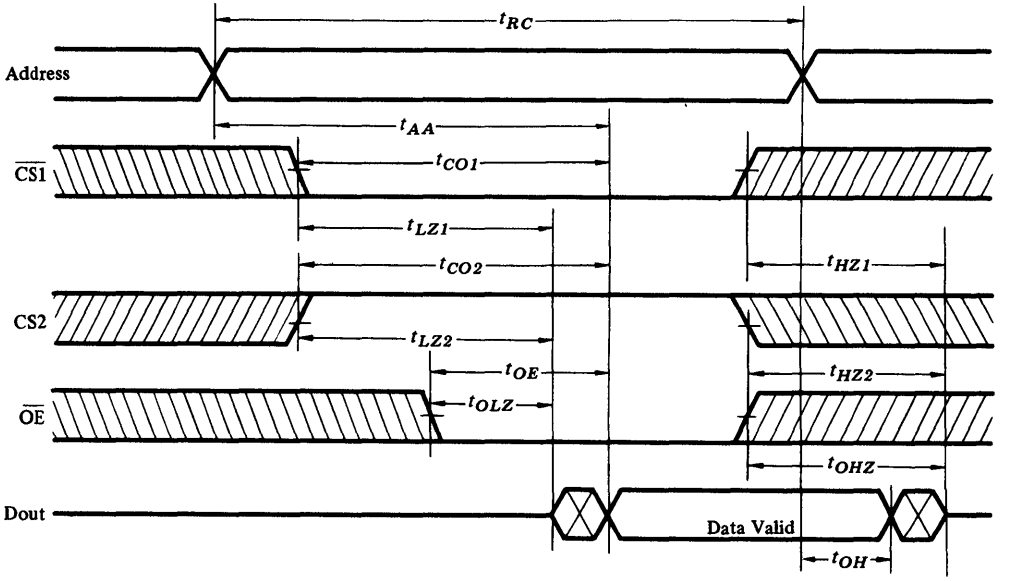
Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10ns
Input and Output Timing Reference Level: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

• READ CYCLE

Item		Symbol	HM6264LP-10		HM6264LP-12		HM6264LP-15		Unit
			min	max	min	max	min	max	
Read Cycle Time		t_{RC}	100	–	120	–	150	–	ns
Address Access Time		t_{AA}	–	100	–	120	–	150	ns
Chip Selection to Output	$\overline{CS1}$	t_{CO1}	–	100	–	120	–	150	ns
	CS2	t_{CO2}	–	100	–	120	–	150	ns
Output Enable to Output Valid		t_{OE}	–	50	–	60	–	70	ns
Chip Selection to Output in Low Z	$\overline{CS1}$	t_{LZ1}	10	–	10	–	15	–	ns
	CS2	t_{LZ2}	10	–	10	–	15	–	ns
Output Enable to Output in Low Z		t_{OLZ}	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	$\overline{CS1}$	t_{HZ1}	0	35	0	40	0	50	ns
	CS2	t_{HZ2}	0	35	0	40	0	50	ns
Output Disable to Output in High Z		t_{OHZ}	0	35	0	40	0	50	ns
Output Hold from Address Change		t_{OH}	10	–	10	–	15	–	ns

NOTES: 1 t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
2 At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

• **READ CYCLE**

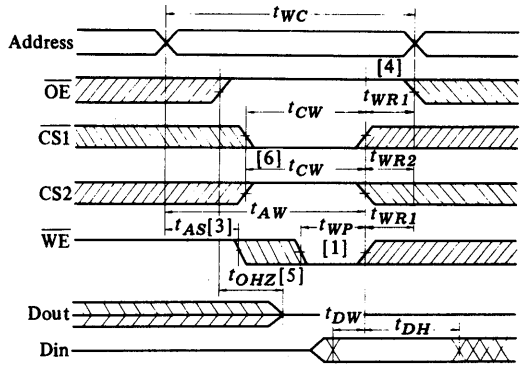


NOTE : 1) $\overline{WE}$ is high for Read Cycle

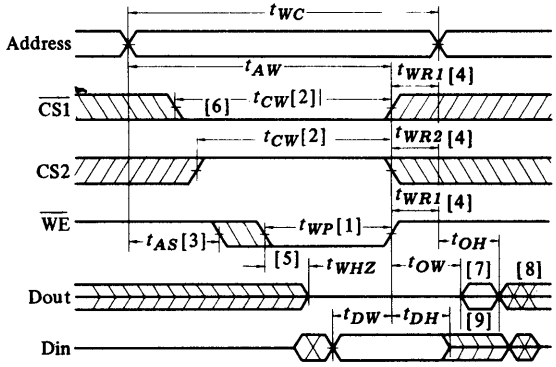
• **WRITE CYCLE**

Item		Symbol	HM6264LP-10		HM6264LP-12		HM6264LP-15		Unit
			min	max	min	max	min	max	
Write Cycle Time		t_{WC}	100	–	120	–	150	–	ns
Chip Selection to End of Write		t_{CW}	80	–	85	–	100	–	ns
Address Setup Time		t_{AS}	0	–	0	–	0	–	ns
Address Valid to End of Write		t_{AW}	80	–	85	–	100	–	ns
Write Pulse Width		t_{WP}	60	–	70	–	90	–	ns
Write Recovery Time	$\overline{CS1}$, $\overline{WE}$	t_{WR1}	5	–	5	–	10	–	ns
	CS2	t_{WR2}	15	–	15	–	15	–	ns
Write to Output in High Z		t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap		t_{DW}	40	–	50	–	60	–	ns
Data Hold from Write Time		t_{DH}	0	–	0	–	0	–	ns
$\overline{OE}$ to Output in High Z		t_{OHZ}	0	35	0	40	0	50	ns
Output Active from End of Write		t_{OW}	5	–	5	–	10	–	ns

• **WRITE CYCLE (1) ($\overline{OE}$ clock)**



• **WRITE CYCLE (2) ($\overline{OE}$ Low Fix)**



NOTES: 1) A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transtion among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginninng of write to the end of write.

2) t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.

3) t_{AS} is measured from the address valid to the beginning of write.

4) t_{WR} is measured from the end of write to the address change.
t_{WR1} applies in case a write ends at $\overline{CS1}$ or $\overline{WE}$ going high.
t_{WR2} applies in case a write ends at CS2 going low.

5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

6) If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.

7) Dout is the same phase of the latest written data in this write cycle.

8) Dout is the read data of next address.

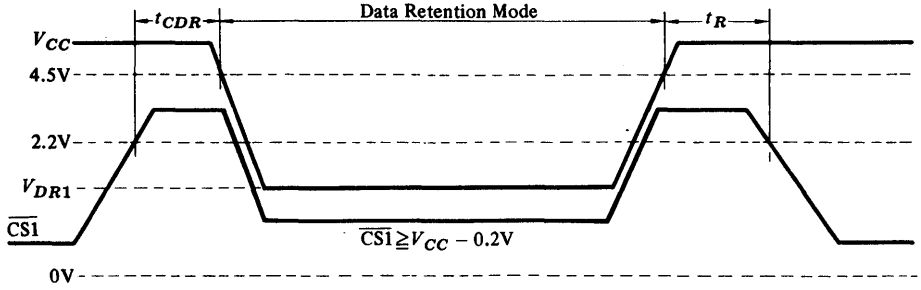
9) If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70 °C)

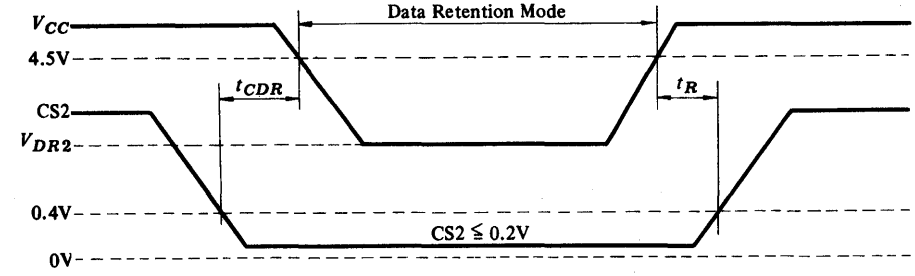
Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR1}	$\overline{CS1} \geqq V_{CC} - 0.2V$, $CS2 \geqq V_{CC} - 0.2V$ or $CS2 \leqq 0.2V$	2.0	–	–	V
	V_{DR2}	$CS2 \leqq 0.2V$	2.0	–	–	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3.0V, $\overline{CS1} \geqq V_{CC} - 0.2V$, $CS2 \geqq V_{CC} - 0.2V$ or $CS2 \leqq 0.2V$	–	1	50*	μA
	I_{CCDR2}	V_{CC} = 3.0V, $CS2 \leqq 0.2V$	–	1	50*	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}**	–	–	ns

* V_{IL} min = −0.3V, 20μA max at T_a=0~40°C
** t_{RC} = Read Cycle Time

• LOW Vcc DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)

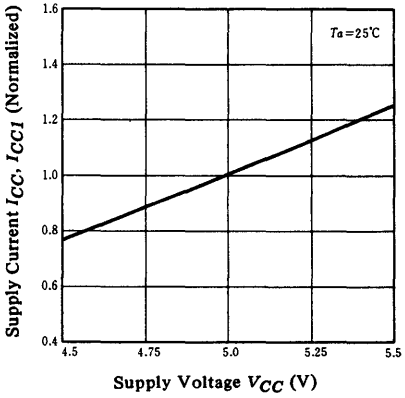


• LOW Vcc DATA RETENTION WAVEFORM (2) (CS2 Controlled)

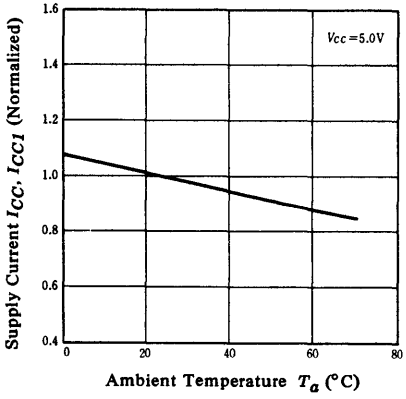


NOTE: In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and Din buffer. If CS2 controls data retention mode, Vin for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either $CS2 \geq Vcc - 0.2V$ or $CS2 \leq 0.2V$. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/$\overline{O}$) can be in the high impedance state.

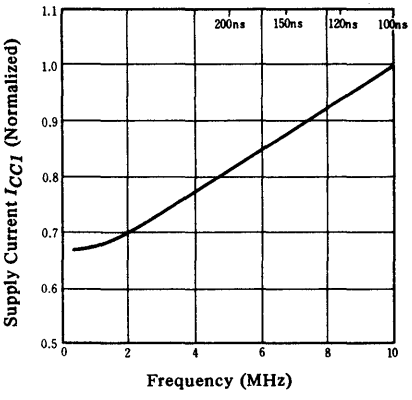
SUPPLY CURRENT vs. SUPPLY VOLTAGE



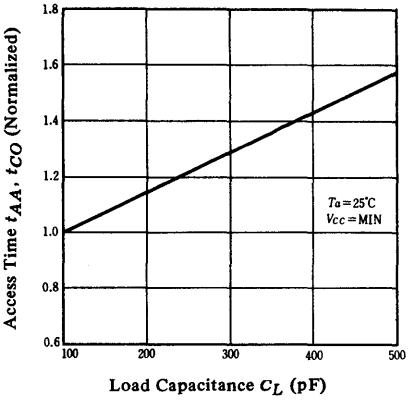
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



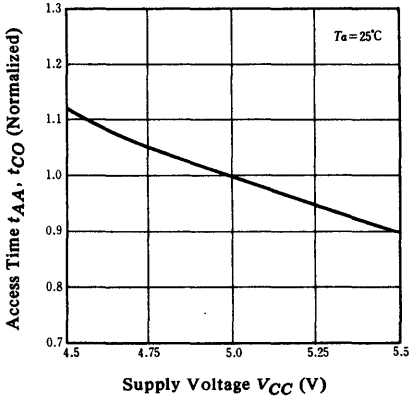
SUPPLY CURRENT vs. FREQUENCY



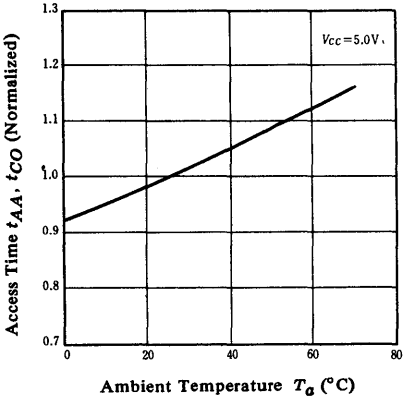
ACCESS TIME vs. LOAD CAPACITANCE



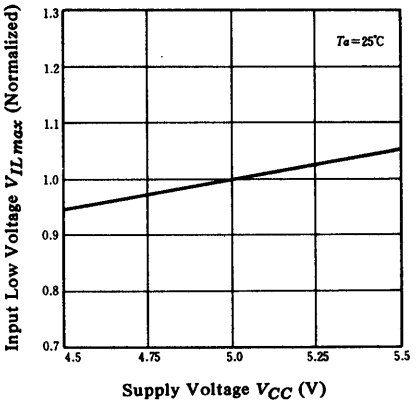
ACCESS TIME vs. SUPPLY VOLTAGE



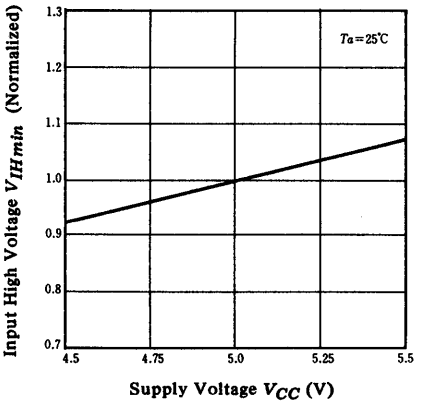
ACCESS TIME vs. AMBIENT TEMPERATURE



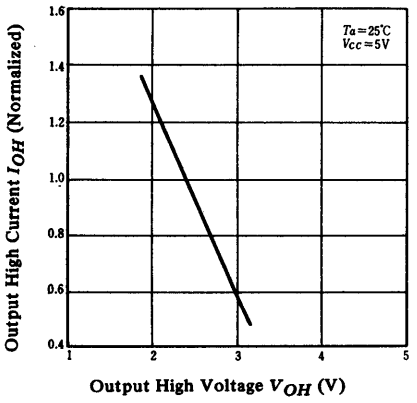
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



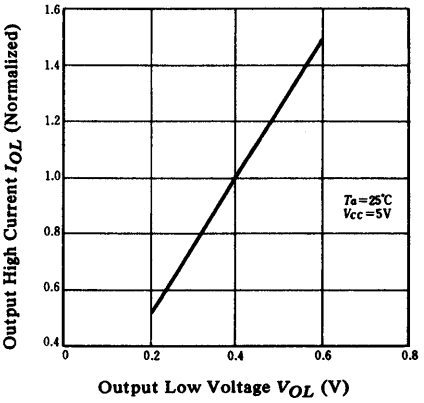
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



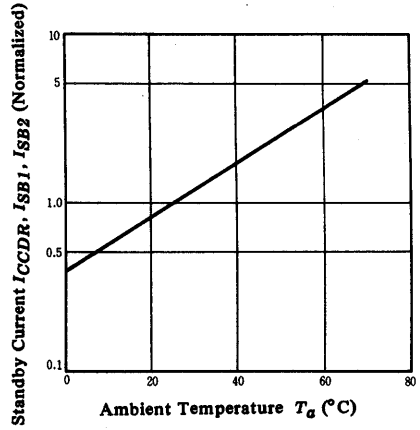
OUTPUT CURRENT vs. OUTPUT VOLTAGE



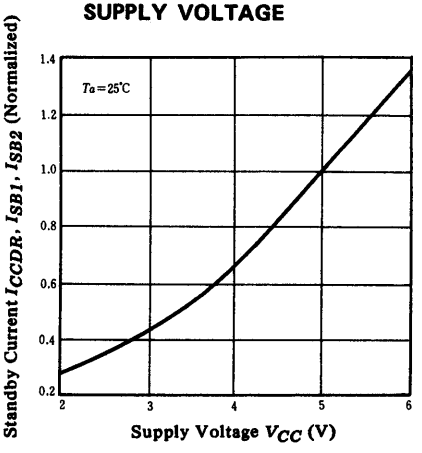
OUTPUT CURRENT vs. OUTPUT VOLTAGE



STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE

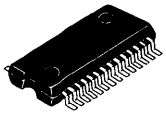


HM6264LFP-12,HM6264LFP-15

8192-word x 8-bit High Speed Static CMOS RAM

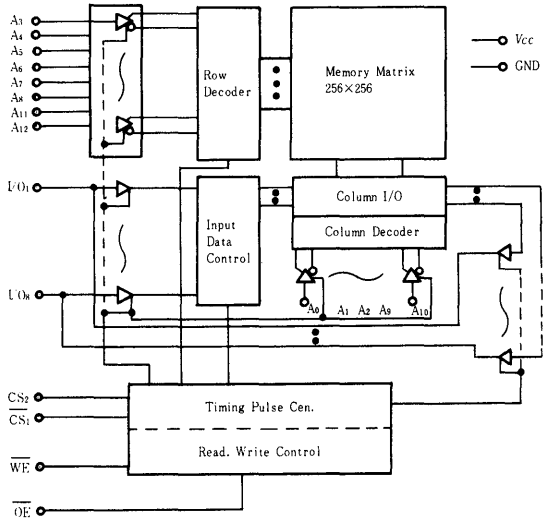
■ FEATURES

- High Density Small-sized Packaged
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- High Speed: Fast Access Time 120/150ns (max)
- Single 5V Supply
- Low Power Standby and Low Power Operation
  Standby: 10μW (typ.), Operation: 200mW (typ.)
- Capability of Battery Back-up Operation
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time

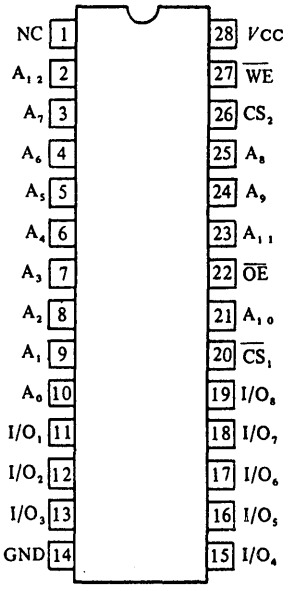


(FP-28)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	−0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

* With respect to GND. ** Pulse width 50ns: −3.0V

■ TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

X: H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.3*	–	0.8	V

* Pulse Width 50ns: −3.0V

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V±10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{in}=GND to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=GND or V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS1}$=V_{IL}, CS2=V_{IH}, $I_{I/O}$=0mA	–	40	80	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $I_{I/O}$=0mA	–	60	110	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$=V_{IH} or CS2=V_{IL}	–	1	3	mA
	I_{SB1}**	$\overline{CS1}$≧V_{CC}−0.2V, CS2≧V_{CC}−0.2V or CS2≦0.2V	–	2	100	μA
	I_{SB2}**	CS2≦0.2V	–	2	100	μA
Output Voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	–	–	V

* Typical limits are at V_{CC}=5.0V, T_a=25°C and specified loading.
** V_{IL} min=−0.3V

■ CAPACITANCE (f= 1MHz, T_a = 25°C)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	8	pF

Note) This parameter is sampled and not 100% tested.

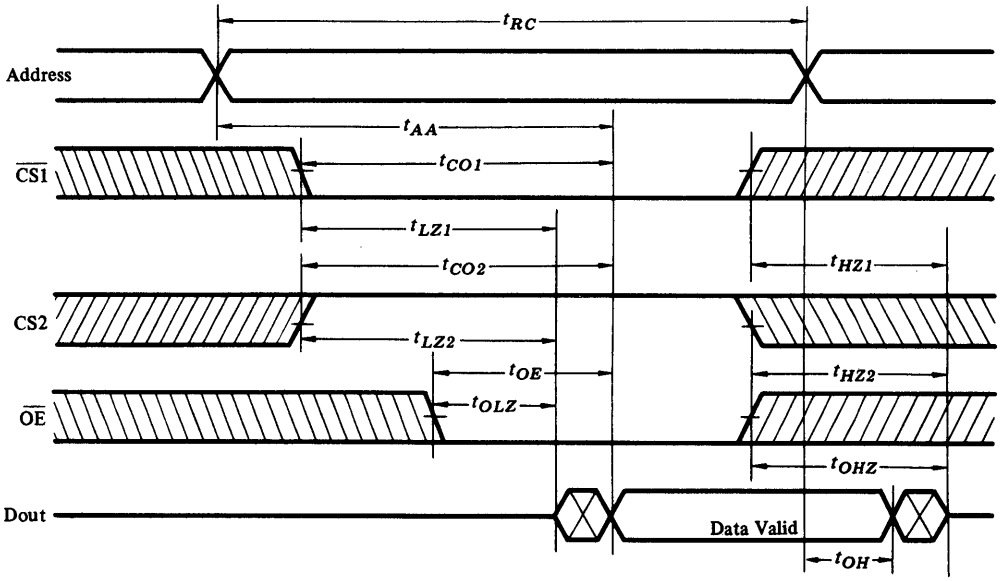
■ AC CHARACTERISTICS (V_{CC} = 5V±10%, Ta = 0 to +70°C)

- **AC TEST CONDITIONS**
  - Input Pulse Levels: 0.8 to 2.4V
  - Input Rise and Fall Times: 10ns
  - Input and Output Timing Reference Level: 1.5V
  - Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)
- **READ CYCLE**

Item		Symbol	HM6264LFP-12		HM6264LFP-15		Unit
			min	max	min	max	
Read Cycle Time		t_{RC}	120	–	150	–	ns
Address Access Time		t_{AA}	–	120	–	150	ns
Chip Selection to Output	$\overline{CS1}$	t_{CO1}	–	120	–	150	ns
	CS2	t_{CO2}	–	120	–	150	ns
Output Enable to Output Valid		t_{OE}	–	60	–	70	ns
Chip Selection to Output in Low Z	$\overline{CS1}$	t_{LZ1}	10	–	15	–	ns
	CS2	t_{LZ2}	10	–	15	–	ns
Output Enable to Output in Low Z		t_{OLZ}	5	–	5	–	ns
Chip Deselection to Output in High Z	$\overline{CS1}$	t_{HZ1}	0	40	0	50	ns
	CS2	t_{HZ2}	0	40	0	50	ns
Output Disable to Output in High Z		t_{OHZ}	0	40	0	50	ns
Output Hold from Address Change		t_{OH}	10	–	15	–	ns

NOTES: 1 t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
2 At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

• **READ CYCLE**

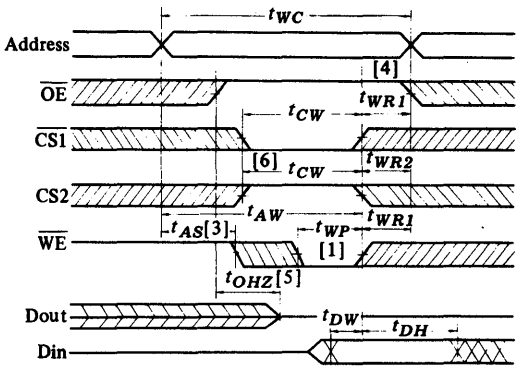


NOTE : 1) $\overline{WE}$ is high for Read Cycle

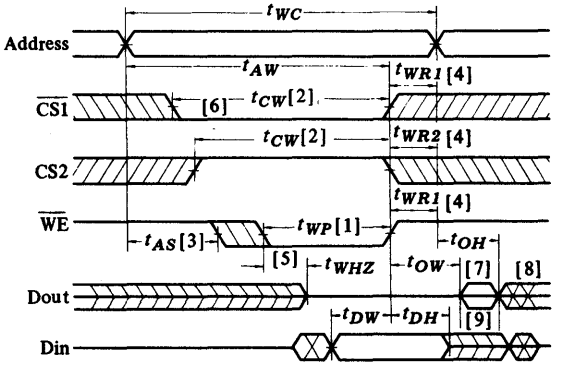
• **WRITE CYCLE**

Item		Symbol	HM6264LFP-12		HM6264LFP-15		Unit
			min	max	min	max	
Write Cycle Time		t_{WC}	120	–	150	–	ns
Chip Selection to End of Write		t_{CW}	85	–	100	–	ns
Address Setup Time		t_{AS}	0	–	0	–	ns
Address Valid to End of Write		t_{AW}	85	–	100	–	ns
Write Pulse Width		t_{WP}	70	–	90	–	ns
Write Recovery Time	$\overline{CS1}$, $\overline{WE}$	t_{WR1}	5	–	10	–	ns
	CS2	t_{WR2}	15	–	15	–	ns
Write to Output in High Z		t_{WHZ}	0	40	0	50	ns
Data to Write Time Overlap		t_{DW}	50	–	60	–	ns
Data Hold from Write Time		t_{DH}	0	–	0	–	ns
OE to Output in High Z		t_{OHZ}	0	40	0	50	ns
Output Active from End of Write		t_{OW}	5	–	10	–	ns

• **WRITE CYCLE (1) ($\overline{OE}$ clock)**



• **WRITE CYCLE (2) ($\overline{OE}$ Low Fix)**



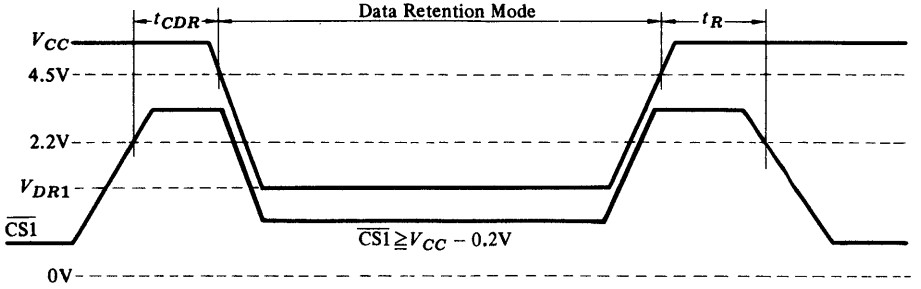
NOTES: 1) A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transtion among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginninng of write to the end of write.
2) t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3) t_{AS} is measured from the address valid to the beginning of write.
4) t_{WR} is measured from the end of write to the address change.
t_{WR1} applies in case a write ends at $\overline{CS1}$ or $\overline{WE}$ going high.
t_{WR2} applies in case a write ends at CS2 going low.
5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6) If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7) Dout is the same phase of the latest written data in this write cycle.
8) Dout is the read data of next address.
9) If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70 °C)

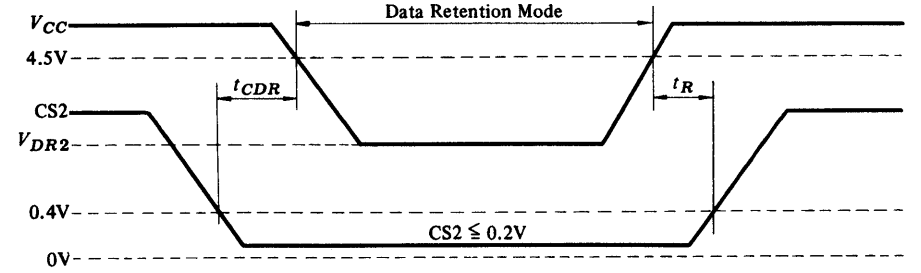
Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR1}	$\overline{CS1} \geqq V_{CC} - 0.2V$, $CS2 \geqq V_{CC} - 0.2V$ or $CS2 \leqq 0.2V$	2.0	–	–	V
	V_{DR2}	$CS2 \leqq 0.2V$	2.0	–	–	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3.0V, $\overline{CS1} \geqq V_{CC} - 0.2V$, $CS2 \geqq V_{CC} - 0.2V$ or $CS2 \leqq 0.2V$	–	1	50*	μA
	I_{CCDR2}	V_{CC} = 3.0V, $CS2 \leqq 0.2V$	–	1	50*	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}**	–	–	ns

* V_{IL} min = −0.3V, 20μA max at T_a=0 ~ 40°C.
** t_{RC} = Read Cycle Time

• LOW Vcc DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)



• LOW Vcc DATA RETENTION WAVEFORM (2) (CS2 Controlled)



NOTE: In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and Din buffer. If CS2 controls data retention mode, Vin for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either $CS2 \geq Vcc - 0.2V$ or $CS2 \leq 0.2V$. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O)can be in the high impedance state.

HM6287P/HM6287CG Series

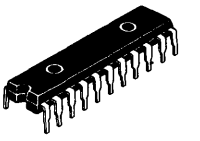
Under Development

65536-word x 1-bit High Speed Static CMOS RAM

■ FEATURES

- High Speed: Fast Access Time 55/70ns (max.)
- Low Power-Standby and Low Power Operation
  Standby: 0.1mW (typ.), Operation: 300mW (typ.)
- Single 5V Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Inputs and Output

HM6287P-55, HM6287P-70

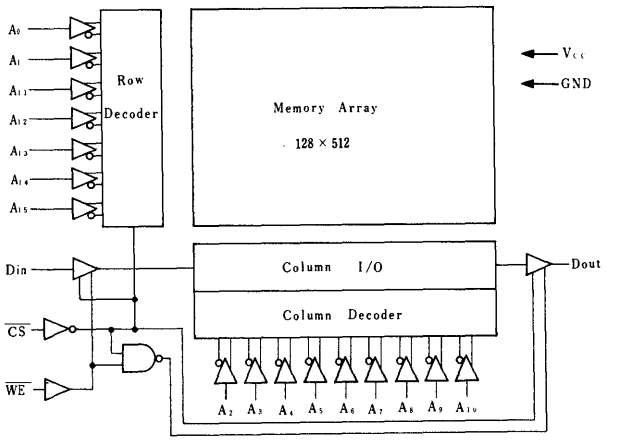


(DP-22A)

HM6287CG-55, HM6287CG-70

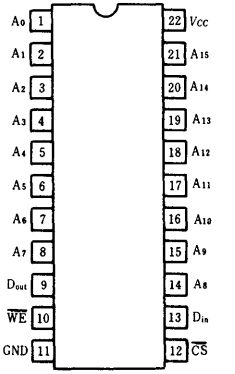
(CG-22)

■ BLOCK DIAGRAM



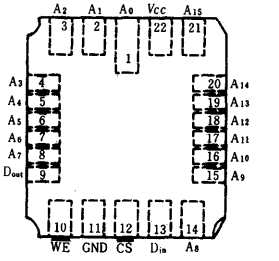
■ PIN ARRANGEMENT

- HM6287P Series



(Top View)

- HM6287CG Series



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin*	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature**	T_{stg}	−65 to +150	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

* with respect to GND. $V_{T\ min}$ = −3.5V (Pulse width 20ns)
** −55 to +125°C for Plastic DIP

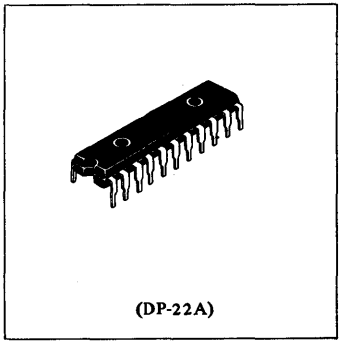
HM6287LP Series

Under Development

65536-word x 1-bit High Speed Static CMOS RAM

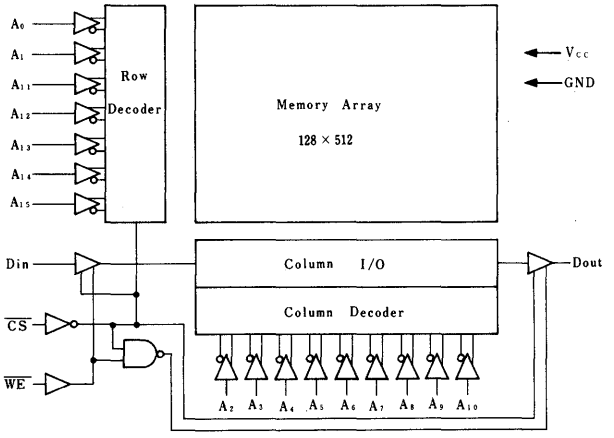
■ FEATURES

- High Speed: Fast Access Time 55/70ns (max.)
- Low Power Standby and Low Power Operation
  Standby: 10μW (typ.), Operation: 300mW (typ.)
- Capability of Battery Back-up Operation
- Single 5V Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Inputs and Output

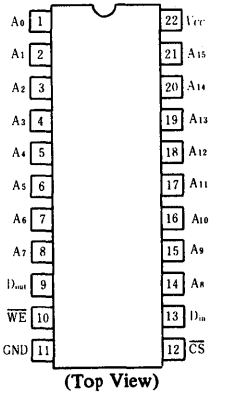


(DP-22A)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin*	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

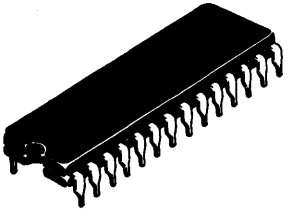
* with respect to GND. V_T min = −3.5V (Pulse width 20ns)

HM65256P Series

Under Development

32768-word x 8-bit High Speed Pseudo Static CMOS RAM

The HM65256P is a 32,768-words x 8-bits, high speed, pseudo static CMOS Random Access memory.
This new breed of pseudo static RAM utilizes HITACHI's double-layers CMOS technology and advanced circuit techniques for high performance and high functional density.
The HM65256P is offered in a standard 600 mil 28 pin dual-in-line plastic package, and guaranteed for operation from 0°C to 70°C at the condition of 5-V single power supply with ±10% tolerances.
All inputs and outputs are compatible with high performance logic families, such as Schottky TTL.
As for refresh functions, including address refresh, refresh control function available on 22 pin provides automatic and self-refresh modes.



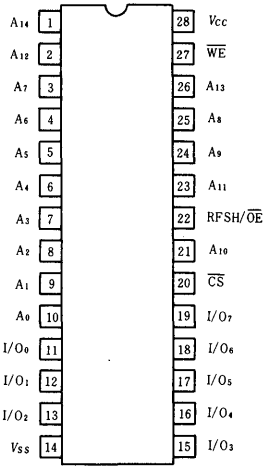
(DP-28)

■ FEATURES

- Organized as 32768-words x 8-bits
- Single 5V Power Supply
- High Speed · · · · · Access Time 150/200ns (max).
- Control on Pin-22 for automatic and self reflesh
- Equal access and cycle time
- All inputs and outputs TTL compatible
- 22 pin function

$\overline{CS}$	$\overline{OE}$/RFSH
H	RFSH
L	$\overline{OE}$

■ PIN ARRANGEMENT



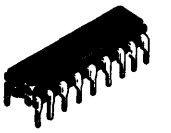
(Top View)

MOS DYNAMIC RAM

HM48416AP-12, HM48416AP-15
HM48416AP-20

16384-word X 4-bit Dynamic Random Access Memory

HM48416AP-12, HM48416AP-15, HM48416AP-20

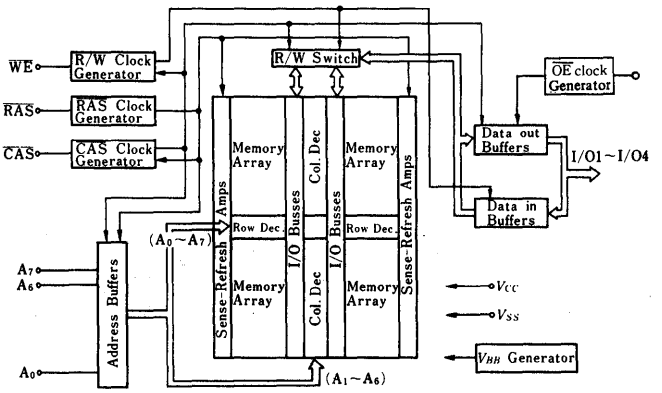


(DP-18)

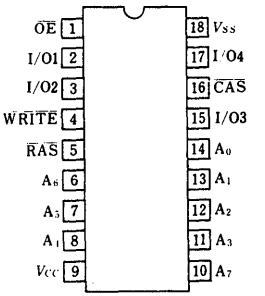
■ FEATURES

- 16384-word x 4-bit Organization
- Single 5V (±10%)
- Low Power; 303mW Active, 20mW Standby
- High speed: Access Time 120ns/150ns/200ns (max)
- Page mode capability
- Output data controlled by $\overline{CAS}$, $\overline{OE}$
- TTL compatible
- 128 refresh cycles ($A_0 \sim A_6$, 2ms)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

A0~A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
I/O1~I/O4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperatue	T_{stg}	−55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.4	–	6.5	V
	V_{IL}	−1.0	–	0.8	V

Note All voltages referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (Ta=0 to 70°C, V_{CC}=5V±10%, V_{SS}=0V)

Paramater	Smbol	HM48416AP -12		HM48416AP -15		HM48416AP -20		Unit	Notes
		min	max	min	max	min	max		
Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=min)	I_{CC1}	–	60	–	55	–	45	mA	1, 2
Standby Current ($\overline{RAS}$=V_{IH}, Dout=High Impedance)	I_{CC2}	–	3.5	–	3.5	–	3.5	mA	
Refresh Current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}, t_{RC}=min)	I_{CC3}	–	42	–	38	–	33	mA	2
Standby Current ($\overline{RAS}$=V_{IH}, Dout Enable)	I_{CC5}	–	5.5	–	5.5	–	5.5	mA	1
Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling; t_{PC}=min)	I_{CC6}	–	42	–	38	–	33	mA	1, 2
Input Leakage (0< V_{in} <6.5V)	I_{LI}	–10	10	–10	10	–10	10	μA	
Output Leakage (Dout is disabled, 0< V_{out}<5.5V)	I_{LO}	–10	10	–10	10	–10	10	μA	
Output Levels High (I_{out}=–5mA)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Levels Low (I_{out}=4.2mA)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Notes) 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

■ CAPACITANCE (V_{CC}=5V±10%, Ta=25°C)

Parameter		Symbol	typ	max	Unit	Notes
Input Capacitance	Address	C_{in1}	–	5	pF	1
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$	C_{in2}	–	10	pF	1
Output Capacitance	Data In/Data out	$C_{I/O}$	–	10	pF	1, 2

Notes) 1. Capacitance mesured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Ta=0 to 70°C, V_{CC}=5V±10%, V_{SS}=0V)[1), 10)]

Parameter	Symbol	HM48416AP-12		HM48416AP-15		HM48416AP-20		Unit	Note
		min	mas	min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	230	–	260	–	330	–	ns	
Read-Write Cycle Time	t_{RWC}	320	–	360	–	450	–	ns	
Page Mode Cycle Time	t_{PC}	130	–	145	–	190	–	ns	
Access Time from $\overline{RAS}$	t_{RAC}	–	120	–	150	–	200	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	–	60	–	75	–	100	ns	3, 4
Output Buffer Turn-off Delay referenced to $\overline{CAS}$	t_{OFF1}	–	35	–	40	–	50	ns	5
Transition Time (Rise and Fall)	t_T	3	35	3	35	3	50	ns	6
$\overline{RAS}$ Precharge Time	t_{RP}	100	–	100	–	120	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	60	–	75	–	100	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	120	–	150	–	200	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	–10	–	–10	–	–10	–	ns	
Row Address Set-up Time	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	15	–	15	–	20	–	ns	
Column Address Set-up Time	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	20	–	25	–	30	–	ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	80	–	100	–	130	–	ns	
Write Command Set-up Time	t_{WCS}	0	–	0	–	0	–	ns	8
Write Command Hold Time	t_{WCH}	40	–	45	–	55	–	ns	

(to be continued)

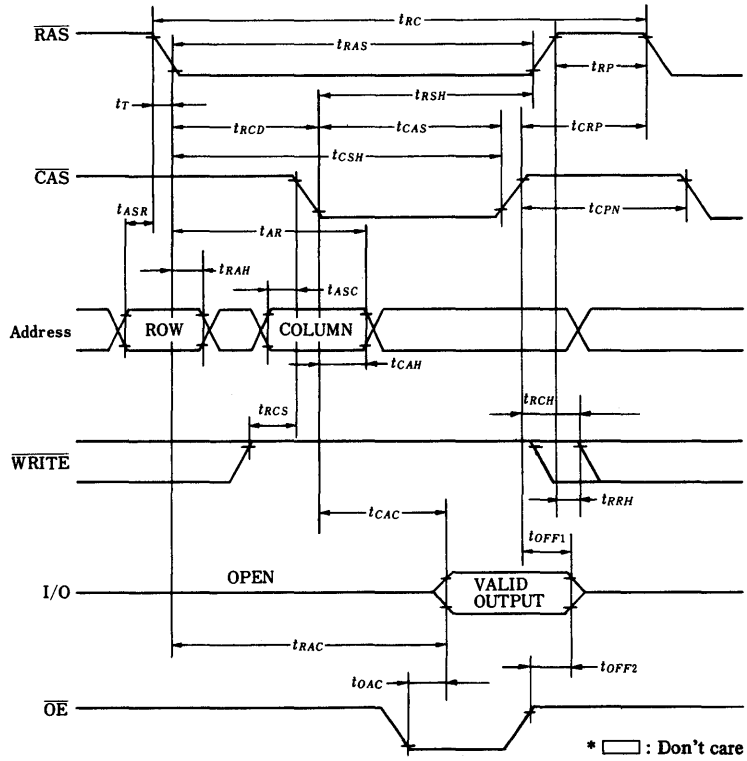
Parameter	Symbol	HM48416AP-12		HM48416AP-15		HM48416AP-20		Unit	Note
		min	max	min	max	min	max		
Write Command Hold Time refferenced to $\overline{RAS}$	t_{WCR}	100	–	120	–	155	–	ns	
Write Command Pulse Width	t_{WP}	40	–	45	–	55	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	40	–	45	–	55	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	40	–	45	–	55	–	ns	
Data-in Set-up Time	t_{DS}	0	–	0	–	0	–	ns	9
Data-in Hold Time	t_{DH}	40	–	45	–	55	–	ns	9
Data-in Hold Time refferenced to $\overline{RAS}$	t_{DHR}	100	–	120	–	155	–	ns	
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time refferenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	
Read Command Hold Time refferenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Refresh Period	t_{REF}	–	2	–	2	–	2	ms	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	105	–	125	–	160	–	ns	8
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	165	–	200	–	260	–	ns	8
$\overline{CAS}$ Precharge Time (for Page-mode Cycle Only)	t_{CP}	60	–	60	–	80	–	ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	35	–	40	–	50	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	–	0	–	0	–	ns	
Access Time from $\overline{OE}$	t_{OAC}	–	35	–	40	–	50	ns	3
Output Buffer Turn-off Delay refferenced to $\overline{OE}$	t_{OFF2}	–	35	–	40	–	50	ns	5
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	35	–	40	–	50	–	ns	11

Notes:

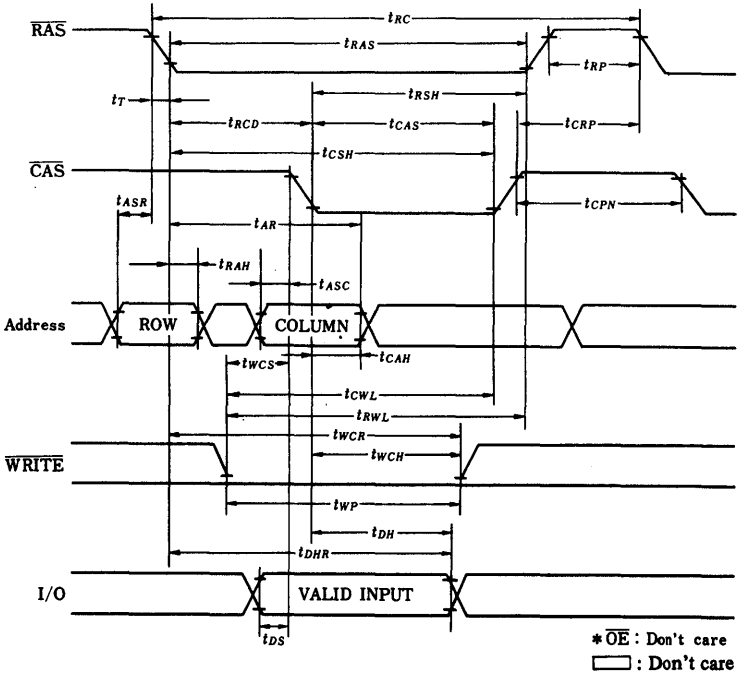
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. t_{OFF1} (max) and t_{OFF2} (max) define the time at which the output achieves the open circuit condition.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC}(max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min) the cycle is a read-write cycle and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100μs is required after power-up followed by a minimum of 8 initialization cycles.
11. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffers prior to applying data to the device.

■ TIMING WAVEFORMS

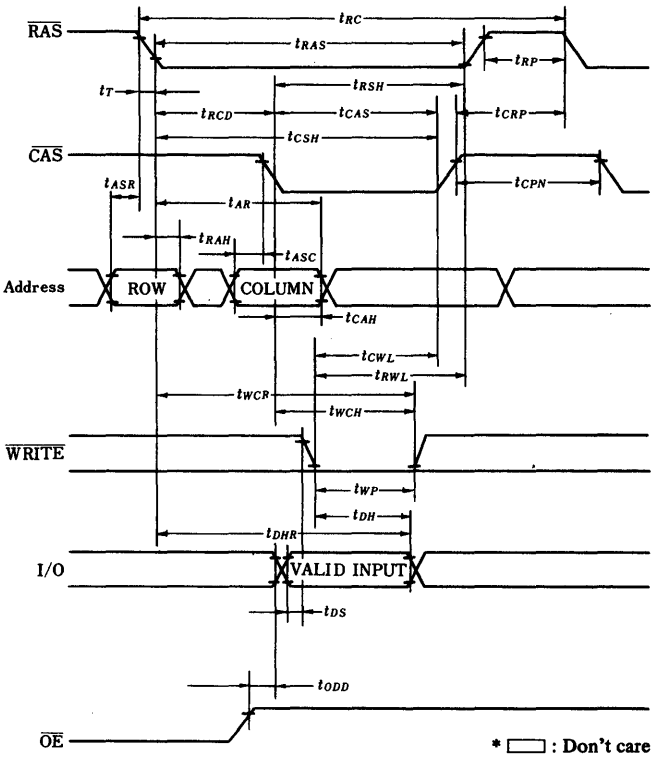
● Read Cycle



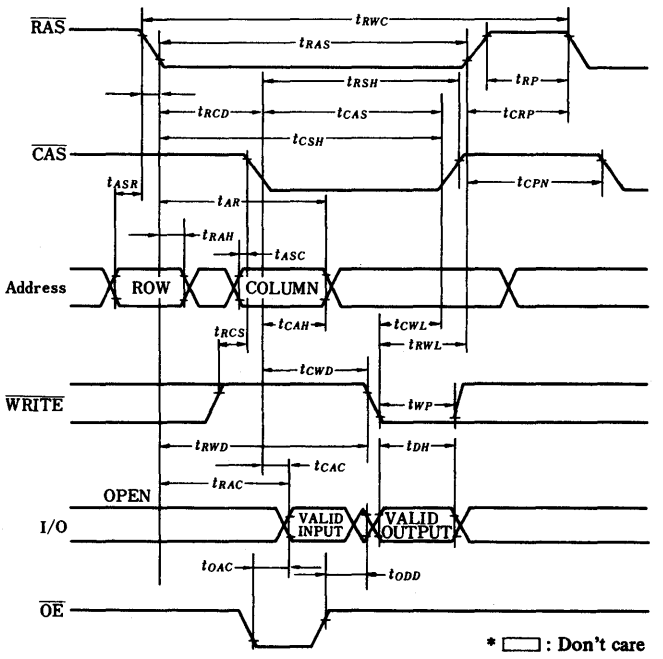
● Early Write Cycle



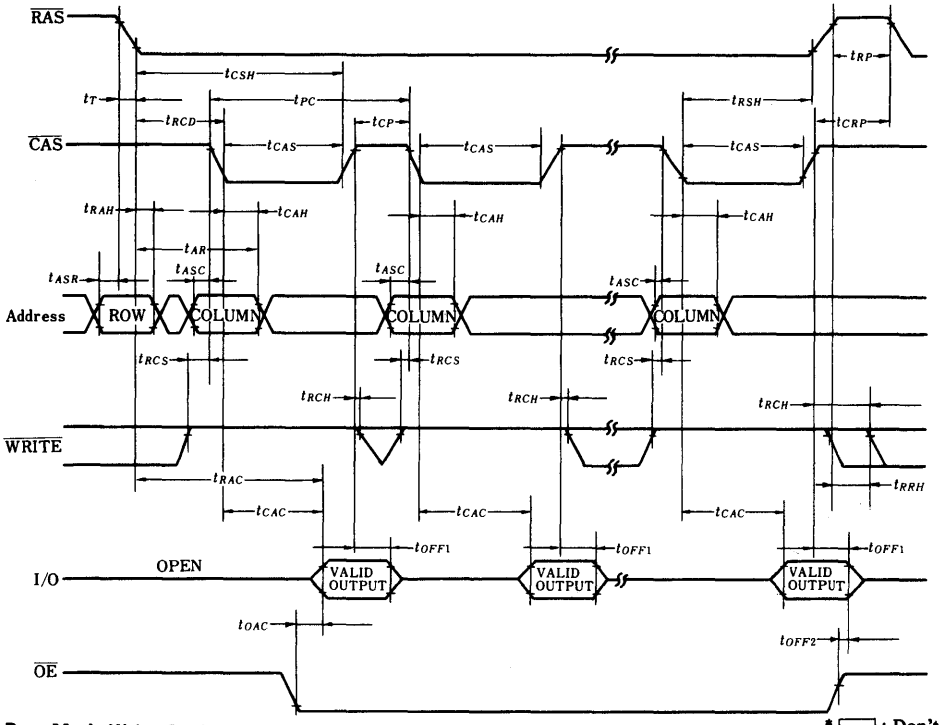
- **Delayed Write Cycle**



- **Read Modify Write Cycle**

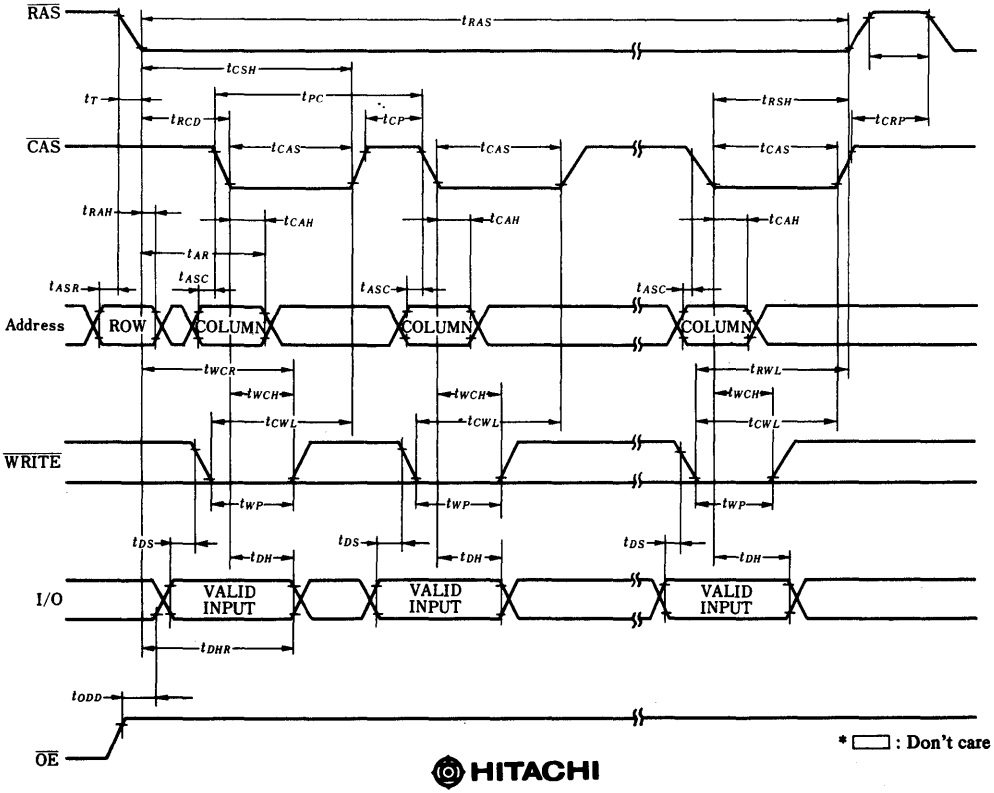


- **Page Mode Read Cycle**



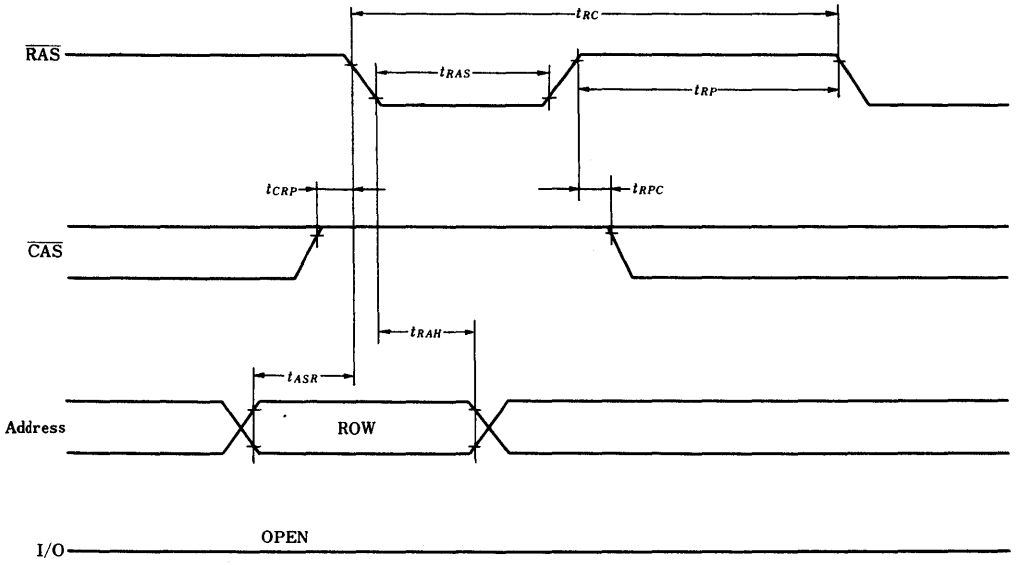
* ☐ : Don't care

- **Page Mode Write Cycle**



* ☐ : Don't care

- **$\overline{RAS}$ Only Refresh Cycle**



*$\overline{OE}$, $\overline{WE}$: Don't care
□ : Don't care

HM4864-2, HM4864-3
HM4864P-2, HM4864P-3

65536-word × 1-bit Dynamic Random Access Memory

The HM4864 is a 65,536-words by 1-bit, MOS random access memory circuit fabricated with HITACHI's double-poly N-channel silicon gate process for high performance and high functional density. The HM4864 uses a single transistor dynamic storage cell and dynamic control circuitry to achieve high speed and low power dissipation.

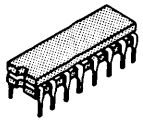
Multiplexed address inputs permit the HM4864 to be packaged in a standard 16 pin DIP on 0.3 inch centers.

This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of +5V with ±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs, on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of this memory system. The HM4864 also incorporates several flexible timing/operating modes.

In addition to the usual read,write, and read-modify-write cycles, the HM4864 is capable of delayed write cycles, page-mode operation and $\overline{RAS}$-only refresh.

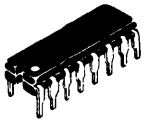
Proper control of the clock inputs ($\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

HM4864-2, HM4864-3



(DG-16A)

HM4864P-2, HM4864P-3

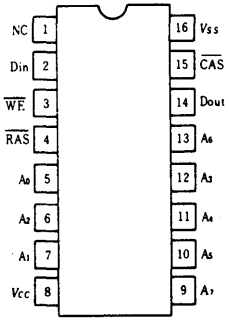


(DP-16)

■ FEATURES

- Recognized industry standard 16-pin configuration
- 150ns access time, 270ns cycle time (HM4864-2, HM4864P-2)
- 200ns access time, 335ns cycle time (HM4864-3, HM4864P-3)
- Single power supply of +5V±10% with a built-in V_{BB} generator
- Low Power; 330 mW active. 20 mW standby (max)
- The inputs TTL compatible, low capacitance, and protected against static charge
- Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-mode capability
- 128 refresh cycle

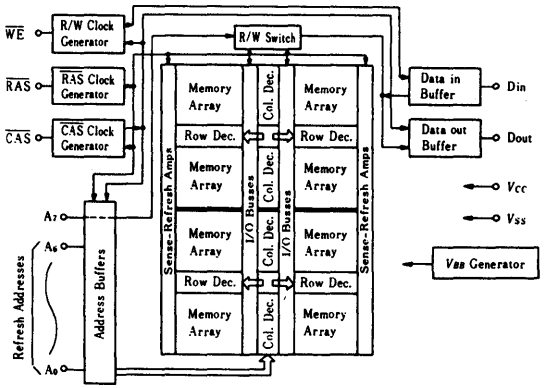
■ PIN ARRANGEMENT



(Top View)

A_0-A_7	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
A_0-A_6	Refresh Address Input

■ FUNCTIONAL BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . -1.0 to +7V
Operating Temperature, Ta (Ambient) . . . . . 0 to +70°C
Storage Temperature (Ambient) . . . . . -65 to +150°C (Cerdip)
-55 to +125°C (Plastic)
Short-circuit Output Current . 50 mA
Power Dissipation . . . . . 1 W

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

■ DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	min	max	Unit	Notes
OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling; t_{RC}=min.)	I_{CC1}	—	60	mA	2, 4
STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = V_{IH}, Dout = High Impedance)	I_{CC2}	—	3.5	mA	2
REFRESH CURRENT Average Power Supply Current, Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}; t_{RC}=min.)	I_{CC3}	—	45	mA	2, 4
PAGE MODE CURRENT Average Power Supply Current, Page-mode Operation ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling; t_{PC}=min.)	I_{CC4}	—	45	mA	2, 4
INPUT LEAKAGE Input Leakage Current, any Input (V_{in}=0 to +6.5V, all other pins not under test=0V)	I_{LI}	−10	10	μA	
OUTPUT LEAKAGE Output Leakage Current (Dout is disabled, V_{out}=0 to +5.5V)	I_{LO}	−10	10	μA	3
OUTPUT LEVELS Output High (Logic 1) Voltage (I_{out}=−5mA) Output Low (Logic 0) Voltage (I_{out}=4.2mA)	V_{OH} V_{OL}	2.4 0	V_{CC} 0.4	V V	

NOTES
1. All voltages referenced to V_{SS}.
2. I_{CC} depends on output loading condition when the device is selected. I_{CC} max. is specified at the output open condition.
3. I_{LO} consists of leakage current only.
4. Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

■ AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	typ	max	Unit	Notes
Input Capacitance (A_0-A_7, Din)	C_{in1}	—	7	pF	1
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{in2}	—	10	pF	1
Output Capacitance (Dout)	C_{out}	—	7	pF	1, 2

NOTES
1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS [1], [2]

(Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

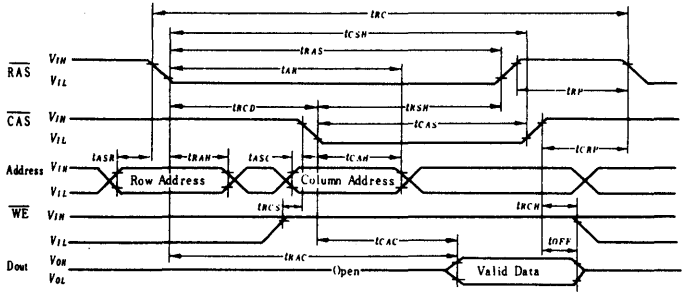
Parameter	Symbol	HM4864-2/P-2		HM4864-3/P-3		Unit	Notes
		min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	270	—	335	—	ns	
Read-Write Cycle Time	t_{RWC}	270	—	335	—	ns	
Page Mode Cycle Time	t_{PC}	170	—	225	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	150	—	200	ns	4, 6
Access Time from $\overline{CAS}$	t_{CAC}	—	100	—	135	ns	5, 6
Output Buffer Turn-off Delay	t_{OFF}	0	40	0	50	ns	7
Transition Time (Rise and Fall)	t_T	3	35	3	50	ns	3
$\overline{RAS}$ Precharge Time	t_{RP}	100	—	120	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	150	10000	200	10000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	100	—	135	—	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	100	—	135	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	150	—	200	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	25	65	ns	8
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	−20	—	−20	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	20	—	25	—	ns	
Column Address Set-up Time	t_{ASC}	−10	—	−10	—	ns	
Column Address Hold Time	t_{CAH}	45	—	55	—	ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	95	—	120	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	ns	
Write Command Hold Time	t_{WCH}	45	—	55	—	ns	
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	95	—	120	—	ns	
Write Command Pulse Width	t_{WP}	45	—	55	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	45	—	55	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	45	—	55	—	ns	9
Data-in Hold Time referenced to $\overline{RAS}$	t_{DHR}	95	—	120	—	ns	
$\overline{CAS}$ Precharge Time (for Page-mode Cycle Only)	t_{CP}	60	—	80	—	ns	
Refresh Period	t_{REF}	—	2	—	2	ms	
Write Command Set-up Time	t_{WCS}	−20	—	−20	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	60	—	80	—	ns	10
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	110	—	145	—	ns	10
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	—	0	—	ns	

NOTES

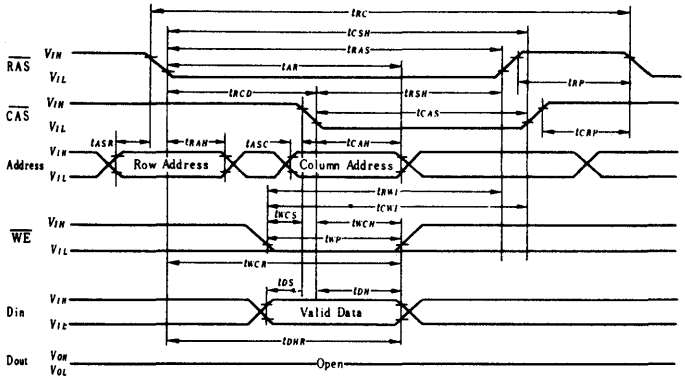
1. AC measurements assume t_T = 5ns.
2. 8 cycles are required after power-on or prolonged periods (greater than 2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table t_{RAC} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively be t_{CAC}.
9. These parameters are reference to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min) the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

■ TIMING WAVEFORMS

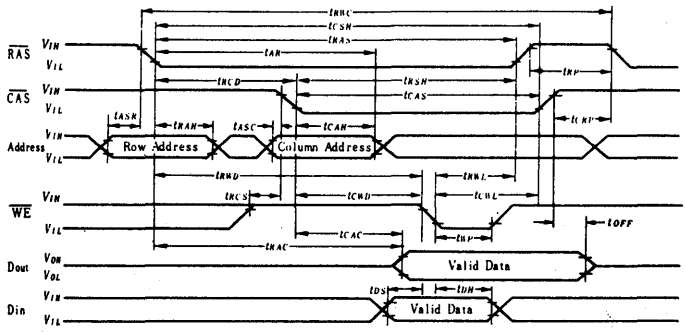
● READ CYCLE



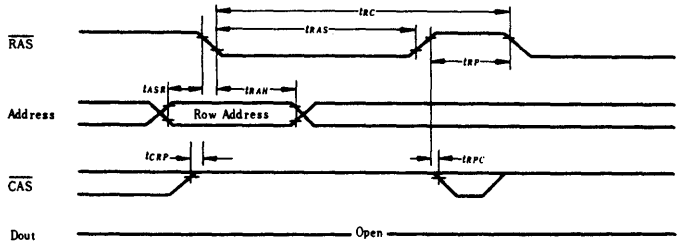
● WRITE CYCLE



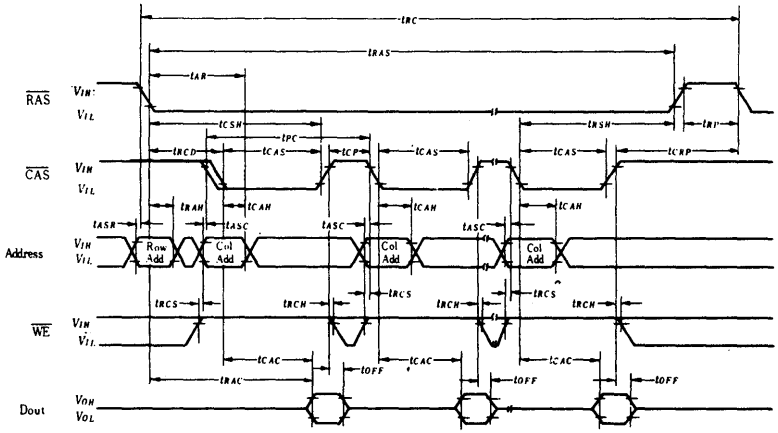
● READ-WRITE/READ-MODIFY-WRITE CYCLE



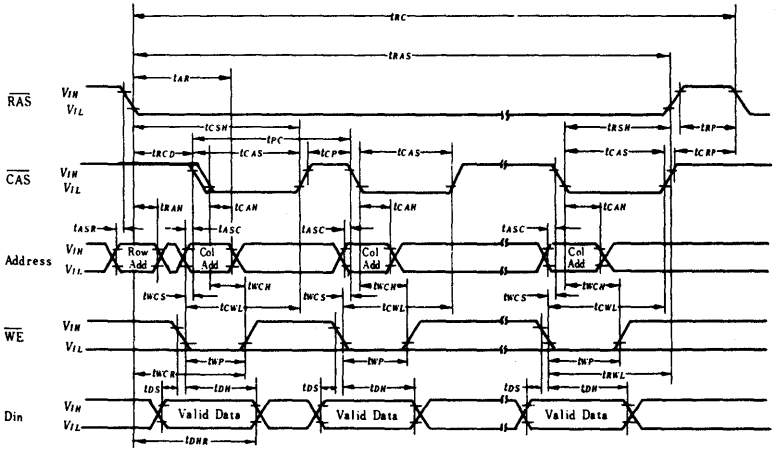
●"$\overline{RAS}$-ONLY" REFRESH CYCLE



●PAGE MODE READ CYCLE

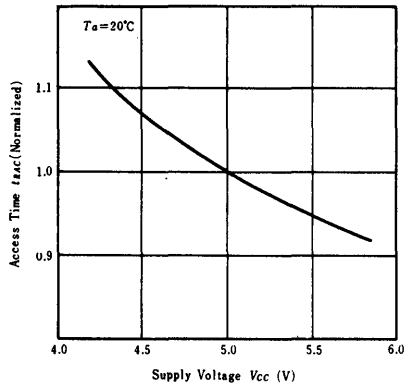


●PAGE MODE WRITE CYCLE

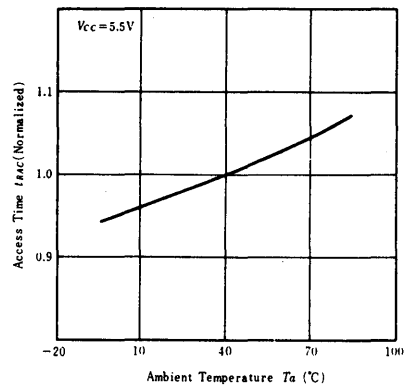


■ TYPICAL CHARACTERISTICS

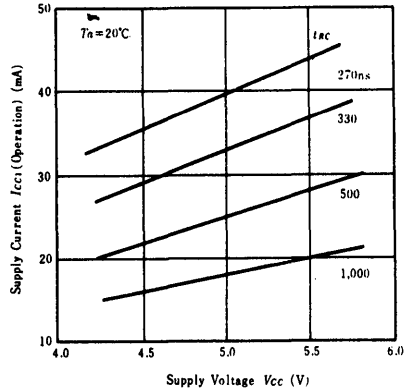
ACCESS TIME vs. SUPPLY VOLTAGE



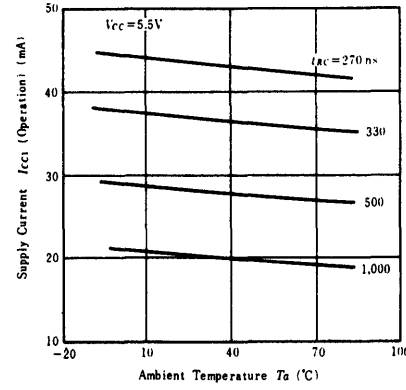
ACCESS TIME vs. AMBIENT TEMPERATURE



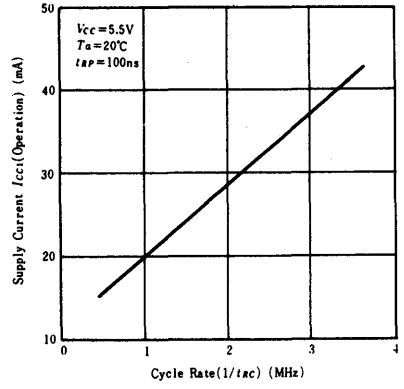
SUPPLY CURRENT vs. SUPPLY VOLTAGE



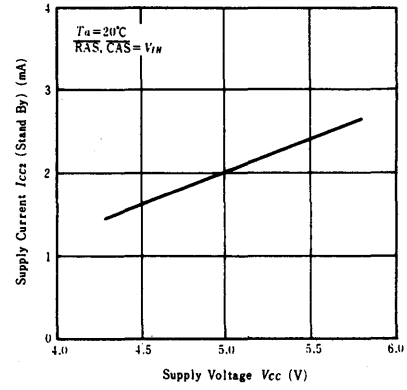
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



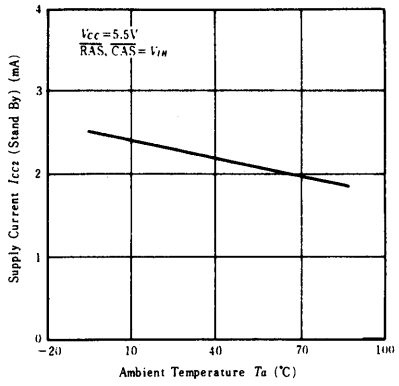
SUPPLY CURRENT vs. CYCLE RATE



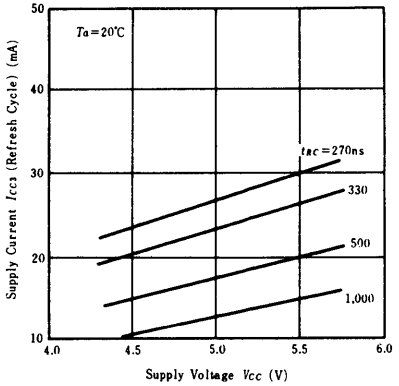
SUPPLY CURRENT vs. SUPPLY VOLTAGE



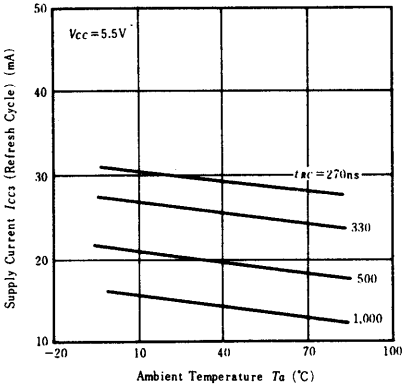
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



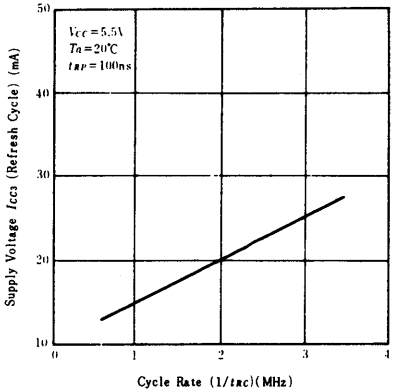
SUPPLY CURRENT vs. SUPPLY VOLTAGE



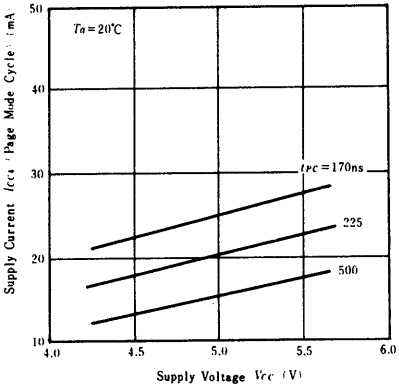
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



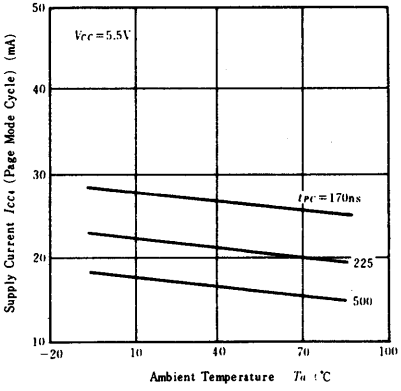
SUPPLY CURRENT vs. CYCLE RATE



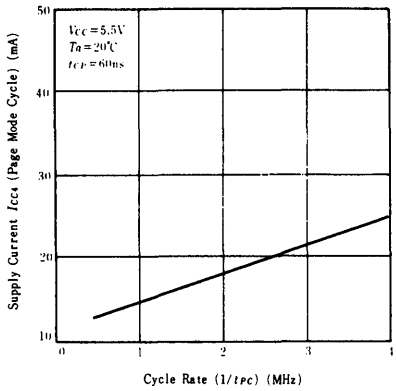
SUPPLY CURRENT vs. SUPPLY VOLTAGE



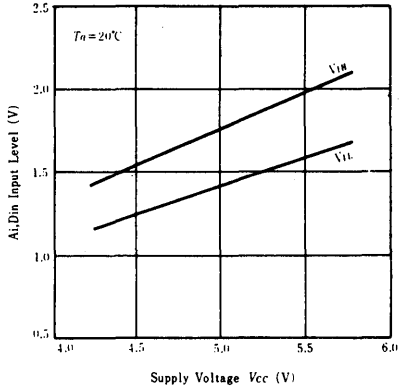
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



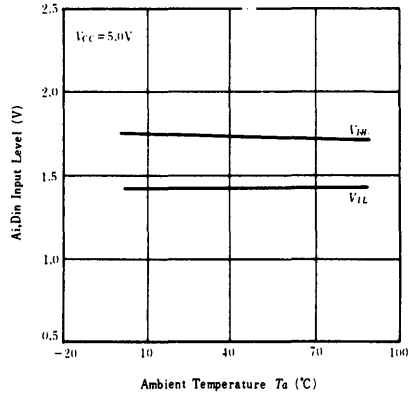
SUPPLY CURRENT vs. CYCLE RATE



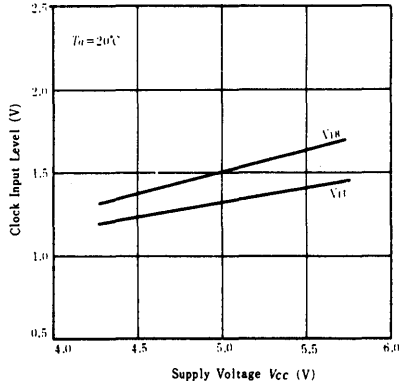
INPUT LEVEL vs. SUPPLY VOLTAGE



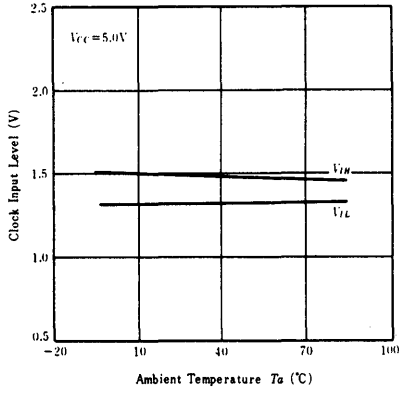
INPUT LEVEL vs. AMBIENT TEMPERATURE

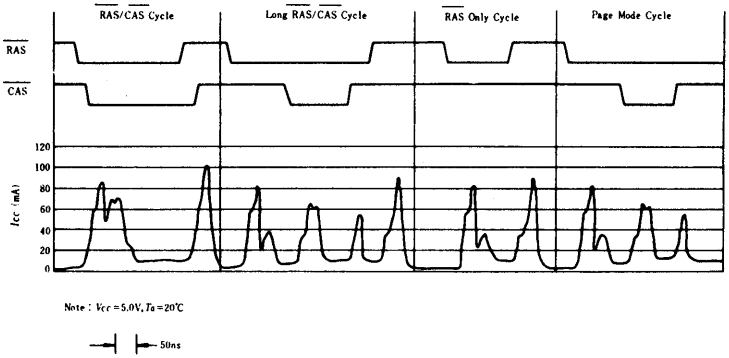


CLOCK INPUT LEVEL vs. SUPPLY VOLTAGE



CLOCK INPUT LEVEL vs. AMBIENT TEMPERATURE



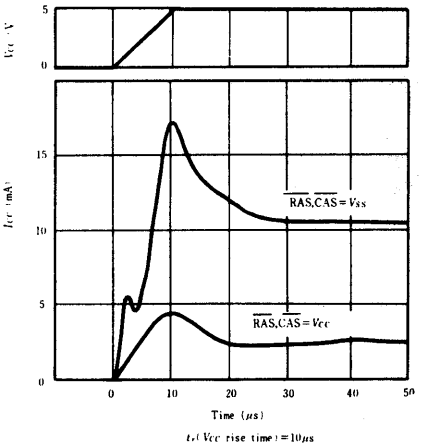


■APPLICATION INFORMATION

●POWER ON

An initial pause of 500 μs is required after power-up and a minimum of eight (8) initialization cycle,(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh) must follow an initial pause.

The V_{CC} current (I_{CC}) requirement of the HM4864 during power on is, however, dependent upon the input levels ($\overline{RAS}$, $\overline{CAS}$) and the rise time of V_{CC}, as shown in Fig. 1.



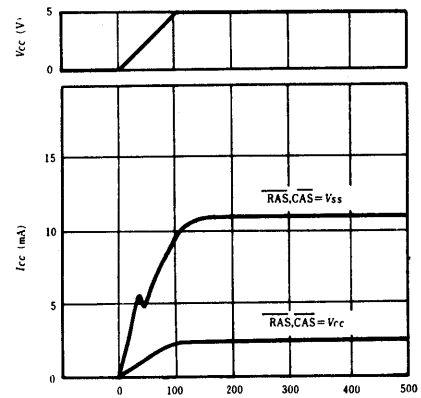


Fig.1 I_{CC} vs. V_{CC} during power up.

●READ CYCLE

A read cycle begins with addresses stable and a negative going transition of $\overline{RAS}$. The time delay between the stable address and the start of $\overline{RAS}$-on is controlled by parameter t_{ASR}.

Following the time when $\overline{RAS}$ reaches its low level, the row address must be held stable long enough to be captured. This controlling parameter is t_{RAH}. Following this interval, the address can be changed from row address to column address. When the column address is stable,$\overline{CAS}$ can be turned on. The leading edge of $\overline{CAS}$ is controlled by parameter t_{RCD}. The basic limit on the $\overline{CAS}$ leading edge is that $\overline{CAS}$ can not start until the column address is stable, and this is controlled by parameter t_{ASC}. The column address must be held stable long enough to be captured. The controlling parameter is t_{CAH}. Note that t_{RCD} (max) is not an operating limit of the HM4864 though its specification is listed on the data sheets. If $\overline{CAS}$ becomes on later than t_{RCD} (max), the access time from $\overline{RAS}$ will be increased by the time which t_{RCD} exceeds t_{RCD} (max).

Following the time when $\overline{CAS}$ reaches its low level, the data-out pin remains in a high impedance state until a valid data appears. This parameter is t_{CAC}-access time from $\overline{CAS}$.

The access time from $\overline{RAS}$–t_{RAC}–is the time from $\overline{RAS}$-on to valid Dout.

The minimum value of t_{RAC} is derived as the sum of t_{RCD} (max) and t_{CAC}.

The selected output data is held valid internally until $\overline{CAS}$ becomes high, and then Dout pin becomes high impedance. This parameter is t_{OFF}.

• WRITE CYCLE

A write cycle is performed by bringing $\overline{WE}$ low before or during $\overline{CAS}$-on.

Two different write cycles can be defined as;

Write cycle—Write data are available at the beginning of the $\overline{CAS}$-on so that the write operation starts at the beginning. In this mode, Dout and $\overline{WE}$ signal times are not in any critical path for determining cycle time.

Following the time when $\overline{WE}$ reaches its low level, $\overline{WE}$ must be held stable long enough to be captured. This $\overline{WE}$-on pulse deration is called t_{WP}. The time required to capture write data in a latch is called t_{DH}. This cycle is called an "early write".

Read Write cycle—This cycle starts as a read cycle, but as soon as the device specification is met, a write cycle is initiated.

$\overline{WE}$ and Din are delayed until after Dout. This cycle is called a "delayed write". A "Read-modify-write" cycle is a variation of this operation. In this mode, Din and $\overline{WE}$ become critical path signals for determining cycle time.

• CLOCK-OFF TIMING

$\overline{RAS}$ and $\overline{CAS}$ must stay on for Dout stabilized to valid data. In the case of $\overline{CAS}$, this is controlled by parameter t_{CAS} (min).

In the case of $\overline{RAS}$, this is controlled by parameter t_{CAS} (min). Following the end of $\overline{RAS}$, $\overline{CAS}$ must stay off long enough to precharge internal circuits. The only parameter of concern is t_{RP}. Normally $\overline{CAS}$ is not required to be off for minimum time of t_{CRP}. However, in a page mode memory operation, there is a t_{CP} (min) specification to control the $\overline{CAS}$-off time.

• DATA OUTPUT

Dout is three-state TTL compatible with a fan-out of two standard TTL loads.

When $\overline{CAS}$ is high, Dout is in a high impedance state. When $\overline{CAS}$ is low, valid data appears after t_{CAC} at a read cycle, and Dout is not valid as an early-write cycle.

• REFRESH

Refresh of the HM4864 is accomplished by performing a memory cycle at each of the 128 row addresses within each two millisecond time interval. A0 to A6 are refresh address pin compatible with standard 16K RAM (HM4716A, HM4816A). During refresh, either V_{IL} or V_{IH} is permitted for A7. Any cycle in which $\overline{RAS}$ signal occurs refreshes the entire selected row. $\overline{RAS}$-only refresh results in substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

• PAGE MODE

Page mode operation allows faster successive memory operations at multiple column locations of the same row address with increased speed.

This is done by strobing the row address into the chip and maintaining $\overline{RAS}$ at a logic low throughout all successive $\overline{CAS}$ memory cycles in which the row address is latched. As the time normally required for strobing a new row address is eliminated, access and cycle times can be descreaded and the operating power is reduced. These are specifications.

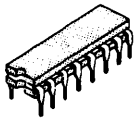
HM4864A-12, HM4864A-15, HM4864A-20, HM4864AP-12, HM4864AP-15, HM4864AP-20

65536-word × 1-bit Dynamic Random Access Memory

■ FEATURES

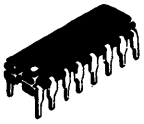
- Industry standard 16-Pin DIP (plastic, Cerdip)
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 250mW active, 18mW standby
- High speed: Access Time 120ns / 150ns / 200ns
- Common I/O capability using early write operation
- Page mode capability
- Output data controlled by $\overline{CAS}$
- TTL compatible
- 128 refresh cycles – (2ms)
- Hidden refresh capability

HM4864A-12, HM4864A-15, HM4864A-20



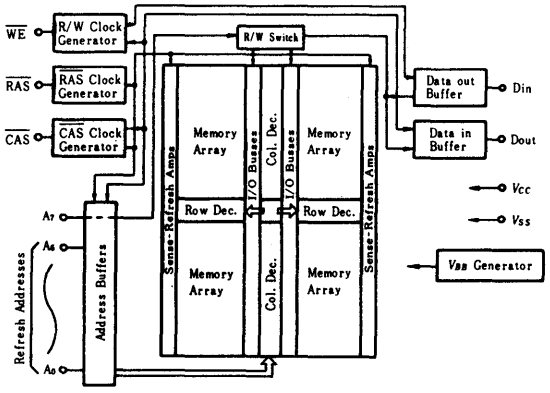
(DG-16B)

HM4864AP-12, HM4864AP-15, HM4864AP-20

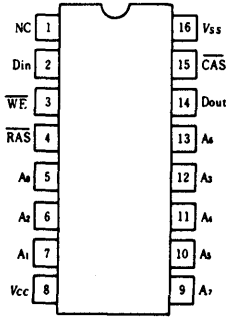


(DP-16)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS}	−1V to 7V
Operating temperature, Ta (Ambient)	0°C to 70°C
Storage temperature (Cerdip)	−65°C to 150°C
Storage temperature (Plastic)	−55°C to 125°C
Power dissipation	1 W
Short circuit output current	50 mA

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to 70°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Notes : 1. All voltages referenced to V_{SS}

A0–A7	:	Address Inputs
$\overline{CAS}$	:	Column Address Strobe
Din	:	Data In
Dout	:	Data Output
$\overline{RAS}$	:	Row Address Strobe
$\overline{WE}$	:	Read/Write Input
V_{CC}	:	Power (+5V)
V_{SS}	:	Ground
A0–A6	:	Refresh Address Inputs

■ DC ELECTRICAL CHARACTERISTICS (Ta=0 to 70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	HM4864A/P-12		HM4864A/P-15		HM4864A/P-20		Unit	Notes
		min	max	min	max	min	max		
Operating Current($\overline{RAS}$,$\overline{CAS}$ Cycling:t_{RC}=min)	I_{CC1}	—	55	—	50	—	44	mA	1,2
Standby Cnrrent($\overline{RAS}$=V_{IH},Dout=High Impedance)	I_{CC2}	—	3.5	—	3.5	—	3.5	mA	
Refresh Current($\overline{RAS}$ Cycling,$\overline{CAS}$=V_{IH},t_{RC}=min)	I_{CC3}	—	42	—	38	—	33	mA	2
Standby Current($\overline{RAS}$=V_{IH},Dout Enable)	I_{CC5}	—	5.5	—	5.5	—	5.5	mA	1
Page Mode Current($\overline{RAS}$=V_{IL},$\overline{CAS}$ Cycling;t_{PC}=min)	I_{CC6}	—	38	—	35	—	31	mA	1,2
Input Leakage(0<V_{out}<6.5V)	I_{LI}	−10	10	−10	10	−10	10	μA	
Output Leakage(Dout is disabled,0<V_{out}<5.5V)	I_{LO}	−10	10	−10	10	−10	10	μA	
Output Levels High(I_{out}=−5mA)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Levels Low(I_{out}=4.2mA)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Notes) 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max. is specified at the output open condition.
2. Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

■ CAPACITANCE (V_{CC}=5V±10%, Ta=25°C)

Parameter		Symbol	typ	max	Unit	Notes
Input Capacitance	A_0~A_7, Din	C_{in1}	—	5	pF	1
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{in2}	—	10	pF	1
Output Capacitance	Dout	C_{out}	—	7	pF	1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Ta=0 to 70°C, V_{CC}=5V±10%, V_{SS}=0V)

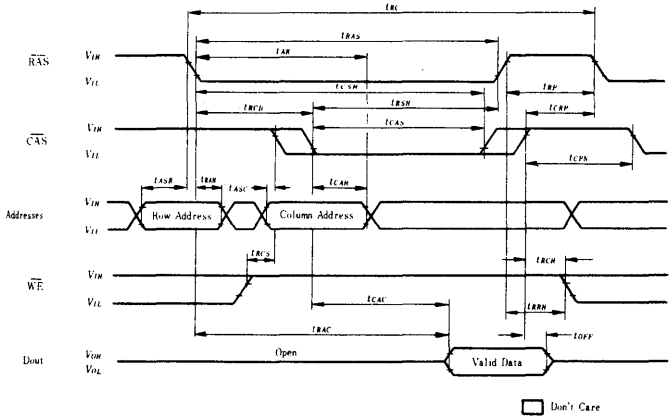
Parameter	Symbol	HM4864A-12		HM4864A-15		HM4864A-20		Unit	Notes
		min	max	min	max	min	max		
Access Time From $\overline{RAS}$	t_{RAC}	—	120	—	150	—	200	ns	2, 3
Access Time From $\overline{CAS}$	t_{CAC}	—	60	—	75	—	100	ns	3, 4
Output Buffer Turn-off Delay	t_{OFF}	—	35	—	40	—	50	ns	5
Transition Time (Rise and Fall)	t_T	3	35	3	35	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	220	—	260	—	330	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	90	—	100	—	120	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	60	—	75	—	100	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	120	—	150	—	200	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	−10	—	−10	—	−10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	25	—	30	—	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	80	—	100	—	130	—	ns	
$\overline{WE}$ Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	40	—	45	—	55	—	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	100	—	120	—	155	—	ns	
Write Command Pulse Width	t_{WP}	40	—	45	—	55	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	40	—	45	—	55	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	40	—	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	40	—	45	—	55	—	ns	9
Data-in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	100	—	120	—	155	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	2	—	2	—	2	ms	
Read-Write Cycle Time	t_{RWC}	245	—	280	—	345	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	40	—	45	—	55	—	ns	8
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	100	—	120	—	155	—	ns	
Page Mode Cycle Time	t_{PC}	120	—	145	—	190	—	ns	
$\overline{CAS}$ Precharge Time (for Page-mode Cycle Only)	t_{CP}	50	—	60	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	30	—	35	—	45	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	—	0	—	0	—	ns	

Notes

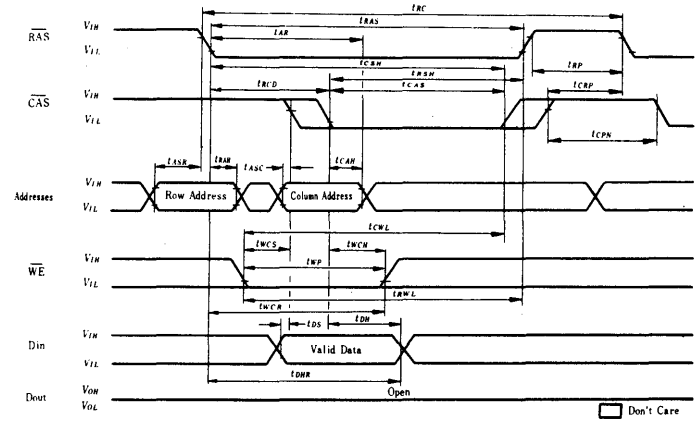
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters.
   They are included in the data sheet is electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min) the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. There parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge is delayed write or read-modify-write cycles.
10. An initial pause of 100μs is required after power-up followed by a minimum of 8 initialization cycles.

■ TIMING WAVEFORMS

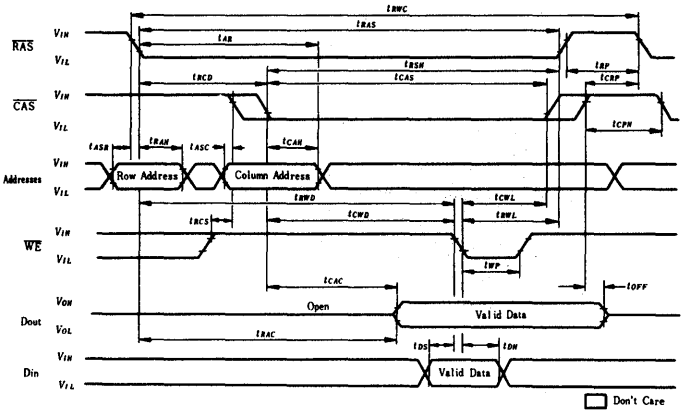
● READ CYCLE



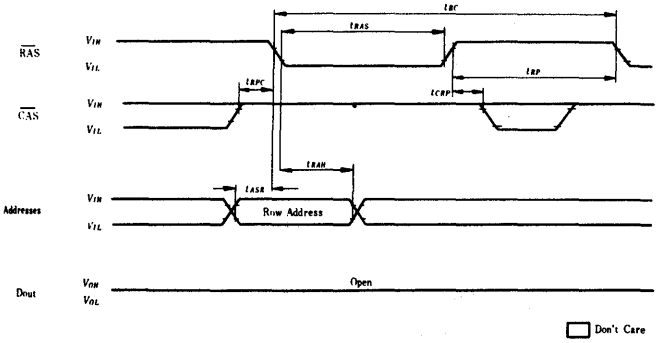
● WRITE CYCLE (EARLY WRITE)



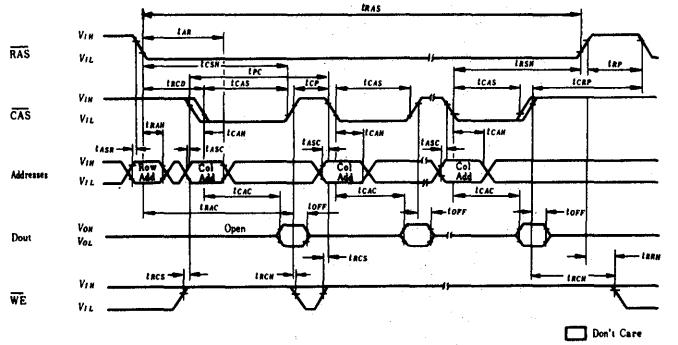
●READ-WRITE/READ-MODIFY-WRITE CYCLE



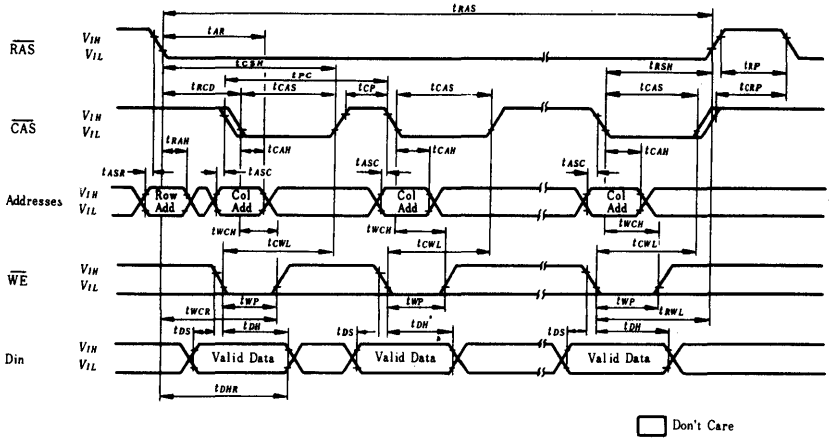
●"RAS-ONLY" REFRESH CYCLE



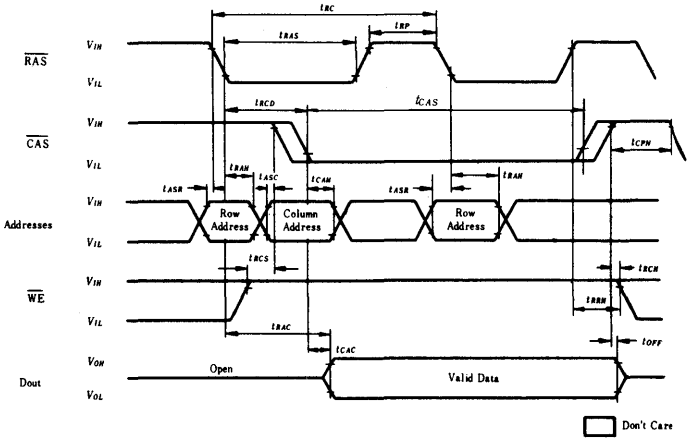
●PAGE MODE READ CYCLE



●PAGE MODE WRITE CYCLE



●HIDDEN REFRESH CYCLE

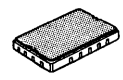


HM4864ACG-12, HM4864ACG-15, HM4864ACG-20

65536-word × 1-bit Dynamic Random Access Memory

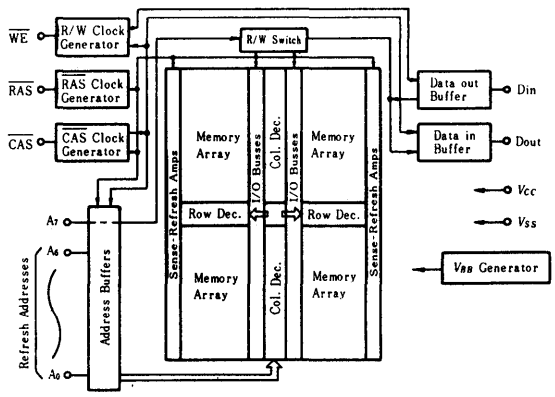
■ FEATURES

- 18-pin Leadless Chip Carrier
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 250mW active, 18mW standby
- High speed: Access Time 120/150/200ns (max)
- Common I/O capability using early write operation
- Page mode capability
- Output data controlled by $\overline{CAS}$
- TTL compatible
- 128 refresh cycles/2ms
- Hidden refresh capability

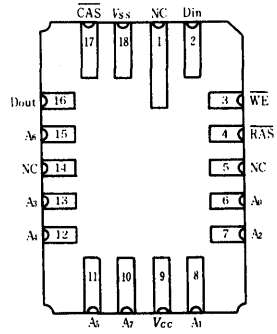


(CG-18)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Bottom View)

A0–A7	:	Address Inputs
$\overline{CAS}$	:	Column Address Strobe
Din	:	Data In
Dout	:	Data Output
$\overline{RAS}$	:	Row Address Strobe
$\overline{WE}$	:	Read/Write Input
V_{CC}	:	Power (+5V)
V_{SS}	:	Ground
A0–A6	:	Refresh Address Inputs

■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS}	−1V to +7V
Operating temperature, Ta (Ambient)	0°C to +70°C
Storage temperature	−65°C to +150°C
Power Dissipation	1W
Short circuit output current	50mA

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to 70°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Notes : 1. All voltages referenced to V_{SS}

■ DC ELECTRICAL CHARACTERISTICS (Ta=0 to 70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	HM4864ACG-12		HM4864ACG-15		HM4864ACG-20		Unit	Notes
		min	max	min	max	min	max		
Operating Current($\overline{RAS}$,$\overline{CAS}$ Cycling:t_{RC}=min)	I_{CC1}	—	55	—	50	—	44	mA	1,2
Standby Cnrrent($\overline{RAS}$=V_{IH},Dout=High Impedance)	I_{CC2}	—	3.5	—	3.5	—	3.5	mA	
Refresh Current($\overline{RAS}$ Cycling,$\overline{CAS}$=V_{IH},t_{RC}=min)	I_{CC3}	—	42	—	38	—	33	mA	2
Standby Current($\overline{RAS}$=V_{IH},Dout Enable)	I_{CC5}	—	5.5	—	5.5	—	5.5	mA	1
Page Mode Current($\overline{RAS}$=V_{IL},$\overline{CAS}$ Cycling;t_{PC}=min)	I_{CC6}	—	38	—	35	—	31	mA	1,2
Input Leakage(0<V_{in}<6.5V)	I_{LI}	−10	10	−10	10	−10	10	μA	
Output Leakage(Dout is disabled,0<V_{out}<5.5V)	I_{LO}	−10	10	−10	10	−10	10	μA	
Output Levels High(I_{out}=−5mA)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Levels Low(I_{out}=4.2mA)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Notes) 1. I_{CC} depends on output loading condition when the device is selected, I_{O} max. is specified at the output open condition.
2. Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

■ CAPACITANCE (V_{CC}=5V±10%, Ta=25°C)

Item		Symbol	typ	max	Unit	Notes
Input Capacitance	A_0~A_7, Din	C_{in1}	—	5	pF	1
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{in2}	—	10	pF	1
Output Capacitance	Dout	C_{out}	—	7	pF	1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Ta=0 to 70°C, V_{CC}=5V±10%, V_{SS}=0V)

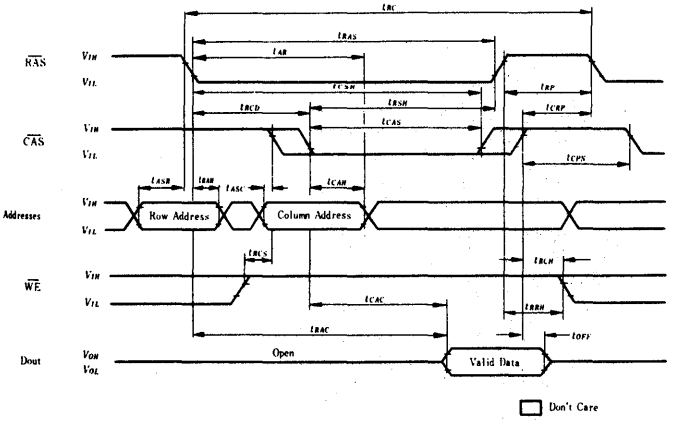
Parameter	Symbol	HM4864ACG-12		HM4864ACG-15		HM4864ACG-20		Unit	Notes
		min	max	min	max	min	max		
Access Time From $\overline{RAS}$	t_{RAC}	—	120	—	150	—	200	ns	2,3
Access Time From $\overline{CAS}$	t_{CAC}	—	60	—	75	—	100	ns	3,4
Output Buffer Turn-off Delay	t_{OFF}	—	35	—	40	—	50	ns	5
Transition Time (Rise and Fall)	t_T	3	35	3	35	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	220	—	260	—	330	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	90	—	100	—	120	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	60	—	75	—	100	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	120	—	150	—	200	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	−10	—	−10	—	−10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	25	—	30	—	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	80	—	100	—	130	—	ns	
$\overline{WE}$ Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	40	—	45	—	55	—	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	100	—	120	—	155	—	ns	
Write Command Pulse Width	t_{WP}	40	—	45	—	55	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	40	—	45	—	55	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	40	—	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	40	—	45	—	55	—	ns	9
Data-in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	100	—	120	—	155	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	2	—	2	—	2	ms	
Read-Write Cycle Time	t_{RWC}	245	—	280	—	345	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	40	—	45	—	55	—	ns	8
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	100	—	120	—	155	—	ns	
Page Mode Cycle Time	t_{PC}	120	—	145	—	190	—	ns	
$\overline{CAS}$ Precharge Time (for Page-mode Cycle Only)	t_{CP}	50	—	60	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	30	—	35	—	45	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	—	0	—	0	—	ns	

Notes

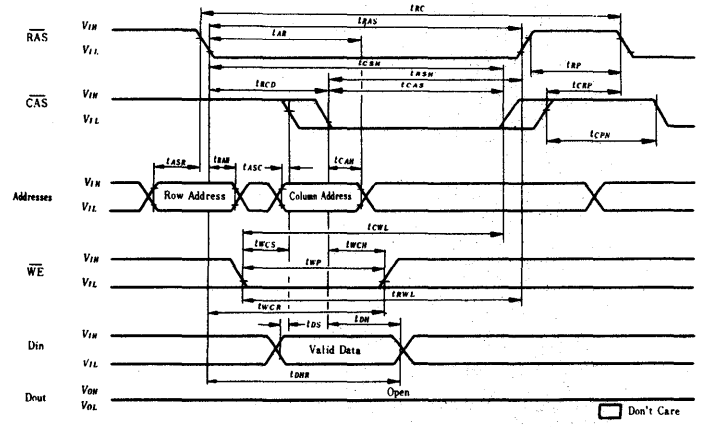
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters.
   They are included in the data sheet is electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min) the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. There parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge is delayed write or read-modify-write cycles.
10. An initial pause of 100μs is required after power-up followed by a minimum of 8 initialization cycles.

■ TIMING WAVEFORMS

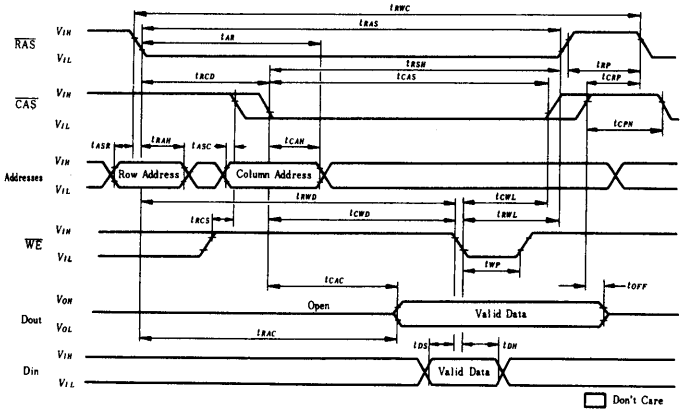
● READ CYCLE



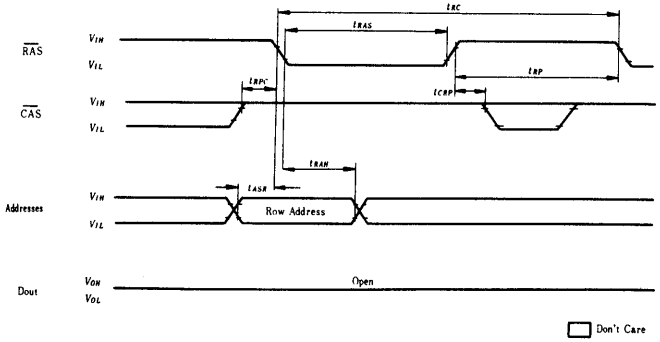
● WRITE CYCLE (EARLY WRITE)



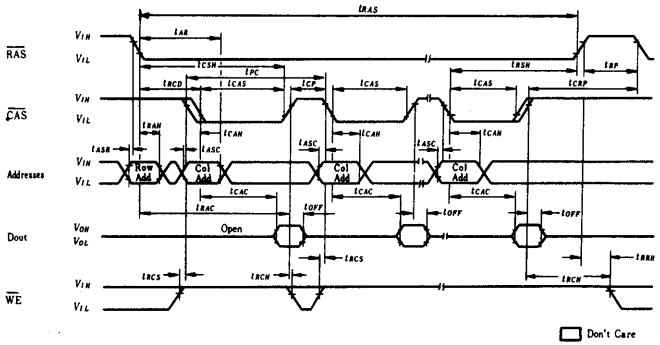
●READ-WRITE/READ-MODIFY-WRITE CYCLE



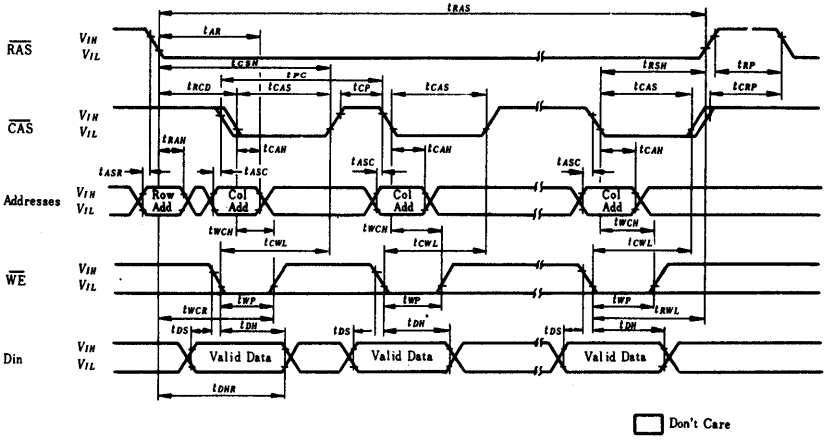
●"RAS-ONLY" REFRESH CYCLE



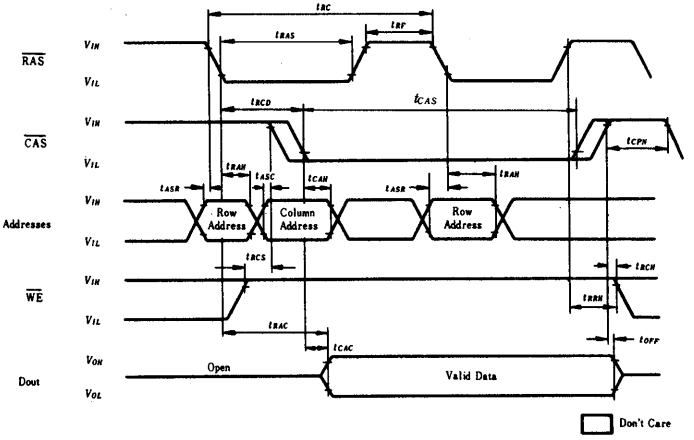
●PAGE MODE READ CYCLE



●PAGE MODE WRITE CYCLE



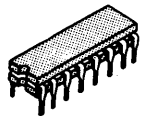
●HIDDEN REFRESH CYCLE



HM50256-12,HM50256-15, HM50256-20,HM50256P-12, HM50256P-15,HM50256P-20

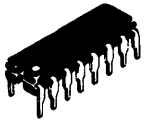
262144-word × 1-bit Dynamic Random Access Memory

HM50256 Series



(DG-16B)

HM50256P Series

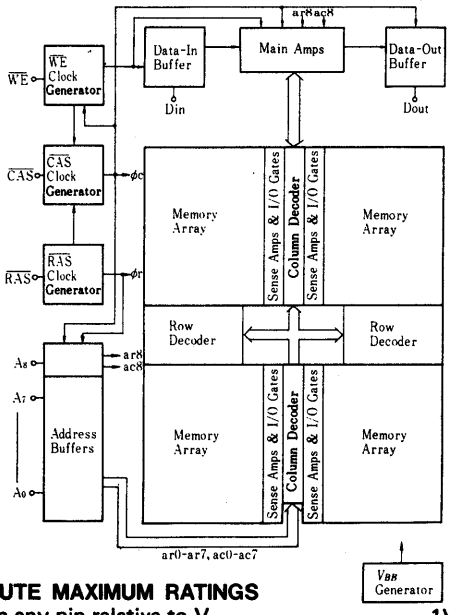


(DP-16A)

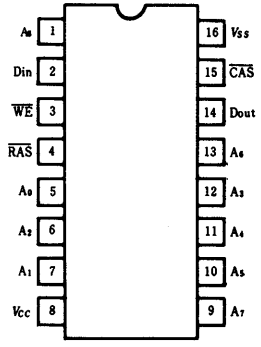
■FEATURES

- Industry Standard 16-Pin DIP
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 350mW active, 20mW standby
- High speed: Access Time 120ns/150ns/200ns(max.)
- Common I/O capability using early write operation
- Page mode capability
- TTL compatible
- 256 refresh cycles · · · (4ms)
- 3 variations of refresh · · · $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

A_0~A_8	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
A_0~A_7	Refresh Address Inputs

■ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . −1V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature . . . . . (Cerdip) −65°C to +150°C
(Plastic DIP) −55°C to +125°C
Power dissipation 1W
Short circuit output current 50mA

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note) 1. All voltages referenced to V_{SS}

■DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	HM50256/P-12		HM50256/P-15		HM50256/P-20		Unit	Notes
		min	max	min	max	min	max		
Operating Current($\overline{RAS}$, $\overline{CAS}$ Cycling : t_{RC}=min)	I_{CC1}	—	83	—	70	—	55	mA	1
Standby Current($\overline{RAS}$=V_{IH}, Dout=High Impedance)	I_{CC2}	—	4.5	—	4.5	—	4.5	mA	
Refresh Current($\overline{RAS}$ only Refresh, t_{RC}=min)	I_{CC3}	—	62	—	53	—	42	mA	
Standby Current($\overline{RAS}$=V_{IH}, Dout Enable)	I_{CC5}	—	10	—	10	—	10	mA	1
Refresh Current($\overline{CAS}$ before $\overline{RAS}$ Refresh, t_{RC}=min)	I_{CC6}	—	69	—	58	—	45	mA	
Input leakage(0< V_{out}<7V)	I_{LI}	−10	10	−10	10	−10	10	μA	
Output leakage(0< V_{out}<7V)	I_{LO}	−10	10	−10	10	−10	10	μA	
Output levels High(I_{out}=−5mA)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output levels Low(I_{out}=4.2mA)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Notes) 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.

■CAPACITANCE (V_{CC}=5V±10%, Ta=25°C)

Parameter		Symbol	typ	max	Unit	Notes
Input Capacitance	Address, Data-in	C_{I1}	—	5	pF	1
	Clocks, Data-out	C_{I2}	—	7		1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable Dout.

■ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V) [1), 10), 11)]

Parameter	Symbol	HM50256/P-12		HM50256/P-15		HM50256/P-20		Unit	Notes
		min	max	min	max	min	max		
Access Time from $\overline{RAS}$	t_{RAC}	—	120	—	150	—	200	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	60	—	75	—	100	ns	3, 4
Output Buffer Turn-off Delay	t_{OFF}	—	30	—	40	—	50	ns	5
Transition Time(Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	220	—	260	—	330	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	90	—	100	—	120	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	60	—	75	—	100	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	120	—	150	—	200	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	25	—	30	—	ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	80	—	100	—	130	—	ns	
$\overline{WE}$ Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	40	—	45	—	55	—	ns	
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	100	—	120	—	155	—	ns	
Write Command Pulse Width	t_{WP}	40	—	45	—	55	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	40	—	45	—	55	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	40	—	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	40	—	45	—	55	—	ns	8, 9
Data-in Hold Time referenced to $\overline{RAS}$	t_{DHR}	100	—	120	—	155	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	

(to be continued)

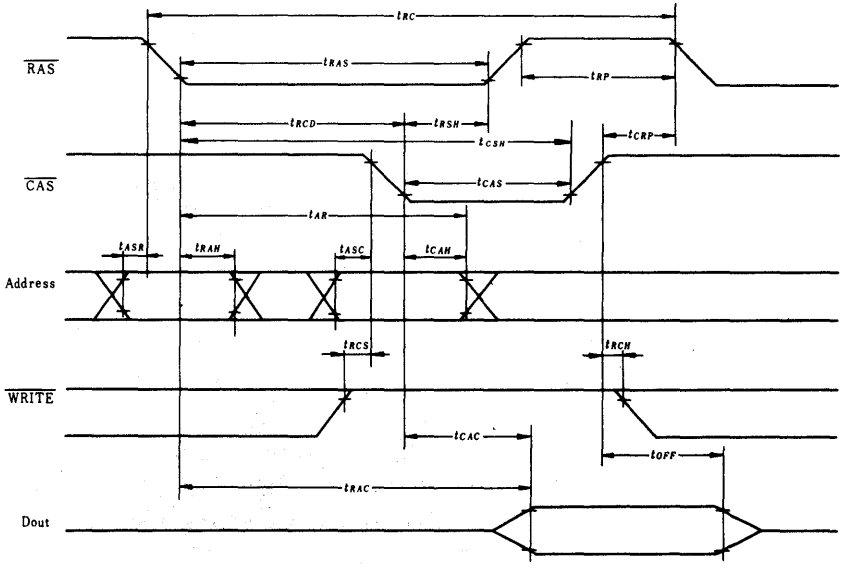
Parameter	Symbol	HM50256/P-12		HM50256/P-15		HM50256/P-20		Unit	Notes
		min	max	min	max	min	max		
Read-Write Cycle Time	t_{RWC}	265	—	310	—	390	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	60	—	75	—	100	—	ns	8
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	120	—	150	—	200	—	ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	50	—	60	—	80	—	ns	
$\overline{CAS}$ Setup Time	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	120	—	150	—	200	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	—	0	—	0	—	ns	

Notes

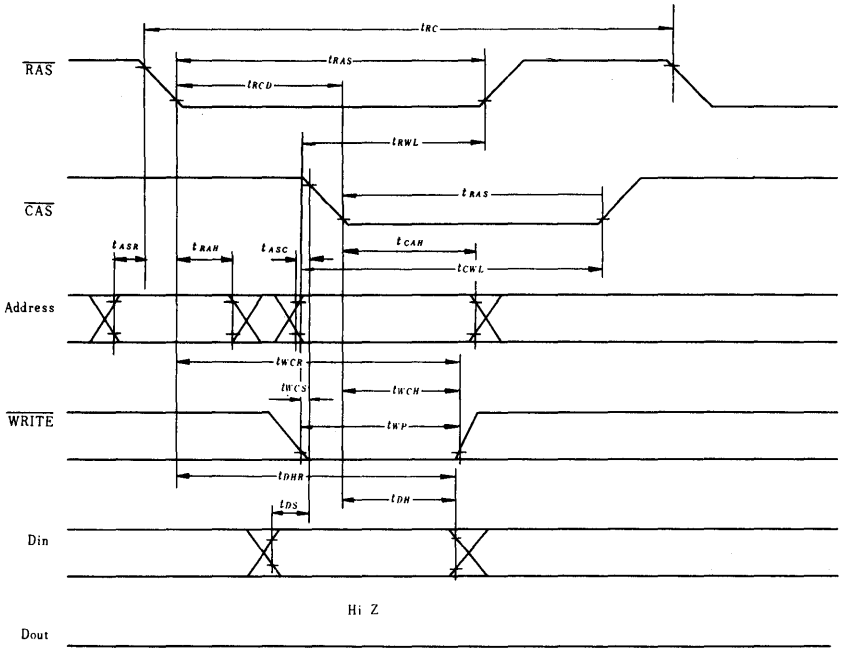
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and output voltage levels are not referred.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters.
   They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100μs is required after power-up then execute at least 8 initialization cycles.
11. At least, 8 $\overline{CAS}$ before $\overline{RAS}$ refesh cycle are required before using internal refresh counter.

■ TIMING WAVEFORMS

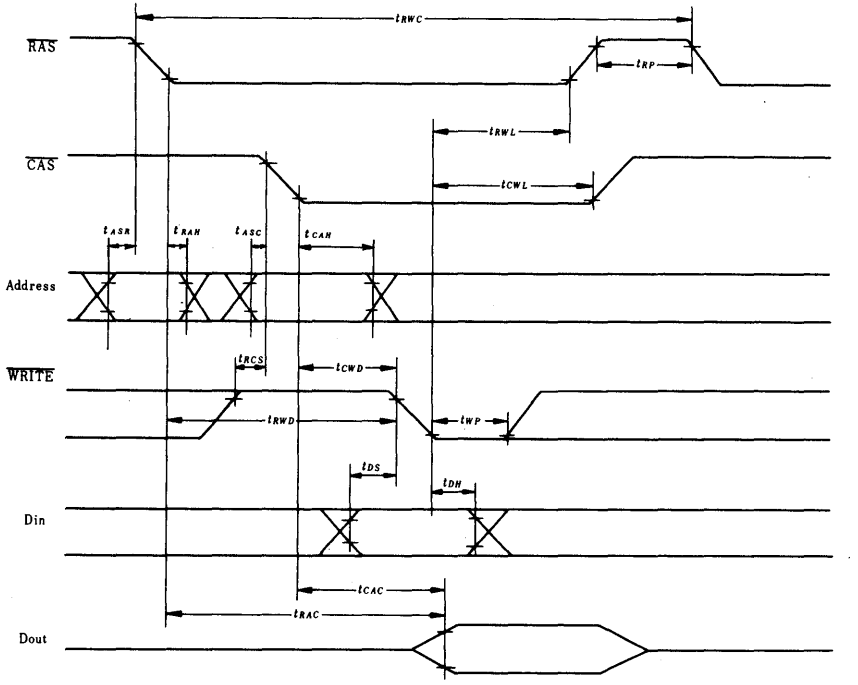
● READ CYCLE



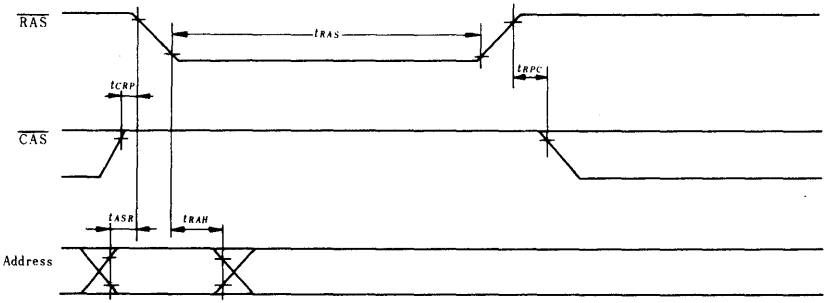
● WRITE CYCLE



● READ MODIFY WRITE CYCLE

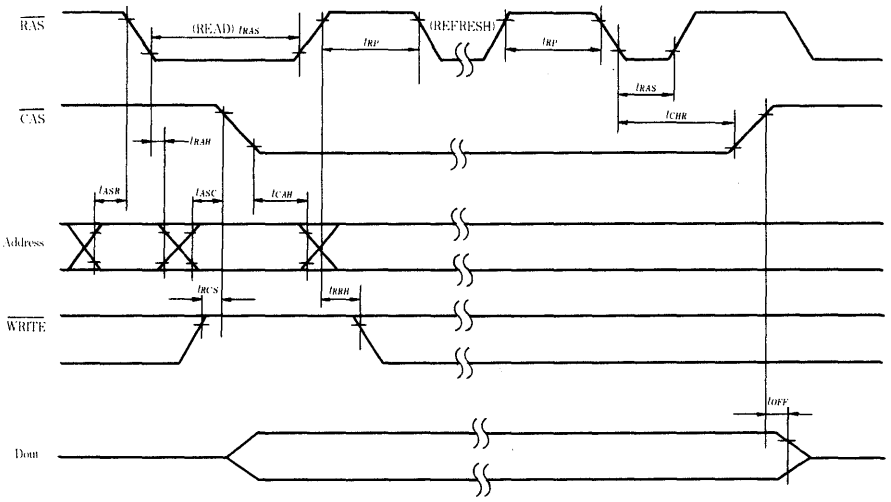


● $\overline{RAS}$ ONLY REFRESH CYCLE

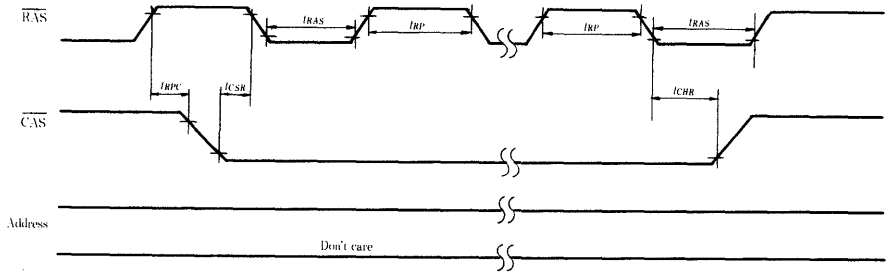


* REFRESH ADDRESS $A_0 - A_7$ ($AX_0 - AX_7$)

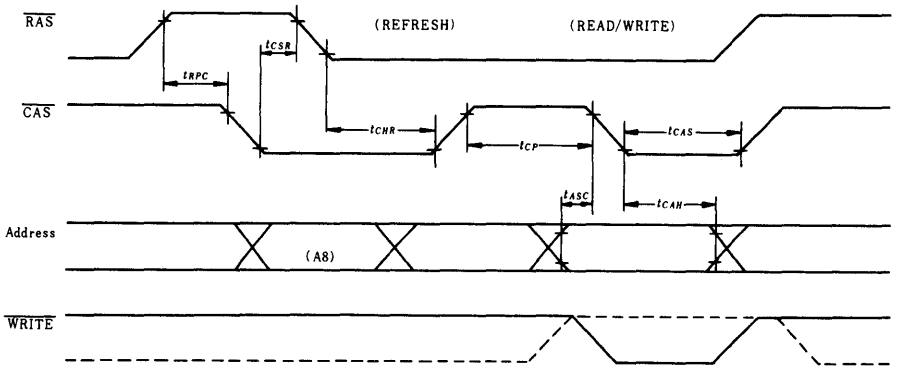
● HIDDEN REFRESH CYCLE



● $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



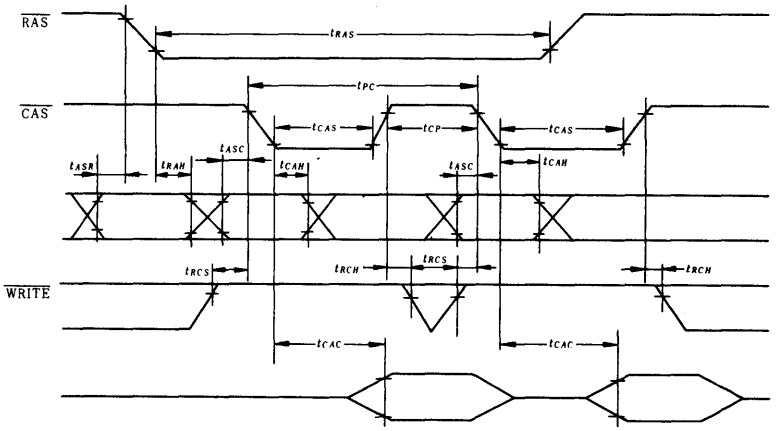
● COUNTER TEST



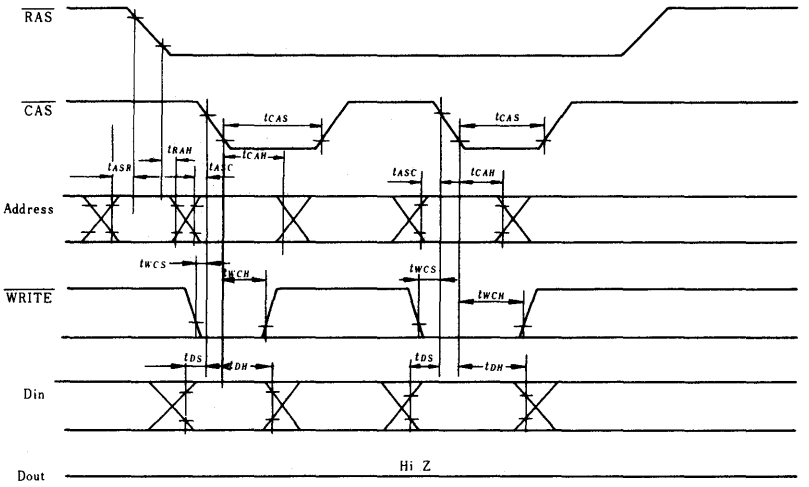
■ PAGE MODE CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	HM50256/P-12		HM50256/P-15		HM50256/P-20		Unit
		min	max	min	max	min	max	
Page Mode Supply Current	I_{CC7}	—	57	—	48	—	37	mA
Page Mode Read or Write Cycle	t_{PC}	120	—	145	—	190	—	ns
$\overline{CAS}$ Precharge Time, Page Cycle	t_{CP}	50	—	60	—	80	—	ns
Page Mode Read Modify Write Cycle	t_{PCM}	165	—	195	—	250	—	ns

● PAGE MODE READ CYCLE



● PAGE MODE WRITE CYCLE



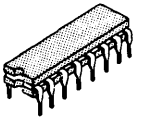
HM50257-12,HM50257-15, HM50257-20,HM50257P-12, HM50257P-15,HM50257P-20

262144-word × 1-bit Dynamic Random Access Memory

■ FEATURES

- Industry standard 16-pin DIP
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 350mW active, 20mW standby
- High speed: Access Time 120ns/150ns/200ns (max.)
- Common I/O capability using early write operation
- Nibble mode capability
- TTL compatible
- 256 refresh cycles . . . . . (4ms)
- 3 Variations of refresh; $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh

HM50257 Series

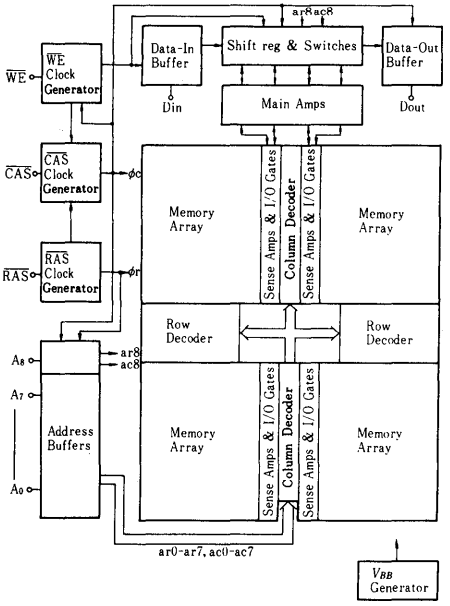


(DG-16B)

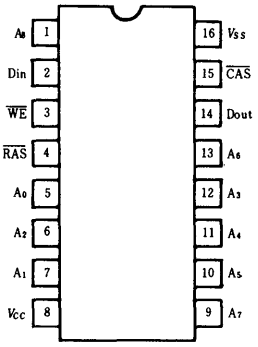
HM50257P Series

(DP-16A)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

A_0~A_8	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
A_0~A_7	Refresh Address Inputs

■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . -1V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature . . . . . (Cerdip) -65°C to +150°C
(Plastic DIP) -55°C to +125°C
Power dissipation 1W
Short circuit output current 50mA

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note 1) All voltages referenced to V_{SS}.

HITACHI

■DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	HM50257-12		HM50257-15		HM50257-20		Unit	Notes
		min	max	min	max	min	max		
Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=min)	I_{CC1}	—	83	—	70	—	55	mA	1
Stand by Current ($\overline{RAS}$=V_{IH}, Dout=High Impedance)	I_{CC2}	—	4.5	—	4.5	—	4.5	mA	
Refresh Current ($\overline{RAS}$ only Refresh, t_{RC}=min)	I_{CC3}	—	62	—	53	—	42	mA	
Standby Current ($\overline{RAS}$=V_{IH}, Dout Enable)	I_{CC5}	—	10	—	10	—	10	mA	1
Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh, t_{RC}=min)	I_{CC6}	—	69	—	58	—	45	mA	
Input leakage (0<V_{out}<7V)	I_{LI}	−10	10	−10	10	−10	10	μA	
Output leakage (0<V_{out}<7V)	I_{LO}	−10	10	−10	10	−10	10	μA	
Output levels High (I_{out}=−5mA)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output levels Low (I_{out}=4.2mA)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Notes) 1. I_{CC} depends on output loading condition when the device is selected I_{CC} max, is specified at the output open condition.

■CAPACITANCE (V_{CC}=5V±10%, Ta=25°C)

Parameter		Symbol	typ	max	Unit	Notes
Input Capacitance	Address, Data-In	C_{I1}	—	5	pF	1
	Clocks, Data-Out	C_{I2}	—	7		1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable Dout.

■ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V) [1), 10), 11)]

Parameter	Symbol	HM50257/P-12		HM50257/P-15		HM50257/P-20		Unit	Notes
		min	max	min	max	min	max		
Access Time from $\overline{RAS}$	t_{RAC}	—	120	—	150	—	200	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	60	—	75	—	100	ns	3, 4
Output Buffer Turn-off Delay	t_{OFF}	—	30	—	40	—	50	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	220	—	260	—	330	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	90	—	100	—	120	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{RAS}$ Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	60	—	75	—	100	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	120	—	150	—	200	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	25	—	30	—	ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	80	—	100	—	130	—	ns	
$\overline{WE}$ Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	40	—	45	—	55	—	ns	
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	100	—	120	—	155	—	ns	
Write Command Pulse Width	t_{WP}	40	—	45	—	55	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	40	—	45	—	55	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	40	—	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	40	—	45	—	55	—	ns	8, 9
Data-in Hold Time referenced to $\overline{RAS}$	t_{DHR}	100	—	120	—	155	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	

(to be continued)

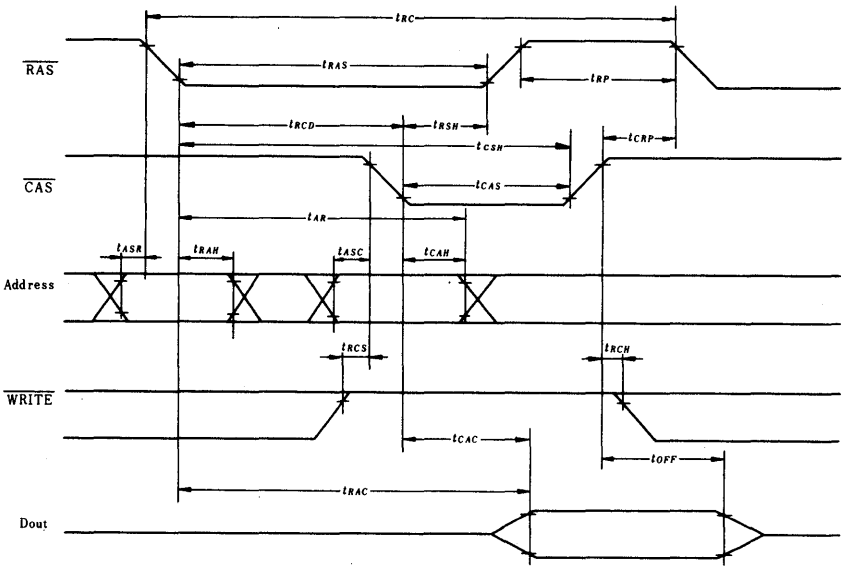
Parameter	Symbol	HM50257/P-12		HM50257/P-15		HM50257/P-20		Unit	Notes
		min	max	min	max	min	max		
Read-Write Cycle Time	t_{RWC}	265	—	310	—	390	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	60	—	75	—	100	—	ns	8
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	120	—	150	—	200	—	ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	50	—	60	—	80	—	ns	
$\overline{CAS}$ Setup Time	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	120	—	150	—	200	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	—	0	—	0	—	ns	

Notes

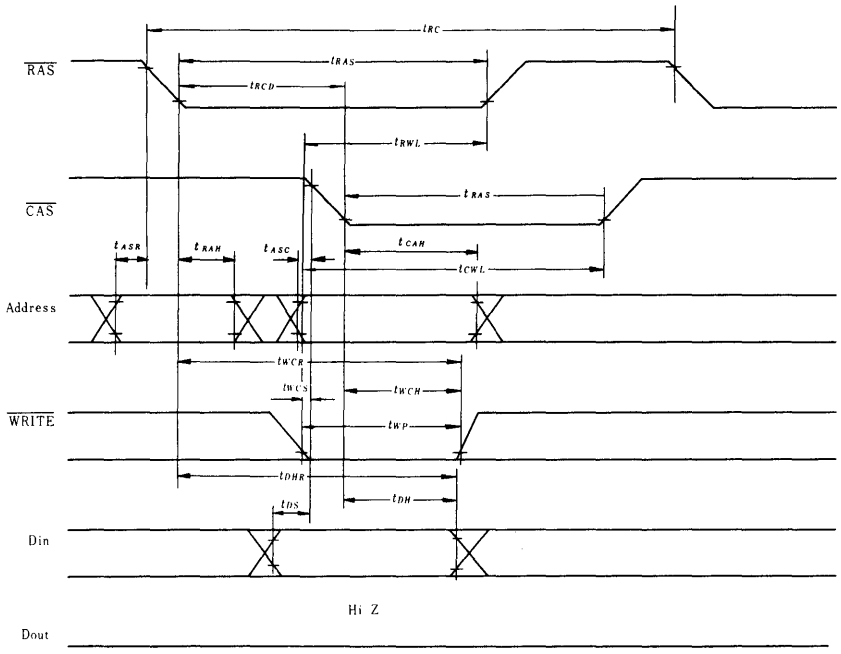
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and output voltage levels are not referred.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters.
   They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100μs is required after power-up then excute at least 8 initialization cycles.
11. At least, 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycle are required before using internal refresh counter.

■ TIMING WAVEFORMS

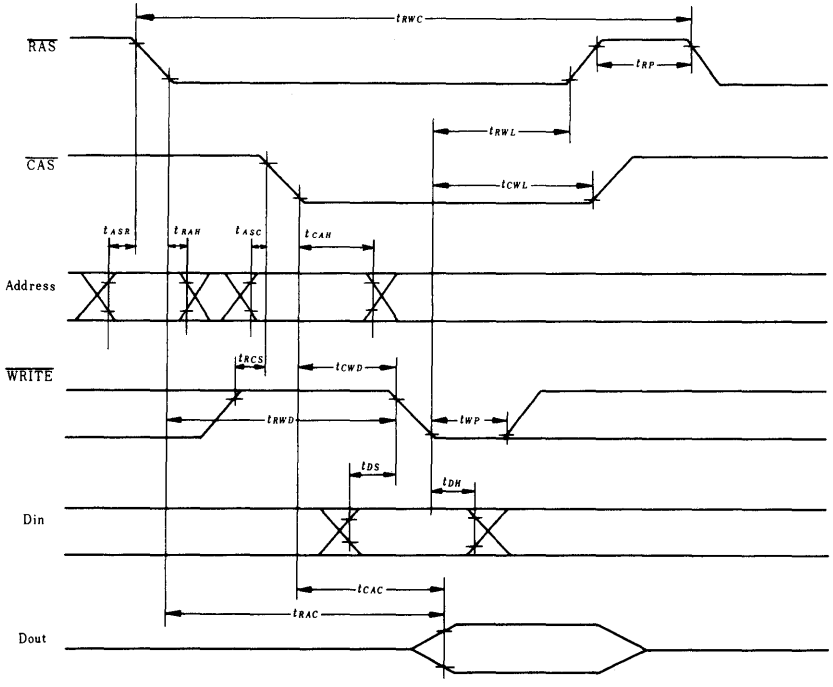
● READ CYCLE



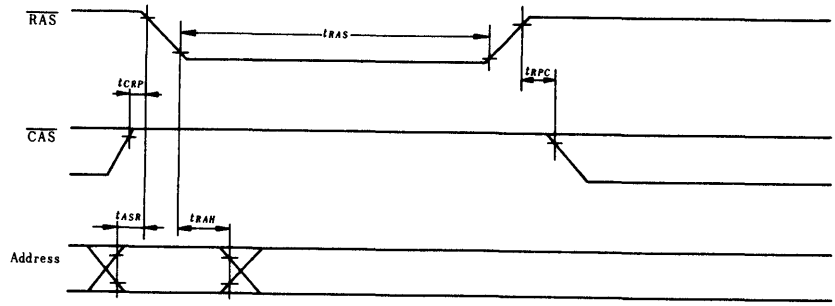
● WRITE CYCLE



● READ MODIFY WRITE CYCLE

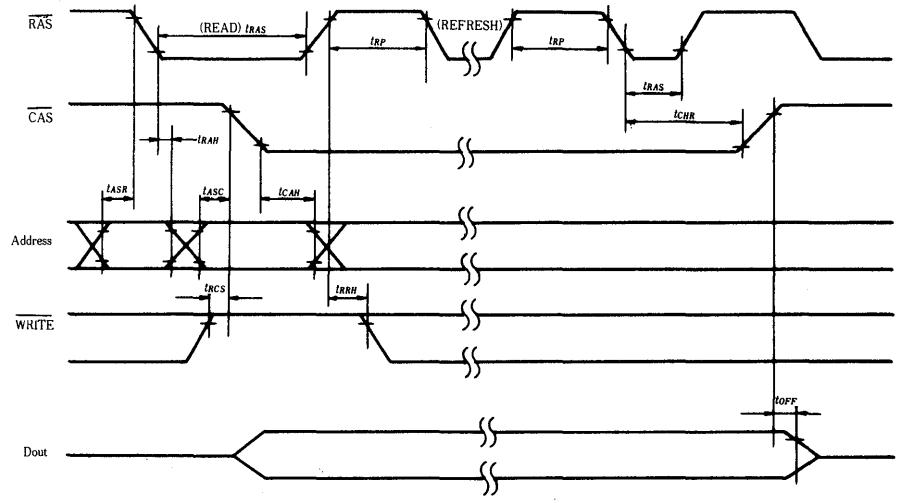


● $\overline{RAS}$ ONLY REFRESH CYCLE

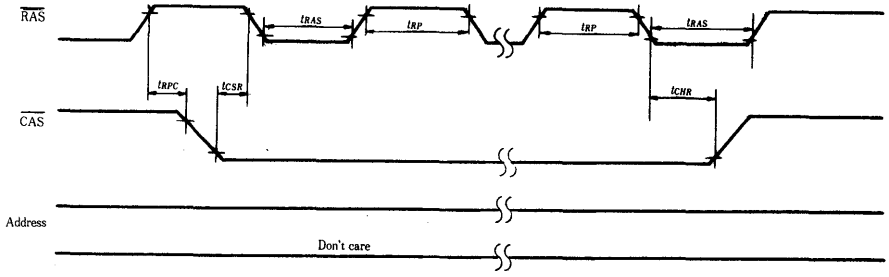


* REFRESH ADDRESS $A_0 - A_7$ ($AX_0 - AX_7$)

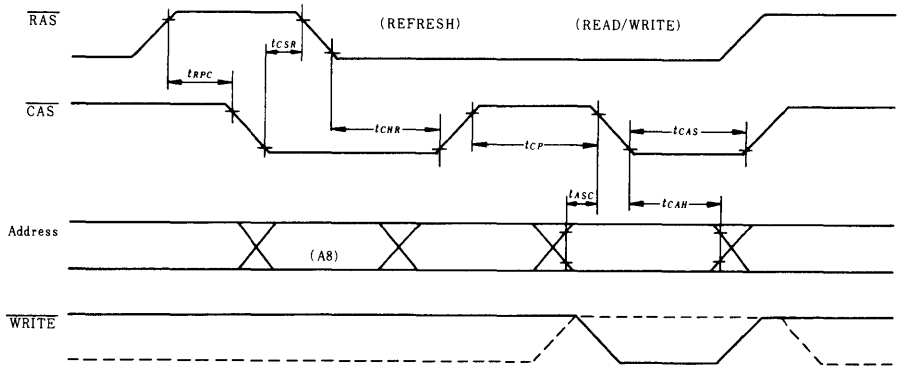
● HIDDEN REFRESH CYCLE



● $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



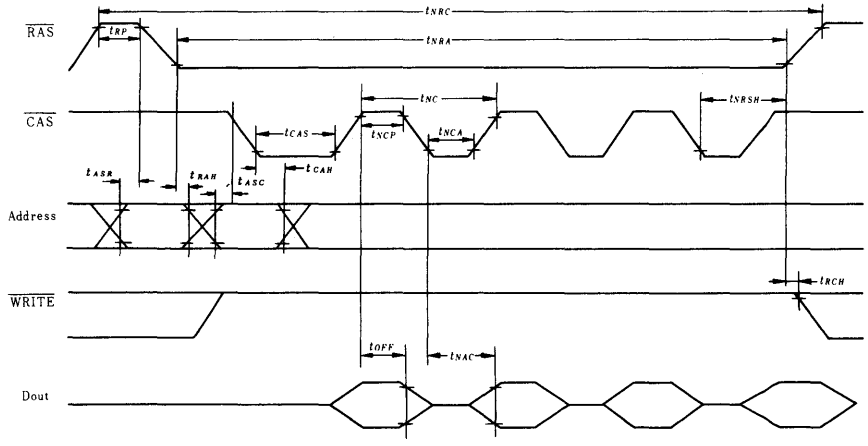
● COUNTER TEST



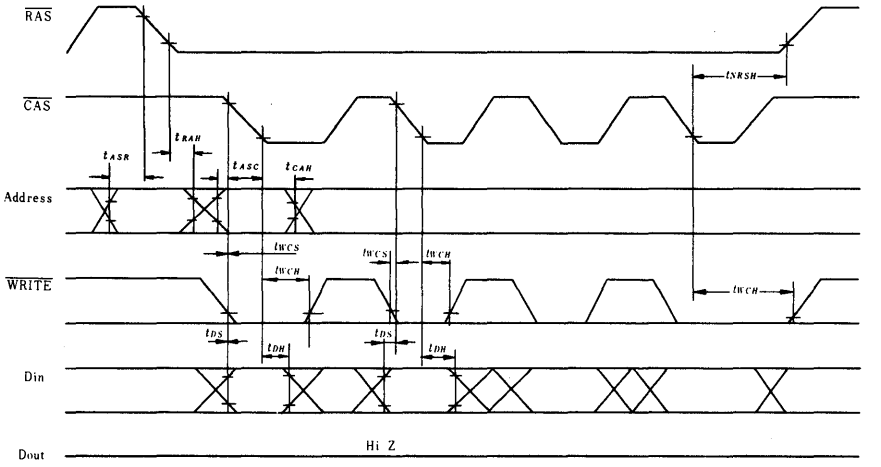
■ NIBBLE MODE CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	HM50257/P-12		HM50257/P-15		HM50257/P-20		Unit
		min	max	min	max	min	max	
Nibble Mode Supply Current	I_{CC8}	–	57	–	48	–	37	mA
Nibble Mode Access Time	t_{NAC}	–	25	–	25	–	35	ns
Nibble Mode $\overline{RAS}$ Cycle Time	t_{NRC}	390	–	460	–	590	–	ns
Nibble Mode $\overline{RAS}$ Pulse Width	t_{NRA}	290	–	350	–	460	–	ns
Nibble Mode Cycle Time	t_{NC}	55	–	60	–	80	–	ns
Nibble Mode $\overline{CAS}$ Precharge Time	t_{NCP}	20	–	25	–	35	–	ns
Nibble Mode $\overline{CAS}$ Pulse Width	t_{NCA}	25	–	25	–	35	–	ns
Nibble Mode $\overline{RAS}$ Hold Time	t_{NRSH}	40	–	45	–	55	–	ns
Nibble Mode $\overline{CAS}$ to $\overline{WE}$ Delay	t_{NCWD}	20	–	25	–	35	–	ns
Nibble Mode Write Command to $\overline{CAS}$ Lead Time	t_{NCWL}	20	–	25	–	35	–	ns
Nibble Mode Write Command to $\overline{RAS}$ Lead Time	t_{NRWL}	40	–	45	–	35	–	ns
Nibble Mode Write Command Pulse Widt	t_{NWP}	20	–	25	–	35	–	ns

● NIBBLE MODE READ CYCLE



● NIBBLE MODE WRITE CYCLE



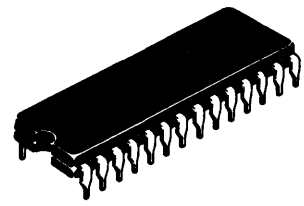
MOS MASK ROM

HN61364P, HN61364FP

8192-word x 8-bit Mask Programmable Read Only Memory

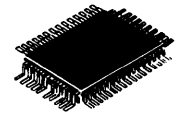
The HN61364P/FP is a mask-programmable, byte-organized memory designed for use in bus-organized systems.
To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation.
The active level of the CS, $\overline{OE}_0 \sim \overline{OE}_2$ inputs and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a powerdown mode.

HN61364P



(DP-28)

HN61364FP

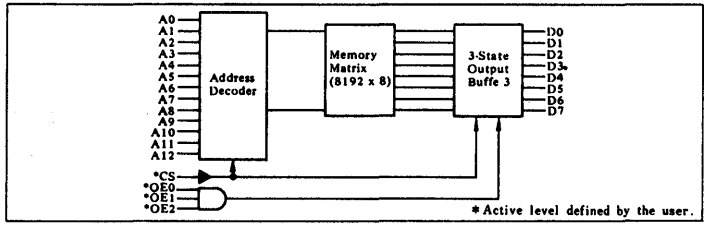


(FP-54)

■ FEATURES

- Fully Static Operation
- Automatic Power Down
- Single +5V Power Supply
- Three-state Data Output for OR-ties
- Mask Programmable Chip Select and Output Enable
- TTL Compatible
- Maximum Access Time; 250ns
- Low Power Standby and Low Power Operation; Standby 5μW (typ), Operation 50mW (typ)
- Pin Compatible with EPROM

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature	T_{opr}	−20 to +75	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Bias Storage Temperature	T_{bias}	−20 to +85	°C

* with respect to V_{SS}

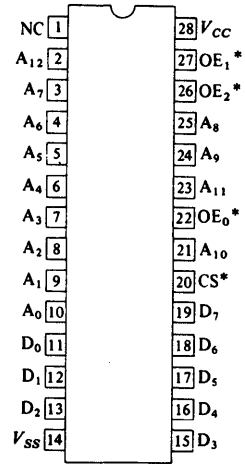
■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage *	V_{CC}	4.5	5.0	5.5	V
Input Voltage *	V_{IL}	−0.3	–	0.8	V
	V_{IH}	2.2	–	V_{CC}	V
Operating Temperature	T_{opr}	−20	–	75	°C

* with respect to V_{SS}

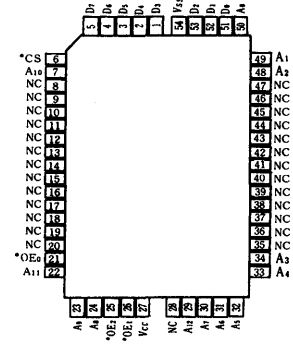
■ PIN ARRANGEMENT

● HN61364P



(Top View)

● HN61364FP



(Top View)

■ ELECTRICAL CHARAGTERISTICS (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = −20 to +75°C

Item		Symbol	Test Condition	min	typ**	max	Unit
Input High-level Voltage		V_{IH}		2.2	–	V_{CC}	V
Input Low-level Voltage		V_{IL}		−0.3	–	0.8	V
Output High-level Voltage		V_{OH}	I_{OH}=−205μA	2.4	–	–	V
Output Low-level Voltage		V_{OL}	I_{OL}=3.2mA	–	–	0.4	V
Input Leakage Current		I_{in}	V_{in}=0 to 5.5V	–	–	2.5	μA
Output High-level Leakage Current		I_{LOH}	V_{out}=2.4V, CS=0.8V, $\overline{CS}$=2.2V	–	–	10	μA
Output Low-level Leakage Current		I_{LOL}	V_{out}=0.4V, CS=0.8V, $\overline{CS}$=2.2V	–	–	10	μA
Supply Current	Active	I_{CC} *	V_{CC}=5.5V, Iout=0mA, trc=min, duty=100%	–	10	25	mA
	Standby	I_{SB}	V_{CC}=5.5V, $\overline{CS}\geqq V_{CC}$−0.2V, CS≦0.2V	–	1	30	μA
Input Capacitance		C_{in}	V_{in}=0V, f=1MHz, T_a=25°C	–	–	10	pF
Output Capacitance		C_{out}		–	–	15	pF

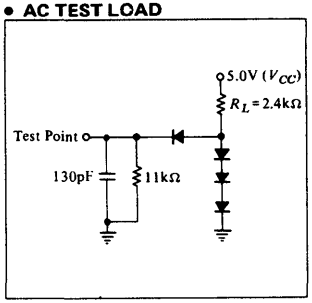
* Steady state current ** V_{CC} = 5V, T_a = 25°C

■ RECOMMENDED AC OPERATING CONDITIONS (READ SEQUENCE)

(V_{CC}=5V±10%, V_{SS}=0V, Ta=−20 to +75°C, t_r=t_f=20ns)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	250	–	ns
Address Access Time	t_{AA}	–	250	ns
Chip Select Access Time	t_{ACS}	–	250	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	–	ns
Output Enable to Output Valid	t_{OE}	–	100	ns
Output Enable to Output in Low Z	t_{OLZ}	10	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	100	ns
Chip Disable to Output in High Z	t_{OHZ}	0	100	ns
Output Hold from Address Change	t_{OH}	10	–	ns

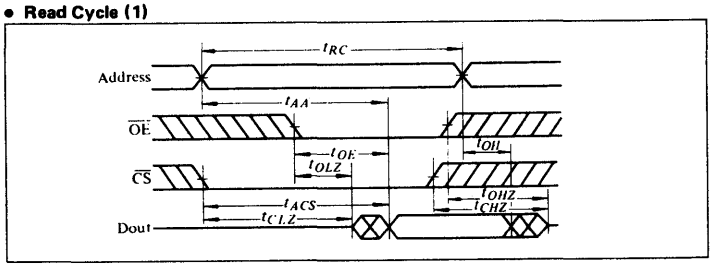
• AC TEST LOAD



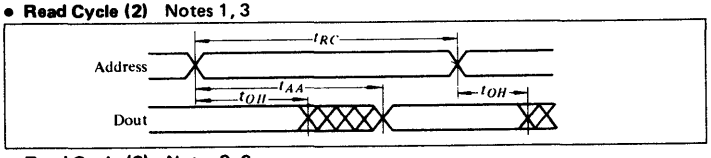
Notes) 1. t_r=t_f=20ns
2. C_L includes jig capacitance.
3. All diodes are 1S2074Ⓗ.

■ TIMING WAVEFORM

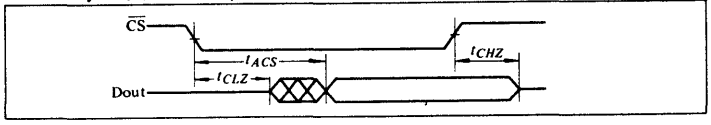
• Read Cycle (1)



• Read Cycle (2) Notes 1, 3



• Read Cycle (3) Notes 2, 3

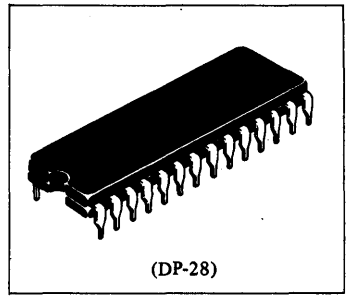


NOTES:
1. Device is continuously selected.
2. Address Vaild prior to or coincident with $\overline{CS}$ transition low.
3. $\overline{OE}$ = V_{IL}
4. Input pulse level: 0.8 to 2.4V
5. Input and output reference level: 1.5V

HN61364HP — Preliminary

8192-word x 8-bit Mask Programmable Read Only Memory

The HN61364HP is a mask-programmable, byte-organized memory designed for use in bus-organized systems.
To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation.
The active level of the CS, $OE_0 \sim OE_2$ inputs and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a powerdown mode.

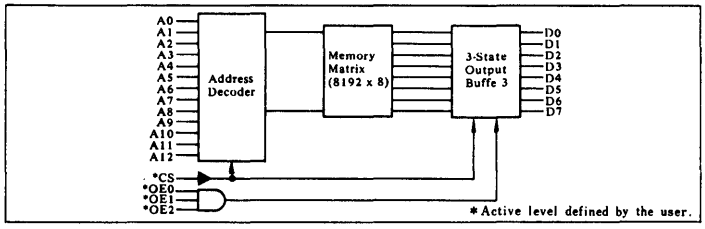


(DP-28)

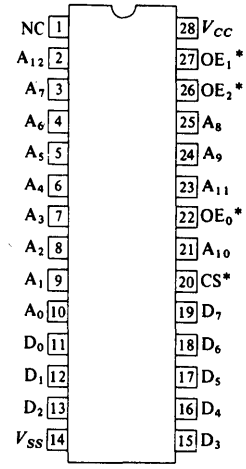
■ FEATURES

- Fully Static Operation
- Automatic Power Down
- Single +5V Power Supply
- Three-state Data Output for OR-ties
- Mask Programmable Chip Select and Output Enable
- TTL Compatible
- Maximum Access Time; 200ns
- Low Power Standby and Low Power Operation; Standby 5μW (typ), Operation 50mW (typ)
- Pin Compatible with EPROM

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

NOTE:
The specifications of this device are subject to change without notice.
Please contact your nearest Hitachis Sales Dept, regarding specifications.

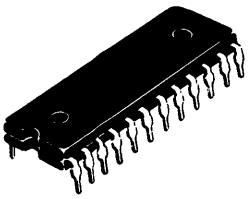
HN61365P

8192-word×8-bit Mask Programmable Read Only Memory

The HN61365P is a mask-programmable, byte-organized memory designed for use in bus-organized systems.

To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation.

The active level of the CS input and the memory content are defined by the user. The chip select input deselects the output and puts the chip in a power-down mode.

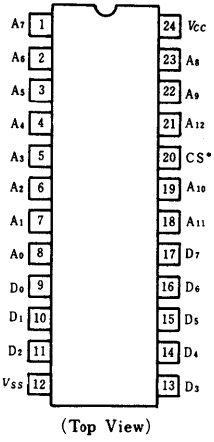


(DP-24)

■FEATURES

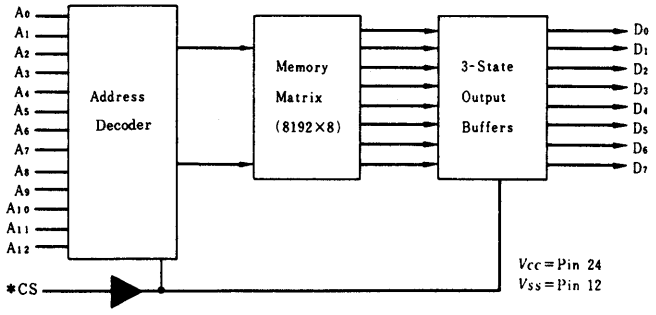
- Fully Static Operation
- Automatic Power Down
- Single +5 Volt Power Supply
- Three-State Data Output for OR-Ties
- Mask Programmable Chip Select
- TTL Compatible
- Maximum Access Time; 250ns
- Low Power Standby and Low Power Operation; Standby 5μW (typ.), Operation 50mW (typ.)
- Pin Compatible with EPROM

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



* Active level defined by the user.

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature	T_{opr}	−20 to +75	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (under bias)	T_{bias}	−20 to +85	°C

* with respect to V_{SS}

■RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
Input Voltage*	V_{IL}	−0.3	—	0.8	V
	V_{IH}	2.2	—	V_{CC}	V
Operating Temperature	T_{opr}	−20	—	75	℃

* With respect to V_{SS}

■ELECTRICAL CHARACTERISTICS (V_{CC}=5V ±10%, V_{SS}=0V, Ta=−20 to +75℃)

Item	Symbol	Test Conditions		min	typ**	max	Unit
Input Voltage	V_{IH}			2.2	—	V_{CC}	V
	V_{IL}			−0.3	—	0.8	V
Output Voltage	V_{OH}	I_{OH}=−205μA		2.4	—	—	V
	V_{OL}	I_{OL}=3.2mA		—	—	0.4	V
Input Leakage Current	I_{LI}	V_{IN}=0~5.5V		—	—	2.5	μA
Output Leakage Current	I_{LOH}	CS=0.8V, $\overline{CS}$=2.2V	V_{out}=2.4V	—	—	10	μA
	I_{LOL}		V_{out}=0.4V	—	—	10	μA
Active Supply Current	I_{CC}*	V_{CC}=5.5V, I_{DOUT}=0mA, t_{RC}=min, duty=100%		—	10	25	mA
Stand by Supply Current	I_{SB}	$\overline{CS}\geq V_{CC}-0.2V$, CS≦0.2V, V_{CC}=5.5V		—	1	30	μA
Input Capacitance	C_{in}	V_{in}=0V, f=1MHz, Ta=25℃		—	—	10	pF
Output Capacitance	C_{out}			—	—	15	pF

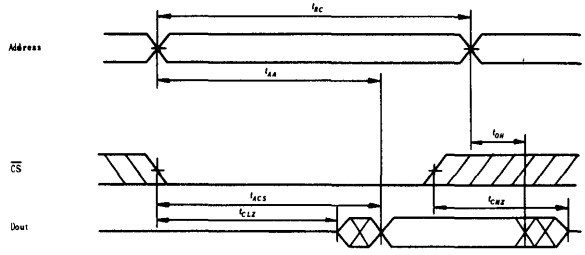
* Steady state current ** V_{CC}=5V, T_a=25℃

■RECOMMENDED AC OPERATING CHARACTERISTICS

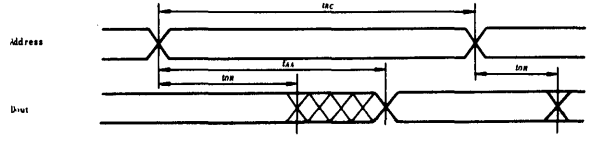
●READ SEQUENCE (V_{CC}=5V±10%, V_{SS}=0V, Ta=−20 to +75℃, t_r=t_f=20ns)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	250	—	ns
Address Access Time	t_{AA}	—	250	ns
Chip Select Access Time	t_{ACS}	—	250	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	ns
Chip deselection to Output in High Z	t_{CHZ}	0	100	ns
Output Hold from Address Change	t_{OH}	10	—	ns

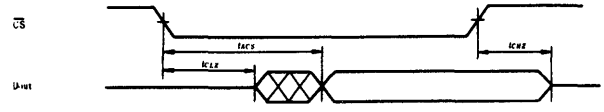
●READ CYCLE (1)



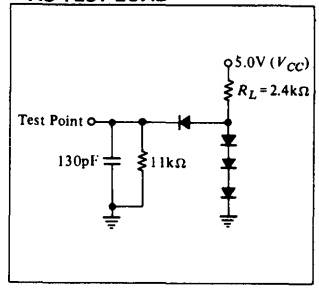
●READ CYCLE (2) (Notes 1)



●READ CYCLE (3) (Notes 2)



● AC TEST LOAD



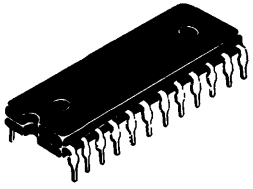
Notes) 1. t_r=t_f=20ns.
2. C_L includes jig capacitance.
3. All diodes are 1S2074Ⓗ.

Notes)
1. Device is continuously selected
2. Address Valid prior to or coincident with $\overline{CS}$ transition low.
3. Input pulse level : 0.8 to 2.4V
4. Input and output timing reference level : 1.5V

HN61366P

8192-word×8-bit Mask Programmable Read Only Memory

The HN61366P is a mask-programmable, byte-organized memory designed for use in bus-organized systems.
To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation.
The active level of the OE input and the memory content are defined by the user.

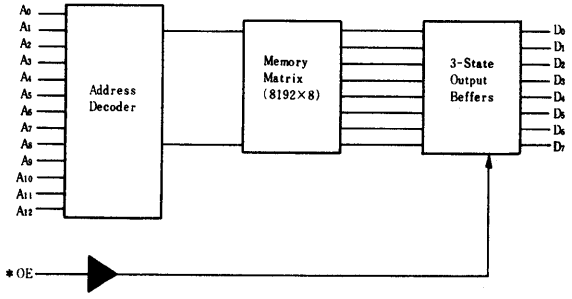


(DP-24)

■FEATURES

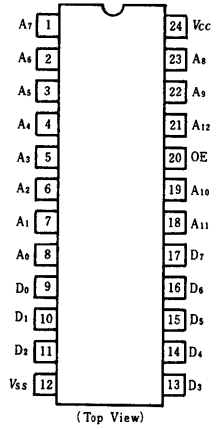
- Fully Static Operation
- Single +5V power supply
- Three-State Data Output for OR-Ties
- Mask Programmable Output Enable
- TTL Compatible
- Maximum Access Time; 250ns
- Low Power Operation; 50mW (typ.)
- Pin Compatible with EPROM

■BLOCK DIAGRAM



* Active level defined by the user.

■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature	T_{opr}	−20 to +75	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (under bias)	T_{bias}	−20 to +85	°C

* With respect to V_{SS}

■RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
Input Voltage*	V_{IL}	−0.3	—	0.8	V
	V_{IH}	2.2	—	V_{CC}	V
Operating Temprature	T_{opr}	−20	—	75	°C

* With respect to V_{SS}

■ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, Ta=−20 to +75°C)

Item	Symbol	Test Conditions		min	typ**	max	Unit
Input Voltage	V_{IH}			2.2	—	V_{CC}	V
	V_{IL}			−0.3	—	0.8	V
Output Voltage	V_{OH}	I_{OH}=−205μA		2.4	—	—	V
	V_{OL}	I_{OL}=3.2mA		—	—	0.4	V
Input Leakage Current	I_{LI}	V_{IN}=0~5.5V		—	—	2.5	μA
Output Leakage Current	I_{LOH}	OE=0.8V, $\overline{OE}$=2.2V	V_{OUT}=2.4V	—	—	10	μA
	I_{LOL}		V_{OUT}=0.4V	—	—	10	μA
Operating Supply Current	I_{CC}*	V_{CC}=5.5V, I_{OUT}=0mA, t_{RC}=min		—	10	25	mA
Input Capacitance	C_{in}	V_{in}=0V, f=1MHz, Ta=25°C		—	—	10	pF
Output Capacitance	C_{out}			—	—	15	pF

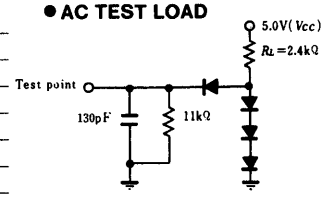
* Steady state current ** V_{CC}=5V, T_a=25°C

■RECOMMENDED AC OPERATING CONDITIONS

●READ CYCLE (V_{CC}=5V±10%, V_{SS}=0V, Ta=−20~+75°C, t_r=t_f=20ns)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	250	—	ns
Address Access Time	t_{AA}	—	250	ns
Output Enable to Output Valid	t_{OE}	—	100	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	100	ns
Output Hold from Address Change	t_{OH}	10	—	ns

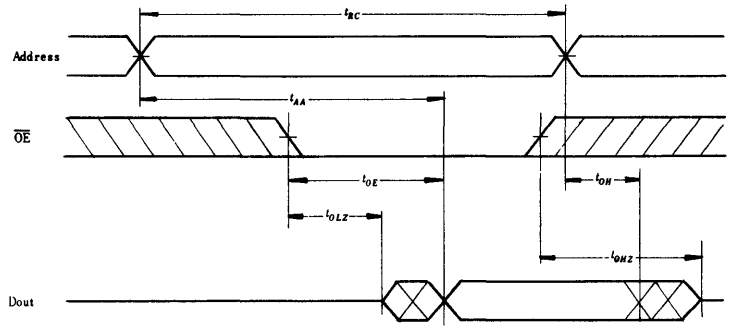
●AC TEST LOAD



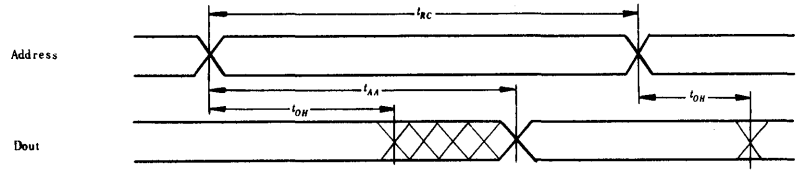
Notes) 1. t_r=t_f=20ns
2. C_L includes jig capacitance.
3. All diodes are 1S2074Ⓗ.

■TIMING WAVEFORM

●READ CYCLE (1)



●READ CYCLE (2)Note 1)



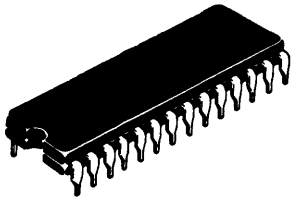
Note) 1. $\overline{OE}$=V_{IL}
2. Imput pulse level : 0.8 to 2.4V
3. Imput and output timing reference level : 1.5V

HN613128P, HN613128FP

16384-word×8-bit Mask Programmable Read Only Memory

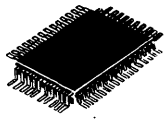
The HN613128P/FP is a mask-programmable, byte-organized memory designed for use in bus-organized systems. To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation. The active level of the CS, OE_0, OE_1 input and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a power-down mode.

HN613128P



(DP-28)

HN613128FP

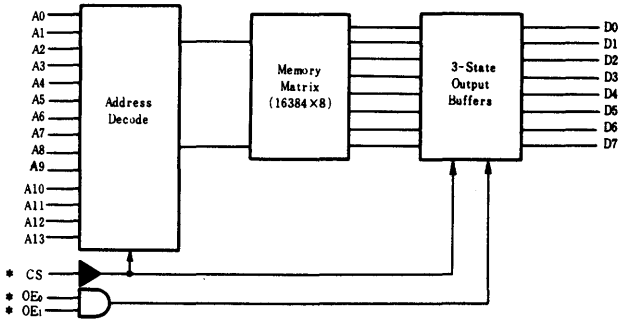


(FP-54)

■FEATURES

- Fully Static Operation
- Automatic Power Down
- Single +5-Volt Power Supply
- Three-State Data Output for OR-Ties
- Mask Programmable Chip Select, Output Enable
- TTL Compatible
- Maximum Access Time; 250ns
- Low Power Standby and Low Power Operation;
  Standby: 5μW (typ.)
  Operation: 50mW (typ.)
- Pin Compatible with EPROM

■BLOCK DIAGRAM



* Active level defined by the user.

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{opr}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range (under bias)	T_{bias}	−20 to +85	°C

* With respect to V_{SS}.

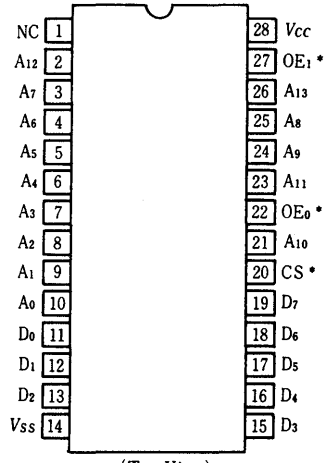
■RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
Input Voltage*	V_{IL}	−0.3	—	0.8	V
	V_{IH}	2.2	—	V_{CC}	V
Operating Temperature	T_{opr}	−20	—	75	°C

* With respect to V_{SS}.

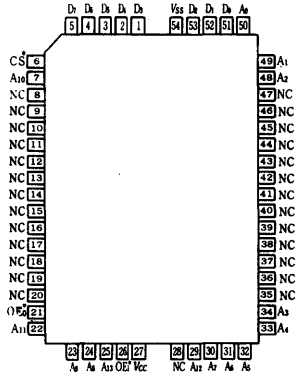
■PIN ARRANGEMENT

●HN613128P



(Top View)

●HN613128FP



(Top View)

■ ELECTRICAL CHARACTERISTICS (V_{CC}=5.0V±10%, V_{SS}=0V, Ta=−20 to +75°C)

Item	Symbol	Test Condition	min	typ**	max	Unit
Input High-level Voltage	V_{IH}		2.2	—	V_{CC}	V
Input Low-level Voltage	V_{IL}		−0.3	—	0.8	V
Output High-level Voltage	V_{OH}	I_{OH}=−205μA	2.4	—	—	V
Output Low-level Voltage	V_{OL}	I_{OL}=3.2mA	—	—	0.4	V
Input Leakage Current	I_{in}	V_{in}=0 to 5.5V	—	—	2.5	μA
Output High-level Leakage Current	I_{LOH}	V_{out}=2.4V, CS=0.8V, $\overline{CS}$=2.2V	—	—	10	μA
Output Low-level Leakage Current	I_{LOL}	V_{out}=0.4V, CS=0.8V, $\overline{CS}$=2.2V	—	—	10	μA
Supply Current (Active/Standby)	I_{CC}*/ I_{SB}	V_{CC}=5.5V, I_{DOUT}=0mA, t_{RC}=min, duty=100%/$\overline{CS}$≧V_{CC}−0.2V, CS≦0.2V	—	10/1	25/30	mA/μA
Input Capacitance	C_{in}	V_{in}=0V, f=1.0MHz, Ta=25°C	—	—	10	pF
Output Capacitance	C_{out}	V_{in}=0V, f=1.0MHz, Ta=25°C	—	—	15	pF

* Steady state current ** V_{CC}=5V, Ta=25°C

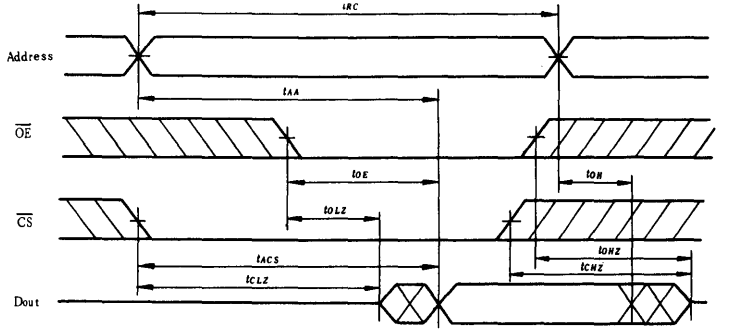
■ RECOMMENDED AC OPERATING CONDITIONS (READ SEQUENCE)

(V_{CC}=5.0V±10%, V_{SS}=0V, Ta=−20 to +75°C, All timing with t_r=t_f=20ns)

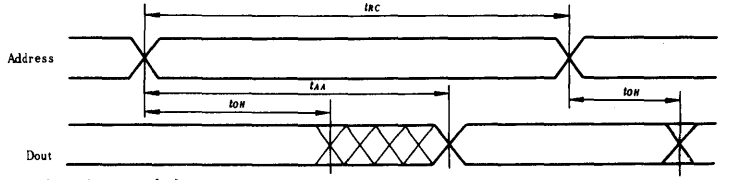
Item	Symbol	HN613128P		Unit
		min	max	
Read Cycle Time	t_{RC}	250	—	ns
Address Access Time	t_{AA}	—	250	ns
Chip Select Access Time	t_{ACS}	—	250	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	ns
Output Enable to Output Valid	t_{OE}	—	100	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	ns
Chip deselection to Output in High Z	t_{CHZ}	0	100	ns
Chip Disable to Output in High Z	t_{OHZ}	0	100	ns
Output Hold from Address Change	t_{OH}	10	—	ns

■ TIMING WAVEFORM

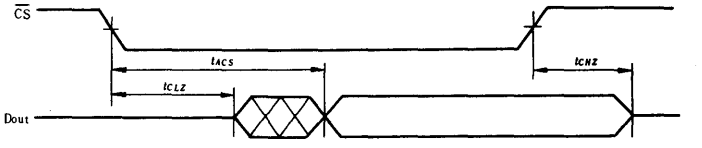
● READ CYCLE (1)



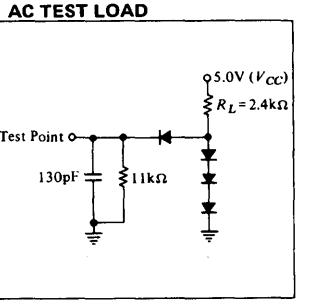
● READ CYCLE (2) (Notes 1, 3)



● READ CYCLE (3) (Notes 2, 3)



● AC TEST LOAD



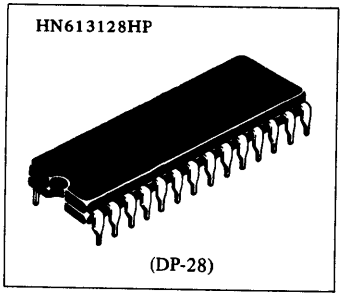
Notes) 1. t_r=t_f=20ns.
2. C_L includes jig capacitance.
3. All diodes are 1S2074Ⓗ.

NOTES:
1. Device is continuously selected.
2. Address Valid prior to or coincident with $\overline{CS}$ transition low.
3. $\overline{OE}$ = V_{IL}.
4. Input pulse level: 0.8 to 2.4V
5. Input and output reference level: 1.5V

HN613128HP — Preliminary

16384-word x 8-bit Mask Programmable Read Only Memory

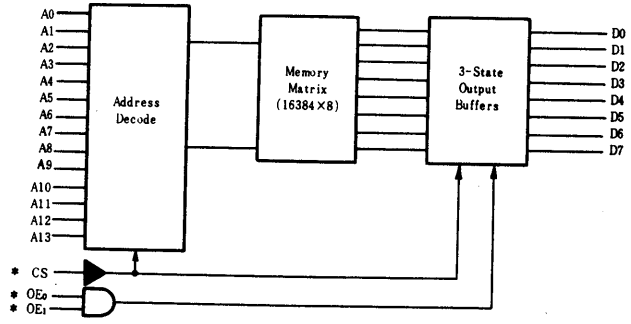
The HN613128HP is a mask-programmable, byte-organized memory designed for use in bus-organized systems. To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation. The active level of the CS, OE_0, OE_1 input and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a power-down mode.



■ FEATURES

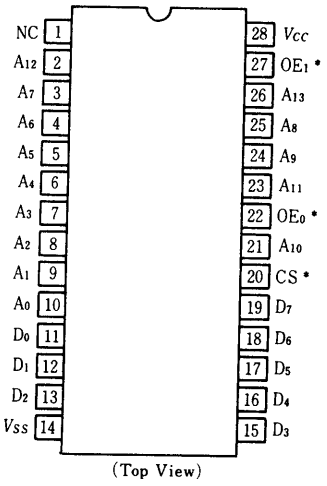
- Fully Static Operation
- Automatic Power Down
- Single +5-Volt Power Supply
- Three-State Data Output for OR-Ties
- Mask Programmable Chip Select, Output Enable
- TTL Compatible
- Maximum Access Time: 200ns
- Lower Standby and Low Power Operation;
  - Standby: 5μW (typ.)
  - Operation: 50mW (typ.)
- Pin Compatible with EPROM

■ BLOCK DIAGRAM



* Active level defined by the user.

■ PIN ARRANGEMENT



(Top View)

NOTES:

The specifications of this device are subject to change without notice.

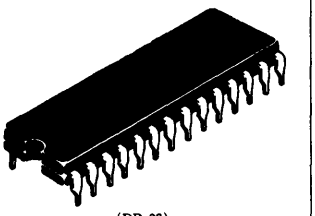
Please contact your nearest Hitachis Sales Dept, regarding specifications.

HN61256P, HN61256FP

32768×8-bit or 65536×4-bit CMOS Mask Programmable Read Only Memory

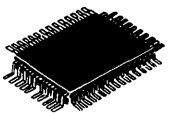
The Hitachi HN61256P/FP is a mask programmable 32768 x 8-bit or 65536x4-bit CMOS read only memory. It operates from a single power supply and is compatible with TTL. Low power consumption makes this memory well-suited for battery-operation or hand-held personal computers. Memory expansion can be implemented through one chip select input. Either active "High" or active "Low" or chip select input and a chip enable input are defined at mask level. The organization of 8 bit or 4 bit is defined by the user.

HN61256P



(DP-28)

HN61256FP

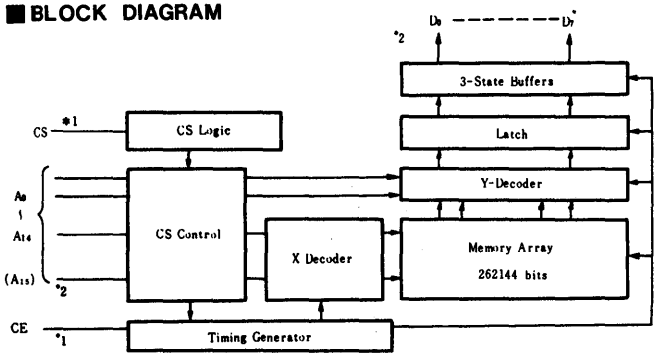


(FP-54)

■FEATURES

- Mask-programmable selection of either 4-bit or 8-bit organization
- Three-state outputs, can be wire-ORed.
- One mask programmable chip select terminal facilitates memory expansion.
- A single 5V power supply (±10%)
- Low power consumption: Operation 7.5mW (typ.), Standby 5μW (typ.)
- TTL compatible
- Access time: 3.5μs (max)

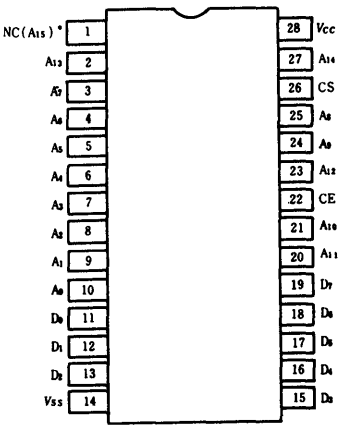
■BLOCK DIAGRAM



*1 Active level defined at mask level.
*2 Mask programmable selection of either 4-bit or 8-bit organization.
In 4-bit organization, data outputs are D_0 to D_3.

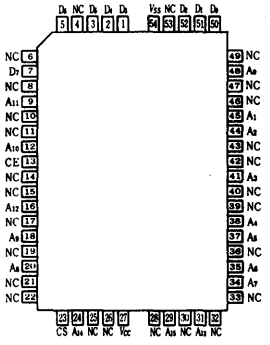
■PIN ARRANGEMENT

●HN61256P



(Top View)

●HN61256FP



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage*	V_{CC}	−0.3～+7.0	V
Input Voltage*	V_{in}	−0.3～+7.0	V
Operating Temperature Range	T_{opr}	0～+75	°C
Storage Temperature Range	T_{stg}	−55～+125	°C
Bias Storage Temperature Range	T_{bias}	−20～+85	°C

Note : * Referenced to V_{SS}.

■ ELECTRICAL CHARACTERISTICS

(V_{CC}=5V±10%, V_{SS}=0V, Ta=0～+75°C)

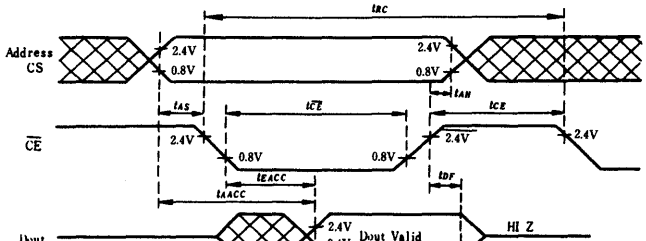
Item		Symbol	Test Condition		min	typ**	max	Unit
Input "High" Level Voltage		V_{IH}			2.4	—	V_{CC}	V
Input "Low" Level Voltage		V_{IL}			0	—	0.8	V
Output "High" Level Voltage		V_{OH}	I_{OH}=−100μA		2.4	—	—	V
Output "Low" Level Voltage		V_{OL}	I_{OL}=1.6mA		—	—	0.4	V
Input Leakage Current		I_{in}	V_{in}=0～5.5V		—	—	2.5	μA
Output "High" Level Leakage Current		I_{LOH}	$\overline{CE}$=0.8V	V_{out}=2.4V	—	—	5	μA
Output "Low" Level Leakage Current		I_{LOL}	$\overline{CE}$=2.4V	V_{out}=0.4V	—	—	5	μA
Supply Current	In stand-by	I_{SB}	$\overline{CS}\geqq V_{CC}-0.2V$, $CS\leqq V_{SS}+0.2V$	V_{CC}=5.5V	—	1	30	μA
	In operation	I_{CC}*	t_{RC}=4.0μs, I_{out}=0mA, $t_{\overline{CE}}$=3.0μs		—	1.5	3.0	mA
Input Capacitance		C_{in}	V_{in}=0V, f=1MHz, Ta=25°C		—	—	10	pF
Output Capacitance		C_{out}			—	—	12.5	pF

* Steady state current ** V_{CC}=5V, T_a=25°C

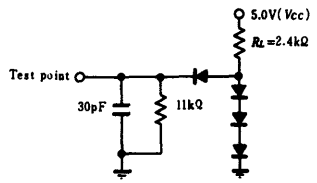
■ AC OPERATING CONDITION AND CHARACTERISTICS

● READ SEQUENCE (V_{CC}=5V±10%, V_{SS}=0V, Ta=0～+75°C, t_r=t_f=20ns)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	4.0	—	μs
Address Access Time	t_{AACC}	—	3.5	μs
Chip Enable Access Time	t_{EACC}	—	3.0	μs
Data Hold Time from Address	t_{DF}	0.05	0.5	μs
Address Set-up Time	t_{AS}	0.5	—	μs
Address Hold Time	t_{AH}	0	—	μs
Chip Enable ON Time	$t_{\overline{CE}}$	3.0	—	μs
Chip Enable OFF Time	t_{CE}	0.5	—	μs



● AC TEST LOAD



Notes : 1. t_r=t_f=20ns.
2. C_L includes jig capacitance.
3. All diodes are 1S2074Ⓗ.

HN613256P, HN613256FP

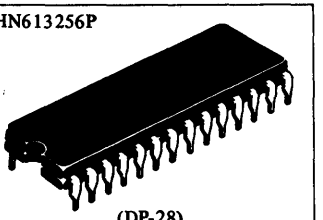
32768-word x 8-bit Mask Programmable Read Only Memory

The HN613256P/FP is a mask-programmable, byte-organized memory designed for use in bus-organized system.

To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks nor refreshing because of static operation.

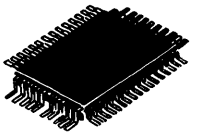
The active level of the CS and OE input, and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a power-down mode.

HN613256P



(DP-28)

HN613256FP

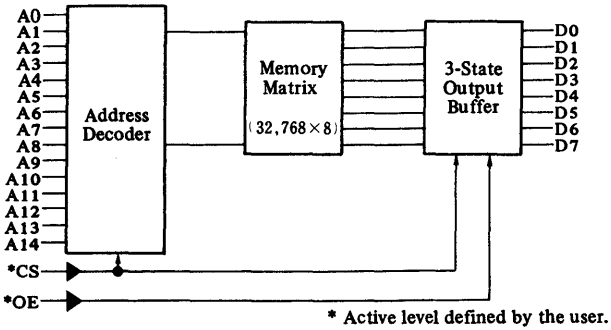


(FP-54)

■ FEATURES

- Fully Static Operation
- Automatic Power Down
- Single +5V Power Supply
- Three-state Data Output for OR-ties
- Mask Programmable Chip Select and Output Enable
- TTL Compatible
- Maximum Access Time: 250ns
- Low Power Standby and Low Power Operation; Standby 5μW (typ.), Operation 50mW (typ.)
- Pin Compatible with EPROM

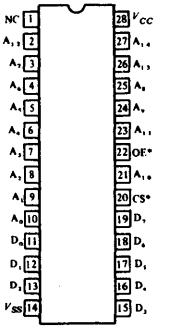
■ BLOCK DIAGRAM



* Active level defined by the user.

■ PIN ARRANGEMENT

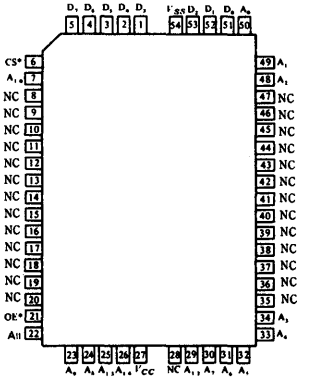
- **HN613256P**



(Top View)

* Active level can be defined by the customer.

- **HN613256FP**



(Top View)

* Active level can be defined by the customer.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{opr}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range (Under Bias)	T_{bias}	−20 to +85	°C

*With respect to V_{SS}

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
Input Voltage*	V_{IL}	−0.3	—	0.8	V
	V_{IH}	2.2	—	V_{CC}	V
Operating Temperature	T_{opr}	−20	—	75	°C

* With respect to V_{SS}.

HITACHI

■ ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V±10%, V_{SS} = 0V, T_a = −20 ~ +75 °C)

Item		Symbol	Test Condition		min	typ**	max	Unit
Input Voltage		V_{IH}			2.2	–	V_{CC}	V
		V_{IL}			−0.3	–	0.8	V
Output Voltage		V_{OH}	I_{OH} = −205 µA		2.4	–	–	V
		V_{OL}	I_{OL} = 3.2 mA		–	–	0.4	V
Input Leakage Current		I_{in}	V_{in} = 0 ~ 5.5V		–	–	2.5	µA
Output Leakage Current		I_{LOH}	CS = 0.8V, $\overline{CS}$ = 2.2V	V_{out} = 2.4V	–	–	10	µA
		I_{LOL}		V_{out} = 0.4V	–	–	10	µA
Supply Current	Active	I_{CC}*	V_{CC} = 5.5V, I_{out} = 0mA, t_{RC} = min, duty = 100%.		–	10	30	mA
	Standby	I_{SB}	V_{CC} = 5.5V, $\overline{CS} \geqq V_{CC}$ − 0.2V, CS ≦ 0.2V		–	1	30	µA
Input Capacitance		C_{in}	V_{in} = 0V, f = 1 MHz, T_a = 25 °C		–	–	10	pF
Output Capacitance		C_{out}			–	–	15	pF

* Steady state current
** V_{CC}=5V, T_a=25°C

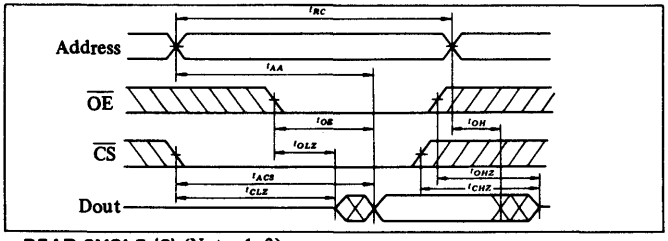
■ RECOMMENDED AC OPERATING CONDITIONS (READ SEQUENCE)

(V_{CC}=5V±10%, V_{SS}=0V, Ta=−20~+75°C, t_r=t_f=20ns)

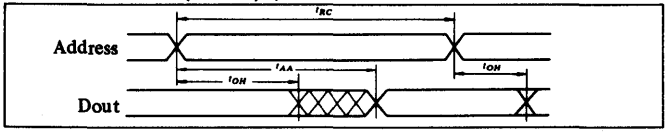
Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	200	–	ns
Address Access Time	t_{AA}	–	200	ns
Chip Select Access Time	t_{ACS}	–	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	–	ns
Output Enable to Output Valid	t_{OE}	–	100	ns
Output Enable to Output in Low Z	t_{OLZ}	10	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	100	ns
Chip Disable to Output in High Z	t_{OHZ}	0	100	ns
Output Hold from Address Change	t_{OH}	10	–	ns

■ TIMING WAVEFORM

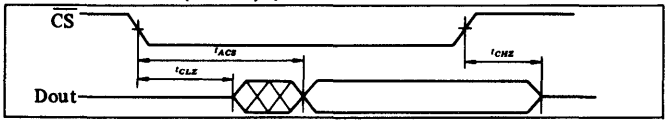
• READ CYCLE (1)



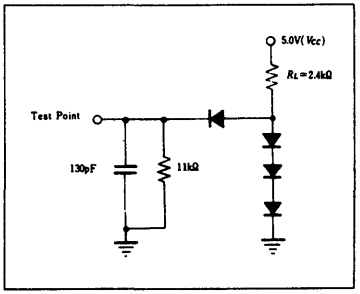
• READ CYCLE (2) (Notes 1, 3)



• READ CYCLE (3) (Notes 2, 3)



• AC TEST LOAD



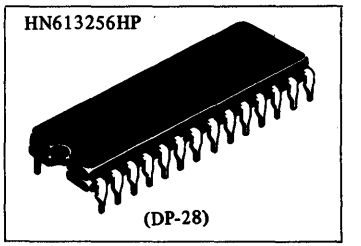
Notes : 1. t_r = t_f = 20ns
2. C_L includes jig capacitance
3. All diodes are 1S2074Ⓗ

NOTES:
1. Device is continuously selected.
2. Address Valid prior to or coincident with $\overline{CS}$ transition low.
3. $\overline{OE}$ = V_{IL}.
4. Input pulse level: 0.8 to 2.4V
5. Input and output reference level: 1.5V

HN613256HP — Preliminary

32768-word x 8-bit Mask Programmable Read Only Memory

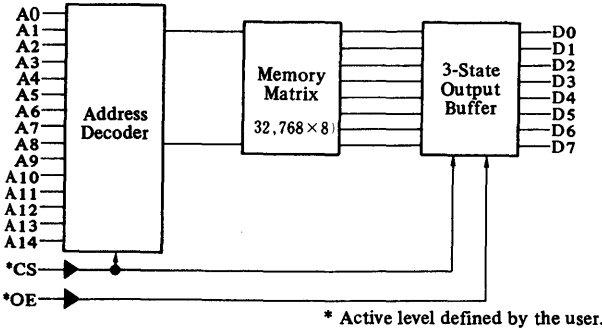
The HN613256HP is a mask-programmable, byte-organized memory designed for use in bus-organized system.
To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks nor refreshing because of static operation.
The active level of the CS and OE input, and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a power-down mode.



■ FEATURES

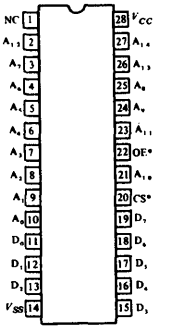
- Fully Static Operation
- Automatic Power Down
- Single +5V Power Supply
- Three-state Data Output for OR-ties
- Mask Programmable Chip Select and Output Enable
- TTL Compatible
- Maximum Access Time: 200ns
- Low Power Standby and Low Power Operation; Standby 5μW (typ.), Operation 50mW (typ.)
- Pin Compatible with EPROM

■ BLOCK DIAGRAM



* Active level defined by the user.

■ PIN ARRANGEMENT



(Top View)

* Active level can be defined by the customer.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{opr}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range (Under Bias)	T_{bias}	−20 to +85	°C

*With respect to V_{SS}

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
Input Voltage*	V_{IL}	−0.3	—	0.8	V
	V_{IH}	2.0	—	V_{CC}	V
Operating Temperature	T_{opr}	−20	—	75	°C

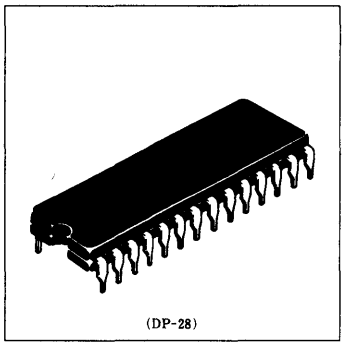
* With respect to V_{SS}.

Note)
The specifications of this device are subject to change without notice.
Please contact your nearest Hitachis Sales Dept, regarding specifications.

HN62301P — Preliminary

131,072-word×8-bit Mask Programmable Read Only Memory

The HN62301P is a mask-programmable, byte-organized memory designed for use in bus-organized systems. To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation. The Chip Enable and the memory content are defined by the user. The Chip Enable input deselects the output and puts the chip in a power-down mode.

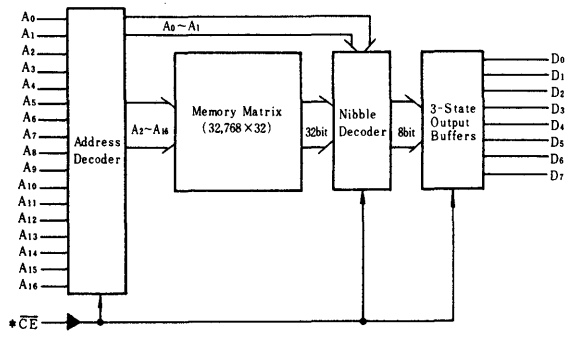


(DP-28)

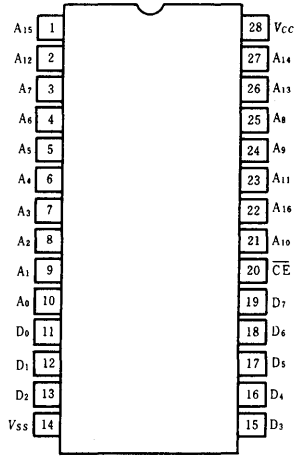
■FEATURES

- Static Operation
- Automatic Power Down
- Single +5-Volt Power Supply
- Three-State Data Output for OR-Ties
- TTL Compatible
- Maximum Access Time-350ns
- Lower Power Standby and Low Power Operation; Standby: 2mW (typ.), Operation: 75mW (typ.)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Bias Storage Temperature Range	T_{bias}	−20 to +85	°C

* With respect to V_{SS}

Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi Sales Dept, regarding specifications.

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to 70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
Input Voltage*	V_{IL}	−0.3	—	0.8	V
	V_{IH}	2.4+0.4(V_{CC}−5)	—	V_{CC}	V

* with respect to V_{ss}

■ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, Ta=0 to +70°C)

Item	Symbol	Test Conditions		min	typ***	max	Unit
Normal Operating Current	I_{CC1}*	t_{RC1}=min, V_{CC}=5.5V, I_{out}=0mA, duty=100%		—	15	50	mA
Nibble Operating Current	I_{CC2}*	t_{RC2}=min, V_{CC}=5.5V, I_{out}=0mA, duty=100%		—	5	15**	mA
Stand by Current	I_{SB}	$\overline{CE}$≧V_{CC}−0.2V, V_{CC}=5.5V		—	0.4	10	mA
Input Leakage Current	I_{LI}	V_{in}=0 to 5.5V, other 0V		−10	—	10	μA
Output Leakage Current	I_{LOH}	$\overline{CE}$=2.4V	V_{out}=2.4V	—	—	10	μA
	I_{LOL}		V_{out}=0.4V	—	—	10	μA
Output Voltage	V_{OH}	I_{out}=−205μA		2.4	—	—	V
	V_{OL}	I_{out}=3.2mA		—	—	0.4	V

* Steady state current *** V_{CC}=5V, T_a=25°C
** TBD

■CAPACITANCE (V_{CC}=5V±10%, Ta=25°C, 1MHz V_{in}=0V)

Item	Symbol	typ	max	Unit
Input Capacitance (A_0~A_{16}, $\overline{CE}$)	C_{in}	—	10	pF
Output Capacitance (D_0~D_7)	C_{out}	—	15	pF

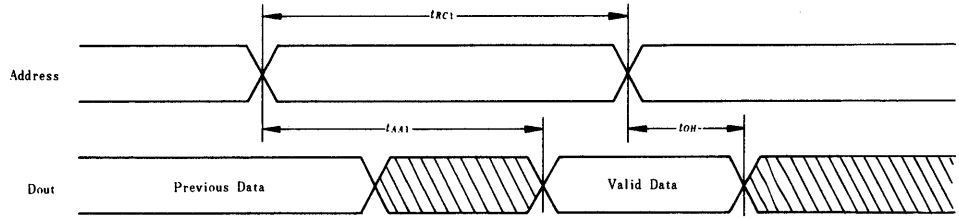
■AC CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, Ta=0 to +70°C, t_r=t_f=20ns)

Mode	Item	Symbol	min	max	Unit
Normal	Cycle Time	t_{RC1}	350	—	ns
	Address Access Time	t_{AA1}	—	350	ns
	Data Hold Time	t_{OH}	10	—	ns
$\overline{CE}$ operation	$\overline{CE}$ Access Time	t_{ACE}	—	350	ns
	$\overline{CE}$ Enable Pulse Width	t_{CE}	350	—	ns
	$\overline{CE}$ Disable Pulse Width	$t_{\overline{CE}}$	15	—	ns
	Address Set up Time	t_{AS}	0	—	ns
	Data Hold Time from $\overline{CE}$	t_{CHZ}	10	** 150	ns
	Data Set Time from $\overline{CE}$	t_{CLZ}	10	—	ns
Nibble operation***	Nibble Address Access Time*	t_{AA2}	—	100	ns
	Nibble Cycle Time	t_{RC2}	100	—	ns

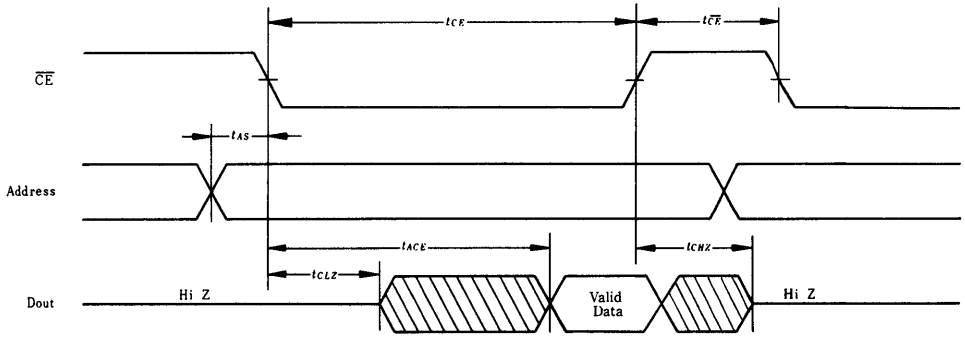
* Nibble Address A_0, A_1 **TBD
*** The specifications of this mode are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept, regarding specifications.

■ TIMMING CHART

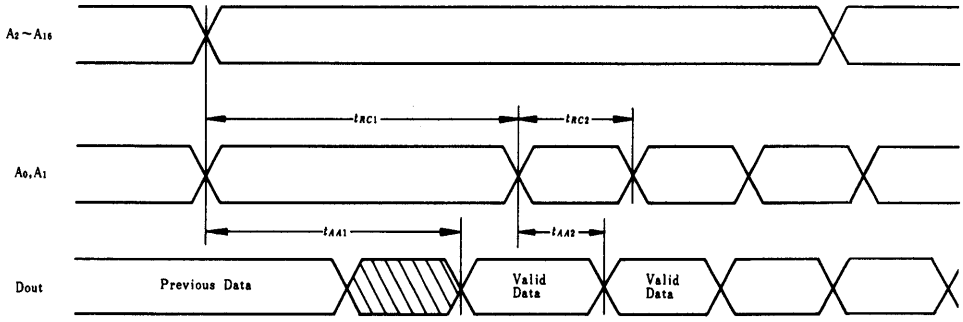
● NORMAL CYCLE ($\overline{CE}$ = Low)



● $\overline{CE}$ CYCLE

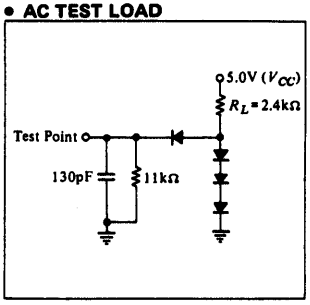


● NIBBLE CYCLE*



* Please contact your nearest Hitachi's Sales Dept. regarding specifications.

● AC TEST LOAD

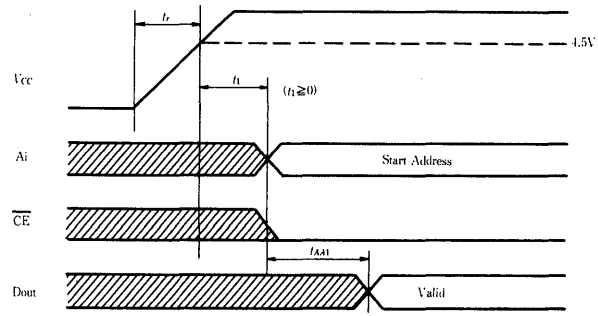


Notes) 1. $t_r = t_f = 20$ns
2. C_L includes jig capacitance.
3. All diodes are 1S2074Ⓗ.
4. Input pulse level : 0.8 to 2.4V
5. Input and output timing reference level : 1.5V

• $\overline{CE}$ DUMMY CYCLE

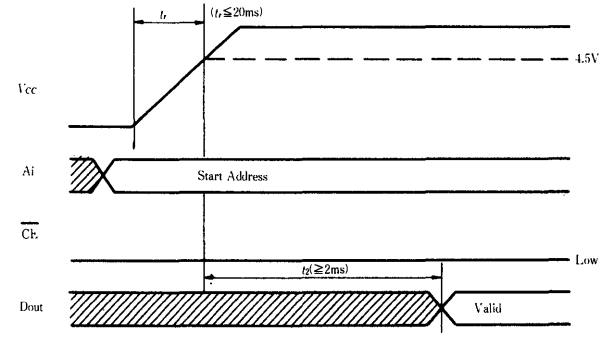
$\overline{CE}$ dummy cycle is necessary when V_{CC} rise time is longer than 20 ms.

CASE 1



(Note) 1. There is no limitation for V_{CC} rise time when at least one of addresses or $\overline{CE}$ signal is changed after power-up ($V_{CC} \geq 4.5V$). 350ns is required for the access after the transition.

CASE 2



(Note) 1. Transition of neither address nor $\overline{CE}$ is necessary for system initialization when V_{CC} rise time is less than 20ms, because of Vcc–detective-circuit-operation.
2ms is required for the access after power-up.

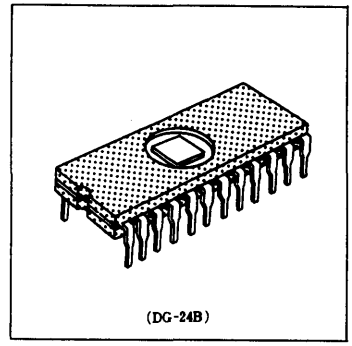
MOS PROM

HN482732AG-20, HN482732AG-25, HN482732AG-30

4096-word × 8-bit U. V. Erasable and Programmable Read Only Memory

The HN482732A is a 4096-word by 8-bit erasable and electrically programmable ROM. This device is packaged in a 24 pin dual-in-line package with transparent lid.

The transparent lid on the package allow the memory content to be erased with ultraviolet light.

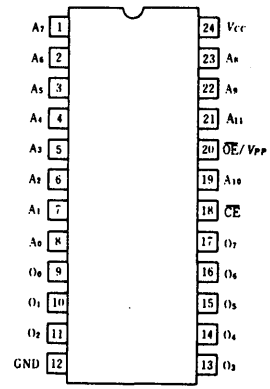


(DG-24B)

■ FEATURES

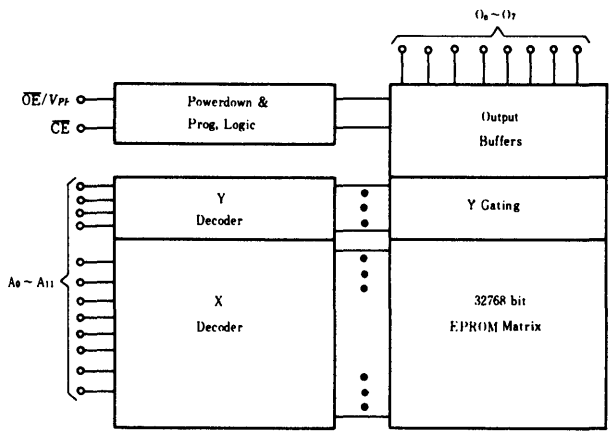
- Single Power Supply ..... +5V ±5%
- Simple Programming ..... Program Voltage: +21V D.C
  Program with one 50ms Pulse
- Static..... No clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Mode
- Access Time ..... HN482732AG-20 200ns (max)
  HN482732AG-25 250ns (max)
  HN482732AG-30 300ns (max)
- Absolute Max. Rating of Vpp Pin ... 26.5V
- Low Stand-by Current ..... 35mA (max)
- Compatible with Intel 2732A

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

MODE \ Pins	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	Outputs (9~11, 13~17)
Read	V_{IL}	V_{IL}	+5	D_{out}
Stand by	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{in}
Program Verify	V_{IL}	V_{IL}	+5	D_{out}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	℃
Storage Temperature Range	T_{stg}	−65 to +125	℃
All Input and Output Voltages*	V_{in}, V_{out}	−0.3 to +7	V
V_{PP} Voltage*	$\overline{OE}/V_{PP}$	−0.3 to 26.5	V
V_{CC} Voltage*	V_{CC}	−0.3 to +7	V

* with respect to GND

■ READ OPERATION

● D.C. AND OPERATING CHARACTERISTICS (Ta=0 to 70℃, V_{CC}=5V±5%, V_{pp}=V_{cc} ±0.6V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{IN}=5.25V	—	—	10	μA
Output Leakage Current	I_{LO}	V_{out}=5.25V	—	—	10	μA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$=V_{IH}, $\overline{OE}$=V_{IL}	—	—	35	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{OE}$=$\overline{CE}$=V_{IL}	—	—	150	mA
Input Low Voltage	V_{IL}		−0.1	—	0.8	V
Input High Voltage	V_{IH}		2.0	—	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	—	—	V

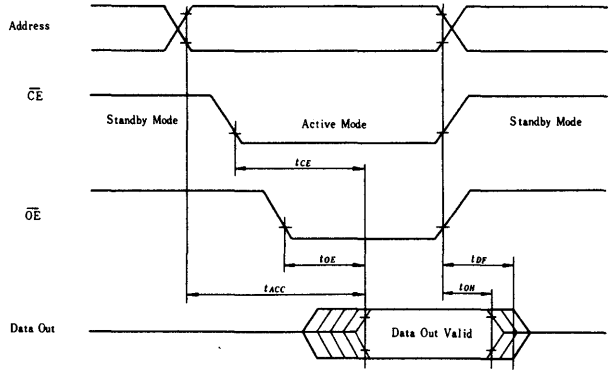
● AC CHARACTERISTICS (Ta=0 to 70℃, V_{CC}=5V±5%, V_{pp}=V_{cc} ±0.6V)

Parameter	Symbol	Test Conditions	HN482732AG-20		HN482732AG-25		HN482732AG-30		Unit
			min	max	min	max	min	max	
Address to Output Delay	t_{ACC}	$\overline{CE}$=$\overline{OE}$=V_{IL}	—	200	—	250	—	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$=V_{IL}	—	200	—	250	—	300	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$=V_{IL}	10	90	10	100	10	150	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$=V_{IL}	0	80	0	90	0	130	ns
Address to Output Hold	t_{OH}	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	—	0	—	0	—	ns

● SWITCHING CHARACTERISTICS

Test Conditions

Input Pulse Level: . . . . . 0.8V to 2.2V
Input Rise and Fall Times: . . . . . ≦ 20ns
Output Load: . . . . . 1 TTL Gate + 100PF
Reference Level for Measuring Timing . . . . . Inputs, 1V and 2V, Outputs; 0.8V and 2V



● CAPACITANCE (Ta=25℃, f=1MHz)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Capacitance (Except $\overline{OE}/V_{PP}$)	C_{IN1}	V_{IN}=0V	—	—	6	pF
$\overline{OE}/V_{PP}$ Input Capacitance	C_{IN2}	V_{IN}=0V	—	—	20	pF
Output Capacitance	C_{out}	V_{out}=0V	—	—	12	pF

■ PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{IN}=V_{IL}$ or V_{IH}	—	—	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH}=−400μA	2.4	—	—	V
V_{CC} Supply Current	I_{CC}		—	—	150	mA
Input Low Level	V_{IL}		−0.1	—	0.8	V
Input High Level (All Inputs Except $\overline{OE}/V_{PP}$)	V_{IH}		2.0	—	V_{CC}+1	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{PP}$	—	—	30	mA

● AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
$\overline{OE}$ Hold Time	t_{OEH}		2	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
Chip Enable to Output Float Delay*	t_{DF}		0	—	130	ns
Data Valid from $\overline{CE}$	t_{DV}	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IL}$	—	—	1	μs
$\overline{CE}$ Pulse Width During Programming	t_{PW}		45	50	55	ms
$\overline{OE}$ Pulse Rise Time During Programming	t_{PRT}		50	—	—	ns
V_{PP} Recovery Time	t_{VR}		2	—	—	μs

* t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

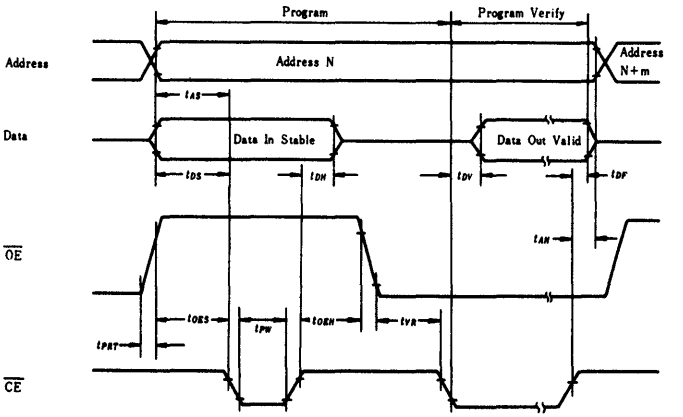
● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level ..... 0.8V to 2.2V

Input Rise and Fall Time ..... ≦ 20ns

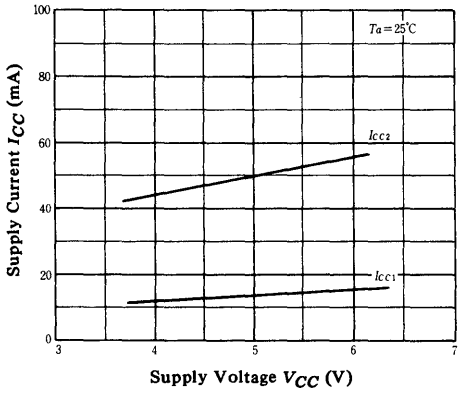
Reference Level for Measuring Timing: ..... Inputs 1V and 2V; Outputs 0.8V and 2V



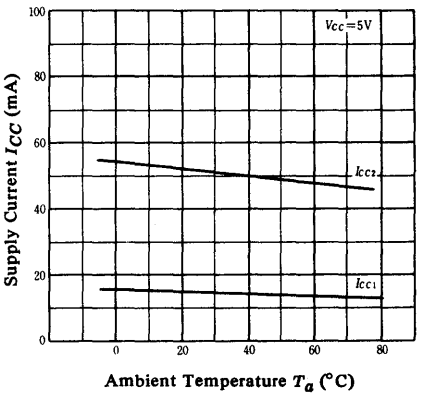
● ERASE

Erasure of HN482732A is performed by exposure to ultraviolet light of 2537Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W-sec/cm^2

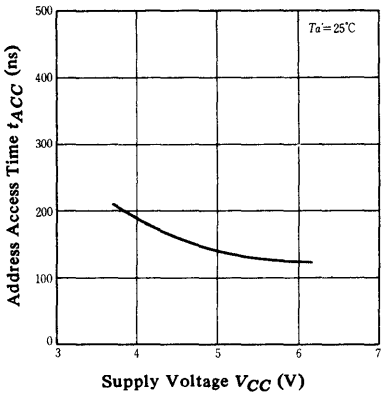
SUPPLY CURRENT vs. SUPPLY VOLTAGE



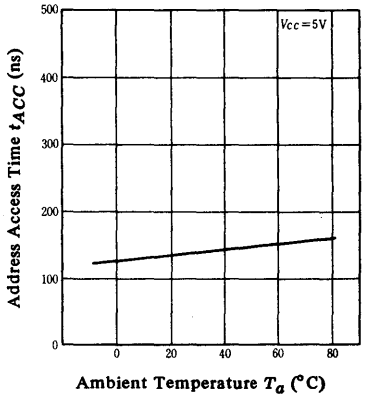
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE

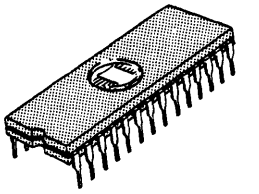


HN482764G,HN482764G-2, HN482764G-3

8192-word x 8-bit UV Erasable and Programmable Read Only Memory

The HN482764 is a 8192 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a 28 pin dual-in-line package with transparent lid. The transparent lid on the package allows the memory content to be erased with ultraviolet light.

HN482764G, HN482764G-2
HN482764G-3

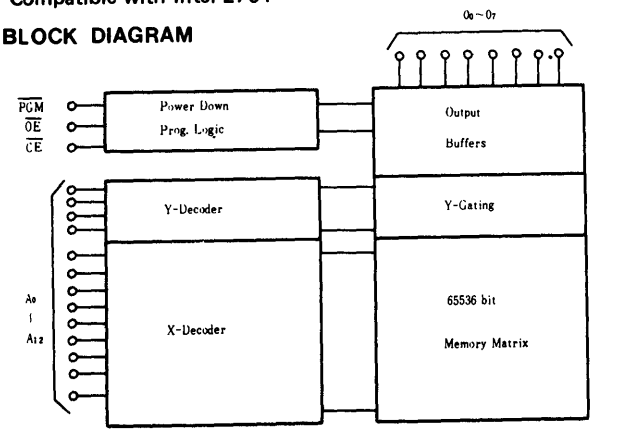


(DG-28)

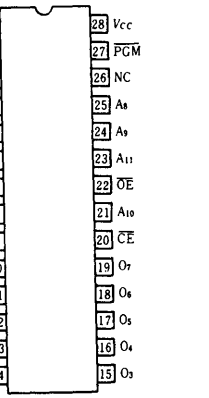
■ FEATURES

- Single Power Supply . . . . . +5V ± 5%
- Simple Programming . . . . . Program Voltage: +21V D.C.
  Program with one 50ms Pulse
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Mode.
- Access Time . . . . . HN482764G-2 200ns max
  HN482764G 250ns max
  HN482764G-3 300ns max
- High Performance Programming Available
- Low Standby Current . . . . . 35mA max.
- Compatible with Intel 2764

■ BLOCK DIAGRAM



■ PIN ARRANGMENT



(Top View)

■ MODE SELECTION

Mode \ Pins	CE (20)	OE (22)	PGM (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Stand-by	V_{IH}	×	×	V_{CC}	V_{CC}	High Z
Program	V_{IL}	×	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	×	×	V_{PP}	V_{CC}	High Z

× : don't care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C
All Input and Output Voltage*	V_T	−0.6 to +7	V
V_{PP} Voltage	V_{PP}	−0.6 to +26.5	V

* : with respect to GND

HITACHI

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{CC}=5.25V, V_{in}=5.25V	—	—	10	μA
Output Leakage Current	I_{LO}	V_{CC}=5.25V, V_{out}=5.25V/0.45V	—	—	10	μA
V_{PP} Current	I_{PP1}	V_{PP}=V_{CC}+0.6V	—	—	15	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$=V_{IH}	—	—	35	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$=$\overline{OE}$=V_{IL}	—	40	100	mA
Input Low Voltage	V_{IL}		−0.1	—	0.8	V
Input High Voltage	V_{IH}		2.0	—	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	—	—	V

● AC CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

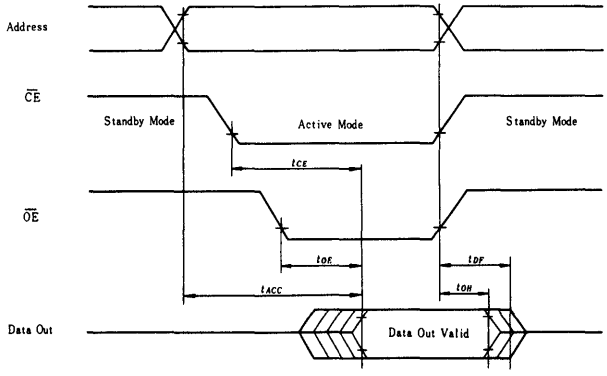
Parameter	Symbol	Test Conditions	HN482764G-2		HN482764G		HN482764G-3		Unit
			min	max	min	max	min	max	
Address to Output Delay	t_{ACC}	$\overline{CE}$=$\overline{OE}$=V_{IL}	—	200	—	250	—	300	ns
CE to Output Delay	t_{CE}	$\overline{OE}$=V_{IL}	—	200	—	250	—	300	ns
OE to Output Delay	t_{OE}	$\overline{CE}$=V_{IL}	10	80	10	100	10	150	ns
OE High to Output Float	t_{DF}	$\overline{CE}$=V_{IL}	0	70	0	90	0	130	ns
Address to Output Hold	t_{OH}	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	—	0	—	0	—	ns

Note : t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Levels:	0.8V to 2.2V
Input Rise and Fall Time:	≤ 20ns
Output Load:	1TTL Gate + 100pF
Reference Level for Measuring Timing:	Inputs; 1V and 2V Output; 0.8V and 2.0V



● CAPACITANCE (Ta=25°C, f=1MHz)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	—	4	6	pF
Output Capacitance	C_{out}	V_{out}=0V	—	8	12	pF

■ PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS (Ta=25℃±5℃, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{in}=5.25V	—	—	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH}=−400μA	2.4	—	—	V
V_{CC} Current (Active)	I_{CC2}		—	—	100	mA
Input Low Level	V_{IL}		−0.1	—	0.8	V
Input High Level	V_{IH}		2.0	—	V_{CC}+1	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$=$\overline{PGM}$=V_{IL}	—	—	30	mA

● AC PROGRAMMING CHARACTERISTICS (Ta=25℃±5℃, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

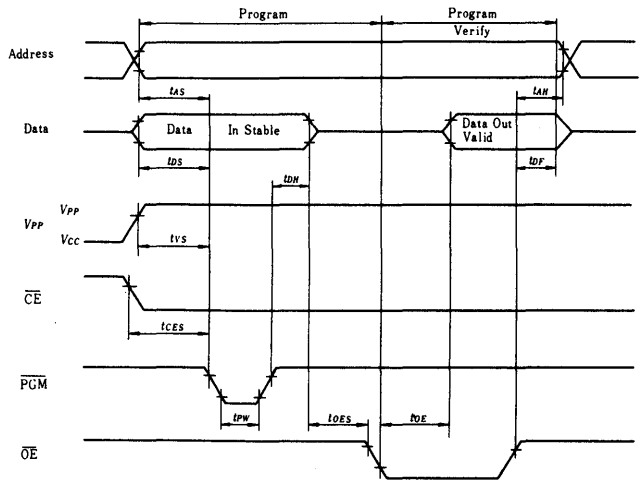
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VS}		2	—	—	μs
$\overline{PGM}$ Pulse Width During Programming	t_{PW}		45	50	55	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}		—	—	150	ns

Note : t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

Test Condition

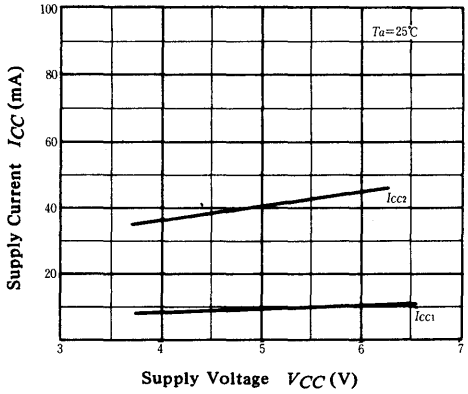
Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Time:	≤ 20 ns
Reference Level for Measuring Timing:	Input; 1V and 2V
	Output; 0.8V and 2V



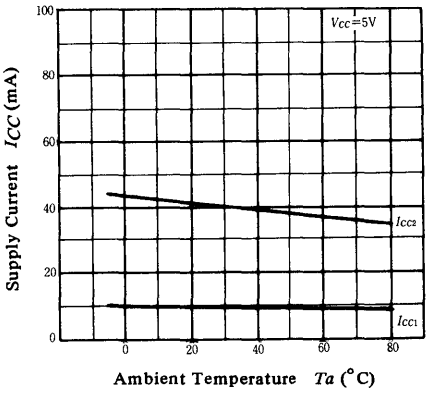
■ ERASE

Erasure of HN482764 is performed by exposure to Ultraviolet light of 2537Å, and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W • sec/cm²

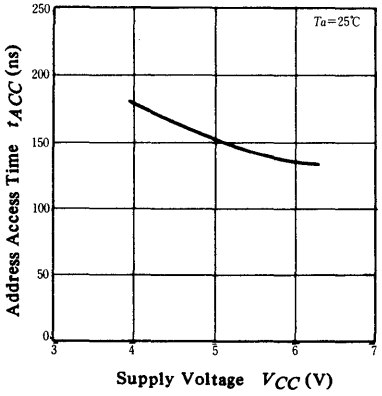
SUPPLY CURRENT VS. SUPPLY VOLTAGE



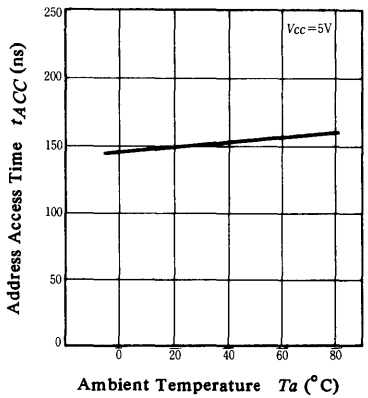
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME VS. SUPPLY VOLTAGE

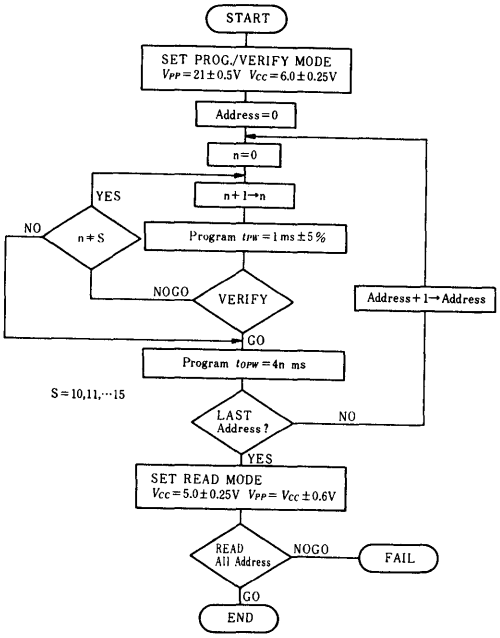


ADDRESS ACCESS TIME VS. AMBIENT TEMPERATURE



■ HIGH PERFOMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

● AC PROGRAMMING CHARACTERISTICS (Ta=25℃±5℃, V_{CC}=6V±0.25V, V_{PP}=21V±0.5V)

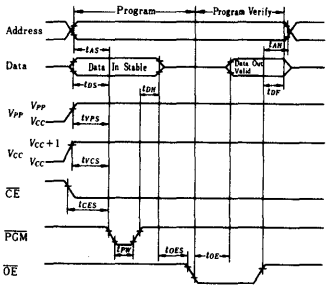
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay*	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VPS}		2	—	—	μs
V_{CC} Setup Time	t_{VCS}		2	—	—	μs
$\overline{PGM}$ Pulse Width during Initial Program	t_{PW}		0.95	1.0	1.05	ms
$\overline{PGM}$ Pulse Width during Over Program**	t_{OPW}		3.8	—	63	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}		—	—	150	ns

Notes) * t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
** t_{OPW} is defined as mentioned in flort chart.

● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Time:	≤ 20 ns
Reference Level for Measuring Timing:	Input; 1V and 2V
	Output; 0.8V and 2V

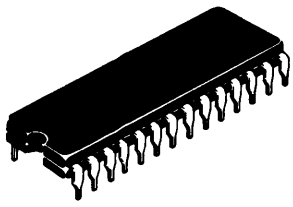


HN482764P-3

8192-word x 8-bit One Time Electrically Programmable ROM

The HN482764P-3 is a 8192 word by 8-bit one time electrically programmable ROM. Initially, all bits of the HN482764P-3 are in the "1" state (Output High). Data is introduced by selectively programming "0" into the desired bit locations. This device is packaged in a 28 pin, dual-in-line plastic package. Therefore, this device can not be re-written.

HN482764P-3

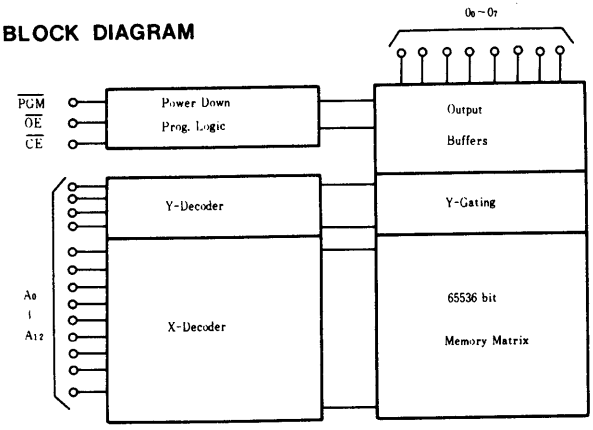


(DP-28)

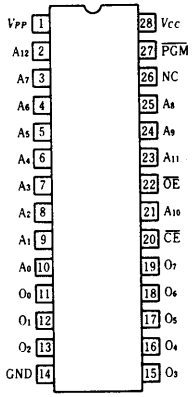
■ FEATURES

- Spring Power Supply . . . . . +5V ±5%
- Simple Programming . . . . Program Voltage: +21V D.C.
  Program with one 50ms Pulse
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Mode
- Access Time . . . . . 300ns max.
- Low Standby Current . . . . . 35mA max.
- Compatible with Intel P2764

■ BLOCK DIAGRAM



■ PIN ARRANGMENT



(Top View)

■ MODE SELECTION

Mode \ Pins	CE (20)	OE (22)	PGM (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Stand-by	V_{IH}	×	×	V_{CC}	V_{CC}	High Z
Program	V_{IL}	×	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	×	×	V_{PP}	V_{CC}	High Z

× : don't care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
All Input and Output Voltage*	V_T	−0.6 to +7	V
V_{PP} Voltage	V_{PP}	−0.6 to +26.5	V

* with respect to GND

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC} ± 0.6V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.25V, V_{in} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{CC} = 5.25, V_{out} = 5.25V/0.45V	–	–	10	μA
V_{PP} Current	I_{PP1}	V_{PP} = V_{CC} + 0.6V	–	–	15	mA
V_{CC} Current (Standby)	I_{CC1}	CE = V_{IH}	–	–	35	mA
V_{CC} Current (Active)	I_{CC2}	CE = OE = V_{IL}	–	40	100	mA
Input Low Voltage	V_{IL}		-0.1	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage	V_{OH}	I_{OH} = -400μA	2.4	–	–	V

● AC CHARACTERISTICS (T_a = 5V ± 5%, V_{PP} = V_{CC} ± 0.6V, T_a = 0 to +70°C)

Parameter	Symbol	Test Conditions	min	max	Unit
Address to Output Delay	t_{ACC}	CE = OE = V_{IL}	–	300	ns
CE to Output Delay	t_{CE}	OE = V_{IL}	–	300	ns
OE to Output Delay	t_{OE}	CE = V_{IL}	10	150	ns
OE High to Output Float*	t_{DF}	CE = V_{IL}	0	130	ns
Address to Output Hold	t_{OH}	CE = OE = V_{IL}	0	–	ns

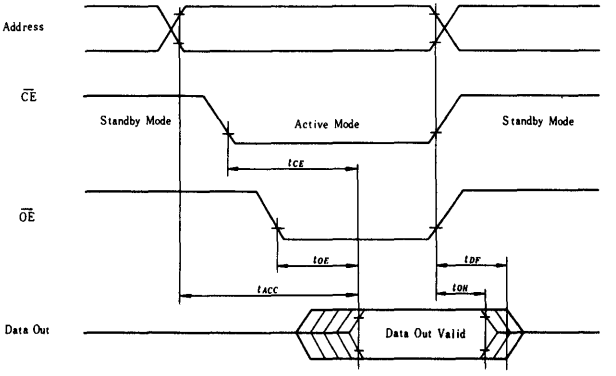
* t_{DF} defines the time at which the output achives the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Levles: 0.8V to 2.2V
Input Rise and Fall Times: ≦ 20ns.
Output Load: 1TTL Gate + 100pF

Reference Level for Measuring Timing:
Inputs ; 1V and 2V
Outputs; 0.8V and 2V



● CAPACITANCE (Ta = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	4	6	pF
Output Capacitance	C_{out}	V_{out} = 0V	–	8	12	pF

■ PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS (Ta=25℃±5℃, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{in}=5.25V	—	—	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH}=−400μA	2.4	—	—	V
V_{CC} Current (Active)	I_{CC2}		—	—	150	mA
Input Low Level	V_{IL}		−0.1	—	0.8	V
Input High Level	V_{IH}		2.0	—	V_{CC}+1	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$=$\overline{PGM}$=V_{IL}	—	—	30	mA

● AC PROGRAMMING CHARACTERISTICS (Ta=25℃±5℃, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

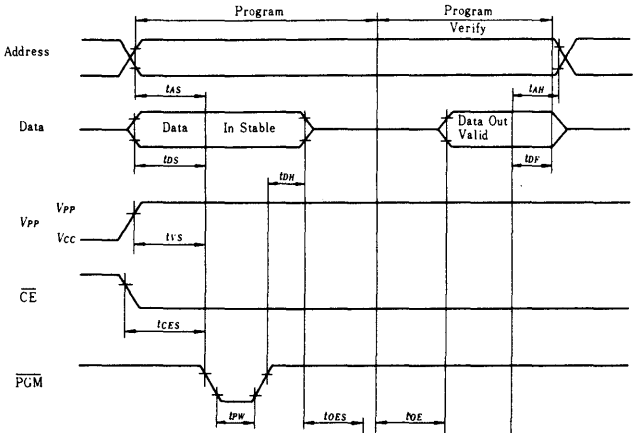
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay	t_{DF}		0	—	1 0	ns
V_{PP} Setup Time	t_{VS}		2	—	—	μs
$\overline{PGM}$ Pulse Width During Programming	t_{PW}		45	50	55	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}		—	—	150	ns

Note : t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

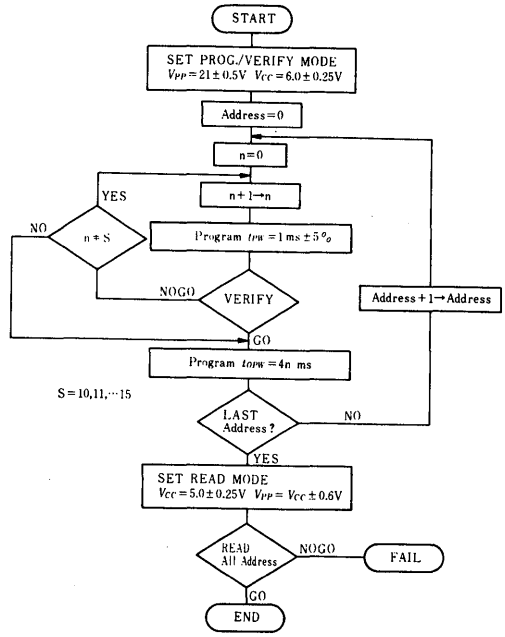
Test Condition

Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Time:	≤ 20 ns
Reference Level for Measuring Timing:	Input; 1V and 2V Output; 0.8V and 2V



■ HIGH PERFOMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

● AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=21V±0.5V)

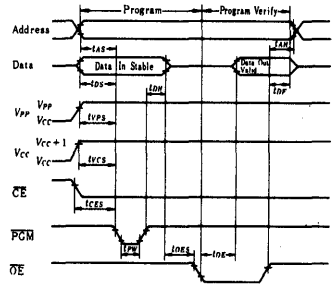
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay*	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VPS}		2	—	—	μs
V_{CC} Setup Time	t_{VCS}		2	—	—	μs
$\overline{PGM}$ Pulse Width during Initial Program	t_{PW}		0.95	1.0	1.05	ms
$\overline{PGM}$ Pulse Width during Over Program**	t_{OPW}		3.8	—	63	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}		—	—	150	ns

Notes) * t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
** t_{OPW} is defined as mentioned in flort chart.

● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Time:	≤ 20 ns
Reference Level for Measuring Timing:	Input; 1V and 2V
	Output; 0.8V and 2V

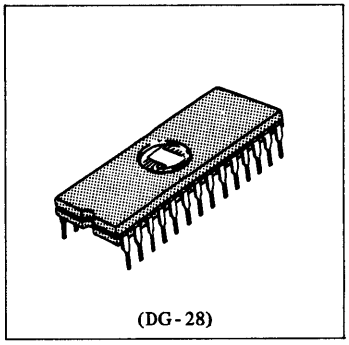


HN27C64G-15, HN27C64G-20, HN27C64G-25, HN27C64G-30

8192-word x 8-bit U.V. Erasable and Programmable CMOS ROM

The CMOS EPROM HN27C64 is a 8192-word by 8-bit erasable and electrically programmable ROM. This device is packaged in a 28-pin, dual-in-line package with transparent lid.

The transparent lid allows the memory content to be erased with ultraviolet light, where by a new pattern can then be written into the device.

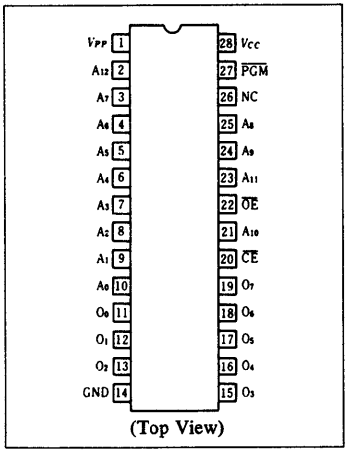


(DG-28)

■ FEATURES

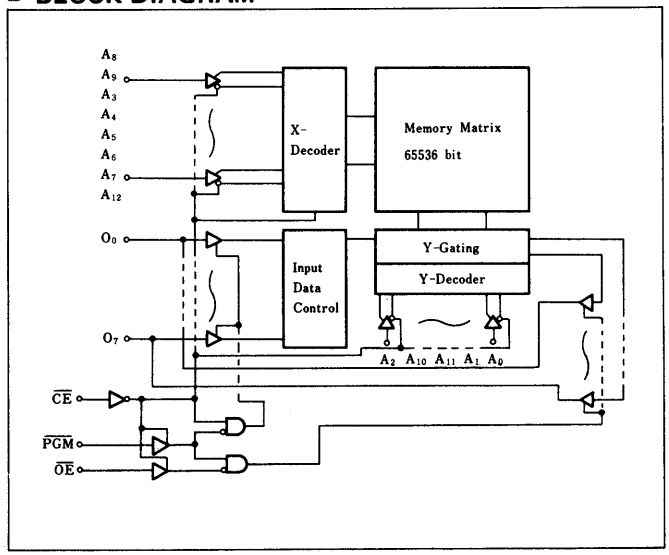
- Low Power Dissipation ..... 40mW/MHz max. (Active Mode)
  550μW max. (Stand by Mode)
- Access Time ..... 150ns max. (HN27C64G-15)
  200ns max. (HN27C64G-20)
  250ns max. (HN27C64G-25)
  300ns max. (HN27C64G-30)
- Single Power Supply ..... +5V±10%
- Simple Programming ..... Program Voltage; +21V D.C.
  Program with One 50ms Pulse
- Support High Performance Programming
- Static ..... No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Fully Decoded On-chip Address Decode
- Compatible with Intel 2764

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Stand-by	V_{IH}	×	×	V_{CC}	V_{CC}	High Z
Program	V_{IL}	×	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	×	×	V_{PP}	V_{CC}	High Z

× : don't care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
All Input and Output Voltage*	V_T	−1.0**~ +7.0	V
V_{CC} Voltage*	V_{CC}	−0.6~ + 7.0	V
V_{PP} Voltage*	V_{PP}	−0.6~ + 25	V
Operating Temperature Range	T_{opr}	0~ + 70	°C
Storage Temperature Range	T_{stg}	−65~ + 125	°C

* With respect to GND
**Pulse Width: 50ns, DC: −0.5V

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS (Ta=0~ + 70°C, V_{CC}=5V ± 10%, $V_{PP}=V_{CC}$ ±0.6V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{CC}=5.5V, V_{in}=GND to V_{CC}	–	–	2	μA
Output Leakage Current	I_{LO}	V_{CC}=5.5V, V_{out}=GND to V_{CC}	–	–	2	μA
V_{PP} Current	I_{PP1}	$V_{PP}=V_{CC}$ + 0.6V	–	1	100	μA
V_{CC} Current (Stand-by)	I_{SB1}	$\overline{CE}=V_{IH}$	–	–	1	mA
	I_{SB2}	$\overline{CE}=V_{CC}$ ± 0.3V	–	1	100	μA
V_{CC} Current (Active)	I_{CC1}	$\overline{CE}=V_{IL}$, I_{out}=0 mA	–	–	30	mA
	I_{CC2}	f=5MHz, I_{out}=0 mA	–	–	30	mA
Input Voltage	V_{IL}		−1.0*	–	0.8	V
	V_{IH}		2.2	–	V_{CC} + 1.0	V
Output Voltage	V_{OL}	I_{OL}=2.1 mA	–	–	0.45	V
	V_{OH}	I_{OH} = −400μA	2.4	–	–	V

*Pulse Width: 50ns, DC: V_{IL} min = −0.3V

● AC CHARACTERISTICS (Ta=0~ + 70°C, V_{CC}=5V ± 10%, $V_{PP}=V_{CC}$ ±0.6V)

Parameter	Symbol	Test Condition	HN27C64G-15		HN27C64G-20		HN27C64G-25		HN27C64G-30		Unit
			min	max	min	max	min	max	min	max	
Address to Output Delay	t_{ACC}	$\overline{CE}=\overline{OE}=V_{IL}$, $\overline{PGM}=V_{IH}$	–	150	–	200	–	250	–	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}=V_{IL}$, $\overline{PGM}=V_{IH}$	–	150	–	200	–	250	–	300	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$	10	60	10	70	10	100	10	150	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$	0	50	0	60	0	90	0	130	ns
Address to Output Hold	t_{OH}	$\overline{CE}=\overline{OE}=V_{IL}$, $\overline{PGM}=V_{IH}$	0	–	0	–	0	–	0	–	ns

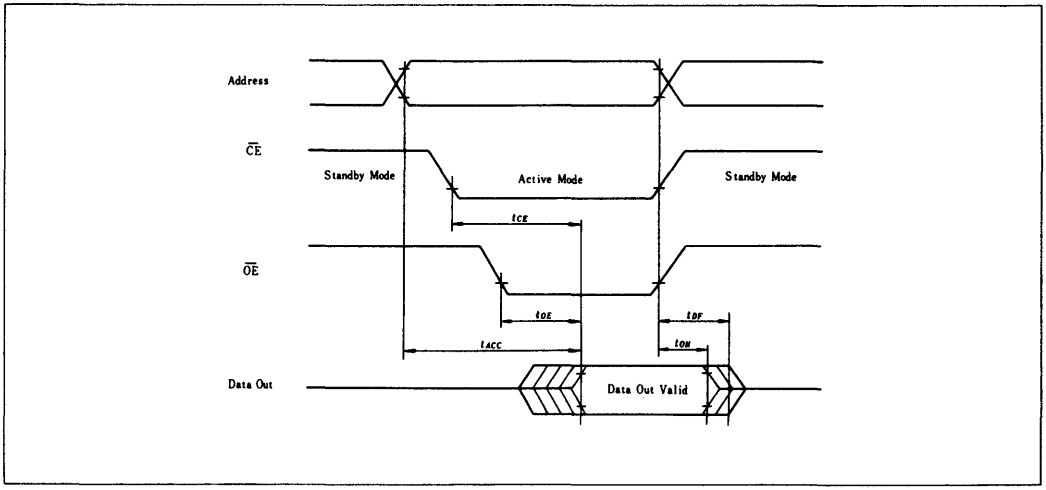
● CAPACITANCE (Ta=25°C, f=1MHz)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	4	6	pF
Output Capacitance	C_{out}	V_{out} = 0V	–	8	12	pF

• SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Levels:	0.8V to 2.2V
Input Rise and Fall Time:	≤20ns
Output Load:	1TTL + 100pF
Reference Level for Measuring Timing:	Input; 1V and 2V Output; 0.8V and 2V



■ PROGRAMMING OPERATION

• DC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{IN}=5.25V/0.45V	–	–	2	μA
Output Low Voltage During Verify	V_{OL}	I_{OL}=2.1 mA	–	–	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH}=–400 μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC}		–	–	30	mA
Input Low Level	V_{IL}		–0.1	–	0.8	V
Input High Level	V_{IH}		2.2	–	V_{CC}+1.0	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$=$\overline{PGM}$=V_{IL}	–	–	30	mA

Notes) 1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 25V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}= 21V.
4. Do not alter V_{PP} either V_{IL} to 21V or 21V to V_{IL} when $\overline{CE}$=$\overline{PGM}$=Low.

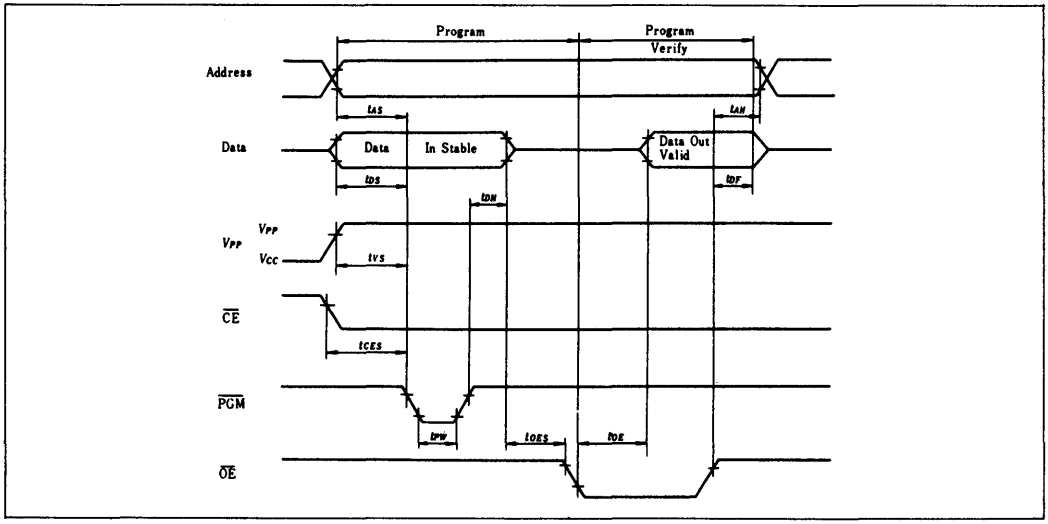
• AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	–	–	μs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ to Output Float Delay	t_{DF}		0	–	130	ns
V_{PP} Setup Time	t_{VS}		2	–	–	μs
$\overline{PGM}$ Pulse Width During Programming	t_{PW}		25	50	55	ms
$\overline{CE}$ Setup Time	t_{CES}		2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}		–	–	150	ns

● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Time:	≤20ns
Reference Level for Measuring Timing:	Input; 1V and 2V
	Output; 0.8V and 2V

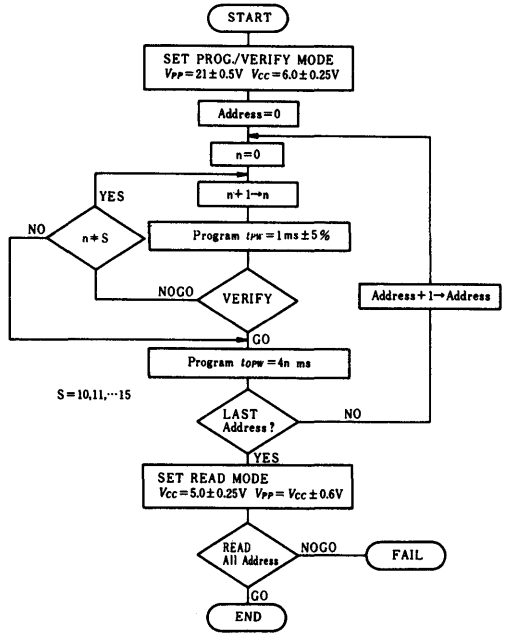


■ ERASE

Erasure of HN27C64 is performed by exposure to ultraviolet light of 2537Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W-sec/cm^2.

■ HIGH PERFOMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

• AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=21V±0.5V)

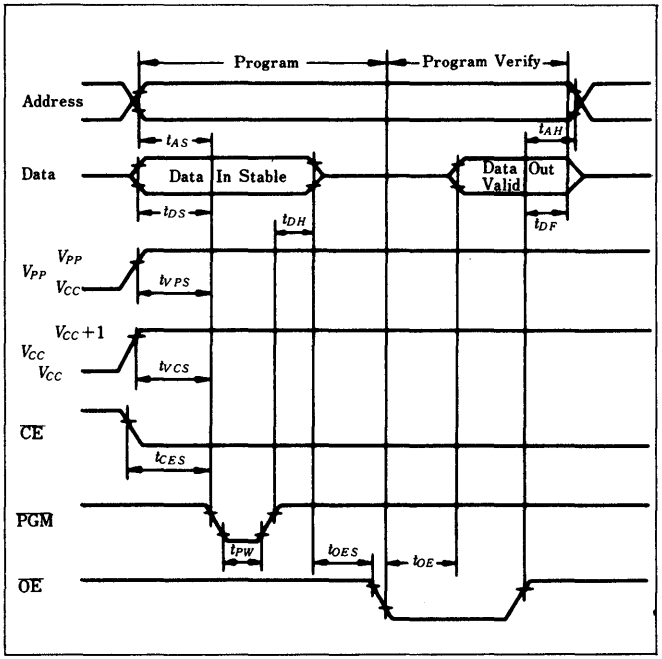
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay*	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VPS}		2	—	—	μs
V_{CC} Setup Time	t_{VCS}		2	—	—	μs
$\overline{PGM}$ Pulse Width during Initial Program	t_{PW}		0.95	1.0	1.05	ms
$\overline{PGM}$ Pulse Width during Over Program**	t_{OPW}		3.8	—	63	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}		—	—	150	ns

Notes) * t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
** t_{OPW} is defined as mentioned in flort chart.

• SWITCHING CHARACTERISTICS

Test Condition

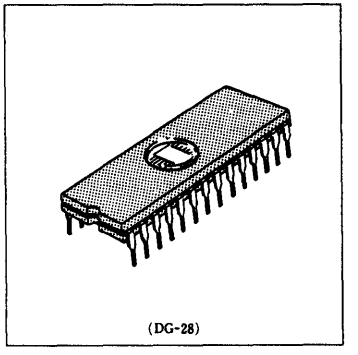
Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Time:	≤20ns
Reference Level for Measuring Timing:	Input; 1V and 2V Output; 0.8V and 2V



HN4827128G-25, HN4827128G-30, HN4827128G-45

16384-Word x 8-bit UV Erasable and Programmable Read Only Memory

The HN4827128 is a 16384 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

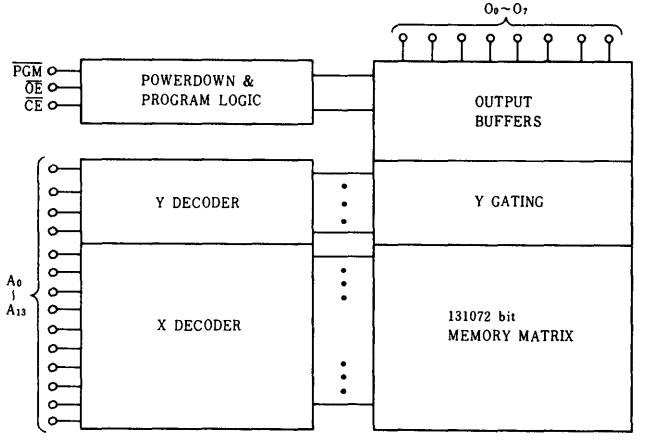


(DG-28)

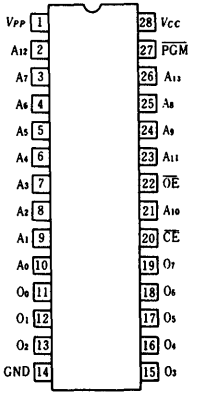
■FEATURES

- Single Power Supply ..... +5V ± 5%
- Simple Programming ..... Program Voltage: +21V DC
  Program with One 50ms Pulse
- Static ..... No Clocks Required
  Inputs and Outputs TTL Compatible During Both Read and Program Mode.
- Access Time 250ns/300ns/450ns
- Absolute Max. Rating of Vpp Pin 26.5V
- Low Stand-by Current 35mA
- High Performance Programming Available
- Compatible with INTEL 27128

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■MODE SELECTION

MODE \ Pins	CE (20)	OE (22)	PGM (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Stand by	V_{IH}	×	×	V_{CC}	V_{CC}	High Z
Program	V_{IL}	×	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	×	×	V_{PP}	V_{CC}	High Z

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C
All Input and Output Voltages*	V_{IN}, V_{out}	−0.3 to +7	V
V_{PP} Voltage*	V_{PP}	−0.6 to +26.5	V
V_{CC} Voltage*	V_{CC}	−0.6 to +7	V

* with respect to GND

■READ OPERATION

●DC AND OPERATING CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{CC}=5.25V, V_{IN}=5.25V	—	—	10	μA
Output Leakage Current	I_{LO}	V_{CC}=5.25V, V_{out}=5.25V/0.45V	—	—	10	μA
V_{PP} Current	I_{PP1}	V_{PP}=V_{CC}+0.6V	—	—	5	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$=V_{IH}	—	—	35	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$=$\overline{OE}$=V_{IL}	—	60	100	mA
Input Low Voltage	V_{IL}		−0.1	—	0.8	V
Input High Voltage	V_{IH}		2.0	—	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	—	—	V

●AC CHARACTERISTICS (Ta=0 to 70°C, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

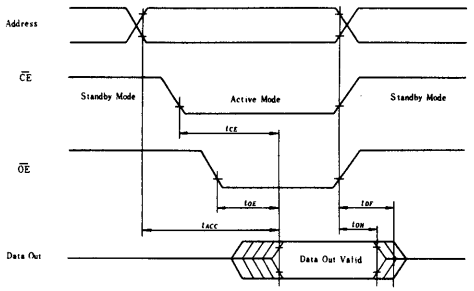
Parameter	Symbol	Test Condition	HN4827128G-25		HN4827128G-30		HN4827128G-45		Unit
			min	max	min	max	min	max	
Address to Output Delay	t_{ACC}	$\overline{CE}$=$\overline{OE}$=V_{IL}	—	250	—	300	—	450	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$=V_{IL}	—	250	—	300	—	450	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$=V_{IL}	—	100	—	120	—	150	ns
$\overline{OE}$ High to Output Float	t_{DF}*	$\overline{CE}$=V_{IL}	0	85	0	105	0	130	ns
Address to Output Hold	t_{OH}	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	—	0	—	0	—	ns

* t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

●SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Levels:	0.8V to 2.2V
Input Rise and Fall Time:	≤ 20 ns
Output Load:	1 TTL Gate + 100 pF
Reference Level for Measuring Timing:	Inputs; 1V and 2V
	Outputs; 0.8V and 2.0V



●CAPACITANCE (Ta=25°C, f= 1 MHz)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	—	4	6	pF
Output Capacitance	C_{out}	V_{out}=0V	—	8	12	pF

■PROGRAMMING OPERATION

●DC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{IN}=5.25V	—	—	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH}=−400μA	2.4	—	—	V
V_{CC} Current (Active)	I_{CC2}		—	—	100	mA
Input Low Level	V_{IL}		−0.1	—	0.8	V
Input High Level	V_{IH}		2.0	—	V_{CC}+1	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$=$\overline{PGM}$=V_{IL}	—	—	30	mA

●AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VS}		2	—	—	μs
$\overline{PGM}$ Pulse Width During Programming	t_{PW}		45	50	55	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}		—	—	150	ns

Note : t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

●SWITCHING CHARACTERISTICS

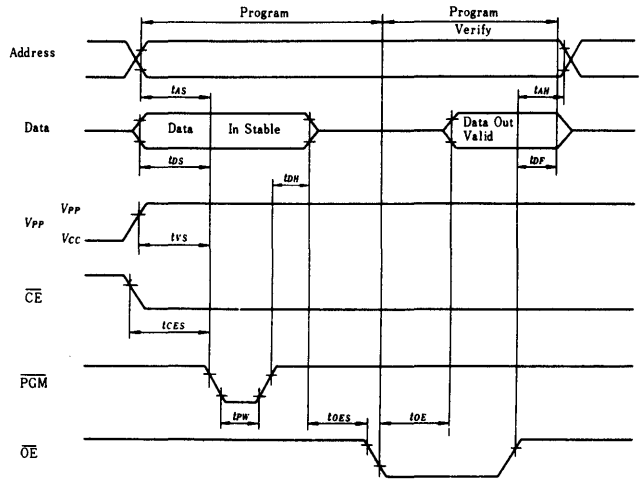
Test Condition

Input Pulse Level: 0.8V to 2.2V

Input Rise and Fall Time: ≤ 20 ns

Reference Level for Measuring Timing: Input; 1V and 2V

Output; 0.8V and 2V

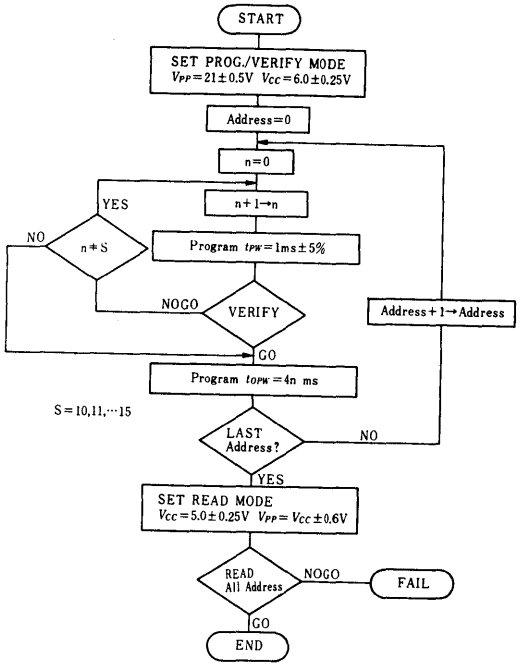


●ERASE

Erasure of HN4827128 is performed by exposure to ultraviolet light of 2537Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15 W·sec/cm^2.

■HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flow chart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

●AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=21V±0.5V)

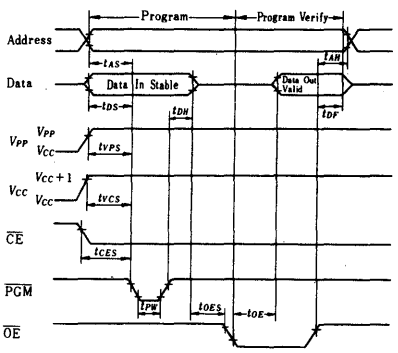
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay*	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VPS}		2	—	—	μs
V_{CC} Setup Time	t_{VCS}		2	—	—	μs
$\overline{PGM}$ Pulse Width during Initial Program	t_{PW}		0.95	1.0	1.05	ms
$\overline{PGM}$ Pulse Width during Over Program**	t_{OPW}		3.8	—	63	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}		—	—	150	ns

* t_{DF} defines the time at which the output achieves the open circuit conditions and is not referenced to output voltage levels.
** t_{OPW} is defined as mentioned in flow chart.

●SWITCHING CHARACTERISTICS

Test Condition

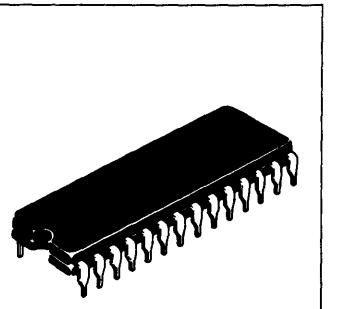
Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Time:	≤ 20 ns
Reference Level for Measuring Timing:	Input; 1V and 2V
	Output; 0.8V and 2V



HN4827128P-30 — Preliminary

16384-word x 8-bit One Time Electrically Programmable ROM

The HN4827128P-30 is a 16384-word by 8-bit one time electrically programmable ROM. Initially, all bits of the HN4827128P-30 are in the "1" state (Output High).
Data is introduced by selectively programing "0" into the desired bit locations. This device is packaged in a 28 pin, dual-in-line plastic package. Therefore, this device can not be re-written.

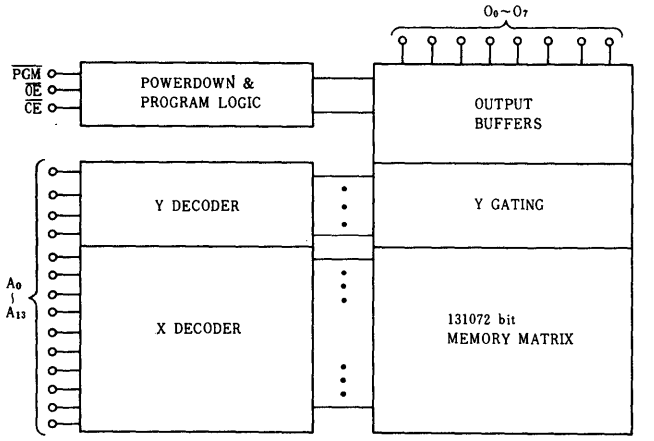


(DP-28)

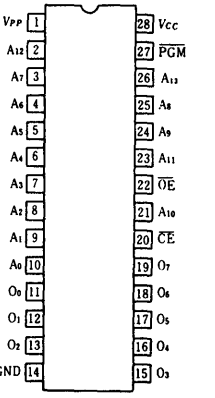
■ FEATURES

- Single Power Supply . . . . . +5V ±5%
- Simple Programming . . . . . Program Voltage: +21V DC
  Program with One 50ms Pulse
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Mode.
- Access Time 300ns
- Absolute Max. Rating of V_{PP} Pin 26.5V
- Low Stand-by Current 35mA
- High Performance Programming Available
- Compatible with Intel 27128

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ MODE SELECTION

MODE \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Stand by	V_{IH}	×	×	V_{CC}	V_{CC}	High Z
Program	V_{IL}	×	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	×	×	V_{PP}	V_{CC}	High Z

× : Don't care

Note: The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
All Input and Output Voltages*	V_{IN}, V_{out}	−0.3 to +7	V
V_{PP} Voltage*	V_{PP}	−0.3 to +26.5	V
V_{CC} Voltage*	V_{CC}	−0.3 to +7	V

* with respect to GND

■READ OPERATION

● DC AND OPERATING CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC} ± 0.6V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{CC}=5.25V, V_{IN}=5.25V	—	—	10	μA
Output Leakage Current	I_{LO}	V_{CC}=5.25V, V_{out}=5.25V/0.45V	—	—	10	μA
V_{PP} Current	I_{PP1}	V_{PP}=V_{CC}+0.6V	—	—	5	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$=V_{IH}	—	—	35	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$=$\overline{OE}$=V_{IL}	—	60	100	mA
Input Low Voltage	V_{IL}		−0.1	—	0.8	V
Input High Voltage	V_{IH}		2.0	—	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	—	—	V

● AC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC} ± 0.6V)

Parameter	Symbol	Test Conditions	min	max	Unit
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	300	ns
CE to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	–	300	ns
OE to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	–	120	ns
OE High to Output Float*	t_{DF}	$\overline{CE}$ = V_{IL}	0	105	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	ns

* t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

●SWITCHING CHARACTERISTICS

Test Condition

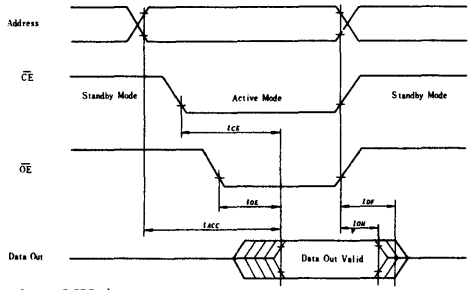
Input Pulse Levels: 0.8V to 2.2V

Input Rise and Fall Time: ≤ 20 ns

Output Load: 1 TTL Gate + 100 pF

Reference Level for Measuring Timing: Inputs; 1V and 2V

Outputs; 0.8V and 2.0V



●CAPACITANCE (Ta=25°C, f= 1 MHz)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	—	4	6	pF
Output Capacitance	C_{out}	V_{out}=0V	—	8	12	pF

■PROGRAMMING OPERATION

●DC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{IN}=5.25V	—	—	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH}=−400μA	2.4	—	—	V
V_{CC} Current (Active)	I_{CC2}		—	—	100	mA
Input Low Level	V_{IL}		−0.1	—	0.8	V
Input High Level	V_{IH}		2.0	—	V_{CC}+1	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$=$\overline{PGM}$=V_{IL}	—	—	30	mA

●AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VS}		2	—	—	μs
$\overline{PGM}$ Pulse Width During Programming	t_{PW}		45	50	55	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}		—	—	150	ns

Note: t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

●SWITCHING CHARACTERISTICS

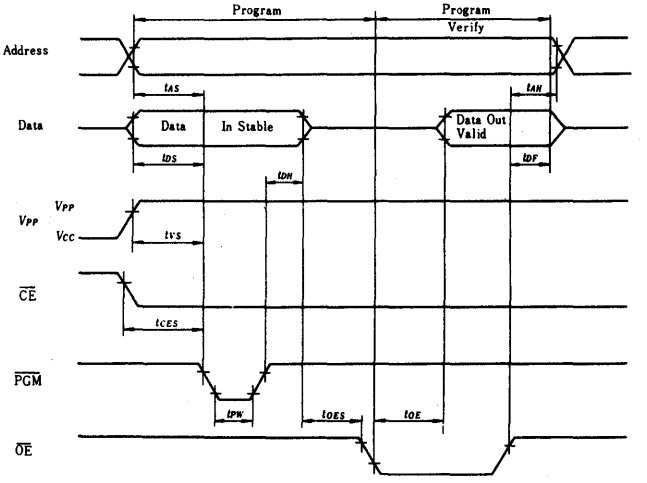
Test Condition

Input Pulse Level: 0.8V to 2.2V

Input Rise and Fall Time: ≤ 20 ns

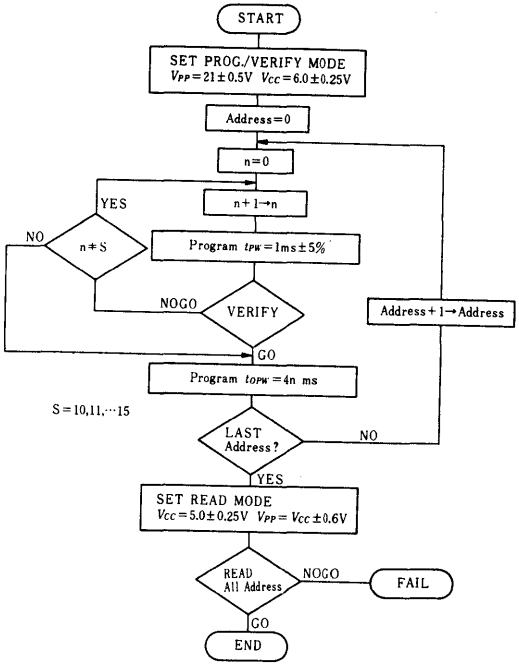
Reference Level for Measuring Timing: Input; 1V and 2V

Output; 0.8V and 2V



■HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flow chart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

●AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=21V±0.5V)

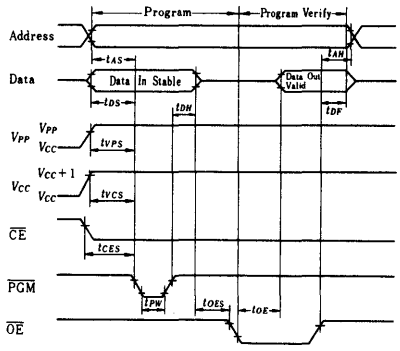
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay*	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VPS}		2	—	—	μs
V_{CC} Setup Time	t_{VCS}		2	—	—	μs
$\overline{PGM}$ Pulse Width during Initial Program	t_{PW}		0.95	1.0	1.05	ms
$\overline{PGM}$ Pulse Width during Over Program**	t_{OPW}		3.8	—	63	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}		—	—	150	ns

* t_{DF} defines the time at which the output achieves the open circuit conditions and is not referenced to output voltage levels.
** t_{OPW} is defined as mentioned in flow chart.

●SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Time:	≤ 20 ns
Reference Level for Measuring Timing:	Input; 1V and 2V
	Output; 0.8V and 2V



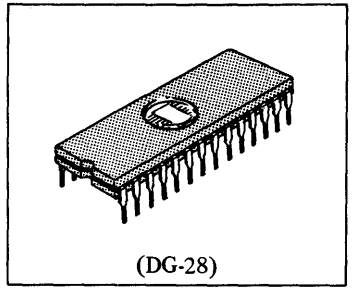
HN27256G-25, HN27256G-30

32768-word x 8-bit UV Erasable and Programmable ROM

Preliminary

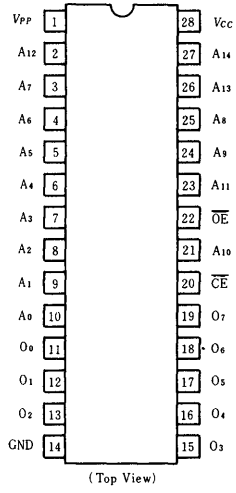
■ FEATURES

- Single Power Supply . . . . . +5V ± 5%
- High Performance Programming . . Program Voltage: +12.5V D.C.
  Automated Programming Operations
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time . . . . . HN27256G-25:250ns(max.)
  HN27256G-30:300ns(max.)
- Absolute Max. Rating of V_{pp} pin . . 13.0V
- Low Stand-by Current . . . . . 40mA (stand-by)
- Compatible with INTEL 27256



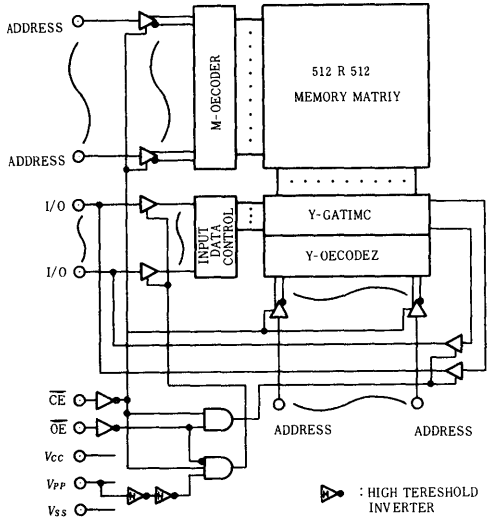
(DG-28)

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A_9 (24)	V_{pp} (1)	V_{CC} (28)	Outputs (11 ~ 13, 15 ~ 19)
Read	V_{IL}	V_{IL}	×	V_{CC}	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	×	V_{CC}	V_{CC}	High Z
Stand by	V_{IH}	×	×	V_{CC}	V_{CC}	High Z
High Performance Program	V_{IL}	V_{IH}	×	V_{PP}	V_{CC}	Din
Program Verify	V_{IH}	V_{IL}	×	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	V_{IH}	×	V_{PP}	V_{CC}	High Z

Note) × : Don't care.

Note: The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ ABSOLUTE MAXIMUM RATING

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	− 65 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	− 10 to +80	°C
All Input and Output Voltages*	V_{IN}, V_{out}	−0.6 to +7	V
Voltage on Pin 24 (A_9)*	V_{ID}	−0.6 to +13.5	V
V_{PP} Voltage*	V_{PP}	−0.6 to +13.0	V
V_{CC} Voltage*	V_{CC}	−0.6 to +7	V

* with respect to GND.

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS (Ta=0~+70°C, V_{CC}=5V±5%, V_{pp}=V_{CC})

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.5 V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{out} = 5.5V/0.45V	–	–	10	μA
V_{PP} Current	I_{PP1}	V_{PP} = 5.5 V	–	–	5	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	40	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	45	100	mA
Input Low Voltage	V_{IL}		−0.1	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V
Output High Voltage	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V

● AC CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±5%, V_{pp}=V_{CC})

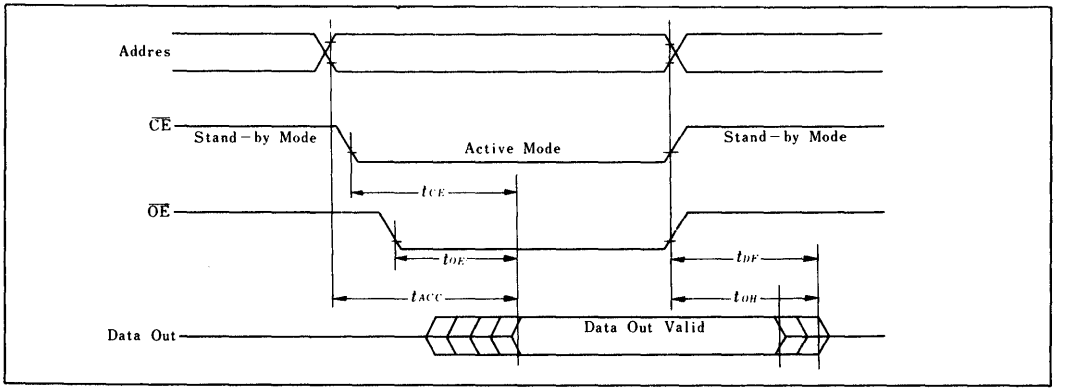
Parameter	Symbol	Test Condition	HN27256G-25		HN27256G-30		Unit
			min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	250	–	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	–	250	–	300	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{OE}$ = V_{IL}	–	100	–	120	ns
$\overline{OE}$ High Output Float	t_{DF}	$\overline{CE}$ = V_{IL}	0	60	0	105	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	0	–	ns

Note: t_{DF} defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

■ SWITCHING CHARACTERISTICS

● TEST CONDITION

- Input pulse levels: 0.8V to 2.2V
- Input rise and fall time: ≤20ns
- Output load: 1 TTL Gate +100pF
- Reference level for measuring timing: Inputs ; 1.0V and 2.0V
  Outputs ; 0.8V and 2.0V

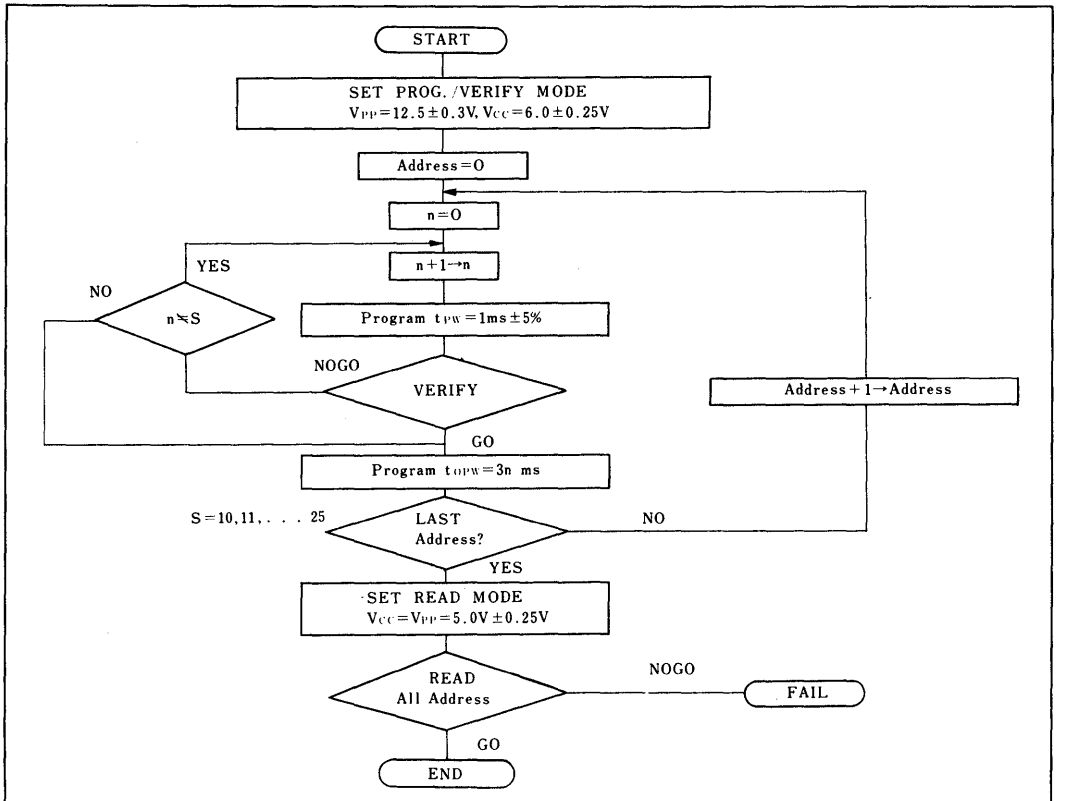


■ CAPACITANCE (Ta=25°C, f=1MHz)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{in}	V_{in} = 0 V	–	4	6	pF
Output Capacitance	C_{out}	V_{out} = 0 V	–	8	12	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

■ HIGH PERFORMANCE PROGRAMMING OPERATION

• DC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25 V	–	–	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
V_{cc} Current (Active)	I_{cc2}		–	–	100	mA
Input Low Level	V_{IL}		−0.1	–	0.8	V
Input High Level	V_{IH}		2.0	–	V_{cc} + 1	V
V_{pp} Supply Current	I_{pp2}	$\overline{CE}$ = V_{IL}	–	–	50	mA

• AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V)

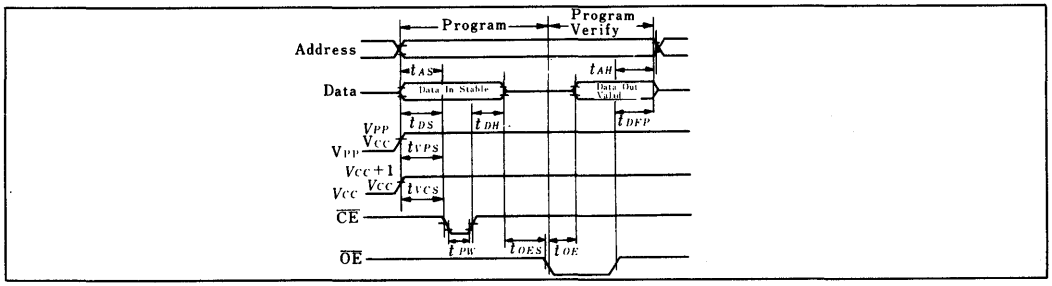
Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ to Output Float Delay	t_{DFP}		0	–	130	ns
V_{pp} Setup Time	t_{VPS}		2	–	–	μs
V_{cc} Setup Time	t_{VCP}		2	–	–	μs
PGM Pulse Width During Initial Programming	t_{PW}		0.95	1.0	1.05	ms
$\overline{CE}$ Pulse Width During Overprogramming	t_{OPW}		2.85	–	78.75	ms
$\overline{CE}$ Setup Time	t_{CES}		2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}		–	–	150	ns

Notes: t_{OPW} is defined as mentioned in flow chart.
t_{DFP} defines the time at which the output achieves the open circuit condition and data is no longer driven.

■ SWITCHING CHARACTERISTICS

• TEST CONDITION

- Input pulse level: 0.8V to 2.2V
- Input rise and fall time: ≤20ns
- Reference level for measuring timing: Input ; 1.0V and 2.0V Output; 0.8V and 2.0V



■ ERASE

Erasure of HN27256G is performed by exposure to ultraviolet light of 2537Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W. sec/cm^2.

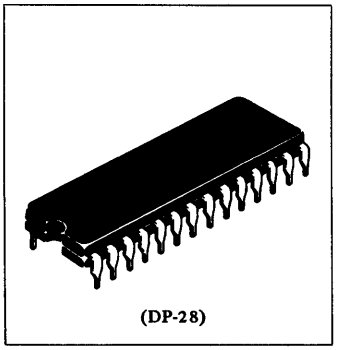
HN58064P-25, HN58064P-30, HN58064P-45

Preliminary

8192-word x 8-bit Electrically Erasable and Programmable ROM

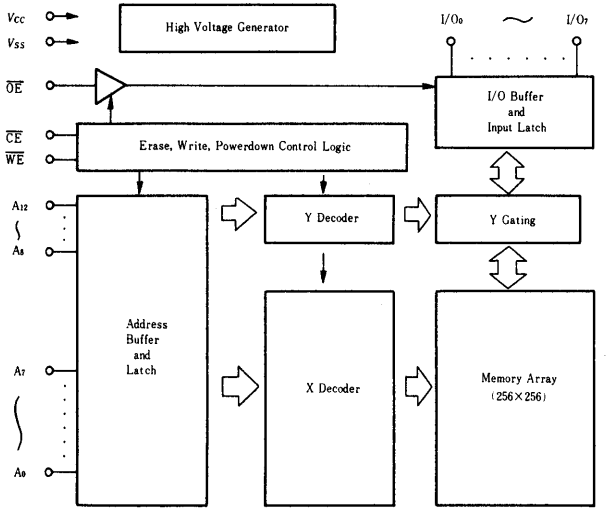
■ FEATURES

- Single 5V Supply
- Address, Data, $\overline{CE}$, $\overline{OE}$ Lathes
- Byte Erase/Byte Write Time . . . . . 10ms typ.
- Chip Erase Time . . . . . 20ms typ.
- Fast Access Time . . . . . 250/300/450ns max.
- Low Power Disipation . . . . . 100mA (max) Active
  40mA (max) Standby
- Comforms to JEDEC Byte-Wide Standard
- Reliable N-channel MNOS Technology
- 10000 Erase/Write Cycles

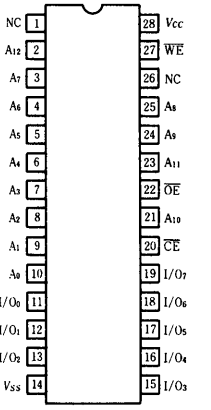


(DP-28)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	D_{out}
Standby	V_{IH}	X	X	High Z
Byte Erase	V_{IL}	V_{IH}	V_{IL}	$D_{in} = V_{IH}$
Byte Write	V_{IL}	V_{IH}	V_{IL}	D_{in}
Chip Erase	V_{IL}	V_{IL}	V_{IL}	$D_{in} = V_{IH}$
Deselect	V_{IL}	V_{IH}	V_{IH}	High Z

X: V_{IL} or V_{IH}

$A_0 \sim A_{12}$	Address Input
$I/O_0 \sim I/O_7$	Data in/Data out
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
V_{CC}	Power (+5V)
V_{SS}	GND
NC	No Connect

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	–0.3 to +7.0	V
Input Voltage*	V_{in}	–0.3 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	– 55 to +125	°C

* With Respect to V_{SS}

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	–0.1	–	0.8	V
	V_{IH}	2.0	–	V_{CC}+1	V
Operating Temperature	T_{opr}	0	–	70	°C

■ DC AND OPERATING CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V +10%)

Parameter	Symbol	Test Condition	min	typ	max	unit
Input Leakage Current	I_{L1}	V_{CC} = 5.5V V_{in} = 5.5V	–	–	10	μA
Output Leakage Current	I_{L0}	V_{CC} = 5.5V V_{out} = 5.5 ~ 0.4V	–	–	10	μA
V_{CC} Current (Standby)	I_{CC1}		–	20	40	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH}	–	60	100	mA
Input Low Voltage	V_{IL}		–0.1	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = –400μA	2.4	–	–	V

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	min	typ	max	unit
Input Capacitance	C_{in}	V_{in} = 0V	–	–	6	pF
Output Capacitance	C_{out}	V_{in} = 0V	–	–	12	pF

■ AC TEST CONDITIONS

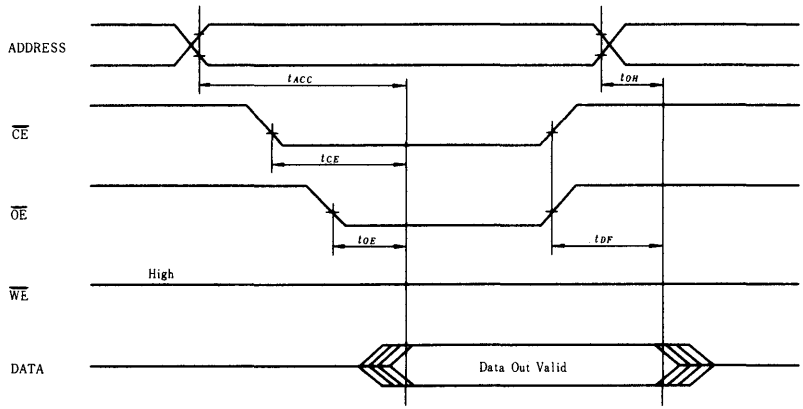
Input Pulse Levels:	0.8V to 2.0V Input
Rise and Fall Time:	≦ 20ns
Output Load:	1TTL Gate + 100pF
Reference Level for Measuring Timing:	Inputs; 1V and 2V Outputs; 0.8V and 2.0V

■ AC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V + 10%)

● READ OPERATION

Parameter	Symbol	Test Condition	HN58064P-25		HN58064P-30		HN58064P-45		Unit
			min	max	min	max	min	max	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	–	250	–	300	–	450	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	–	250	–	300	–	450	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	–	100	–	150	–	150	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	0	–	0	–	0	–	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}	0	90	0	130	0	130	ns

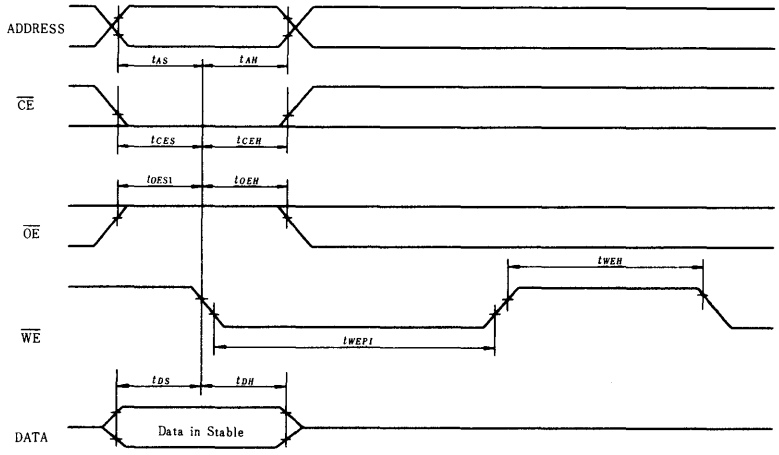
● WAVEFORM ····· READ CYCLE



● BYTE ERASE AND BYTE WRITE OPERATION

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		10	–	–	ns
Address Hold Time	t_{AH}		50	–	–	ns
$\overline{CE}$ Setup Time	t_{CES}		10	–	–	ns
$\overline{CE}$ Hold Time	t_{CEH}		50	–	–	ns
$\overline{OE}$ Setup Time	t_{OES1}		10	–	–	ns
$\overline{OE}$ Hold Time	t_{OEH}		50	–	–	ns
$\overline{WE}$ Pulse Width	t_{WEP1}		8	10	15	ms
$\overline{WE}$ High Time	t_{WEH}		500	–	–	ns
Data Setup Time	t_{DS}		10	–	–	ns
Data Hold Time	t_{DH}		50	–	–	ns

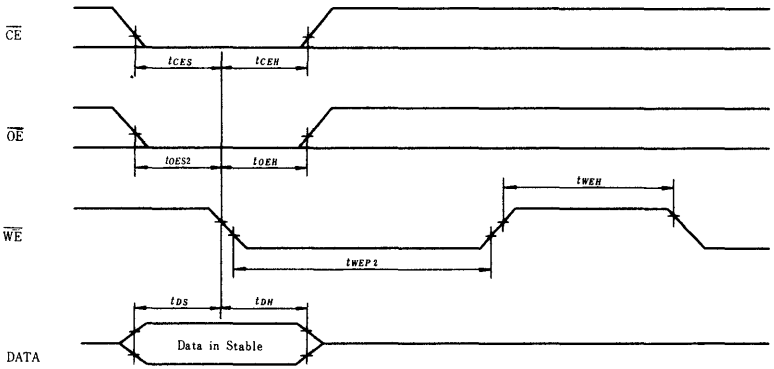
● WAVEFORM ····· ERASE AND WRITE CYCLE



● CHIP ERASE OPERATION

Parameter	Symbol	Test Condition	min	typ	max	Unit
$\overline{CE}$ Setup Time	t_{CES}		10	–	–	ns
$\overline{CE}$ Hold Time	t_{CEH}		50	–	–	ns
$\overline{OE}$ Setup Time	t_{OES2}		0	–	50	ns
$\overline{OE}$ Hold Time	t_{OEH}		50	–	–	ns
$\overline{WE}$ Pulse Width	t_{WEP2}		15	20	50	ms
$\overline{WE}$ High Time	t_{WEH}		500	–	–	ns
Data Setup Time	t_{DS}		10	–	–	ns
Data Hold Time	t_{DH}		50	–	–	ns

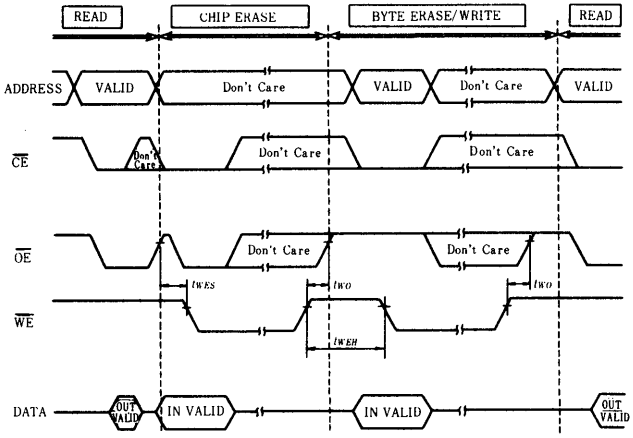
WAVE FORM ····· CHIP ERASE

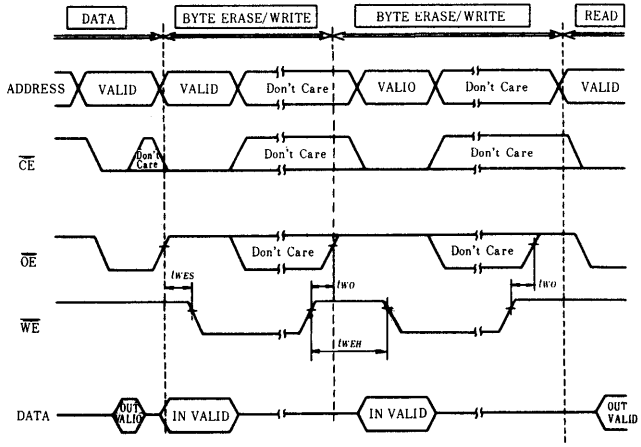


• SEQUENCE OPERATION

Parameter	Symbol	Test Condition	min	typ	max	Unit
$\overline{WE}$ Setup Time	t_{WES}		150	–	–	ns
$\overline{WE}$ to $\overline{OE}$ Time	t_{WO}		50	–	–	ns
$\overline{WE}$ High Time	t_{WEH}		500	–	–	ns

• WAVE FORM



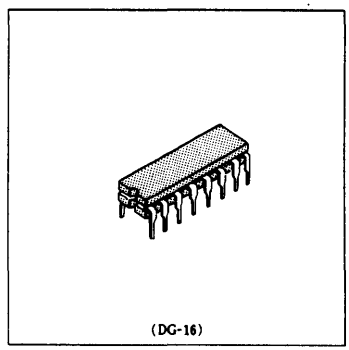


BIPOLAR RAM

256-word × 1-bit Fully Decoded Random Access Memory

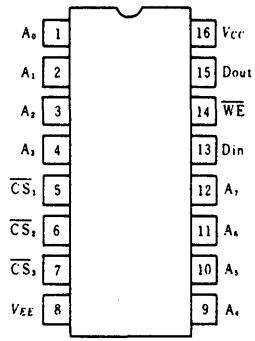
The HM10414 is ECL 10K compatible, 256-word x 1-bit, read write, random access memory developed for high speed systems such as scratch pad and control/buffer storages.
The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM10414 is encapsulated in cerdip-16pin package, compatible with Fairchild's F10414.

- Fully compatible with 10K ECL level
- Address access time: HM10414: 10ns (max.)
  HM10414-1: 8ns (max.)
- Write pulse width: 6ns (min.)
- Three chip select pins
- Output obtainable by wired-OR (open emitter)



(DG-16)

■ PIN ARRANGEMENT



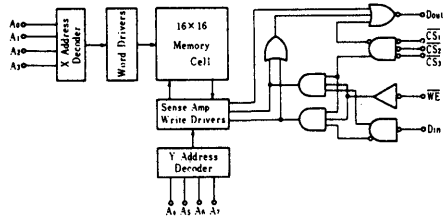
(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
any one H	×	×	L	Not Selected
all L	L	L	L	Write "0"
all L	L	H	L	Write "1"
all L	H	×	Dout *	Read

× : Don't care
* : Read out non-inverted

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE}=-5.2V$, $R_L=50\Omega$ to $-2.0V$, $Ta=0$ to $+75°C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	−	−840	mV
			+25°C	−960	−	−810	
			+75°C	−900	−	−720	
	V_{OL}		0°C	−1870	−	−1665	
			+25°C	−1850	−	−1650	
			+75°C	−1830	−	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	−	−	mV
			+25°C	−980	−	−	
			+75°C	−920	−	−	
	V_{OLC}		0°C	−	−	−1645	
			+25°C	−	−	−1630	
			+75°C	−	−	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	−	−840	mV
			+25°C	−1105	−	−810	
			+75°C	−1045	−	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	−	−1490	
			+25°C	−1850	−	−1475	
			+75°C	−1830	−	−1450	
Input Current	I_{IH}	$V_{IN}=V_{IHA}$	0 to +75°C	−	−	220	μA
	I_{IL}	$\overline{CS}$ / $V_{IN}=V_{ILB}$	0 to +75°C	0.5	−	170	
		Other		−50	−	−	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 8	+75°C	−	−130	−	mA
			0°C	−180	−140	−	

● AC CHARACTERISTICS

($V_{EE}=-5.2V\pm5\%$, $Ta=0$ to $+75°C$, air flow exceeding 2m/sec, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	HM10414			HM10414-1			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACR}		−	3	6	−	3	6	ns
Chip Select Recovery Time	t_{RCS}		−	3	6	−	3	6	ns
Address Access Time	t_{AA}		−	7	10	−	6	8	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	$t_{WSA}=2ns$	6	4	−	ns
Data Setup Time	t_{WSD}		1	0	−	ns
Data Hold Time	t_{WHD}		1	0	−	ns
Address Setup Time	t_{WSA}	$t_W=6ns$	2	0	−	ns
Address Hold Time	t_{WHA}		2	0	−	ns
Chip Select Setup Time	t_{WSCS}		1	0	−	ns
Chip Select Hold Time	t_{WHCS}		1	0	−	ns
Write Disable Time	t_{WS}		−	−	5	ns
Write Recovery Time	t_{WR}		−	−	5	ns

3. RISE/FALL TIME

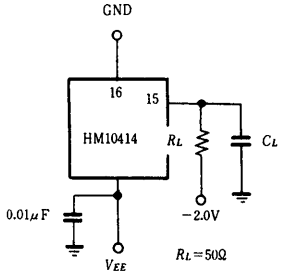
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		−	1.5	2.5	ns
Output Fall Time	t_f		−	1.5	2.5	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		−	3	5	pF
Output Capacitance	C_{out}		−	5	8	pF

■ TEST CIRCUIT AND WAVEFORMS

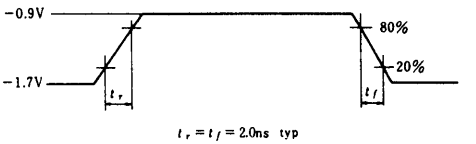
1. LOADING CONDITIONS



R_L=50Ω

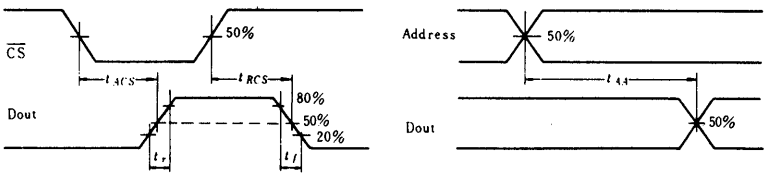
C_L=30pF(includes jig and stray capacitance)

2. INPUT PULSE

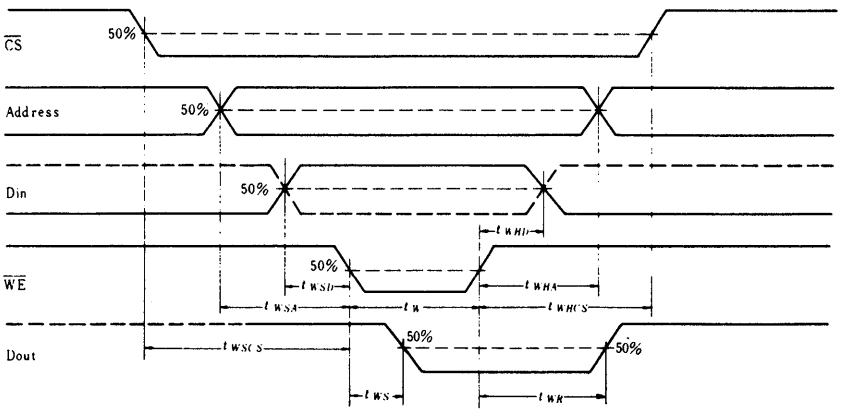


$t_r = t_f$ = 2.0ns typ

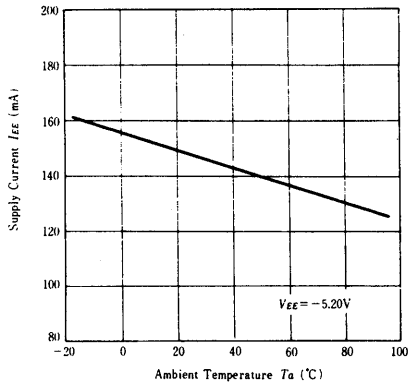
3. READ MODE



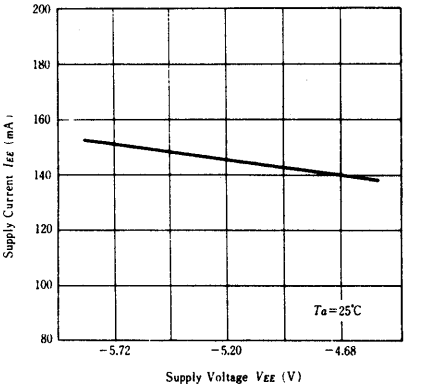
4. WRITE MODE



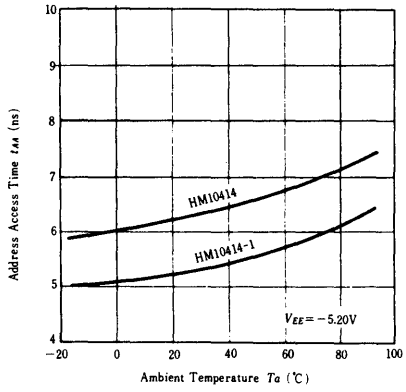
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



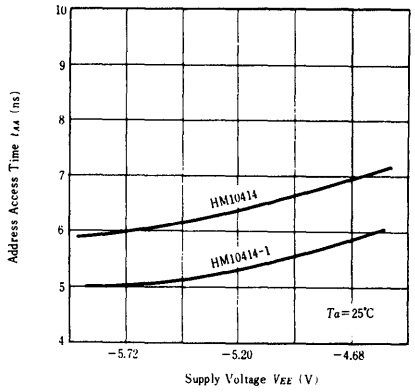
SUPPLY CURRENT vs. SUPPLY VOLTAGE



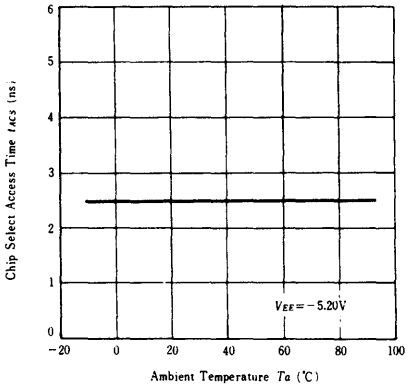
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



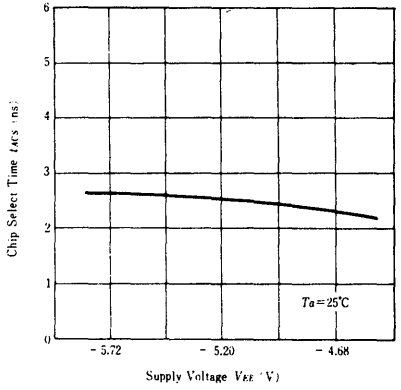
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



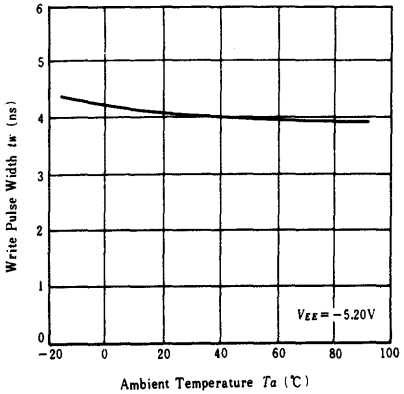
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



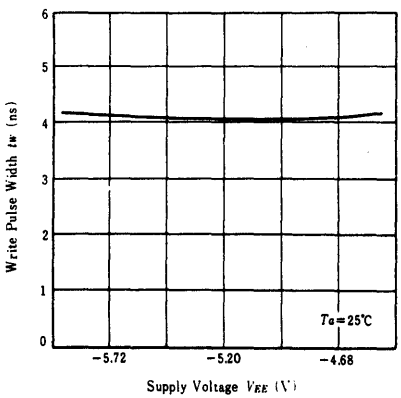
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE

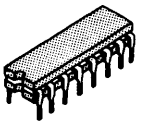


HM2110, HM2110-1

1024-word×1-bit Fully Decoded Random Access Memory

The HM2110 Series item is an ECL compatible, 1024-word x 1-bit, read/write, random access memory developed for application to scratch pads, control and buffer memories, etc. which require high speeds.

- It is compatible with 10K ECL logic.
- Chip select access time .....10ns (max.)
- Address access time .....HM2110: 35ns (max.)
  HM2110-1: 25ns (max.)
- Power consumption .....0.5mW/bit (typ)
- Output obtainable by Wired-OR (open emitter).



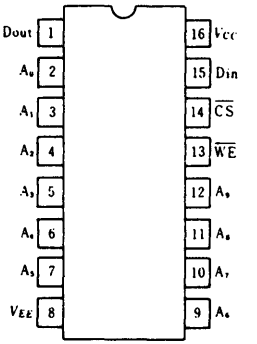
(DG-16A)

■TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

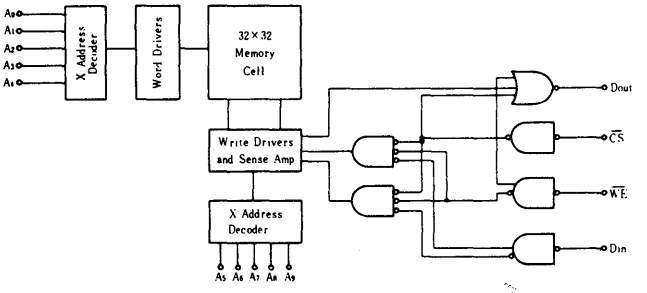
× : irrelevant
* : Read out noninverted

■PIN ARRANGEMENT



Top View

■BLOCK DIAGRAM



■ABSOLUTE MAXMUM RATINGS

Item	Symbol	HM2110 Series	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS ($V_{EE}=-5.2V$, $R_L=50\Omega$ to $-2.0V$, $Ta=0$ to $+75°C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN}=V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / $V_{IN}=V_{ILB}$	0 to +75°C	0.5	—	170	
		Other		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 8	$0\leq Ta<25°C$	−150	−100	—	mA
			$Ta\geq 25°C$	−125	−90	—	

●AC CHARACTERISTICS

($V_{EE}=-5.2V\ \pm 5\%$, $Ta=0$ to $+75°C$, air flow exceeding 2m/sec, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	HM2110			HM2110-1			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	7	10	—	7	10	ns
Chip Select Recovery Time	t_{RCS}		—	7	10	—	7	10	ns
Address Access Time	t_{AA}		—	20	35	—	15	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM2110			HM2110-1			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	$t_{WSA}=8ns$	25	—	—	25	—	—	ns
Data Setup Time	t_{WSD}		5	—	—	5	—	—	ns
Data Hold Time	t_{WHD}		5	—	—	5	—	—	ns
Address Setup Time	t_{WSA}	$t_W=25ns$	8	—	—	8	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		5	—	—	5	—	—	ns
Chip Select Hold Time	t_{WHCS}		5	—	—	5	—	—	ns
Write Disable Time	t_{WS}		—	—	10	—	—	10	ns
Write Recovery Time	t_{WR}		—	—	10	—	—	10	ns

3. RISE/FALL TIME

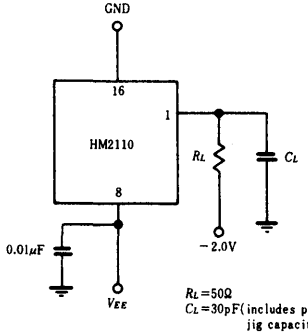
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	5	—	ns
Output Fall Time	t_f		—	5	—	ns

4. CAPACITANCE

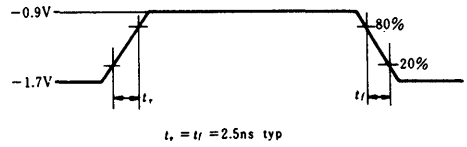
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	5	pF
Output Capacitance	C_{out}		—	7	8	pF

■ TEST CIRCUIT AND WAVEFORMS

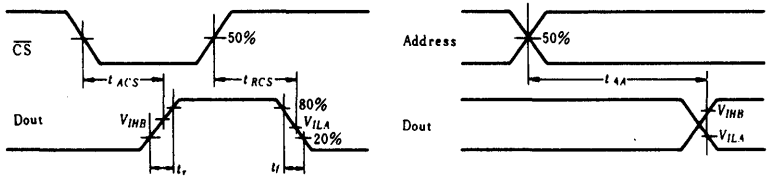
1. LOADING CONDITION



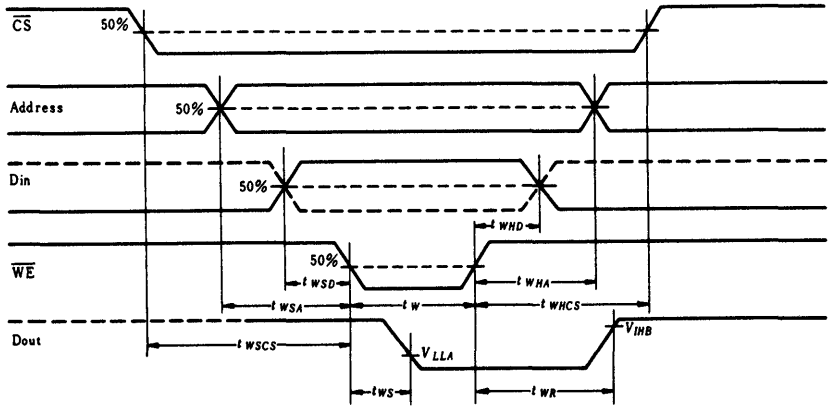
2. INPUT PULSE



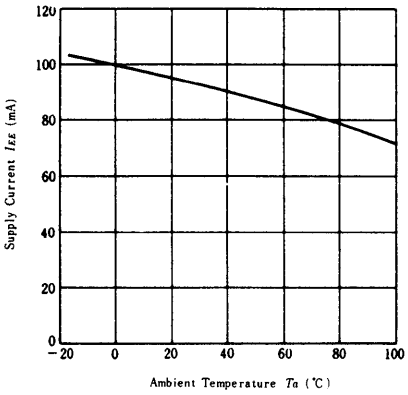
3. READ MODE



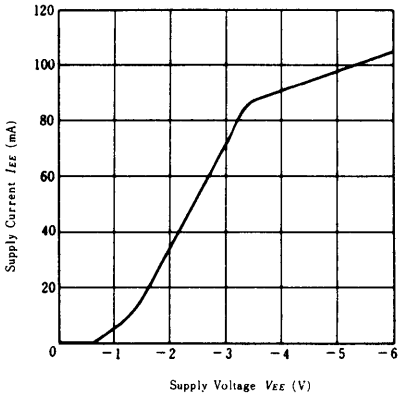
4. WRITE MODE



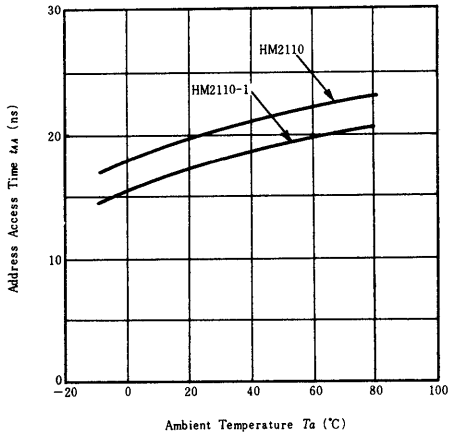
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



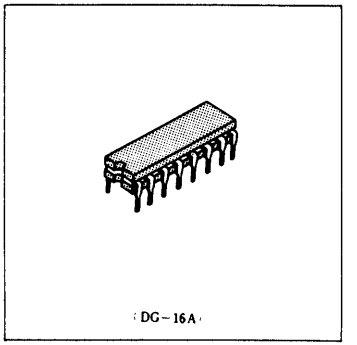
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



HM2112, HM2112-1

1024-word×1-bit Fully Decoded Random Access Memory

The HM2112 is an ECL compatible, 1024-word x 1-bit, read/write, random access memory developed for application to scratch pads, control and buffer memories, etc. which require high speeds.



(DG-16A)

■ FEATURES

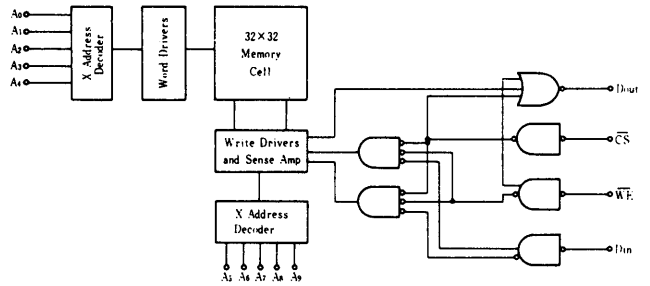
- Level ..... 10k ECL Compatible
- Construction ..... 1024-word by 1-bit
- Address Access Time ..... HM2112 10ns (max.)
  HM2112-1 8ns (max.)
- Chip Select Access Time ..... 5ns (max.)
- Power Consumption ..... 0.8mW/bit (typ)
- Output Obtainable by Wired-OR (open emitter)
- Fully Pin Compatible with F10415

■ TRUTH TABLE

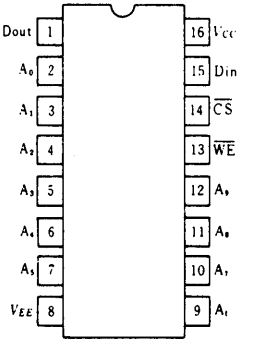
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

× : Irrelevant
* : Read out noniverted

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HM2112	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg} (Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

(V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

●DC CHARACTERISTICS

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IL}	$V_{IN} = V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / $V_{IN} = V_{ILB}$	0 to +75°C	0.5	—	170	
		Other		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 8	Ta = 0°C	−200	—	—	mA
			Ta = 75°C	−170	—	—	

●AC CHARACTERISTICS

(V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	HM2112-1			HM2112			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		1	3	5	1	3	5	ns
Chip Select Recovery Time	t_{RCS}		1	3	5	1	3	5	ns
Address Access Time	t_{AA}		3	6.5	8	3	7.5	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM2112-1			HM2112			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA} = 3ns	6	2	—	6	2	—	ns
Data Setup Time	t_{WSD}		1	0	—	1	0	—	ns
Data Hold Time	t_{WHD}		1	0	—	1	0	—	ns
Address Setup Time	t_{WSA}	t_W = 6ns	3	0	—	3	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	2	0	—	ns
Chip Select Setup Time	t_{WSCS}		1	0	—	1	0	—	ns
Chip Select Hold Time	t_{WHCS}		1	0	—	1	0	—	ns
Write Disable Time	t_{WS}		1	3	5	1	3	5	ns
Write Recovery Time	t_{WR}		1	3	5	1	3	5	ns

3. RISE/FALL TIME

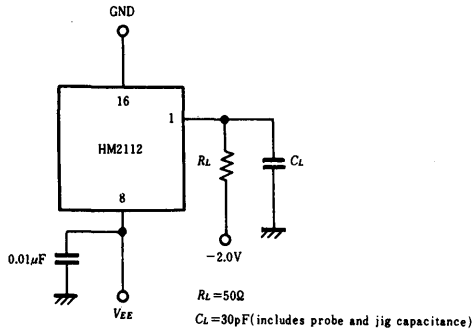
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		0.8	1.5	2.5	ns
Output Fall Time	t_f		0.8	1.5	2.5	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		1	3	5	pF
Output Capacitance	C_{out}		3	5	8	pF

■ TEST CIRCUIT AND WAVEFORMS

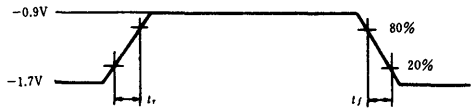
1. LOADING CONDITION



R_L=50Ω

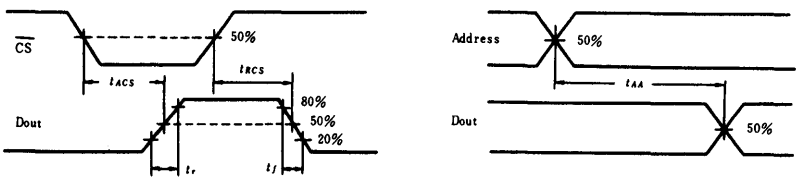
C_L=30pF(includes probe and jig capacitance)

2. INPUT PULSE

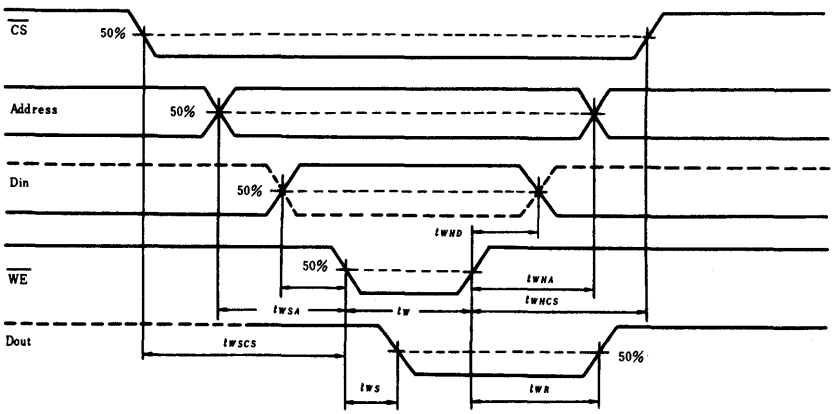


t_r=t_f=2.0ns typ

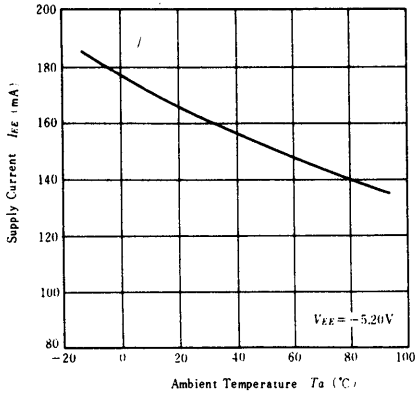
3. READ MODE



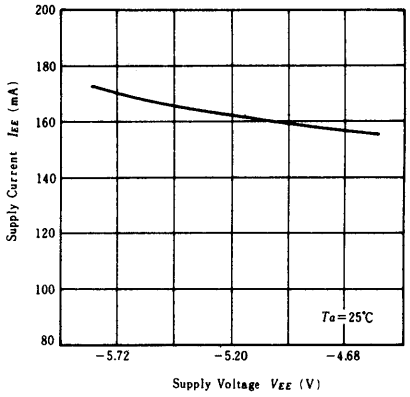
4. WRITE MODE



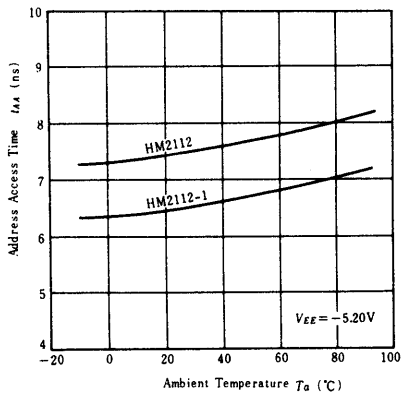
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



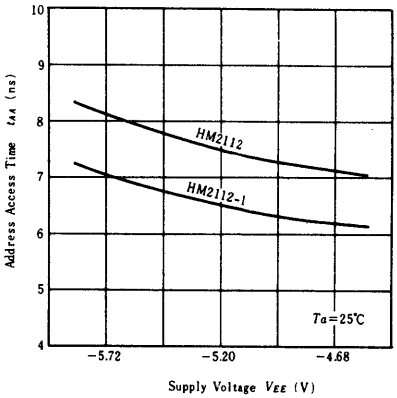
SUPPLY CURRENT vs. SUPPLY VOLTAGE



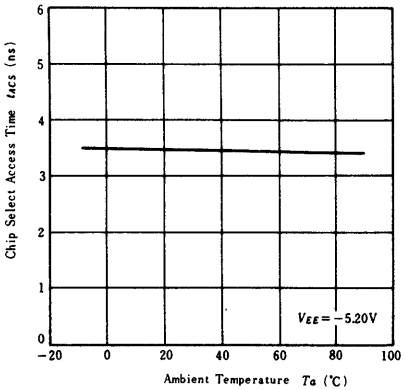
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



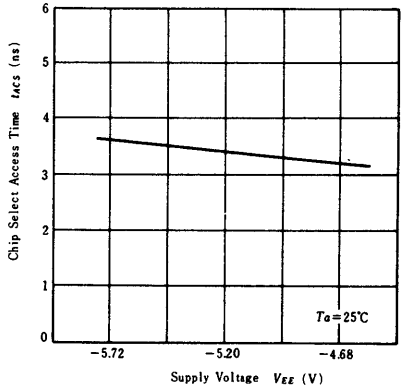
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



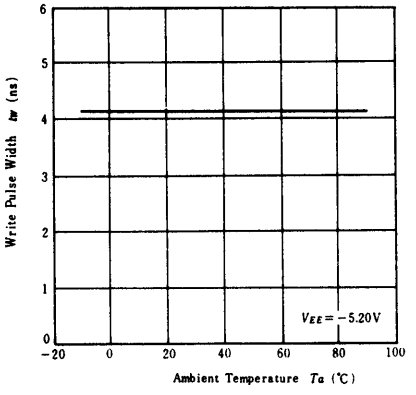
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



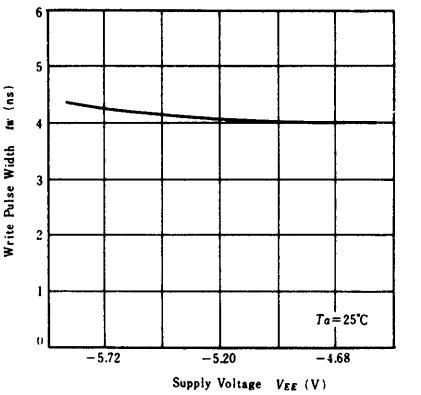
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



HM10422

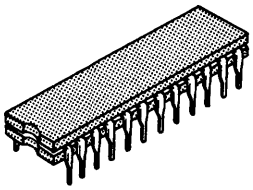
256-word×4-bit Fully Decoded Random Access Memory

The HM10422 is ECL 10K compatible, 256-word x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control buffer storages.

Four active Low Block Select lines are provided to select each block independently.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10422 is encapsulated in cerdip-24 pin package, compatible with Fairchild's F10422.



(DG-24A)

■ FEATURES

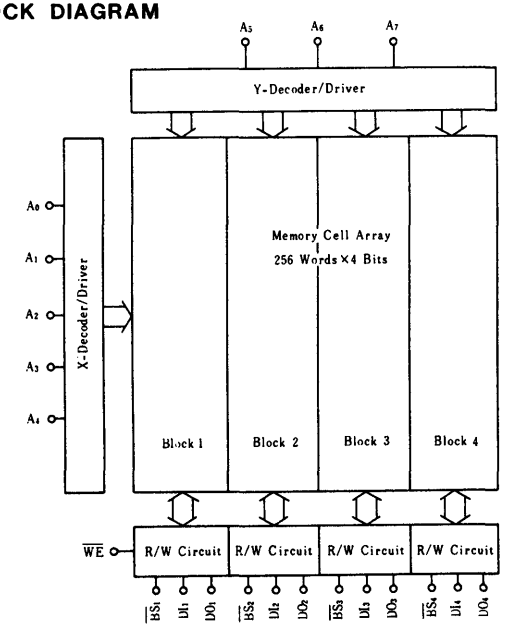
- 256-word x 4 bit organization.
- Fully compatible with 10K ECL level
- Address access time: 10ns (max)
- Write pulse width: 6ns (min)
- Power dissipation: 0.8mW/bit
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

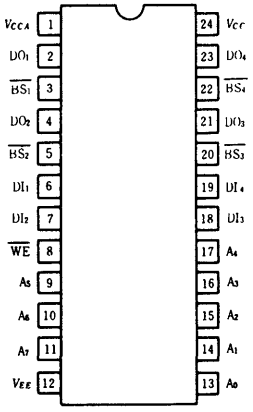
Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read out noninvert

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

(V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

● DC CHARACTERISTICS

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{BS}$	0 to +75°C	0.5	—	170	
		Other (V_{IN} = V_{ILB})		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	Ta = 0°C	−200	−160	—	mA
			Ta = 75°C	—	−145	—	

● AC CHARACTERISTICS

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Block Select Access Time	t_{ABS}		—	—	5	ns
Block Select Recovery Time	t_{RBS}		—	—	5	ns
Address Access Time	t_{AA}		—	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} = 2ns	6	4.5	—	ns
Data Setup Time	t_{WSD}		2	0	—	ns
Data Hold Time	t_{WHD}		2	0	—	ns
Address Setup Time	t_{WSA}	t_W = 6ns	2	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	ns
Block Select Setup Time	t_{WSBS}		2	0	—	ns
Block Select Hold Time	t_{WHBS}		2	0	—	ns
Write Disable Time	t_{WS}		—	4	5	ns
Write Recovery Time	t_{WR}		—	4.5	9	ns

3. RISE/FALL TIME

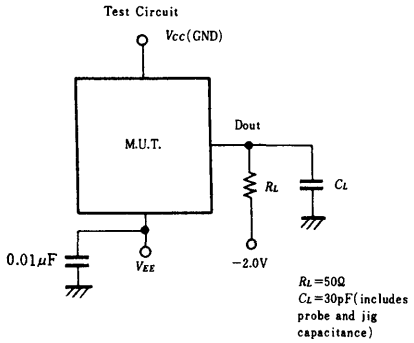
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

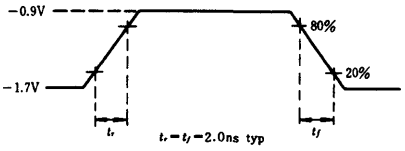
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■TEST CIRCUIT AND WAVEFORMS

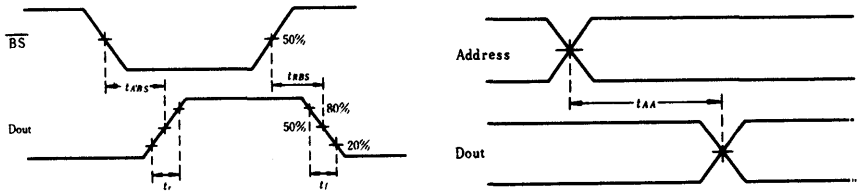
1. LOADING CONDITION



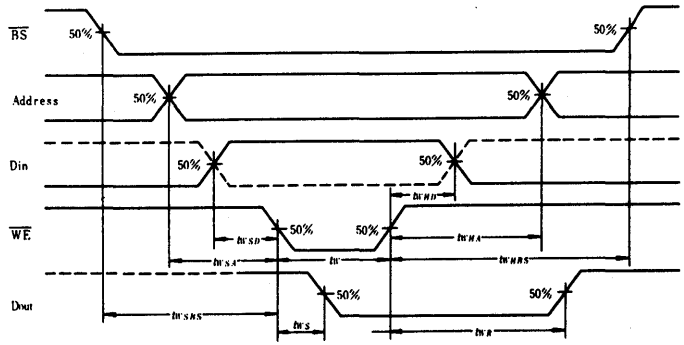
2. INPUT PULSE



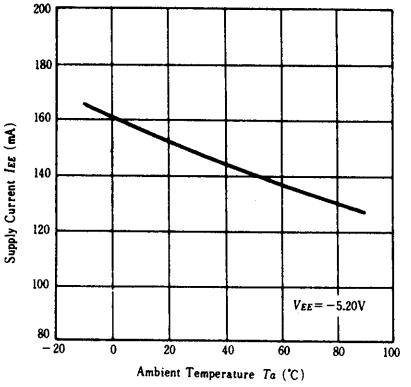
3. READ MODE



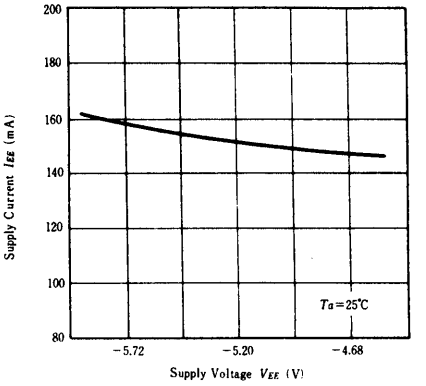
4. WRITE MODE



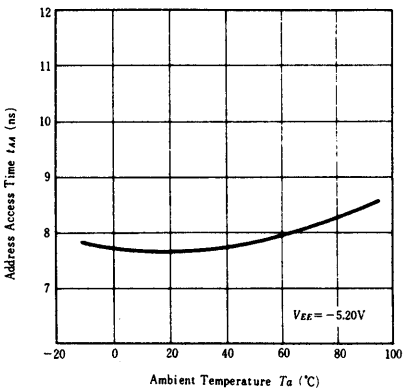
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



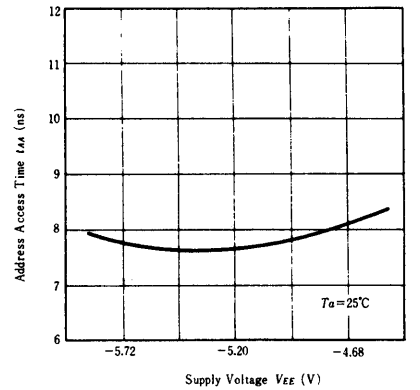
SUPPLY CURRENT vs. SUPPLY VOLTAGE



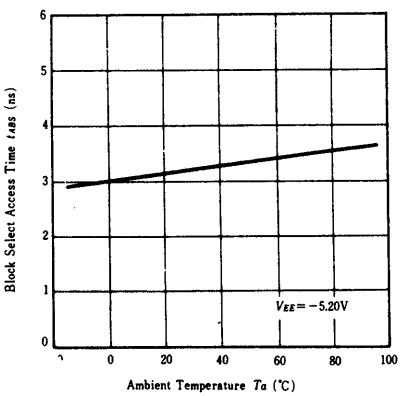
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



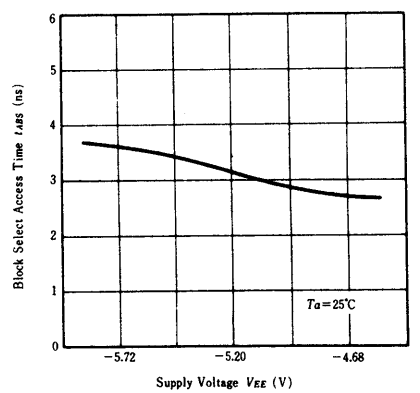
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



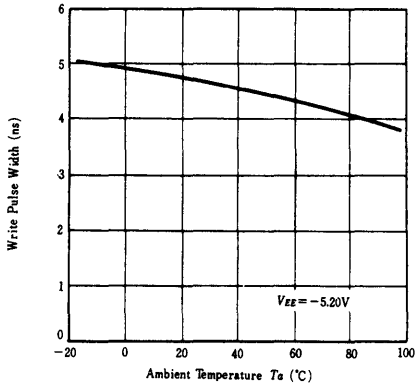
BLOCK SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



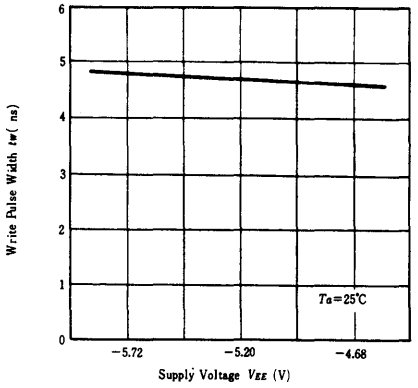
BLOCK SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



HM10422-7

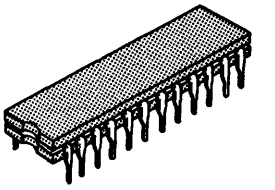
256-word × 4-bit Fully Decoded Random Access Memory

The HM10422 is ECL 10K compatible, 256-word x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control buffer storages.

Four active Low Block Select lines are provided to select each block independently.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10422 is encapsulated in cerdip-24 pin package, compatible with Fairchild's F10422.



(DG-24A)

■ FEATURES

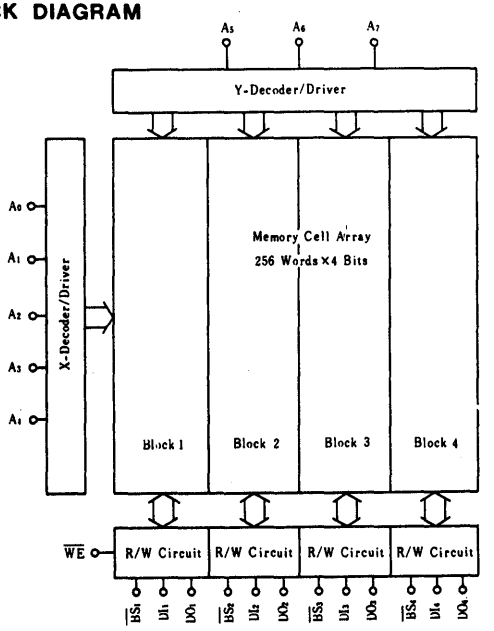
- 256-word x 4 bit organization
- Fully compatible with 10K ECL level
- Address access time: 7ns (max)
- Write pulse width: 4ns (min)
- Power dissipation: 1.0 mW/bit
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

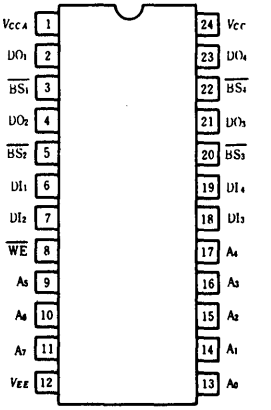
Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read out noninvert

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

HITACHI

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

(V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

● DC CHARACTERISTICS

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{BS}$	0 to +75°C	0.5	—	170	
		Other		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	Ta = 0°C	−240	−200	—	mA
			Ta = 75°C	—	−180	—	

● AC CHARACTERISTICS

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Block Select Access Time	t_{ABS}		—	—	5	ns
Block Select Recovery Time	t_{RBS}		—	—	5	ns
Address Access Time	t_{AA}		—	4	7	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} = 2ns	4	3	—	ns
Data Setup Time	t_{WSD}		1		—	ns
Data Hold Time	t_{WHD}		1		—	ns
Address Setup Time	t_{WSA}	t_W = 4ns	2		—	ns
Address Hold Time	t_{WHA}		1		—	ns
Block Select Setup Time	t_{WSBS}		1		—	ns
Block Select Hold Time	t_{WHBS}		1		—	ns
Write Disable Time	t_{WS}		—	3	5	ns
Write Recovery Time	t_{WR}		—	3	5	ns

3. RISE/FALL TIME

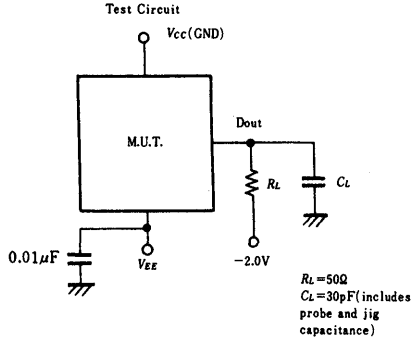
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

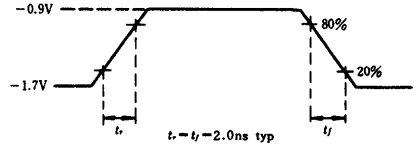
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

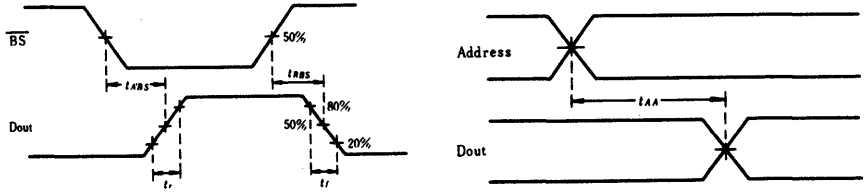
1. LOADING CONDITION



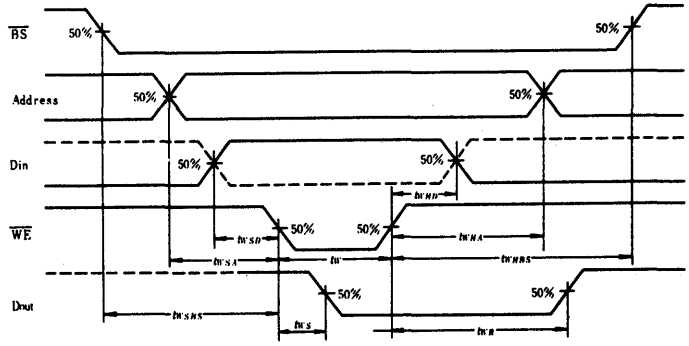
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



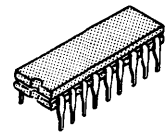
HM10470, HM10470-1

4096-word x 1-bit Fully Decoded Random Access Memory

The HM10470 is ECL 10K compatible, 4096-words x 1-bit, read write random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10470 is encapsulated in cerdip-18 pin package, compatible with Fairchild's F10470.



(DG-18)

■ FEATURES

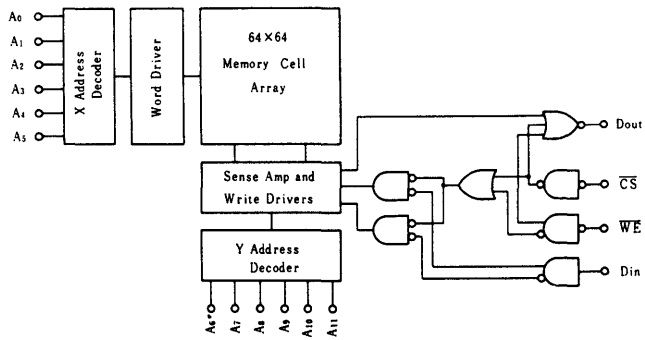
- 4096-word x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: HM10470 25ns (max)
  HM10470-1 15ns (max)
- Write pulse width: HM10470 25ns (min)
  HM10470-1 15ns (min)
- Low power dissipation: 0.2mW/bit
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

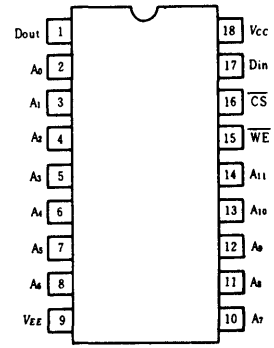
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Noninvert

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN} = V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / $V_{IN} = V_{ILB}$	0 to +75°C	0.5	—	170	
		Other		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 9	Ta = 0°C	−200* / −280**	−160* / −200**	—	mA
			Ta = 75°C	—	−145	—	

* HM10470
** HM10470-1

● AC CHARACTERISTICS (V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM10470			HM10470-1			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	—	10	—	—	8	ns
Chip Select Recovery Time	t_{RCS}		—	—	10	—	—	8	ns
Address Access Time	t_{AA}		—	15	25	—	12	15	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM10470			HM10470-1			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA} = 3ns	25	—	—	15	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	$t_W = t_{W\,min}$	3	—	—	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	10	—	—	8	ns
Write Recovery Time	t_{WR}		—	—	10	—	—	8	ns

3. RISE/FALL TIME

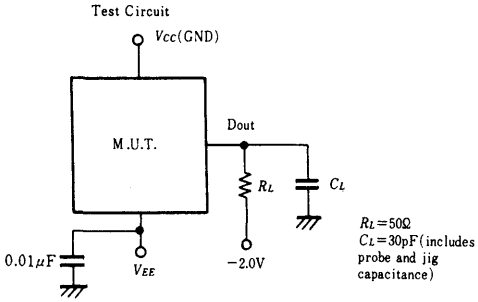
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

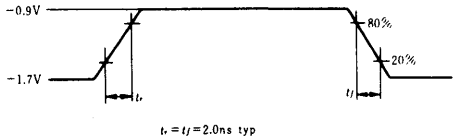
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

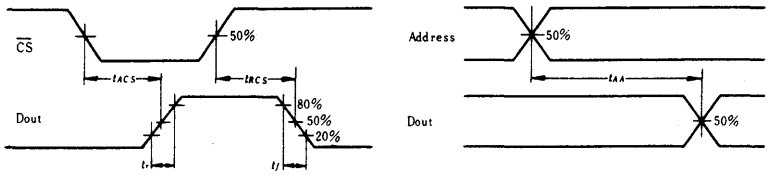
1. LOADING CONDITION



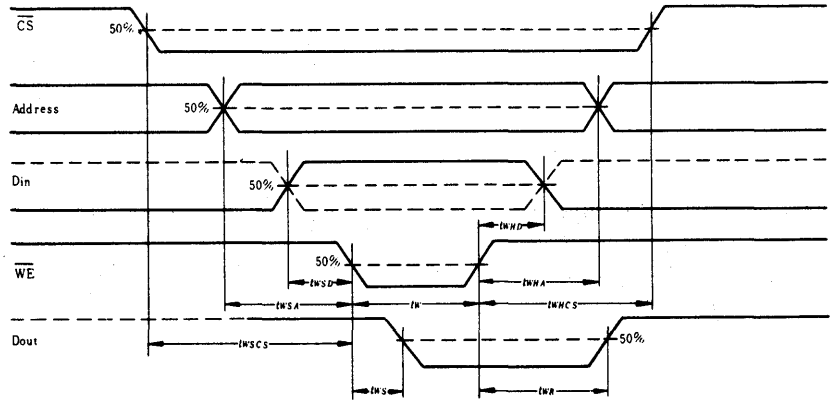
2. INPUT PULSE



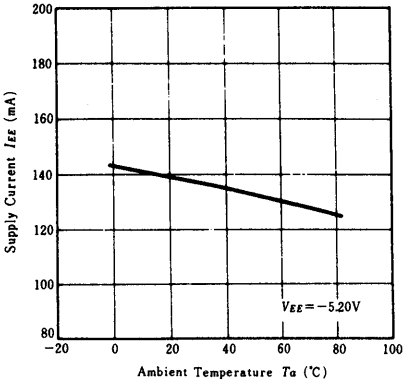
3. READ MODE



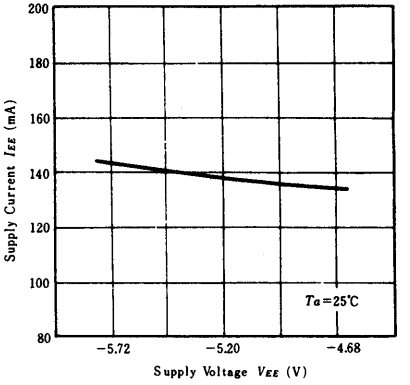
4. WRITE MODE



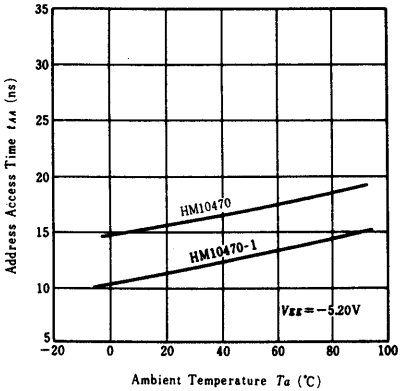
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



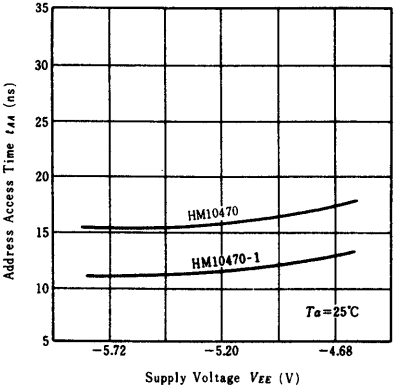
SUPPLY CURRENT vs. SUPPLY VOLTAGE



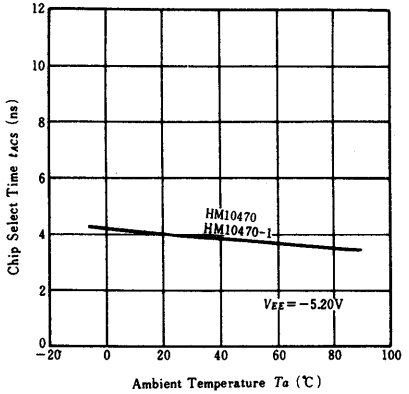
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



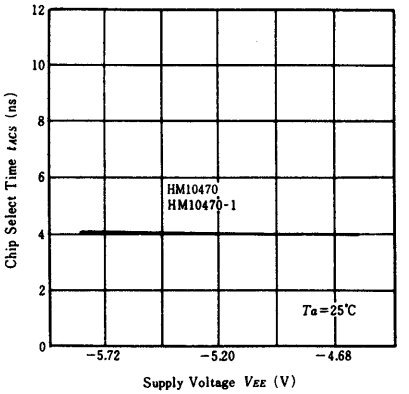
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



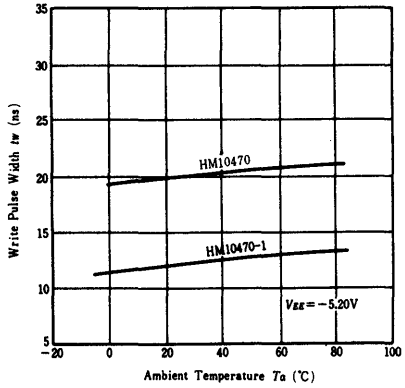
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



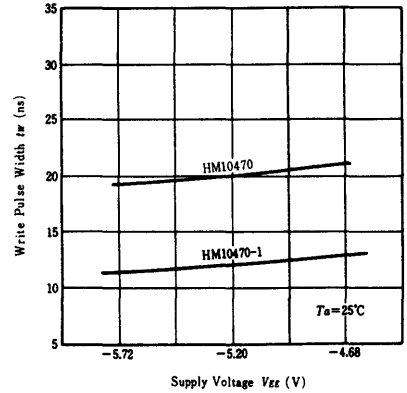
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



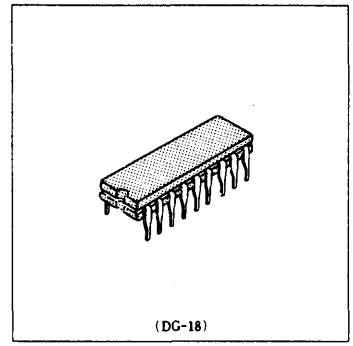
WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



HM10470-20

4096-word × 1-bit Fully Decoded Random Access Memory

The HM10470 is ECL 10K compatible, 4096-words x 1-bit, read/write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.
The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM10470 is encapsulated in cerdip-18 pin package, compatible with Fairchild's F10470.


(DG-18)

■ FEATURES

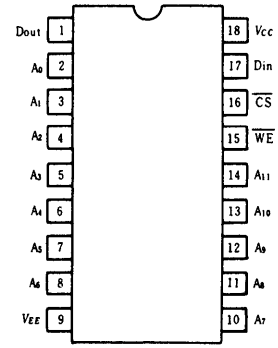
- 4096-word x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: 20ns (max)
- Write pulse width: 20ns (min)
- Low power dissipation: 0.25 mW/bit
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout *	Read

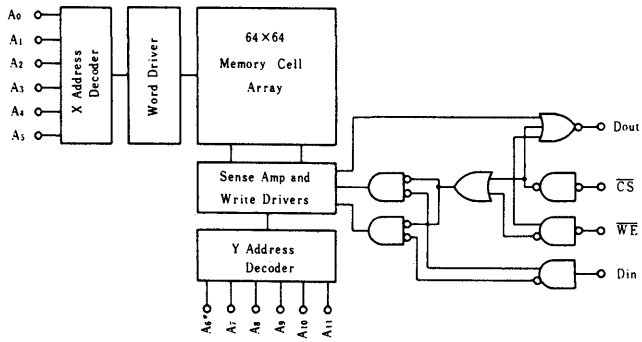
Notes) × : Irrelevant
* : Read Out Nonivert

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	℃
Storage Temperature	T_{stg} (Bias)*	−55 to +125	℃

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / V_{IN} = V_{ILB}	0 to +75°C	0.5	—	170	
		Other		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	Ta = 0°C	−260	−220	—	mA
			Ta = 75°C	—	−210	—	

● AC CHARACTERISTICS (V_{EE} = −5.2V±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	—	8	ns
Chip Select Recovery Time	t_{RCS}		—	—	8	ns
Address Access Time	t_{AA}		—	—	20	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} = 3ns	20	—	—	ns
Data Setup Time	t_{WSD}		3	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	ns
Address Setup Time	t_{WSA}	t_W = 20ns	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		3	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	ns
Write Disable Time	t_{WS}		—	—	8	ns
Write Recovery Time	t_{WR}		—	—	22	ns

3. RISE/FALL TIME

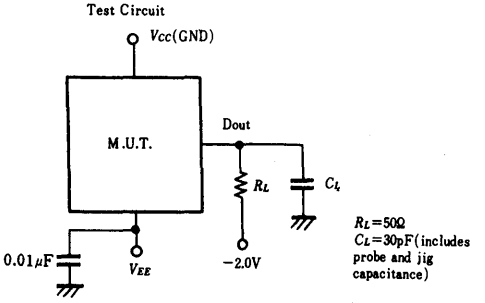
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

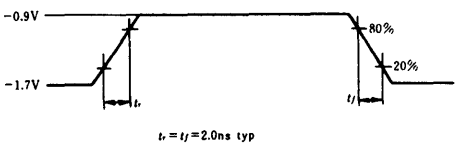
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

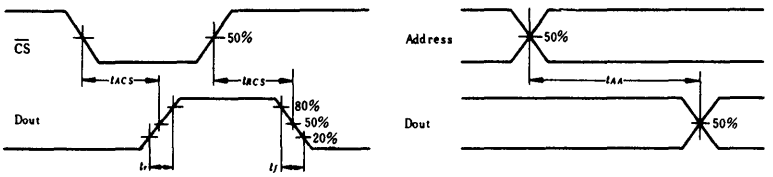
1. LOADING CONDITION



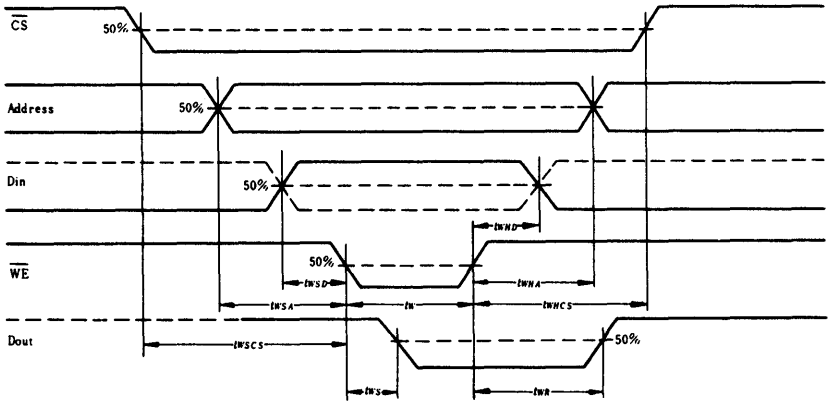
2. INPUT PULSE



3. READ MODE



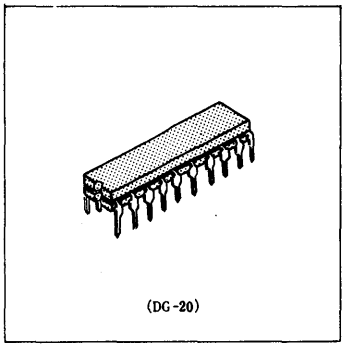
4. WRITE MODE



HM2142

4096-words × 1-bit Very High Speed Random Access Memory

The HM2142 is 4096-words x 1-bit very high speed read/write, random access memory developed for high speed systems such as pads and control/buffer storages.
The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM2142 is encapsulated in cerdip-20 pin package.



■ FEATURES

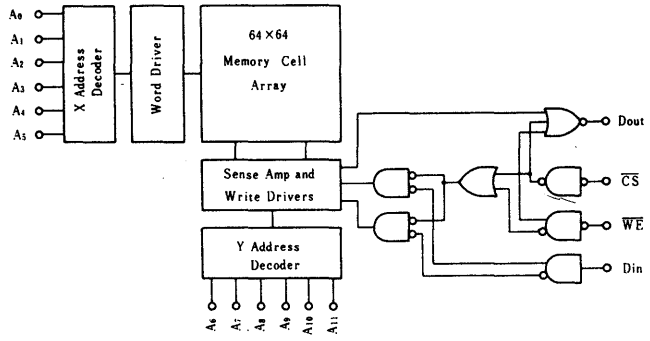
- 4096-words x 1 bit organization
- Very high speed address access time: 10ns (max)
- Write pulse width: 10ns (min)
- Power dissipation: 0.3 mW/bit
- Output obtainable by wired-OR

■ TRUTH TABLE

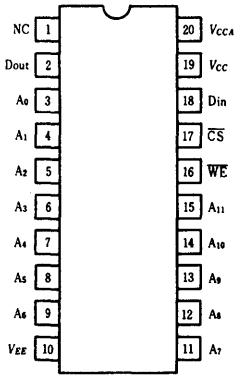
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout *	Read

Notes) × : Irrelevant
* : Read Out Nonivert

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg} (Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE}=−5.2V, R_L=50Ω to −2.0V, Ta=0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{IH}=V_{IHA} or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−980	—	−810	
			+75°C	−950	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IH}=V_{IHB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1165	—	−880	mV
			+25°C	−1165	—	−880	
			+75°C	−1165	—	−880	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1810	—	−1560	
			+25°C	−1810	—	−1560	
			+75°C	−1810	—	−1560	
Input Current	I_{IH}	V_{IN}=V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$	0 to +75°C	0.5	—	170	
		Others		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open.	Ta=0°C	−270	−240	—	mA
			Ta=75°C	—	−220	—	

● AC CHARACTERISTICS (V_{EE}=−5.2V±5%, Ta=0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	—	6	ns
Chip Select Recovery Time	t_{RCS}		—	—	6	ns
Address Access Time	t_{AA}		—	—	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA}=3ns	10	—	—	ns
Data Setup Time	t_{WSD}		1	—	—	ns
Data Hold Time	t_{WHD}		1	—	—	ns
Address Setup Time	t_{WSA}	t_W=10ns	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		1	—	—	ns
Chip Select Hold Time	t_{WHCS}		1	—	—	ns
Write Disable Time	t_{WS}		—	—	6	ns
Write Recovery Time	t_{WN}		—	—	6	ns

3. RISE/FALL TIME

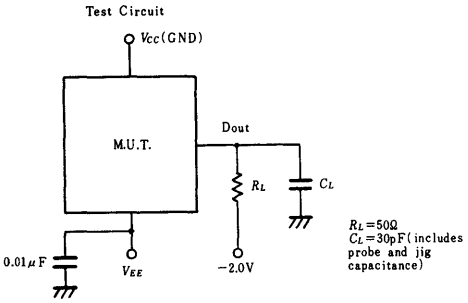
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

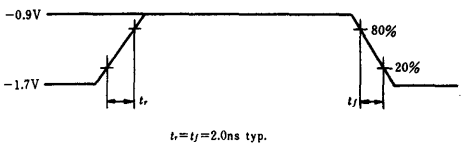
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}^{*}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

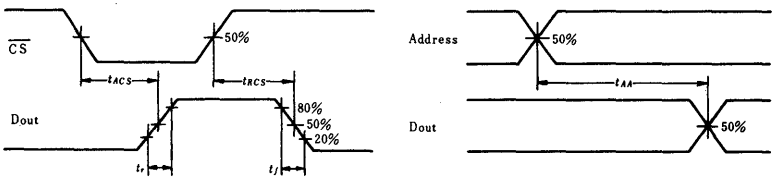
1. LOADING CONDITION



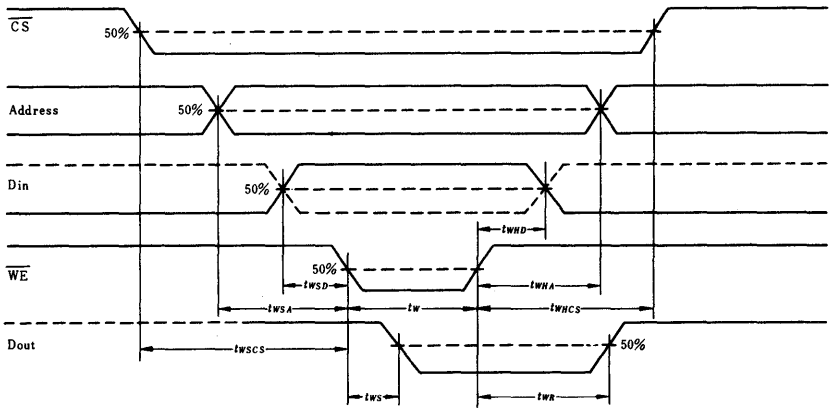
2. INPUT PULSE



3. READ MODE



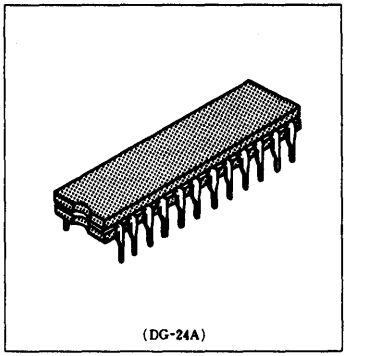
4. WRITE MODE



HM10474

1024-word×4-bit Fully Decoded Random Access Memory

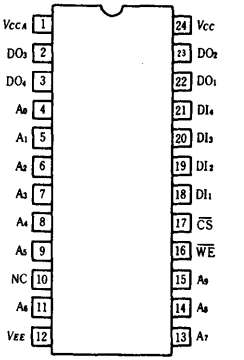
The HM10474 is ECL 10k compatible, 1024-words x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.
The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM10474 is encapsulated in cerdip-24pin package, compatible with Fairchild's F10474.


(DG-24A)

■ FEATURES

- 1024-word x 4-bit organization
- Fully compatible with 10K ECL level
- Address access time: HM10474 25ns (max)
- Write pulse width: HM10474 25ns(min)
- Low power dissipation: 0.2mW/bit
- Output obtainable by wired-OR (open emitter)

■ PIN ARRANGEMENT



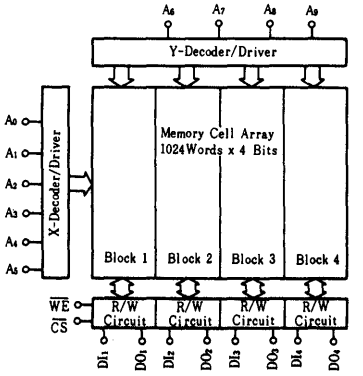
(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Nonivert

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / V_{IN} = V_{ILB}	0 to +75°C	0.5	—	170	
		Others		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	Ta = 0°C	−200	−160	—	mA
			Ta = 75°C	—	−145	—	

●AC CHARACTERISTICS (V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM10474			Unit
			min	typ	max	
Chip Select Access Time	t_{ACS}		—	—	10	ns
Chip Select Recovery Time	t_{RCS}		—	—	10	ns
Address Access Time	t_{AA}		—	15	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM10474			Unit
			min	typ	max	
Write Pulse Width	t_W	t_{WSA} = 3ns	25	15	—	ns
Data Setup Time	t_{WSD}		2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	ns
Address Setup Time	t_{WSA}	t_W = $t_{W\,min}$	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	ns
Write Disable Time	t_{WS}		—	—	10	ns
Write Recovery Time	t_{WR}		—	—	27	ns

3. RISE/FALL TIME

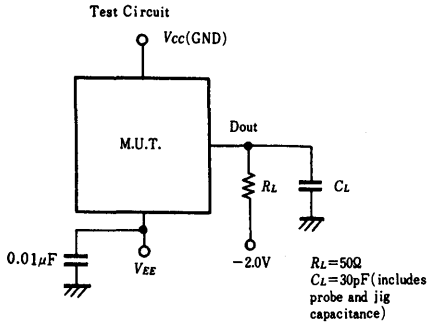
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

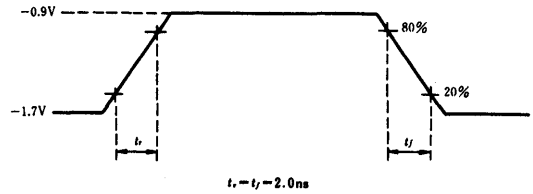
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

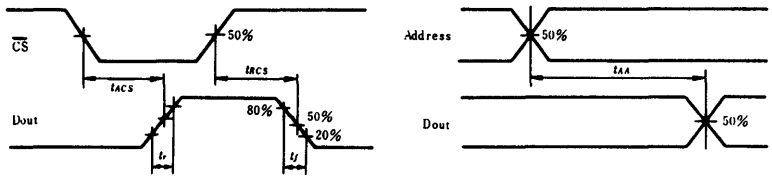
1. LOADING CONDITION



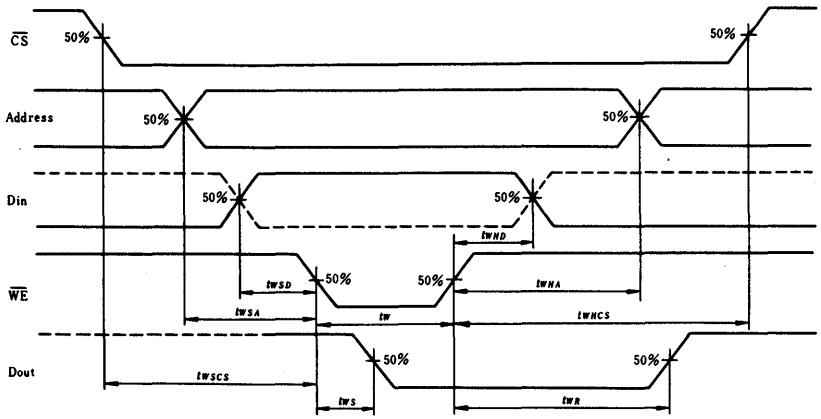
2. INPUT PULSE



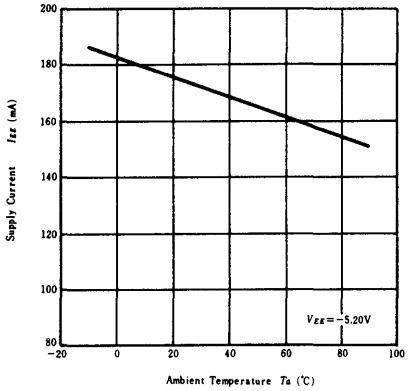
3. READ MODE



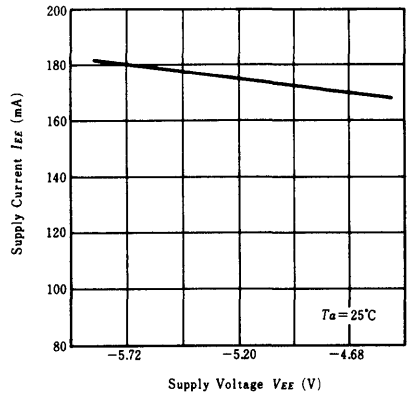
4. WRITE MODE



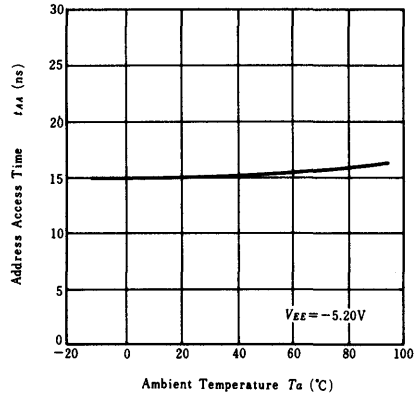
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



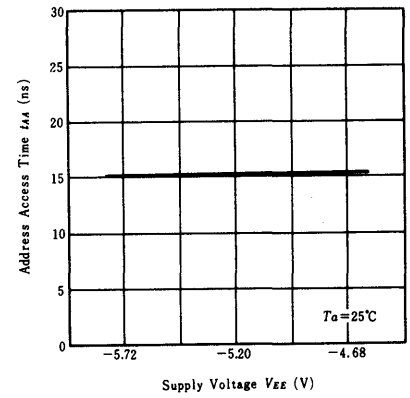
SUPPLY CURRENT vs. SUPPLY VOLTAGE



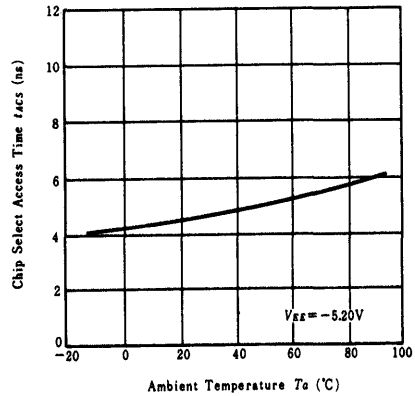
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



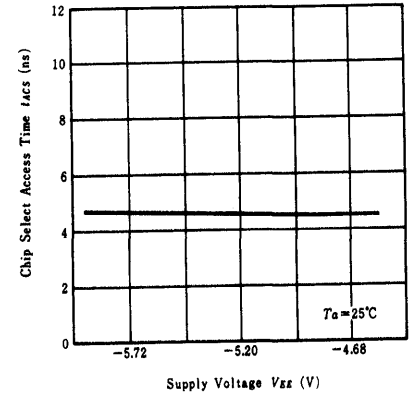
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



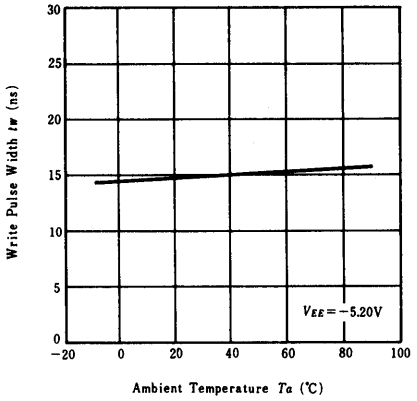
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



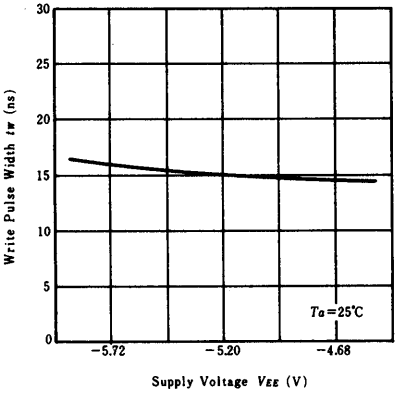
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



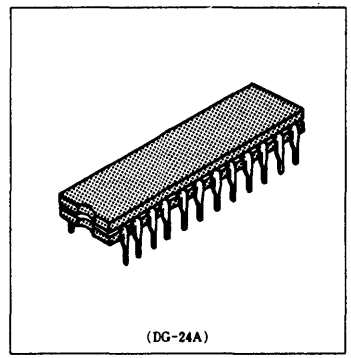
HM10474-8,HM10474-10 Under Development

1024-word×4-bit Fully Decoded Random Access Memory

The HM10474 is ECL 10k compatible, 1024-words x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10474 is encapsulated in cerdip-24pin package, compatible with Fairchild's F10474.

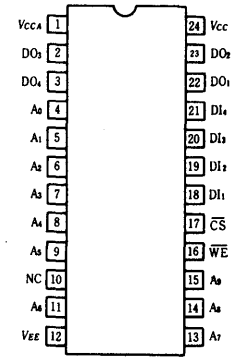


(DG-24A)

■FEATURES

- 1024-word x 4-bit organization
- Fully compatible with 10K ECL level
- Address access time: HM10474-8 8ns (max)
  HM10474-10 10ns (max)
- Write pulse width: HM10474-8 5ns (min)
  HM10474-10 5ns (min)
- Low power dissipation: 0.3mW/bit
- Output obtainable by wired-OR (open emitter)

■PIN ARRANGEMENT



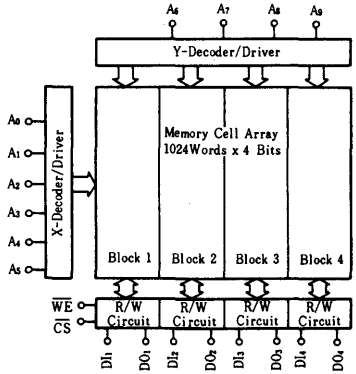
(Top View)

■TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Nonivert

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

Note)
The specifications of this device are subject to change without notice.
Please contact your nearest Hitachis Sales Dept, regarding specifications.

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$	V_{IN} = V_{ILB} 0 to +75°C	0.5	—	170	
		Others		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	Ta = 0°C	−240	−220	—	mA
			Ta = 75°C	—	−205	—	

● AC CHARACTERISTICS (V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM10474-8			HM10474-10			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	—	5	—	—	6	ns
Chip Select Recovery Time	t_{RCS}		—	—	5	—	—	6	ns
Address Access Time	t_{AA}		—	—	8	—	—	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM10474-8			HM10474-10			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA} = 2ns	5	—	—	5	—	—	ns
Data Setup Time	t_{WSD}		1	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		1	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	t_W = $t_{W\,min}$	2	—	—	2	—	—	ns
Address Hold Time	t_{WHA}		1	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		1	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		1	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	5	—	—	5	ns
Write Recovery Time	t_{WR}		—	—	9	—	—	12	ns

3. RISE/FALL TIME

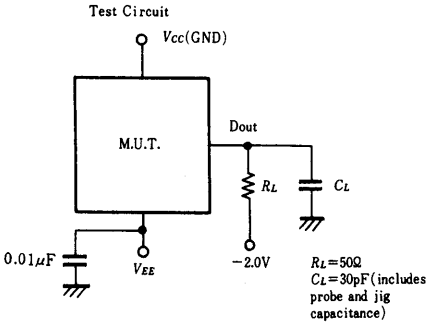
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

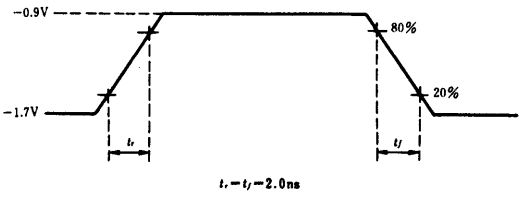
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

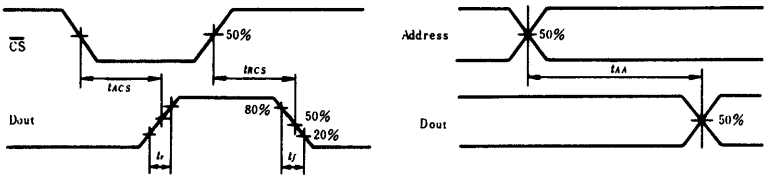
1. LOADING CONDITION



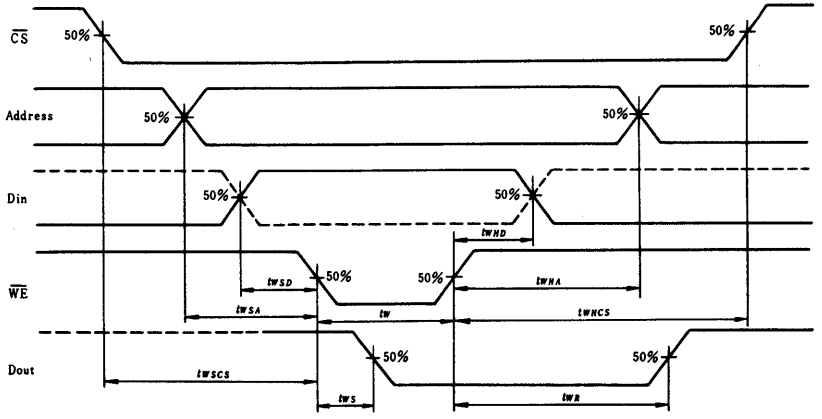
2. INPUT PULSE



3. READ MODE



4. WRITE MODE

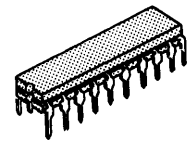


HM10480,HM10480F

16,384-words × 1-bit Fully Decoded Random Access Memory

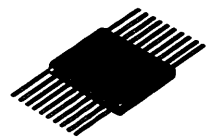
The HM10480 is ECL 10K compatible, 16,384-words x 1-bit, read/write random access memory developed for high speed systems such as scratch pads and control/buffer storages.
The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM10480 is encapsulated in cerdip-20 pin and flat 20-pin package, compatible with Fairchild's F10480.

HM10480



(DG-20)

HM10480F



(FG-20)

■FEATURES

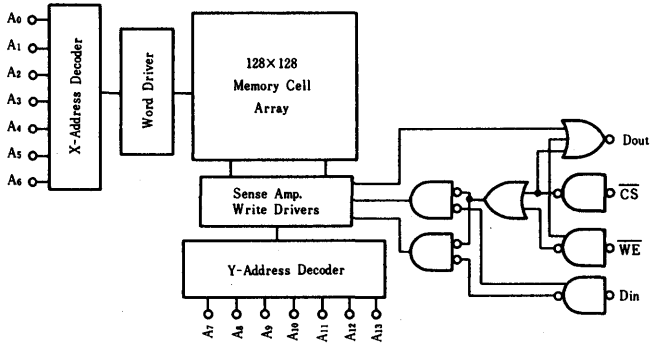
- 16,384-words x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: 25ns (max)
- Write pulse width: 25ns(min)
- Low power dissipation: 0.05mW/bit
- Output obtainable by wired-OR (open emitter)

■TRUTH TABLE

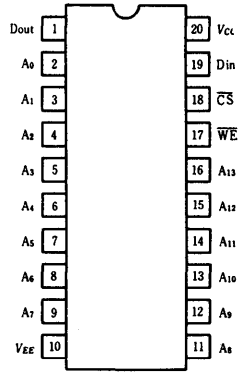
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Noninvert

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	℃
Storage Temperature	T_{stg}(Bias)*	−55 to +125	℃

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$	V_{IN} = V_{ILB} 0 to +75°C	0.5	—	170	
		Others		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 10	Ta = 0°C	−170	−140	—	mA
			Ta = 75°C	—	−130	—	

●AC CHARACTERISTICS (V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		2	—	10	ns
Chip Select Recovery Time	t_{RCS}		2	—	10	ns
Address Access Time	t_{AA}		3	15	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} = 5ns	25	—	—	ns
Data Setup Time	t_{WSD}		5	—	—	ns
Data Hold Time	t_{WHD}		5	—	—	ns
Address Setup Time	t_{WSA}	t_W = 25ns	5	—	—	ns
Address Hold Time	t_{WHA}		5	—	—	ns
Chip Select Setup Time	t_{WSCS}		5	—	—	ns
Chip Select Hold Time	t_{WHCS}		5	—	—	ns
Write Disable Time	t_{WS}		—	—	10	ns
Write Recovery Time	t_{WR}		—	—	10	ns

3. RISE/FALL TIME

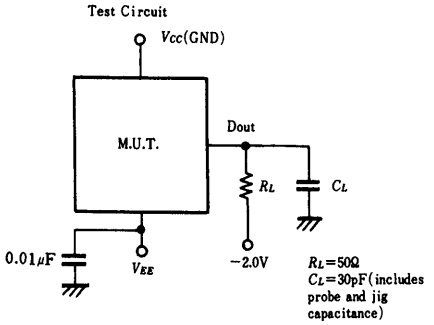
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

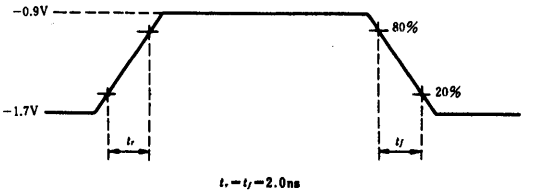
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

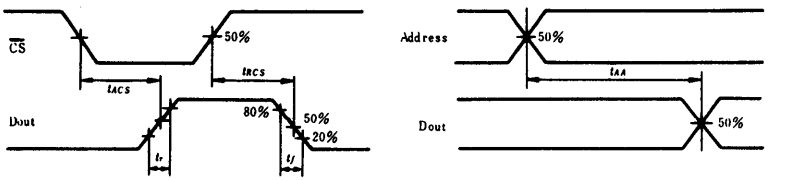
1. LOADING CONDITION



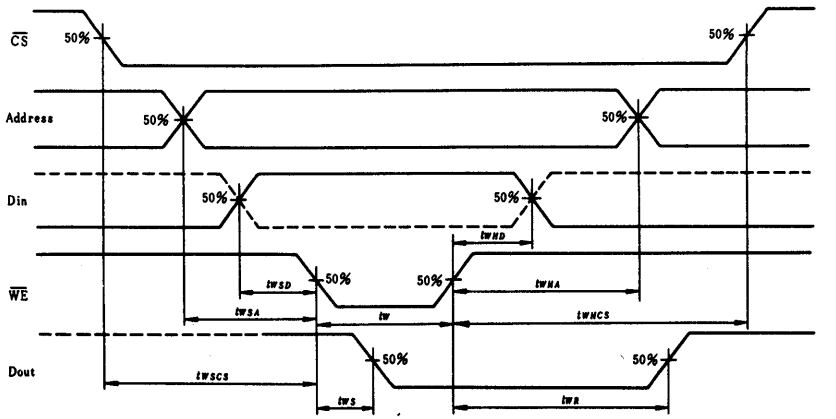
2. INPUT PULSE



3. READ MODE



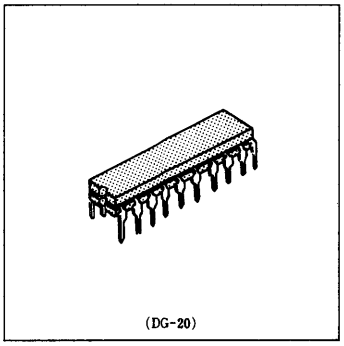
4. WRITE MODE



HM10480-15,HM10480-20 Under Development

16,384-words×1-bit Fully Decoded Random Access Memory

The HM10480 is ECL 10K compatible, 16,384-words x 1-bit, read/write random access memory developed for high speed systems such as scratch pads and control/buffer storages.
The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM10480 is encapsulated in cerdip-20 pin package, compatible with Fairchild's F10480.

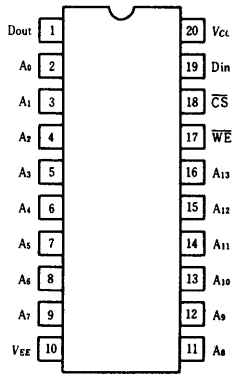


(DG-20)

■FEATURES

- 16,384-words x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: HM10480-15 15ns (max)
  HM10480-20 20ns (max)
- Write pulse width: HM10480-15 15ns (min)
  HM10480-20 20ns (min)
- Low power dissipation: 0.06mW/bit
- Output obtainable by wired-OR (open emitter)

■PIN ARRANGEMENT



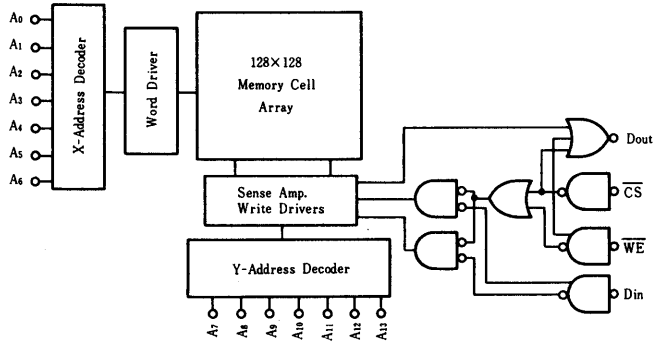
(Top View)

■TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Noninvert

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

Note)
The specifications of this device are subject to change without notice.
Please contact your nearest Hitachis Sales Dept, regarding specifications.

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN}=V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / $V_{IN}=V_{ILB}$	0 to +75°C	0.5	—	170	
		Others		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 10	Ta=0°C	−240	−220	—	mA
			Ta=75°C	—	−200	—	

● AC CHARACTERISTICS (V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM10480-15			HM10480-20			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		2	—	8	2	—	10	ns
Chip Select Recovery Time	t_{RCS}		2	—	8	2	—	10	ns
Address Access Time	t_{AA}		3	12	15	3	15	20	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM10480-15			HM10480-20			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA}=2ns	15	—	—	20	—	—	ns
Data Setup Time	t_{WSD}		3	—	—	3	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	$t_W=t_W$ min	3	—	—	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		3	—	—	3	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	8	—	—	10	ns
Write Recovery Time	t_{WR}		—	—	17	—	—	22	ns

3. RISE/FALL TIME

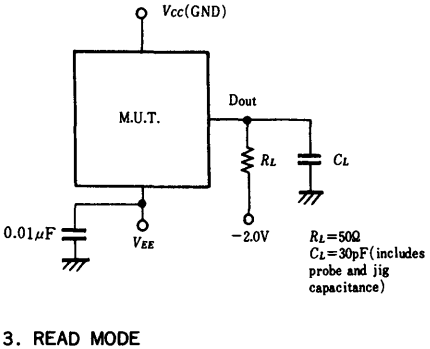
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

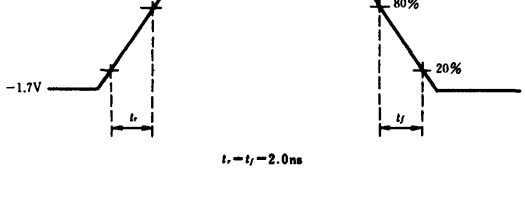
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

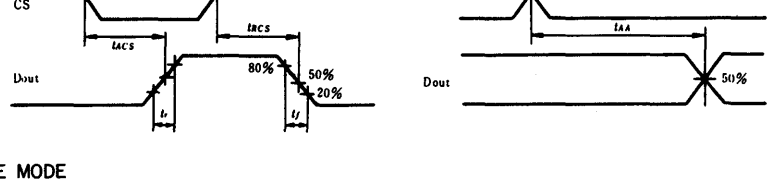
1. LOADING CONDITION



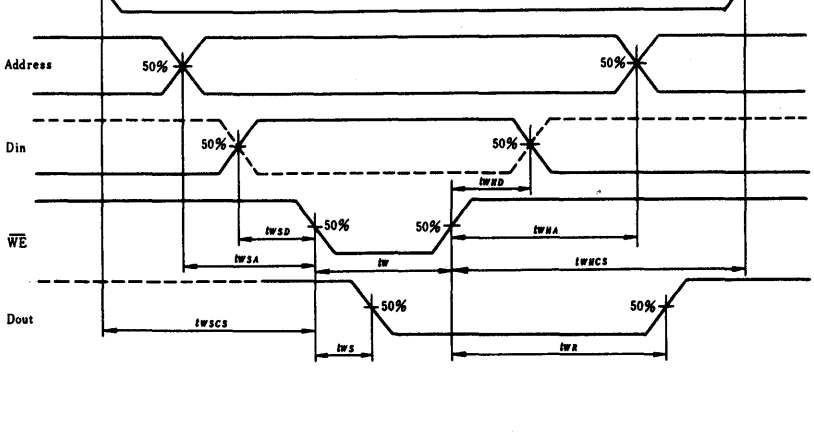
2. INPUT PULSE



3. READ MODE



4. WRITE MODE

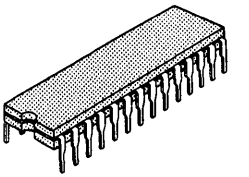


HM10484-15,HM10484-20

4096-word x 4-bit Fully Decoded Random Access Memory

Under Development

The HM10484 is ECL 10K compatible, 4096 words x 4-bit read write, random access memory developed for high speed systems such as scratch pads and control/buffer storage. The fabrication process is the Hitachi's low capacitance U-groove isolation method with double metalization. The HM10484 is encapsulated in cerdip-28 pin package.



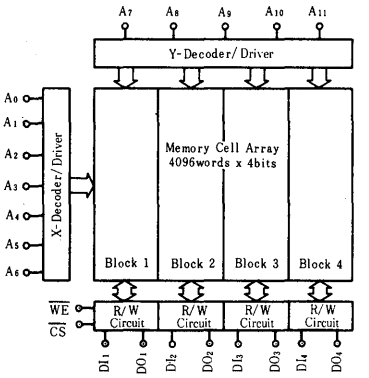
(DG-28A)

■ TRUTH TABLE

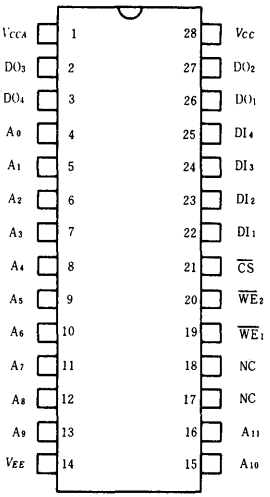
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Nonivert

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN} = V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / $V_{IN} = V_{ILB}$	0 to +75°C	0.5	—	170	
		Others		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 10	Ta = 0°C	−240	—	—	mA
			Ta = 75°C	—	—	—	

● AC CHARACTERISTICS (V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM10484-15			HM10484-20			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		2	—	8	2	—	10	ns
Chip Select Recovery Time	t_{RCS}		2	—	8	2	—	10	ns
Address Access Time	t_{AA}		3	12	15	3	15	20	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM10484-15			HM10484-20			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA} = 2ns	15	—	—	20	—	—	ns
Data Setup Time	t_{WSD}		3	—	—	3	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	$t_W = t_W$ min	3	—	—	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		3	—	—	3	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	8	—	—	10	ns
Write Recovery Time	t_{WR}		—	—	17	—	—	22	ns

3. RISE/FALL TIME

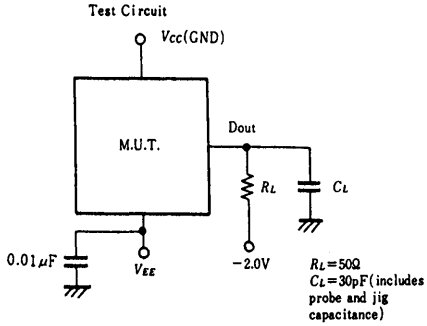
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

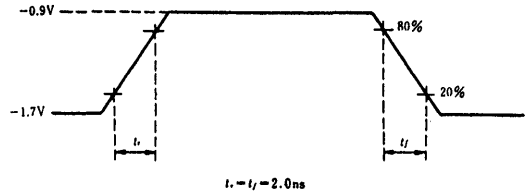
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

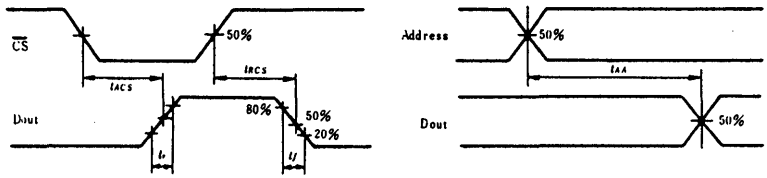
1. LOADING CONDITION



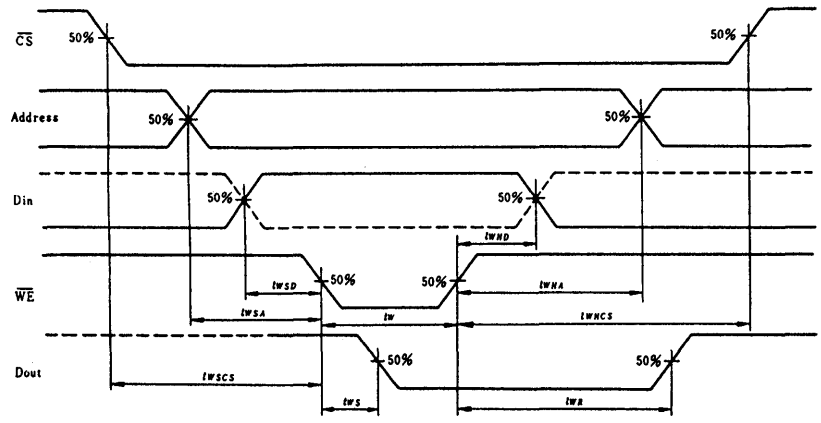
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



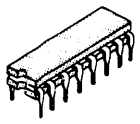
HM100415,HM100415CC

1024-word×1-bit Fully Decoded Random Access Memory

The HM100415 is a 1024-word x 1-bit, read/write random access memory developed for application to scratch pads, control and buffer storages which require very high speeds.

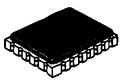
The HM100415 is compatible with the HD100K families and includes on-chip voltage and temperature compensation for improved noise margin. This memory is encapsulated in cerdip-16pin package.

HM100415



(DG-16A)

HM100415CC



(CC-24)

■FEATURES

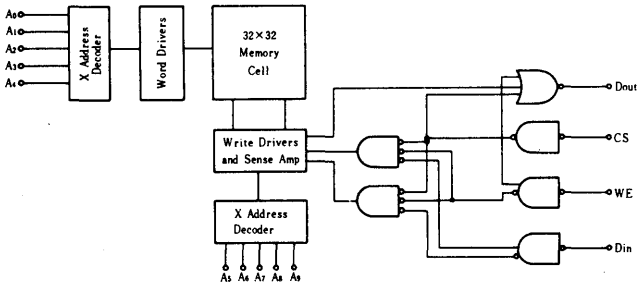
- Level ..... 100K ECL Compatible
- Organization ..... 1024-word by 1-bit
- Address Access Time ..... 10ns (max)
- Chip Select Access Time ..... 5ns (max.)
- Power Consumption ..... 0.6mW/bit (typ)
- Output Obtainable by Wired-OR (open emitter)
- Compatible with Fairchild F100415.

■TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

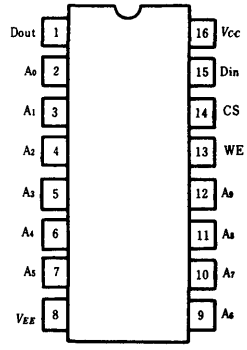
Notes) × : Irrelevant
* : Read Out Noninvert

■BLOCK DIAGRAM



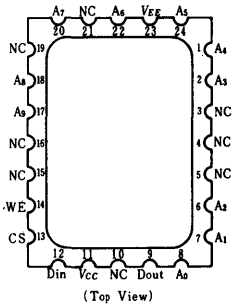
■PIN ARRANGEMENT

●HM100415



(Top View)

●HM100415CC



(Top View)

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE} = −4.5V, R_L = 50Ω to −2.0V, Ta = 0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	$V_{in} = V_{IHA}$ or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{in} = V_{IHB}$ or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs		−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV
Input Current	I_{IH}	$V_{in} = V_{IHA}$		—	—	220	μA
	I_{IL}	$V_{in} = V_{ILB}$	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−150	—	mA

● AC CHARACTERISTICS (V_{EE} = −4.5V ±5%, Ta = 0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	3	5	ns
Chip Select Recovery Time	t_{RCS}		—	3	5	ns
Address Access Time	t_{AA}		—	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} = 2ns	6	4	—	ns
Data Setup Time	t_{WSD}		2	0	—	ns
Data Hold Time	t_{WHD}		2	0	—	ns
Address Setup Time	t_{WSA}	t_W = 6ns	2	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	ns
Chip Select Setup Time	t_{WSCS}		2	0	—	ns
Chip Select Hold Time	t_{WHCS}		2	0	—	ns
Write Disable Time	t_{WS}		—	3	5	ns
Write Recovery Time	t_{WR}		—	3	5	ns

3. RISE/FALL TIME

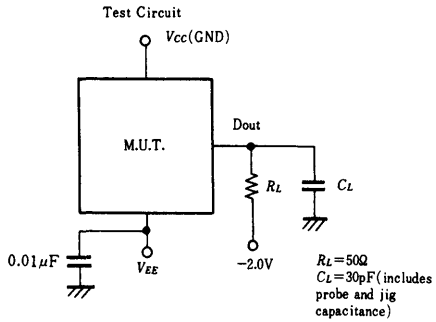
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

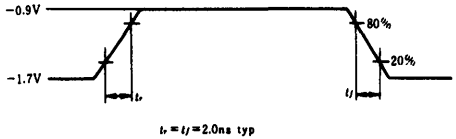
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

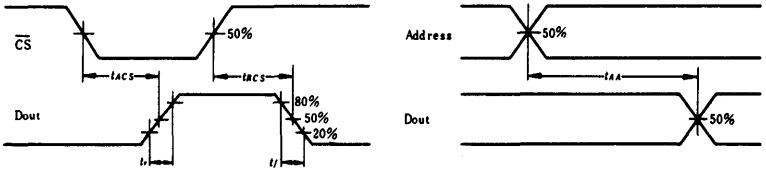
1. LOADING CONDITION



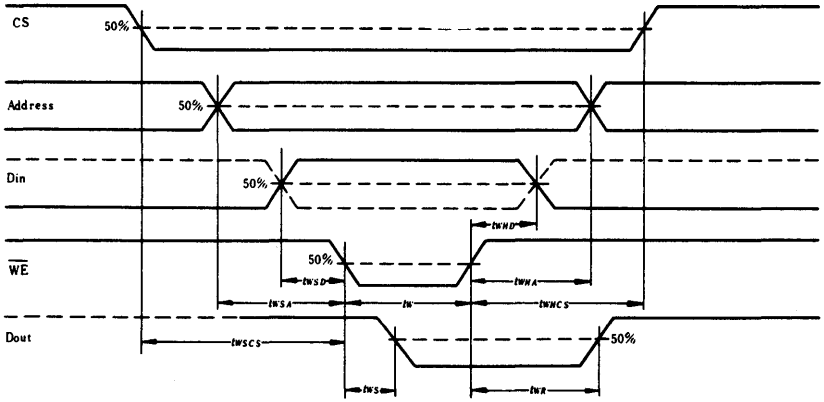
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



HM100422,HM100422F
HM100422CC

256-word×4-bit Fully Decoded Random Access Memory

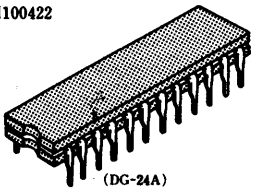
The HM100422 is ECL 100K compatible, 256-word x 4-bit, read write, random access memory developed for high speed system such as scratch pads and control/buffer storages.

Four active Low Block Select lines are provided to select each block independently.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

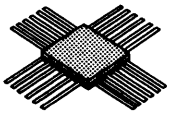
The HM100422 is encapsulated in cerdip-24pin package, or 24pin flat package compatible with Fairchild's F100422.

HM100422



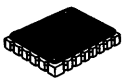
(DG-24A)

HM100422F



(FG-24)

HM100422CC



(CC-24)

■ FEATURES

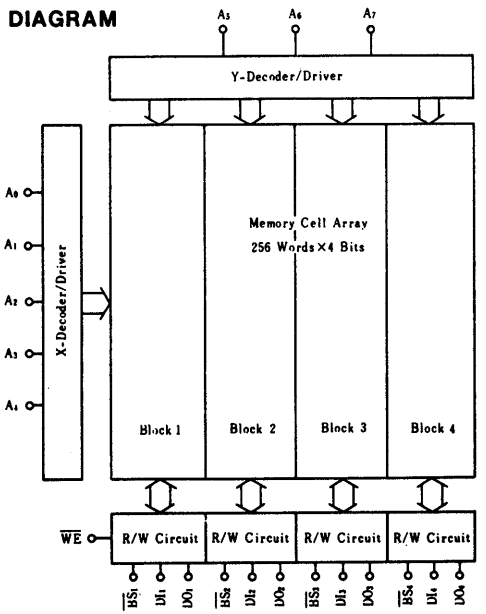
- 256-word x 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: 10ns (max.)
- Minimum write pulse width: 6ns (min.)
- Low power dissipation: 0.8mW/bit
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

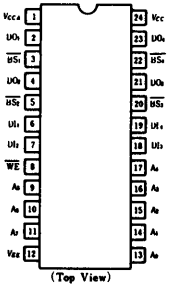
Notes) × : Irrelevant
* : Read Out Noninvert

■ BLOCK DIAGRAM



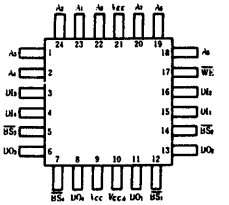
■ PIN ARRANGEMENT

●HM100422



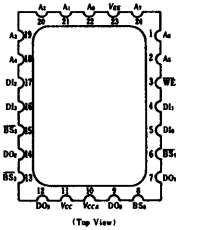
(Top View)

●HM100422F



(Top View)

●HM100422CC



(Top View)

HITACHI

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE}=−4.5V, R_L=50Ω to −2.0V, Ta=0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{in}=V_{IHA}$ or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{in}=V_{IHB}$ or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage		−1165	—	−880	mV
	V_{IL}	High/Low for All Inputs		−1810	—	−1475	mV
Input Current	I_{IH}	$V_{in}=V_{IHA}$		—	—	220	μA
	I_{IL}	$V_{in}=V_{ILB}$	$\overline{BS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−165	—	mA

● AC CHARACTERISTICS (V_{EE}=−4.5V ±5%, Ta=0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Block Select Access Time	t_{ABS}		—	—	5	ns
Block Select Recovery Time	t_{RBS}		—	—	5	ns
Address Access Time	t_{AA}		—	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA}=2ns	6	4.5	—	ns
Data Setup Time	t_{WSD}		2	0	—	ns
Data Hold Time	t_{WHD}		2	0	—	ns
Address Setup Time	t_{WSA}	t_W=6ns	2	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	ns
Block Select Setup Time	t_{WSBS}		2	0	—	ns
Block Select Hold Time	t_{WHBS}		2	0	—	ns
Write Disable Time	t_{WS}		—	4	5	ns
Write Recovery Time	t_{WR}		—	4.5	9	ns

3. RISE/FALL TIME

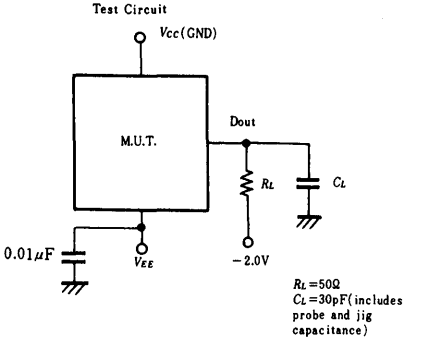
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

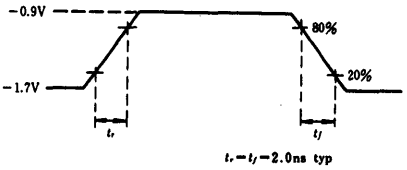
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

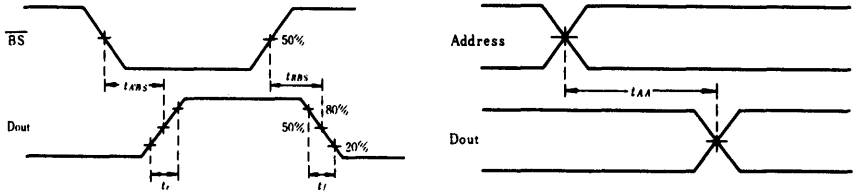
1. LOADING CONDITION



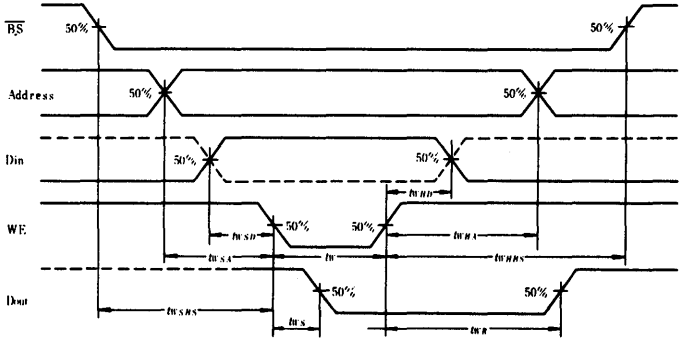
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



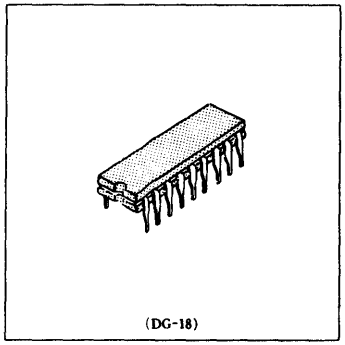
HM100470

4096-word×1-bit Fully Decoded Random Access Memory

The HM100470 is a 4096-words x 1-bit, read/write, random access memory developed for high speed systems such as scratch pads and control buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM100470 is compatible with the HD100K ECL families and includes on-chip voltage and temperature compensation for improved noise margin. This device is encapsulated in cerdip-18pin package, compatible with Fairchild's F100470.



(DG-18)

■FEATURES

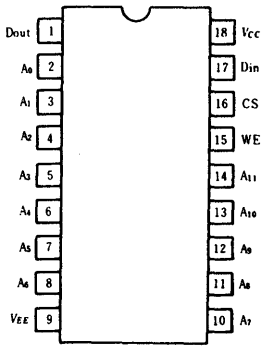
- 4096-word x 1-bit organization
- Full compatible with 100K ECL level
- Address access time: 25ns(max)
- Write pulse width: 25ns (min)
- Output obtainable by wired-OR (open emitter)

■TRUTH TABLE

Input			Output	Mode
CS	WE	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

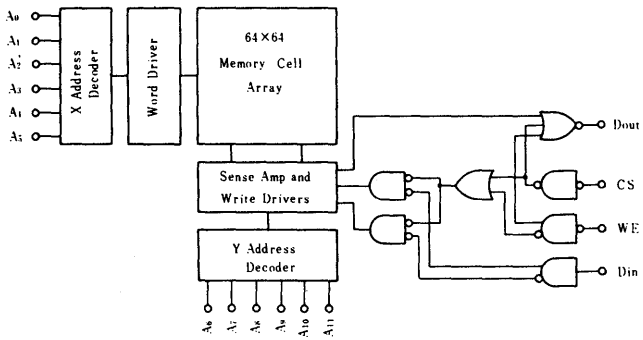
Notes) × : Irrelevant
* : Read Out Nonivert

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE} = −4.5V, R_L = 50Ω to −2.0V, Ta = 0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	$V_{in} = V_{IHA}$ or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{in} = V_{IHB}$ or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs		−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV
Input Current	I_{IH}	$V_{in} = V_{IHA}$		—	—	220	μA
	I_{IL}	$V_{in} = V_{ILB}$	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−165	—	mA

● AC CHARACTERISTICS (V_{EE} = −4.5V ±5%, Ta = 0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	—	10	ns
Chip Select Recovery Time	t_{RCS}		—	—	10	ns
Address Access Time	t_{AA}		—	—	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WAS} = 3ns	25	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	ns
Address Setup Time	t_{WSA}	$t_W = t_W$ min	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	ns
Write Disable Time	t_{WS}		—	—	10	ns
Write Recovery Time	t_{WR}		—	—	10	ns

3. RISE/FALL TIME

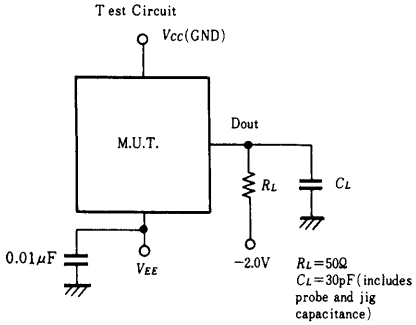
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

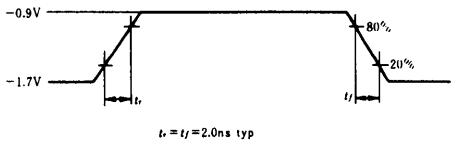
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

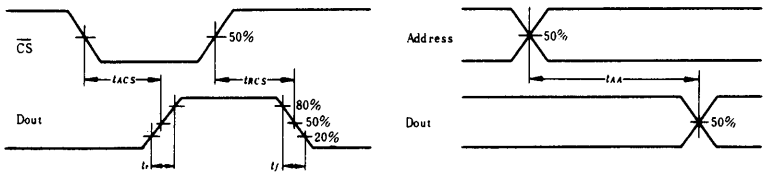
1. LOADING CONDITION



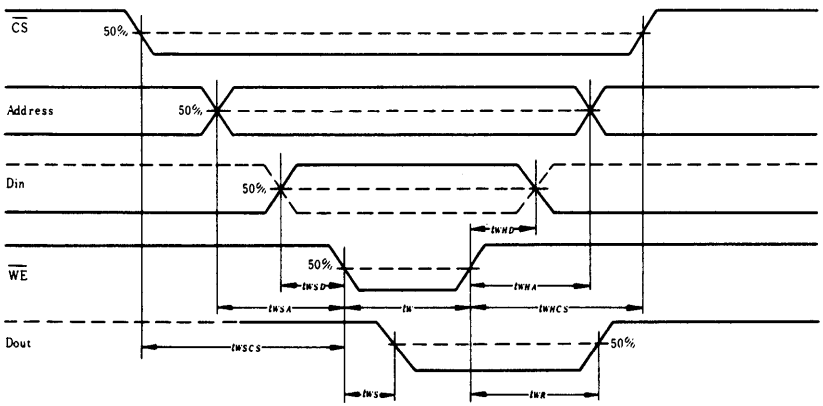
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



HM100474, HM100474F

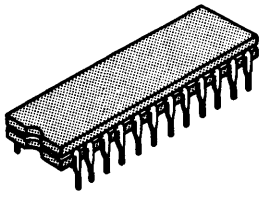
1024-word×4-bit Fully Decoded Random Access Memory

The HM100474 is a 1024-words x 4-bit, read/write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

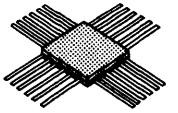
The HM100474 is compatible with the HD100K ECL families and includes on-chip voltage and temperature compensation for improved noise margin. This device is encapsulated in cerdip-24-pin and flat 24pin package, compatible with Fairchild's F100474.

HM100474



(DG-24A)

HM100474F



(FG-24)

■FEATURES

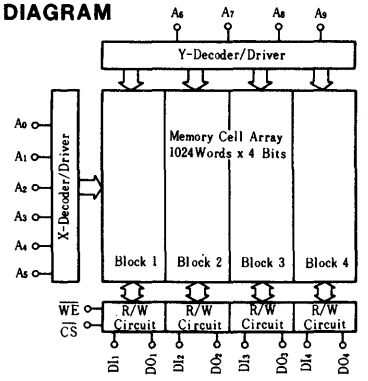
- 1024-word x 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: HM100474/F 25ns(max)
- Write pulse width: HM100474/F 25ns(min)
- Output obtainble by wired-OR (open emitter)

■TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Nonivert

■BLOCK DIAGRAM



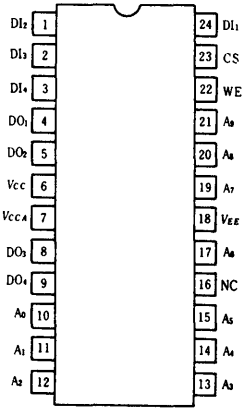
■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

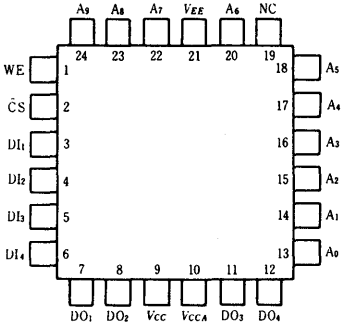
■PIN ARRANGEMENT

●HM100474



(Top View)

●HM100474F



(Top View)

HITACHI

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −4.5V, R_L = 50Ω to −2.0V, Ta = 0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{in} = V_{IHA}$ or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{in} = V_{IHB}$ or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs		−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV
Input Current	I_{IH}	$V_{in} = V_{IHA}$		—	—	220	μA
	I_{IL}	$V_{in} = V_{ILB}$	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−165	—	mA

●AC CHARACTERISTICS (V_{EE} = −4.5V ±5%, Ta = 0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM100474/F			Unit
			min	typ	max	
Chip Select Access Time	t_{ACS}		—	—	10	ns
Chip Select Recovery Time	t_{RCS}		—	—	10	ns
Address Access Time	t_{AA}		—	15	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM100474/F			Unit
			min	typ	max	
Write Pulse Width	t_W	t_{WSA} = 3ns	25	15	—	ns
Data Setup Time	t_{WSD}		2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	ns
Address Setup Time	t_{WSA}	t_W = twmin	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	ns
Write Disable Time	t_{WS}		—	—	10	ns
Write Recovery Time	t_{WR}		—	—	27	ns

3. RISE/FALL TIME

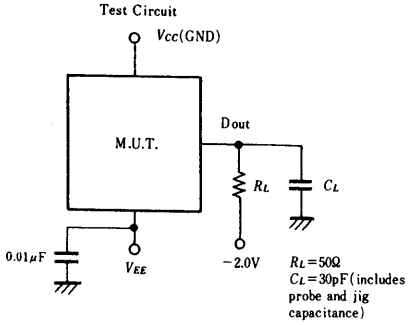
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

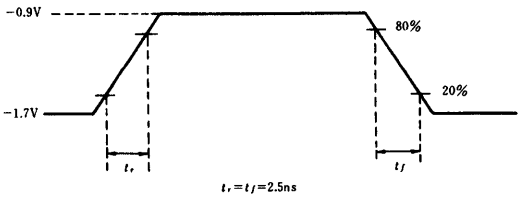
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

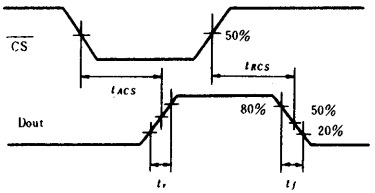
1. LOADING CONDITION

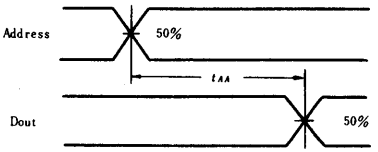


2. INPUT PULSE

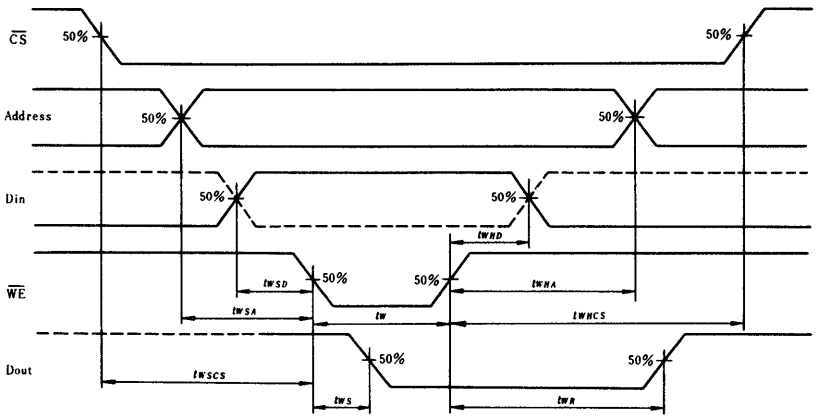


3. READ MODE

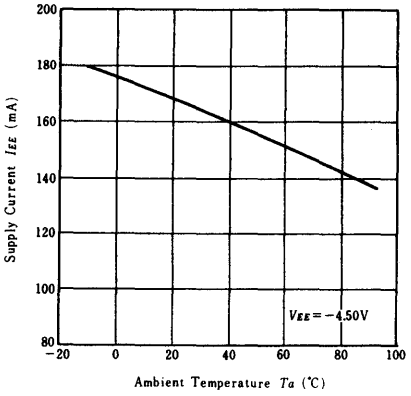




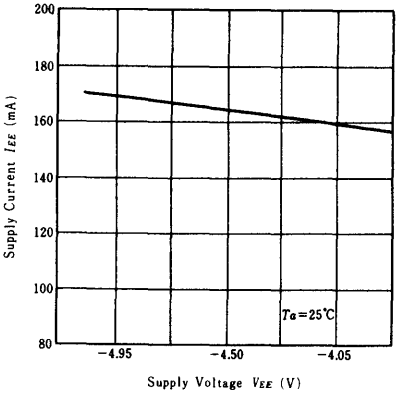
4. WRITE MODE



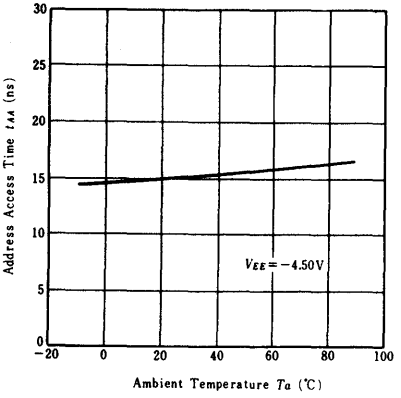
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



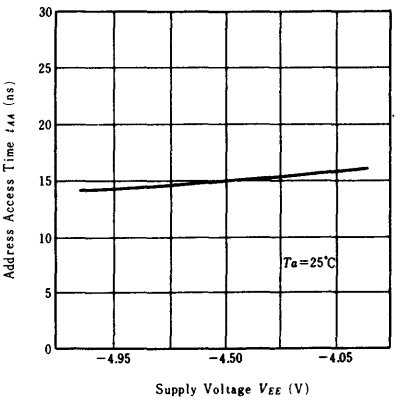
SUPPLY CURRENT vs. SUPPLY VOLTAGE



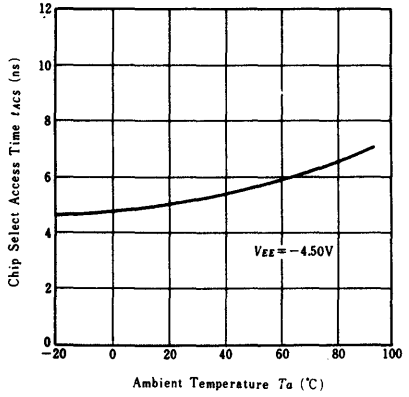
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



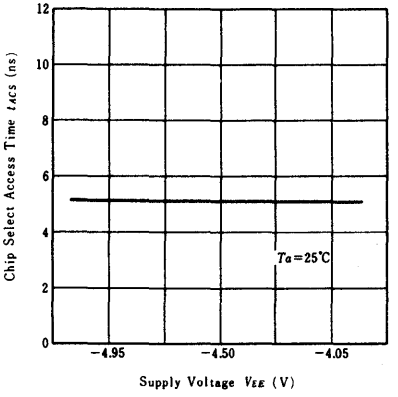
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



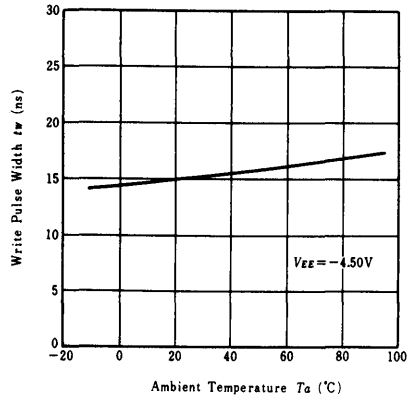
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



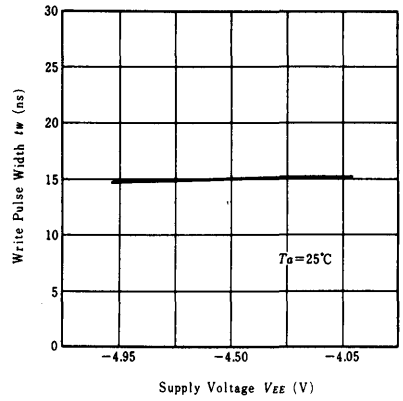
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE

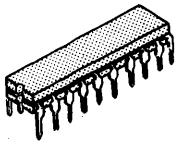


HM100480, HM100480F

16,384-words×1-bit Fully Decoded Random Access Memory

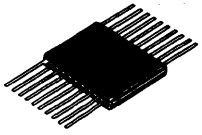
The HM100480 is ECL 100K compatible, 16,384-words x 1-bit, read/write random access memory developed for high speed systems such as scratch pads and control/buffer storages.
The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM100480 is encapsulated in cerdip-20 pin and flat-20 pin package, compatible with Fairchild's 100480.

HM100480



(DG-20)

HM100480F



(FG-20)

■FEATURES

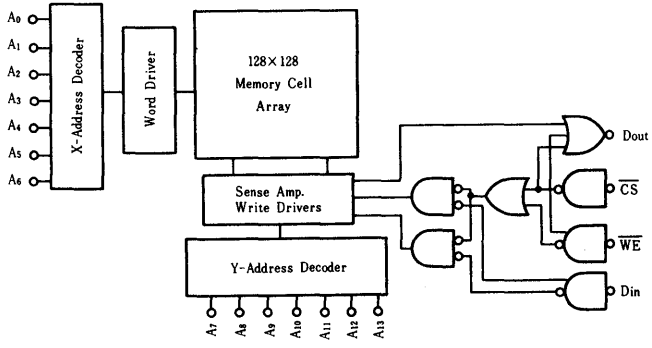
- 16,384-words x 1-bit organization
- Fully compatible with 100K ECL level
- Address access time: 25ns (max)
- Write pulse width: 25ns (min)
- Low power dissipation: 0.05mW/bit
- Output obtainable by wired-OR (open emitter)

■TRUTH TABLE

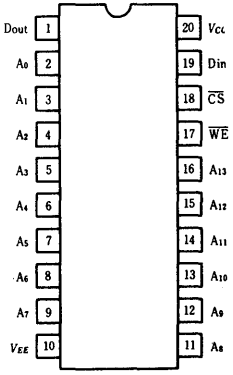
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selcted
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : irrelevant
* : Read Out Noninvert

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS(V_{EE}=−4.5V, R_L=50Ω to −2.0V, Ta=0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{in}=V_{IHA} or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	V_{in}=V_{IHB} or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage		−1165	—	−880	mV
	V_{IL}	High/Low for All Input		−1810	—	−1475	mV
Input Current	I_{IH}	V_{in}=V_{IHA}		—	—	220	μA
	I_{IL}	V_{in}=V_{ILB}	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−165	—	mA

●AC CHARACTERISTICS (V_{EE}=−4.5V±5%, Ta=0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		2	—	10	ns
Chip Select Recovery Time	t_{RCS}		2	—	10	ns
Address Access Time	t_{AA}		3	—	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA}=5ns	25	—	—	ns
Data Setup Time	t_{WSD}		5	—	—	ns
Data Hold Time	t_{WHD}		5	—	—	ns
Address Setup Time	t_{WSA}	t_W=t_W min	5	—	—	ns
Address Hold Time	t_{WHA}		5	—	—	ns
Chip Select Setup Time	t_{WSCS}		5	—	—	ns
Chip Select Hold Time	t_{WHCS}		—	—	5	ns
Write Disable Time	t_{WS}		—	—	10	ns
Write Recovery Time	t_{WR}		—	—	10	ns

3. RISE/FALL TIME

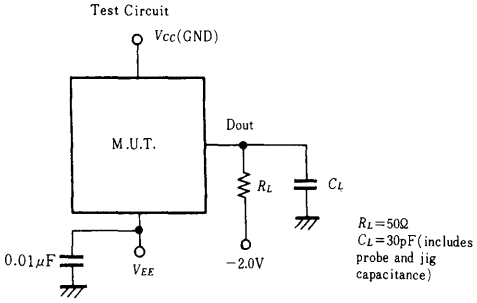
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

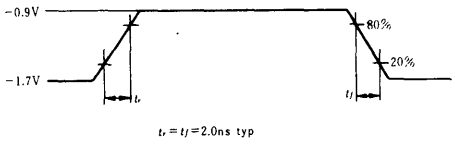
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

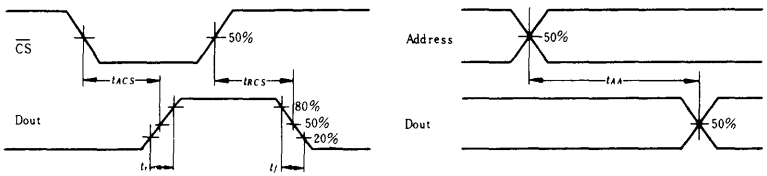
1. LOADING CONDITION



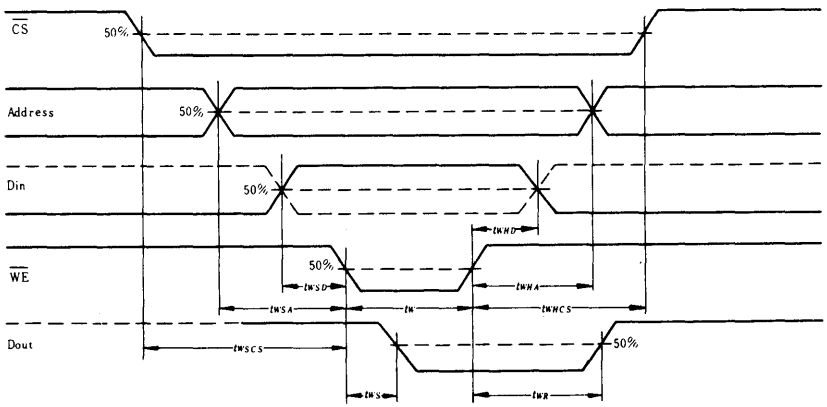
2. INPUT PULSE



3. READ MODE



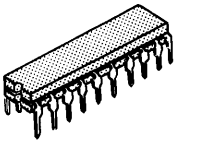
4. WRITE MODE



HM100480-15,HM100480-20

16,384-words×1-bit Fully Decoded Random Access Memory Under Development

The HM100480 is ECL 100K compatible, 16,384-words x 1-bit, read/write random access memory developed for high speed systems such as scratch pads and control/buffer storages.
The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM100480 is encapsulated in cerdip-20 pin package, compatible with Fairchild's 100480.

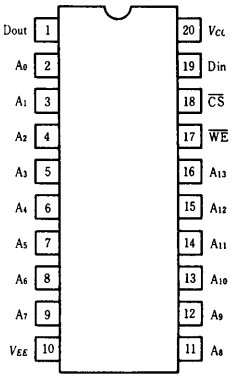


(DG-20)

■FEATURES

- 16,384-words x 1-bit organization
- Fully compatible with 100K ECL level
- Address access time: HM100480-15 15ns (max)
  HM100480-20 20ns (max)
- Write pulse width: HM100480-15 15ns (min)
  HM100480-20 20ns (min)
- Low power dissipation: 0.06mW/bit
- Output obtainable by wired-OR (open emitter)

■PIN ARRANGEMENT



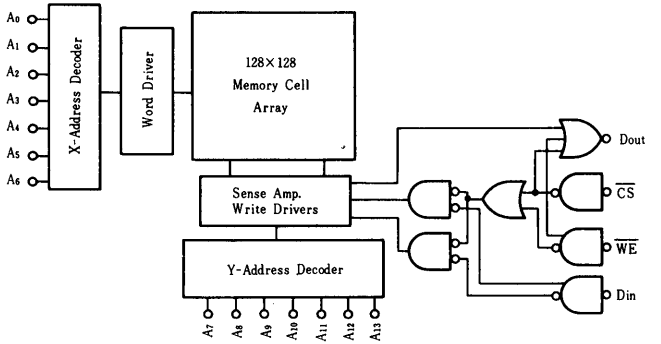
(Top View)

■TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : irrelevant
* : Read Out Noninvert

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

HITACHI

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE}=−4.5V, R_L=50Ω to −2.0V, Ta=0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{in}=V_{IHA} or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	V_{in}=V_{IHB} or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage		−1165	—	−880	mV
	V_{IL}	High/Low for All Input		−1810	—	−1475	mV
Input Current	I_{IH}	V_{in}=V_{IHA}		—	—	220	μA
	I_{IL}	V_{in}=V_{ILB}	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	—	—	mA

●AC CHARACTERISTICS (V_{EE}=−4.5V±5%, Ta=0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM100480-15			HM100480-20			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		2	–	8	2	–	10	ns
Chip Select Recovery Time	t_{RCS}		2	–	8	2	–	10	ns
Address Access Time	t_{AA}		3	–	15	3	–	20	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM100480-15			HM100480-20			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA} = 3ns	15	–	–	20	–	–	ns
Data Setup Time	t_{WSD}		3	–	–	3	–	–	ns
Data Hold Time	t_{WHD}		2	–	–	2	–	–	ns
Address Setup Time	t_{WSA}	t_W = t_W min	3	–	–	3	–	–	ns
Address Hold Time	t_{WHA}		2	–	–	2	–	–	ns
Chip Select Setup Time	t_{WSCS}		3	–	–	3	–	–	ns
Chip Select Hold Time	t_{WHCS}		2	–	–	2	–	–	ns
Write Disable Time	t_{WS}		–	–	8	–	–	10	ns
Write Recovery Time	t_{WR}		–	–	17	–	–	22	ns

3. RISE/FALL TIME

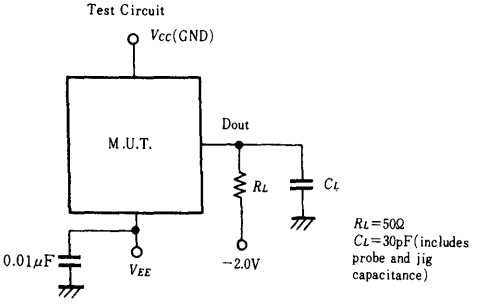
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

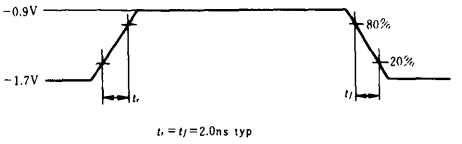
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

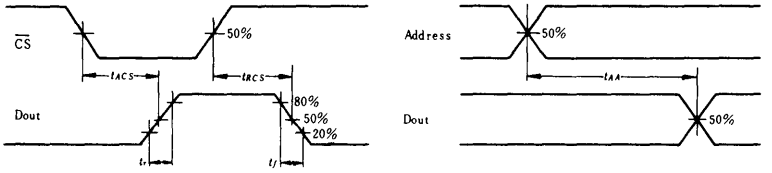
1. LOADING CONDITION



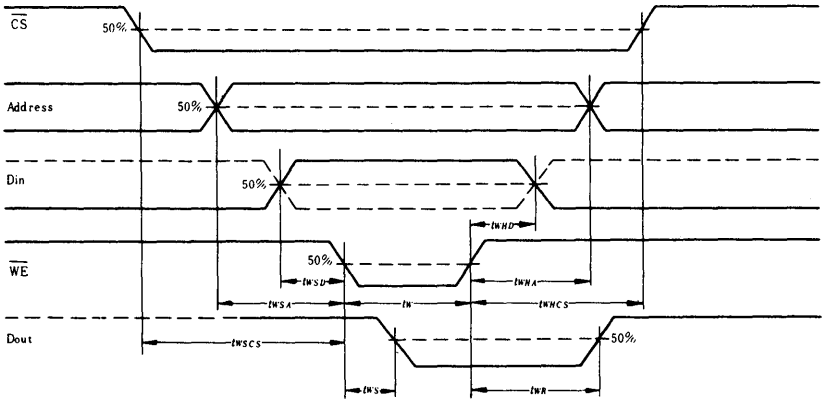
2. INPUT PULSE



3. READ MODE



4. WRITE MODE

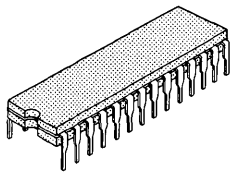


HM100484-15,HM100484-20

4096-word x 4-bit Fully Decoded Random Access Memory

Under Development

The HM100484 is ECL 100K compatible, 4096-words by 4-bits read/write random access memory developed for high speed systems such as acratch pads and control/buffer storage. The fabrication process is the Hitachi's low capacitance U-groove isolation method with double metalization. The HM100484 is encapsulated in cerdip -28 pin package.



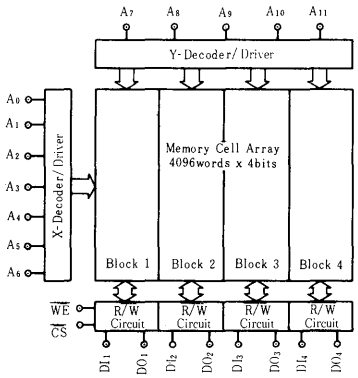
(DG-28A)

■ TRUTH TABLE

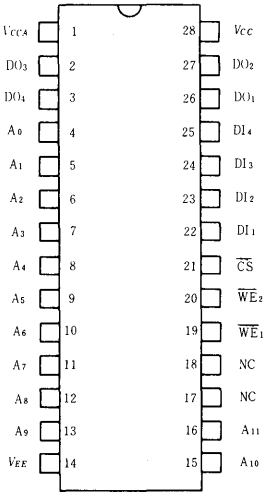
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Nonivert

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE}=−4.5V, R_L=50Ω to −2.0V, Ta=0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{in}=V_{IHA} or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	V_{in}=V_{IHB} or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage		−1165	—	−880	mV
	V_{IL}	High/Low for All Inputs		−1810	—	−1475	mV
Input Current	I_{IH}	V_{in}=V_{IHA}		—	—	220	μA
	I_{IL}	V_{in}=V_{ILB}	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−240	—	—	mA

●AC CHARACTERISTICS (V_{EE}=−4.5V ±5%, Ta=0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM100484-15			HM100484-20			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	—	8	—	—	10	ns
Chip Select Recovery Time	t_{RCS}		—	—	8	—	—	10	ns
Address Access Time	t_{AA}		—	—	15	—	—	20	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM100484/15			HM100484-20			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA}=3ns	15	—	—	20	—	—	ns
Data Setup Time	t_{WSD}		3	—	—	3	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	t_W=twmin	3	—	—	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		3	—	—	3	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	8	—	—	10	ns
Write Recovery Time	t_{WR}		—	—	17	—	—	22	ns

3. RISE/FALL TIME

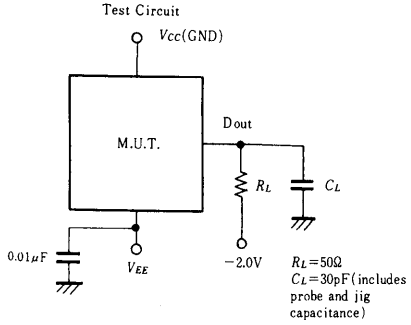
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

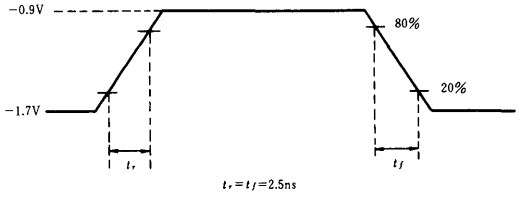
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

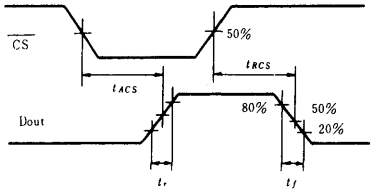
1. LOADING CONDITION

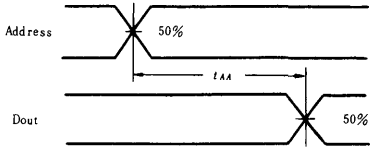


2. INPUT PULSE

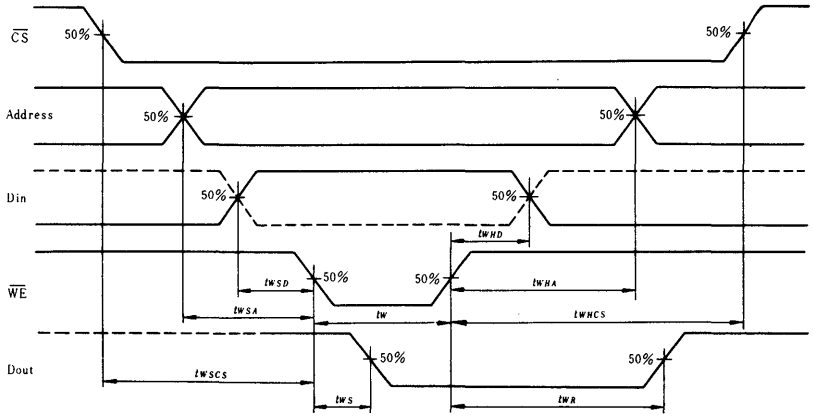


3. READ MODE





4. WRITE MODE



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MAY 1985

Printed in U.S.A.