HITACHI

4-BIT SINGLE-CHIP MICROCOMPUTER DATA BOOK

ADVANCE COPY

#AP1

4-BIT SINGLE-CHIP MICROCOMPUTER DATABOOK

HITACHI

This advance data has been preliminarily prepared based on manuscript translated in Japan. Use this information with caution, therefore, as the accuracy of the copy cannot be guaranteed. A revised, U.S. edition of this technical data is currently in preparation, and may be ordered by returning the Business Reply Card at the back of this publication.

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INDEX

NOTE: No new designs for HMCS 42/43/44A/45A/47A/42C/42CL/43C/43CL accepted after April 1984.

GENERAL INFORMATION

- Quick Reference Guide
- Introduction of Packages
- Quality Assurance
- Reliability Test Data
- Design Procedure and Support Tools for 8-bit Single-chip Microcomputers

QUICK REFERENCE GUIDE

■ CMOS 4-BIT SINGLE-CHIP MICROCOMPUTER HMCS40 SERIES

	Family Name (Type Name)			HMCS44CL (HD44808) HMCS44C (HD44801)		HMCS45CL (HD44828) HMCS45C (HD44820)	
LSI Characteristics	Supply Voltage		(V)	3/5		3/5	
	Power Dissipation (typ.)		(mW)	0.4/0.9		0.4/0.9	
	Max. I/O Terminal Voltage		(V)	V_{CC}+0.3		V_{CC}+0.3	
	Operating Temperature Range *1		(°C)	-20 to+75		-20 to +75	
	Package			DP-42, DP-42S		FP-54, DP-64S	
Functions	Memory	ROM	(bits)	2,048 x 10 128x10*2		2,048 x 10 128x10*2	
		RAM	(bits)	160 x 4		160 x 4	
	Registers			8		6	
	Stack Registers			4		4	
	I/O Ports	4-Bit Data Input		32	–	44	–
		4-Bit Data Output			–		4 x 1
		Discrete Output			–		–
		4-Bit Data Input/Output			4 x 4		4 x 6
		Discrete Input/Output			1 x 16		1 x 16
	Interrupts	External		2		2	
		Timer/Counter		1		1	
	Instructions	Number of Instructions		71		71	
		Cycle Time	(μs)	20/10		20/10	
	Built-in Clock Pulse Generator						
	Power on Reset			No/Yes		No/Yes	
	Battery Back-up			Halt		Halt	
Evaluation Chip				HD44850E HD44857E		HD44850E HD44857E	
Reference Page				174		196	

*1 Wide Temperature Range (-40 to +85°C) version is available, except LCD-IV
*2 Pattern Memory
*3 LCD DRIVE FUNCTION

LCD Drive	Common	4
	Segment	32
	Duty	Static, 1/2, 1/3, 1/4
	Bias	1/2, 1/3
Display Capability		4x32 Matrix (1/4 Duty)

Expandable using the LCD Driver HD44100H.

HMCS46CL (HD44848) HMCS46C (HD44840)	HMCS47CL (HD44868) HMCS47C (HD44860)	LCD-III[*3] (HD44795, HD44790)	LCD-IV[*3] (HD613901)
3/5	3/5	3/5	3/5
0.4/9	0.4/9	0.4/6	0.8/13.5
V_{CC}+0.3	V_{CC}+0.3	V_{CC}+0.3	V_{CC}+0.3
-20 to +75	-20 to +75	-20 to +75	-20 to +75
DP-42, DP-42S	FP-54, DP-64S	FP-80	FP-80
4,096 x 10	4,096 x 10	2,048 x 10 128 x 10[*2]	4,096 x 10
256 x 4	256 x 4	160 x 4	256 x 4
8	6	6	6
4	4	4	4
32 –	44 –	32 4 x 1	32 4 x 1
–	4 x 1	4 x 1	4 x 1
–	–	–	–
4 x 4	4 x 6	4 x 2	4 x 2
1 x 16	1 x 16	1 x 16	1 x 16
2	2	2	2
1	1	1	1
71	71	71	71
20/5	20/5	20/10	20/5
Yes			
No/Yes	No/Yes	Yes	No
Halt	Halt	Halt	Halt
HD44857E	HD44857E	HD44797E	HD44797E
218	244	273	310

■ CMOS 4-BIT SINGLE-CHIP MICROCOMPUTER HMCS400 SERIES

	Family Name (Type Name)			HMCS404C (HD614042)	HMCS404AC*	HMCS404CL*	HD614P080S†
LSI Characteristics	Supply Voltage		(V)	4 to 6	4.5 to 6.0	2.7 to 6.0	4.5 to 5.5
	Power Dissipation		(typ) (mW)	9.0	13.5	4.5	9.0
	Max. I/O Terminal Voltage		(V)	V_{CC}-40	V_{CC}-40	V_{CC}-40	V_{CC}-40
	Operating Temperature Range		(°C)	-20 to +75	-20 to +75	-20 to +75	-20 to +75
	Package			FP-64, DP-64S	FP-64, DP-64S	FP-64, DP-64S	DC-64SP
Functions	Memory	ROM	(bits)	4096 x 10	4096 x 10	4096 x 10	∘4,096-word x 10-bit with standard EPROM 2764 ∘8,192-word x 10-bit with standard EPROM 27128
		RAM	(bits)	256 x 4	256 x 4	256 x 4	576 x 4
	Registers			7	7	7	7
	Stack Registers			16	16	16	16
	I/O Ports	4-Bit Input		58 4 x 1 2 x 1	58 4 x 1 2 x 1	58 4 x 1 2 x 1	58 4 x 1 2 x 1
		4-Bit Output		4 x 4	4 x 4	4 x 4	4 x 4
		4-Bit Input/Output		4 x 5	4 x 5	4 x 5	4 x 5
		1-Bit Input/Output		1 x 16	1 x 16	1 x 16	1 x 16
	Interrupts	External		2	2	2	2
		Timer/Counter		2	2	2	2
		Serial Interface		1	1	1	1
	Instructions	Number of Instructions		99	99	99	99
		Cycle Time	(μs)	2	1.33	4	1.33
	Built-in Clock Pulse Generator			Yes (External drive is possible)			
	Others			Low Power Dissipation Mode (Stop mode, Stand-by mode)			
Reference Page				357	394	396	398

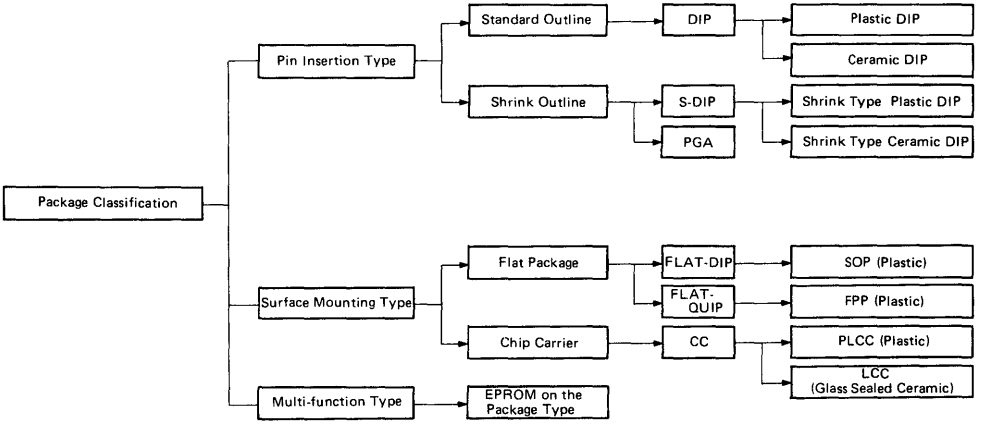
* Under Development
† EPROM on the Package Type

INTRODUCTION OF PACKAGES

Hitachi microcomputer devices are offered in a variety of packages, to meet various user requirements.

1. Package Classification

When selecting suitable packaging, please refer to the Package Classifications given in Fig. 1 for pin insertion, surface mount, and multi-function types, in plastic and ceramic.



DIP; DUAL IN LINE PACKAGE
S-DIP; SHRINK DUAL IN LINE PACKAGE
PGA: PIN GRID ARRAY
FLAT-DIP; FLAT DUAL IN LINE PACKAGE
FLAT-QUIP; FLAT QUAD IN LINE PACKAGE
CC: CHIP CARRIER
SOP; SMALL OUTLINE PACKAGE
FPP; FLAT PLASTIC PACKAGE
PLCC; PLASTIC LEADED CHIP CARRIER
LCC ; LEADLESS CHIP CARRIER

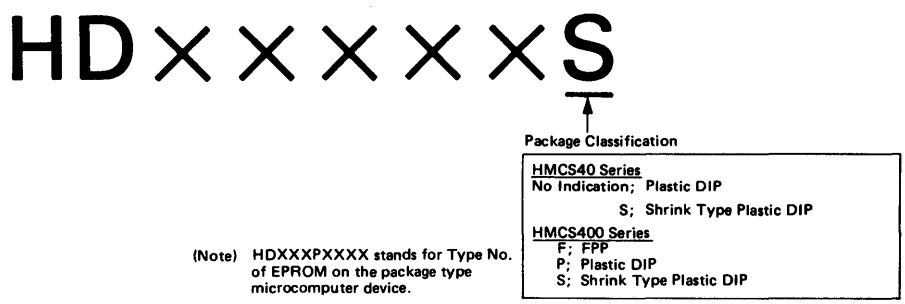
Fig. 1 Package Classification according to Material and Printed Circuit Board Mounting Type

2. Type No. and Package Code Indication

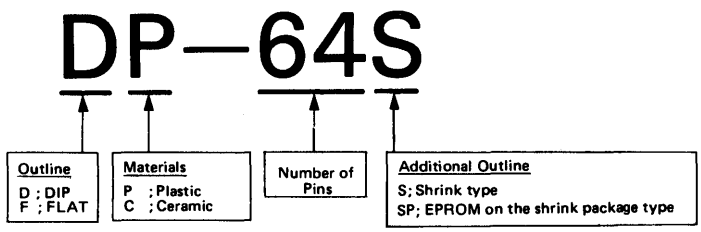
The Hitachi type No. for 4-bit single-chip microcomputer devices is followed by package material and outline specifications, as shown below. The package type used for each device is identified by code as follows, illustrated in the data sheet of each device.

When ordering, please write the package code next to the type number.

Type No. Indication



Package Code Indication



3. Package Dimensional Outline

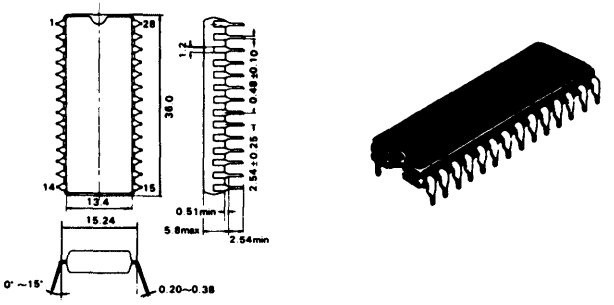
Hitachi 4-bit single-chip microcomputer devices employ the packages shown in Table 1 according to PCB mounting method.

Table 1 Package List

Mounting method	Package classification		Package material	Package code
Pin insertion type	Standard outline (DIP)		Plastic	DP-28 DP-42
	Shrink outline (S-DIP)		Plastic	DP-28S DP-42S DP-64S
Surface mounting type	Flat package	FPP	Plastic	FP-54 FP-64 FP-80 FP-100
		FPC	Ceramic	FC-80
Multi-function type	EPROM on the package type		Ceramic	DC-64SP

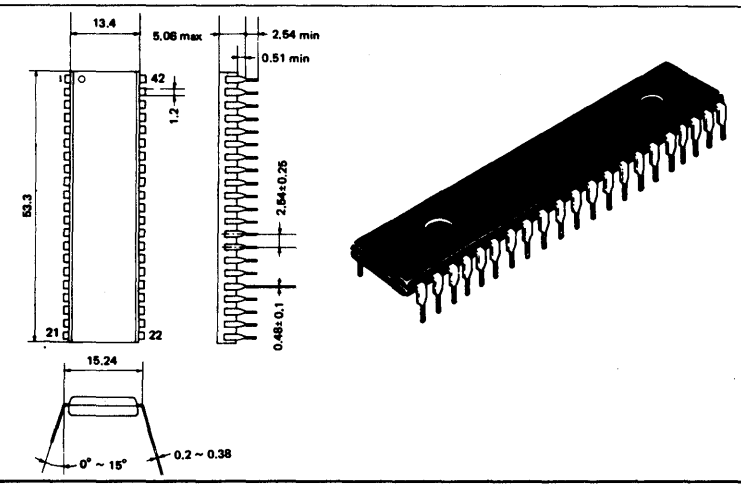
Plastic DIP

- **DP-28**



(Unit: mm)

- **DP-42**

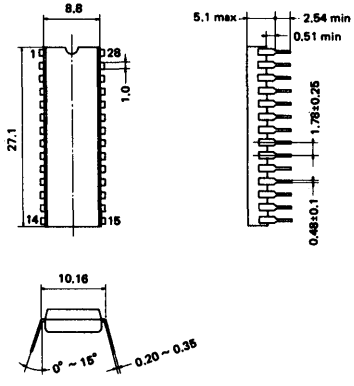


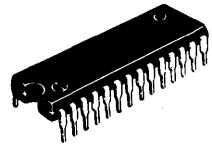
(Unit: mm)

INTRODUCTION OF PACKAGES

Shrink Type Plastic DIP

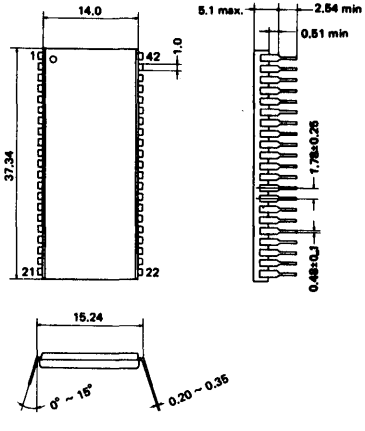
- **DP-28S**

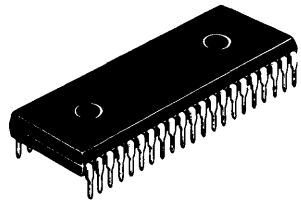




(Unit: mm)

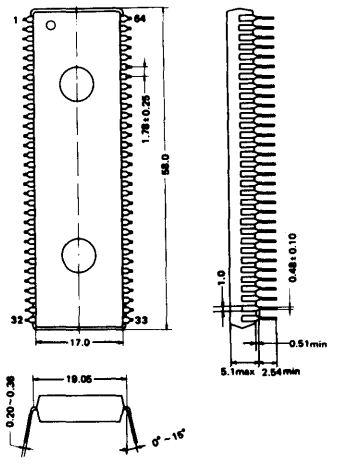
- **DP-42S**

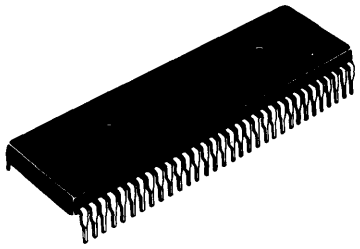




(Unit: mm)

● **DP-64S**

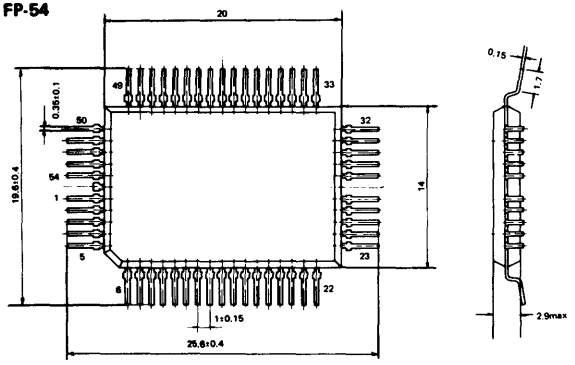


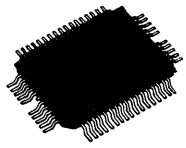


(Unit: mm)

Flat Plastic Package

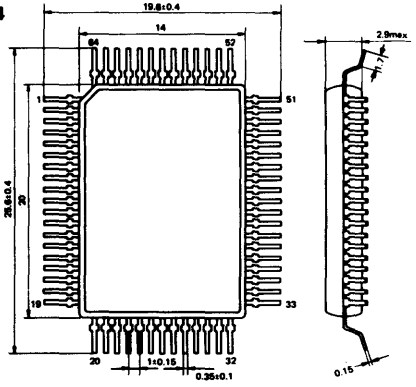
● **FP-54**

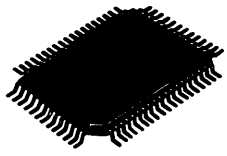




(Unit: mm)

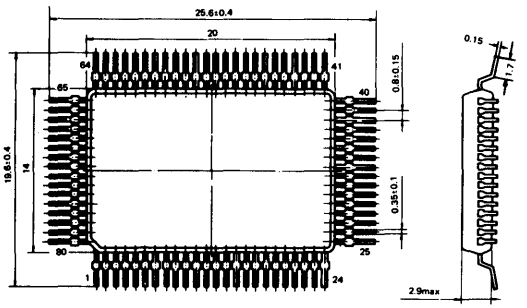
● **FP-64**

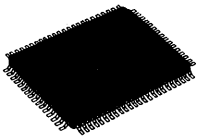




(Unit: mm)

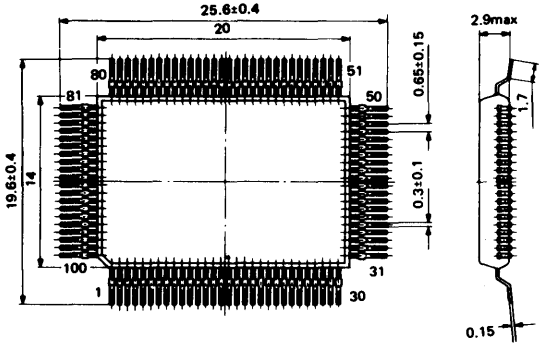
- **FP-80**

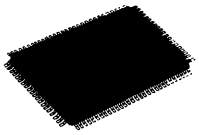




(Unit: mm)

- **FP-100**

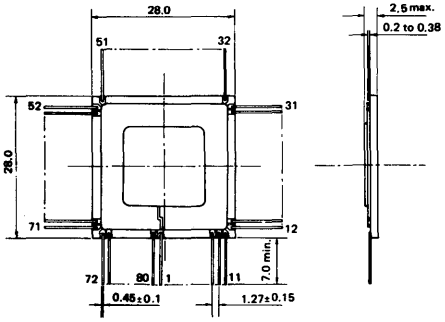


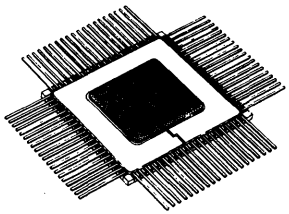


(Unit: mm)

Flat Package of Ceramic

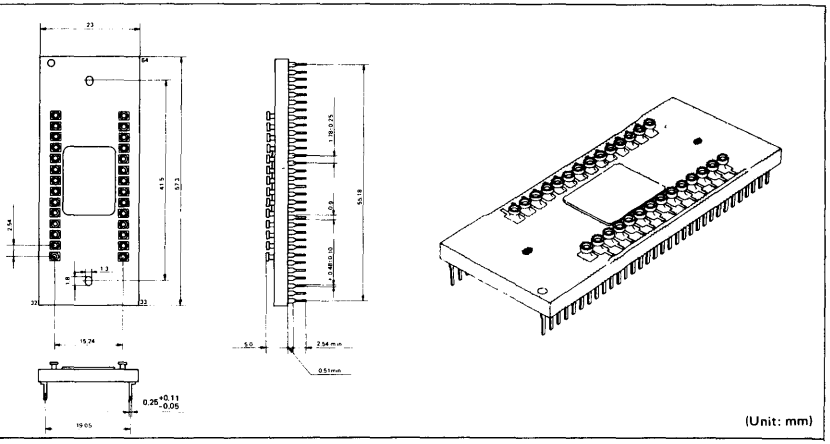
- **FC-80**





(Unit: mm)

• DC-64SP



(Unit: mm)

4. Mounting Method

Package lead pins are surface treated with solder coating or plating to facilitate PCB mounting. The lead pins are connected to the package by eutectic solder. Common connecting method of leads and precautions are explained as follows:

4.1 Mounting Methods of Pin Insertion Type Package

Insert lead pins into the PCB through-holes (usually about ϕ0.8mm). Soak leads in a wave solder tub.

Lead pins held by the through-holes enable handling of the package through the soldering process, and facilitate automated soldering. When soldering leads in the wave solder tub, do not get solder on the package.

4.2 Mounting Method of Surface Mount Type Package

Apply the specified quantity of solder paste to the pattern on any printed board by the screen printing method, to temporarily fix the package to the board. The solder paste melts when heated in a reflowing furnace, and package leads and the pattern of the printed board are fixed by the surface tension of the melted solder and self alignment.

The size of the pattern where leads are attached should be 1.1 to 1.3 times the leads' width, depending on paste material or furnace adjustment.

The temperature of the reflowing furnace is dependent on packaging material and type. Fig. 2 lists the adjustment of the reflowing furnace for FPP. Pre-heat the furnace to 150° C. Surface temperature of the resin should be kept at 235° C maximum for 10 minutes or less.

(1) The temperature of the leads should be kept at 260° for 10 minutes or less.
(2) The temperature of the resin should be kept at 235° for 10 minutes or less.
(3) Below is shown the temperature profile when soldering a package by the reflowing method.

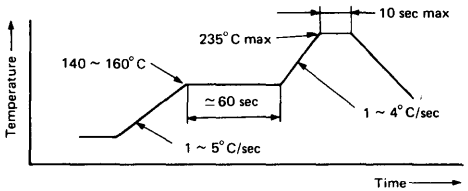


Fig. 2 Reflowing Furnace Adjustment for FPP

Employ adequate heating or temperature control equipment to prevent damage to the plastic package epoxy-resin material. When using an infrared heater, avoid long exposure at temperatures higher than the glass transition point of epoxy-resin (about 150° C), which may cause package damage and loss of reliability characteristics. Equalize the temperature inside and outside of packages by reducing the heat of the upper surface of the packages.

FPP leads may easily bend in shipment or during handling, and impact soldering onto the printed board. Heat the bent leads again with a soldering iron to reshape them.

Use a rosin flux when soldering. Do not use chloric flux because the chlorine in the flux has a tendency to remain on the leads and reduce reliability. Use alcohol, chlorothene or freon to wash away rosin flux from packages. These solvents should not remain on the packages for an excessive length of time, because the package markings may disappear.

QUALITY ASSURANCE

1. VIEWS ON QUALITY AND RELIABILITY

Basic views on quality at Hitachi are to meet the individual uers' required quality level and maintain a general quality level equal to or above that of the general market. The quality required by the user may be specified by contract, or may be indefinite. In either case, efforts are made to assure reliable performance in actual operating circumstances. Quality control during the manufacturing process, and quality awareness from design through production lead to product quality and customer satisfaction. Our quality assurance technique consists basically of the following steps:

(1) Build in reliability at the design stage of new product development.
(2) Build in quality at all steps in the manufacturing process.
(3) Execute stringent inspection and reliability confirmation of final products.
(4) Enhance quality levels through field data feed back.
(5) Cooperate with research laboratories for higher quality and reliability.

With the views and methods mentioned above, utmost efforts are made to meet users' requirements.

2. RELIABILITY DESIGN OF SEMICONDUCTOR DEVICES

2.1 Reliability Targets

The reliability target is an important factor in sales, manufacturing, performance, and price. It is not adequate to set a reliability target based on a single set of common test conditions. The reliability target is set based on many factors:

(1) End use of semiconductor device.
(2) End use of equipment in which device is used.
(3) Device manufacturing process.
(4) End user manufacturing techniques.
(5) Quality control and screening test methods.
(6) Reliability target of system.

2.2 Reliability Design

The following steps are taken to meet the reliability targets:

(1) Design Standardization
As for design rules, critical items pertaining to quality and reliability are always studied at circuit design, device design, layout design, etc. Therefore, as long as standardized processing and materials are used the reliability risk is extremely small even in the case of new development devices, with the exception of special requirements imposed by functional needs.

(2) Device Design
It is important for the device design to consider total balance of process, structure, circuit, and layout design, especially in the case where new processes and/or new materials are employed. Rigorous technical studies are conducted prior to device development.

(3) Reliability Evaluation by Functional Test
Functional Testing is a useful method for design and process reliability evaluation of IC's and LSI devices which have complicated functions.

The objectives of Functional Test are:

- Determining the fundamental failure mode.
- Analysis of relation between failure mode and manufacturing process.
- Analysis of failure mechanism.
- Establishment of QC points in manufacturing process.

2.3 Design Review

Design Review is an organized method to confirm that a design satisfies the performance required and meets design specifications. In addition, design review helps to insure quality and reliability of the finished products. At Hitachi, design review is performed from the planning stage to production for new products, and also for design changes on existing products. Items discussed and considered at design review are:

(1) Description of the products based on design documents.
(2) From the standpoint of each participant, design documents are studied, and for points needing clarification, further investigation will be carried out.
(3) Specify quality control and test methods based on design documents and drawings.
(4) Check process and ability of manufacturing line to achieve design goal.
(5) Preparation for production.
(6) Planning and execution of sub-programs for design changes proposed by individual specialists,

for test, experiments, and calculations to confirm the design changes.

(7) Analysis of past failures with similar devices, discussion of methods to prevent them, and planning and execution of test programs to confirm success.

3. QUALITY ASSURANCE SYSTEM

3.1 Activity of Quality Assurance

General views of overall quality assurance in Hitachi are as follows:

(1) Problems in each individual process should be solved in the process. Therefore, at the finished product stage the potential failure factors have been removed.

(2) Feedback of information is used to insure a satisfactory level of ability process.

3.2 Quality Approval

To insure quality and reliability, quality approval is carried out at the preproduction stage of device design, as described in section 2. Our views on quality approval are:

(1) A third party executes approval objectively from the standpoint of the customer.

(2) Full consideration is given to past failures and information from the field.

(3) No design change or process change without QA approval.

(4) Parts, materials, and processes are closely monitored.

(5) Control points are established in mass production after studying the process abilities and variables.

3.3 Quality and Reliability Control at Mass Production

Quality control is accomplished through division of functions in manufacturing, quality assurance, and other related departments. The total function flow is shown in Fig. 2. The main points are described below.

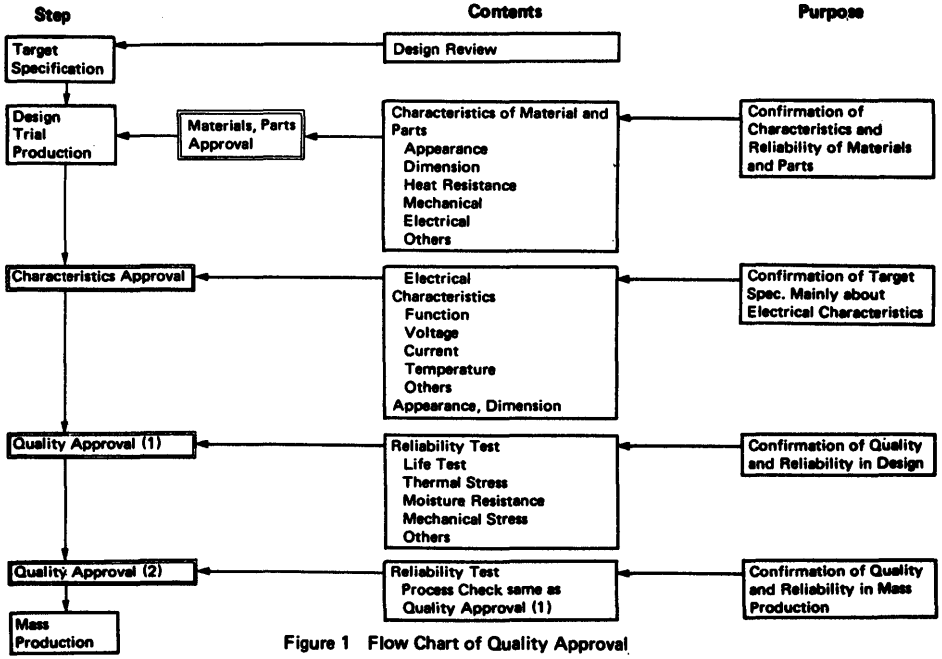


Figure 1 Flow Chart of Quality Approval

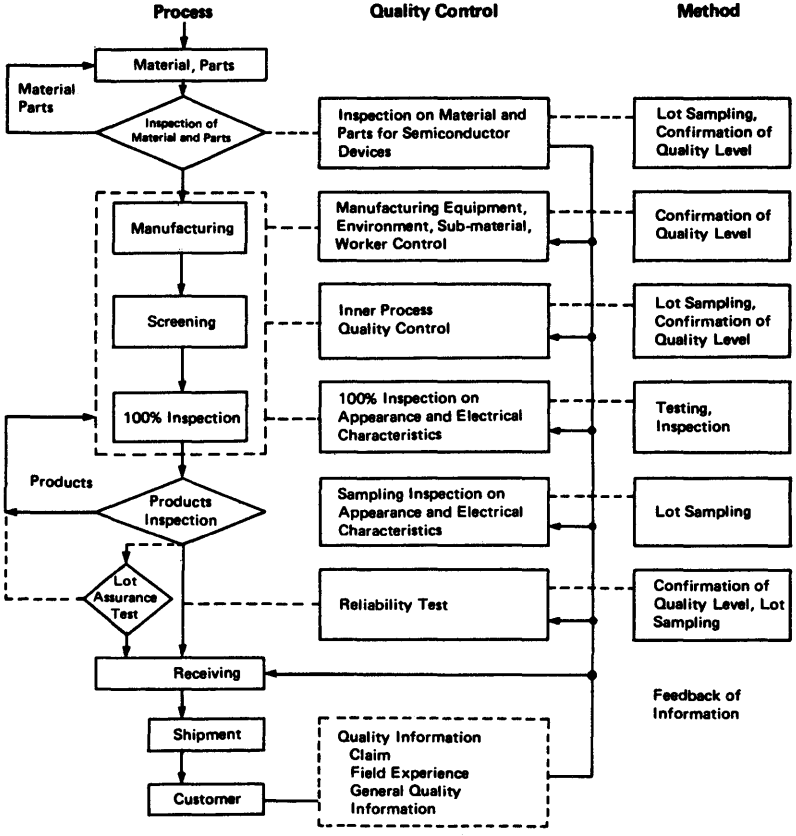


Figure 2 Flow Chart of Quality Control in Manufacturing Process

3.3.1 Quality Control of Parts and Materials

As semiconductor devices tend towards higher performance and higher reliability, the importance of quality control of parts and materials becomes paramount. Items such as crystals, lead frames, fine wire for wire bonding, packages, and materials needed in manufacturing processes such as masks and chemicals, are all subject to rigorous inspection and control. Incoming inspection is performed based on the purchase specification and drawing. The sampling is executed based mainly on MIL-STD-105D.

The other activities of quality assurance are as follows:

(1) Outside vendor technical information meeting.
(2) Approval and guidance of outside vendors.
(3) Chemical analysis and test.

The typical check points of parts and materials are shown in Table 1.

Table 1 Quality Control Check Points of Material and Parts (Example)

Material, Parts	Important Control Items	Point for Check
Wafer	Appearance	Damage and Contamination on Surface
	Dimension	Flatness
	Sheet Resistance	Resistance
	Defect Density	Defect Numbers
	Crystal Axis	
Mask	Appearance	Defect Numbers, Scratch
	Dimension	Dimension Level
	Resistoration	
	Gradation	Uniformity of Gradation
Fine Wire for Wire Bonding	Appearance	Contamination, Scratch, Bend, Twist
	Dimension	
	Purity	Purity Level
	Elongation Ratio	Mechanical Strength
Frame	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Processing Accuracy	
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
Ceramic Package	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Leak Resistance	Airtightness
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
	Electrical Characteristics	
	Mechanical Strength	Mechanical Strength
Plastic	Composition	Characteristics of Plastic Material
	Electrical Characteristics	
	Thermal Characteristics	
	Molding Performance	Molding Performance
	Mounting Characteristics	Mounting Characteristics

3.3.2 Inner Process Quality Control

Inner Process Quality Control performs very important functions in quality assurance of semiconductor devices. The manufacturing Inner Process Quality Control is shown in Fig. 3.

(1) Quality Control of Semi-final Products and Final Products

Potential failure factors of semiconductor devices are removed in the manufacturing process. To achieve this, check points are set-up in each process and products which have potential failure factors are not moved to the next process step. Manufacturing lines are rigidly selected and tight inner process quality controls are executed—rigid checks in each process and each lot, 100% inspection to remove failure factors caused by manufacturing variables and high temperature aging and temperature cycling. Elements of inner process quality control are as follows:

- Condition control of equipment and workers environment and random sampling of semi-final products.
- Suggestion system for improvement of work.
- Education of workers.
- Maintenance and improvement of yield.
- Determining quality problems, and implementing countermeasures.
- Transfer of quality information.

(2) Quality Control of Manufacturing Facilities and Measuring Equipment

Manufacturing equipment is improving as higher performance devices are needed. At Hitachi, the automation of manufacturing equipment is encouraged. Maintenance Systems maintain operation of high performance equipment. There are daily inspections which are performed based on related specifications. Inspection points are listed in the specification and are checked one by one to prevent any omission. As for adjustment and maintenance of measuring equipment, specifications are checked one by one to maintain and improve quality.

(3) Quality Control of Manufacturing Circumstances and Sub-Materials

The quality and reliability of semiconductor devices are highly affected by the manufacturing process. Therefore, controls of manufacturing circum-

stances such as temperature, humidity and dust, and the control of submaterials, like gas, and pure water used in a manufacturing process, are intensively executed.

Dust control is essential to realize higher integration and higher reliability of devices. At Hitachi, maintenance and improvement of cleanliness at manufacturing sites is accomplished through attention to buildings, facilities, air conditioning systems, delivered materials, clothes, work environment, and periodic inspection of floating dust concentration.

3.3.3 Final Product Inspection and Reliability Assurance

(1) Final Product Inspection

Lot inspection is done by the quality assurance

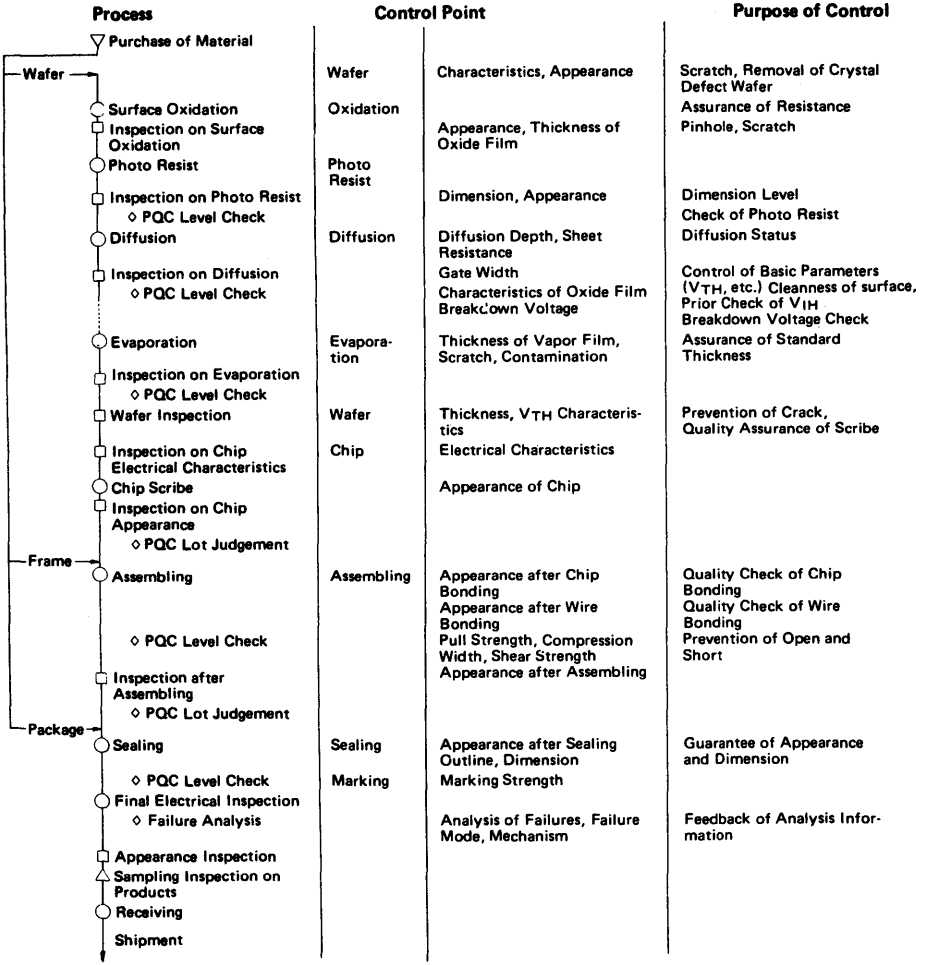


Figure 3 Example of Inner Process Quality Control

department for products which were judged good in 100% test . . . the final process in manufacturing. Though 100% yield is expected, sampling inspection is executed to prevent mixture of bad product by mistake. The inspection is executed not only to confirm that the products have met the users' requirements but also to consider potential quality factors. Lot inspection is executed based on MIL-STD-105D.

(2) Reliability Assurance Tests
To assure the reliability of semiconductor devices, reliability tests and tests on individual manufacturing lots that are required by the user, are periodically performed.

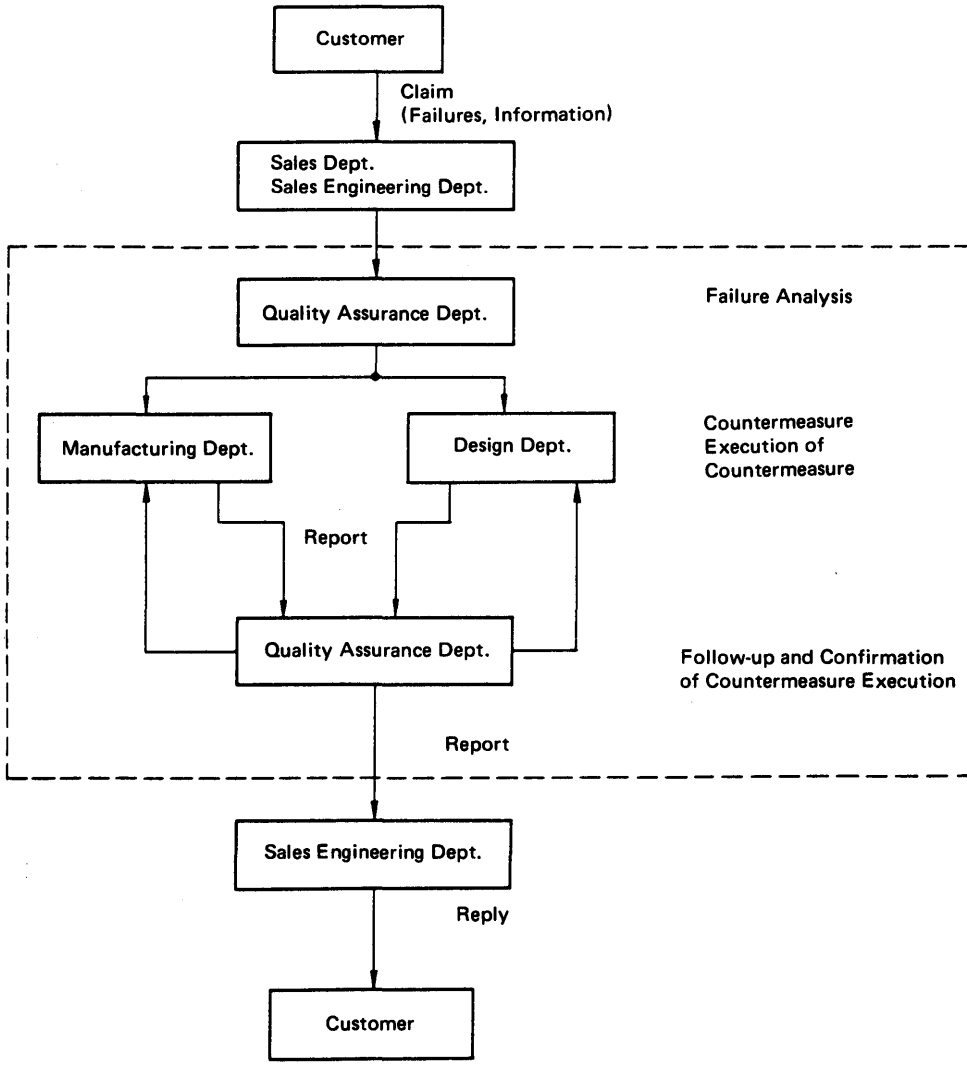


Figure 4 Process Flow Chart of Field Failure

RELIABILITY TEST DATA

1. INTRODUCTION

Microcomputers provide high reliability and quality to meet the demands of increased functions, enlarging scale, and widening application. Hitachi has improved the quality level of microcomputer products by evaluating reliability, building quality into the manufacturing process, strengthening inspection techniques, and analyzing field data.

The following reliability and quality assurance data for Hitachi 8-bit single-chip microcomputers indicates results from test and failure analysis.

2. PACKAGE AND CHIP STRUCTURE

2.1 Packaging

Production output and application of plastic packaging continues to increase, expanding to automobile measuring and control systems, and computer terminal equipment operating under severe conditions. To meet this demand, Hitachi has significantly improved moisture resistance and operational stability in the plastic manufacturing process.

Plastic and side-brazed ceramic package structures are shown in Figure 1 and Table 1.

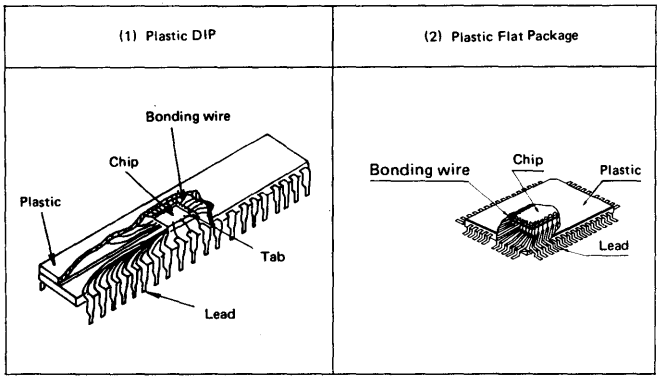


Figure 1 Package Structure

Table 1 Package Material and Properties

Item	Plastic DIP	Plastic Flat Package
Package	Epoxy	Epoxy
Lead	Solder dipping Alloy 42	Solder plating Alloy 42
Die bond	Au-Si or Ag paste	Au-Si or Ag paste
Wire bond	Thermo compression	Thermo compression
Wire	Au	Au

2.2 Chip Structure

The HMCS40 family is produced in low power CMOS technology. The Si-gate process is used because of high reliability and high density.

Chip structure and basic circuitry are shown in Figure 2.

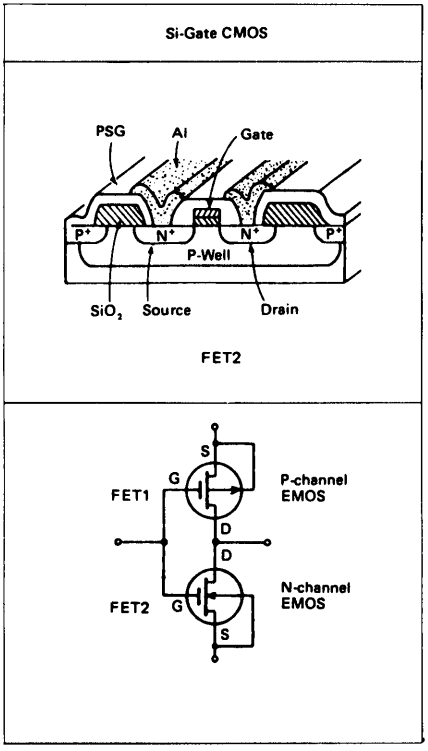


Figure 2 Chip Structure and Basic Circuit

3. QUALITY QUALIFICATION AND EVALUATION

3.1 Reliability Test Methods

Reliability test methods shown in Table 2 are used to qualify and evaluate the new products and new process.

Table 2 Reliability Test Methods

Test Items	Test Condition	MIL-STD-883B Method No.
Operating Life Test	125°C, 1000hr	1005,2
High Temp, Storage	Tstg max, 1000hr	1008,1
Low Temp, Storage	Tstg min, 1000hr	
Steady State Humidity	65°C 95%RH, 1000hr	
Steady State Humidity Biased	85°C 85%RH, 1000hr	
Temperature Cycling	-55°C ~ 150°C, 10 cycles	1010,4
Temperature Cycling	-20°C ~ 125°C, 200 cycles	
Thermal Shock	0°C ~ 100°C, 100 cycles	1011,3
Soldering Heat	260°C, 10 sec	
Mechanical Shock	1500G 0.5 msec, 3 times/X, Y, Z	2002,2
Vibration Fatigue	60Hz 20G, 32hrs/X, Y, Z	2005,1
Variable Frequency	20~2000Hz 20G, 4 min/X, Y, Z	2007,1
Constant Acceleration	20000G, 1 min/X, Y, Z	2001,2
Lead Integrity (DIP)	225gr, 90° 3 times	2004,3
Lead Integrity (FPP)	225gr, 90° 1 time	2004

3.2 Reliability Test Results

Reliability Test Results of 4-bit single-chip microcomputer devices is shown in Table 3 to Table 7.

Table 3 Dynamic Life Test

Device	Package	Sample Size	Component Hours	Failure
HMCS47C	DP-64S	90	90000	0
	FP-54	90	90000	0
HMCS46C	DP-42	90	90000	0
	DP-42S	45	45000	0
HMCS45C	DP-64S	45	45000	0
	FP-54	120	120000	1 *
HMCS44C	DP-42	162	162000	1 **
	DP-42S	45	45000	0
LCD-III	FP-80	90	90000	0

* Surface contamination
** Aluminum metallization open

Table 4 High Temperature, High Humidity Test (Moisture Resistance Test)

(1) 85°C 85%RH Bias Test

Package	168 hrs	500 hrs	1000 hrs
DIP-type	0/205	0/205	1*/205
FP-type	0/185	0/185	1*/185

*Aluminum corrosion

Condition; C MOS: V_{CC} = 5.5V

(2) High Temperature High Humidity Storage Life Test

a) 65°C/95%RH

Package	168 hrs	500 hrs	1000 hrs
DIP-type	0/870	0/870	1*/870
FP-type	0/545	0/545	1*/545

*Aluminum corrosion

(to be continued)

b) 85°C/95%RH

Package	168 hrs	500 hrs	1000 hrs
DIP-type	0/220	0/220	1*/220
FP-type	0/165	0/165	1*/165

*Aluminum corrosion

(3) Pressure Cooker Test

(121°C, 2 atm)

Package	40 hrs	60 hrs	100 hrs	200 hrs
DIP-type	0/55	0/55	0/55	0/55
FP-type	0/55	0/55	0/55	1*/55

*Current leakage

(4) MIL-STD-883B Moisture Resistance Test

(-65°C ~ -10°C, 90%RH or more)

Package	10 cycles	20 cycles	40 cycles
DIP-type	0/50	0/50	0/50
FP-type	0/22	0/22	0/22

Table 5 Temperature Cycling Test

(-55°C ~ 150°C)

Package	10 cycles	100 cycles	200 cycles
DIP-type	0/1637	0/1637	0/1637
FP-type	0/1514	0/1514	0/1514

Table 6 High Temperature, Low Temperature Storage Life Test

Package	Temperature	168 hrs	500 hrs	1000 hrs
DIP-type	150°C	0/43	0/43	0/43
	-55°C	0/50	0/50	0/50
FP-type	150°C	0/53	0/53	0/53
	-55°C	0/40	0/40	0/40

Table 7 Mechanical and Environmental Test

Test Item	Condition	Plastic DIP		Flat Plastic Package	
		Sample Size	Failure	Sample Size	Failure
Thermal Shock	0°C ~ 100°C 10 cycles	150	0	100	0
Soldering Heat	260°C, 10 sec.	140	0	160	0
Salt Water Spray	35°C, NaCl 5% 24 hrs	40	0	40	0
Solderability	230°C, 5 sec. Rosin flux	34	0	34	0
Drop Test	75cm, maple board 3 times	38	0	38	0
Mechanical Shock	1500G, 0.5ms 3 times/X, Y, Z	45	0	45	0
Vibration Fatigue	60 Hz, 20G 32hrs/X, Y, Z	120	0	45	0
Vibration Variable Freq.	100 ~ 2000Hz 20G, 4 times/X, Y, Z	45	0	45	0
Lead Integrity	225g, 90° Bonding 3 times	45	0	–	–
	225g, 90° Bonding 1 time	–	–	45	0

4. PRECAUTIONS

4.1 Storage

To prevent deterioration of electrical characteristics, solderability, appearance or structure, Hitachi recommends semiconductor devices be stored as follows:

(1) Store in ambient temperatures of 5 to 30° C, with a relative humidity of 40 to 60%.
(2) Store in a clean, dust- and active gas-free environment.
(3) Store in conductive containers to prevent static electricity.
(4) Store without any physical load.
(5) When storing devices for an extended period, store in an unfabricated form, to minimize corrosion of pre-formed lead wires.
(6) Unsealed chips should be stored in a cool, dry, dark and dust-free environment. Assembly should be performed within 5 days of unpacking. Devices can be stored for up to 20 days in dry nitrogen gas with a dew point at -30° C or less.
(7) Prevent condensation during storage due to rapid temperature changes.

4.2 Transportation

General precautions for electronic components are applicable in transporting semiconductors, units incorporating semiconductors, and other similar systems. In addition, Hitachi recommends the following:

(1) When transporting semiconductor devices or printed circuit boards, minimize mechanical vibration and shock. Use containers or jigs which will not induce static electricity as a result of vibration. Use of an electrically conductive container or aluminum foil is recommended.
(2) To prevent device deterioration from clothing-induced static electricity, workers should be properly grounded while handling devices. Use of a 1 M ohm resistor is recommended to prevent electric shock.
(3) When transporting printed curcuit boards containing semiconductor devices, suitable preventive measures against static electricity must be taken. Voltage build-up can be avoided by shorting the card-edge terminals. When a belt conveyor is used, apply some surface treatment to prevent build-up of electrical charge.
(4) Minimize mechanical vibration and shock when transporting semiconductor devices or printed circuit boards.

4.3 Handling for Measurement

Avoid static electricity, noise and voltage surge when measuring or mounting devices. Precaution should be taken against current leakage through terminals and housings of curve tracers, synchroscopes, pulse generators, and DC power sources.

When testing devices, prevent voltage surges from the tester, attached clamping circuit, and any excessive voltage possible through accidental contact.

In inspecting a printed circuit board, power should not be applied if any solder bridges or foreign matter is present.

4.4 Soldering

Semiconductor devices should not be exposed to high temperatures for excessive periods. Soldering must be performed consistent with temperature conditions of 260° C for 10 seconds, 350° C for 3 seconds, and at a distance of 1 to 1.5mm from the end of the device package.

A soldering iron with secondary voltage supplied through a grounded transformer is recommended to protect against leakage current. Use of alkali or acid flux, which may corrode the leads, is not recommended.

4.5 Removing Residual Flux

Detergent or ultrasonic removal of residual flux from circuit boards is necessary to ensure system reliability. Selection of detergent type and cleaning conditions are important factors.

When chloric detergent is used for plastic packaged devices, care must be taken against package corrosion. Extended cleaning periods and excessive temperature conditions can cause the chip coating to swell due to solvent permeation. Hitachi recommends use of Lotus and Dyfron solvents. Trichloroethylene solvent is not suitable.

The following conditions are advisable for ultrasonic cleaning:

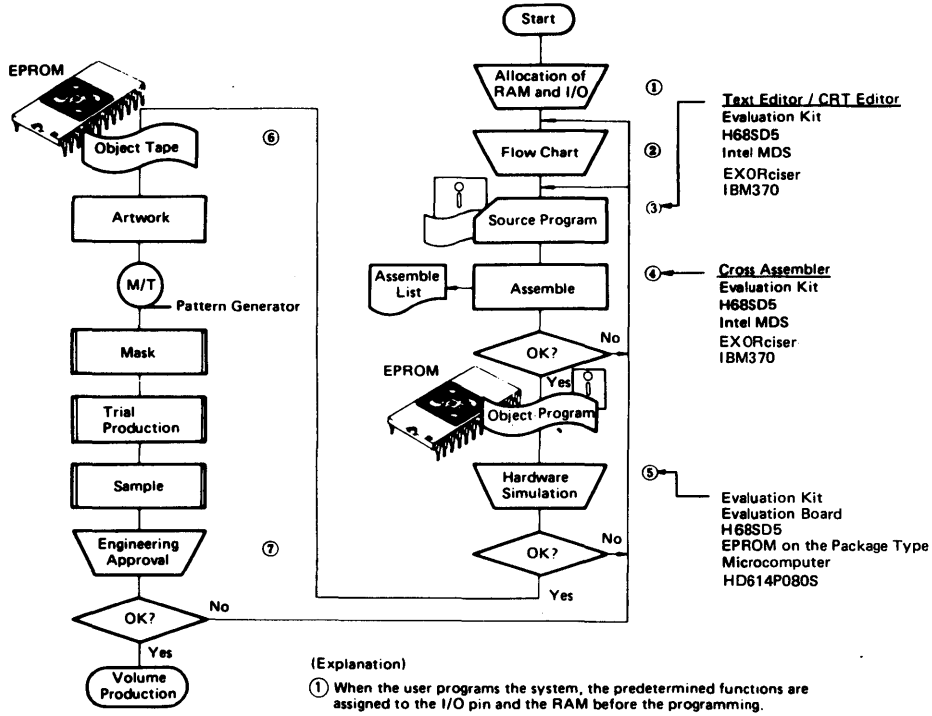
- Frequency: 28 to 29 k Hz (to avoid device resonation)
- Ultrasonic output: 15W/ℓ
- Keep devices from making direct contact with power generator
- Cleaning time: Less than 30 seconds.

DESIGN PROCEDURE AND SUPPORT TOOLS FOR 4-BIT SINGLE-CHIP MICROCOMPUTER

The cross assembler and the hardware simulator using various types of computer are prepared by Hitachi as supporting systems to develop user's programs.

User's programs are mask programmed into the ROM and delivered as the LSI by the company.

Fig. 1 shows the typical program design procedure and Table 1 shows the system development support tools for 4-bit single-chip microcomputer family used in these processes.



(Explanation)

① When the user programs the system, the predetermined functions are assigned to the I/O pin and the RAM before the programming.

② A flow chart is designed to achieve the predetermined functions and the flow chart is coded by using the mnemonic code.

③ The coded flow chart is punched into the card or the paper tape or written into the floppy disk, to generate a source program.

④ The source program is assembled by the evaluation kit or the H68SD5, to generate the object program. In this case, errors during the assembling are also detected.

⑤ Hardware simulation is performed to confirm the program. The company provides four kinds of hardware, the H68SD5, the evaluation kit, the evaluation board and the EPROM on the package type microcomputer. The consumers are able to choose the best suitable tool.

⑥ The completed program is sent to the company in the form of EPROM or the object tape.

⑦ Options such as ROM is masked by the company, LSI is testatively produced and the sample is handed in to the user. After the user has evaluated the sample and confirmed that the program is correct, mass production is started.

Figure 1 Program Design Procedure

Table 1 System Development Support Tools

Family No.	Resident System				Cross System			
	Evaluation Kit*2	Evaluation Board	EPROM on the Package	H68SD5 + Emulator set*3 (Hardware+Software)	IBM370	Intel MDS220/230 ISIS-II	Intel MDS220/230 CP/M	EXORciser-II
HMCS44C HMCS45C	H40EVKIT2	H45CEV00 H47CEV00	–	H68SD5+H40MIX1	S40XAM1-T	S40MDS1-F	–	S40EXR1-F
HMCS46C HMCS47C	H40EVKIT2	H47CEV00	–	H68SD5+H40MIX1	–	S40MDS1-F	–	S40EXR1-F
LCD-III	H40EVKIT4*1	H40LCEV00 H40LCEV04*1	–	H68SD5+H40MIX2 H68SD5+H40MIX4*1	S40XAM1-T	S40MDS1-F	–	S40EXR1-F
LCD-IV	H40EVKIT4*1	H40LCEV04*1	–	H68SD5+H40MIX4*1	–	S40MDS1-F	–	S40EXR1-F
HMCS404C	–	–	HD614P080S	H68SD5+H400CMIX1	–	S400MDS1F	S400MDS2F	–
HMCS404CL*1 HMCS404AC*1	–	–	*1	*1	–	S400MDS1-F	S400MDS2 F	–

*1 : Under Development
*2 : Cross Assembler is Supplied with Evaluation Kit.
*3 : Cross Assembler is Supplied with Emulator.
*4 : MDS is a registered trade mark of Mohorwk Data Science Corp.
ISIS-II is a registered trade mark of Intel Corp.
CP/M is a registered trade mark of Digital Research Inc.
EXORciser is a registered trade mark of Motorola Inc.

■ SINGLE-CHIP MICROCOMPUTER DEVELOPMENT SYSTEM

The H68SD5 is a development system for Hitachi 4-bit and 8-bit single-chip microcomputers.

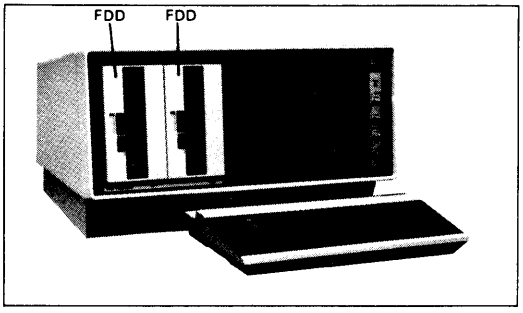
It is compact HD6800—based CRT/Key board microcomputer terminal, with two Floppy disk drivers, and has standard interface for the TTY (RS-232C or TTL level) and printer (Centronics parallel interface). An optional EPROM Writer is available.

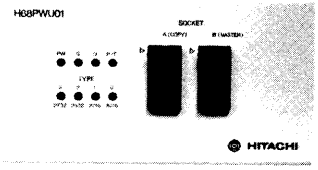
Features

- Supports system development for 8-bit and 4-bit single chip microcomputers
- **Disk based low cost system**
- **Provides the CRT Editor, Assembler, Emulator and EPROM Writer controlled by FDOS-III**
- **56k-byte RAM**
- **Allows linking between the H68SD5 and the I/O devices (TTY and Printer)**
- **Easy to debug user's prototype system using the Emulator Module**

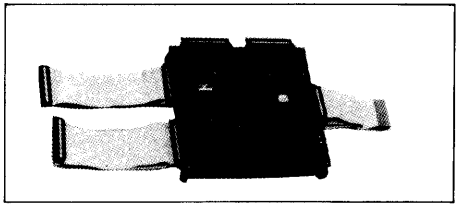
System Configuration

H68SD5





EPROM Writer



Emulator Module { 8-bit single-chip microcomputer family: HMCS40 series, HMCS400 series }

DATA SHEETS

4-BIT SINGLE-CHIP MICROCOMPUTER HMCS40 SERIES

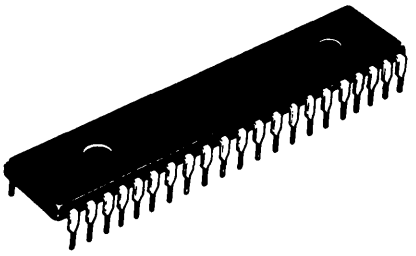
Preliminary data sheets herein contain information on new products. Specifications and information are subject to change without notice.

Advance Information data sheets herein contain information on a product under development. Hitachi reserves the right to change or discontinue these products without notice.

HMCS44C(HD44801)
HMCS44CL(HD44808)

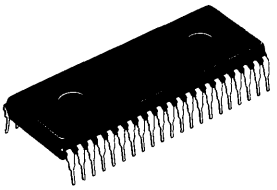
The HMCS44C is the CMOS 4-bit single chip microcomputer which contains ROM, RAM, I/O and Timer/Event Counter on single chip. The HMCS44C is designed to perform efficient controller function as well as arithmetic function for both binary and BCD data. The CMOS technology of the HMCS44C provides the flexibility of microcomputers for battery powered and battery back-up applications.

HMCS44C,HMCS44CL



(DP-42)

HMCS44C,HMCS44CL

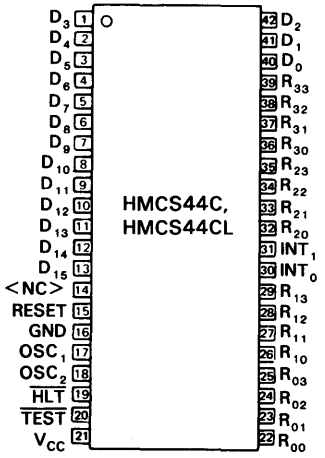


(DP-42S)

■ FEATURES

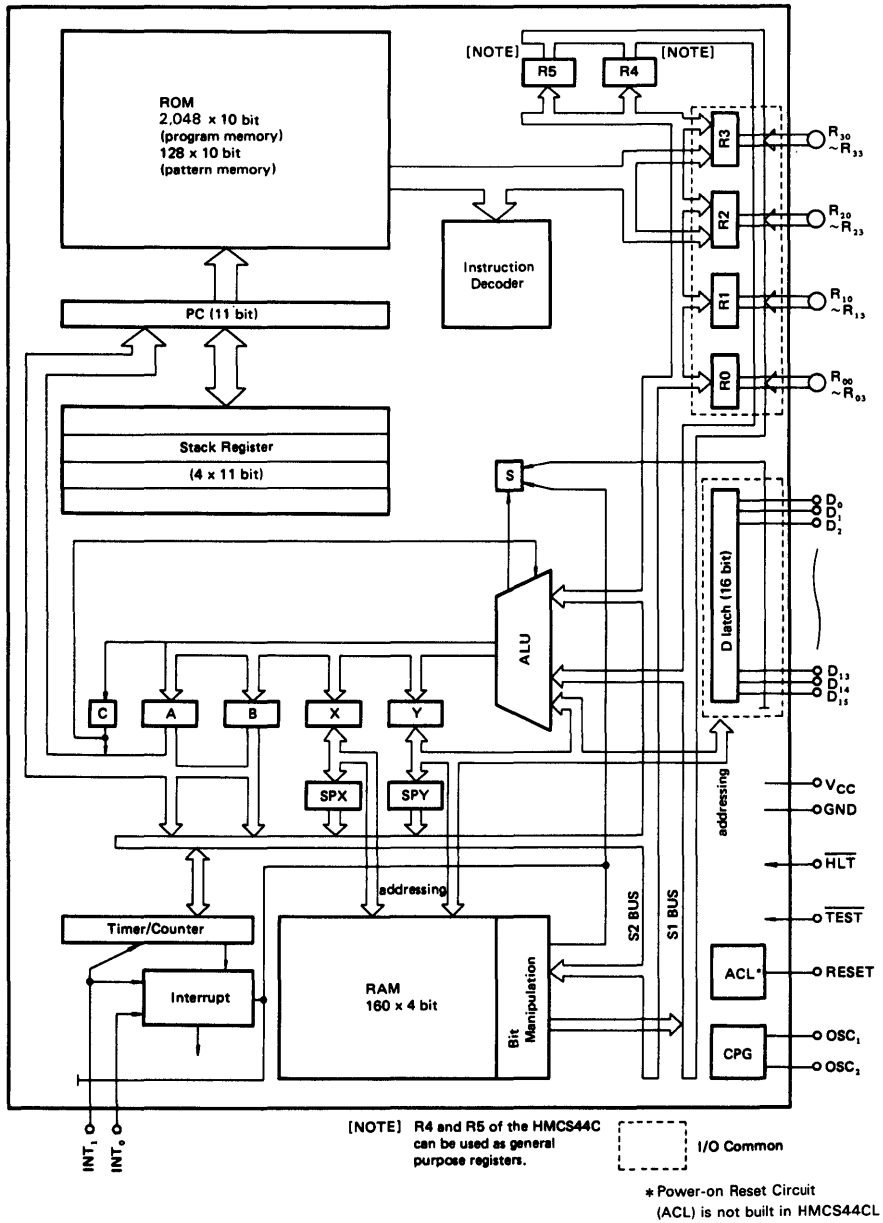
- 4-bit Architecture
- 2,048 Words of Program ROM (10 bits/Word)
  128 Words of Pattern ROM (10 bits/Word)
- 160 Digits of Data RAM (4 bits/Digit)
- 32 I/O Lines and 2 External Interrupt Lines
- Timer/Event Counter
- Instruction Cycle Time: HMCS44C; 10 μs
  HMCS44CL; 20 μs
- All Instructions except One Instruction; Single Word and Single Cycle
- BCD Arithmetic Instructions
- Pattern Generation Instruction
  – Table Look Up Capability –
- Powerful Interrupt Function
  3 Interrupt Sources
  ├ 2 External Interrupt Lines
  └ Timer/Event Counter
  Multiple Interrupt Capability
- Bit Manipulation Instructions for Both RAM and I/O
- Option of I/O Configuration Selectable on Each Pin; Pull Up MOS or CMOS or Open Drain
- Built-in Oscillator
- Built-in Power-on Reset Circuit (HMCS44C only)
- Low Operating Power Dissipation; 2mW typ.
- Stand-by Mode (Halt Mode); 50 μW max.
- CMOS Technology
- Single Power Supply: HMCS44C; 5V±10%
  HMCS44CL; 2.5V to 5.5V

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ HMCS44C ELECTRICAL CHARACTERISTICS (V_{CC}=5V ± 10%)

• ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Remarks
Supply Voltage	V_{CC}	−0.3 to +7.0	V	
Terminal Voltage (1)	V_{T1}	−0.3 to V_{CC}+0.3	V	Except for terminals specified by V_{T2}
Terminal Voltage (2)	V_{T2}	−0.3 to +10.0	V	Applied to only open drain output pins, open drain I/O common pins.
Maximum Total Output Current (1)	$-\Sigma I_{O1}$	45	mA	[NOTE 3]
Maximum Total Output Current (2)	ΣI_{O2}	45	mA	[NOTE 3]
Operating Temperature	T_{opr}	−20 to +75	℃	
Storage Temperature	T_{stg}	−55 to +125	℃	

[NOTE 1] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under the conditions of "ELECTRICAL CHARACTERISTICS-1, -2." If these conditions are exceeded, it could affect reliability of LSI.
[NOTE 2] All voltages are with respect to GND.
[NOTE 3] Maximum Total Output Current is total sum of output currents which can flow out (or flow in) simultaneously.

● **ELECTRICAL CHARACTERISTICS-1** (V_{CC}=5V±10%, Ta=−20℃ to +75℃)

Item	Symbol	Test Conditions	Value			Unit	Note
			min.	typ.	max.		
Input "Low" Voltage	V_{IL}		–	–	1.0	V	
Input "High" Voltage (1)	V_{IH1}		V_{CC}−1.0	–	V_{CC}	V	2
Input "High" Voltage (2)	V_{IH2}		V_{CC}−1.0	–	10	V	3
Output "Low" Voltage	V_{OL}	I_{OL}=1.6mA	–	–	0.8	V	
Output "High" Voltage (1)	V_{OH1}	$-I_{OH}$=1.0mA	2.4	–	–	V	4
Output "High" Voltage (2)	V_{OH2}	$-I_{OH}$=0.01mA	V_{CC}−0.3	–	–	V	5
Interrupt Input Hold Time	tINT		2·T_{inst}	–	–	μs	
Interrupt Input Fall Time	tfINT		–	–	50	μs	
Interrupt Input Rise Time	trINT		–	–	50	μs	
Output "High" Current	I_{OH}	V_{OH}=10V	–	–	3	μA	6
Input Leakage Current	I_{IL}	V_{in}=0 to V_{CC}	–	–	1.0	μA	2
		V_{in}=0 to 10V	–	–	3		3
Pull up MOS Current	$-I_P$	V_{CC}=5V	60	–	250	μA	
Supply Current (1)	I_{CC1}	V_{in}=V_{CC}, Ceramic Filter Oscillation	–	–	2	mA	7
Supply Current (2)	I_{CC2}	V_{in}=V_{CC}, R_f Oscillation, External Clock Operation	–	–	1.0	mA	7
Standby I/O Leakage Current	I_{LS}	$\overline{HLT}$=1.0V, V_{in}=0 to V_{CC}	–	–	1	μA	2, 8
		$\overline{HLT}$=1.0V, V_{in}=0 to 10V	–	–	3	μA	3, 8
Standby Supply Current	I_{CCS}	V_{in}=V_{CC}, $\overline{HLT}$=0.2V		–	10	μA	9
External Clock Operation							
External Clock Frequency	f_{CP}		200	400	440	kHz	
External Clock Duty	Duty		45	50	55	%	
External Clock Rise Time	t_{rCP}		0	–	0.2	μs	
External Clock Fall Time	t_{fCP}		0	–	0.2	μs	
Instruction Cycle Time	T_{inst}	T_{inst}=4/f_{CP}	9.1	10	20	μs	
Internal Clock Operation (R_f Oscillation)							
Clock Oscillation Frequency	f_{OSC}	R_f=91kΩ±2%	300	–	500	kHz	
Instruction Cycle Time	T_{inst}	T_{inst}=4/f_{OSC}	8.0	–	13.3	μs	
Internal Clock Operation (Ceramic Filter Oscillation)							
Clock Oscillation Frequency	f_{OSC}	Ceramic Filter Circuit	392	–	408	kHz	
Instruction Cycle Time	T_{inst}	T_{inst}=4/f_{OSC}	9.8	–	10.2	μs	

[NOTE 1] All voltages are with respect to GND.
[NOTE 2] This is applied to RESET, $\overline{HLT}$, OSC_1, INT_0, INT_1 and the With Pull up MOS or CMOS type of I/O pins.
[NOTE 3] This is applied to the Open Drain type of I/O pins.
[NOTE 4] This is applied to the CMOS type of I/O or Output pins.
[NOTE 5] This is applied to the With Pull up MOS or CMOS type of I/O or Output pins.
[NOTE 6] This is applied to the Open Drain type of I/O or Output pins.
[NOTE 7] I/O current is excluded.
[NOTE 8] The Standby I/O Leakage Current is the I/O leakage current in the Halt and Disable State.
[NOTE 9] I/O current is excluded.
The Standby Supply Current is the supply current at V_{CC}=5V±10% in the Halt State. The supply current in the case where the supply voltage falls to the Halt Duration Voltage is called the Halt Current (I_{DH}), and it is shown in "ELECTRICAL CHARACTERISTICS-2."

● **ELECTRICAL CHARACTERISTICS-2** (Ta=−20 to +75℃)

Reset and Halt

Item	Symbol	Test Conditions	Value min.	Value max.	Unit
Halt Duration Voltage	V_{DH}	$\overline{HLT}$=0.2V	2.3	–	V
Halt Current	I_{DH}	$V_{in}=V_{CC}$ $\overline{HLT}$=0.2V, V_{DH}=2.3V	–	10	μA
Halt Delay Time	tHD		100	–	μs
Operation Recovery Time	tRC		100	–	μs
$\overline{HLT}$ Fall Time	tfHLT		–	1000	μs
$\overline{HLT}$ Rise Time	trHLT		–	1000	μs
$\overline{HLT}$ "Low" Hold Time	tHLT		400	–	μs
$\overline{HLT}$ "High" Hold Time	tOPR	R_f Oscillation, External Clock Operation	0.1	–	ms
		Ceramic Filter Oscillation	4	–	
Power Supply Rise Time	trCC	Built-in Reset, $\overline{HLT}=V_{CC}$	0.1	10	ms
Power Supply OFF Time	tOFF	Built-in Reset, $\overline{HLT}=V_{CC}$	1	–	ms
RESET Pulse Width (1)	tRST1	External Reset, V_{CC}=4.5 to 5.5V, $\overline{HLT}=V_{CC}$ (R_f Oscillation, External Clock Operation)	1	–	ms
		External Reset V_{CC}=4.5 to 5.5V, $\overline{HLT}=V_{CC}$ (Ceramic Filter Oscillation)	4	–	
RESET Pulse Width (2)	tRST2	External Reset V_{CC}=4.5 to 5.5V, $\overline{HLT}=V_{CC}$	2 · T_{inst}	–	μs
RESET Rise Time	trRST	External Reset V_{CC}=4.5 to 5.5V, $\overline{HLT}=V_{CC}$	–	20	ms
RESET Fall Time	tfRST	External Reset V_{CC}=4.5 to 5.5V, $\overline{HLT}=V_{CC}$	–	20	ms

[NOTE] All voltages are with respect to GND.

■ **HMCS44CL ELECTRICAL CHARACTERISTICS** (V_{CC}=2.5 to 5.5V)

● **ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Value	Unit	Remarks
Supply Voltage	V_{CC}	−0.3 to +7.0	V	
Terminal Voltage (1)	V_{T1}	−0.3 to V_{CC}+0.3	V	Except for terminals specified by V_{T2}
Terminal Voltage (2)	V_{T2}	−0.3 to +10.0	V	Applied to only open-drain output pins and open-drain I/O common pins.
Maximum Total Output Current (1)	$-\Sigma I_{O1}$	45	mA	(Note 3)
Maximum Total Output Current (2)	ΣI_{O2}	45	mA	(Note 3)
Operating Temperature	T_{opr}	−20 to +75	℃	
Storage Temperature	T_{stg}	−55 to +125	℃	

[NOTE 1] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under the conditions of "ELECTRICAL CHARACTERISTICS-1, -2." If these conditions are exceeded, it could affect reliability of LSI.

[NOTE 2] All voltages are with respect to GND.

[NOTE 3] Maximum Total Output Current is total sum of output currents which can flow out (or flow in) simultaneously.

● **ELECTRICAL CHARACTERISTICS-1** (V_{CC}=2.5 to 5.5V, Ta=−20 to +75℃)

Item	Symbol	Test Conditions	Value min.	Value typ.	Value max.	Unit	Note
Input "Low" Voltage	V_{IL}		—	—	0.15·V_{CC}	V	
Input "High" Voltage (1)	V_{IH1}		0.85·V_{CC}	—	V_{CC}	V	2
Input "High" Voltage (2)	V_{IH2}		0.85·V_{CC}	—	10	V	3
Output "Low" Voltage	V_{OL}	I_{OL}=0.4mA	—	—	0.4	V	
Output "High" Voltage	V_{OH}	−I_{OH}=0.08mA	V_{CC}−0.4	—	—	V	4
Interrupt Input Hold Time	tINT		2·Tinst	—	—	μs	
Interrupt Input Fall Time	tfINT		—	—	50	μs	
Interrupt Input Rise Time	trINT		—	—	50	μs	
Output "High" Current	I_{OH}	V_{OH}=10V	—	—	3	μA	5
Input Leakage Current	I_{IL}	V_{in}=0 to V_{CC}	—	—	1.0	μA	2
		V_{in}=0 to 10V	—	—	3		3
Pull-up MOS Current	−I_P	V_{CC}=3V	10	—	80	μA	
Supply Current	I_{CC}	V_{in}=V_{CC}, V_{CC}=3V (f_{OSC}/f_{CP}=200kHz) R_f Oscillation, External Clock Operation	—	—	140	μA	6
Standby I/O Leakage Current	I_{LS}	$\overline{HLT}$=0.5V, V_{in}=0 to V_{CC}	—	—	1	μA	2, 7
		$\overline{HLT}$=0.5V, V_{in}=0 to 10V	—	—	3	μA	3, 7
Standby Supply Current	I_{CCS}	V_{in}=V_{CC}, V_{CC}=2.5 to 3.5V	—	—	6	μA	8
		$\overline{HLT}$=0.1V, V_{CC}=2.5 to 5.5V	—	—	10	μA	
External Clock Operation							
External Clock Frequency	f_{CP}		130	200	240	kHz	
External Clock Duty	Duty		45	50	55	%	
External Clock Rise Time	trcp		0	—	0.2	μs	
External Clock Fall Time	tfcp		0	—	0.2	μs	
Instruction Cycle Time	T_{inst}	T_{inst}=4/f_{CP}	16.8	20	30.8	μs	
Internal Clock Operation (R_f Oscillation)							
Clock Oscillation Frequency	f_{OSC}	R_f=180kΩ±2% V_{CC}=2.5 to 3.5V	130	—	250	kHz	
		R_f=180kΩ±2% V_{CC}=2.5 to 5.5V	130	—	350		
Instruction Cycle Time	T_{inst}	T_{inst}=4/f_{OSC}, V_{CC}=2.5 to 3.5V	16	—	30.8	μs	
		T_{inst}=4/f_{OSC}, V_{CC}=2.5 to 5.5V	11.4	—	30.8		

[NOTE 1] All voltages are with respect to GND.
[NOTE 2] This is applied to RESET, $\overline{HLT}$, OSC_1, INT_0, INT_1 and the With Pull up MOS or CMOS type of I/O pins.
[NOTE 3] This is applied to the Open Drain type of I/O pins.
[NOTE 4] This is applied to the CMOS type of I/O or Output pins.
[NOTE 5] This is applied to the Open Drain type of I/O or Output pins.
[NOTE 6] I/O current is excluded.
[NOTE 7] The Standby I/O Leakage Current is the I/O leakage current in the Halt and Disable State.
[NOTE 8] I/O current is excluded.
The Standby Supply Current is the supply current at V_{CC}=2.5V to 5.5V in the Halt State. The supply current in the case where the supply voltage falls to the Halt Duration Voltage is called the Halt Current (I_{DH}), and it is shown in "ELECTRICAL CHARACTERISTICS-2."

●**ELECTRICAL CHARACTERISTICS-2** (Ta = −20 to +75°C)

Reset and Halt

Item	Symbol	Test Conditions	Value		Unit
			min.	max.	
Halt Duration Voltage	V_{DH}	$\overline{HLT}$=0.2V	2.0	—	V
Halt Current	I_{DH}	$V_{in}=V_{CC}$, $\overline{HLT}$=0.1V V_{DH}=2.0V	—	10	μA
Halt Delay Time	t_{HD}		200	—	μs
Operation Recovery Time	t_{RC}		200	—	μs
$\overline{HLT}$ Fall Time	t_{fHLT}		—	1000	μs
$\overline{HLT}$ Rise Time	t_{rHLT}		—	1000	μs
$\overline{HLT}$ "Low" Hold Time	t_{HLT}		800	—	μs
$\overline{HLT}$ "High" Hold Time	t_{OPR}	R_f Oscillation, External Clock Operation V_{CC}=2.5 to 5.5V	0.2	—	ms
RESET Pulse Width (1)	t_{RST1}	External Reset, V_{CC}=2.5 to 5.5V, $\overline{HLT}=V_{CC}$ (R_f Oscillation, External Clock Operation)	2	—	ms
RESET Pulse Width (2)	t_{RST2}	External Reset, V_{CC}=2.5 to 5.5V $\overline{HLT}=V_{CC}$	2 · T_{inst}	—	μs
RESET Fall Time	t_{fRST}	$\overline{HLT}=V_{CC}$	—	20	ms
RESET Rise Time	t_{rRST}	$\overline{HLT}=V_{CC}$	—	20	ms

[NOTE] All voltages are with respect to GND.

■ SIGNAL DESCRIPTION

The input and output signals for the HMCS44C, shown in PIN ARRANGEMENT, are described in the following paragraphs.

• V_{CC} and GND

Power is supplied to the HMCS44C using these two pins. V_{CC} is power and GND is the ground connection.

• RESET

This pin allows resetting of the HMCS44C at times other than the automatic resetting capability (ACL; Built-in Reset Circuit) already in the HMCS44C.

The HMCS44C can be reset by pulling RESET high. Refer to RESET FUNCTION for additional information.

• OSC_1 and OSC_2

These pins provide control input for the built-in oscillator circuit. Resistor and capacitor, ceramic filter circuit, or an external oscillator can be connected to these pins to provide a system clock with various degrees of stability/cost tradeoffs.

Lead length and stray capacitance on these two pins should be minimized. Refer to OSCILLATOR for recommendations about these pins.

• $\overline{HLT}$

This pin is used to place the HMCS44C in the Halt State. Refer to HALT FUNCTION for details of the Halt Mode.

• $\overline{TEST}$

This pin is not for user application and must be connected to V_{CC}.

• INT_0 and INT_1

These pins provide the capability for asynchronously applying external interrupts to the HMCS44C.

Refer to INTERRUPTS for additional information.

• R_{00} to R_{03}, R_{10} to R_{13}, R_{20} to R_{23}, R_{30} to R_{33}

These 16 lines are arranged into four 4-bit Data Input/Output Common Channels.

The 4-bit registers (Data I/O Register) are attached to these channels. Each channel is directly addressed by the operand of input/output instruction. Refer to INPUT/OUTPUT for additional information.

• D_0 to D_{15}

These lines are 16 1-bit Discrete Input/Output Common Pins. The 1-bit latches are attached to these pins. Each pin is addressed by the Y register. The D_0 to D_3 pins are also addressed directly by the operand of input/output instruction. Refer to INPUT/OUTPUT for additional information.

■ ROM

• ROM Address Space

ROM is used as a memory for the instructions and the patterns (constants). The instruction used in the HMCS44C consists of 10 bits. These 10 bits are called "a word", which is a unit for writing into ROM.

The ROM address is composed of the program area (0 page to 31 page) and the pattern area (61, 62 page) (64 words/page).

The ROM capacity is 2,176 words (1 word = 10 bits) in all.

Only the program area can contain both the instructions and the patterns (constants).

The ROM address space is shown in Figure 1.

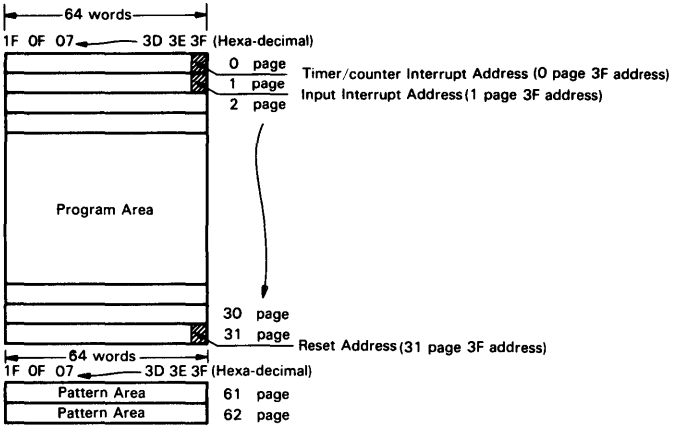


Figure 1 ROM Address Space

- **Program Counter (PC)**

The program counter is used for addressing of ROM. It consists of the page part and the address part as shown in Figure 2.

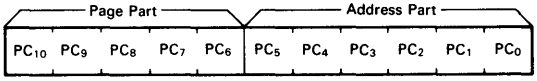


Figure 2 Configuration of Program Counter

Once a certain value is loaded into a page part, the content is unchanged until other value is loaded by the program. The settable value of a page part is any number between 0 to 31.

The address part is a 6-bit polynomial counter and counts up for each instruction cycle time. The sequence in the decimal and hexa-decimal system is shown in Table 1. This sequence is circulating and has neither the starting nor ending point. It doesn't generate an overflow carry. Consequently, the program on a same page is executed in order unless the value of the page part is changed.

Table 1 Program Counter Address Part Sequence

Decimal	Hexadecimal	Decimal	Hexadecimal	Decimal	Hexadecimal
63	3F	5	05	9	09
62	3E	11	0B	19	13
61	3D	23	17	38	26
59	3B	46	2E	12	0C
55	37	28	1C	25	19
47	2F	56	38	50	32
30	1E	49	31	37	25
60	3C	35	23	10	0A
57	39	6	06	21	15
51	33	13	0D	42	2A
39	27	27	1B	20	14
14	0E	54	36	40	28
29	1D	45	2D	16	10
58	3A	26	1A	32	20
53	35	52	34	0	00
43	2B	41	29	1	01
22	16	18	12	3	03
44	2C	36	24	7	07
24	18	8	08	15	0F
48	30	17	11	31	1F
33	21	34	22		
2	02	4	04		

- **Designation of ROM Address and ROM Code**

The page part of the ROM address is represented by decimal and the address part is divided into 2 parts (2 bits and 4 bits) and represented by hexa-decimal.

One word (10 bits) is divided into three parts (2 bits, 4 bits and 4 bits from the most significant bit O_{10}) and represented by hexadecimal. The examples are shown in Figure 3.

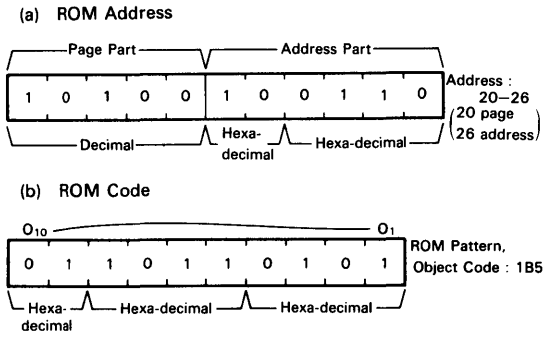


Figure 3 Designation of ROM Address and ROM Code

■ PATTERN GENERATION

The pattern (constants) can be accessed by the pattern instruction (P). The pattern can be written in any address of the ROM address space.

- **Reference**

ROM addressing for reference of the patterns is achieved by modifying the program counter with the accumulator, the B register, the Carry F/F and the operand p. Figure 4 shows how to modify the program counter. The address part is replaced with the accumulator and the lower 2 bits of B register, while the page part is ORed with the upper 2 bits of B register, the Carry F/F and the operand p (p_0, p_1). The upper bit (p_2) of the operand is for referring to the pattern area.

The value of the operand p is 0 to 7.

The content of the program counter is only modified apparently and is not changed. Then the address is counted up after the execution of the pattern instruction and the next instruction is executed.

The execution time of this instruction is 2-cycle time.

Even when interrupt is enable, interrupt is disabled in the second cycle of the pattern instruction. However, the interrupt request is latched into the interrupt request F/F.

- **Generation**

The pattern of referred ROM address is generated as the following two ways:

(i) The pattern is loaded into the accumulator and B register.

(ii)The pattern is loaded into the Data I/O registers R2 and R3.

Selection is determined by the command bits (O_9, O_{10}) in the pattern.

Mode (i) is performed when O_9 is "1" and mode (ii) is performed when O_{10} is "1".

Mode (i) and mode (ii) are simultaneously performed when both O_9 and O_{10} are "1".

The correspondence of each bit of the pattern is shown in Figure 5.

Examples of the pattern instruction usage is shown in Table 2.

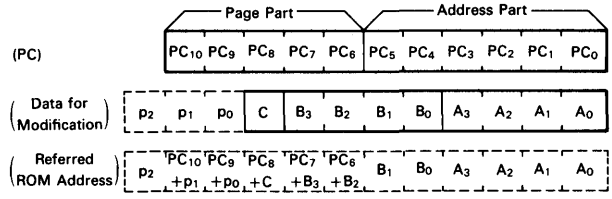


Figure 4 ROM Addressing for Pattern Generation

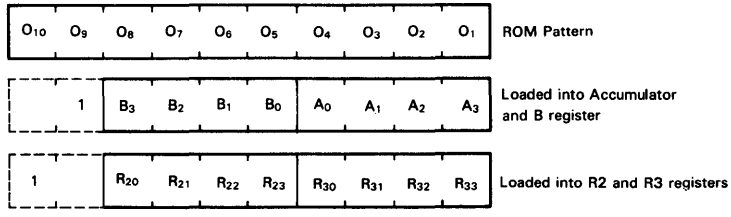


Figure 5 Correspondence of Each Bit of Pattern

Table 2 Example of Pattern Instruction Usage

Before Execution					Referred ROM Address	Pattern	After Execution			
PC Value	p	C	B	A			B	A	R2	R3
0-3F	1	0	A	0	10-20	12D	2	B		
0-3F	7	1	4	0	61-00	22D			4	B
30-00	4	0/1	0	9	62-09	32D	2	B	4	B
30-00	4	0/1	F	9	63-39					

"—" means that the value is unchanged after the execution.
"0/1" means that either "0" or "1" will do.

■ BRANCH

ROM is accessed according to the program counter sequence and the program is executed. In order to jump to any address out of the sequence, there are four ways.

They are explained in the following paragraphs.

• BR

By BR instruction, the program branches to an address in the current page.

The lower 6 bits of ROM Object Code (operand a, O_6 to O_1) are transferred to the lower 6 bits of the program counter. This instruction is a conditional instruction and executed only when the Status F/F is "1". If it is "0", the instruction is skipped and the Status F/F becomes "1". The operation is shown in Figure 6.

• LPU

By LPU instruction, the jump of page is performed.

The lower 5 bits of the ROM Object Code (operand u) are transferred to the page part of the program counter with a delay of 1 instruction cycle time. Therefore, the cycle just after the issuing of this instruction is on the same page and the page jump is performed at the next cycle.

This instruction is a conditional instruction and performed only when the Status is "1". But the Status is unchanged (remains "0") even if it is skipped. The operation is shown in Figure 7.

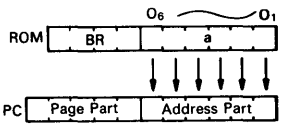


Figure 6 BR Operation

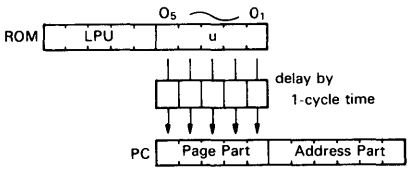


Figure 7 LPU Operation

• BRL

By BRL instruction, the program branches to an address in any page.

This instruction is a macro instruction of LPU and BR instructions, which is divided into two instructions as follows.

BRL a – b → LPU a
<Jump to b address on a page> BR b

BRL instruction is a conditional instruction because of characteristics of LPU and BR instructions, and is executed only when the Status F/F is "1". If the Status F/F is "0", the instruction is skipped and the Status F/F becomes "1".

• TBR (Table Branch)

By TBR instruction, the program branches by the table.

The program counter is modified with the accumulator, the B register, the Carry F/F, the operand p. The method for modification is shown in Figure 8.

The accumulator and the lower 2 bits of B register are assigned into the address part of the program counter. The upper 2 bits of B register, Carry F/F, and the operand p_1, p_0 are ORed with the page part of the program counter.

TBR instruction is executed regardless of the Status F/F, and does not affect the Status F/F.

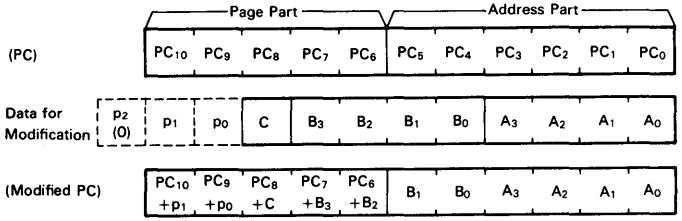


Figure 8 Modification of Program Counter by TBR Instruction

■ SUBROUTINE JUMP

There are two types of subroutine jumps. They are explained in the following paragraphs.

• CAL

By CAL instruction, subroutine jump to an address in the Subroutine Page.

The Subroutine Page is 0 page.

The address next to CAL instruction address is pushed onto the stack ST1 and the contents of the stacks ST1, ST2 and ST3 are pushed onto the stacks ST2, ST3 and ST4 respectively as shown in Figure 9.

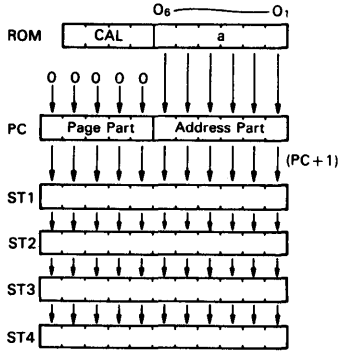


Figure 9 Subroutine Jump Stacking Order

The page part of the program counter is 0. The lower 6 bits (operand a, O_6 to O_1) of the ROM Object Code is transferred to the address part of the program counter.

The HMCS44C has 4 levels of stack (ST1, ST2, ST3 and ST4) which allows the programmer to use up to 4 levels of subroutine jumps (including interrupts).

CAL is a conditional instruction and executed only when the Status F/F is "1". If the Status F/F is "0", it is skipped and the Status F/F changes to "1".

• CALL

By CALL instruction, subroutine jump to an address in any page.

Subroutine jump to any address can be implemented by the subroutine jump to the page specified by LPU instruction.

This instruction is a macro instruction of LPU and CAL instructions, which is divided into two instructions as follows.

```
                                CALL  a, b → LPU  a
<Subroutine jump to b address on a page>      CAL  b
```

CALL instruction is conditional because of characteristics of LPU and CAL instructions and is executed when the Status F/F is "1". If the Status F/F is "0", it is skipped and the Status F/F changes to "1".

■ RAM

RAM is a memory used for storing data and saving the contents of the registers. Its capacity is 160 digits (640 bits) where one digit consists of 4 bits.

Addressing of RAM is performed by a matrix of the file No. and the digit No.

The file No. is set in the X register and the digit No. in the Y register for reading, writing or testing. Specific digits in RAM can be addressed not via the X register and Y register. These digits are called "Memory Register (MR)", 0 to 15 (16 digits in all). The memory register can be exchanged with the accumulator by XAMR instruction.

The RAM address space is shown in Figure 10.

In an instruction in which reading from RAM and writing to RAM coexist (exchange between RAM and the register), reading precedes writing and the write data does not affect the read data.

The RAM bit manipulation instruction enables any addressed RAM bit to be set, reset or tested. The bit assignment is specified by the operand n of the instruction.

The bit test makes the Status F/F "1" and makes it "0" when the assigned bit is "0".

Correspondence between the RAM bit and the operand n is shown in Figure 11.

X \ f \ d	Y 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 ← digit No.
0	0															
1	1															
2	2															
3	3															
4	4															
5	5															
6	6															
7	7															
8~11*	8															
12~15*	9	MR15	MR14	MR13	MR12	MR11	MR10	MR9	MR8	MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0

↑ file No.

*The file 8 is selected when X register has any value in 8 to 11, and the file 9 is selected when 12 to 15.

Figure 10 RAM Address Space

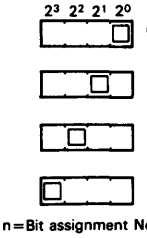


Figure 11 RAM Bit and Operand n

■ REGISTER

The HMCS44C has six 4-bit registers and two 1-bit registers available to the programmer. The 1-bit registers are the Carry F/F and the Status F/F. They are explained in the following paragraphs.

• Status F/F (S)

The Status F/F latches the result of logical or arithmetic operations (Not Zero, Overflow) and bit test operations. The Status F/F affects conditional instructions (LPU, BR and CAL instructions). These instructions are executed only when the Status F/F is "1". If it is "0", these instructions are skipped and the Status F/F becomes "1".

- **Accumulator (A; A Register) and Carry F/F (C)**

The result of the Arithmetic Logic Unit (ALU) operation (4 bits) and the overflow of the ALU are loaded into the accumulator and the Carry F/F. The Carry F/F can be set, reset or tested. Combination of the accumulator and the Carry F/F can be right or left rotated. The accumulator is the main register for ALU operation and the Carry F/F is used to store the overflow generated by ALU operation when the calculation of two or more digits (4 bits/digit) is performed.

- **B Register (B)**

The result of ALU operation (4 bits) is loaded into this register. The B register is used as a sub-accumulator to stack data temporarily and also used as a counter.

- **X Register (X)**

The result of ALU operation (4 bits) is loaded into this register. The X register has exchangeability for the SPX register. The X register addresses the RAM file and is composed of 4-bit register.

- **SPX Register (SPX)**

The SPX register has exchangeability for the X register.

The SPX register is used to stack the X register and expand the addressing system of RAM in combination with the X register. It is composed of 4-bit register.

- **Y Register (Y)**

The result of ALU operation (4 bits) is loaded into this register. The Y register has exchangeability for the SPY register. The Y register can calculate itself simultaneously with transferring data by the bus lines, which is usable for the calculation of two or more digits (4 bits/digit). The Y register addresses the RAM digit and 1-bit Discrete I/O.

- **SPY Register (SPY)**

The SPY register has exchangeability for the Y register. The SPY register is used to stack the Y register and expand the addressing system of RAM and 1-bit Discrete I/O in combination with the Y register.

■ INPUT/OUTPUT

- **4-bit Data Input/Output Channel (R)**

The HMCS44C has four 4-bit Data I/O Common Channels (R0, R1, R2, R3).

The 4-bit registers (Data I/O Register) are attached to R1, R2 and R3 channels.

Each channel is directly addressed by the operand p of input/output instruction.

The data is transferred from the accumulator and the B register to the Data I/O Registers R0 to R3 via the bus lines. Pattern instruction enables the patterns of ROM to be taken into the Data I/O Registers R2 and R3.

Input instruction enables the 4-bit data to be sent to the accumulator and the B register from R0 to R3. Note that, since the Data I/O Register output is directly connected to the pin even during execution of input instruction, the input data is wired logic of the Data I/O Register output and the pin input.

Therefore, the Data I/O Register should be set to 15 (all bits of the Data I/O Register is "1") not to affect the pin input before execution of input instruction.

The block diagram is shown in Figure 12. The I/O timing is shown in Figure 13.

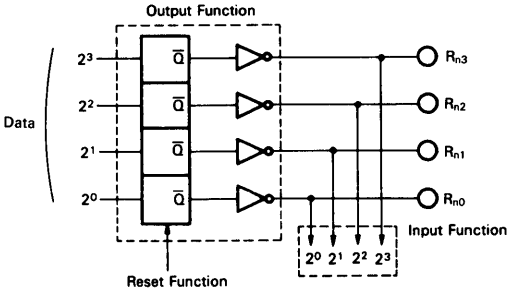


Figure 12 4-bit Data I/O Block Diagram

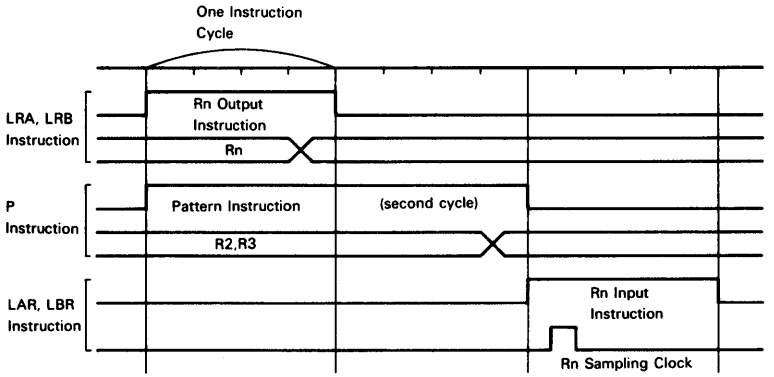


Figure 13 4-bit Data I/O Timing

- **1-bit Discrete Input/Output Common Terminals (D)**

The HMCS44C has 16 1-bit Discrete I/O Common Terminals.

The 1-bit Discrete I/O Common Terminal consists of a 1-bit latch and an I/O common pin.

The 1-bit Discrete I/O is addressed by the Y register. The addressed latch can be set or reset by output instruction and "0" and "1" a level can be tested with the addressed pin by input instruction.

Note that, since the latch output is directly connected to the pin even during execution of input instruction, the input data is wired logic of the latch output and the pin input. Therefore, the latch should be set to "1" not to affect the pin input before ex-

ecution of input instruction.

The D_0 to D_3 terminals are also addressed directly by the operand n of input/output instruction and can be set or reset.

The block diagram is shown in Figure 14 and the I/O timing is shown in Figure 15.

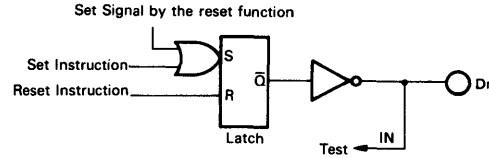


Figure 14 1-bit Discrete I/O Block Diagram

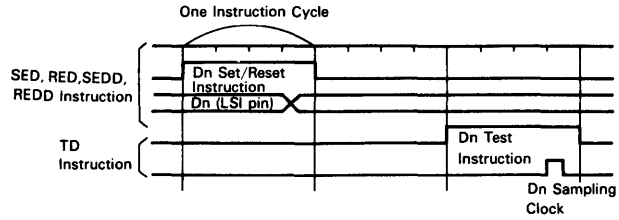
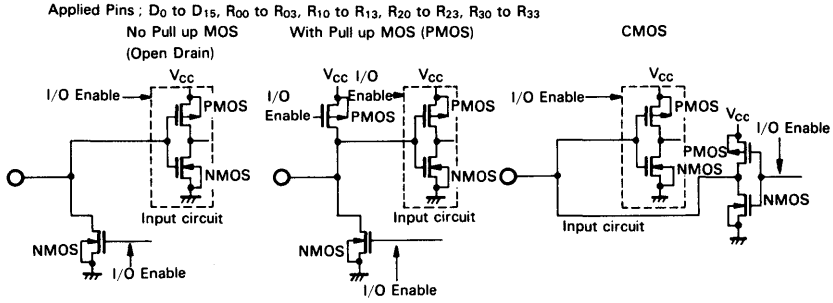


Figure 15 1-bit Discrete I/O Timing

- **I/O Configuration**

The I/O configuration of each pin can be specified among Open Drain and With Pull up MOS using a mask option as shown in Figure 16.



*When "Disable" is specified for the I/O State at the Halt State, the I/O Enable signal shown in the figure turns off the input circuit, Pull up MOS and NMOS output and sets CMOS output to high impedance (PMOS, NMOS; OFF).

Figure 16 I/O Configuration

■ TIMER/COUNTER

The timer/counter consists of the 4-bit counter and the 6-bit prescaler as shown in Figure 17. The 4-bit counter may be loaded under program control and is incremented toward 15 by the prescaler overflow output pulse or the input pulse of INT_1 pin (its leading edge is counted). The clock input to the counter is selected by the CF F/F. When the CF F/F is "0", the clock input is the prescaler overflow output pulse (Timer Mode). When the CF F/F is "1", the clock input is the input pulse of INT_1 pin (Counter Mode). When the counter reaches zero (returns from 15 to zero), the overflow output pulse is generated and the counter continues to count ($14 \rightarrow 15 \rightarrow 0 \rightarrow 1 \rightarrow 2 \cdots$).

The TF F/F is a flip-flop which masks interrupts from the timer/counter. It can be set and reset by interrupt instruction. If the overflow output pulse of the counter is generated when the TF F/F is reset ("0"), an interrupt request occurs and the TF F/F becomes "1". If the overflow output pulse is generated when the TF F/F is set ("1"), no interrupt request occurs. The TTF instruction enables the TF F/F to be tested.

The prescaler is a 6-bit frequency divider. It divides a system clock (instruction frequency) by 64 into the overflow output pulses of "instruction frequency ÷ 64".

The prescaler is cleared when data is loaded into the counter (by LTA or LTI instruction). The frequency division is 0 when the prescaler is cleared. At the 64th clock, an overflow output pulse is generated from the prescaler. During operation of the LSI, the prescaler is operating and cannot be stopped. The relation between the specified value of the counter and specified time in the Timer Mode is shown in Table 3.

The pulse width of the INT_1 pin in the Counter Mode must be at least 2-cycle time for both "High" and "Low" levels as shown in Figure 18.

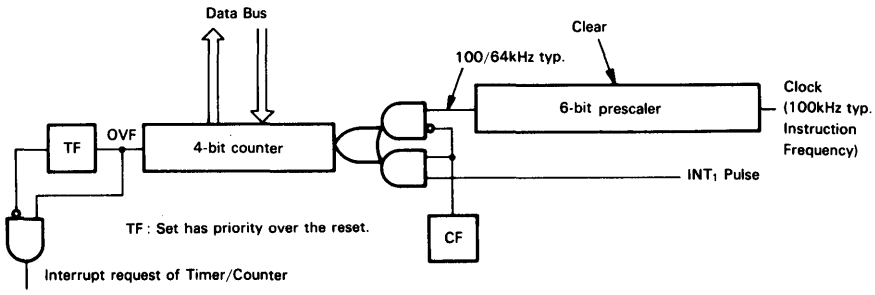


Figure 17 Timer/Counter Block Diagram

Table 3 Timer Range

Specified Value	Number of cycles	Time (ms)	Specified Value	Number of cycles	Time (ms)
0	1,024	10.24	8	512	5.12
1	960	9.60	9	448	4.48
2	896	8.96	10	384	3.84
3	832	8.32	11	320	3.20
4	768	7.68	12	256	2.56
5	704	7.04	13	192	1.92
6	640	6.40	14	128	1.28
7	576	5.76	15	64	0.64

[NOTE] Time is based on instruction frequency 100kHz. (one instruction cycle = 10μs)

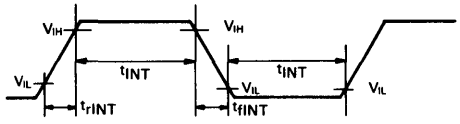


Figure 18 The Pulse Width of the INT_1 pin in the Counter Mode

■ INTERRUPT

The HMCS44C can be interrupted in two different ways: through the external interrupt input pins (INT_0, INT_1) and the timer/counter interrupt request. When any interrupt occurs, processing is suspended, the Status F/F is unchanged, the present program counter is pushed onto the stack ST1 and the contents of the stacks ST1, ST2 and ST3 are pushed onto the stacks ST2, ST3 and ST4 respectively. At that time, the Interrupt Enable F/F (I/E) is set and the address jumps to a fixed destination (Interrupt Address), and then the interrupt routine is executed. Stacking the registers other than the program counter must be performed by the program. The interrupt routine must end with RTNI (Return Interrupt) instruction which sets the I/E F/F simultaneously with the RTN instruction.

The Interrupt Address:

Input Interrupt Address . . . . .
1 Page 3F Address
Timer/Counter Interrupt Address . . . . .
0 Page 3F Address

The input interrupt has priority over the timer/counter interrupt.

The INT_0 and INT_1 pin have an interrupt request function.

Each terminal consists of a circuit which generates leading pulse and the interrupt mask F/F (IF0, IF1). An interrupt is enabled (unmasked) when the IF0 F/F or IF1 F/F is reset. When the INT_0 or INT_1 pin changes from "0" to "1" (from "Low" level to "High" level), a leading pulse is generated to produce an interrupt request. At the same time, the IF0 F/F or IF1 F/F is set. When the IF0 F/F or IF1 F/F is set, the interrupt masking for the pin will result. (If a leading pulse is generated, no interrupt request occurs.)

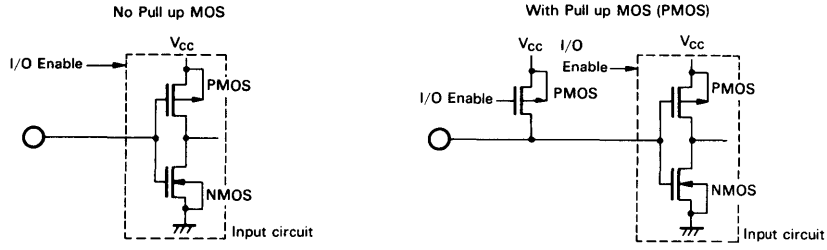
An interrupt request generated by the leading pulse is latched into the input interrupt request F/F (I/RI) on the input side. If the Interrupt Enable F/F (I/E) is "1" (Interrupt Enable State), an interrupt occurs immediately and the I/RI F/F and the I/E F/F are reset. If the I/E F/F is "0" (Interrupt Disable State), the I/RI F/F is held at "1" until the HMCS44C gets into the Interrupt Enable State.

The IF0 F/F, the IF1 F/F, the INT_0 pin and the INT_1 pin can be tested by interrupt instruction. Therefore, the INT_0 and the INT_1 can be used as additional input pins with latches.

The INT_0 pin and INT_1 pin can be provided with Pull up MOS using a mask option as shown in Figure 19.

An interrupt request from the timer/counter is latched into the timer interrupt request F/F (I/RT). The succeeding operations are the same as an interrupt from the input. Only the exception is that, since an interrupt from the input precedes a timer/counter interrupt, the input interrupt occurs if both the I/RI F/F and the I/RT F/F are "1" (when the input interrupt and the timer/counter interrupts are generated simultaneously). During this processing, the I/RT F/F remains "1". The timer/counter interrupt can be implemented after the input interrupt processing is achieved.

The interrupt circuit block diagram is shown in Figure 20.



*When "Disable" is specified for the I/O State at the Halt State, the I/O Enable signal shown in the figure turns off the input circuit and Pull up MOS.

Figure 19 Configuration of INT_0 and INT_1

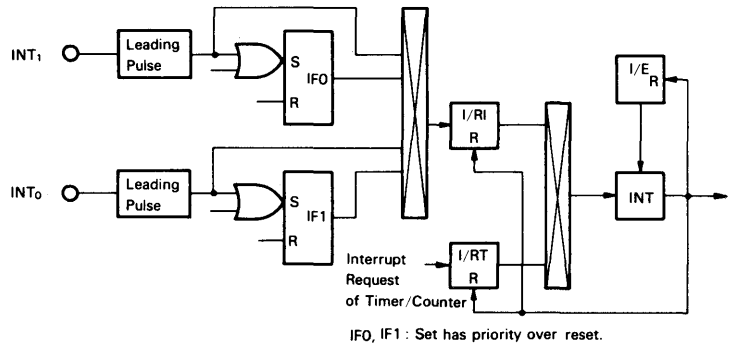


Figure 20 Interrupt Circuit Block Diagram

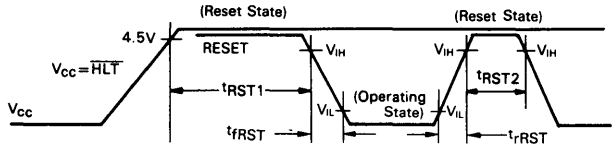
■ RESET FUNCTION

The reset is performed by setting the RESET pin to "1" ("High" level) and the HMCS44C gets into operation by setting it to "0" ("Low" level). Refer to Figure 21. Moreover, the HMCS44C has the automatic reset function (ACL; Built-in Reset Circuit). The Built-in Reset Circuit restricts the rise condition of the power supply. Refer to Figure 22. When the Built-in Reset Circuit is used, RESET should be connected to V_{SS}.

Internal state of the HMCS44C are specified as follows by the reset function.

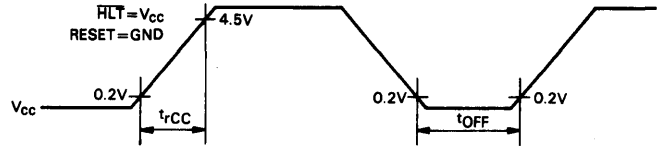
- Program Counter (PC) is set to 3F address on 31 page (31-3F).
- I/RI, I/RT, I/E and CF are reset to "0".
- IF0, IF1 and TF are set to "1".
- Reset/Set of I/O latch and register (D_0 to D_{15}, R0 to R6) are set to "1".

Note that other blocks (Status, Register, Timer/Counter, RAM, etc.) are not cleared.



- t_{RST1} includes the time required from the power ON until the operation gets into the constant state.
- t_{RST2} is applied when the operation is in the constant state.

Figure 21 RESET Timing



t_{OFF} specifies the period when the power supply is OFF in the case that a short break of the power supply occurs and the power supply ON/OFF is repeated.

Figure 22 Power Supply Timing for Built-in Reset Circuit

■ HALT FUNCTION

When the $\overline{HLT}$ pin is set to "0" ("Low" level), the internal clock stops and all the internal statuses (RAM, the Registers, the Carry F/F, the Status F/F, the Program Counter, and all the internal statuses) are held. Because all internal logic operation stop, power consumption is reduced. There are two input/output statuses in the Halt State. The user should specify either "Enable" or "Disable" using a mask option at the time of ordering ROM.

"Enable"
- Output ..... The Status before the Halt State is held.
- Pull up MOS... ON
- Input..... No relation to "Halt"

Since Pull up MOS is ON, Pull up MOS current flows with output "0" ("Low" level) in the Halt State (NMOS;ON). When an input signal changes, transmission current flows into an input circuit. Also, current flows into Pull up MOS. These currents are added to the Stand-by Supply Current (or Halt Current).

"Disable"
- Output ..... High Impedance (NMOS, PMOS: OFF)
- Pull up MOS... OFF
- Input..... Input Circuit: OFF

Both input and output are at high impedance state. Since an input circuit is OFF, any current other than the Stand-by Supply Current (or Halt Current) does not flow even if an input signal changes.

When the $\overline{HLT}$ pin is set to "1" ("High" level), the HMCS-44C gets into operation from the status just before the Halt State. The halt timing is shown in Figure 23.

CAUTION

If, during the Halt State, the external reset input is applied (RESET = "1" ("High" level)), the internal status is not held.

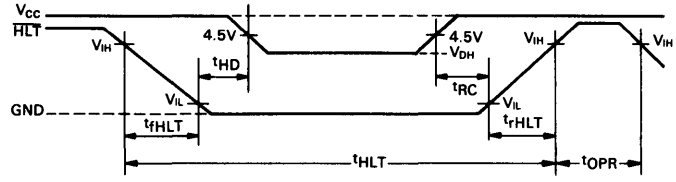


Figure 23 Halt Timing

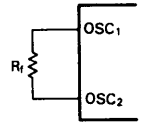
■ OSCILLATOR

The HMCS44C contains its own oscillator and frequency divider (CPG). The user can obtain the desired timing for operation of the LSI by merely connecting an resistor R_f or ceramic filter circuit (Internal Clock Operation).

The OSC_1 clock frequency is internally divided by four to produce the internal system clocks.

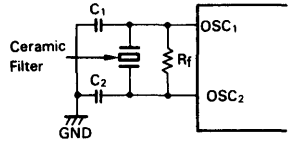
The user may exchange the external parts for the same LSI to select either of these two operational modes as shown in Figure 24. There is no need of specifying it by using the mask option.

(a) Internal Clock Operation Using Resistor R_f

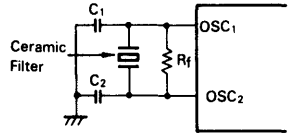


Wiring of OSC_1 and OSC_2 terminals should be as short as possible because the oscillation frequency is modified by capacitance of these terminals.

(b) Internal Clock Operation Using Ceramic Filter Circuit (Built-in CPG ; Ceramic Filter Oscillator) (This is not applied to HMCS44CL.)



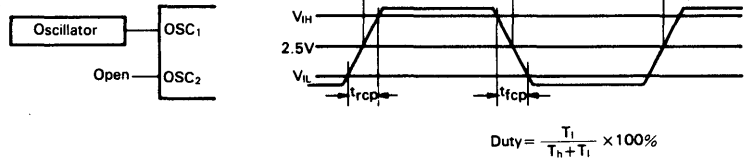
Ceramic Filter : CSB400P (MURATA)
R_f : 1MΩ±10%
C_1 : 2200pF±10% (ceramic capacitor)
C_2 : 470pF±10% (ceramic capacitor)



Ceramic Filter : FCR-400K (TDK)
R_f : 1MΩ±10%
C_1 : 1000pF±10% (ceramic capacitor)
C_2 : 1000pF±10% (ceramic capacitor)

The ceramic filter oscillation does not apply when using "Halt" and not resetting at the time of "Halt" cancellation.
This circuit is the example of the typical use. As the oscillation characteristics is not guaranteed, please consider and examine the circuit constants carefully on your application.

(c) External Clock Operation (External CPG)



$$\text{Duty} = \frac{T_l}{T_h + T_l} \times 100\%$$

Figure 24 Clock Operation Mode

■ INSTRUCTION LIST

The instructions of the HMCS44C are listed according to their functions, as shown in Table 4.

Table 4 Instruction List

Group	Mnemonic	Function	Status
Register · Register Instruction	LAB	B → A	
	LBA	A → B	
	LAY	Y → A	
	LASPX	SPX → A	
	LASPY	SPY → A	
	XAMR m	A ↔ MR (m)	
RAM Address Register Instruction	LXA	A → X	
	LYA	A → Y	
	LXI i	i → X	
	LYI i	i → Y	
	IY	Y+1 → Y	NZ
	DY	Y−1 → Y	NB
	AYY	Y+A → Y	C
	SYY	Y−A → Y	NB
	XSPX	X ↔ SPX	
	XSPY	Y ↔ SPY	
	XSPXY	X ↔ SPX, Y ↔ SPY	
RAM · Register Instruction	LAM (XY)	M → A (XY ↔ SPXY)	
	LBM (XY)	M → B (XY ↔ SPXY)	
	XMA (XY)	M ↔ A (XY ↔ SPXY)	
	XMB (XY)	M ↔ B (XY ↔ SPXY)	
	LMAIY (X)	A → M, Y+1 → Y (X ↔ SPX)	NZ
	LMADY (X)	A → M, Y−1 → Y (X ↔ SPX)	NB
Immediate Transfer Instruction	LMIIY i	i → M, Y+1 → Y	NZ
	LAI i	i → A	
	LBI i	i → B	
Arithmetic Instruction	AI i	A+i → A	C
	IB	B+1 → B	NZ
	DB	B−1 → B	NB
	AMC	M+A+C (F/F) → A	C
	SMC	M−A−$\overline{C}$ (F/F) → A	NB
	AM	M+A → A	C
	DAA	Decimal Adjustment (Addition)	
	DAS	Decimal Adjustment (Subtraction)	
	NEGA	$\overline{A}$+1 → A	
	COMB	$\overline{B}$ → B	
	SEC	"1" → C (F/F)	
	REC	"0" → C (F/F)	
	TC	Test C (F/F)	C (F/F)
	ROTL	Rotation Left	
	ROTR	Rotation Right	
	OR	A ∪ B → A	

(to be continued)

Group	Mnemonic	Function	Status
Compare Instruction	MNEI i	M ≠ i	NZ
	YNEI i	Y ≠ i	NZ
	ANEM	A ≠ M	NZ
	BNEM	B ≠ M	NZ
	ALEI i	A ≦ i	NB
	ALEM	A ≦ M	NB
	BLEM	B ≦ M	NB
RAM Bit Manipulation Instruction	SEM n	"1" → M (n)	
	REM n	"0" → M (n)	
	TM n	Test M (n)	M(n)
ROM Address Instruction	BR a	Branch on Status 1	1
	CAL a	Subroutine Jump on Status 1	1
	LPU u	Load Program Counter Upper on Status 1	
	TBR p	Table Branch	
	RTN	Return from Subroutine	
Interrupt Instruction	SEIE	"1" → I/E	
	SEIF0	"1" → IF0	
	SEIF1	"1" → IF1	
	SETF	"1" → TF	
	SECF	"1" → CF	
	REIE	"0" → I/E	
	REIF0	"0" → IF0	
	REIF1	"0" → IF1	
	RETF	"0" → TF	
	RECF	"0" → CF	
	TI0	Test INT_0	INT_0
	TI1	Test INT_1	INT_1
	TIF0	Test IF0	IF0
	TIF1	Test IF1	IF1
	TTF	Test TF	TF
	LTI i	i → Timer/Counter	
	LTA	A → Timer/Counter	
	LAT	Timer/Counter → A	
	RTNI	Return Interrupt	
Input/Output Instruction	SED	"1" → D (Y)	
	RED	"0" → D (Y)	
	TD	Test D (Y)	D(Y)
	SEDD n	"1" → D (n)	
	REDD n	"0" → D (n)	
	LAR p	R(p) → A	
	LBR p	R(p) → B	
	LRA p	A → R (p)	
	LRB p	B → R (p)	
	P p	Pattern Generation	
	NOP	No Operation	

[NOTE] 1. (XY) after a mnemonic code has four meanings as follows.

Mnemonic only	Instruction execution only
Mnemonic with X	After instruction execution, X ↔ SPX
Mnemonic with Y	After instruction execution, Y ↔ SPY
Mnemonic with XY	After instruction execution, X ↔ SPX, Y ↔ SPY

[Example]

LAM	M → A
LAMX	M → A, X ↔ SPX
LAMY	M → A, Y ↔ SPY
LAMXY	M → A, X ↔ SPX, Y ↔ SPY

2. Status column shows the factor which brings the Status F/F "1" under judgement instruction or instruction accompanying the judgement.
   - NZ ·····ALU Not Zero
   - C ·····ALU Overflow in Addition, that is, Carry
   - NB ·····ALU Overflow in Subtraction, that is, No Borrow
   - Except above ·····Contents of the status column affects the Status F/F directly.
3. The Carry F/F (C(F/F)) is not always affected by executing the instruction which affects the Status F/F.
   Instructions which affect the Carry F/F are eight as follows.

AMC	SEC
SMC	REC
DAA	ROTL
DAS	ROTR

4. All instructions except the pattern instruction (P) are executed in 1 instruction cycle. The pattern instruction (P) is executed in 2 instruction cycles.

HMCS44C Mask Option List

Date	
Customer's Name	
ROM CODE ID	
Hitachi P/N	

(1) I/O Option

Pin Name	I/O	I/O Option A	I/O Option B	I/O Option C	Remarks	Pin Name	I/O	I/O Option A	I/O Option B	I/O Option C	Remarks
D_0	I/O					R_{00}	I/O				
D_1	I/O					R_{01}	I/O				
D_2	I/O					R_{02}	I/O				
D_3	I/O					R_{03}	I/O				
D_4	I/O					R_{10}	I/O				
D_5	I/O					R_{11}	I/O				
D_6	I/O					R_{12}	I/O				
D_7	I/O					R_{13}	I/O				
D_8	I/O					R_{20}	I/O				
D_9	I/O					R_{21}	I/O				
D_{10}	I/O					R_{22}	I/O				
D_{11}	I/O					R_{23}	I/O				
D_{12}	I/O					R_{30}	I/O				
D_{13}	I/O					R_{31}	I/O				
D_{14}	I/O					R_{32}	I/O				
D_{15}	I/O					R_{33}	I/O				
INT_0	I										
INT_1	I										

☆ Specify the I/O composition with a mark of "○" in the applicable composition column.
A : No pull up MOS B : With pull up MOS C : CMOS Output

(2) Oscillator & Halt

Oscillator \ Halt	Not Used	Used (Reset is applied when Halt release)	Used (Reset is not applied when Halt release)
Resistor			
Ceramic Resonator			
External Clock			

☆ Please check one section on the above chart.

(3) I/O State at "Halt" Mode

I/O State
□ Enable
□ Disable

☆ Mark "✓" in "□" for the selected I/O state.

(4) Supply Voltage (V_{CC})

Supply Voltage (V_{CC})
□ 5±0.5V
□ 2.5V to 5.5V

☆ Mark "✓" in "□" for the selected supply voltage.

(5) Package

Package
□ DP-42
□ DP-42S

☆ Mark "✓" in "□" for the selected package.

HMCS45C(HD44820)
HMCS45CL(HD44828)

The HMCS45C is the CMOS 4-bit single chip microcomputer which contains ROM, RAM, I/O and Timer/Event Counter on single chip. The HMCS45C is designed to perform efficient controller function as well as arithmetic function for both binary and BCD data. The CMOS technology of the HMCS45C provides the flexibility of microcomputers for battery powered and battery back-up applications.

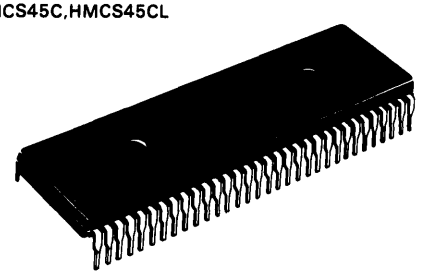
■ FEATURES

- 4-bit Architecture
- 2,048 Words of Program ROM (10 bits/Word)
  128 Words of Pattern ROM (10 bits/Word)
- 160 Digits of Data RAM (4 bits/Digit)
- 44 I/O Lines and 2 External Interrupt Lines
- Timer/Event Counter
- Instruction Cycle Time: HMCS45C; 10 μs
  HMCS45CL; 20 μs
- All Instructions except One Instruction; Single Word and Single Cycle
- BCD Arithmetic Instructions
- Pattern Generation Instruction
  – Table Look Up Capability –
- Powerful Interrupt Function
  3 Interrupt Sources
  ├ 2 External Interrupt Lines
  └ Timer/Event Counter
  Multiple Interrupt Capability
- Bit Manipulation Instructions for Both RAM and I/O
- Option of I/O Configuration Selectable on Each Pin; Pull Up MOS or CMOS or Open Drain
- Built-in Oscillator
- Built-in Power-on Reset Circuit (HMCS45C only)
- Low Operating Power Dissipation; 2mW typ.
- Stand-by Mode (Halt Mode); 50 μW max.
- CMOS Technology
- Single Power Supply: HMCS45C; 5V±10%
  HMCS45CL; 2.5V to 5.5V

HMCS45C,HMCS45CL

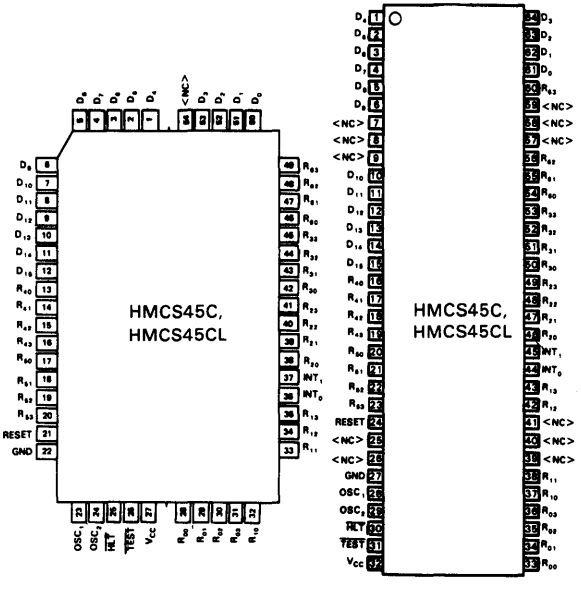
(FP-54)

HMCS45C,HMCS45CL



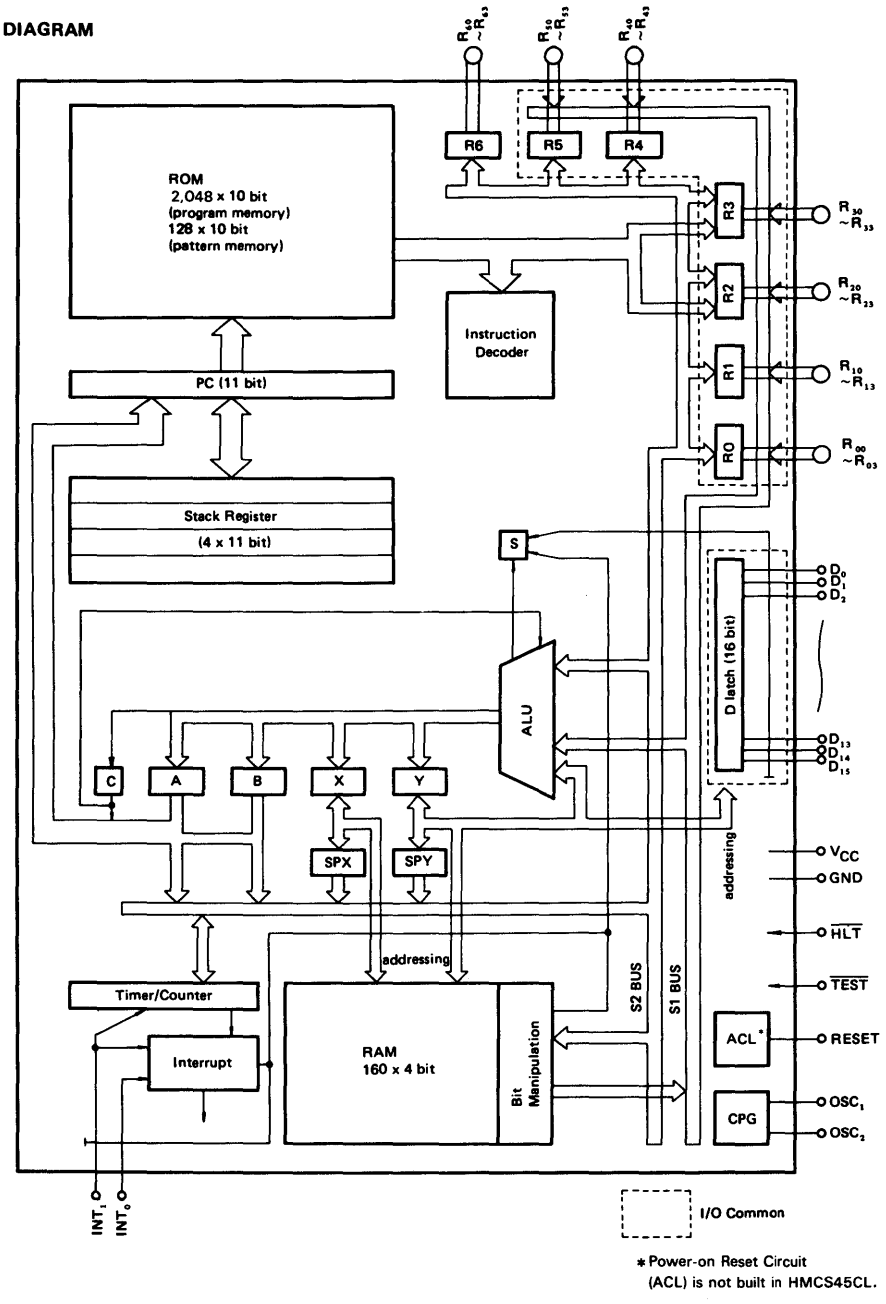
(DP-64S)

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



*Power-on Reset Circuit (ACL) is not built in HMCS45CL.

■ HMCS45C ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%)

• ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Remarks
Supply Voltage	V_{CC}	−0.3 to +7.0	V	
Terminal Voltage (1)	V_{T1}	−0.3 to V_{CC}+0.3	V	Except for terminals specified by V_{T2}
Terminal Voltage (2)	V_{T2}	−0.3 to +10.0	V	Applied to only open-drain output pins and open-drain I/O common pins.
Maximum Total Output Current (1)	$-\Sigma I_{O1}$	45	mA	[NOTE 3]
Maximum Total Output Current (2)	ΣI_{O2}	45	mA	[NOTE 3]
Operating Temperature	T_{opr}	−20 to +75	℃	
Storage Temperature	T_{stg}	−55 to +125	℃	

[NOTE 1] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under the conditions of "ELECTRICAL CHARACTERISTICS -1, -2". If these conditions are exceeded, it could affect reliability of LSI.
[NOTE 2] All voltages are with respect to GND.
[NOTE 3] Maximum Total Output Current is total sum of output currents which can flow out (or flow in) simultaneously.

● **ELECTRICAL CHARACTERISTICS-1** (V_{CC}=5V±10%, Ta=−20℃ to +75℃)

Item	Symbol	Test Conditions	Value			Unit	Note
			min.	typ.	max.		
Input "Low" Voltage	V_{IL}		–	–	1.0	V	
Input "High" Voltage (1)	V_{IH1}		V_{CC}−1.0	–	V_{CC}	V	2
Input "High" Voltage (2)	V_{IH2}		V_{CC}−1.0	–	10	V	3
Output "Low" Voltage	V_{OL}	I_{OL}=1.6mA	–	–	0.8	V	
Output "High" Voltage (1)	V_{OH1}	−I_{OH}=1.0mA	2.4	–	–	V	4
Output "High" Voltage (2)	V_{OH2}	−I_{OH}=0.01mA	V_{CC}−0.3	–	–	V	5
Interrupt Input Hold Time	tINT		2·T_{inst}	–	–	μs	
Interrupt Input Fall Time	tfINT		–	–	50	μs	
Interrupt Input Rise Time	trINT		–	–	50	μs	
Output "High" Current	I_{OH}	V_{OH}=10V	–	–	3	μA	6
Input Leakage Current	I_{IL}	V_{in}=0 to V_{CC}	–	–	1.0	μA	2
		V_{in}=0 to 10V	–	–	3		3
Pull up MOS Current	−I_P	V_{CC}=5V	60	–	250	μA	
Supply Current (1)	I_{CC1}	V_{in}=V_{CC}, Ceramic Filter Oscillation	–	–	2	mA	7
Supply Current (2)	I_{CC2}	V_{in}=V_{CC}, R_f Oscillation, External Clock Operation	–	–	1.0	mA	7
Standby I/O Leakage Current	I_{LS}	$\overline{HLT}$=1.0V, V_{in}=0 to V_{CC}	–	–	1	μA	2, 8
		$\overline{HLT}$=1.0V, V_{in}=0 to 10V	–	–	3	μA	3, 8
Standby Supply Current	I_{CCS}	V_{in}=V_{CC}, $\overline{HLT}$=0.2V	–	–	10	μA	9
External Clock Operation							
External Clock Frequency	f_{cp}		200	400	440	kHz	
External Clock Duty	Duty		45	50	55	%	
External Clock Rise Time	t_{rcp}		0	–	0.2	μs	
External Clock Fall Time	t_{fcp}		0	–	0.2	μs	
Instruction Cycle Time	T_{inst}	T_{inst}=4/f_{cp}	9.1	10	20	μs	
Internal Clock Operation (R_f Oscillation)							
Clock Oscillation Frequency	f_{osc}	R_f=91kΩ±2%	300	–	500	kHz	
Instruction Cycle Time	T_{inst}	T_{inst}=4/f_{osc}	8.0	–	13.3	μs	
Internal Clock Operation (Ceramic Filter Oscillation)							
Clock Oscillation Frequency	f_{osc}	Ceramic Filter Circuit	392	–	408	kHz	
Instruction Cycle Time	T_{inst}	T_{inst}=4/f_{osc}	9.8	–	10.2	μs	

[NOTE 1] All voltages are with respect to GND.
[NOTE 2] This is applied to RESET, $\overline{HLT}$, OSC_1, INT_0, INT_1 and the With Pull up MOS or CMOS type of I/O pins.
[NOTE 3] This is applied to the Open Drain type of I/O pins.
[NOTE 4] This is applied to the CMOS type of I/O or Output pins.
[NOTE 5] This is applied to the With Pull up MOS or CMOS type of I/O or Output pins.
[NOTE 6] This is applied to the Open Drain type of I/O or Output pins.
[NOTE 7] I/O current is excluded.
[NOTE 8] The Standby I/O Leakage Current is the I/O leakage current in the Halt and Disable State.
[NOTE 9] I/O current is excluded.
The Standby Supply Current is the supply current at V_{CC}=5V±10% in the Halt State. The supply current in the case where the supply voltage falls to the Halt Duration Voltage is called the Halt Current (I_{DH}), and it is shown in "ELECTRICAL CHARACTERISTICS-2."

●ELECTRICAL CHARACTERISTICS-2 (Ta=−20 to +75℃)

Reset and Halt

Item	Symbol	Test Conditions	Value			Unit
			min.	typ.	max.	
Halt Duration Voltage	V_{DH}	$\overline{HLT}$=0.2V	2.3	—	—	V
Halt Current	I_{DH}	$V_{in}=V_{CC}$ $\overline{HLT}$=0.2V, V_{DH}=2.3V	—	—	10	μA
Halt Delay Time	tHD		100	—	—	μs
Operation Recovery Time	tRC		100	—	—	μs
$\overline{HLT}$ Fall Time	tfHLT		—	—	1000	μs
$\overline{HLT}$ Rise Time	trHLT		—	—	1000	μs
$\overline{HLT}$ "Low" Hold Time	tHLT		400	—	—	μs
$\overline{HLT}$ "High" Hold Time	tOPR	R_f Oscillation, External Clock Operation	0.1	—	—	ms
		Ceramic Filter Oscillation	4	—	—	
Power Supply Rise Time	t_{rCC}	Built-in Reset, $\overline{HLT}=V_{CC}$	0.1	—	10	ms
Power Supply OFF Time	tOFF	Built-in Reset, $\overline{HLT}=V_{CC}$	1	—	—	ms
RESET Pulse Width (1)	tRST1	External Reset, V_{CC}=4.5 to 5.5V, $\overline{HLT}=V_{CC}$ (R_f Oscillation, External Clock Operation)	1	—	—	ms
		External Reset V_{CC}=4.5 to 5.5V, $\overline{HLT}=V_{CC}$ (Ceramic Filter Oscillation)	4	—	—	
RESET Pulse Width (2)	tRST2	External Reset V_{CC}=4.5 to 5.5V, $\overline{HLT}=V_{CC}$	2 · T_{inst}	—	—	μs
RESET Rise Time	t_{rRST}	External Reset V_{CC}=4.5 to 5.5V, $\overline{HLT}=V_{CC}$	—	—	20	ms
RESET Fall Time	tfRST	External Reset V_{CC}=4.5 to 5.5V, $\overline{HLT}=V_{CC}$	—	—	20	ms

[NOTE] All voltages are with respect to GND.

■ HMCS45CL ELECTRICAL CHARACTERISTICS (V_{CC}=2.5V to 5.5V)

●ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Remarks
Supply Voltage	V_{CC}	−0.3 to +7.0	V	
Terminal Voltage (1)	V_{T1}	−0.3 to V_{CC}+0.3	V	Except for terminals specified by V_{T2}
Terminal Voltage (2)	V_{T2}	−0.3 to +10.0	V	Applied to only open-drain output pins and open-drain I/O common pins.
Maximum Total Output Current (1)	$-\Sigma I_{O1}$	45	mA	(Note 3)
Maximum Total Output Current (2)	ΣI_{O2}	45	mA	(Note 3)
Operating Temperature	T_{opr}	−20 to +75	℃	
Storage Temperature	T_{stg}	−55 to +125	℃	

[NOTE 1] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under the conditions of "ELECTRICAL CHARACTERISTICS-1, -2." If these conditions are exceeded, it could affect reliability of LSI.

[NOTE 2] All voltages are with respect to GND.

[NOTE 3] Maximum Total Output Current is total sum of output currents which can flow out (or flow in) simultaneously.

● **ELECTRICAL CHARACTERISTICS-1** (V_{CC}=2.5 to 5.5V, Ta=−20 to +75℃)

Item	Symbol	Test Conditions		Value min.	Value typ.	Value max.	Unit	Note
Input "Low" Voltage	V_{IL}			—	—	0.15·V_{CC}	V	
Input "High" Voltage (1)	V_{IH1}			0.85·V_{CC}	—	V_{CC}	V	2
Input "High" Voltage (2)	V_{IH2}			0.85·V_{CC}	—	10	V	3
Output "Low" Voltage	V_{OL}	I_{OL}=0.4mA		—	—	0.4	V	
Output "High" Voltage	V_{OH}	−I_{OH}=0.08mA		V_{CC}−0.4	—	—	V	4
Interrupt Input Hold Time	tINT			2·Tinst	—	—	μs	
Interrupt Input Fall Time	tfINT			—	—	50	μs	
Interrupt Input Rise Time	trINT			—	—	50	μs	
Output "High" Current	I_{OH}	V_{OH}=10V		—	—	3	μA	5
Input Leakage Current	I_{IL}	V_{in}=0 to V_{CC}		—	—	1.0	μA	2
		V_{in}=0 to 10V		—	—	3		3
Pull-up MOS Current	−I_P	V_{CC}=3V		10	—	80	μA	
Supply Current	I_{CC}	V_{in}=V_{CC}, V_{CC}=3V (f_{OSC}/f_{CP}=200kHz) R_f Oscillation, External Clock Operation		—	—	140	μA	6
Standby I/O Leakage Current	I_{LS}	$\overline{HLT}$ =0.5V	V_{in}=0 to V_{CC}	—	—	1	μA	2, 7
			V_{in}=0 to 10V	—	—	3	μA	3, 7
Standby Supply Current	I_{CCS}	V_{in}=V_{CC}	V_{CC}=2.5 to 3.5V	—	—	6	μA	8
		$\overline{HLT}$=0.1V	V_{CC}=2.5 to 5.5V	—	—	10	μA	
External Clock Operation								
External Clock Frequency	f_{CP}			130	200	240	kHz	
External Clock Duty	Duty			45	50	55	%	
External Clock Rise Time	t_{rCP}			0	—	0.2	μs	
External Clock Fall Time	t_{fCP}			0	—	0.2	μs	
Instruction Cycle Time	T_{inst}	T_{inst}=4/f_{CP}		16.8	20	30.8	μs	
Internal Clock Operation (R_f Oscillation)								
Clock Oscillation Frequency	f_{OSC}	R_f=180kΩ±2% V_{CC}=2.5 to 3.5V		130	—	250	kHz	
		R_f=180kΩ±2% V_{CC}=2.5 to 5.5V		130	—	350		
Instruction Cycle Time	T_{inst}	T_{inst}=4/f_{OSC}, V_{CC}=2.5 to 3.5V		16	—	30.8	μs	
		T_{inst}=4/f_{OSC}, V_{CC}=2.5 to 5.5V		11.4	—	30.8		

[NOTE 1] All voltages are with respect to GND.
[NOTE 2] This is applied to RESET, $\overline{HLT}$, OSC_1, INT_0, INT_1 and the With Pull up MOS or CMOS type of I/O pins.
[NOTE 3] This is applied to the Open Drain type of I/O pins.
[NOTE 4] This is applied to the CMOS type of I/O or Output pins.
[NOTE 5] This is applied to the Open Drain type of I/O or Output pins.
[NOTE 6] I/O current is excluded.
[NOTE 7] The Standby I/O Leakage Current is the I/O leakage current in the Halt and Disable State.
[NOTE 8] I/O current is excluded.
The Standby Supply Current is the supply current at V_{CC}=2.5V to 5.5V in the Halt State. The supply current in the case where the supply voltage falls to the Halt Duration Voltage is called the Halt Current (I_{DH}), and it is shown in "ELECTRICAL CHARACTERISTICS-2."

● **ELECTRICAL CHARACTERISTICS-2** (Ta = −20 to +75℃)

Reset and Halt

Item	Symbol	Test Conditions	Value		Unit
			min.	max.	
Halt Duration Voltage	V_{DH}	$\overline{HLT}$=0.2V	2.0	—	V
Halt Current	I_{DH}	$V_{in}=V_{CC}$, $\overline{HLT}$=0.1V V_{DH}=2.0V	—	10	μA
Halt Delay Time	t_{HD}		200	—	μs
Operation Recovery Time	t_{RC}		200	—	μs
$\overline{HLT}$ Fall Time	t_{fHLT}		—	1000	μs
$\overline{HLT}$ Rise Time	t_{rHLT}		—	1000	μs
$\overline{HLT}$ "Low" Hold Time	t_{HLT}		800	—	μs
$\overline{HLT}$ "High" Hold Time	tOPR	R_f Oscillation, External Clock Operation V_{CC}=2.5 to 5.5V	0.2	—	ms
RESET Pulse Width (1)	t_{RST1}	External Reset, V_{CC}=2.5 to 5.5V, $\overline{HLT}=V_{CC}$ (R_f Oscillation, External Clock Operation)	2	—	ms
RESET Pulse Width (2)	t_{RST2}	External Reset, V_{CC}=2.5 to 5.5V $\overline{HLT}=V_{CC}$	2 · T_{inst}	—	μs
RESET Fall Time	t_{fRST}	$\overline{HLT}=V_{CC}$	—	20	ms
RESET Rise Time	t_{rRST}	$\overline{HLT}=V_{CC}$	—	20	ms

[NOTE] All voltages are with respect to GND.

■ SIGNAL DESCRIPTION

The input and output signals for the HMCS45C, shown in PIN ARRANGEMENT, are described in the following paragraphs.

● V_{CC} and GND

Power is supplied to the HMCS45C using these two pins. V_{CC} is power and GND is the ground connection.

● RESET

This pin allows resetting of the HMCS45C at times other than the automatic resetting capability (ACL; Built-in Reset Circuit) already in the HMCS45C.

The HMCS45C can be reset by pulling RESET high. Refer to RESET FUNCTION for additional information.

● OSC_1 and OSC_2

These pins provide control input for the built-in oscillator circuit. Resistor and capacitor, ceramic filter circuit, or an external oscillator can be connected to these pins to provide a system clock with various degrees of stability/cost tradeoffs.

Lead length and stray capacitance on these two pins should be minimized. Refer to OSCILLATOR for recommendations about these pins.

● $\overline{HLT}$

This pin is used to place the HMCS45C in the Halt State. Refer to HALT FUNCTION for details of the Halt Mode.

● TEST

This pin is not for user application and must be connected to V_{CC}

● INT_0 and INT_1

These pins provide the capability for asynchronously applying external interrupts to the HMCS45C.

Refer to INTERRUPTS for additional information.

● R_{00} to R_{03}, R_{10} to R_{13}, R_{20} to R_{23}, R_{30} to R_{33}, R_{40} to R_{43}, R_{50} to R_{53}

These 24 lines are arranged into six 4-bit Data Input/Output Common Channels.

The 4-bit registers (Data I/O Register) are attached to these channels. Each channel is directly addressed by the operand of input/output instruction. Refer to INPUT/OUTPUT for additional information.

● R_{60} to R_{63}

These 4 lines are the 4 bit Data Output Channel.

The 4-bit register (Data I/O Register) is attached to this channel. This channel is directly addressed by the operand of input/output instruction. Refer to INPUT/OUTPUT for additional information.

● D_0 to D_{15}

These lines are 16 1-bit Discrete Input/Output Common Pins. The 1-bit latches are attached to these pins. Each pin is addressed by the Y register. The D_0 to D_3 pins are also addressed directly by the operand of input/output instruction. Refer to INPUT/OUTPUT for additional information.

■ ROM

● ROM Address Space

ROM is used as a memory for the instructions and the patterns (constants). The instruction used in the HMCS45C consists of 10 bits. These 10 bits are called "a word", which is a unit for writing into ROM.

The ROM address is composed of the program area (0 page to 31 page) and the pattern area (61, 62 page) (64 words/page).

The ROM capacity is 2,176 words (1 word = 10 bits) in all.

Only the program area can contain both the instructions and the patterns (constants).

The ROM address space is shown in Figure 1.

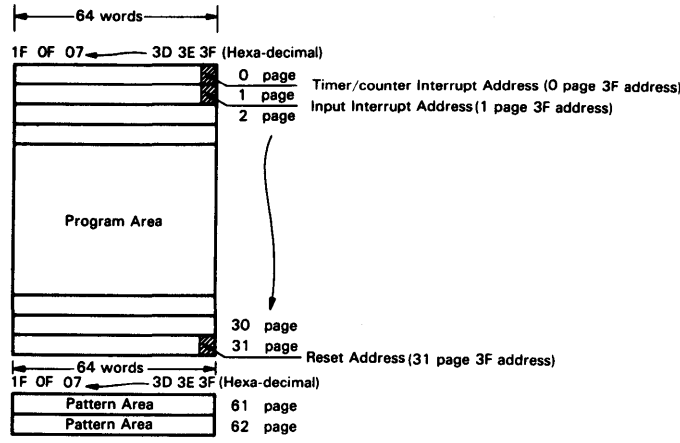


Figure 1 ROM Address Space

- **Program Counter (PC)**

The program counter is used for addressing of ROM. It consists of the page part and the address part as shown in Figure 2.

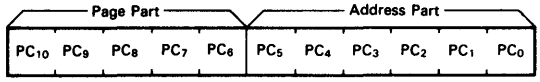


Figure 2 Configuration of Program Counter

Once a certain value is loaded into a page part, the content is unchanged until other value is loaded by the program. The settable value of a page part is any number between 0 to 31.

The address part is a 6-bit polynomial counter and counts up for each instruction cycle time. The sequence in the decimal and hexa-decimal system is shown in Table 1. This sequence is circulating and has neither the starting nor ending point. It doesn't generate an overflow carry. Consequently, the program on a same page is executed in order unless the value of the page part is changed.

Table 1 Program Counter Address Part Sequence

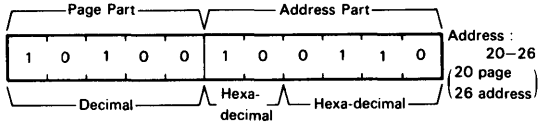
Decimal	Hexadecimal	Decimal	Hexadecimal	Decimal	Hexadecimal
63	3F	5	05	9	09
62	3E	11	0B	19	13
61	3D	23	17	38	26
59	3B	46	2E	12	0C
55	37	28	1C	25	19
47	2F	56	38	50	32
30	1E	49	31	37	25
60	3C	35	23	10	0A
57	39	6	06	21	15
51	33	13	0D	42	2A
39	27	27	1B	20	14
14	0E	54	36	40	28
29	1D	45	2D	16	10
58	3A	26	1A	32	20
53	35	52	34	0	00
43	2B	41	29	1	01
22	16	18	12	3	03
44	2C	36	24	7	07
24	18	8	08	15	0F
48	30	17	11	31	1F
33	21	34	22		
2	02	4	04		

- **Designation of ROM Address and ROM Code**

The page part of the ROM address is represented by decimal and the address part is divided into 2 parts (2 bits and 4 bits) and represented by hexa-decimal.

One word (10 bits) is divided into three parts (2 bits, 4 bits and 4 bits from the most significant bit O_{10}) and represented by hexadecimal. The examples are shown in Figure 3.

(a) ROM Address



(b) ROM Code

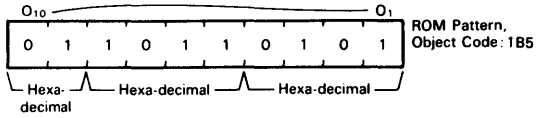


Figure 3 Designation of ROM Address and ROM Code

■ PATTERN GENERATION

The pattern (constants) can be accessed by the pattern instruction (P). The pattern can be written in any address of the ROM address space.

- **Reference**

ROM addressing for reference of the patterns is achieved by modifying the program counter with the accumulator, the B register, the Carry F/F and the operand p. Figure 4 shows how to modify the program counter. The address part is replaced with the accumulator and the lower 2 bits of B register, while the page part is ORed with the upper 2 bits of B register, the Carry F/F and the operand p (p_0, p_1). The upper bit (p_2) of the operand is for referring to the pattern area.

The value of the operand p is 0 to 7.

The content of the program counter is only modified apparently and is not changed. Then the address is counted up after the execution of the pattern instruction and the next instruction is executed.

The execution time of this instruction is 2-cycle time.

Even when interrupt is enable, interrupt is disabled in the second cycle of the pattern instruction. However, the interrupt request is latched into the interrupt request F/F.

- **Generation**

The pattern of referred ROM address is generated as the following two ways:

(i) The pattern is loaded into the accumulator and B register.

(ii)The pattern is loaded into the Data I/O registers R2 and R3.

Selection is determined by the command bits (O_9, O_{10}) in the pattern.

Mode (i) is performed when O_9 is "1" and mode (ii) is performed when O_{10} is "1".

Mode (i) and mode (ii) are simultaneously performed when both O_9 and O_{10} are "1".

The correspondence of each bit of the pattern is shown in Figure 5.

Examples of the pattern instruction usage is shown in Table 2.

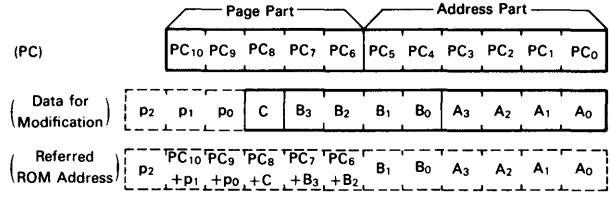


Figure 4 ROM Addressing for Pattern Generation

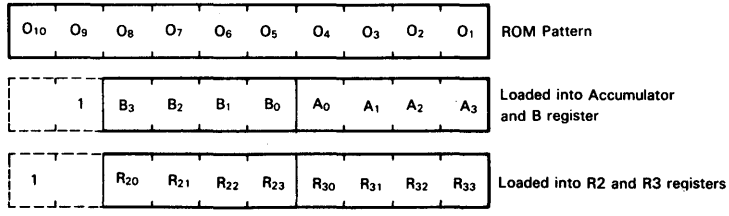


Figure 5 Correspondence of Each Bit of Pattern

Table 2 Example of Pattern Instruction Usage

Before Execution					Referred ROM Address	Pattern	After Execution			
PC Value	p	C	B	A			B	A	R2	R3
0-3F	1	0	A	0	10-20	12D	2	B	–	–
0-3F	7	1	4	0	61-00	22D	–	–	4	B
30-00	4	0/1	0	9	62-09	32D	2	B	4	B
30-00	4	0/1	F	9	63-39					

"–" means that the value is unchanged after the execution.
"0/1" means that either "0" or "1" will do.

■ BRANCH

ROM is accessed according to the program counter sequence and the program is executed. In order to jump to any address out of the sequence, there are four ways.

They are explained in the following paragraphs.

• BR

By BR instruction, the program branches to an address in the current page.

The lower 6 bits of ROM Object Code (operand a, O_6 to O_1) are transferred to the lower 6 bits of the program counter. This instruction is a conditional instruction and executed only when the Status F/F is "1". If it is "0", the instruction is skipped and the Status F/F becomes "1". The operation is shown in Figure 6.

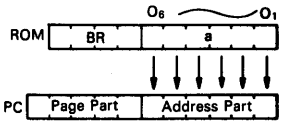


Figure 6 BR Operation

• LPU

By LPU instruction, the jump of page is performed.

The lower 5 bits of the ROM Object Code (operand u) are transferred to the page part of the program counter with a delay of 1 instruction cycle time. Therefore, the cycle just after the issuing of this instruction is on the same page and the page jump is performed at the next cycle.

This instruction is a conditional instruction and performed only when the Status is "1". But the Status is unchanged (remains "0") even if it is skipped. The operation is shown in Figure 7.

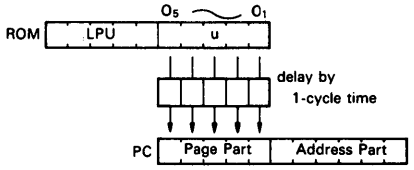


Figure 7 LPU Operation

• BRL

By BRL instruction, the program branches to an address in any page.

This instruction is a macro instruction of LPU and BR instructions, which is divided into two instructions as follows.

BRL a – b → LPU a
< Jump to b address on a page > BR b

BRL instruction is a conditional instruction because of characteristics of LPU and BR instructions, and is executed only when the Status F/F is "1". If the Status F/F is "0", the instruction is skipped and the Status F/F becomes "1".

• TBR (Table Branch)

By TBR instruction, the program branches by the table.

The program counter is modified with the accumulator, the B register, the Carry F/F, the operand p. The method for modification is shown in Figure 8.

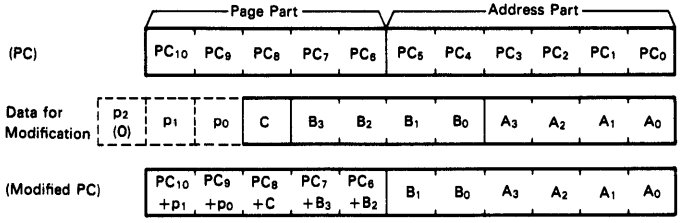


Figure 8 Modification of Program Counter by TBR Instruction

The accumulator and the lower 2 bits of B register are assigned into the address part of the program counter. The upper 2 bits of B register, Carry F/F, and the operand p_1, p_0 are ORed with the page part of the program counter.

TBR instruction is executed regardless of the Status F/F, and does not affect the Status F/F.

■ SUBROUTINE JUMP

There are two types of subroutine jumps. They are explained in the following paragraphs.

• CAL

By CAL instruction, subroutine jump to an address in the Subroutine Page.

The Subroutine Page is 0 page.

The address next to CAL instruction address is pushed onto the stack ST1 and the contents of the stacks ST1, ST2 and ST3 are pushed onto the stacks ST2, ST3 and ST4 respectively as shown in Figure 9.

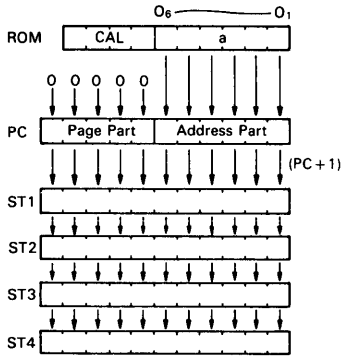


Figure 9 Subroutine Jump Stacking Order

The page part of the program counter is 0. The lower 6 bits (operand a, O_6 to O_1) of the ROM Object Code is transferred to the address part of the program counter.

The HMCS45C has 4 levels of stack (ST1, ST2, ST3 and ST4) which allows the programmer to use up to 4 levels of subroutine jumps (including interrupts).

CAL is a conditional instruction and executed only when the Status F/F is "1". If the Status F/F is "0", it is skipped and the Status F/F changes to "1".

• CALL

By CALL instruction, subroutine jump to an address in any page.

Subroutine jump to any address can be implemented by the subroutine jump to the page specified by LPU instruction.

This instruction is a macro instruction of LPU and CAL instructions, which is divided into two instructions as follows.

```
                                  CALL  a – b→LPU a
<Subroutine jump to b address on a page>   CAL b
```

CALL instruction is conditional because of characteristics of LPU and CAL instructions and is executed when the Status F/F is "1". If the Status F/F is "0", it is skipped and the Status F/F changes to "1"

■ RAM

RAM is a memory used for storing data and saving the contents of the registers. Its capacity is 160 digits (640 bits) where one digit consists of 4 bits.

Addressing of RAM is performed by a matrix of the file No. and the digit No.

The file No. is set in the X register and the digit No. in the Y register for reading, writing or testing. Specific digits in RAM can be addressed not via the X register and Y register. These digits are called "Memory Register (MR)", 0 to 15 (16 digits in all). The memory register can be exchanged with the accumulator by XAMR instruction.

The RAM address space is shown in Figure 10.

In an instruction in which reading from RAM and writing to RAM coexist (exchange between RAM and the register), reading precedes writing and the write data does not affect the read data.

The RAM bit manipulation instruction enables any addressed RAM bit to be set, reset or tested. The bit assignment is specified by the operand n of the instruction.

The bit test makes the Status F/F "1" and makes it "0" when the assigned bit is "0".

Correspondence between the RAM bit and the operand n is shown in Figure 11.

X \ Y (f \ d)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0															
1	1															
2	2															
3	3															
4	4															
5	5															
6	6															
7	7															
8–11*	8															
12–15*	9	MR15	MR14	MR13	MR12	MR11	MR10	MR9	MR8	MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0

← digit No.

↑ file No.

*The file 8 is selected when X register has any value in 8 to 11, and the file 9 is selected when 12 to 15.

Figure 10 RAM Address Space

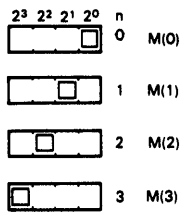


Figure 11 RAM Bit and Operand n

■ REGISTER

The HMCS45C has six 4-bit registers and two 1-bit registers available to the programmer. The 1-bit registers are the Carry F/F and the Status F/F. They are explained in the following paragraphs.

• Status F/F (S)

The Status F/F latches the result of logical or arithmetic operations (Not Zero, Overflow) and bit test operations. The Status F/F affects conditional instructions (LPU, BR and CAL instructions). These instructions are executed only when the Status F/F is "1". If it is "0", these instructions are skipped and the Status F/F becomes "1".

- **Accumulator (A; A Register) and Carry F/F (C)**

The result of the Arithmetic Logic Unit (ALU) operation (4 bits) and the overflow of the ALU are loaded into the accumulator and the Carry F/F. The Carry F/F can be set, reset or tested. Combination of the accumulator and the Carry F/F can be right or left rotated. The accumulator is the main register for ALU operation and the Carry F/F is used to store the overflow generated by ALU operation when the calculation of two or more digits (4 bits/digit) is performed.

- **B Register (B)**

The result of ALU operation (4 bits) is loaded into this register. The B register is used as a sub-accumulator to stack data temporarily and also used as a counter.

- **X Register (X)**

The result of ALU operation (4 bits) is loaded into this register. The X register has exchangeability for the SPX register. The X register addresses the RAM file and is composed of 4-bit register.

- **SPX Register (SPX)**

The SPX register has exchangeability for the X register.

The SPX register is used to stack the X register and expand the addressing system of RAM in combination with the X register. It is composed of 4-bit register.

- **Y Register (Y)**

The result of ALU operation (4 bits) is loaded into this register. The Y register has exchangeability for the SPY register. The Y register can calculate itself simultaneously with transferring data by the bus lines, which is usable for the calculation of two or more digits (4 bits/digit). The Y register addresses the RAM digit and 1-bit Discrete I/O.

- **SPY Register (SPY)**

The SPY register has exchangeability for the Y register. The SPY register is used to stack the Y register and expand the addressing system of RAM and 1-bit Discrete I/O in combination with the Y register.

■ INPUT/OUTPUT

- **4-bit Data Input/Output Channel (R)**

The HMCS45C has four 4-bit Data I/O Common Channels (R0, R1, R2, R3).

The 4-bit registers (Data I/O Register) are attached to R1, R2 and R3 channels.

Each channel is directly addressed by the operand p of input/output instruction.

The data is transferred from the accumulator and the B register to the Data I/O Registers R0 to R3 via the bus lines. Pattern instruction enables the patterns of ROM to be taken into the Data I/O Registers R2 and R3.

Input instruction enables the 4-bit data to be sent to the accumulator and the B register from R0 to R3. Note that, since the Data I/O Register output is directly connected to the pin even during execution of input instruction, the input data is wired logic of the Data I/O Register output and the pin input.

Therefore, the Data I/O Register should be set to 15 (all bits of the Data I/O Register is "1") not to affect the pin input before execution of input instruction.

The block diagram is shown in Figure 12. The I/O timing is shown in Figure 13.

- **1-bit Discrete Input/Output Common Terminals (D)**

The HMCS45C has 16 1-bit Discrete I/O Common Terminals.

The 1-bit Discrete I/O Common Terminal consists of a 1-bit latch and a I/O common pin.

The 1-bit Discrete I/O is addressed by the Y register. The addressed latch can be set or reset by output instruction and "0" and "1" a level can be tested with the addressed pin by input instruction.

Note that, since the latch output is directly connected to the pin even during execution of input instruction, the input data is wired logic of the latch output and the pin input. Therefore, the latch should be set to "1" not to affect the pin input before execution of input instruction.

The D_0 to D_3 terminals are also addressed directly by the operand n of input/output instruction and can be set or reset.

The block diagram is shown in Figure 14 and the I/O timing is shown in Figure 15.

- **I/O Configuration**

The I/O configuration of each pin can be specified among Open Drain and With Pull up MOS using a mask option as shown in Figure 16.

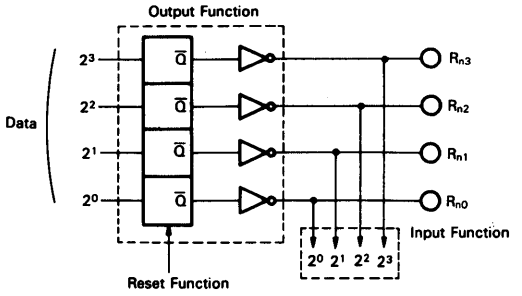


Figure 12 4-bit Data I/O Block Diagram

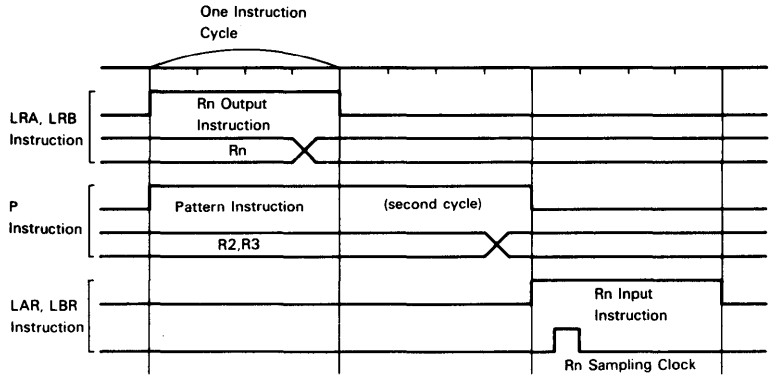


Figure 13 4-bit Data I/O Timing

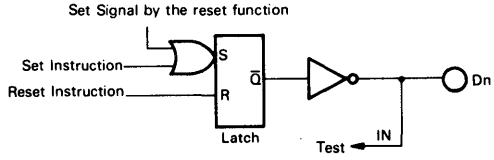


Figure 14 1-bit Discrete I/O Block Diagram

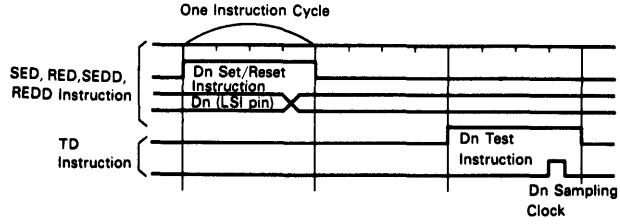
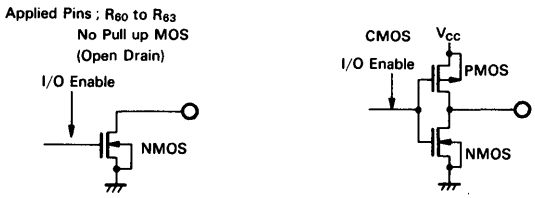
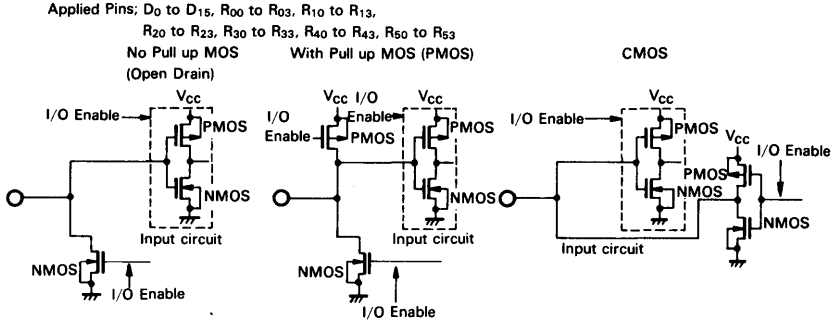


Figure 15 1-bit Discrete I/O Timing

(a) Configuration of Output Pin



(b) Configuration of I/O Pin



*When "Disable" is specified for the I/O State at the Halt State, the I/O Enable signal shown in the figure turns off the input circuit, Pull up MOS and NMOS output and sets CMOS output to high impedance (PMOS, NMOS; OFF).

Figure 16 I/O Configuration

■ TIMER/COUNTER

The timer/counter consists of the 4-bit counter and the 6-bit prescaler as shown in Figure 17. The 4-bit counter may be loaded under program control and is incremented toward 15 by the prescaler overflow output pulse or the input pulse of INT_1 pin (its leading edge is counted). The clock input to the counter is selected by the CF F/F. When the CF F/F is "0", the clock input is the prescaler overflow output pulse (Timer Mode). When the CF F/F is "1", the clock input is the input pulse of INT_1 pin (Counter Mode). When the counter reaches zero (returns from 15 to zero), the overflow output pulse is generated and the counter continues to count ($14 \rightarrow 15 \rightarrow 0 \rightarrow 1 \rightarrow 2 \cdots$).

The TF F/F is a flip-flop which masks interrupts from the timer/counter. It can be set and reset by interrupt instruction. If the overflow output pulse of the counter is generated when the TF F/F is reset ("0"), an interrupt request occurs and the TF F/F becomes "1". If the overflow output pulse is generated when the TF F/F is set ("1"), no interrupt request occurs. The TTF instruction enables the TF F/F to be tested.

The prescaler is a 6-bit frequency divider. It divides a system clock (instruction frequency) by 64 into the overflow output pulses of "instruction frequency ÷ 64".

The prescaler is cleared when data is loaded into the counter (by LTA or LTI instruction). The frequency division is 0 when the prescaler is cleared. At the 64th clock, an overflow output pulse is generated from the prescaler. During operation of the LSI, the prescaler is operating and cannot be stopped. The relation between the specified value of the counter and specified time in the Timer Mode is shown in Table 3.

The pulse width of the INT_1 pin in the Counter Mode must be at least 2-cycle time for both "High" and "Low" levels as shown in Figure 18.

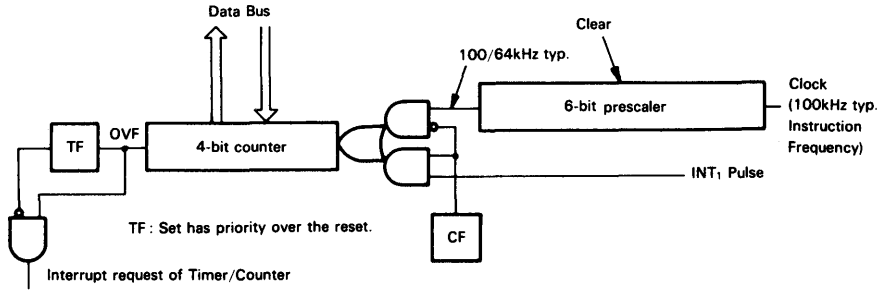


Figure 17 Timer/Counter Block Diagram

Table 3 Timer Range

Specified Value	Number of cycles	Time (ms)	Specified Value	Number of cycles	Time (ms)
0	1,024	10.24	8	512	5.12
1	960	9.60	9	448	4.48
2	896	8.96	10	384	3.84
3	832	8.32	11	320	3.20
4	768	7.68	12	256	2.56
5	704	7.04	13	192	1.92
6	640	6.40	14	128	1.28
7	576	5.76	15	64	0.64

[NOTE] Time is based on instruction frequency 100kHz. (one instruction cycle = 10μs)

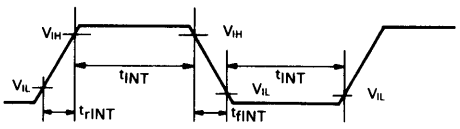


Figure 18 The Pulse Width of the INT_1 pin in the Counter Mode

■ INTERRUPT

The HMCS45C can be interrupted in two different ways: through the external interrupt input pins (INT_0, INT_1) and the timer/counter interrupt request. When any interrupt occurs, processing is suspended, the Status F/F is unchanged, the present program counter is pushed onto the stack ST1 and the contents of the stacks ST1, ST2 and ST3 are pushed onto the stacks ST2, ST3 and ST4 respectively. At that time, the Interrupt Enable F/F (I/E) is set and the address jumps to a fixed destination (Interrupt Address), and then the interrupt routine is executed. Stacking the registers other than the program counter must be performed by the program. The interrupt routine must end with RTNI (Return Interrupt) instruction which sets the I/E F/F simultaneously with the RTN instruction.

The Interrupt Address:

Input Interrupt Address .....
1 Page 3F Address

Timer/Counter Interrupt Address .....
0 Page 3F Address

The input interrupt has priority over the timer/counter interrupt.

The INT_0 and INT_1 pin have an interrupt request function.

Each terminal consists of a circuit which generates leading pulse and the interrupt mask F/F (IF0, IF1). An interrupt is enabled (unmasked) when the IF0 F/F or IF1 F/F is reset. When the INT_0 or INT_1 pin changes from "0" to "1" (from "Low" level to "High" level), a leading pulse is generated to produce an interrupt request. At the same time, the IF0 F/F or IF1 F/F is set. When the IF0 F/F or IF1 F/F is set, the interrupt masking for the pin will result. (If a leading pulse is generated, no interrupt request occurs.)

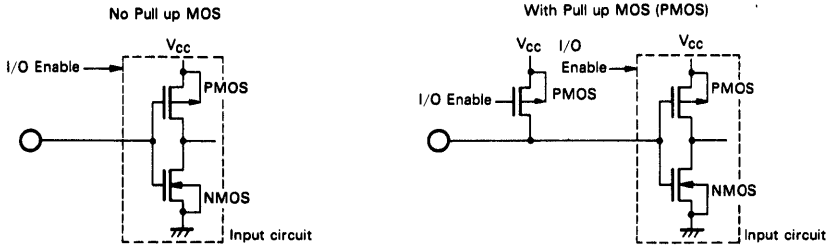
An interrupt request generated by the leading pulse is latched into the input interrupt request F/F (I/RI) on the input side. If the Interrupt Enable F/F (I/E) is "1" (Interrupt Enable State), an interrupt occurs immediately and the I/RI F/F and the I/E F/F are reset. If the I/E F/F is "0" (Interrupt Disable State), the I/RI F/F is held at "1" until the HMCS45C gets into the Interrupt Enable State.

The IF0 F/F, the IF1 F/F, the INT_0 pin and the INT_1 pin can be tested by interrupt instruction. Therefore, the INT_0 and the INT_1 can be used as additional input pins with latches.

The INT_0 pin and INT_1 pin can be provided with Pull up MOS using a mask option as shown in Figure 19.

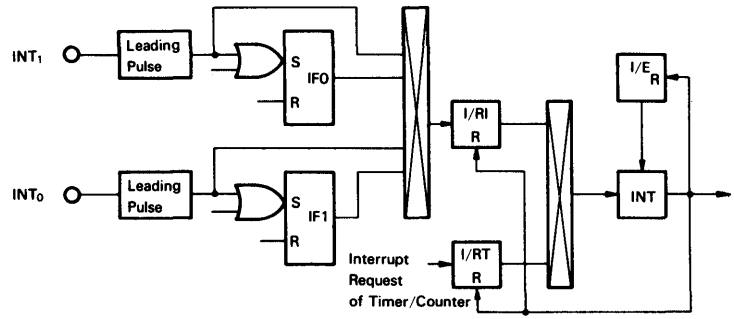
An interrupt request from the timer/counter is latched into the timer interrupt request F/F (I/RT). The succeeding operations are the same as an interrupt from the input. Only the exception is that, since an interrupt from the input precedes a timer/counter interrupt, the input interrupt occurs if both the I/RI F/F and the I/RT F/F are "1" (when the input interrupt and the timer/counter interrupts are generated simultaneously). During this processing, the I/RT F/F remains "1". The timer/counter interrupt can be implemented after the input interrupt processing is achieved.

The interrupt circuit block diagram is shown in Figure 20.



*When "Disable" is specified for the I/O State at the Halt State, the I/O Enable signal shown in the figure turns off the input circuit and Pull up MOS.

Figure 19 Configuration of INT_0 and INT_1



IF0, IF1 : Set has priority over reset.

Figure 20 Interrupt Circuit Block Diagram

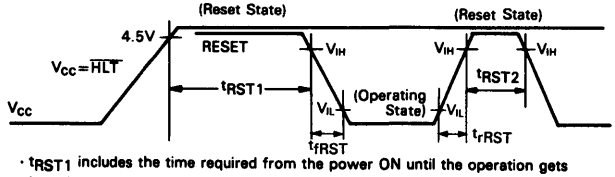
■ RESET FUNCTION

The reset is performed by setting the RESET pin to "1" ("High" level) and the HMCS45C gets into operation by setting it to "0" ("Low" level). Refer to Figure 21. Moreover, the HMCS45C has the automatic reset function (ACL; Built-in Reset Circuit). The Built-in Reset Circuit restricts the rise condition of the power supply. Refer to Figure 22. When the Built-in Reset Circuit is used, RESET should be connected to V_{SS}.

Internal state of the HMCS45C are specified as follows by the reset function.

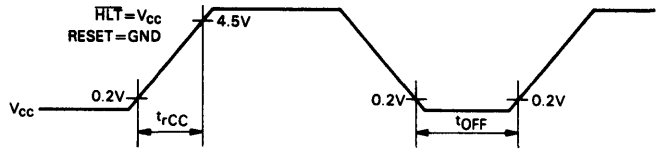
- Program Counter (PC) is set to 3F address on 31 page (31-3F).
- I/RI, I/RT, I/E and CF are reset to "0".
- IF0, IF1 and TF are set to "1".
- Reset/Set of I/O latch and register (D_0 to D_{15}, R0 to R6) are set to "1".

Note that other blocks (Status, Register, Timer/Counter, RAM, etc.) are not cleared.



- t_{RST1} includes the time required from the power ON until the operation gets into the constant state.
- t_{RST2} is applied when the operation is in the constant state.

Figure 21 RESET Timing



t_{OFF} specifies the period when the power supply is OFF in the case that a short break of the power supply occurs and the power supply ON/OFF is repeated.

Figure 22 Power Supply Timing for Built-in Reset Circuit

■ HALT FUNCTION

When the $\overline{HLT}$ pin is set to "0" ("Low" level), the internal clock stops and all the internal statuses (RAM, the Registers, the Carry F/F, the Status F/F, the Program Counter, and all the internal statuses) are held. Because all internal logic operation stop, power consumption is reduced. There are two input/output statuses in the Halt State. The user should specify either "Enable" or "Disable" using a mask option at the time of ordering ROM.

"Enable" — Output ..... The Status before the Halt State is held.
"Enable" — Pull up MOS... ON
"Enable" — Input..... No relation to "Halt"

Since Pull up MOS is ON, Pull up MOS current flows with output "0" ("Low" level) in the Halt State (NMOS;ON). When an input signal changes, transmission current flows into an input circuit. Also, current flows into Pull up MOS. These currents are added to the Stand-by Supply Current (or Halt Current).

"Disable" — Output ..... High Impedance (NMOS, PMOS: OFF)
"Disable" — Pull up MOS... OFF
"Disable" — Input..... Input Circuit: OFF

Both input and output are at high impedance state. Since an input circuit is OFF, any current other than the Stand-by Supply Current (or Halt Current) does not flow even if an input signal changes.

When the $\overline{HLT}$ pin is set to "1" ("High" level), the HMCS-45C gets into operation from the status just before the Halt State.

The halt timing is shown in Figure 23.

CAUTION

If, during the Halt State, the external reset input is applied (RESET = "1" ("High" level)), the internal status is not held.

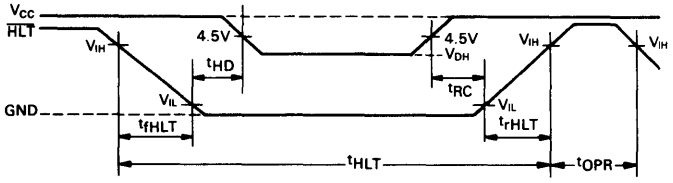


Figure 23 Halt Timing

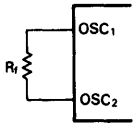
■ OSCILLATOR

The HMCS45C contains its own oscillator and frequency divider (CPG). The user can obtain the desired timing for operation of the LSI by merely connecting an resistor R_f or ceramic filter circuit (Internal Clock Operation).

The OSC_1 clock frequency is internally divided by four to produce the internal system clocks.

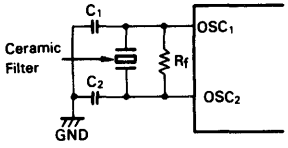
The user may exchange the external parts for the same LSI to select either of these two operational modes as shown in Figure 24. There is no need of specifying it by using the mask option.

(a) Internal Clock Operation Using Resistor R_f

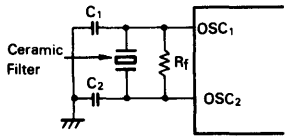


Wiring of OSC_1 and OSC_2 terminals should be as short as possible because the oscillation frequency is modified by capacitance of these terminals.

(b) Internal Clock Operation Using Ceramic Filter Circuit (Built-in CPG ; Ceramic Filter Oscillator) (This is not applied to HMCS45CL.)



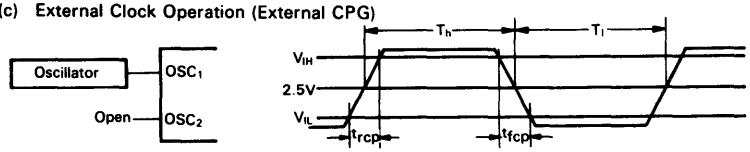
Ceramic Filter : CSB400P (MURATA)
R_f : 1MΩ ± 10%
C_1 : 2200pF ± 10% (ceramic capacitor)
C_2 : 470pF ± 10% (ceramic capacitor)



Ceramic Filter : FCR-400K (TDK)
R_f : 1MΩ ± 10%
C_1 : 1000pF ± 10% (ceramic capacitor)
C_2 : 1000pF ± 10% (ceramic capacitor)

The ceramic filter oscillation does not apply when using "Halt" and not resetting at the time of "Halt" cancellation.
This circuit is the example of the typical use. As the oscillation characteristics is not guaranteed, please consider and examine the circuit constants carefully on your application.

(c) External Clock Operation (External CPG)



$$Duty = \frac{T_l}{T_h + T_l} \times 100\%$$

Figure 24 Clock Operation Mode

■ INSTRUCTION LIST

The instructions of the HMCS45C are listed according to their functions, as shown in Table 4.

Table 4 Instruction List

Group	Mnemonic	Function	Status
Register · Register Instruction	LAB	B → A	
	LBA	A → B	
	LAY	Y → A	
	LASPX	SPX → A	
	LASPY	SPY → A	
	XAMR m	A ↔ MR (m)	
RAM Address Register Instruction	LXA	A → X	
	LYA	A → Y	
	LXI i	i → X	
	LYI i	i → Y	
	IY	Y+1 → Y	NZ
	DY	Y−1 → Y	NB
	AYY	Y+A → Y	C
	SYY	Y−A → Y	NB
	XSPX	X ↔ SPX	
	XSPY	Y ↔ SPY	
	XSPXY	X ↔ SPX, Y ↔ SPY	
RAM · Register Instruction	LAM (XY)	M → A (XY ↔ SPXY)	
	LBM (XY)	M → B (XY ↔ SPXY)	
	XMA (XY)	M ↔ A (XY ↔ SPXY)	
	XMB (XY)	M ↔ B (XY ↔ SPXY)	
	LMAIY (X)	A → M, Y+1 → Y (X ↔ SPX)	NZ
	LMADY (X)	A → M, Y−1 → Y (X ↔ SPX)	NB
Immediate Transfer Instruction	LMIIY i	i → M, Y+1 → Y	NZ
	LAI i	i → A	
	LBI i	i → B	
Arithmetic Instruction	AI i	A+i → A	C
	IB	B+1 → B	NZ
	DB	B−1 → B	NB
	AMC	M+A+C (F/F) → A	C
	SMC	M−A−$\overline{C}$ (F/F) → A	NB
	AM	M+A → A	C
	DAA	Decimal Adjustment (Addition)	
	DAS	Decimal Adjustment (Subtraction)	
	NEGA	$\overline{A}$+1 → A	
	COMB	$\overline{B}$ → B	
	SEC	"1" → C (F/F)	
	REC	"0" → C (F/F)	
	TC	Test C (F/F)	C (F/F)
	ROTL	Rotation Left	
	ROTR	Rotation Right	
	OR	A ∪ B → A	

(to be continued)

Group	Mnemonic	Function	Status
Compare Instruction	MNEI i	M ≠ i	NZ
	YNEI i	Y ≠ i	NZ
	ANEM	A ≠ M	NZ
	BNEM	B ≠ M	NZ
	ALEI i	A ≦ i	NB
	ALEM	A ≦ M	NB
	BLEM	B ≦ M	NB
RAM Bit Manipulation Instruction	SEM n	"1" → M (n)	
	REM n	"0" → M (n)	
	TM n	Test M (n)	M(n)
ROM Address Instruction	BR a	Branch on Status 1	1
	CAL a	Subroutine Jump on Status 1	1
	LPU u	Load Program Counter Upper on Status 1	
	TBR p	Table Branch	
	RTN	Return from Subroutine	
Interrupt Instruction	SEIE	"1" → I/E	
	SEIF0	"1" → IF0	
	SEIF1	"1" → IF1	
	SETF	"1" → TF	
	SECF	"1" → CF	
	REIE	"0" → I/E	
	REIF0	"0" → IF0	
	REIF1	"0" → IF1	
	RETF	"0" → TF	
	RECF	"0" → CF	
	TI0	Test INT_0	INT_0
	TI1	Test INT_1	INT_1
	TIF0	Test IF0	IF0
	TIF1	Test IF1	IF1
	TTF	Test TF	TF
	LTI i	i → Timer/Counter	
	LTA	A → Timer/Counter	
	LAT	Timer/Counter → A	
	RTNI	Return Interrupt	
Input/Output Instruction	SED	"1" → D (Y)	
	RED	"0" → D (Y)	
	TD	Test D (Y)	D(Y)
	SEDD n	"1" → D (n)	
	REDD n	"0" → D (n)	
	LAR p	R(p) → A	
	LBR p	R(p) → B	
	LRA p	A → R (p)	
	LRB p	B → R (p)	
	P p	Pattern Generation	
	NOP	No Operation	

[NOTE] 1. (XY) after a mnemonic code has four meanings as follows.

Mnemonic only	Instruction execution only
Mnemonic with X	After instruction execution, X ↔ SPX
Mnemonic with Y	After instruction execution, Y ↔ SPY
Mnemonic with XY	After instruction execution, X ↔ SPX, Y ↔ SPY

[Example]

LAM	M → A
LAMX	M → A, X ↔ SPX
LAMY	M → A, Y ↔ SPY
LAMXY	M → A, X ↔ SPX, Y ↔ SPY

2. Status column shows the factor which brings the Status F/F "1" under judgement instruction or instruction accompanying the judgement.
   - NZ ·····ALU Not Zero
   - C ·····ALU Overflow in Addition, that is, Carry
   - NB ·····ALU Overflow in Subtraction, that is, No Borrow
   - Except above ·····Contents of the status column affects the Status F/F directly.
3. The Carry F/F (C(F/F)) is not always affected by executing the instruction which affects the Status F/F.
   Instructions which affect the Carry F/F are eight as follows.

AMC	SEC
SMC	REC
DAA	ROTL
DAS	ROTR

4. All instructions except the pattern instruction (P) are executed in 1 instruction cycle. The pattern instruction (P) is executed in 2 instruction cycles.

HMCS45C Mask Option List

Date	
Customer's Name	
ROM CODE ID	
Hitachi P/N	

(1) I/O

Pin Name	I/O	I/O Option A	I/O Option B	I/O Option C	Remarks	Pin Name	I/O	I/O Option A	I/O Option B	I/O Option C	Remarks
D_0	I/O					R_{00}	I/O				
D_1	I/O					R_{01}	I/O				
D_2	I/O					R_{02}	I/O				
D_3	I/O					R_{03}	I/O				
D_4	I/O					R_{10}	I/O				
D_5	I/O					R_{11}	I/O				
D_6	I/O					R_{12}	I/O				
D_7	I/O					R_{13}	I/O				
D_8	I/O					R_{20}	I/O				
D_9	I/O					R_{21}	I/O				
D_{10}	I/O					R_{22}	I/O				
D_{11}	I/O					R_{23}	I/O				
D_{12}	I/O					R_{30}	I/O				
D_{13}	I/O					R_{31}	I/O				
D_{14}	I/O					R_{32}	I/O				
D_{15}	I/O					R_{33}	I/O				
						R_{40}	I/O				
						R_{41}	I/O				
						R_{42}	I/O				
						R_{43}	I/O				
						R_{50}	I/O				
						R_{51}	I/O				
						R_{52}	I/O				
						R_{53}	I/O				
						R_{60}	O				
						R_{61}	O				
INT_0	I					R_{62}	O				
INT_1	I					R_{63}	O				

☆ Specify the I/O composition with a mark of "○" in the applicable composition column.
A : No pull up MOS B : With pull up MOS C : CMOS Output

(2) Oscillator & Halt

Oscillator \ Halt	Not Used	Used (Reset is applied when Halt release)	Used (Reset is not applied when Halt release)
Resistor			
Ceramic Resonator			
External Clock			

☆ Please check one section on the above chart.

(3) I/O State at "Halt" Mode

I/O State
□ Enable
□ Disable

☆ Mark "v" in "□" for the selected I/O state.

(4) Supply Voltage (V_{CC})

Supply Voltage (V_{CC})
□ 5±0.5V
□ 2.5V to 5.5V

☆ Mark "v" in "□" for the selected supply voltage.

(5) Package

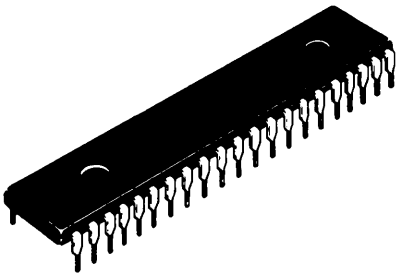
Package
□ FP-54
□ DP-64S

☆ Mark "v" in "□" for the selected package.

HMCS46C(HD44840), HMCS46CL(HD44848)

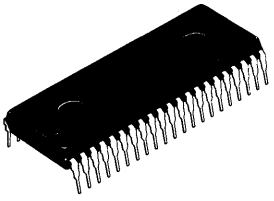
The HMCS46C is the CMOS 4-bit single chip microcomputer which contains ROM, RAM, I/O and Timer/Counter on single chip. The HMCS46C is designed to perform efficient controller function as well as arithmetic function for both binary and BCD data. The CMOS technology of the HMCS46C provides the flexibility of microcomputers for battery powered and battery back-up applications.

HMCS46C, HMCS46CL



(DP-42)

HMCS46C, HMCS46CL

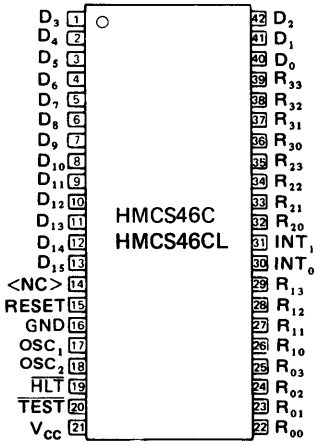


(DP-42S)

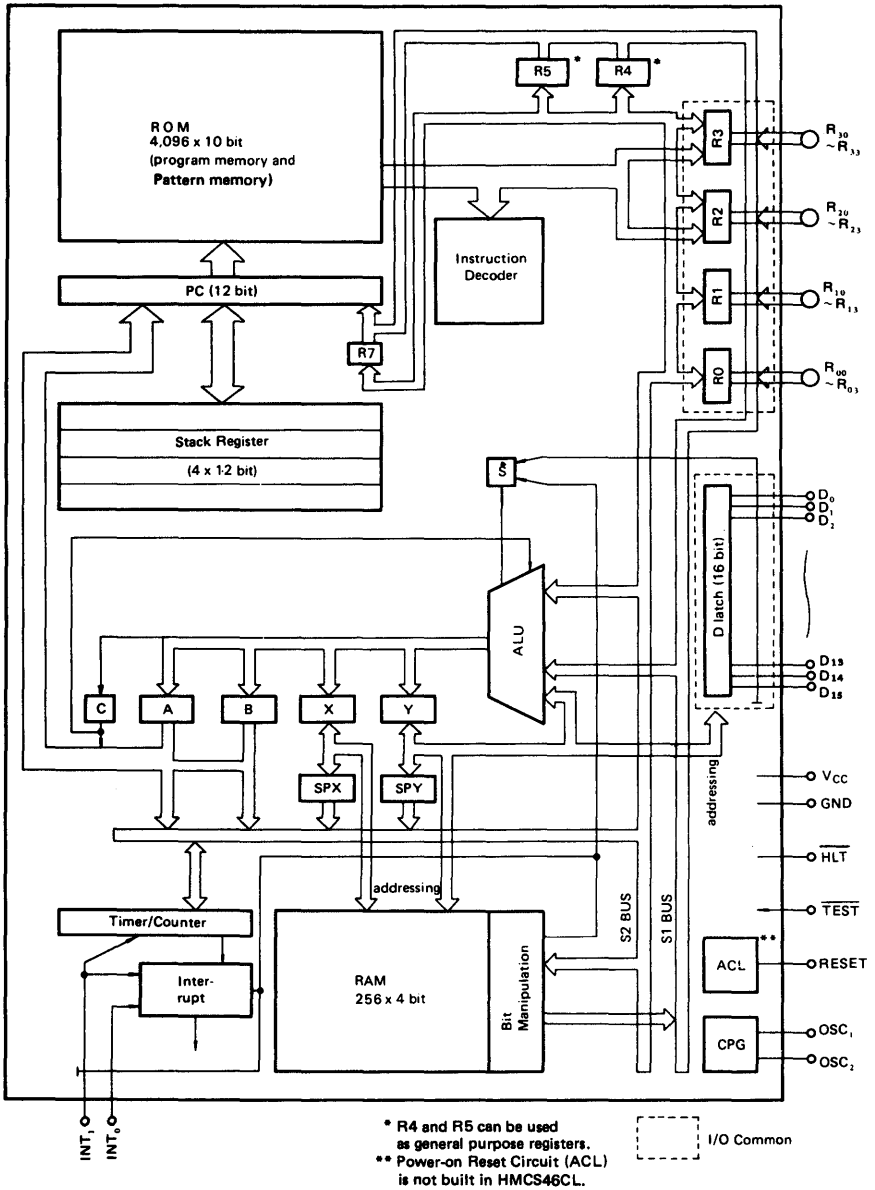
■ FEATURES

- 4-bit Architecture
- 4,096 Words of Program ROM and Pattern ROM (10 bits/Word)
- 256 Digits of Data RAM (4 bits/Digit)
- 32 I/O Lines and 2 External Interrupt Lines
- Timer/Counter
- Instruction Cycle Time;
  HMCS46C: 5μs
  HMCS46CL: 20μs
- All Instructions except One Instruction; Single Word and Single Cycle
- BCD Arithmetic Instructions
- Pattern Generation Instruction
  – Table Look Up Capability –
- Powerful Interrupt Function
  3 Interrupt Sources
  ├ 2 External Interrupt Lines
  └ Timer/Counter
  Multiple Interrupt Capability
- Bit Manipulation Instructions for Both RAM and I/O
- Option of I/O Configuration Selectable on Each Pin; With Puil up MOS or CMOS or Open Drain
- Built-in Oscillator
- Built-in Power-on Reset Circuit (HMCS46C only)
- Low Operating Power Dissipation; 3.3mW typ.
- Stand-by Mode (Half Mode); 66μW max.
- CMOS Technology
- Single Power Supply;
  HMCS46C: 5V ± 10%
  HMCS46CL: 2.5V to 5.5V

■ PIN ARRANGEMENT



■ BLOCK DIAGRAM



* R4 and R5 can be used as general purpose registers.
** Power-on Reset Circuit (ACL) is not built in HMCS46CL.

- **HMCS46C ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%)**
- **ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Value	Unit	Remarks
Supply Voltage	V_{CC}	-0.3 to +7.0	V	
Terminal Voltage (1)	V_{T1}	-0.3 to V_{CC} + 0.3	V	Except for the terminals specified by V_{T2}
Terminal Voltage (2)	V_{T2}	-0.3 to +10.0	V	Applied to the Open Drain type of Output pins and Open Drain type of I/O pins.
Maximum Total Output Current (1)	$-\Sigma I_{O1}$	45	mA	[NOTE 3]
Maximum Total Output Current (2)	ΣI_{O2}	45	mA	[NOTE 3]
Operating Temperature	T_{opr}	-20 to +75	°C	
Storage Temperature	T_{stg}	-55 to +125	°C	

[NOTE 1] Permanent LSI damage may occur if "Maximum Ratings" are exceeded. Normal operation should be under the conditions of "ELECTRICAL CHARACTERISTICS -1, -2." If these conditions are exceeded, it could be cause of malfunction of LSI and affects reliability of LSI.

[NOTE 2] All voltages are with respect to GND.

[NOTE 3] The Maximum Total Output Current is total sum of output currents which can flow out (or flow in) from or into the I/O pins and Output pins simultaneously.

• ELECTRICAL CHARACTERISTICS-1 (V_{CC} = 5V ± 10%, Ta = -20°C to +75°C)

Item	Symbol	Test Conditions	Value min.	Value typ.	Value max.	Unit	Note
Input "Low" Voltage	V_{IL}		–	–	1.0	V	
Input "High" Voltage (1)	V_{IH1}		V_{CC} - 1.0	–	V_{CC}	V	2
Input "High" Voltage (2)	V_{IH2}		V_{CC} - 1.0	–	10	V	3
Output "Low" Voltage	V_{OL}	I_{OL} = 1.6mA	–	–	0.8	V	
Output "High" Voltage (1)	V_{OH1}	$-I_{OH}$ = 1.0mA	2.4	–	–	V	4
Output "High" Voltage (2)	V_{OH2}	$-I_{OH}$ = 0.01mA	V_{CC} - 0.3	–	–	V	5
Interrupt Input Hold Time	t_{INT}		2·Tinst	–	–	μs	
Interrupt Input Fall Time	t_{fINT}		–	–	50	μs	
Interrupt Input Rise Time	t_{rINT}		–	–	50	μs	
Output "High" Current	I_{OH}	V_{OH} = 10V	–	–	3	μA	6
Input Leakage Current	I_{IL}	V_{in} = 0 to V_{CC}	–	–	1	μA	2
		V_{in} = 0 to 10V	–	–	3		3
Pull up MOS Current	$-I_P$	V_{CC} = 5V	60	–	250	μA	
Supply Current (1)	I_{CC1}	V_{in} = V_{CC}, V_{CC} = 5V, Ceramic Filter Oscillation, (f_{osc} = 800kHz)	–	–	2.0	mA	
Supply Current (2)	I_{CC2}	V_{in} = V_{CC}, V_{CC} = 5V R_f Oscillation, (f_{osc} = 800kHz) External Clock Operation (f_{cp} = 800kHz)	–	–	0.85	mA	7
Standby I/O Leakage Current	I_{LS}	$\overline{HLT}$ = 1.0V, V_{in} = 0 to V_{CC}	–	–	1	μA	5, 8
		$\overline{HLT}$ = 1.0V, V_{in} = 0 to 10V	–	–	3	μA	6, 8
Standby Supply Current	I_{CCS}	V_{in} =V_{CC}, $\overline{HLT}$ = 0.2V	–	–	12	μA	9
External Clock Operation							
External Clock Frequency	f_{cp}		350	–	850	kHz	
External Clock Duty	Duty		45	50	55	%	
External Clock Rise Time	t_{rcp}		0	–	0.2	μs	
External Clock Fall Time	t_{fcp}		0	–	0.2	μs	
Instruction Cycle Time	T_{inst}	T_{inst} = $4/f_{cp}$	4.7	–	11.4	μs	
Internal Clock Operation (R_f Oscillation)							
Clock Oscillation Frequency	f_{osc}	R_f = 51kΩ ± 2%	540	–	900	kHz	
Instruction Cycle Time	T_{inst}	T_{inst} = $4/f_{osc}$	4.4	–	7.4	μs	
Internal Clock Operation (Ceramic Filter Oscillation)							
Clock Oscillation Frequency	f_{osc}	Ceramic Filter Circuit	784	–	816	kHz	
Instruction Cycle Time	T_{inst}	T_{inst} = $4/f_{osc}$	4.9	–	5.1	μs	

[NOTE 1] All voltages are with respect to GND.

[NOTE 2] This is applied to RESET, $\overline{HLT}$, OSC_1, INT_0, INT_1 and the with Pull up MOS or CMOS type of I/O pins.

[NOTE 3] This is applied to the Open Drain type of I/O pins.

[NOTE 4] This is applied to the CMOS type of I/O pins.

[NOTE 5] This is applied to the with Pull up MOS or CMOS type of I/O pins.

[NOTE 6] This is applied to the Open Drain type of I/O pins.

[NOTE 7] I/O current is excluded.

[NOTE 8] The Standby I/O Leakage Current is the I/O leakage current in the Halt and Disable State.

[NOTE 9] I/O current is excluded.
The Standby Supply Current is the supply current at V_{CC} = 5V ± 10% in the Halt State. The supply current in the case where the supply voltage falls to the Halt Duration voltage is called the Halt Current (I_{DH}), and it is shown in "ELECTRICAL CHARACTERISTICS –2."

- **ELECTRICAL CHARACTERISTICS-2 (Ta = -20°C to +75°C)**

Reset and Halt

Item	Symbol	Test Conditions	Value min.	Value max.	Unit
Halt Duration Voltage	V_{DH}	$\overline{HLT}$ = 0.2V	2.3	–	V
Halt Current	I_{DH}	$V_{in} = V_{CC}$, $\overline{HLT}$ = 0.2V, V_{DH} = 2.3V	–	12	μA
Halt Delay Time	t_{HD}		100	–	μs
Operation Recovery Time	t_{RC}		100	–	μs
$\overline{HLT}$ Fall Time	t_{fHLT}		–	1000	μs
$\overline{HLT}$ Rise Time	t_{rHLT}		–	1000	μs
$\overline{HLT}$ "Low" Hold Time	t_{HLT}		400	–	μs
$\overline{HLT}$ "High" Hold Time	t_{OPR}	R_f Oscillation, External Clock Operation	0.1	–	ms
		Ceramic Filter Oscillation	4	–	
Power Supply Rise Time	t_{rCC}	Built-in Reset, $\overline{HLT} = V_{CC}$	0.1	10	ms
Power Supply OFF Time	t_{OFF}	Built-in Reset $\overline{HLT} = V_{CC}$	1	–	ms
RESET Pulse Width (1)	t_{RST1}	External Reset V_{CC} = 4.5 to 5.5V, $\overline{HLT} = V_{CC}$ (R_f Oscillation, External Clock Operation)	1	–	ms
		External Reset V_{CC} = 4.5 to 5.5V, $\overline{HLT} = V_{CC}$ (Ceramic Filter Oscillation)	4	–	
RESET Pulse Width (2)	t_{RST2}	External Reset V_{CC} = 4.5 to 5.5V, $\overline{HLT} = V_{CC}$	$2 \cdot T_{inst}$	–	μs
RESET Fall Time	t_{fRST}		–	20	ms
RESET Rise Time	t_{rRST}		–	20	ms

[NOTE] All voltages are with respect to GND.

- **HMCS46CL ELECTRICAL CHARACTERISTICS (2.5V to 5.5V)**
- **ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Value	Unit	Remarks
Supply Voltage	V_{CC}	-0.3 to +7.0	V	
Terminal Voltage (1)	V_{T1}	-0.3 to V_{CC} + 0.3	V	Except for the terminals specified by V_{T2}
Terminal Voltage (2)	V_{T2}	-0.3 to +10.0	V	Applied to the Open Drain type of Output pins and Open Drain type of I/O pins.
Maximum Total Output Current (1)	$-\Sigma I_{O1}$	45	mA	[NOTE 3]
Maximum Total Output Current (2)	ΣI_{O2}	45	mA	[NOTE 3]
Operating Temperature	T_{opr}	-20 to +75	°C	
Storage Temperature	T_{stg}	-55 to +125	°C	

[NOTE 1] Permanent LSI damage may occur if "Maximum Ratings" are exceeded. Normal operation should be under the conditions of "ELECTRICAL CHARACTERISTICS -1, -2." If these conditions are exceeded, it could be cause of malfunction of LSI and affects reliability of LSI.

[NOTE 2] All voltages are with respect to GND.

[NOTE 3] The Maximum Total Output Current is total sum of output currents which can flow out (or flow in) from or into the I/O pins and Output pins simultaneously.

- **ELECTRICAL CHARACTERISTICS – 1 (V_{CC} = 2.5 to 5.5V, Ta = -20 to +75°C)**

Item	Symbol	Test Condition	Value min.	Value typ.	Value max.	Unit	Note
Input "Low" Voltage	V_{IL}		–	–	0.15·V_{CC}	V	
Input "High" Voltage (1)	V_{IH1}		0.85·V_{CC}	–	V_{CC}	V	2
Input "High" Voltage (2)	V_{IH2}		0.85·V_{CC}	–	10	V	3
Output "Low" Voltage	V_{OL}	I_{OL} = 0.4 mA	–	–	0.4	V	
Output "High" Voltage	V_{OH}	$-I_{OH}$ = 0.08 mA	V_{CC}-0.4	–	–	V	4
Interrupt Input Hold Time	t_{INT}		2·T_{inst}	–	–	μs	
Interrupt Input Fall Time	t_{fINT}		–	–	50	μs	
Interrupt Input Rise Time	t_{rINT}		–	–	50	μs	
Output "High" Level Current	I_{OH}	V_{OH} = 10 V	–	–	3	μA	6
Input Leakage Current	I_{IL}	V_{in} = 0 to V_{CC}	–	–	1.0	μA	2
		V_{in} = 0 to 10V	–	–	3		3
Pull up MOS Current	$-I_P$	V_{CC} = 3V	10	–	80	μA	
Supply Current	I_{CC}	V_{in}=V_{CC}, V_{CC}=3V (f_{osc}/f_{cp} = 200kHz) R_f Oscillation, External Clock Operation	–	–	140	μA	7
Standby I/O Leakage Current	I_{LS}	$\overline{HLT}$ = 0.5V, V_{in}=0 to V_{CC}	–	–	1	μA	5, 8
		$\overline{HLT}$ = 0.5V, V_{in}=0 to 10V	–	–	3	μA	6, 8
Standby Supply Current	I_{CCS}	V_{in} = V_{CC}, V_{CC}=2.5 to 3.5V	–	–	6	μA	9
		$\overline{HLT}$ = 0.1 V, V_{CC}=2.5 to 5.5 V	–	–	10	μA	
External Clock Operation							
External Clock Frequency	f_{cp}		130	200	240	kHz	
External Clock Duty	Duty		45	50	55	%	
External Clock Rise Time	t_{rcp}		0	–	0.2	μs	
External Clock Fall Time	t_{fcp}		0	–	0.2	μs	
Instruction Cycle Time	T_{inst}	T_{inst} = 4/f_{cp}	16.8	20	30.8	μs	
Internal Clock Operation (R_f Oscillation)							
Clock Oscillation Frequency	f_{osc}	R_f = 200kΩ ± 2% V_{CC}=2.5 to 3.5V	130	–	250	kHz	
	f_{osc}	R_f= 200kΩ±2% V_{CC}=2.5 to 5.5V	130	–	350	kHz	
Instruction Cycle Time	T_{inst}	T_{Inst}=4/f_{osc} VCC=2.5 to 3.5V	16	–	30.8	μs	
	T_{inst}	T_{inst}=4/f_{osc} V_{CC}=2.5 to 5.5V	11.4	–	30.8	μs	

[NOTE 1] All voltages are with respect to GND.

[NOTE 2] This is applied to RESET, $\overline{HLT}$, OSC_1, INT_0, INT_1 and the with Pull up MOS or CMOS type of I/O pins.

[NOTE 3] This is applied to the Open Drain type of I/O pins.

[NOTE 4] This is applied to the CMOS type of I/O pins.

[NOTE 5] This is applied to the with Pull up MOS or CMOS type of I/O pins.

[NOTE 6] This is applied to the Open Drain type of I/O pins.

[NOTE 7] I/O current is excluded.

[NOTE 8] The Standby I/O Leakage Current is the I/O leakage current in the Halt and Disable State.

[NOTE 9] I/O current is excluded.
The Standby Supply Current is the supply current at V_{CC}=2.5 to 5.5V in the Halt State. The supply current in the case where the supply voltage falls to the Halt Duration voltage is called the Halt Current (I_{DH}), and it is shown in "ELECTRICAL CHARACTERISTICS-2."

- **ELECTRICAL CHARACTERISTICS-2 (Ta = -20 to +75°C)**
  Reset and Halt

Item	Symbol	Test Conditions	Value		Unit
			min.	max.	
Halt Duration Voltage	V_{DH}	$\overline{HLT}$ = 0.2V	2.0	–	V
Halt Current	I_{DH}	V_{in}=V_{CC}, V_{DH}=2.0V $\overline{HLT}$ = 0.1V	–	12	μA
Halt Delay Time	t_{HD}		200	–	μs
Operation Recovery Time	t_{RC}		200	–	μs
$\overline{HLT}$ Fall Time	t_{fHLT}		–	1000	μs
$\overline{HLT}$ Rise Time	t_{rHLT}		–	1000	μs
$\overline{HLT}$ "Low" Hold Time	t_{HLT}		800	–	μs
$\overline{HLT}$ "High" Hold Time	t_{OPR}	R_f Oscillation, External Clock Operation, V_{CC}=2.5 to 5.5V	0.2	–	ms
RESET Pulse Width (1)	t_{RST1}	External Reset V_{CC}=2.5 to 5.5V $\overline{HLT}$ = V_{CC} R_f Oscillation, External Clock Operation	2	–	ms
RESET Pulse Width (2)	t_{RST2}	External Reset V_{CC}=2.5 to 5.5V $\overline{HLT}$ = V_{CC}	$2 \cdot T_{inst}$	–	μs
RESET Fall Time	t_{fRST}	$\overline{HLT}$ = V_{CC}	–	20	ms
RESET Rise Time	t_{rRST}	$\overline{HLT}$ = V_{CC}	–	20	ms

(NOTE) All voltages are with respect to GND.

■ SIGNAL DESCRIPTION

The input and output signals for the HMCS46C, shown in PIN ARRANGEMENT, are described in the following paragraphs.

- **V_{CC} and GND**

Power is supplied to the HMCS46C using these two pins. V_{CC} is power and GND is the ground connection.

- **RESET**

This pin allows resetting of the HMCS46C at times other than the automatic resetting capability (ACL; Built-in Reset Circuit) already in the HMCS46C. The HMCS46C can be reset by pulling RESET high. Refer to RESET FUNCTION for additional information.

- **OSC_1 and OSC_2**

These pins provide control input for the built-in oscillator circuit. A resistor, ceramic filter circuit, or an external oscillator can be connected to these pins to provide a system clock with various degrees of stability/cost tradeoffs. Lead length and stray capacitance on these two pins should be minimized. Refer to OSCILLATOR for recommendations about these pins.

- **$\overline{HLT}$**

This pin is used to place the HMCS46C in the Halt State (Stand-by Mode).

The HMCS46C can be moved into the Halt State by pulling $\overline{HLT}$ low.

In the Halt State, the internal clock stops and all the internal statuses (the RAM, the registers, the Carry F/F, the Status F/F, the Program Counter, and all the internal statuses) are held.

Consequently, the power consumption is reduced. By pulling $\overline{HLT}$ high, the HMCS46C starts operation from the state just before the Halt State.

Refer to HALT FUNCTION for details of the Halt Mode.

- **$\overline{TEST}$**

This pin is not for user application and must be connected to V_{CC}.

- **INT_0 and INT_1**

These pins provide the capability for asynchronously applying external interrupts to the HMCS46C.

Refer to INTERRUPTS for additional information.

- **$R_{00} - R_{03}$, $R_{10} - R_{13}$, $R_{20} - R_{23}$, $R_{30} - R_{33}$**

These 16 lines are arranged into four 4-bit Data Input/Output Common Channels.

The 4-bit registers (Data I/O Register) are attached to these channels. Each channel is directly addressed by the operand of input/output instruction. Refer to INPUT/OUTPUT for additional information.

- **$D_0 - D_{15}$**

These lines are 16 1-bit Discrete Input/Output Common Terminals.

The 1-bit latches are attached to these terminals. Each terminal is addressed by the Y register. The D_0 to D_3 terminals are also addressed directly by the operand of input/output instruction. Refer to INPUT/OUTPUT for additional information.

- **ROM**
- **ROM Address Space**

ROM is used as a memory for the instructions and the patterns (constants). The instruction used in the HMCS46C consists of 10 bits. These 10 bits are called "a word", which is a unit for writing into ROM.

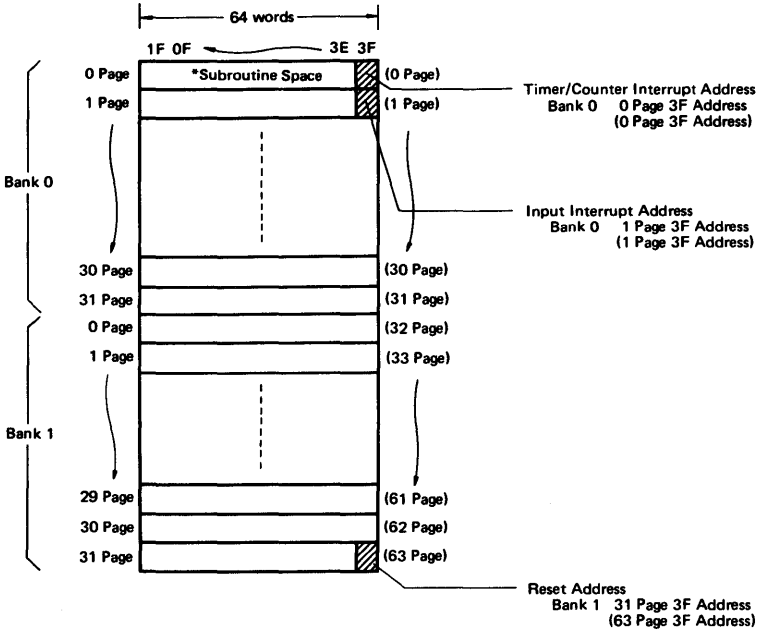
The ROM address has been split into two banks.

Each bank is composed of 32 pages (64 words/page).

The ROM capacity is 4,096 words (1 word = 10 bits) in all.

All addresses can contain both the instructions and the patterns (constants).

The ROM address space is shown in Figure 1.



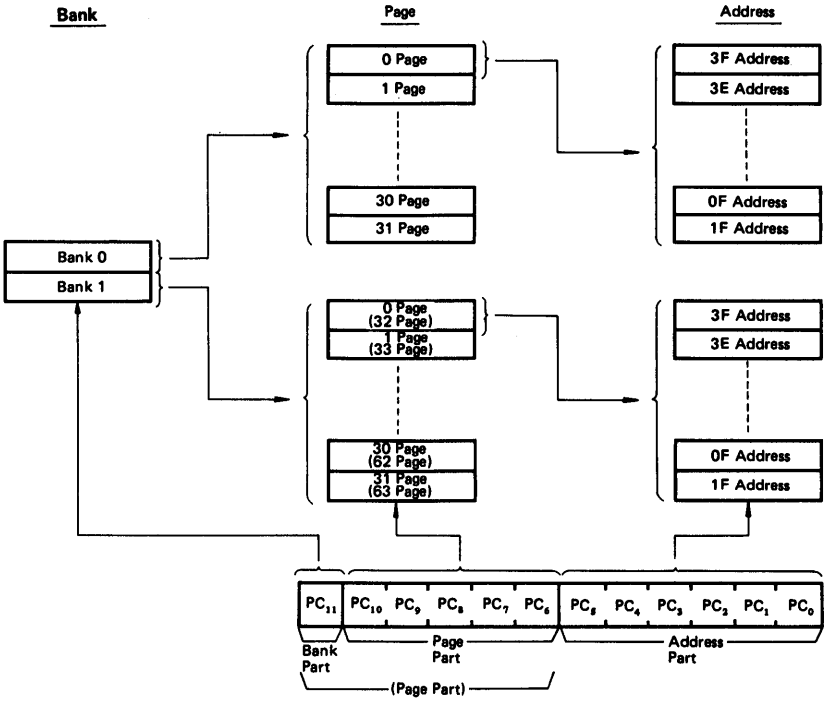
*Bank 0 0 Page (0 Page) is the Subroutine Space.

Note: The parenthesized contents are expressions of the Page, combining the bank part with the page part.

Figure 1 ROM Address Space

- **Program Counter (PC)**

The program counter is used for addressing of ROM. The program counter consists of the bank part, the page part, and the address part as shown in Figure 2.



Note: The parenthesized contents are expressions of the Page, combining the bank part with the page part.

Figure 2 Configuration of Program Counter

The bank part is a 1-bit register and the page part is a 5-bit register.

Once a certain value is loaded into the bank part or the page part, the content is unchanged until other value is loaded by a program.

The settable value is "0" (the Bank 0) or "1" (the Bank 1) for the bank part, and 0 to 31 for the page part.

The address part is a 6-bit polynomial counter and counts up for each instruction cycle time. The sequence in the decimal and hexa-decimal system is shown in Table 1. This sequence is circulating and has neither the starting nor ending point. It doesn't generate an overflow carry. Consequently, the program on a same page is executed in order unless the value of the bank part or the page part is changed.

Table 1 Program Counter Address Part Sequence

Decimal	Hexa-decimal	Decimal	Hexa-decimal	Decimal	Hexa-decimal
63	3F	5	05	9	09
62	3E	11	0B	19	13
61	3D	23	17	38	26
59	3B	46	2E	12	0C
55	37	28	1C	25	19
47	2F	56	38	50	32
30	1E	49	31	37	25
60	3C	35	23	10	0A
57	39	6	06	21	15
51	33	13	0D	42	2A
39	27	27	1B	20	14
14	0E	54	36	40	28
29	1D	45	2D	16	10
58	3A	26	1A	32	20
53	35	52	34	0	00
43	28	41	29	1	01
22	16	18	12	3	03
44	2C	36	24	7	07
24	18	8	08	15	0F
48	30	17	11	31	1F
33	21	34	22		
2	02	4	04		

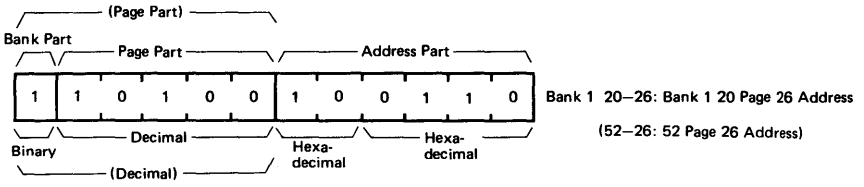
- **Designation of ROM Address and ROM Code**

The bank part of the ROM address is shown in the binary system and the page part in the decimal system. The address part is divided into 2 bits and 4 bits, and shown in the hexa-decimal system.

It is possible to combine the bank part and the page part and show the combined part as the Page (in the decimal system). In this case, the 0 Page to the 31 Page in the Bank 1 are shown as the 32 Page to the 63 Page. The examples are shown in Figure 3.

One word (10 bits) of ROM is divided into three parts (2 bits, 4 bits and 4 bits from the most significant bit O_{10} in order) shown in the hexa-decimal system. The examples are shown in Figure 3.

(a) ROM Address



(b) ROM Code

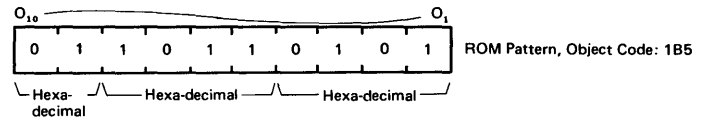


Figure 3 Designation of ROM Address and ROM Code

■ PATTERN GENERATION

The pattern (constant) can be accessed by the pattern instruction (P). The pattern can be written in any address of the ROM address space.

- **Reference**

ROM addressing for reference of the patterns is achieved by modifying the program counter with the accumulator, the B register, the Carry F/F and the operand p. Figure 4 shows how to modify the program counter. The address part is replaced with the accumulator and the lower 2 bits of B register, while the page part and the bank part are ORed with the upper 2 bits of B register, the Carry F/F and the operand p.

The value of the operand p (p_2, p_1, p_0) is 0 to 7 (decimal).

The bank part of the ROM address to be referenced to is determined by the logical equation: $PC_{11} + p_2$ (p_2 = the MSB of the operand p).

If the address where the pattern instruction exists is in the Bank 1, only the pattern of the Bank 1 can be referenced.

If the address where the pattern instruction exists is in the Bank 0, the pattern of the either Bank 1 or Bank 0 can be referenced depending on the value of p_2. The truth table of the bank part of the ROM address is shown in Table 2.

The value of the program counter is apparently modified and does not change actually. After execution of the pattern instruction, the program counter counts up and the next instruction is executed.

The pattern instruction is executed in 2-cycle time.

- **Generation**

The pattern of referred ROM address is generated as the following two ways:

(i) The pattern is loaded into the accumulator and B register.

(ii) The pattern is loaded into the Data I/O Registers R2 and R3.

Selection is determined by the command bits (O_9, O_{10}) in the pattern.

Mode (i) is performed when O_9 is "1" and mode (ii) is performed when O_{10} is "1".

Mode (i) and (ii) are simultaneously performed when both of O_9 and O_{10} are "1". The correspondence of each bit of the pattern is shown in Figure 5.

Examples of the pattern instruction usage is shown in Table 3.

CAUTION

In the program execution, the pattern can not be distinguished from the instruction. When the program is executed at the addresses into which pattern is written, the instruction corresponding to the pattern bit is executed. Take care that a pattern is not executed as an instruction.

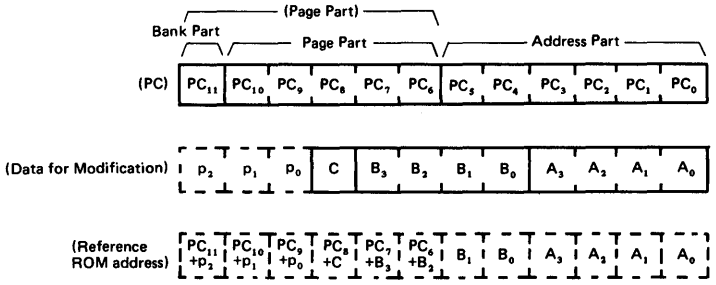


Figure 4 ROM Addressing for Pattern Generation

Table 2 Bank Part Truth Table of Pattern Generation

PC_{11}	p_2	Bank part of ROM address to be referenced to
1 (Bank 1)	1	1 (Bank 1)
	0	1 (Bank 1)
0 (Bank 0)	1	1 (Bank 1)
	0	0 (Bank 0)

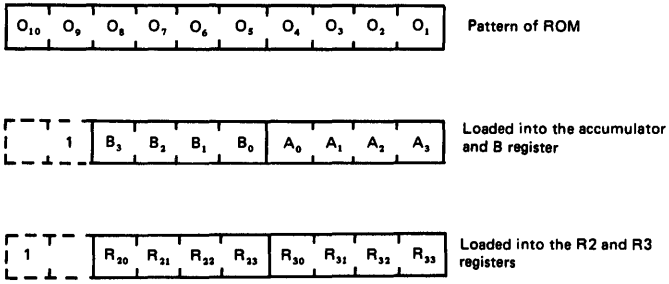


Figure 5 Correspondence of Each Bit of Pattern

Table 3 Example of Pattern Instructions Usage

Before Execution					Referred ROM Address	ROM Pattern	After Execution			
PC	p	C	B	A			B	A	R2	R3
Bank 0 0-3F (0-3F)	1	0	A	0	Bank 0 10-20 (10-20)	12D	2	B	–	–*
Bank 0 0-3F (0-3F)	7	1	4	0	Bank 1 29-00 (61-00)	22D	–	–	4	B
Bank 1 30-00 (62-00)	4	0/1**	0	9	Bank 1 30-09 (62-09)	32D	2	B	4	B
Bank 1 30-00 (62-00)	1	0/1**	F	9	Bank 1 31-39 (63-39)	223	–	–	4	C

* "–" means that the value does not change after execution of the instruction.
** "0/1" means that either "0" or "1" may be selected.

■ BRANCH

ROM is accessed according to the program counter sequence and the program is executed. In order to jump to any address out of the sequence, there are four ways. They are explained in the following paragraphs.

• BR

By BR instruction, the program branches to an address in the current page.

The lower 6 bits of ROM Object Code (operand a, O_6 to O_1) are transferred to the address part of the program counter. This instruction is a conditional instruction and executed only when the Status F/F is "1". If it is "0", the instruction is skipped and the Status F/F becomes "1". The operation is shown in Figure 6.

• LPU

By LPU instruction, the jump of the bank and page is performed.

The lower 5 bits of the ROM Object Code (operand u, O_5 to O_1) are transferred to the page part of the program counter with a delay of 1-cycle time. At the same time, the signal $\overline{R_{70}}$ (the reversed-phase signal of the Data I/O Register R_{70}) is transferred to the bank part of the program counter with a delay of 1-cycle time. The operation is shown in Figure 7.

Consequently, the bank and page will remain unchanged in the cycle immediately following this instruction. In the next cycle, a jump of the bank and page is achieved.

This instruction (LPU) is conditional, and is executed only when the Status F/F is "1". Even after a skip, the Status F/F will remain unchanged ("0").

LPU instruction is used in combination with BR instruction or CAL instruction as the macro instruction of BRL or CALL instruction.

• BRL

By BRL instruction, the program branches to an address in any bank and page.

This instruction is a macro instruction of LPU and BR instructions, which is divided into two instructions as follows.

BRL a-b → LPU a
BR b

< Jump to Bank "$\overline{R_{70}}$", a Page – b Address >

BRL instruction is a conditional instruction because of characteristics of LPU and BR instructions, and is executed only when the Status F/F is "1". If the Status F/F is "0", the instruction is skipped and the Status F/F becomes "1". The examples of BRL instruction are shown in Figure 8.

• TBR (Table Branch)

By TBR instruction, the program branches by the table.

The program counter is modified with the accumulator, the B register, the Carry F/F and the operand p.

The method for modification is shown in Figure 9.

The bank part is determined by the logical equation: $PC_{11} + p_2$, as shown in Table 4.

If the address where TBR instruction exists is in the Bank 1, it is possible to jump to an address only in the Bank 1, not to an address in the Bank 0.

If the address where TBR instruction exists is in the Bank 0, it is possible to jump to an address in either the Bank 1 or the Bank 0 depending on the value of the operand p_2.

TBR instruction is executed regardless of the Status F/F, and does not affect the Status F/F.

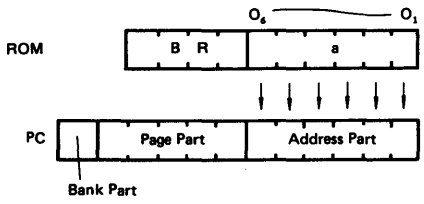


Figure 6 BR Operation

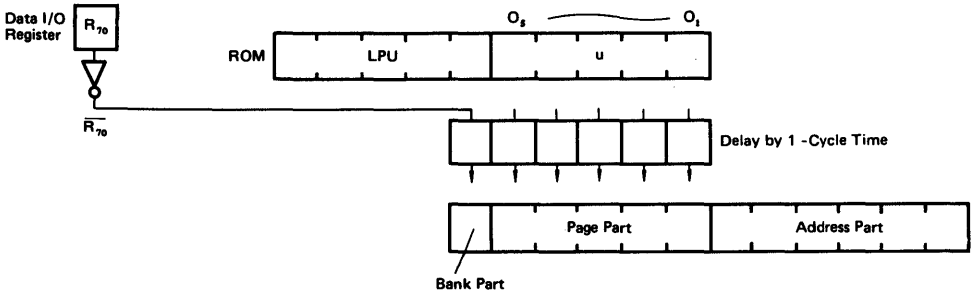


Figure 7 LPU Operation

```
Branch to Bank 0
·  LAI   15
   LRA   7      R70 = "1" (R̄70 = "0")
   LPU   5   }  BRL 5-3F
   BR    3F  }  (Branch to Bank 0 5-3F (5-3F))
·  LAI   15
   LBA
   LRA   7      R70 = "1" (R̄70 = "0")
   COMB
   LPU   31  }
   BR    3F  }  BRL 31-3F
                (Branch to Bank 0 31-3F (31-3F))
Branch to Bank 1
·  LAI   0
   LRA   7      R70 = "0" (R̄70 = "1")
   LPU   15  }
   BR    3F  }  BRL 15-3F
                (Branch to Bank 1 15-3F (47-3F))
·  LAI   0
   LTA
   LRA   7      R70 = "0" (R̄70 = "1")
   LYI   3
   XMA
   LPU   10  }
   BR    2E  }  BRL 10-2E
                (Branch to Bank 1 10-2E (42-2E))
```

Figure 8 BRL Example

Table 4 Bank Part Truth Table of TBR Instruction

PC_{11}	P_2	Bank Part of PC after TBR
1 (Bank 1)	1	1 (Bank 1)
	0	1 (Bank 1)
0 (Bank 0)	1	1 (Bank 1)
	0	0 (Bank 0)

■ SUBROUTINE JUMP

There are two types of subroutine jumps. They are explained in the following paragraphs.

• CAL

By CAL instruction, subroutine jump to the Subroutine Space is performed.

The Subroutine Space is the Bank 0 0 Page (0 Page).

The address next to CAL instruction address is pushed onto the stack ST1 and the contents of the stacks ST1, ST2 and ST3 are pushed onto the stacks ST2, ST3 and ST4 respectively as shown in Figure 10.

The bank part of the program counter becomes the Bank 0 and the page part becomes the 0 Page. The lower 6 bits (operand a, O_6 to O_1) of the ROM Object Code is transferred to the address part of the program counter.

The HMCS46C has 4 levels of stack (ST1, ST2, ST3 and ST4) which allows the programmer to use up to 4 levels of subroutine jumps (including interrupts).

CAL is a conditional instruction and executed only when the Status F/F is "1". If the Status F/F is "0", it is skipped and the Status F/F changes to "1".

• CALL

By CALL instruction, subroutine jump to an address in any bank and page is performed.

Subroutine jump to any address can be implemented by the subroutine jump to the page specified by LPU instruction in the bank designated by the reversed-phase signal $\overline{R_{70}}$ of the Data I/O Register R_{70}.

This instruction is a macro instruction of LPU and CAL instructions, which is divided into two instructions as follows.

```
CALL    a-b ──────► LPU  a
                    CAL  b
```

< Subroutine Jump to Bank "$\overline{R_{70}}$", a Page – b Address >

CALL instruction is conditional because of characteristics of LPU and CAL instructions, and is executed when the Status F/F is "1" If the Status F/F is "0", the instruction is skipped and the Status F/F changes to "1". The examples of CALL instruction are shown in Figure 11.

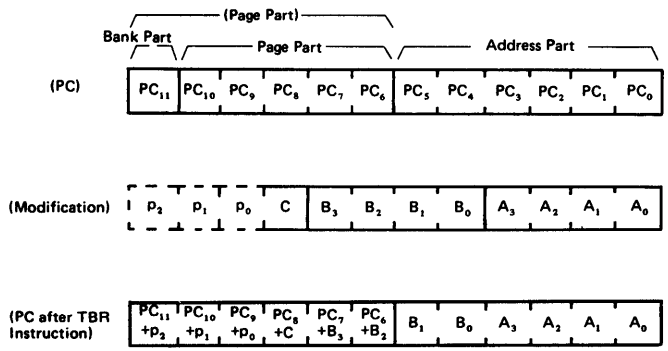


Figure 9 Modification of Program Counter by TBR Instruction

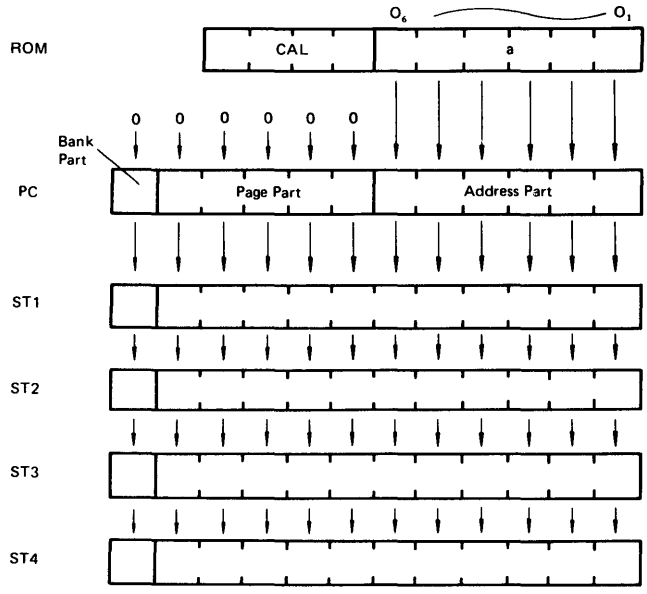


Figure 10 Subroutine Jump Stacking Order

```
Subroutine Jump to Bank 0
·  LAI   15
   LRA   7          R70 = "1" (R̄70 = "0")
   LPU   5
   CAL   3F         CALL 5-3F
                    (Subroutine Jump to Bank 0 5-3F (5-3F))

·  LAI   15
   LBA
   LRA   7          R70 = "1" (R̄70 = "0")
   COMB
   LPU   31
   CAL   3F         CALL 31-3F
                    (Subroutine Jump to Bank 0 31-3F (31-3F))
Subroutine Jump to Bank 1
·  LAI   0
   LRA   7          R70 = "0" (R̄70 = "1")
   LPU   15
   CAL   3F         CALL 15-3F
                    (Subroutine Jump to Bank 1 15-3F (47-3F))

·  LAI   0
   LTA
   LRA   7          R70 = "0" (R̄70 = "1")
   LYI   3
   XMA
   LPU   10
   CAL   2E         CALL 10-2E
                    (Subroutine Jump to Bank 1 10-2E (42-2E)
```

Figure 11 CALL Example

■ RAM

RAM is a memory used for storing data and saving the contents of the registers. Its capacity is 256 digits (1,024 bits) where one digit consists of 4 bits.

Addressing of RAM is performed by a matrix of the file No. and the digit No.

The file No. is set in the X register and the digit No. in the Y register for reading, writing or testing. Specific digits in RAM can be addressed not via the X register and Y register. These digits are called "Memory Register (MR)", 0 to 15 (16 digits in all). The memory register can be exchanged with the accumulator by XAMR instruction.

The RAM address space is shown in Figure 12.

In an instruction in which reading from RAM and writing to RAM coexist (exchange between RAM and the register), reading precedes writing and the write data does not affect the read data.

The RAM bit manipulation instruction enables any addressed RAM bit to be set, reset or tested. The bit assignment is specified by the operand n of the instruction.

The bit test makes the Status F/F "1" when the assigned bit is "1" and makes it "0" when the assigned bit is "0".

Correspondence between the RAM bit and the operand n is shown in Figure 13.

X \ Y	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
f d	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0															
1	1															
2	2															
3	3															
4	4															
5	5															
6	6															
7	7															
8	8															
9	9															
10	10															
11	11															
12	12															
13	13															
14	14															
15	15	MR15	MR14	MR13	MR12	MR11	MR10	MR9	MR8	MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0

Y register Digit No.

X register File No.

Figure 12 RAM Address Space

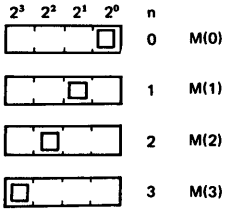


Figure 13 RAM Bit and Operand n

■ REGISTER

The HMCS46C has eight 4-bit registers and two 1-bit registers available to the programmer. The 1-bit registers are the Carry F/F and the Status F/F. They are explained in the following paragraphs.

- **Status F/F (S)**

The Status F/F latches the result of logical or arithmetic operations (Not Zero, Overflow) and bit test operations. The Status F/F affects conditional instructions (LPU, BR and CAL instructions). These instructions are executed only when the Status F/F is "1". If it is "0", these instructions are skipped and the Status F/F becomes "1".

- **Accumulator (A; A Register) and Carry F/F (C)**

The result of the Arithmetic Logic Unit (ALU) operation (4 bits) and the overflow of the ALU are loaded into the accumulator and the Carry F/F. The Carry F/F can be set, reset or tested. Combination of the accumulator and the Carry F/F can be right or left rotated. The accumulator is the main register for ALU operation and the Carry F/F is used to store the overflow generated by ALU operation when the calculation of two or more digits (4 bits/digit) is performed.

- **B Register (B)**

The result of ALU operation (4 bits) is loaded into this register. The B register is used as a sub-accumulator to stack data temporarily and also used as a counter.

- **X Register (X)**

The result of ALU operation (4 bits) is loaded into this register. The X register has exchangeability for the SPX register. The X register addresses the RAM file.

- **SPX Register (SPX)**

The SPX register has exchangeability for the X register.

The SPX register is used to stack the X register and expand the addressing system of RAM in combination with the X register.

- **Y Register (Y)**

The result of ALU operation (4 bits) is loaded into this register. The Y register has exchangeability for the SPY register. The Y register can calculate itself simultaneously with transferring data by the bus lines, which is usable for the calculation of two or more digits (4 bits/digit). The Y register addresses the RAM digit and 1-bit Discrete I/O.

- **SPY Register (SPY)**

The SPY register has exchangeability for the Y register. The SPY register is used to stack the Y register and expand the addressing system of RAM and 1-bit Discrete I/O in combination with the Y register.

The Data I/O Registers R4 and R5, which are not connected to the LSI pin, can be used for general purpose registers.

- **R4 Register (R4)**

The contents of the accumulator and the B register are transferred by LRA and LRB instructions, respectively. The contents of the R4 register are sent to the accumulator and the B register by LAR and LBR instructions, respectively.

- **R5 Register (R5)**

The contents of the accumulator and the B register are transferred by LRA and LRB instructions, respectively. The contents of the R5 register are sent to the accumulator and the B register, respectively.

■ INPUT/OUTPUT

- **4-bit Data Input/Output Common Channel (R)**

The HMCS46C has four 4-bit Data I/O Common Channels (R0, R1, R2 and R3).

The 4-bit registers (Data I/O Register) are attached to these channels.

Each channel is directly addressed by the operand p of input/output instruction.

The data is transferred from the accumulator and the B register to the Data I/O Registers R0 to R3 via the bus lines. Pattern instruction enables the patterns of ROM to be loaded into the Data I/O Registers R2 and R3.

Input instruction enables the 4-bit data to be sent to the accumulator and the B register from R0 to R3. Note that, since the Data I/O Register's output is directly connected to the pin even during execution of input instruction, the input data is wired logic of the Data I/O Register's output and the pin input. Therefore, the Data I/O Register should be set to 15 (all bits of the Data I/O Register is "1") not to affect the pin input before execution of input instruction, and Open Drain or With Pull up MOS should be specified for the I/O configuration of these pins.

The block diagram is shown in Figure 14. The I/O timing is shown in Figure 15.

- **1-bit Discrete Input/Output Common Terminal (D)**

The HMCS46C has 16 1-bit Discrete I/O Common Terminals.

The 1-bit Discrete I/O Common Terminal consists of a 1-bit latch and an I/O common pin.

The 1-bit Discrete I/O is addressed by the Y register. The addressed latch can be set or reset by output instruction and "0" and "1" level can be tested with the addressed pin by input instruction.

Note that, since the latch output is directly connected to the pin even during execution of input instruction, the input data is wired logic of the latch's output and the pin input. Therefore, the latch should be set to "1" not to affect the pin input before execution of input instruction and Open Drain or With Pull up MOS should be specified for the I/O configuration of this pin.

The D_0 to D_3 terminal are also addressed directly by the operand n of input/output instruction and can be set or reset. The block diagram is shown in Figure 16 and the I/O timing is shown in Figure 17.

- **I/O Configuration**

The I/O configuration of each pin can be specified among Open Drain, With Pull up MOS and CMOS using a mask option as shown in Figure 18.

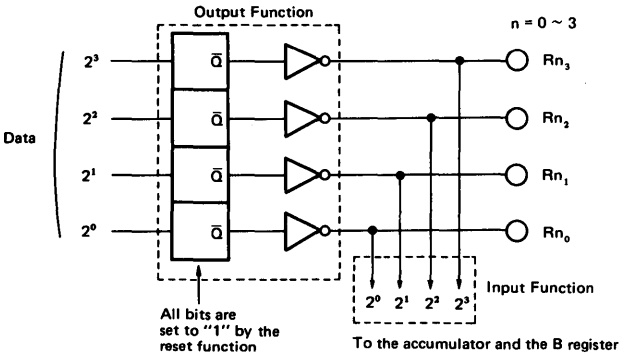


Figure 14 4-bit Data I/O Block Diagram

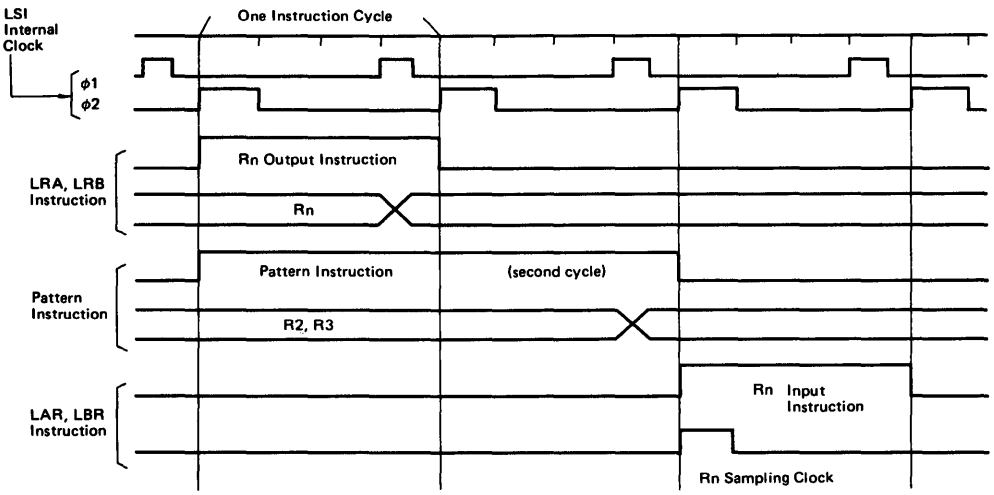


Figure 15 4-bit Data I/O Timing

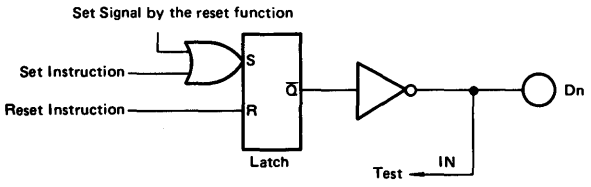


Figure 16 1-bit Discrete I/O Block Diagram

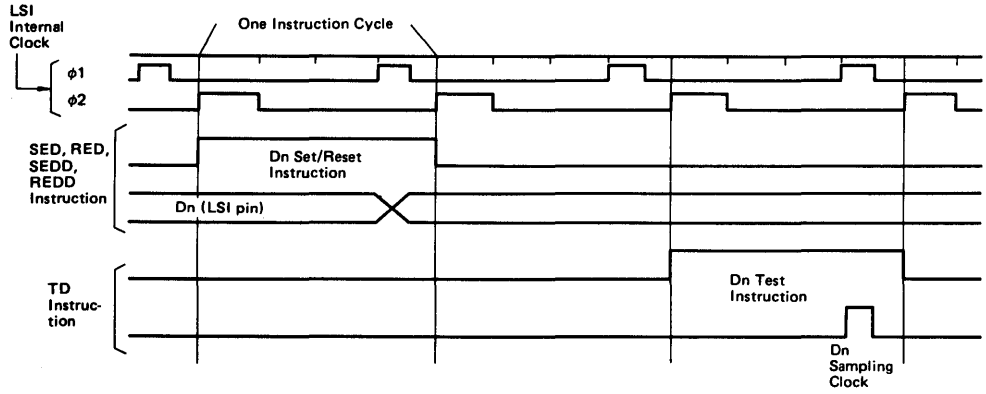
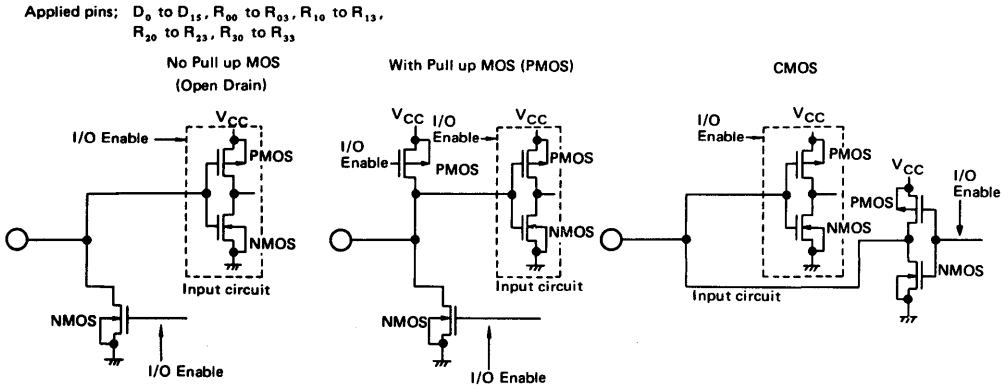


Figure 17 1-bit Discrete I/O Timing



* When "Disable" is specified for the I/O State at the Halt State, the I/O Enable signal shown in the figure turns off the input circuit, Pull up MOS, and NMOS output and sets CMOS output to high impedance (PMOS, NMOS; OFF).

Figure 18 I/O Configuration

■ TIMER/COUNTER

The timer/counter consists of the 4-bit counter and the 6-bit prescaler as shown in Figure 19. The 4-bit counter may be loaded under program control and is incremented toward 15 by the prescaler overflow output pulse or the input pulse of INT_1 pin (its leading edge is counted). The clock input to the counter is selected by the CF F/F. When the CF F/F is "0", the clock input is the prescaler overflow output pulse (Timer Mode). When the CF F/F is "1", the clock input is the input pulse of INT_1 pin (Counter Mode). When the counter reaches zero (returns from 15 to zero), the overflow output pulse is generated and the counter continues to count ($14 \rightarrow 15 \rightarrow 0 \rightarrow 1 \rightarrow 2 \cdots$).

The TF F/F is a flip-flop which masks interrupts from the timer/counter. It can be set and reset by interrupt instruction. If the overflow output pulse of the counter is generated when the TF F/F is reset ("0"), an interrupt request occurs and the TF F/F becomes "1". If the overflow output pulse is generated when the TF F/F is set ("1"), no interrupt request occurs. The TTF instruction enables the TF F/F to be tested.

The prescaler is a 6-bit frequency divider. It divides a system clock (instruction frequency) by 64 into the overflow output pulses of "instruction frequency ÷ 64".

The prescaler is cleared when data is loaded into the counter (by LTA or LTI instruction). The frequency division is 0 when the prescaler is cleared. At the 64th clock, an overflow output

pulse is generated from the prescaler. During operation of the LSI, the prescaler is operating and cannot be stopped. (In the Halt state, it stops.) The relation between the specified value of the counter and specified time in the Timer Mode is shown in Table 5.

The pulse width of the INT_1 pin in the Counter Mode must be at least 2-cycle time for both "High" and "Low" levels as shown in Figure 19.

■ INTERRUPT

The HMCS46C can be interrupted in two different ways: through the external interrupt input pins (INT_0, INT_1) and the timer/counter interrupt request. When any interrupt occurs, processing is suspended, the Status F/F is unchanged, the present program counter is pushed onto the stack ST1 and the contents of the stacks ST1, ST2 and ST3 are pushed onto the stacks ST2, ST3 and ST4 respectively. At that time, the Interrupt Enable F/F (I/E) is set and the address jumps to a fixed destination (Interrupt Address), and then the interrupt routine is executed. Stacking the registers other than the program counter must be performed by the program. The interrupt routine must end with RTNI (Return Interrupt) instruction which sets the I/E F/F simultaneously with the RTN instruction.

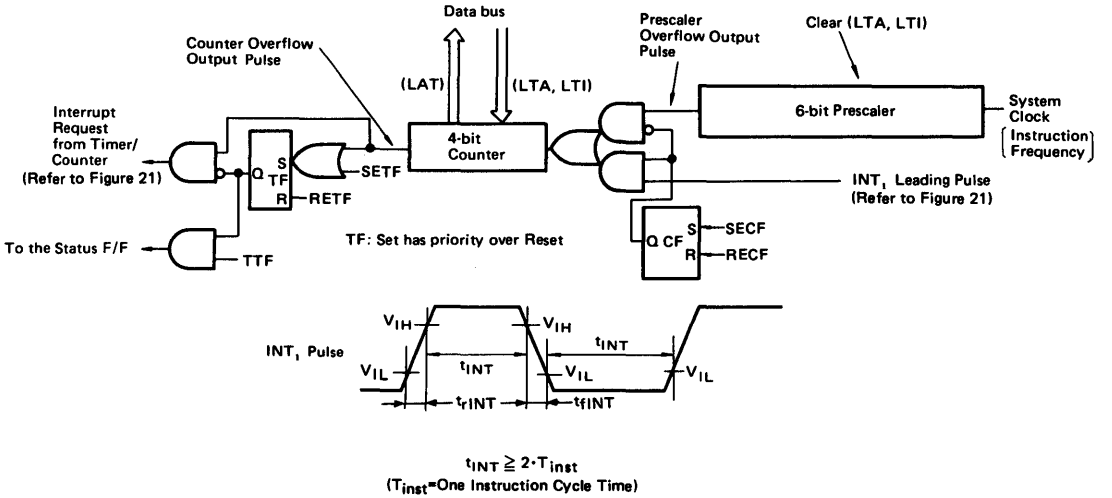
The Interrupt Address:

Input Interrupt Address ..... Bank 0 1 Page 3F Address (1 Page 3F Address)

Timer/Counter Interrupt Address ··· Bank 0 0 Page 3F Address (0 Page 3F Address)

The input interrupt has priority over the timer/counter interrupt.

The INT_0 and INT_1 pin have an interrupt request function. Each terminal consists of a circuit which generates leading pulse and the Interrupt mask F/F (IF0, IF1). An interrupt is enabled (unmasked) when the IF0 F/F or IF1 F/F is reset. When the INT_0 or INT_1 pin changes from "0" to "1" (from "Low" level to "High" level), a leading pulse is generated to produce an interrupt request. At the same time, the IF0 F/F or IF1 F/F is set. When the IF0 F/F or IF1 F/F is set, the interrupt masking for the pin will result. (If a leading pulse is generated, no interrupt request occurs.)



$t_{INT} \geqq 2 \cdot T_{inst}$

(T_{inst}=One Instruction Cycle Time)

Figure 19 Timer/Counter Block Diagram

Table 5 Timer Range

Specified Value	Number of Cycles	*Time (ms)	Specified Value	Number of Cycles	*Time (ms)
0	1024	5.12	8	512	2.56
1	960	4.80	9	448	2.24
2	896	4.48	10	384	1.92
3	832	4.16	11	320	1.60
4	768	3.84	12	256	1.28
5	704	3.52	13	192	0.96
6	640	3.20	14	128	0.64
7	576	2.88	15	64	0.32

* Time is based on instruction frequency 200kHz. (One Instruction Cycle Time (T_{inst}) = 5μs)

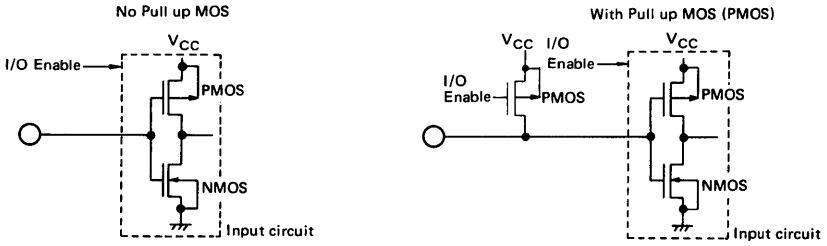
An interrupt request generated by the leading pulse is latched into the input interrupt request F/F (I/RI) on the input side. If the Interrupt Enable F/F (I/E) is "1" (Interrupt Enable State), an interrupt occurs immediately and the I/RI F/F and the I/E F/F are reset. If the I/E F/F is "0" (Interrupt Disable State), the I/RI F/F is held at "1" until the HMCS46C gets into the Interrupt Enable State.

The IF0 F/F, the IF1 F/F, the INT_0 pin and the INT_1 pin can be tested by interrupt instruction. Therefore, the INT_0 and the INT_1 can be used as additional input pins with latches.

The INT_0 pin and INT_1 pin can be provided with Pull up MOS using a mask option as shown in Figure 20.

An interrupt request from the timer/counter is latched into the timer interrupt request F/F (I/RT). The succeeding operations are the same as an interrupt from the input. Only the exception is that, since an interrupt from the input precedes a timer/counter interrupt, the input interrupt occurs if both the I/RI F/F and the I/RT F/F are "1" (when the input interrupt and the timer/counter interrupts are generated simultaneously). During this processing, the I/RT F/F remains "1". The timer/counter interrupt can be implemented after the input interrupt processing is achieved.

The interrupt circuit block diagram is shown in Figure 21.



* When "Disable" is specified for the I/O State at the Halt State, the I/O Enable signal shown in the figure turns off the input circuit and Pull up MOS.

Figure 20 Configuration of INT_0 and INT_1

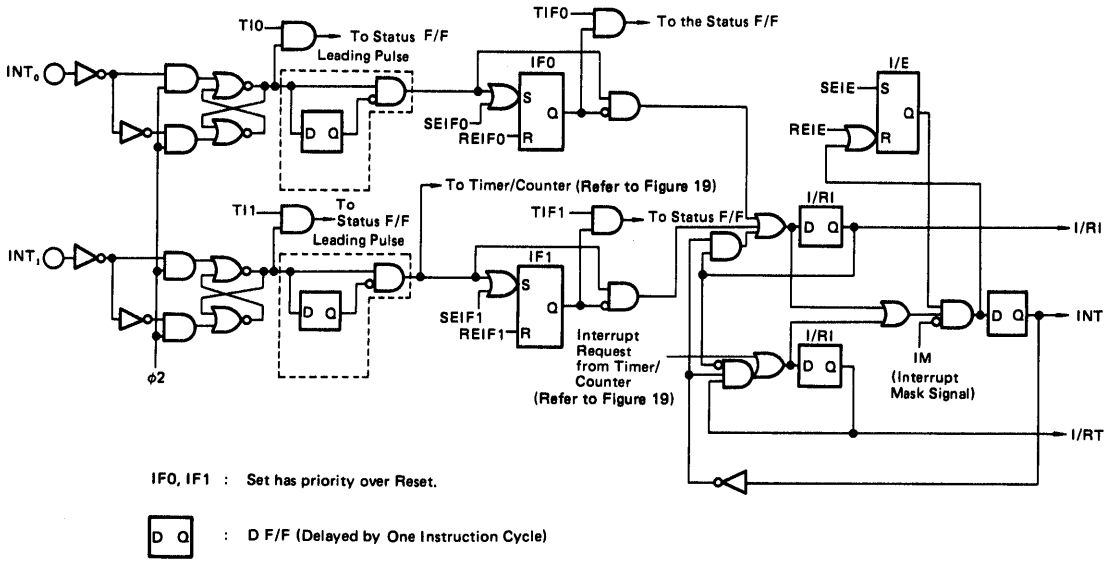


Figure 21 Interrupt Circuit Block Diagram

■ RESET FUNCTION

The reset is performed by setting the RESET pin to "1" ("High" level) and the HMCS46C gets into operation by setting it to "0" ("Low" level); Refer to Figure 22. Moreover, the HMCS46C has the power-on reset function (ACL; Built-in Reset Circuit). The Built-in Reset Circuit restricts the rise condition of the power supply; Refer to Figure 23. When the Built-in Reset Circuit is used, RESET should be connected to GND.

HMCS46CL doesn't have the power-on reset function.

Internal state of the HMCS46C are specified as follows by the reset function.

- Program Counter (PC) is set to Bank 1 31 Page 3F Address (63 Page 3F Address).
- Data I/O Registers R_{70} is set to "1" (Jumps to Bank 0 by execution of LPU instruction after the reset).
- I/RI, I/RT, I/E and CF are reset to "0".
- IF0, IF1, and TF are set to "1".
- Data I/O Registers (R0 to R5) and Discrete I/O Latches (D_0 to D_{15}) are all set to "1".

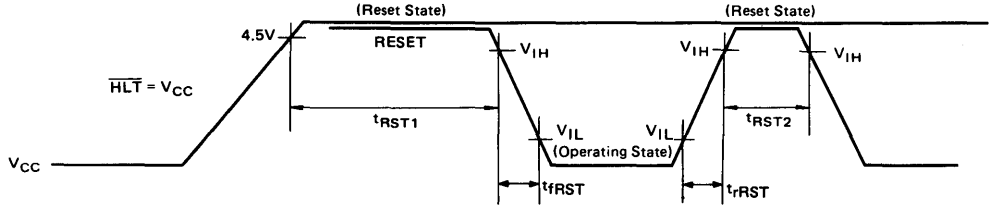
Note that all the other logic blocks (the Stack Registers, the Status F/F, the accumulator, the Carry F/F, the registers, the Timer/Counter, RAM) are not cleared by the reset function. The user should initialize these blocks by software. Because the Status F/F after the reset is not defined, set the Status F/F to "0" or "1" before the first execution of the conditional instructions (LPU, CAL and BR instructions).

■ HALT FUNCTION

When the $\overline{HLT}$ pin is set to "0" ("Low" level), the internal clock stops and all the internal statuses (RAM, the Registers, the Carry F/F, the Status F/F, the Program Counter, and all the internal statuses) are held. Because all internal logic operation stop, power consumption is reduced. There are two input/output statuses in the Halt State. The user should specify either "Enable" or "Disable" using a mask option at the time of ordering ROM.

"Enable"
- Output ..... The status before the Halt State is held
- Pull up MOS ... ON
- Input ..... Independent of the Halt State or Operating State (Input Circuit is ON)

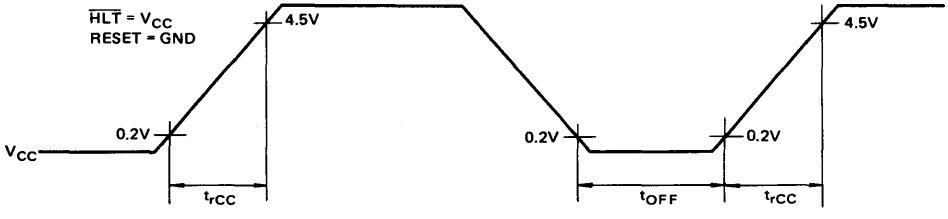
Since Pull up MOS is ON, Pull up MOS current flows with output "0" ("Low" level) in the Halt State (NMOS; ON). When an input signal changes, transition current flows into an input circuit. Also, current flows into Pull up MOS.



* t_{RST1} includes the time required from the power ON until the operation gets into the constant state.

** t_{RST2} is applied when the operation is in the constant state.

Figure 22 RESET Timing



* t_{OFF} specifies the period when the power supply if OFF in the case that a short break of the power supply occurs and the power supply ON/OFF is repeated.

Figure 23 Power Supply Timing for Built-in Reset Circuit

These currents and added to the Stand-by Supply Current (or Halt Current).

"Disable"
- Output ..... NMOS Output: OFF
  CMOS Output: High Impedance (NMOS, PMOS: OFF)
- Pull up MOS ... OFF
- Input ..... Input Circuit: OFF

Both input and output are at high impedance state. Since an input circuit is OFF, any current other than the Stand-by Supply Current (or Halt Current) does not flow even if an input signal changes.

When the $\overline{HLT}$ pin is set to "1" ("High" level), the HMCS46C gets into operation from the status just before the Halt State.

The halt timing is shown in Figure 24.

CAUTION

If, during the Halt State, the external reset input is applied (RESET = "1" ("High" level)), the internal status is not held.

■ OSCILLATOR

The HMCS46C contains its own oscillator and frequency divider (CPG). The user can obtain the desired timing for operation of the LSI by merely connecting an resistor R_f or ceramic filter circuit (Internal Clock Operation). Also an external oscillator can supply a clock (External Clock Operation).

The OSC_1 clock frequency is internally divided by four to produce the internal system clocks.

The user may exchange the external parts for the same LSI to select either of these two operational modes as shown in Figure 25. There is no need of specifying it by using the mask option.

The typical value of clock oscillation frequency (f_{osc}) varies with a oscillation resistor R_f as shown in Figure 26.

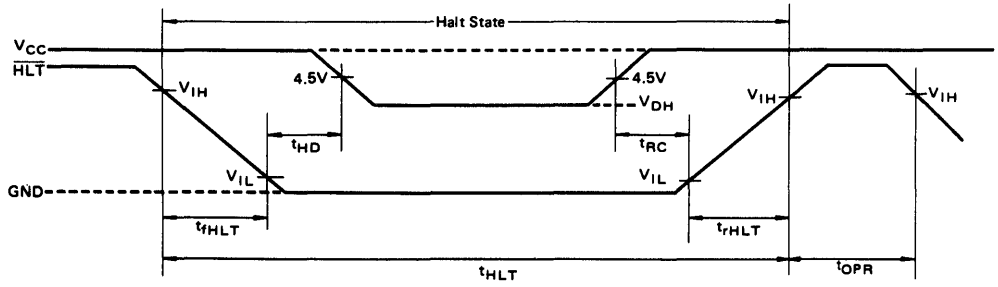
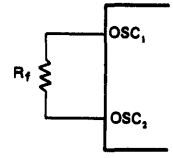


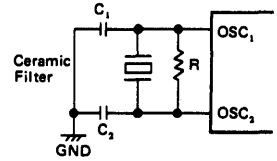
Figure 24 Halt Timing

(a) Internal Clock Operation Using Resistor R_f



Wiring of OSC_1 and OSC_2 terminals should be as short as possible because the oscillation frequency is modified by capacitance of these terminals.

(b) Internal Clock Operation Using Ceramic Filter Circuit (This is not applied to HMCS46CL.)



Ceramic Filter; CSB800A (MURATA)
R_1 ; 1MΩ ± 10%
C_1 ; 100pF ± 10% (Ceramic Capacitor)
C_2 ; 100pF ± 10% (Ceramic Capacitor)

The ceramic filter oscillation does not apply when using "Halt" and not resetting at the time of "Halt" cancellation.
This circuit is the example of the typical use. As the oscillation characteristics is not guaranteed, please consider and examine the circuit constants carefully on your application.

Figure 25 Clock Operation Modes (to be continued)

(c) External Clock Operation

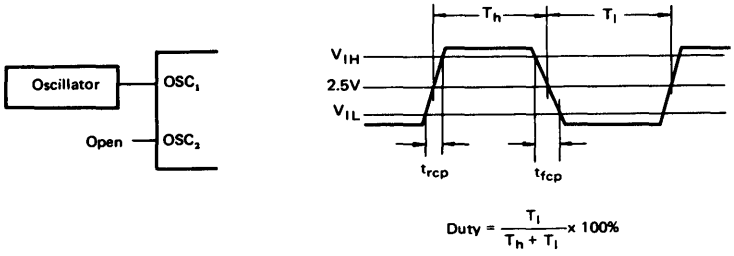


Figure 25 Clock Operation Modes

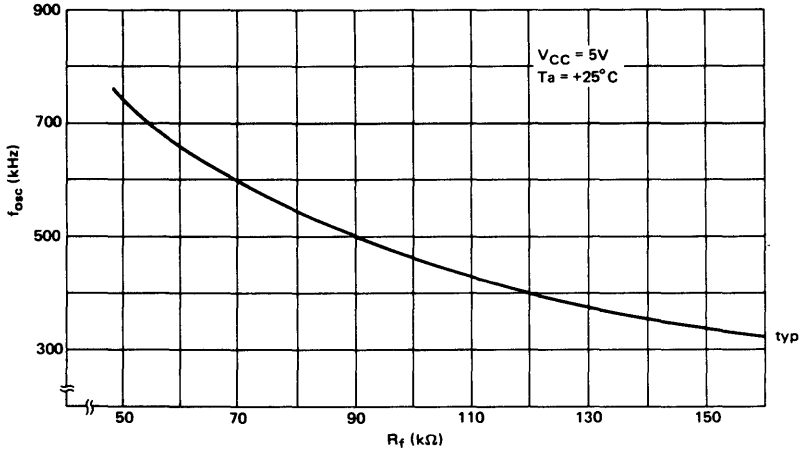


Figure 26 Typical Value of Oscillation Frequency vs. R_f

■ INSTRUCTION LIST

The instructions of the HMCS46C are listed according to their functions, as shown in Table 6.

Table 6 Instruction List

Group	Mnemonic	Function	Status
Register · Register Instruction	LAB	B → A	
	LBA	A → B	
	LAY	Y → A	
	LASPX	SPX → A	
	LASPY	SPY → A	
	XAMR m	A ↔ MR (m)	
RAM Address Register Instruction	LXA	A → X	
	LYA	A → Y	
	LXI i	i → X	
	LYI i	i → Y	
	IY	Y+1 → Y	NZ
	DY	Y−1 → Y	NB
	AYY	Y+A → Y	C
	SYY	Y−A → Y	NB
	XSPX	X ↔ SPX	
	XSPY	Y ↔ SPY	
	XSPXY	X ↔ SPX, Y ↔ SPY	
RAM · Register Instruction	LAM (XY)	M → A (XY ↔ SPXY)	
	LBM (XY)	M → B (XY ↔ SPXY)	
	XMA (XY)	M ↔ A (XY ↔ SPXY)	
	XMB (XY)	M ↔ B (XY ↔ SPXY)	
	LMAIY (X)	A → M, Y+1 → Y (X ↔ SPX)	NZ
	LMADY (X)	A → M, Y−1 → Y (X ↔ SPX)	NB
Immediate Transfer Instruction	LMIIY i	i → M, Y+1 → Y	NZ
	LAI i	i → A	
	LBI i	i → B	
Arithmetic Instruction	AI i	A+i → A	C
	IB	B+1 → B	NZ
	DB	B−1 → B	NB
	AMC	M+A+C (F/F) → A	C
	SMC	M−A−$\bar{C}$ (F/F) → A	NB
	AM	M+A → A	C
	DAA	Decimal Adjustment (Addition)	
	DAS	Decimal Adjustment (Subtraction)	
	NEGA	$\bar{A}$+1 → A	
	COMB	$\bar{B}$ → B	
	SEC	"1" → C (F/F)	
	REC	"0" → C (F/F)	
	TC	Test C (F/F)	C (F/F)
	ROTL	Rotation Left	
	ROTR	Rotation Right	
	OR	A ∪ B → A	

(to be continued)

Group	Mnemonic	Function	Status
Compare Instruction	MNEI i	M ≠ i	NZ
	YNEI i	Y ≠ i	NZ
	ANEM	A ≠ M	NZ
	BNEM	B ≠ M	NZ
	ALEI i	A ≧ i	NB
	ALEM	A ≧ M	NB
	BLEM	B ≧ M	NB
RAM Bit Manipulation Instruction	SEM n	"1" → M (n)	
	REM n	"0" → M (n)	
	TM n	Test M (n)	M(n)
ROM Address Instruction	BR a	Branch on Status 1	1
	CAL a	Subroutine Jump on Status 1	1
	LPU u	Load Program Counter Upper on Status 1	
	TBR p	Table Branch	
	RTN	Return from Subroutine	
Interrupt Instruction	SEIE	"1" → I/E	
	SEIF0	"1" → IF0	
	SEIF1	"1" → IF1	
	SETF	"1" → TF	
	SECF	"1" → CF	
	REIE	"0" → I/E	
	REIF0	"0" → IF0	
	REIF1	"0" → IF1	
	RETF	"0" → TF	
	RECF	"0" → CF	
	TI0	Test INT_0	INT_0
	TI1	Test INT_1	INT_1
	TIF0	Test IF0	IF0
	TIF1	Test IF1	IF1
	TTF	Test TF	TF
	LTI i	i → Timer/Counter	
	LTA	A → Timer/Counter	
	LAT	Timer/Counter → A	
	RTNI	Return Interrupt	
Input/Output Instruction	SED	"1" → D (Y)	
	RED	"0" → D (Y)	
	TD	Test D (Y)	D(Y)
	SEDD n	"1" → D (n)	
	REDD n	"0" → D (n)	
	LAR p	R(p) → A	
	LBR p	R(p) → B	
	LRA p	A → R (p)	
	LRB p	B → R (p)	
	P p	Pattern Generation	
	NOP	No Operation	

[NOTE] 1. (XY) after a mnemonic code has four meanings as follows.

Mnemonic only	Instruction execution only
Mnemonic with X	After instruction execution, X ↔ SPX
Mnemonic with Y	After instruction execution, Y ↔ SPY
Mnemonic with XY	After instruction execution, X ↔ SPX, Y ↔ SPY

[Example]

LAM	M → A
LAMX	M → A, X ↔ SPX
LAMY	M → A, Y ↔ SPY
LAMXY	M → A, X ↔ SPX, Y ↔ SPY

2. Status column shows the factor which brings the Status F/F "1" under judgement instruction or instruction accompanying the judgement.
   - NZ .... ALU Not Zero
   - C ..... ALU Overflow in Addition, that is, Carry
   - NB .... ALU Overflow in Subtraction, that is, No Borrow
   - Except above ..... Contents of the status column affects the Status F/F directly.

3. The Carry F/F (C(F/F)) is not always affected by executing the instruction which affects the Status F/F. Instructions which affect the Carry F/F are eight as follows.

AMC	SEC
SMC	REC
DAA	ROTL
DAS	ROTR

4. All instructions except the pattern instruction (P) are executed in 1-cycle. The pattern instruction (P) is executed in 2-cycye.

HMCS46C Mask Option List

Date	
Customer's Name	
ROM CODE ID	
Hitachi P/N	

(1) I/O Option

Pin Name	I/O	I/O Option			Remarks	Pin Name	I/O	I/O Option			Remarks
		A	B	C				A	B	C	
D_0	I/O					R_{00}	I/O				
D_1	I/O					R_{01}	I/O				
D_2	I/O					R_{02}	I/O				
D_3	I/O					R_{03}	I/O				
D_4	I/O					R_{10}	I/O				
D_5	I/O					R_{11}	I/O				
D_6	I/O					R_{12}	I/O				
D_7	I/O					R_{13}	I/O				
D_8	I/O					R_{20}	I/O				
D_9	I/O					R_{21}	I/O				
D_{10}	I/O					R_{22}	I/O				
D_{11}	I/O					R_{23}	I/O				
D_{12}	I/O					R_{30}	I/O				
D_{13}	I/O					R_{31}	I/O				
D_{14}	I/O					R_{32}	I/O				
D_{15}	I/O					R_{33}	I/O				
INT_0	I										
INT_1	I										

* Specify the I/O composition with a mark of "○" in the applicable composition column.
A: No pull up MOS B: With pull up MOS C: CMOS Output

(2) Oscillator & Halt

Oscillator \ Halt	Not used	Used (Reset is applied when Halt release)	Used (Reset is not applied when Halt release)
Resistor			
Ceramic Resonator			
External Clock			

* Please check one section on the above chart.

(3) I/O State at "Halt" mode

I/O State
□ Enable
□ Disable

* Mark "√" in "□" for the selected I/O state.

(4) Supply Voltage (V_{CC})

Supply Voltage (V_{CC})
□ 5 ± 0.5V
□ 2.5V to 5.5V

* Mark "√" in "□" for the selected supply voltage.

(5) Package

Package
□ DP-42
□ DP-42S

* Mark "√" in "□" for the selected package.

(6) Evchip used for Program Evaluation

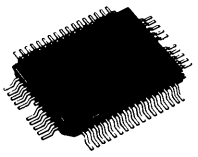
Evchip
□ HD44855E
□ HD44857E

* Mark "√" in "□" for the evchip used for program evaluation.

HMCS47C(HD44860), HMCS47CL(HD44868)

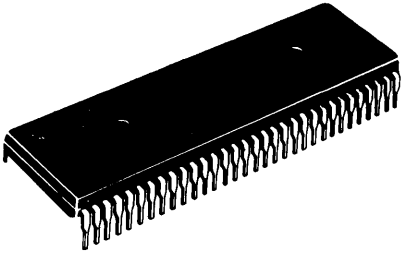
The HMCS47C is the CMOS 4-bit single chip microcomputer which contains ROM, RAM, I/O and Timer/Counter on single chip. The HMCS47C is designed to perform efficient controller function as well as arithmetic function for both binary and BCD data. The CMOS technology of the HMCS47C provides the flexibility of microcomputers for battery powered and battery back-up applications.

HMCS47C, HMCS47CL



(FP-54)

HMCS47C, HMCS47CL

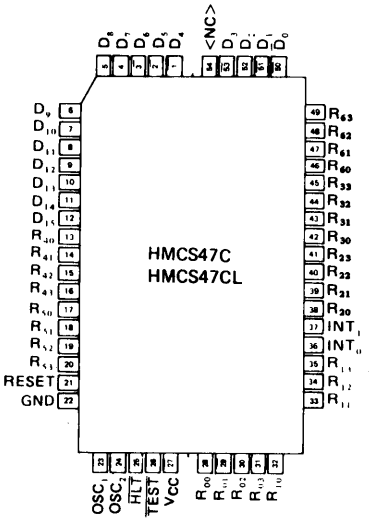


(DP-64S)

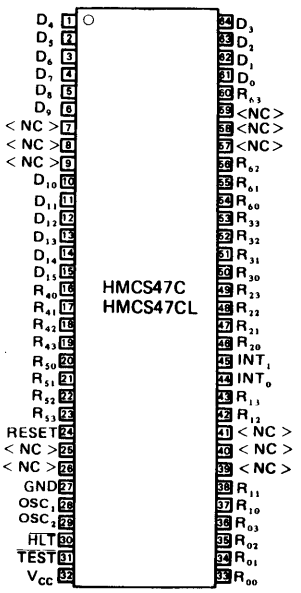
■ FEATURES

- 4-bit Architecture
- 4,096 Words of Program ROM and Pattern ROM (10 bits/Word)
- 256 Digits of Data RAM (4 bits/Digit)
- 44 I/O Lines and 2 External Interrupt Lines
- Timer/Counter
- Instruction Cycle Time;
  HMCS47C : 5 μs
  HMCS47CL : 20 μs
- All Instructions except One Instruction; Single Word and Single Cycle
- BCD Arithmetic Instructions
- Pattern Generation Instruction
  – Table Look Up Capability –
- Powerful Interrupt Function
  3 Interrupt Sources
  ├2 External Interrupt Lines
  └Timer/Counter
  Multiple Interrupt Capability
- Bit Manipulation Instructions for Both RAM and I/O
- Option of I/O Configuration Selectable on Each Pin; With Pull up MOS or CMOS or Open Drain
- Built-in Oscillator
- Built-in Power-on Reset Circuit (HMCS47C only)
- Low Operating Power Dissipation; 3.3mW typ.
- Stand-by Mode (Halt Mode); 66 μW max.
- CMOS Technology
- Single Power Supply;
  HMCS47C : 5V±10%
  HMCS47CL : 2.5V to 5.5V

■ PIN ARRANGEMENT

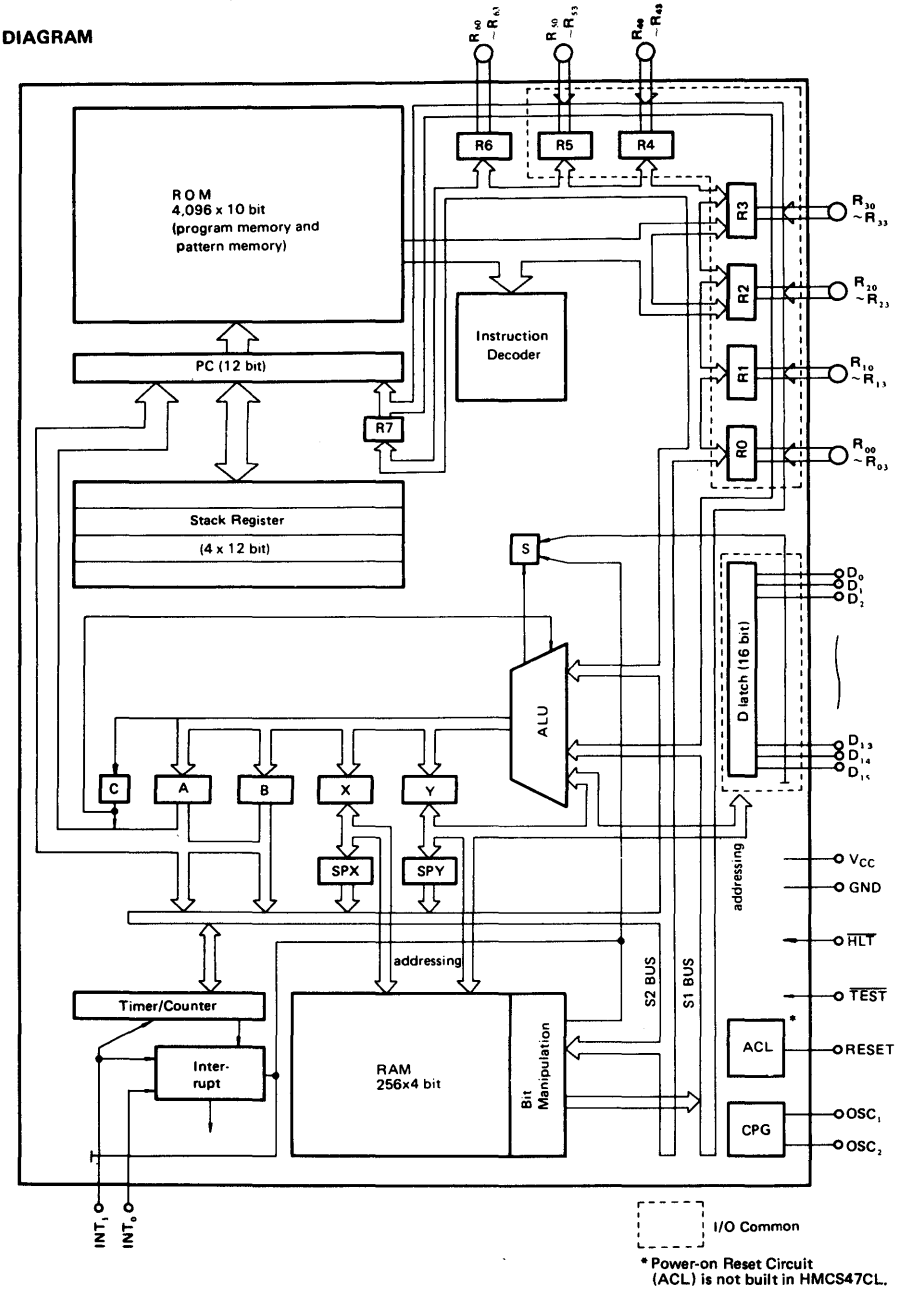


(Top View)



(Top View)

■ BLOCK DIAGRAM



- **HMCS47C ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%)**
- **ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Value	Unit	Remarks
Supply Voltage	V_{CC}	-0.3 to +7.0	V	
Terminal Voltage (1)	V_{T1}	-0.3 to V_{CC} + 0.3	V	Except for the terminals specified by V_{T2}
Terminal Voltage (2)	V_{T2}	-0.3 to +10.0	V	Applied to the Open Drain type of Output pins and Open Drain type of I/O pins.
Maximum Total Output Current (1)	$-\Sigma I_{O1}$	45	mA	[NOTE 3]
Maximum Total Output Current (2)	ΣI_{O2}	45	mA	[NOTE 3]
Operating Temperature	T_{opr}	-20 to +75	°C	
Storage Temperature	T_{stg}	-55 to +125	°C	

[NOTE 1] Permanent LSI damage may occur if "Maximum Ratings" are exceeded. Normal operation should be under the conditions of "ELECTRICAL CHARACTERISTICS -1, -2". If these conditions are exceeded, it could be cause of malfunction of LSI and affects reliability of LSI.

[NOTE 2] All voltages are with respect to GND.

[NOTE 3] The Maximum Total Output Current is total sum of output currents which can flow out (or flow in) from or into the I/O pins and Output pins simultaneously.

• ELECTRICAL CHARACTERISTICS-1 (V_{CC} = 5V ± 10%, Ta = -20°C to +75°C)

Item	Symbol	Test Conditions	Value min.	Value typ.	Value max.	Unit	Note
Input "Low" Voltage	V_{IL}		–	–	1.0	V	
Input "High" Voltage (1)	V_{IH1}		V_{CC} - 1.0	–	V_{CC}	V	2
Input "High" Voltage (2)	V_{IH2}		V_{CC} - 1.0	–	10	V	3
Output "Low" Voltage	V_{OL}	I_{OL} = 1.6mA	–	–	0.8	V	
Output "High" Voltage (1)	V_{OH1}	$-I_{OH}$ = 1.0mA	2.4	–	–	V	4
Output "High" Voltage (2)	V_{OH2}	$-I_{OH}$ = 0.01mA	V_{CC} - 0.3	–	–	V	5
Interrupt Input Hold Time	t_{INT}		$2 \cdot T_{inst}$	–	–	μs	
Interrupt Input Fall Time	t_{fINT}		–	–	50	μs	
Interrupt Input Rise Time	t_{rINT}		–	–	50	μs	
Output "High" Current	I_{OH}	V_{OH} = 10V	–	–	3	μA	6
Input Leakage Current	I_{IL}	V_{in} = 0 to V_{CC}	–	–	1	μA	2
		V_{in} = 0 to 10V	–	–	3		3
Pull up MOS Current	$-I_P$	V_{CC} = 5V	60	–	250	μA	
Supply Current (1)	I_{CC1}	V_{in} = V_{CC}, V_{CC} = 5V, Ceramic Filter Oscillation (f_{osc} = 800kHz)	–	–	2.0	mA	7
Supply Current (2)	I_{CC2}	V_{in} = V_{CC}, V_{CC} = 5V R_f Oscillation (f_{osc} = 800kHz) External Clock Operation (f_{cp} = 800kHz)	–	–	0.85	mA	7
Standby I/O Leakage Current	I_{LS}	$\overline{HLT}$ = 1.0V, V_{in} = 0 to V_{CC}	–	–	1	μA	5, 8
		$\overline{HLT}$ = 1.0V, V_{in} = 0 to 10V	–	–	3	μA	6, 8
Standby Supply Current	I_{CCS}	V_{in} = V_{CC}, $\overline{HLT}$ = 0.2V	–	–	12	μA	9
External Clock Operation							
External Clock Frequency	f_{cp}		350	–	850	kHz	
External Clock Duty	Duty		45	50	55	%	
External Clock Rise Time	t_{rcp}		0	–	0.2	μs	
External Clock Fall Time	t_{fcp}		0	–	0.2	μs	
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{cp}$	4.7	–	11.4	μs	
Internal Clock Operation (R_f Oscillation)							
Clock Oscillation Frequency	f_{osc}	R_f = 51kΩ ± 2%	540	–	900	kHz	
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{osc}$	4.4	–	7.4	μs	
Internal Clock Operation (Ceramic Filter Oscillation)							
Clock Oscillation Frequency	f_{osc}	Ceramic Filter Circuit	784	–	816	kHz	
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{osc}$	4.9	–	5.1	μs	

[NOTE 1] All voltages are with respect to GND.

[NOTE 2] This is applied to RESET, $\overline{HLT}$, OSC_1, INT_0, INT_1 and the With Pull up MOS or CMOS type of I/O pins.

[NOTE 3] This is applied to the Open Drain type of I/O pins.

[NOTE 4] This is applied to the CMOS type of I/O or Output pins.

[NOTE 5] This is applied to the With Pull up MOS or CMOS type of I/O or Output pins.

[NOTE 6] This is applied to the Open Drain type of I/O or Output pins.

[NOTE 7] I/O current is excluded.

[NOTE 8] The Standby I/O Leakage Current is the I/O leakage current in the Halt and Disable State.

[NOTE 9] I/O current is excluded.
The Standby Supply Current is the supply current at V_{CC}=5V ± 10% in the Halt State. The supply current in the case where the supply voltage falls to the Halt Duration voltage is called the Halt Current (I_{DH}), and it is shown in "ELECTRICAL CHARACTERISTICS -2."

- **ELECTRICAL CHARACTERISTICS-2 (Ta = -20°C to +75°C)**

Reset and Halt

Item	Symbol	Test Conditions	Value min.	Value max.	Unit
Halt Duration Voltage	V_{DH}	$\overline{HLT}$ = 0.2V	2.3	–	V
Halt Current	I_{DH}	$V_{in} = V_{CC}$, $\overline{HLT}$ = 0.2V, V_{DH} = 2.3V	–	1 2	μA
Halt Delay Time	t_{HD}		100	–	μs
Operation Recovery Time	t_{RC}		100	–	μs
$\overline{HLT}$ Fall Time	t_{fHLT}		–	1000	μs
$\overline{HLT}$ Rise Time	t_{rHLT}		–	1000	μs
$\overline{HLT}$ "Low" Hold Time	t_{HLT}		400	–	μs
$\overline{HLT}$ "High" Hold Time	t_{OPR}	R_f Oscillation, External Clock Operation	0.1	–	ms
		Ceramic Filter Oscillation	4	–	
Power Supply Rise Time	t_{rCC}	Built-in Reset, $\overline{HLT}$ = V_{CC}	0.1	10	ms
Power Supply OFF Time	t_{OFF}	Built-in Reset $\overline{HLT}$ = V_{CC}	1	–	ms
RESET Pulse Width (1)	t_{RST1}	External Reset V_{CC} = 4.5 to 5.5V, $\overline{HLT}$ = V_{CC} (R_f Oscillation, External Clock Operation)	1	–	ms
		External Reset V_{CC} = 4.5 to 5.5V, $\overline{HLT}$ = V_{CC} (Ceramic Filter Oscillation)	4	–	
RESET Pulse Width (2)	t_{RST2}	External Reset V_{CC} = 4.5 to 5.5V, $\overline{HLT}$ = V_{CC}	$2 \cdot T_{inst}$	–	μs
RESET Fall Time	t_{fRST}	$\overline{HLT}$ = V_{CC}	–	20	ms
RESET Rise Time	t_{rRST}	$\overline{HLT}$ = V_{CC}	–	20	ms

[NOTE] All voltages are with respect to GND.

- **HMCS47CL ELECTRICAL CHARACTERISTICS (2.5V to 5.5V)**
- **ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Value	Unit	Remarks
Supply Voltage	V_{CC}	-0.3 to +7.0	V	
Terminal Voltage (1)	V_{T1}	-0.3 to V_{CC} + 0.3	V	Except for the terminals specified by V_{T2}
Terminal Voltage (2)	V_{T2}	-0.3 to +10.0	V	Applied to the Open Drain type of Output pins and Open Drain type of I/O pins.
Maximum Total Output Current (1)	$-\Sigma I_{O1}$	45	mA	[NOTE 3]
Maximum Total Output Current (2)	ΣI_{O2}	45	mA	[NOTE 3]
Operating Temperature	T_{opr}	-20 to +75	°C	
Storage Temperature	T_{stg}	-55 to +125	°C	

[NOTE 1] Permanent LSI damage may occur if "Maximum Ratings" are exceeded. Normal operation should be under the conditions of "ELECTRICAL CHARACTERISTICS –1, –2." If these conditions are exceeded, it could be cause of malfunction of LSI and affects reliability of LSI.

[NOTE 2] All voltages are with respect to GND.

[NOTE 3] The Maximum Total Output Current is total sum of output currents which can flow out (or flow in) from or into the I/O pins and Output pins simultaneously.

• ELECTRICAL CHARACTERISTICS – 1 (V_{CC} = 2.5 to 5.5V, Ta = -20 to +75°C)

Item	Symbol	Test Conditions	Value min.	Value typ.	Value max.	Unit	Note
Input "Low" Voltage	V_{IL}		–	–	0.15·V_{CC}	V	
Input "High" Voltage (1)	V_{IH1}		0.85·V_{CC}	–	V_{CC}	V	2
Input "High" Voltage (2)	V_{IH2}		0.85·V_{CC}	–	10	V	3
Output "Low" Voltage	V_{OL}	I_{OL} = 0.4 mA	–	–	0.4	V	
Output "High" Voltage	V_{OH}	$-I_{OH}$ = 0.08 mA	V_{CC}-0.4	–	–	V	4
Interrupt Input Hold Time	t_{INT}		2·T_{inst}	–	–	μs	
Interrupt Input Fall Time	t_{fINT}		–	–	50	μs	
Interrupt Input Rise Time	t_{rINT}		–	–	50	μs	
Output "High" Level Current	I_{OH}	V_{OH} = 10 V	–	–	3	μA	6
Input Leakage Current	I_{IL}	V_{in} = 0 to V_{CC}	–	–	1.0	μA	2
		V_{in} = 0 to 10V	–	–	3		3
Pull up MOS Current	$-I_P$	V_{CC} = 3V	10	–	80	μA	
Supply Current	I_{CC}	V_{in}=V_{CC}, V_{CC}=3V (f_{osc}/f_{cp} = 200kHz) R_f Oscillation, External Clock Operation	–	–	140	μA	7
Standby I/O Leakage Current	I_{LS}	$\overline{HLT}$ = 0.5V, V_{in}=0 to V_{CC}	–	–	1	μA	5, 8
		$\overline{HLT}$ = 0.5V, V_{in}=0 to 10V	–	–	3	μA	6, 8
Standby Supply Current	I_{CCS}	V_{in} = V_{CC}, V_{CC}=2.5 to 3.5V	–	–	6	μA	9
		$\overline{HLT}$ = 0.1 V, V_{CC}=2.5 to 5.5 V	–	–	10	μA	
External Clock Operation							
External Clock Frequency	f_{cp}		130	200	240	kHz	
External Clock Duty	Duty		45	50	55	%	
External Clock Rise Time	t_{rcp}		0	–	0.2	μs	
External Clock Fall Time	t_{fcp}		0	–	0.2	μs	
Instruction Cycle Time	T_{inst}	T_{inst} = 4/f_{cp}	16.8	20	30.8	μs	
Internal Clock Operation (R_f Oscillation)							
Clock Oscillation Frequency	f_{osc}	R_f = 200kΩ ± 2%, V_{CC}=2.5 to 3.5V	130	–	250	kHz	
	f_{osc}	R_f=200kΩ ± 2%, V_{CC}=2.5 to 5.5V	130	–	350	kHz	
Instruction Cycle Time	T_{inst}	T_{inst}=4/f_{osc}, V_{CC}= 2.5 to 3.5V	16	–	30.8	μs	
	T_{inst}	T_{inst}=4/f_{osc}, V_{CC}=2.5 to 5.5V	11.4	–	30.8	μs	

[NOTE 1] All voltages are with respect to GND.
[NOTE 2] This is applied to RESET, $\overline{HLT}$, OSC_1, INT_0, INT_1 and the With Pull up MOS or CMOS type of I/O pins.
[NOTE 3] This is applied to the Open Drain type of I/O pins.
[NOTE 4] This is applied to the CMOS type of I/O or Output pins.
[NOTE 5] This is applied to the With Pull up MOS or CMOS type of I/O or Output pins
[NOTE 6] This is applied to the Open Drain type of I/O or Output pins.
[NOTE 7] I/O current is excluded.
[NOTE 8] The Standby I/O Leakage Current is the I/O leakage current in the Halt and Disable State.
[NOTE 9] I/O current is excluded.
The Standby Supply Current is the supply current at V_{CC}=2.5 to 5.5V in the Halt State. The supply current in the case where the supply voltage falls to the Halt Duration voltage is called the Halt Current (I_{DH}), and it is shown in "ELECTRICAL CHARACTERISTICS -2."

- **ELECTRICAL CHARACTERISTICS – 2 (Ta = -20 to +75°C)**

Reset and Halt

Item	Symbol	Test Conditions	Value		Unit
			min.	max.	
Halt Duration Voltage	V_{DH}	$\overline{HLT}$ = 0.2V	2.0	–	V
Halt Current	I_{DH}	$V_{in}=V_{CC}$, V_{DH}=2.0V $\overline{HLT}$ = 0.1V	–	12	μA
Halt Delay Time	t_{HD}		200	–	μs
Operation Recovery Time	t_{RC}		200	–	μs
$\overline{HLT}$ Fall Time	t_{fHLT}		–	1000	μs
$\overline{HLT}$ Rise Time	t_{rHLT}		–	1000	μs
$\overline{HLT}$ "Low" Hold Time	t_{HLT}		800	–	μs
$\overline{HLT}$ "High" Hold Time	t_{OPR}	R_f Oscillation, External Clock Operation, V_{CC}=2.5 to 5.5V	0.2	–	ms
RESET Pulse Width (1)	t_{RST1}	External Reset V_{CC}=2.5 to 5.5V $\overline{HLT}$ = V_{CC} R_f Oscillation, External Clock Operation	2	–	ms
RESET Pulse Width (2)	t_{RST2}	External Reset V_{CC}=2.5 to 5.5V $\overline{HLT}$ = V_{CC}	$2 \cdot T_{inst}$	–	μs
RESET Fall Time	t_{fRST}	$\overline{HLT}$ = V_{CC}	–	20	ms
RESET Rise Time	t_{rRST}	$\overline{HLT}$ = V_{CC}	–	20	ms

(NOTE) All voltages are with respect to GND.

■ SIGNAL DESCRIPTION

The input and output signals for the HMCS47C, shown in PIN ARRANGEMENT, are described in the following paragraphs.

- **V_{CC} and GND**

Power is supplied to the HMCS47C using these two pins. V_{CC} is power and GND is the ground connection.

- **RESET**

This pin allows resetting of the HMCS47C at times other than the automatic resetting capability (ACL; Built-in Reset Circuit) already in the HMCS47C. The HMCS47C can be reset by pulling RESET high. Refer to RESET FUNCTION for additional information.

- **OSC_1 and OSC_2**

These pins provide control input for the built-in oscillator circuit. A resistor, ceramic filter circuit, or an external oscillator can be connected to these pins to provide a system clock with various degrees of stability/cost tradeoffs. Lead length and stray capacitance on these two pins should be minimized. Refer to OSCILLATOR for recommendations about these pins.

- **$\overline{HLT}$**

This pin is used to place the HMCS47C in the Halt State (Stand-by Mode).

The HMCS47C can be moved into the Halt State by pulling $\overline{HLT}$ low.

In the Halt State, the internal clock stops and all the internal statuses (the RAM, the registers, the Carry F/F, the Status F/F, the Program Counter, and all the internal statuses) are held.

Consequently, the power consumption is reduced. By pulling $\overline{HLT}$ high, the HMCS47C starts operation from the state just before the Halt State.

Refer to HALT FUNCTION for details of the Halt Mode.

- **$\overline{TEST}$**

This pin is not for user application and must be connected to V_{CC}.

- **INT_0 and INT_1**

These pins provide the capability for asynchronously applying external interrupts to the HMCS47C.

Refer to INTERRUPTS for additional information.

- **$R_{00} - R_{03}$, $R_{10} - R_{13}$, $R_{20} - R_{23}$, $R_{30} - R_{33}$, $R_{40} - R_{43}$, $R_{50} - R_{53}$**

These 24 lines are arranged into six 4-bit Data Input/Output Common Channels.

The 4-bit registers (Data I/O Register) are attached to these channels. Each channel is directly addressed by the operand of input/output instruction. Refer to INPUT/OUTPUT for additional information.

- **$R_{60} - R_{63}$**

These 4 lines are the 4-bit Data Output Channel.

The 4-bit register (Data I/O Register) is attached to this channel.

The channel is directly addressed by the operand of output instruction.

Refer to INPUT/OUTPUT for additional information.

- **$D_0 - D_{15}$**

These lines are 16 1-bit Discrete Input/Output Common Terminals.

The 1-bit latches are attached to these terminals. Each terminal is addressed by the Y register. The D_0 to D_3 terminals are also addressed directly by the operand of input/output instruction. Refer to INPUT/OUTPUT for additional information.

- **ROM**
- **ROM Address Space**

ROM is used as a memory for the instructions and the patterns (constants). The instruction used in the HMCS47C consists of 10 bits. These 10 bits are called "a word", which is a unit for writing into ROM.

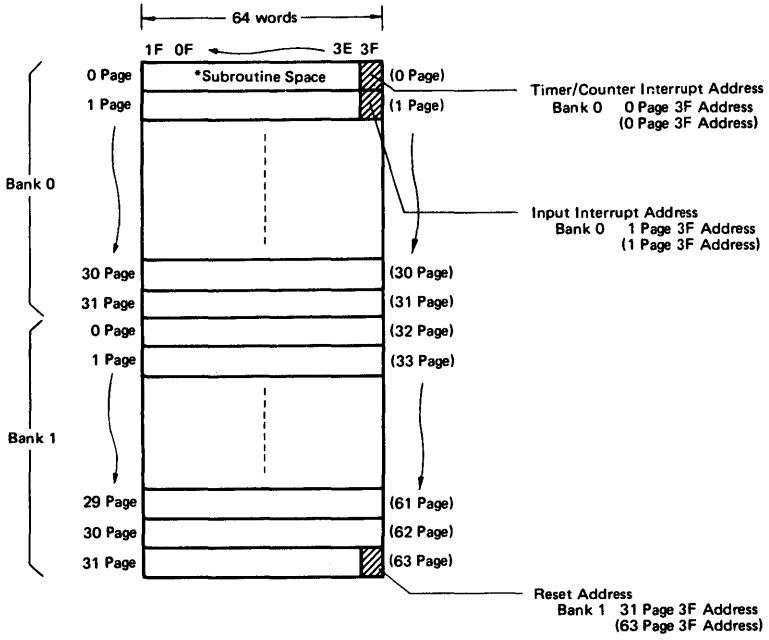
The ROM address has been split into two banks.

Each bank is composed of 32 pages (64 words/page).

The ROM capacity is 4,096 words (1 word = 10 bits) in all.

All addresses can contain both the instructions and the patterns (constants).

The ROM address space is shown in Figure 1.



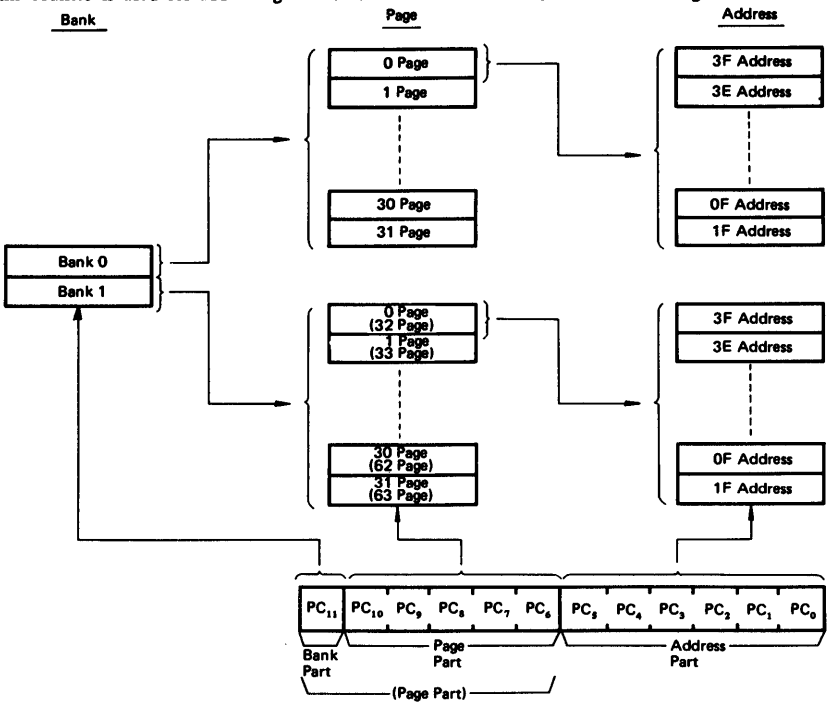
*Bank 0 0 Page (0 Page) is the Subroutine Space.

Note: The parenthesized contents are expressions of the Page, combining the bank part with the page part.

Figure 1 ROM Address Space

- **Program Counter (PC)**

The program counter is used for addressing of ROM. The program counter consists of the bank part, the page part, and the address part as shown in Figure 2.



Note: The parenthesized contents are expressions of the Page, combining the bank part with the page part.

Figure 2 Configuration of Program Counter

The bank part is a 1-bit register and the page part is a 5-bit register.

Once a certain value is loaded into the bank part or the page part, the content is unchanged until other value is loaded by a program.

The settable value is "0" (the Bank 0) or "1" (the Bank 1) for the bank part, and 0 to 31 for the page part.

The address part is a 6-bit polynomial counter and counts up for each instruction cycle time. The sequence in the decimal and hexa-decimal system is shown in Table 1. This sequence is circulating and has neither the starting nor ending point. It doesn't generate an overflow carry. Consequently, the program on a same page is executed in order unless the value of the bank part or the page part is changed.

Table 1 Program Counter Address Part Sequence

Decimal	Hexa-decimal	Decimal	Hexa-decimal	Decimal	Hexa-decimal
63	3F	5	05	9	09
62	3E	11	0B	19	13
61	3D	23	17	38	26
59	3B	46	2E	12	0C
55	37	28	1C	25	19
47	2F	56	38	50	32
30	1E	49	31	37	25
60	3C	35	23	10	0A
57	39	6	06	21	15
51	33	13	0D	42	2A
39	27	27	1B	20	14
14	0E	54	36	40	28
29	1D	45	2D	16	10
58	3A	26	1A	32	20
53	35	52	34	0	00
43	2B	41	29	1	01
22	16	18	12	3	03
44	2C	36	24	7	07
24	18	8	08	15	0F
48	30	17	11	31	1F
33	21	34	22		
2	02	4	04		

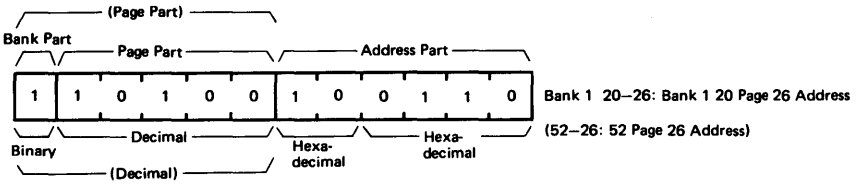
- **Designation of ROM Address and ROM Code**

The bank part of the ROM address is shown in the binary system and the page part in the decimal system. The address part is divided into 2 bits and 4 bits, and shown in the hexa-decimal system.

It is possible to combine the bank part and the page part and show the combined part as the Page (in the decimal system). In this case, the 0 Page to the 31 Page in the Bank 1 are shown as the 32 Page to the 63 Page. The examples are shown in Figure 3.

One word (10 bits) of ROM is divided into three parts (2 bits, 4 bits and 4 bits from the most significant bit O_{10} in order) shown in the hexa-decimal system. The examples are shown in Figure 3.

(a) ROM Address



(b) ROM Code

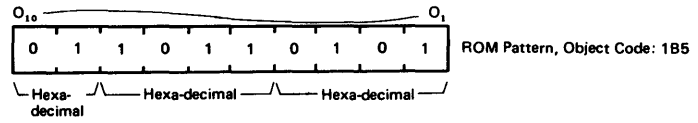


Figure 3 Designation of ROM Address and ROM Code

■ PATTERN GENERATION

The pattern (constant) can be accessed by the pattern instruction (P). The pattern can be written in any address of the ROM address space.

- **Reference**

ROM addressing for reference of the patterns is achieved by modifying the program counter with the accumulator, the B register, the Carry F/F and the operand p. Figure 4 shows how to modify the program counter. The address part is replaced with the accumulator and the lower 2 bits of B register, while the page part and the bank part are ORed with the upper 2 bits of B register, the Carry F/F and the operand p.

The value of the operand p (p_2, p_1, p_0) is 0 to 7 (decimal).

The bank part of the ROM address to be referenced to is determined by the logical equation: $PC_{11} + p_2$ (p_2 = the MSB of the operand p).

If the address where the pattern instruction exists is in the Bank 1, only the pattern of the Bank 1 can be referenced.

If the address where the pattern instruction exists is in the Bank 0, the pattern of the either Bank 1 or Bank 0 can be referenced depending on the value of p_2. The truth table of the bank part of the ROM address is shown in Table 2.

The value of the program counter is apparently modified and does not change actually. After execution of the pattern instruction, the program counter counts up and the next instruction is executed.

The pattern instruction is executed in 2-cycle time.

- **Generation**

The pattern of referred ROM address is generated as the following two ways:

(i) The pattern is loaded into the accumulator and B register.

(ii) The pattern is loaded into the Data I/O Registers R2 and R3.

Selection is determined by the command bits (O_9, O_{10}) in the pattern.

Mode (i) is performed when O_9 is "1" and mode (ii) is performed when O_{10} is "1".

Mode (i) and (ii) are simultaneously performed when both of O_9 and O_{10} are "1". The correspondence of each bit of the pattern is shown in Figure 5.

Examples of the pattern instruction is shown in Table 3.

CAUTION

In the program execution, the pattern can not be distinguished from the instruction. When the program is executed at the addresses into which pattern is written, the instruction corresponding to the pattern bit is executed. Take care that a pattern is not executed as an instruction.

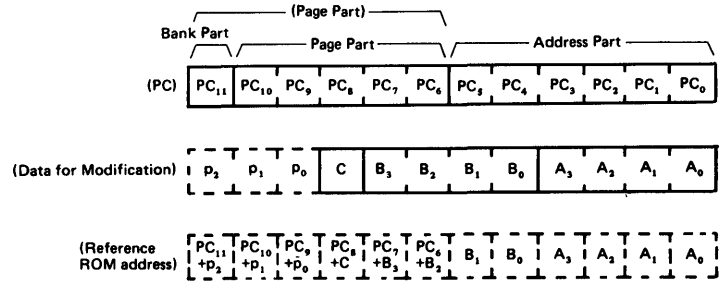


Figure 4 ROM Addressing for Pattern Generation

Table 2 Bank Part Truth Table of Pattern Generation

PC_{11}	p_2	Bank part of ROM address to be referenced to
1 (Bank 1)	1	1 (Bank 1)
	0	1 (Bank 1)
0 (Bank 0)	1	1 (Bank 1)
	0	0 (Bank 0)

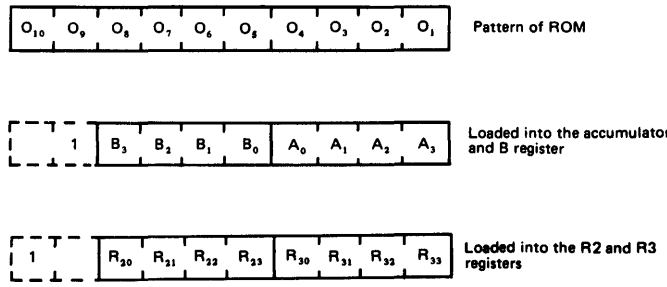


Figure 5 Correspondence of Each Bit of Pattern

Table 3 Example of Pattern Instructions

Before Execution					Referred ROM Address	ROM Pattern	After Execution			
PC	p	C	B	A			B	A	R2	R3
Bank 0 0-3F (0-3F)	1	0	A	0	Bank 0 10-20 (10-20)	12D	2	B	–	–*
Bank 0 0-3F (0-3F)	7	1	4	0	Bank 1 29-00 (61-00)	22D	–	–	4	B
Bank 1 30-00 (62-00)	4	0/1**	0	9	Bank 1 30-09 (62-09)	32D	2	B	4	B
Bank 1 30-00 (62-00)	1	0/1**	F	9	Bank 1 31-39 (63-39)	223	–	–	4	C

* "–" means that the value does not change after execution of the instruction.
** "0/1" means that either "0" or "1" may be selected.

■ BRANCH

ROM is accessed according to the program counter sequence and the program is executed. In order to jump to any address out of the sequence, there are four ways. They are explained in the following paragraphs.

• BR

By BR instruction, the program branches to an address in the current page.

The lower 6 bits of ROM Object Code (operand a, O_6 to O_1) are transferred to the address part of the program counter. This instruction is a conditional instruction and executed only when the Status F/F is "1". If it is "0", the instruction is skipped and the Status F/F becomes "1". The operation is shown in Figure 6.

• LPU

By LPU instruction, the jump of the bank and page is performed.

The lower 5 bits of the ROM Object Code (operand u, O_5 to O_1) are transferred to the page part of the program counter with a delay of 1-cycle time. At the same time, the signal $\overline{R_{70}}$ (the reversed-phase signal of the Data I/O Register R_{70}) is transferred to the bank part of the program counter with a delay of 1-cycle time. The operation is shown in Figure 7.

Consequently, the bank and page will remain unchanged in the cycle immediately following this instruction. In the next cycle, a jump of the bank and page is achieved.

This instruction (LPU) is conditional, and is executed only when the Status F/F is "1". Even after a skip, the Status F/F will remain unchanged ("0").

LPU instruction is used in combination with BR instruction or CAL instruction as the macro instruction of BRL or CALL instruction.

• BRL

By BRL instruction, the program branches to an address in any bank and page.

This instruction is a macro instruction of LPU and BR instructions, which is divided into two instructions as follows.

BRL a-b → LPU a
BR b

< Jump to Bank "$\overline{R_{70}}$", a Page – b Address >

BRL instruction is a conditional instruction because of characteristics of LPU and BR instructions, and is executed only when the Status F/F is "1". If the Status F/F is "0", the instruction is skipped and the Status F/F becomes "1". The examples of BRL instruction are shown in Figure 8.

• TBR (Table Branch)

By TBR instruction, the program branches by the table.

The program counter is modified with the accumulator, the B register, the Carry F/F and the operand p.

The method for modification is shown in Figure 9.

The bank part is determined by the logical equation: $PC_{11} + p_2$, as shown in Table 4.

If the address where TBR instruction exists is in the Bank 1, it is possible to jump to an address only in the Bank 1, not to an address in the Bank 0.

If the address where TBR instruction exists is in the Bank 0, it is possible to jump to an address in either the Bank 1 or the Bank 0 depending on the value of the operand p_2.

TBR instruction is executed regardless of the Status F/F, and does not affect the Status F/F.

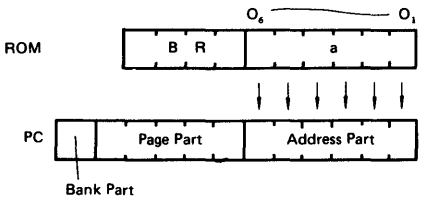


Figure 6 BR Operation

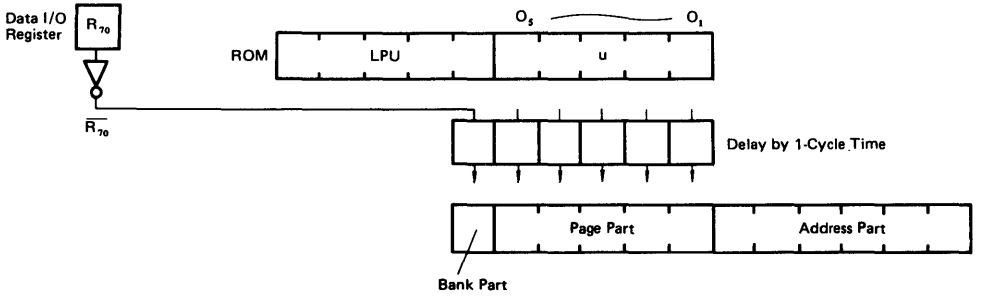


Figure 7 LPU Operation

```
Branch to Bank 0
·  LAI   15
   LRA   7        R70 = "1" (R70 = "0")
   LPU   5   }    BRL 5-3F
   BR    3F  }    (Branch to Bank 0 5-3F (5-3F))

·  LAI   15
   LBA
   LRA   7        R70 = "1" (R70 = "0")
   COMB
   LPU   31  }    BRL 31-3F
   BR    3F  }    (Branch to Bank 0 31-3F (31-3F))

Branch to Bank 1

·  LAI   0
   LRA   7        R70 = "0" (R70 = "1")
   LPU   15  }    BRL 15-3F
   BR    3F  }    (Branch to Bank 1 15-3F (47-3F))

·  LAI   0
   LTA
   LRA   7        R70 = "0" (R70 = "1")
   LYI   2
   XMA
   LPU   10  }    BRL 10-2E
   BR    2E  }    (Branch to Bank 1 10-2E (42-2E))
```

Figure 8 BRL Example

Table 4 Bank Part Truth Table of TBR Instruction

PC_{11}	p_2	Bank Part of PC after TBR
1 (Bank 1)	1	1 (Bank 1)
	0	1 (Bank 1)
0 (Bank 0)	1	1 (Bank 1)
	0	0 (Bank 0)

■ SUBROUTINE JUMP

There are two types of subroutine jumps. They are explained in the following paragraphs.

• CAL

By CAL instruction, subroutine jump to the Subroutine Space is performed.

The Subroutine Space is the Bank 0 0 Page (0 Page).

The address next to CAL instruction address is pushed onto the Stack ST1 and the contents of the stacks ST1, ST2 and ST3 are pushed onto the stacks ST2, ST3 and ST4 respectively as shown in Figure 10.

The bank part of the program counter becomes the Bank 0 and the page part becomes the 0 Page. The lower 6 bits (operand a, O_6 to O_1) of the ROM Object Code is transferred to the address part of the program counter.

The HMCS47C has 4 levels of stack (ST1, ST2, ST3 and ST4) which allows the programmer to use up to 4 levels of subroutine jumps (including interrupts).

CAL is a conditional instruction and executed only when the Status F/F is "1". If the Status F/F is "0", it is skipped and the Status F/F changes to "1".

• CALL

By CALL instruction, subroutine jump to an address in any bank and page is performed.

Subroutine jump to any address can be implemented by the subroutine jump to the page specified by LPU instruction in the bank designated by the reversed-phase signal $\overline{R_{70}}$ of the Data I/O Register R_{70}.

This instruction is a macro instruction of LPU and CAL instructions, which is divided into two instructions as follows.

```
CALL   a-b ----------> LPU  a
                       CAL  b
```

< Subroutine Jump to Bank "$\overline{R_{70}}$", a Page – b Address >

CALL instruction is conditional because of characteristics of LPU and CAL instructions and is executed when the Status F/F is "1". If the Status F/F is "0", the instruction is skipped and the Status F/F changes to "1". The examples of CALL instruction are shown in Figure 11.

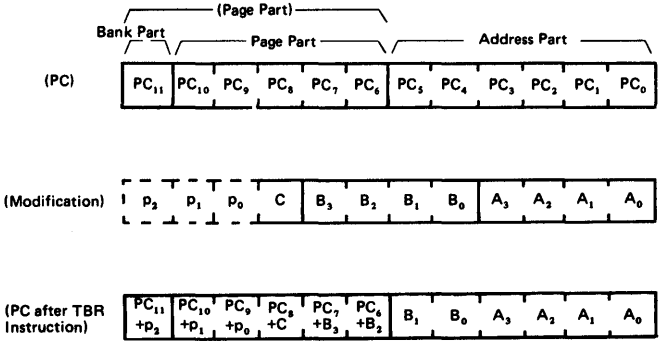


Figure 9 Modification of Program Counter by TBR Instruction

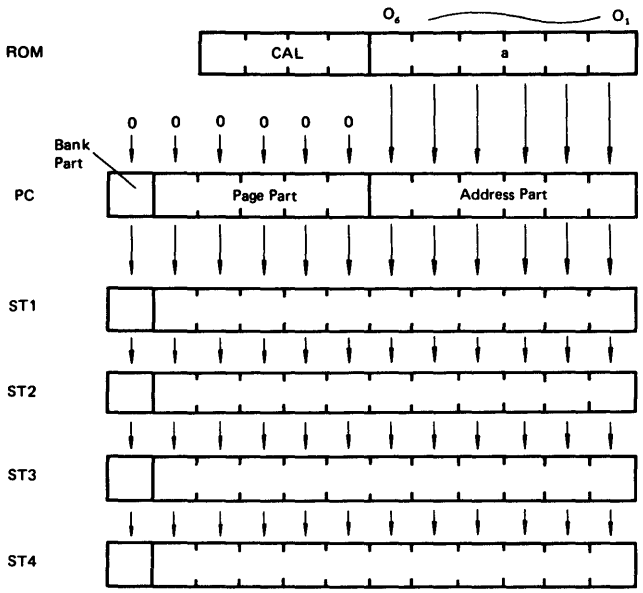


Figure 10 Subroutine Jump Stacking Order

```
Subroutine Jump to Bank 0
·  LAI   15
  ┌-LRA   7          R70 = "1" (R70 = "0")
  └→LPU   5  }
    CAL   3F }       CALL 5-3F
                     (Subroutine Jump to Bank 0 5-3F (5-3F))

·  LAI   15
   LBA
  ┌-LRA   7          R70 = "1" (R70 = "0")
  ¦ COMB
  └→LPU   31 }
    CAL   3F }       CALL 3-3F
                     (Subroutine Jump to Bank 0 31-3F (31-3F))
Subroutine Jump to Bank 1
·  LAI   0
  ┌-LRA   7          R70 = "0" (R70 = "1")
  └→LPU   15 }
    CAL   3F }       CALL 15-3F
                     (Subroutine Jump to Bank 1 15-3F (47-3F))

·  LAI   0
   LTA
  ┌-LRA   7          R70 = "0" (R70 = "1")
  ¦ LYI   3
  ¦ XMA
  └→LPU   10 }
    CAL   2E }       CALL 10-2E
                     (Subroutine Jump to Bank 1 10-2E (42-2E))
```

Figure 11 CALL Example

■ RAM

RAM is a memory used for storing data and saving the contents of the registers. Its capacity is 256 digits (1,024 bits) where one digit consists of 4 bits.

Addressing of RAM is performed by a matrix of the file No. and the digit No.

The file No. is set in the X register and the digit No. in the Y register for reading, writing or testing. Specific digits in RAM can be addressed not via the X register and Y register. These digits are called "Memory Register (MR)", 0 to 15 (16 digits in all). The memory register can be exchanged with the accumulator by XAMR instruction.

The RAM address space is shown in Figure 12.

In an instruction in which reading from RAM and writing to RAM coexist (exchange between RAM and the register), reading precedes writing and the write data does not affect the read data.

The RAM bit manipulation instruction enables any addressed RAM bit to be set, reset or tested. The bit assignment is specified by the operand n of the instruction.

The bit test makes the Status F/F "1" when the assigned bit is "1" and makes it "0" when the assigned bit is "0".

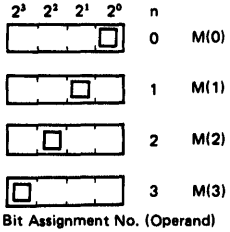
Correspondence between the RAM bit and the operand n is shown in Figure 13.

X \ Y	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Digit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0															
1	1															
2	2															
3	3															
4	4															
5	5															
6	6															
7	7															
8	8															
9	9															
10	10															
11	11															
12	12															
13	13															
14	14															
15	15	MR15	MR14	MR13	MR12	MR11	MR10	MR9	MR8	MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0

Y register Digit No.

X register File No.

Figure 12 RAM Address Space



n = Bit Assignment No. (Operand)

Figure 13 RAM Bit and Operand n

■ REGISTER

The HMCS47C has six 4-bit registers and two 1-bit registers available to the programmer. The 1-bit registers are the Carry F/F and the Status F/F. They are explained in the following paragraphs.

- **Status F/F (S)**

The Status F/F latches the result of logical or arithmetic operations (Not Zero, Overflow) and bit test operations. The Status F/F affects conditional instructions (LPU, BR and CAL instructions). These instructions are executed only when the Status F/F is "1". If it is "0", these instructions are skipped and the Status F/F becomes "1".

- **Accumulator (A; A Register) and Carry F/F (C)**

The result of the Arithmetic Logic Unit (ALU) operation (4 bits) and the overflow of the ALU are loaded into the accumulator and the Carry F/F. The Carry F/F can be set, reset or tested. Combination of the accumulator and the Carry F/F can be right or left rotated. The accumulator is the main register for ALU operation and the Carry F/F is used to store the overflow generated by ALU operation when the calculation of two or more digits (4 bits/digit) is performed.

- **B Register (B)**

The result of ALU operation (4 bits) is loaded into this register. The B register is used as a sub-accumulator to stack data temporarily and also used as a counter.

- **X Register (X)**

The result of ALU operation (4 bits) is loaded into this register. The X register has exchangeability for the SPX register. The X register addresses the RAM file.

- **SPX Register (SPX)**

The SPX register has exchangeability for the X register.

The SPX register is used to stack the X register and expand the addressing system of RAM in combination with the X register.

- **Y Register (Y)**

The result of ALU operation (4 bits) is loaded into this register. The Y register has exchangeability for the SPY register. The Y register can calculate itself simultaneously with transferring data by the bus lines, which is usable for the calculation of two or more digits (4 bits/digit). The Y register addresses the RAM digit and 1-bit Discrete I/O.

- **SPY Register (SPY)**

The SPY register has exchangeability for the Y register. The SPY register is used to stack the Y register and expand the addressing system of RAM and 1-bit Discrete I/O in combination with the Y register.

■ INPUT/OUTPUT

- **4-bit Data Input/Output Common Channel (R)**

The HMCS47C has five 4-bit Data I/O Common Channels (R0, R1, R2, R3, R4 and R5) and one 4-bit Data Output Channel (R6).

The 4-bit registers (Data I/O Register) are attached to these channels.

Each channel is directly addressed by the operand P of input/output instruction.

The data is transferred from the accumulator and the B register to the Data I/O Registers R0 to R6 via the bus lines. Pattern instruction enables the patterns of ROM to be loaded into the Data I/O Registers R2 and R3.

Input instruction enables the 4-bit data to be sent to the accumulator and the B register from R0 to R5. Note that, since the Data I/O Register's output is directly connected to the pin even during execution of input instruction, the input data is wired logic of the Data I/O Register's output and the pin input. Therefore, the Data I/O Register should be set to 15 (all bits of the Data I/O Register is "1") not to affect the pin input before execution of input instruction, and Open Drain or With Pull up MOS should be specified for the I/O configuration of these pins.

The block diagram is shown in Figure 14. The I/O timing is shown in Figure

- **1-bit Discrete Input/Output Common Terminal (D)**

The HMCS47C has 16 1-bit Discrete I/O Common Terminals.

The 1-bit Discrete I/O Common Terminal consists of a 1-bit latch and an I/O common pin.

The 1-bit Discrete I/O is addressed by the Y register. The addressed latch can be set or reset by output instruction and "0" and "1" level can be tested with the addressed pin by input instruction.

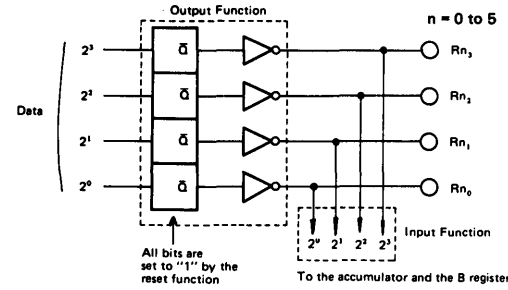
Note that, since the latch output is directly connected to the pin even during execution of input instruction, the input data is wired logic of the latch's output and the pin input. Therefore, the latch should be set to "1" not to affect the pin input before execution of input instruction and Open Drain or With Pull up MOS should be specified for the I/O configuration of this pin.

The D_0 to D_3 terminals are also addressed directly by the operand n of input/output instruction and can be set or reset. The block diagram is shown in Figure 16 and the I/O timing is shown in Figure 17.

- **I/O Configuration**

The I/O configuration of each pin can be specified among Open Drain, With Pull up MOS and CMOS using a mask option as shown in Figure 18.

(a) R0 to R5



(b) R6

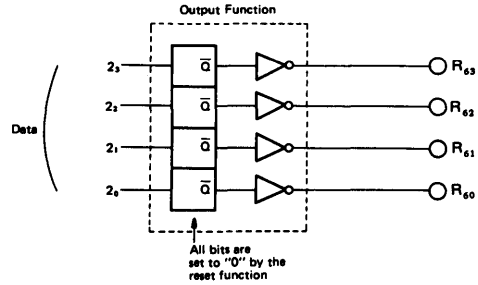


Figure 14 4-bit Data I/O Block Diagram

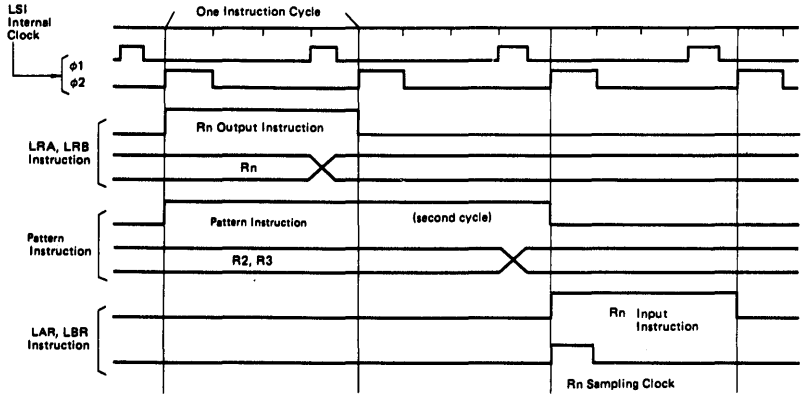


Figure 15 4-bit Data I/O Timing

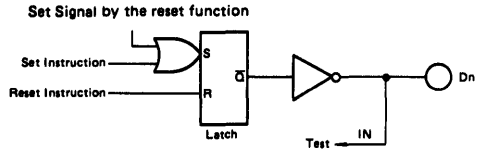


Figure 16 1-bit Discrete I/O Block Diagram

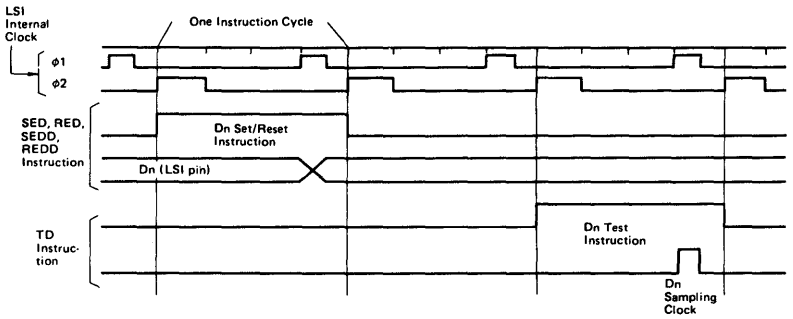
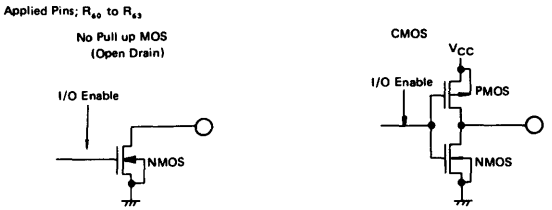
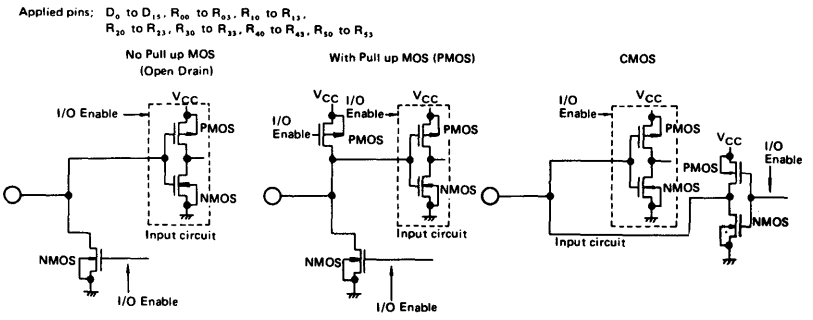


Figure 17 1-bit Discrete I/O Timing

(a) Configuration of Output Pin



(b) Configuration of I/O Pin



* When "Disable" is specified for the I/O State at the Halt State, the I/O Enable signal shown in the figure turns off the input circuit, Pull up MOS and NMOS output and sets CMOS output to high inpedance (PMOS, NMOS; OFF).

Figure 18 I/O Configuration

■ TIMER/COUNTER

The timer/counter consists of the 4-bit counter and the 6-bit prescaler as shown in Figure 19. The 4-bit counter may be loaded under program control and is incremented toward 15 by the prescaler overflow output pulse or the input pulse of INT_1 pin (its leading edge is counted). The clock input to the counter is selected by the CF F/F. When the CF F/F is "0", the clock input is the prescaler overflow output pulse (Timer Mode). When the CF F/F is "1", the clock input is the input pulse of INT_1 pin (Counter Mode). When the counter reaches zero (returns from 15 to zero), the overflow output pulse is generated and the counter continues to count ($14 \rightarrow 15 \rightarrow 0 \rightarrow 1 \rightarrow 2 \cdots$).

The TF F/F is a flip-flop which masks interrupts from the timer/counter. It can be set and reset by interrupt instruction. If the overflow output pulse of the counter is generated when the TF F/F is reset ("0"), an interrupt request occurs and the TF F/F becomes "1". If the overflow output pulse is generated when the TF F/F is set ("1"), no interrupt request occurs. The TTF instruction enables the TF F/F to be tested.

The prescaler is a 6-bit frequency divider. It divides a system clock (instruction frequency) by 64 into the overflow output pulses of "instruction frequency ÷ 64".

The prescaler is cleared when data is loaded into the counter (by LTA or LTI instruction). The frequency division is 0 when the prescaler is cleared. At the 64th clock, an overflow output

pulse is generated from the prescaler. During operation of the LSI, the prescaler is operating and cannot be stopped. (In the Halt state, it stops.) The relation between the specified value of the counter and specified time in the Timer Mode is shown in Table 5.

The pulse width of the INT_1 pin in the Counter Mode must be at least 2-cycle time for both "High" and "Low" levels as shown in Figure 19.

■ INTERRUPT

The HMCS47C can be interrupted in two different ways: through the external interrupt input pins (INT_0, INT_1) and the timer/counter interrupt request. When any interrupt occurs, processing is suspended, the Status F/F is unchanged, the present program counter is pushed onto the stack ST1 and the contents of the stacks ST1, ST2 and ST3 are pushed onto the stacks ST2, ST3 and ST4 respectively. At that time, the Interrupt Enable F/F (I/E) is set and the address jumps to a fixed destination (Interrupt Address), and then the interrupt routine is executed. Stacking the registers other than the program counter must be performed by the program. The interrupt routine must end with RTNI (Return Interrupt) instruction which sets the I/E F/F simultaneously with RTN instruction.

The Interrupt Address:

Input Interrupt Address ..... Bank 0 1 Page 3F Address (1 Page 3F Address)

Timer/Counter Interrupt Address ..... Bank 0 0 Page 3F Address (0 Page 3F Address)

The input interrupt has priority over the timer/counter interrupt.

The INT_0 and INT_1 pin have an interrupt request function. Each terminal consists of a circuit which generates leading pulse and the Interrupt mask F/F (IF0, IF1). An interrupt is enabled (unmasked) when the IF0 F/F or IF1 F/F is reset. When the INT_0 or INT_1 pin changes from "0" to "1" (from "Low" level to "High" level), a leading pulse is generated to produce an interrupt request. At the same time, the IF0 F/F or IF1 F/F is set. When the IF0 F/F or IF1 F/F is set, the interrupt masking for the pin will result. (If a leading pulse is generated, no interrupt request occurs.)

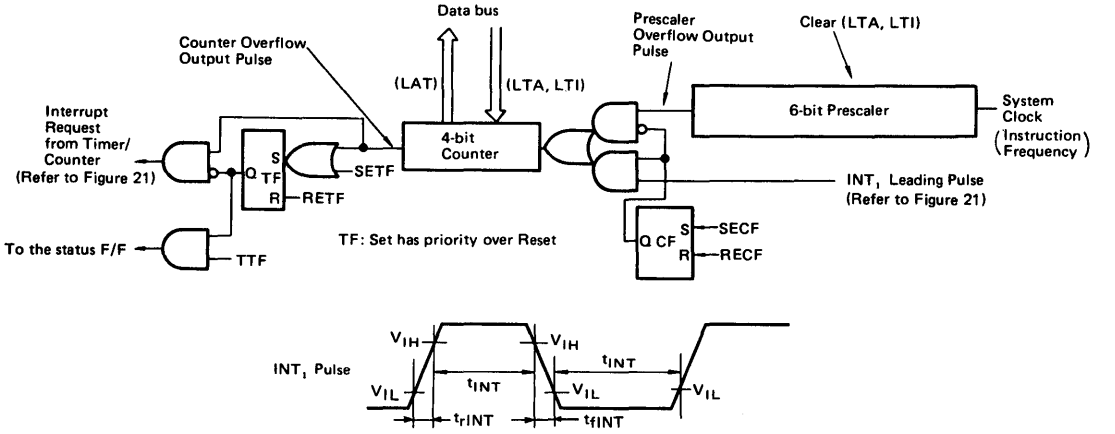


Figure 19 Timer/Counter Block Diagram

Table 5 Timer Range

Specified Value	Number of Cycles	*Time (ms)	Specified Value	Number of Cycles	*Time (ms)
0	1024	5.12	8	512	2.56
1	960	4.80	9	448	2.24
2	896	4.48	10	384	1.92
3	832	4.16	11	320	1.60
4	768	3.84	12	256	1.28
5	704	3.52	13	192	0.96
6	640	3.20	14	128	0.64
7	576	2.88	15	64	0.32

* Time is based on instruction frequency 200kHz. (One Instruction Cycle Time (T_{inst}) = 5μs)

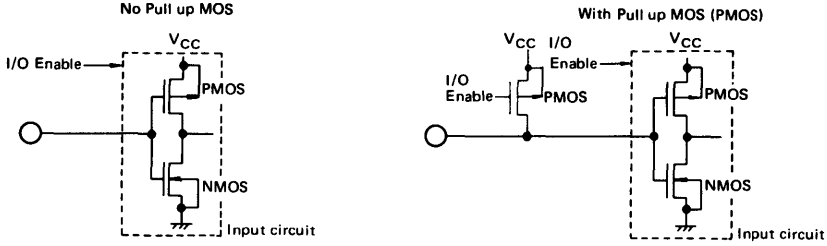
An interrupt request generated by the leading pulse is latched into the input interrupt request F/F (I/RI) on the input side. If the Interrupt Enable F/F (I/E) is "1" (Interrupt Enable State), an interrupt occurs immediately and the I/RI F/F and the I/E F/F are reset. If the I/E F/F is "0" (Interrupt Disable State), the I/RI F/F is held at "1" until the HMCS47C gets into the Interrupt Enable State.

The IF0 F/F, the IF1 F/F, the INT_0 pin and the INT_1 pin can be tested by interrupt instruction. Therefore, the INT_0 and the INT_1 can be used as additional input pins with latches.

The INT_0 pin and INT_1 pin can be provided with Pull up MOS using a mask option as shown in Figure 20.

An interrupt request from the timer/counter is latched into the timer interrupt request F/F (I/RT). The succeeding operations are same as an interrupt from the input. Only the exception is that, since an interrupt from the input precedes a timer/counter interrupt, the input interrupt occurs if both the I/RI F/F and the I/RT F/F are "1" (when the input interrupt and the timer/counter interrupts are generated simultaneously). During this processing, the I/RT F/F remains "1". The timer/counter interrupt can be implemented after the input interrupt processing is achieved.

The interrupt circuit block diagram is shown in Figure 21.



* When "Disable" is specified for the I/O State at the Halt State, the I/O Enable signal shown in the figure turns off the input circuit and Pull up MOS.

Figure 20 Configuration of INT_0 and INT_1

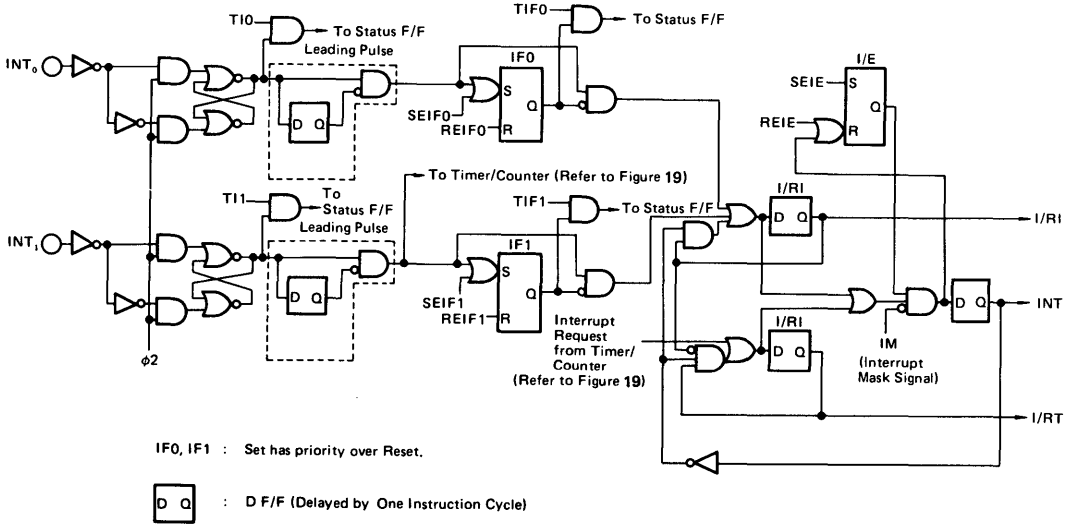


Figure 21 Interrupt Circuit Block Diagram

■ RESET FUNCTION

The reset is performed by setting the RESET pin to "1" ("High" level) and the HMCS47C gets into operation by setting it to "0" ("Low" level); Refer to Figure 22. Moreover, the HMCS47C has the power-on reset function (ACL; Built-in Reset Circuit). The Built-in Reset Circuit restricts the rise condition of the power supply; Refer to Figure 23. When the Built-in Reset Circuit is used, RESET should be connected to GND.

HMCS47CL doesn't have the power-on reset function.

Internal state of the HMCS47C are specified as follows by the reset function.

- Program Counter (PC) is set to Bank 1 31 Page 3F Address (63 Page 3F Address).
- Data I/O Register R_{70} is set to "1" (Jumps to Bank 0 by execution of LPU instruction after the reset).
- I/RI, I/RT, I/E and CF are reset to "0"
- IF0, IF1, and TF are set to "1"
- Data I/O Registers (R0 to R6) and Discrete I/O Latches (D_0 to D_{15}) are all set to "1"

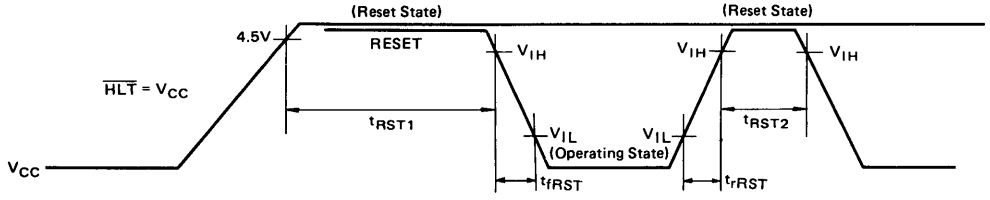
Note that all the other logic blocks (the Stack Registers, the Status F/F, the accumulator, the Carry F/F, the registers, the Timer/Counter, RAM) are not cleared by the reset function. The user should initialize these blocks by software. Because the Status F/F after the reset is not defined, set the Status F/F to "0" or "1" before the first execution of the conditional instructions (LPU, CAL and BR instructions).

■ HALT FUNCTION

When the $\overline{HLT}$ pin is set to "0" ("Low" level), the internal clock stops and all the internal statuses (RAM, the Registers, the Carry F/F, the Status F/F, the Program Counter, and all the internal statuses) are held. Becuase all internal logic operation stop, power consumption is reduced. There are two input/output statuses in the Halt State. The user should specify either "Enable" or "Disable" using a mask option at the time of ordering ROM.

"Enable"
- Output ..... The status before the Halt State is held.
- Pull up MOS ... ON
- Input ..... Independent of the Halt State or Operating State (Input Circuit is ON)

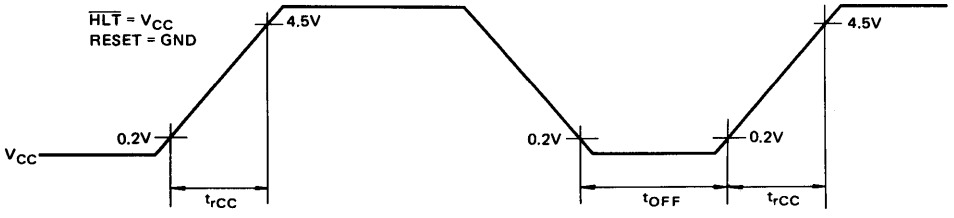
Since Pull up MOS is ON, Pull up MOS current flows with output "0" ("Low" level) in the Halt State (NMOS; ON). When an input signal changes, transition current flows into an input circuit. Also, current flows into Pull



* t_{RST1} includes the time required from the power ON until the operation gets into the constant state.

** t_{RST2} is applied when the operation is in the constant state.

Figure 22 RESET Timing



* t_{OFF} specifies the period when the power supply is OFF in the case that a short break of the power supply occurs and the power supply ON/OFF is repeated.

Figure 23 Power Supply Timing for Built-in Reset Circuit

up MOS. These currents are added to the Stand-by Supply Current (or Halt Current).

"Disable"
- Output ..... NMOS Output: OFF
  CMOS Output: High Impedance (NMOS, PMOS: OFF)
- Pull up MOS ... OFF
- Input ..... Input Circuit: OFF

Both input and output are at high impedance state. Since an input circuit is OFF, any current other than the Stand-by Supply Current (or Halt Current) does not flow even if an input signal changes.

When the $\overline{HLT}$ pin is set to "1" ("High" level), the HMCS47C gets into operation from the status just before the Halt State. The halt timing is shown in Figure 24.

CAUTION

If, during the Halt State, the external reset input is applied (RESET = "1" ("High" level)), the internal status is not held.

■ OSCILLATOR

The HMCS47C contains its own oscillator and frequency divider (CPG). The user can obtain the desired timing for operation of the LSI by merely connecting an resistor R_f or ceramic filter circuit (Internal Clock Operation). Also an external oscillator can supply a clock (External Clock Operation).

The OSC_1 clock frequency is internally divided by four to produce the internal system clocks.

The user may exchange the external parts for the same LSI to select either of these two operational modes as shown in Figure 25. There is no need of specifying it by using the mask option.

The typical value of clock oscillation frequency (f_{osc}) varies with a oscillation resistor R_f as shown in Figure 26.

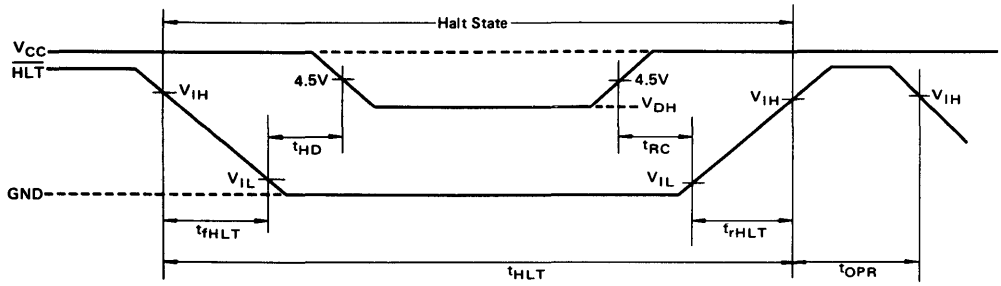
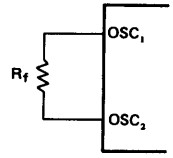


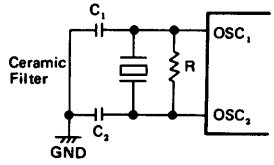
Figure 24 Halt Timing

(a) Internal Clock Operation Using Resistor R_f



Wiring of OSC_1 and OSC_2 terminals should be as short as possible because the oscillation frequency is modified by capacitance of these terminals.

(b) Internal Clock Operation Using Ceramic Filter Circuit (This is not applied to HMCS47CL.)

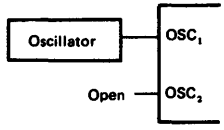


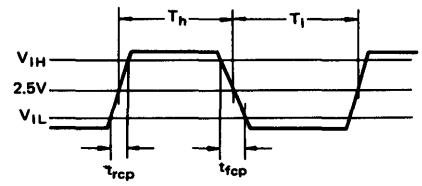
Ceramic Filter; CSB800A (MURATA)
R_1 ; 1MΩ ± 10%
C_1 ; 100pF ± 10% (Ceramic Capacitor)
C_2 ; 100pF ± 10% (Ceramic Capacitor)

The ceramic filter oscillation does not apply when using "Halt" and not resetting at the time of "Halt" cancellation.
This circuit is the example of the typical use. As the oscillation characteristics is not guaranteed, please consider and examine the circuit constants carefully on your application.

Figure 25 Clock Operation Mode (to be continued)

(c) External Clock Operation





$$\text{Duty} = \frac{T_l}{T_h + T_l} \times 100\%$$

Figure 25 Clock Operation Mode

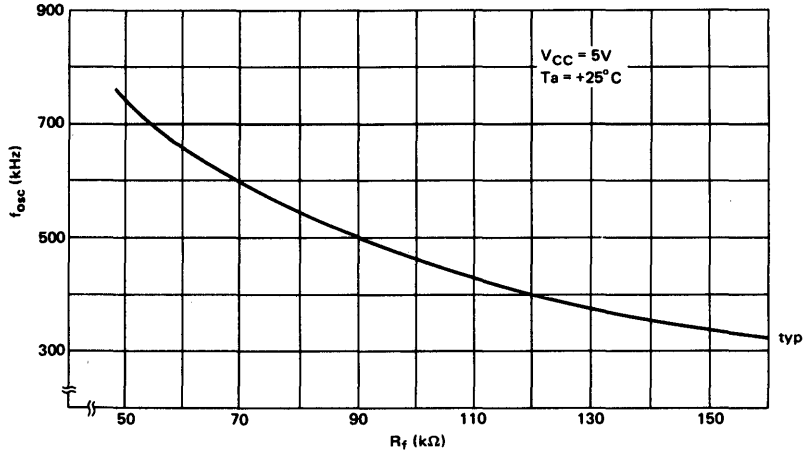


Figure 26 Typical Value of Oscillation Frequency vs. R_f

■ INSTRUCTION LIST

The instructions of the HMCS47C are listed according to their functions, as shown in Table 6 .

Table 6 Instruction List

Group	Mnemonic	Function	Status
Register · Register Instruction	LAB	B → A	
	LBA	A → B	
	LAY	Y → A	
	LASPX	SPX → A	
	LASPY	SPY → A	
	XAMR m	A ↔ MR (m)	
RAM Address Register Instruction	LXA	A → X	
	LYA	A → Y	
	LXI i	i → X	
	LYI i	i → Y	
	IY	Y+1 → Y	NZ
	DY	Y−1 → Y	NB
	AYY	Y+A → Y	C
	SYY	Y−A → Y	NB
	XSPX	X ↔ SPX	
	XSPY	Y ↔ SPY	
	XSPXY	X ↔ SPX, Y ↔ SPY	
RAM · Register Instruction	LAM (XY)	M → A (XY ↔ SPXY)	
	LBM (XY)	M → B (XY ↔ SPXY)	
	XMA (XY)	M ↔ A (XY ↔ SPXY)	
	XMB (XY)	M ↔ B (XY ↔ SPXY)	
	LMAIY (X)	A → M, Y+1 → Y (X ↔ SPX)	NZ
	LMADY (X)	A → M, Y−1 → Y (X ↔ SPX)	NB
Immediate Transfer Instruction	LMIIY i	i → M, Y+1 → Y	NZ
	LAI i	i → A	
	LBI i	i → B	
Arithmetic Instruction	AI i	A+i → A	C
	IB	B+1 → B	NZ
	DB	B−1 → B	NB
	AMC	M+A+$\overline{C}$ (F/F) → A	C
	SMC	M−A−$\overline{C}$ (F/F) → A	NB
	AM	M+A → A	C
	DAA	Decimal Adjustment (Addition)	
	DAS	Decimal Adjustment (Subtraction)	
	NEGA	$\overline{A}$+1 → A	
	COMB	$\overline{B}$ → B	
	SEC	"1" → C (F/F)	
	REC	"0" → C (F/F)	
	TC	Test C (F/F)	C (F/F)
	ROTL	Rotation Left	
	ROTR	Rotation Right	
	OR	A ∪ B → A	

(to be continued)

Group	Mnemonic	Function	Status
Compare Instruction	MNEI i	M ≠ i	NZ
	YNEI i	Y ≠ i	NZ
	ANEM	A ≠ M	NZ
	BNEM	B ≠ M	NZ
	ALEI i	A ≧ i	NB
	ALEM	A ≧ M	NB
	BLEM	B ≧ M	NB
RAM Bit Manipulation Instruction	SEM n	"1" → M (n)	
	REM n	"0" → M (n)	
	TM n	Test M (n)	M(n)
ROM Address Instruction	BR a	Branch on Status 1	1
	CAL a	Subroutine Jump on Status 1	1
	LPU u	Load Program Counter Upper on Status 1	
	TBR p	Table Branch	
	RTN	Return from Subroutine	
Interrupt Instruction	SEIE	"1" → I/E	
	SEIF0	"1" → IF0	
	SEIF1	"1" → IF1	
	SETF	"1" → TF	
	SECF	"1" → CF	
	REIE	"0" → I/E	
	REIF0	"0" → IF0	
	REIF1	"0" → IF1	
	RETF	"0" → TF	
	RECF	"0" → CF	
	TI0	Test INT_0	INT_0
	TI1	Test INT_1	INT_1
	TIF0	Test IF0	IF0
	TIF1	Test IF1	IF1
	TTF	Test TF	TF
	LTI i	i → Timer/Counter	
	LTA	A → Timer/Counter	
	LAT	Timer/Counter → A	
	RTNI	Return Interrupt	
Input/Output Instruction	SED	"1" → D (Y)	
	RED	"0" → D (Y)	
	TD	Test D (Y)	D(Y)
	SEDD n	"1" → D (n)	
	REDD n	"0" → D (n)	
	LAR p	R(p) → A	
	LBR p	R(p) → B	
	LRA p	A → R (p)	
	LRB p	B → R (p)	
	P p	Pattern Generation	
	NOP	No Operation	

[NOTE] 1. (XY) after a mnemonic code has four meanings as follows.

Mnemonic only	Instruction execution only
Mnemonic with X	After instruction execution, X ↔ SPX
Mnemonic with Y	After instruction execution, Y ↔ SPY
Mnemonic with XY	After instruction execution, X ↔ SPX, Y ↔ SPY

[Example]

LAM	M → A
LAMX	M → A, X ↔ SPX
LAMY	M → A, Y ↔ SPY
LAMXY	M → A, X ↔ SPX, Y ↔ SPY

2. Status column shows the factor which brings the Status F/F "1" under judgement instruction or instruction accompanying the judgement.
   NZ .... ALU Not Zero
   C ..... ALU Overflow in Addition, that is, Carry
   NB .... ALU Overflow in Subtraction, that is, No Borrow
   Except above ..... Contents of the status column affects the Status F/F directly.

3. The Carry F/F (C(F/F)) is not always affected by executing the instruction which affects the Status F/F.
   Instructions which affect the Carry F/F are eight as follows.

AMC	SEC
SMC	REC
DAA	ROTL
DAS	ROTR

4. All instructions except the pattern instruction (P) are executed in 1-cycle. The pattern instruction (P) is executed in 2-cycle.

HMCS47C Mask Option List

Date	
Customer's Name	
ROM CODE ID	
Hitachi P/N	

(1) I/O Option

Pin Name	I/O	I/O Option			Remarks	Pin Name	I/O	I/O Option			Remarks
		A	B	C				A	B	C	
D_0	I/O					R_{00}	I/O				
D_1	I/O					R_{01}	I/O				
D_2	I/O					R_{02}	I/O				
D_3	I/O					R_{03}	I/O				
D_4	I/O					R_{10}	I/O				
D_5	I/O					R_{11}	I/O				
D_6	I/O					R_{12}	I/O				
D_7	I/O					R_{13}	I/O				
D_8	I/O					R_{20}	I/O				
D_9	I/O					R_{21}	I/O				
D_{10}	I/O					R_{22}	I/O				
D_{11}	I/O					R_{23}	I/O				
D_{12}	I/O					R_{30}	I/O				
D_{13}	I/O					R_{31}	I/O				
D_{14}	I/O					R_{32}	I/O				
D_{15}	I/O					R_{33}	I/O				
						R_{40}	I/O				
						R_{41}	I/O				
						R_{42}	I/O				
						R_{43}	I/O				
						R_{50}	I/O				
						R_{51}	I/O				
						R_{52}	I/O				
						R_{53}	I/O				
						R_{60}	O				
						R_{61}	O				
INT_0	I					R_{62}	O				
INT_1	I					R_{63}	O				

* Specify the I/O composition with a mark of "O" in the applicable composition column.
A: No pull up MOS B: With pull up MOS C: CMOS Output

(2) Oscillator & Halt

Oscillator \ Halt	Not used	Used (Reset is applied when Halt release)	Used (Reset is not applied when Halt release)
Resistor			
Ceramic Resonator			
External Clock			

* Please check one section on the above chart.

(3) I/O State at "Halt" mode

I/O State
□ Enable
□ Disable

* Mark "√" in "□" for the selected I/O state.

(4) Supply Voltage (V_{CC})

Supply Voltage (V_{CC})
□ 5 ± 0.5V
□ 2.5V to 5.5V

* Mark "√" in "□" for the selected supply voltage.

(5) Package

Package
□ FP-54
□ DP-64S

* Mark "√" in "□" for the selected package.

(6) Evchip used for Program Evaluation

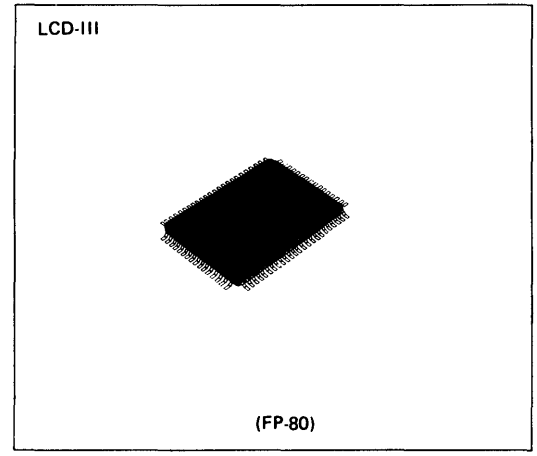
Evchip
□ HD44855E
□ HD44857E

* Mark "√" in "□" for the evchip used for program evaluation.

4-BIT SINGLE-CHIP MICROCOMPUTER HMCS40 SERIES LIQUID CRYSTAL DISPLAY DRIVING TYPE

LCD—III (HD44790, HD44795)

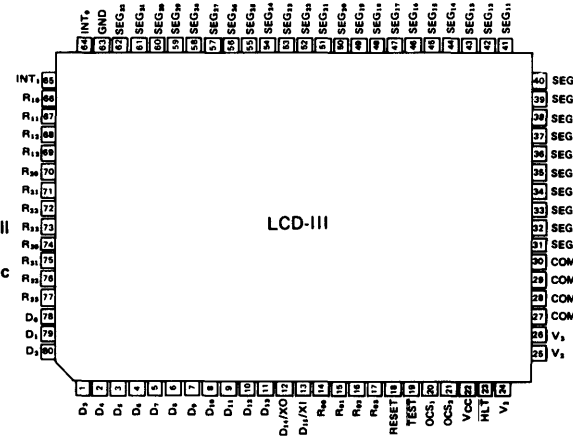
The LCD-III is the CMOS 4-bit single chip microcomputer which contains ROM, RAM, I/O, Timer/Event Counter and Control Circuit, Direct Drive Circuit for LCD on single chip. The LCD-III is designed to drive LCD directly and perform efficient controller function as well as arithmetic function for both binary and BCD data. With the on-chip crystal oscillator for timer, the clock function is easily realized. The CMOS technology of the LCD-III provides the flexibility of microcomputers for battery powered and battery back-up applications in combination with low power consuming LCD.



■ FEATURES

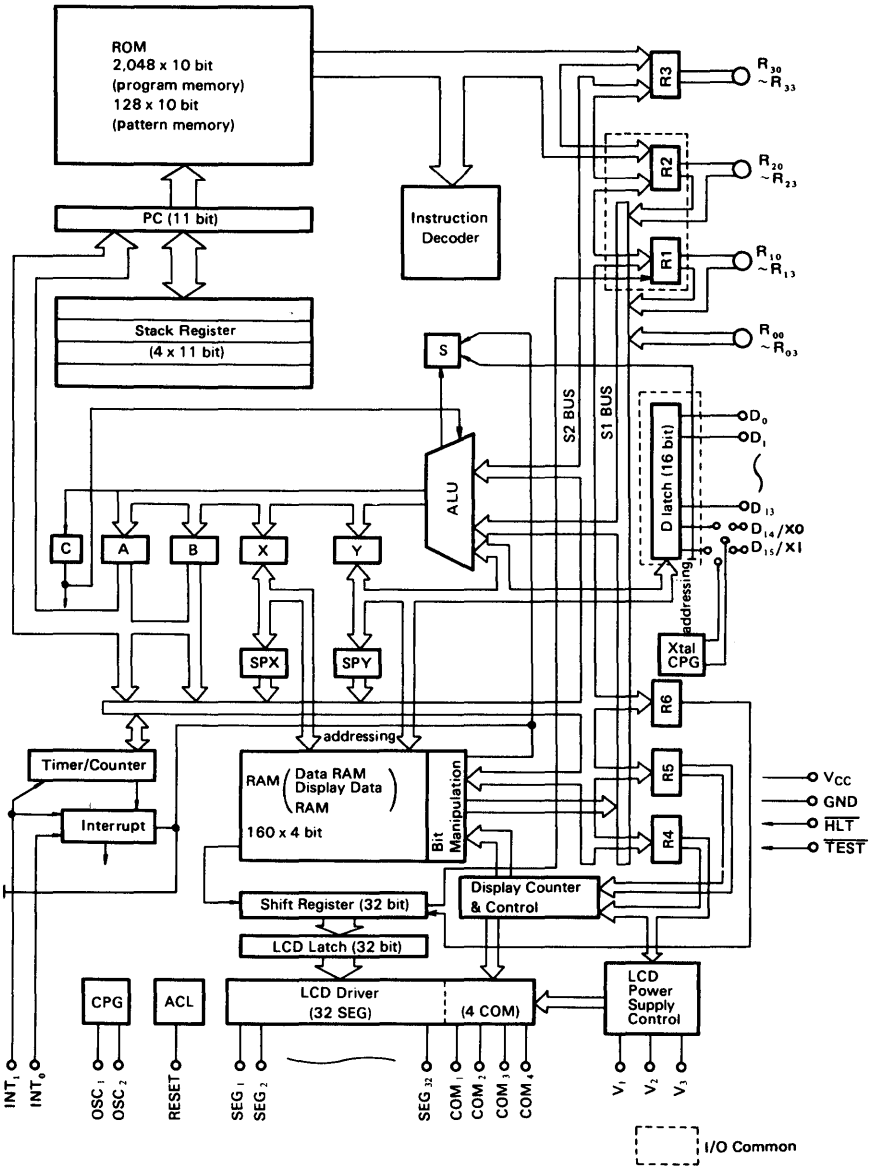
- 4-bit Architecture
- 2,048 Words of Program ROM (10 bits/Word)
  128 Words of Pattern ROM (10 bits/Word)
- 160 Digits of Data RAM and Display Data RAM (4 bits/Digit)
- Control Circuit and Direct Drive Circuit for LCD
  4 Commons (Duty Radio; Static, 1/2, 1/3, 1/4)
  32 Segments (Externally expandable up to 96 Segments using external Drivers HD44100s)
- 32 I/O Lines and 2 External Interrupt Lines
- Timer/Event Counter
- All Instructions except One Instruction; Single Word and Single Cycle
- BCD Arithmetic Instructions
- Pattern Generation Instruction
  – Table Look Up Capability –
- Powerful Interrupt Function
  3 Interrupt Sources
  ├ 2 External Interrupt Lines
  └ Timer/Event Counter
  Multiple Interrupt Capability
- Bit Manipulation Instructions for Both RAM and I/O
- Option of I/O Configuration Selectable on Each Pin; Pull Up MOS or CMOS or Open Drain
- Built-in Oscillator for System Clock (Resistor or Ceramic Filter)
- Built-in Crystal Oscillator for Timer
- Built-in Power-on Reset Circuit
- Low Operating Power Dissipation; 2mW typ.
- Stand-by Mode (Halt Mode); 50μW max.
- 2 Versions; HD44790 V_{CC} = 5V ± 10%, 10μs Instruction Cycle Time
  HD44795 V_{CC} = 2.7V to 5.5V, 20μs Instruction Cycle Time

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ HD44790 ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%)

• ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	-0.3 to +7.0	V	
Terminal Voltage (1)	V_{T1}	-0.3 to V_{CC}+0.3	V	Applied to all terminals except those specified in V_{T2}.
Terminal Voltage (2)	V_{T2}	0.3 to +10.0	V	Applied to open-drain output pins and open-drain I/O common pins.
Maximum Total Output Current (1)	$-\Sigma I_{o1}$	45	mA	(Note 3)
Maximum Total Output Current (2)	ΣI_{o2}	45	mA	(Note 3)
Operating Temperature	T_{opr}	-20 to +75	°C	
Storage Temperature	T_{stg}	-55 to +125	°C	

(NOTE) 1. Stresses above those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. Normal operation should be limited to those conditions specified under "ELECTRICAL CHARACTERISTICS -1" and "-2". The use beyond these conditions may cause LSI's malfunction and at the same time affects device reliability.
2. All voltages are with respect to GND.
3. Maximum Total Output Current is the total sum of output currents which can flow out or in simultaneously.
4. Power supply condition $V_{CC} \geqq V1 \geqq V2 \geqq V3 \geqq GND$ should be maintained.

• ELECTRICAL CHARACTERISTICS – 1 (V_{CC} = 5V±10%, T_a = -20 to +75°C)

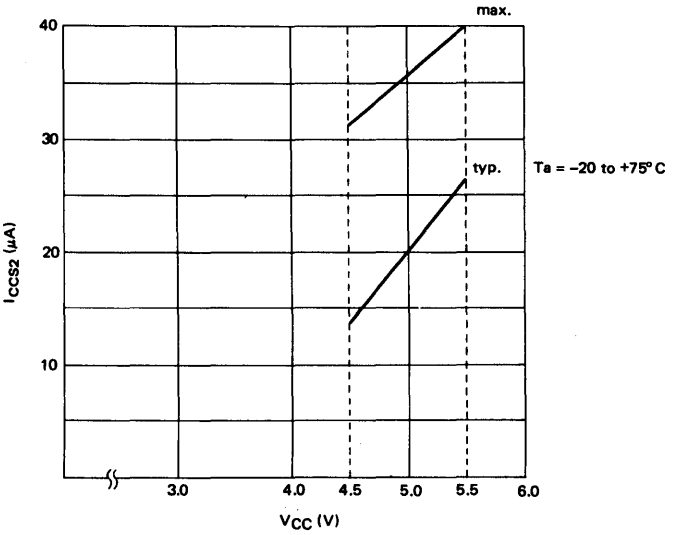
Item	Symbol	Test Conditions	Value min.	Value typ.	Value max.	Unit	Note
Input "Low" Voltage	V_{IL}		–	–	1.0	V	
Input "High" Voltage (1)	V_{IH1}		V_{CC}-1.0	–	V_{CC}	V	(9)
Input "High" Voltage (2)	V_{IH2}		V_{CC}-1.0	–	10	V	(10)
Output "Low" Voltage	V_{OL}	I_{OL} = 1.6 mA	–	–	0.8	V	
Output "High" Voltage (1)	V_{OH1}	$-I_{OH}$ = 1.0 mA	2.4	–	–	V	(1)
Output "High" Voltage (2)	V_{OH2}	$-I_{OH}$ = 0.01 mA	V_{CC}-0.3	–	–	V	(2)
Driver Voltage Descending (COM)	V_{d_1}	Id = 0.05 mA	–	–	0.4	V	(13)
Driver Voltage Descending (SEG)	V_{d_2}	Id = 0.01 mA	–	–	0.4	V	(13)
Dividing Resistor of LCD Power Supply	Rwell		25	–	300	kΩ	
Interrupt Input Hold Time	t_{INT}		$2 \cdot T_{inst}$	–	–	μs	(15)
Interrupt Input Fall Time	t_{fINT}		–	–	50	μs	(15)
Interrupt Input Rise Time	t_{rINT}		–	–	50	μs	(15)
Output "High" Current	I_{OH}	V_{OH} = 10V	–	–	3	μA	(3)
Input Leakage Current	I_{IL}	V_{in} = 0 to V_{CC}	–	–	1.0	μA	(3), (9)
		V_{in} = 0 to 10V	–	–	3		(3), (10)
Pull up MOS Current	$-I_P$	V_{CC} = 5V	45	–	250	μA	
Supply Current (1)	I_{CC1}	V_{in} = V_{CC}, V_{CC} = 5V, Ceramic Filter Oscillation (f_{osc} = 400 kHz)	–	–	1.3	mA	(5)
Supply Current (2)	I_{CC2}	V_{in} = V_{CC}, V_{CC} = 5V R_f Oscillation (f_{osc} = 400 kHz) External Clock Operation (f_{cp} = 400 kHz)	–	–	0.6	mA	(5), (12)
Standby I/O Leakage Current	I_{LS}	$\overline{HLT}$ = 1.0V, V_{in} = 0 to V_{CC}	–	–	1.0	μA	(6), (9)
		$\overline{HLT}$ = 1.0V, V_{in} = 0 to 10V	–	–	3	μA	(6), (10)
Standby Supply Current (1)	I_{CCS1}	V_{in} = V_{CC}, $\overline{HLT}$ = 0.2V	–	–	10	μA	(11)
Standby Supply Current (2)	I_{CCS2}	V_{in} = V_{CC}, $\overline{HLT}$ = 0.2V	–	–	40	μA	(7)
Frame Frequency of LCD Drive	f_F	n = 1 (static) n = 2 (1/2 Duty) n = 3 (1/3 Duty) n = 4 (1/4 Duty)	$\frac{1}{256 \times n \times T_{inst}}$			Hz	
LCD Display Voltage	V_{LCD}	V_{CC}-V_3	2.5	–	V_{CC}	V	(8)
External Clock Operation; System Clock							
External Clock Frequency	f_{cp}		40	400	440	kHz	
External Clock Duty	Duty		45	50	55	%	
External Clock Rise Time	t_{rcp}		0	–	0.2	μs	
External Clock Fall Time	t_{fcp}		0	–	0.2	μs	
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{cp}$	9.1	10	100	μs	
Internal Clock Operation (R_f Oscillation); System Clock							
Clock Oscillation Frequency	f_{osc}	R_f = 82 kΩ±2%	300	–	500	kHz	
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{osc}$	8.0	–	13.3	μs	
Internal Clock Operation (Ceramic Filter Oscillation); System Clock							
Clock Oscillation Frequency	f_{osc}	Ceramic Filter	392	–	408	kHz	
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{osc}$	9.8	–	10.2	μs	
Internal Clock Operation (Crystal Oscillation); Clock for Timer							
Clock Oscillation Frequency	f_{oscx}	Crystal	32.768			kHz	

• ELECTRICAL CHARACTERISTICS – 2 (T_a = -20 to +75°C)

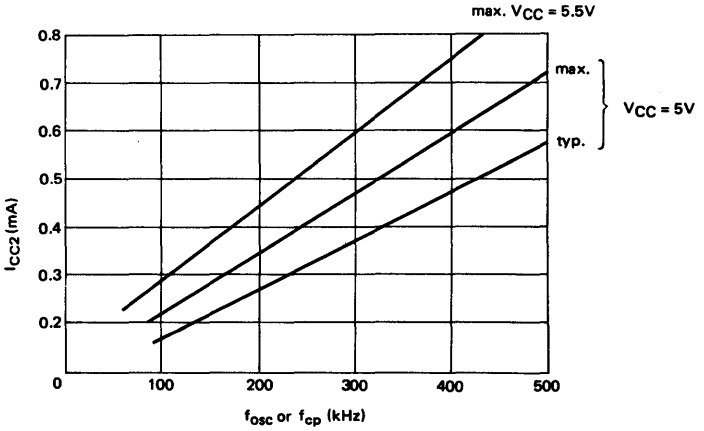
Item	Symbol	Test Conditions	Value min.	Value max.	Unit	Note
Halt Duration Voltage	V_{DH}	$\overline{HLT}$ = 0.2V	2.3	–	V	
Halt Current	I_{DH}	V_{in} = V_{CC}, $\overline{HLT}$ = 0.2V, V_{DH} = 2.3V	–	4.0	μA	(14)
Halt Delay Time	t_{HD}		100	–	μs	
Operation Recovery Time	t_{RC}		100	–	μs	
$\overline{HLT}$ Fall Time	t_{fHLT}		–	1000	μs	
$\overline{HLT}$ Rise Time	t_{rHLT}		–	1000	μs	
$\overline{HLT}$ "Low" Hold Time	t_{HLT}		400	–	μs	
$\overline{HLT}$ "High" Hold Time	t_{OPR}	R_f Oscillation, External Clock Operation	100	–	μs	
		Ceramic Filter Oscillation	4000	–		
Power Supply Rise Time	t_{rCC}	Built-in Reset, $\overline{HLT}$ = V_{CC}	0.1	10	ms	
Power Supply OFF Time	t_{OFF}	Built-in Reset, $\overline{HLT}$ = V_{CC}	1	–	ms	
RESET Pulse Width (1)	t_{RST1}	External Reset, V_{CC} = 4.5 to 5.5V, $\overline{HLT}$ = V_{CC} (R_f Oscillation, External Clock Operation)	1	–	ms	
		External Reset, V_{CC} = 4.5 to 5.5V, $\overline{HLT}$ = V_{CC} (Ceramic Filter Oscillation)	4	–		
RESET Pulse Width (2)	t_{RST2}	External Reset, V_{CC} = 4.5 to 5.5V, $\overline{HLT}$ = V_{CC}, (Prescaler Clock = System Clock)	$2 \cdot T_{inst}$	–	μs	
		External Reset, V_{CC} = 4.5 to 5.5V, $\overline{HLT}$ = V_{CC}, (Prescaler Clock = Crystal Clock)	$32 \times 10^6 / f_{oscx}$	–		
RESET Rise Time	t_{rRST}	External Reset, $\overline{HLT}$ = V_{CC}, V_{CC} = 4.5 to 5.5V	–	100	μs	
RESET Fall Time	t_{fRST}	External Reset, $\overline{HLT}$ = V_{CC}, V_{CC} = 4.5 to 5.5V	–	100	μs	

(NOTE) 1. Applied to PMOS load of CMOS output pins and CMOS I/O common pins among D and R terminals.
2. Applied to CMOS output pins, CMOS I/O common pins, input pins with pull up MOS, and I/O common pins with pull up MOS among D and R terminals.
3. Applied to open-drain output pins and open-drain I/O common pins among D and R terminals.
4. Pull up MOS current is excluded.
5. Applied to the supply current when the LCD-III is in the reset state and the crystal oscillation for timer doesn't operate. (Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded).
Test Condition: RESET, $\overline{HLT}$, $\overline{TEST}$ = V_{CC} (Reset State)
INT_0, INT_1, R_{00} to R_{33}, D_0 to D_{13} = V_{CC}
D_{14}/XO, D_{15}/XI ─┬─ D_{14}/XO, D_{15}/XI = V_{CC} (Crystal oscillation for timer is not selected).
└─ D_{14}/XO = Open, D_{15}/XI = V_{CC} (Crystal oscillation for timer is selected).
V_1, V_2, V_3 = V_{CC}
COM_1 to COM_4, SEG_1 to SEG_{32} = Open
When the crystal oscillation for timer operates, the standby supply current (2) I_{CCS2} flows in addition to I_{CC1} or I_{CC2}.
When the LCD-III is installed in the user's system, and in operation current increases according to the external circuitry and devices. Those are connected to the LCD-III. User should design the power supply in consideration of this point (The difference between the measured current in the above reset state and that measured in the operational state in the user's system is the increased part of the supply current).
6. Standby I/O leakage current is the leakage current of I/O pins in the "Halt" and "Disable" state.

7. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded. The standby supply current (2) is the supply current at V_{CC} = 5V±10% in "Halt" state in the case that the crystal oscillation for timer is selected (only the crystal oscillator for timer, 5-bit divider and 6-bit prescaler are in operation).

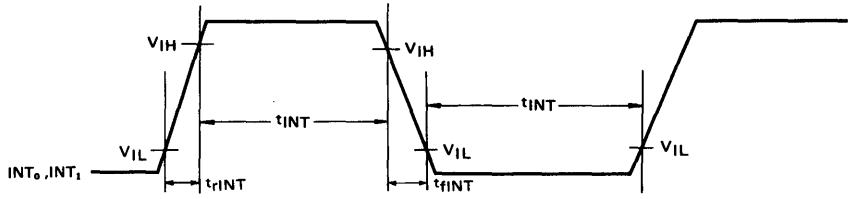


8. Power supply condition $V_{CC} \geqq V_1 \geqq V_2 \geqq V_3 \geqq GND$ should be maintained.
9. Applied to the following terminals.
   (1) Input pins, I/O common pins with pull up MOS, and CMOS I/O common pins among D and R terminals.
   (2) RESET, $\overline{HLT}$, OSC_1, INT_0 and INT_1
10. Applied to open-drain I/O common pins among D and R terminals.
11. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded. The standby supply current is the supply current at V_{CC} = 5V±10% in "Halt" state in the case that the crystal oscillation for timer is selected. The supply current when supply voltage falls to the Halt Duration Voltage is called "Halt Current" (I_{DH}).
12. The supply current changes as follows according to operating frequency.



13. The voltage that drops between the power supply terminals (V_{CC}, V_1, V_2, V_3) and each common or segment output terminal.
14. The supply current at V_{CC} = V_{DH} = 2.3V in "Halt" state, in the case that the crystal oscillation for timer is not selected. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded.

15. Interrupt inputs must be retained for two or more instruction cycle times at both "High" and "Low" levels.



■ HD44795 ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5V)

• ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	-0.3 to +7.0	V	
Terminal Voltage (1)	V_{T1}	-0.3 to V_{CC}+0.3	V	Applied to all terminals except those specified in V_{T2}.
Terminal Voltage (2)	V_{T2}	0.3 to +10.0	V	Applied to open-drain output pins and open-drain I/O common pins.
Maximum Total Output Current (1)	$-\Sigma I_{o1}$	45	mA	(Note 3)
Maximum Total Output Current (2)	ΣI_{o2}	45	mA	(Note 3)
Operating Temperature	T_{opr}	-20 to +75	°C	
Storage Temperature	T_{stg}	-55 to +125	°C	

(NOTE) 1. Stresses above those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. Normal operation should be limited to those conditions specified under "ELECTRICAL CHARACTERISTICS -1" and "-2". The use beyond these conditions may cause LSI's malfunction and at the same time affects device reliability.
2. All voltages are with respect to GND.
3. Maximum Total Output Current is the total sum of output currents which can flow out or in simultaneously.
4. Power supply condition $V_{CC} \geqq V1 \geqq V2 \geqq V3 \geqq GND$ should be maintained.

• ELECTRICAL CHARACTERISTICS – 1 (V_{CC} = 2.7 to 5.5V, T_a = -20 to +75°C)

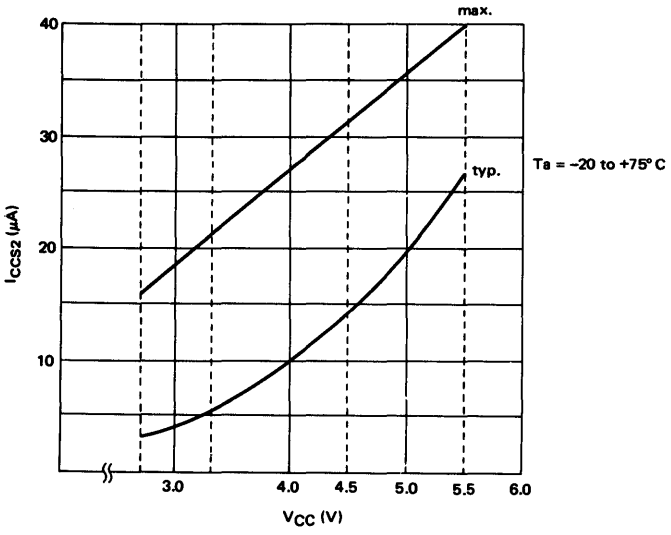
Item	Symbol	Test Conditions	Value min.	Value typ.	Value max.	Unit	Note
Input "Low" Voltage	V_{IL}		–	–	0.4	V	
Input "High" Voltage (1)	V_{IH1}		V_{CC}-0.4	–	V_{CC}	V	(9)
Input "High" Voltage (2)	V_{IH2}		V_{CC}-0.4	–	10	V	(10)
Output "Low" Voltage	V_{OL}	I_{OL} = 0.4 mA	–	–	0.4	V	
Output "High" Voltage (1)	V_{OH1}	$-I_{OH}$ = 0.08 mA	V_{CC}-0.4	–	–	V	(1)
Output "High" Voltage (2)	V_{OH2}	$-I_{OH}$ = 0.01 mA	V_{CC}-0.3	–	–	V	(2)
Driver Voltage Descending (COM)	V_{d_1}	Id = 0.05 mA	–	–	0.4	V	(13)
Driver Voltage Descending (SEG)	V_{d_2}	Id = 0.01 mA	–	–	0.4	V	(13)
Dividing Resistor of LCD Power Supply	Rwell		25	–	300	kΩ	
Interrupt Input Hold Time	t_{INT}		$2 \cdot T_{inst}$	–	–	μs	(15)
Interrupt Input Fall Time	t_{fINT}		–	–	50	μs	(15)
Interrupt Input Rise Time	t_{rINT}		–	–	50	μs	(15)
Output " High" Current	I_{OH}	V_{OH} = 10V	–	–	3	μA	(3)
Input Leakage Current	I_{IL}	V_{in} = 0 to V_{CC}	–	–	1.0	μA	(3), (9)
		V_{in} = 0 to 10V	–	–	3		(3), (10)
Pull up MOS Current	$-I_P$	V_{CC} = 3V	15	–	80	μA	
Supply Current	I_{CC}	V_{in} = V_{CC}, V_{CC} = 3V R_f Oscillation (f_{osc} = 200 kHz) External Clock Operation (f_{cp} = 200 kHz)	–	–	0.15	mA	(5), (12)
Standby I/O Leakage Current	I_{LS}	$\overline{HLT}$ = 1.0V, V_{in} = 0 to V_{CC}	–	–	1.0	μA	(6), (9)
		$\overline{HLT}$ = 1.0V, V_{in} = 0 to 10V	–	–	3	μA	(6), (10)
Standby Supply Current (1)	I_{CCS1}	V_{in} = V_{CC}, $\overline{HLT}$ = 0.1V V_{CC} = 2.7 to 3.3V	–	–	6	μA	(11)
Standby Supply Current (2)	I_{CCS2}	V_{in} = V_{CC}, $\overline{HLT}$ = 0.1V V_{CC} = 2.7 to 3.3V	–	–	21	μA	(7)
Frame Frequency of LCD Drive	f_F	n = 1 (static) n = 2 (1/2 Duty) n = 3 (1/3 Duty) n = 4 (1/4 Duty)	$\frac{1}{128 \times n \times T_{inst}}$			Hz	
LCD Display Voltage	V_{LCD}	V_{CC}-V_3	2.5	–	V_{CC}	V	(8)
External Clock Operation; System Clock							
External Clock Frequency	f_{cp}		40	200	220	kHz	
External Clock Duty	Duty		45	50	55	%	
External Clock Rise Time	t_{rcp}		0	–	0.2	μs	
External Clock Fall Time	t_{fcp}		0	–	0.2	μs	
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{cp}$	16.6	20	100	μs	
Internal Clock Operation (R_f Oscillation); System Clock							
Clock Oscillation Frequency	f_{osc}	R_f = 200kΩ±2%, V_{CC} = 2.7 to 3.3V	150	–	250	kHz	
		R_f = 200kΩ±2%, V_{CC} = 2.7 to 5.5V	150	–	350		
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{osc}$, V_{CC} = 2.7 to 3.3V	16	–	26.6	μs	
		$T_{inst} = 4/f_{osc}$, V_{CC} = 2.7 to 5.5V	11.4	–	26.6		
Internal Clock Operation (Crystal Oscillation); Clock for Timer							
Clock Oscillation Frequency	f_{oscx}	Crystal		32.768		kHz	

- **ELECTRICAL CHARACTERISTICS – 2 (T_a = -20 to +75°C)**

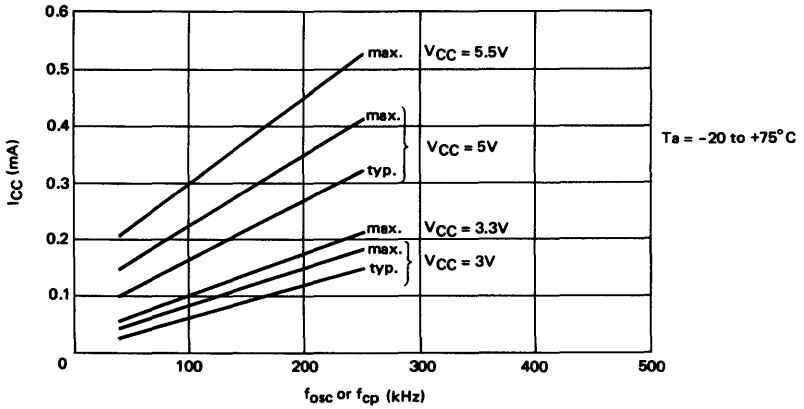
Item	Symbol	Test Conditions	Value min.	Value max.	Unit	Note
Halt Duration Voltage	V_{DH}	$\overline{HLT}$ = 0.1V	2.3	–	V	
Halt Current	I_{DH}	$V_{in} = V_{CC}$, $\overline{HLT}$ = 0.1V, V_{DH} = 2.3V	–	4.0	μA	(14)
Halt Delay Time	t_{HD}		100	–	μs	
Operation Recovery Time	t_{RC}		100	–	μs	
$\overline{HLT}$ Fall Time	t_{fHLT}		–	1000	μs	
$\overline{HLT}$ Rise Time	t_{rHLT}		–	1000	μs	
$\overline{HLT}$ "Low" Hold Time	t_{HLT}		400	–	μs	
$\overline{HLT}$ "High" Hold Time	t_{OPR}	R_f Oscillation, External Clock Operation	100	–	μs	
Power Supply Rise Time	t_{rCC}	Built-in Reset, $\overline{HLT} = V_{CC}$	0.1	10	ms	
Power Supply OFF Time	t_{OFF}	Built-in Reset, $\overline{HLT} = V_{CC}$	1	–	ms	
RESET Pulse Width (1)	t_{RST1}	External Reset, $\overline{HLT} = V_{CC}$	1	–	ms	
RESET Pulse Width (2)	t_{RST2}	External Reset, V_{CC} = 2.7 to 5.5V, $\overline{HLT} = V_{CC}$, (Prescaler Clock = System Clock)	$2 \cdot T_{inst}$	–	μs	
		External Reset, V_{CC} = 2.7 to 5.5V, $\overline{HLT} = V_{CC}$, (Prescaler Clock = Crystal Clock)	$32 \times 10^6 / f_{oscx}$	–		
RESET Rise Time	t_{rRST}	External Reset, $\overline{HLT} = V_{CC}$, V_{CC} = 2.7 to 5.5V	–	100	μs	
RESET Fall Time	t_{fRST}	External Reset, $\overline{HLT} = V_{CC}$, V_{CC} = 2.7 to 5.5V	–	100	μs	

(NOTE)
1. Applied to PMOS load of CMOS output pins and CMOS I/O common pins among D and R terminals.
2. Applied to CMOS output pins, CMOS I/O common pins, input pins with pull up MOS, and I/O common pins with pull up MOS among D and R terminals.
3. Applied to open-drain output pins and open-drain I/O common pins among D and R terminals.
4. Pull up MOS current is excluded.
5. Applied to the supply current when the LCD-III is in the reset state and the crystal oscillation for timer doesn't operate (Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded).
   Test Condition: RESET, $\overline{HLT}$, $\overline{TEST}$ = V_{CC} (Reset State)
   INT_0, INT_1, R_{00} to R_{33}, D_0 to D_{13} = V_{CC}
   D_{14}/XO, D_{15}/XI ┬ D_{14}/XO, D_{15}/XI = V_{CC} (Crystal oscillation for timer is not selected)
   D_{14}/XO, D_{15}/XI ┴ D_{14}/XO = Open, D_{15}/XI = V_{CC} (Crystal oscillation for timer is selected).
   V_1, V_2, V_3 = V_{CC}
   COM_1 to COM_4, SEG_1 to SEG_{32} = Open
   When the crystal oscillation for timer operates, the standby supply current (2) I_{CCS2} flows in addition to I_{CC}.
   When the LCD-III is installed in the user's system, and in operation current increases according to the external circuitry and devices. Those are connected to the LCD-III. User should design the power supply in consideration of this point (The difference between the measured current in the above reset state and that measured in the operational state in the user's system is the increased part of the supply current).
6. Standby I/O leakage current is the leakage current of I/O pins in the "Halt" and "Disable" state.

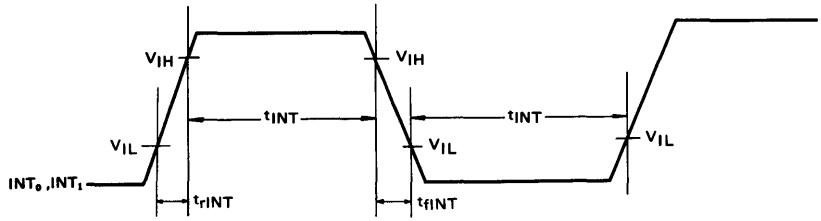
7. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded. The standby supply current (2) is the supply current at V_{CC} = 3V±10% in "Halt" state in the case that the crystal oscillation for timer is selected (only the crystal oscillator for timer, 5-bit divider and 6-bit prescaler are in operation).



8. Power supply condition $V_{CC} \geqq V_1 \geqq V_2 \geqq V_3 \geqq GND$ should be maintained.
9. Applied to the following terminals.
   (1) Input pins, I/O common pins with pull up MOS, and CMOS I/O common pins among D and R terminals.
   (2) RESET, $\overline{HLT}$, OSC_1, INT_0 and INT_1
10. Applied to open-drain I/O common pins among D and R terminals.
11. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded. The standby supply current is the supply current at V_{CC} = 3V±10% in "Halt" state in the case that the crystal oscillation for timer is selected. The supply current when supply voltage falls to the Halt Duration Voltage is called "Halt Current" (I_{DH}).
12. The supply current changes as follows according to operating frequency.



13. The voltage that drops between the power supply terminals (V_{CC}, V_1, V_2, V_3) and each common or segment output terminal.
14. The supply current at $V_{CC} = V_{DH} = 2.3V$ in "Halt" state, in the case that the crystal oscillation for timer is not selected. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded.
15. Interrupt inputs must be retained for two or more instruction cycle time at both "High" and "Low" levels.



■ SIGNAL DESCRIPTION

The input and output signals for the LCD-III shown in PIN ARRANGEMENT are described in the following paragraphs.

• V_{CC} and GND

Power is supplied to the LCD-III using these two pins. V_{CC} is power and GND is the ground connection.

• RESET

This pin allows resetting of the LCD-III at times other than the automatic resetting capability (ACL; Built-in Reset Circuit) already in the LCD-III. The LCD-III can be reset by pulling RESET High.

Refer to RESET FUNCTION for additional information.

• OSC_1 and OSC_2

These pins provide control input for the on-chip clock oscillator circuit. A resistor, a ceramic filter circuit, or an external oscillator can be connected to these pins to provide a system clock with various degrees of stability/cost tradeoffs. Lead length and stray capacitance on these two pins should be minimized.

Refer to OSCILLATOR for recommendations about these pins.

• $\overline{HLT}$

This pin is used to place the LCD-III in the HALT state (Stand-by Mode). The LCD-III can be moved into the halt state by pulling $\overline{HLT}$ Low.

In the halt state the internal clock stops and all the internal status (RAM, Registers, Carry, Status, Program Counter, and all the internal statuses) are maintained. Consequently power consumption is greatly reduced. By pulling $\overline{HLT}$ high, the LCD-III starts operation from the status just before the halt state.

Refer to HALT FUNCTION for details of halt mode.

• $\overline{TEST}$

This pin is not for user application and must be connected to V_{CC}.

• INT_0 and INT_1

These pins provide the capability for asynchronously applying an external interrupt to the LCD-III.

Refer to INTERRUPTS for additional information.

• V_1, V_2 and V_3

Power for liquid crystal display are supplied to the LCD-III using these pins ($V_{CC} \geqq V_1 \geqq V_2 \geqq V_3 \geqq GND$).

• R_{00} to R_{03}

These four lines are a 4-bit input channel.

Refer to INPUT/OUTPUT for additional information.

• R_{10} to R_{13}, R_{20} to R_{23}

These 8 lines are arranged into two 4-bit Input/Output common channels.

4-bit registers (data I/O register) are attached to these channels. Each channel is directly addressed by the operand of an instruction. I/O configuration of each pin can be specified among Open Drain, With Pull Up MOS, and CMOS using a mask option.

Refer to INPUT/OUTPUT for additional information.

• R_{30} to R_{33}

These four lines are a 4-bit output channel.

4-bit register is attached to this channel. This channel is directly addressed by the operand of an instruction. I/O configuration of each pin can be specified among Open Drain and CMOS using a mask option.

Refer to INPUT/OUTPUT for additional information.

• D_0 to D_{13}

These are 14 discrete signals which can be configured as Input/Output lines.

Refer to INPUT/OUTPUT for additional information.

• D_{14}/XO, D_{15}/XI

D_{14}/XO and D_{15}/XI require a mask option in the following 3 types.

- Discrete I/O (common terminal)
- Crystal circuit connecting terminals (with internal halt)
- Crystal circuit connecting terminals (no internal halt)

Refer to INPUT/OUTPUT for additional information.

• COM_1 to COM_4

These pins are common terminals for liquid crystal display.

Refer to LIQUID CRYSTAL DISPLAY for additional information.

• SEG_1 to SEG_{32}

These pins are segment terminals for liquid crystal display.

Refer to LIQUID CRYSTAL DISPLAY for additional information.

■ OSCILLATOR

A resistor, a ceramic filter circuit or an external oscillator can be connected to OSC_1 and OSC_2. However, a ceramic filter circuit cannot be used on the HD44795. The oscillator frequency is initially divided by four to produce the initial system clock. The different connection methods are shown in Figure 1.

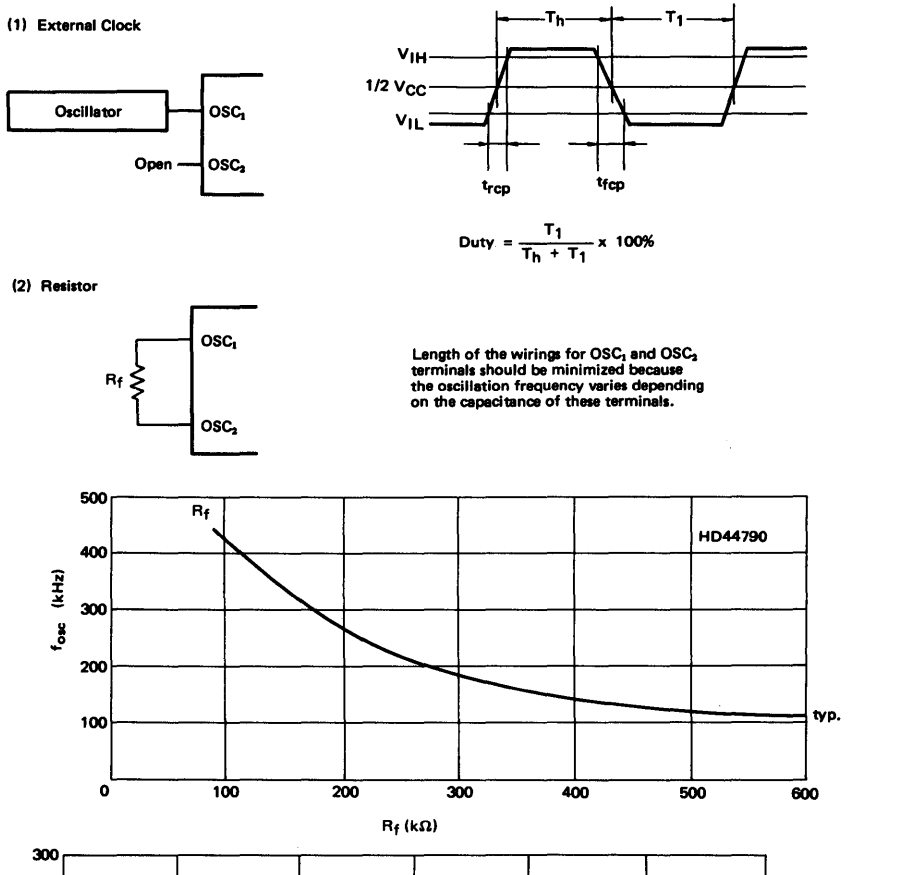
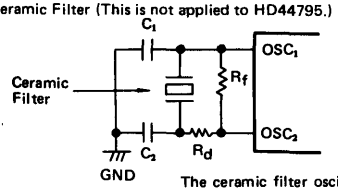


Figure 1 Connection Methods for Oscillator (to be continued)

(3) Ceramic Filter (This is not applied to HD44795.)



Ceramic Filter: CSB400P (MURATA)
R_f : 1MΩ ± 10%
C_1 : 330pF ± 10% (ceramic capacitor)
C_2 : 330pF ± 10% (ceramic capacitor)
R_d : 2.2kΩ ± 10%

The ceramic filter oscillation does not apply when using "Halt" and not resetting at the time of "Halt" cancellation.
This circuit is the example of the typical use. As the oscillation characteristics is not guaranteed, please consider and examine the circuit constant carefully on your application.

Figure 1 Connection Methods for Oscillator

■ ROM

ROM is used as program and pattern (constants) memory. The instruction used in the LCD-III consists of 10 bits.

The pattern area is in pages 61 and 62. No program can be stored in this area. The area is only used to store patterns (constants) that are referred in programs by user.

The program area (instructions can be programmed) consists of 2,048 words (64 x 32) of pages 0 through 31. In this area, either of programs or patterns can be stored.

Table 1 ROM Capacity

Program Area	32 pages
Pattern Area	2 pages
Total Number of the words	2,176 words

(NOTE) 1 page = 64 words

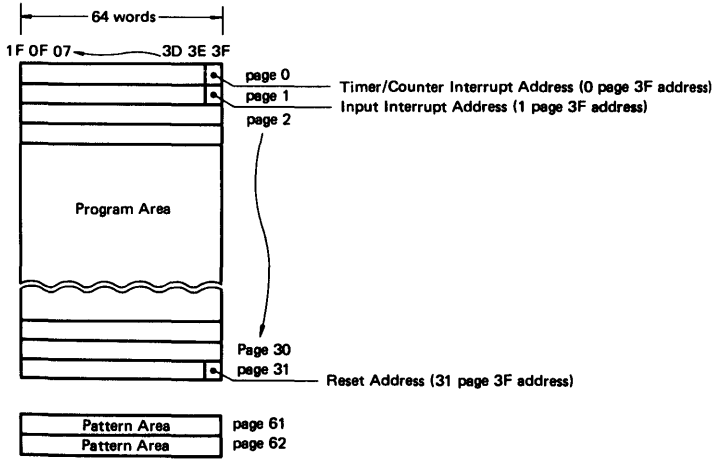


Figure 2 ROM Address Space

■ PROGRAM COUNTER (PC)

PC is the counter for addressing the program area of ROM. It consists of the page part and the address part as shown in Figure 3.

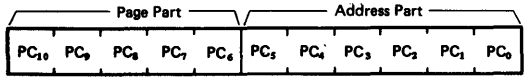


Figure 3 PC Structure

- **Page Part (5-bit register)**

Once a certain value is loaded into a page part, the content is unchanged until other value is loaded by the program. The settable value of a page part is any number from 0 through 31.

- **Address Part (6-bit counter)**

The address part consists of a random sequential counter and this counter counts up for each word, that is, one instruction cycle. All instructions except the pattern instruction are executed in one instruction cycle. (While the pattern instruction is executed in two cycles.)

The sequence indicated in decimal and hexa-decimal is shown in Table 2. This sequence forms a loop and has neither the starting nor ending points. It generates no overflow carry. Therefore, instructions on a same page are executed step by step unless the content of the page part of PC is unchanged.

Table 2 Sequence of the PC Address Part

Decimal	Hex-decimal	Decimal	Hex-decimal	Decimal	Hex-decimal
63	3F	5	05	9	09
62	3E	11	0B	19	13
61	3D	23	17	38	26
59	3B	46	2E	12	0C
55	37	28	1C	25	19
47	2F	56	38	50	32
30	1E	49	31	37	25
60	3C	35	23	10	0A
57	39	6	06	21	15
51	33	13	0D	42	2A
39	27	27	1B	20	14
14	0E	54	36	40	28
29	1D	45	2D	16	10
58	3A	26	1A	32	20
53	35	52	34	0	00
43	2B	41	29	1	01
22	16	18	12	3	03
44	2C	36	24	7	07
24	18	8	08	15	0F
48	30	17	11	31	1F
33	21	34	22		
2	02	4	04		

■ PATTERN GENERATION

The pattern (constants) can be assigned into ROM for user's reference in program. It can be written both in the program area and the pattern area.

Pattern reference is performed by the instruction of pattern (P) in the program.

ROM Addressing for the pattern reference is performed by modifying PC with A, B, C (F/F), and the operand p. The modifying scheme is shown in Figure 4. The address part is replaced by the contents of A (Accumulator) and the lower bits of B. The page part is logically ORed with the PC, the upper 2 bits of the operand is for referring to the pattern area. When the upper bit is preset to 1, the pattern area is referred, and it is preset to 0, the program area is referred. Non-existing ROM area can not be referred.

The value of PC is only modified apparently and is not changed. Then the address is counted up after the execution of P instruction and the next instruction is executed. The execution time of this instruction is 2-cycle time. Moreover, an instruction just after this instruction is masked.

The bit pattern of referred ROM address is generated by two ways.

(i) The pattern is taken into A and B.

(ii) The pattern is taken into the output ports R2 and R3.

The difference is determined by the command bits (O_9, O_{10}) in the pattern. Mode (i) is performed when O_9 is "1" and mode (ii) is performed when O_{10} is "1". Mode (i) and (ii) are simultaneously performed when both O_9 and O_{10} are "1". The correspondence of each bit of the pattern is shown in Figure 5.

In the program run, the pattern can not be distinguished from the instruction. When the program is running at the address written as a pattern by user, the instruction corresponding to the pattern bit is executed.

Therefore, when the pattern is written in the pattern area, the instruction must not be executed.

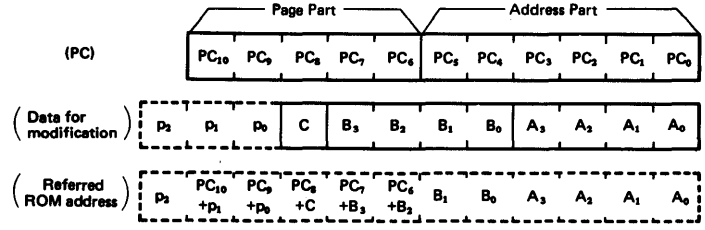


Figure 4 ROM Addressing for Pattern Reference

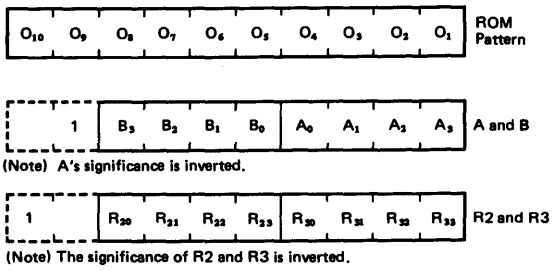


Figure 5 Correspondence of Each Bit of the Pattern

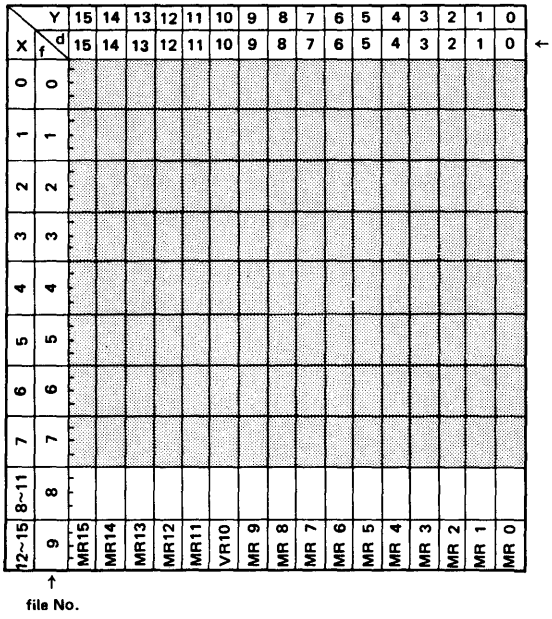
■ RAM (RANDOM ACCESS MEMORY)

RAM is the memory used for data storage and register save (data RAM) and storage of segment data for liquid crystal display (display data RAM). One unit (digit) consists of 4 bits and there is a total of 160 digits (640 bits).

(NOTE) Capacity of display data RAM varies by contents of display, and capacity of data RAM changes corresponding to the former.

Addressing of RAM is performed by the matrix of the file number and the digit number. There are 10 files and 16 digits in the matrix. Normally the file No. is set to X and the digit No. is set to Y, then the matrix of X and Y addresses RAM and performs the Read/Write operation.

Special digits in RAM can be addressed without the use of X and Y. These digits are called as memory register (MR) and the number is 16 (MR0 to MR15). Memory register can be exchanged for A register By XAMR instruction. RAM address space is shown in Figure 6.

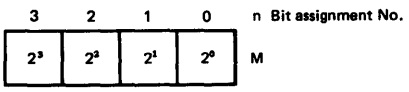


* The area market as ☐ is usable only for data.
* The data marked as ▨ is usable for both data and display.
* The file 8 is selected when X register has any value in 8 to 11, and the file 9 is selected when 12 to 15.

Figure 6 RAM Address Space

In case of the instructions which consist of a simultaneous Read/Write operations of RAM (exchange of RAM and a register), the writing data doesn't affect the reading data because the read operation is followed by the write operation.

RAM bit manipulation is usable, which performs any bit set, reset or test of the addressed RAM. Bit assignment is made by the program as shown below.



The bit test makes the status "1" when the assigned bit is "1" and makes it "0" when the assigned bit is "0".

■ REGISTERS

The LCD-III has six 4-bit registers and two 1-bit registers available to the programmer. 1-bit registers are Carry F/F and Status F/F. They are explained in the following paragraphs.

• Accumulator (A; A Register) and Carry F/F (C)

The result of ALU operation (4 bits) and the overflow of the ALU are put into the accumulator and Carry F/F. Carry F/F can be set, reset or tested. Combination of the accumulator and Carry F/F can be right or left rotated. The accumulator is the main register for ALU operation and Carry F/F is used to store the overflow generated by ALU operation when the calculation of two or more digits (4 bits/digit) is performed.

• B Register (B)

The result of ALU operation (4 bits) is put into this register. B register is used as a sub-accumulator to stack the data temporarily and also used as a counter.

• X Register (X)

The result of ALU operation (4 bits) is put into this register. X register has exchangeability for SPX register. X register addresses the RAM file.

• SPX Register (SPX)

SPX register has exchangeability for X register. SPX register is used to stack X register and expand the addressing system of RAM in combination with X register.

• Y Register (Y)

The result of ALU operation (4 bits) is put into this register. Y register has exchangeability for SPY register. Y register can calculate itself simultaneously with transferring the data by bus lines, which is usable for the calculation of two or more digits (4 bits/digit). Y register addresses the RAM digit and 1-bit discrete input/output common terminals.

• SPY Register (SPY)

SPY register has exchangeability for Y register. SPY register is used to stack Y register and expand the addressing system of RAM and 1-bit discrete input/output common terminals in combination with Y register.

• Status F/F (S)

Status F/F latches the result of logical or arithmetic operations (Not Zero, Overflow) and bit test operations. Status F/F affects conditional instructions (LPU, BR and CAL). These instructions are executed only when Status F/F is "1". If it is "0", these instructions are skipped and Status F/F becomes "1".

■ INPUT/OUTPUT

• Discrete I/O (D Terminal)

The discrete I/O is composed of 1-bit latch and I/O pin. Figure 7 shows the basic block diagram.

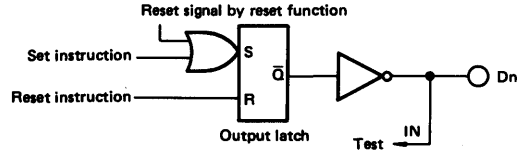


Figure 7 Discrete I/O Block Diagram

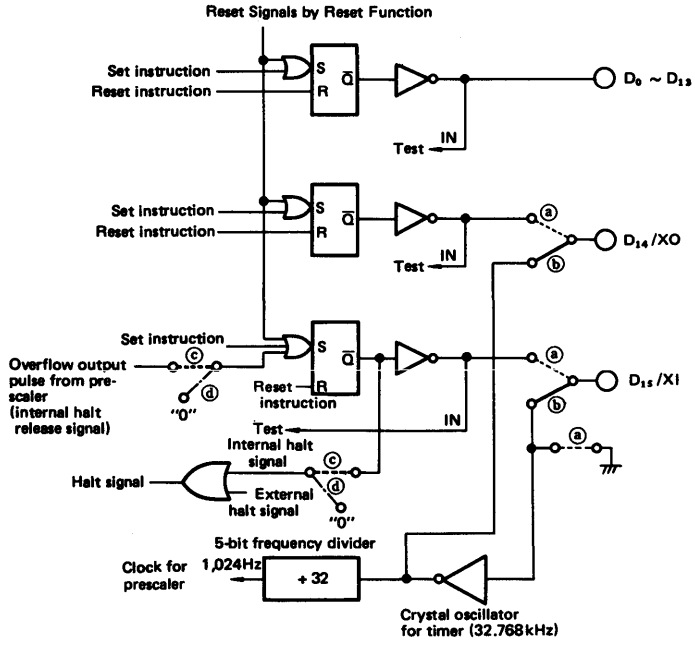


Figure 8 Mask Option of D_{14} and D_{15} Terminals

D_0 to D_{13} are discrete I/O's of common for input and output, D_{14} and D_{15} require a mask option in 3 types. When the crystal oscillation for timer is selected and the latches of D_{14} and D_{15} are not connected to the terminals, D_{14} and D_{15} can be used as 1-bit general purpose registers that can be set, reset and tested. Furthermore, if there is internal halt mode, latch of D_{15} is used as a register for internal halt mode specially.

In such case, since D_{15} means internal halt state and D_{15} = "1" means operating state, LSI can be in internal halt state by resetting D_{15} using an instruction. The prescaler keeps its operation in internal halt state. Therefore, D_{15} may be set by overflow output pulse from the prescaler to return to operating state. Refer to HALT FUNCTION for details of internal halt mode.

Table 3 Mask Option of D_{14}/XO and D_{15}/XI Terminals

Mask Option			a	b	c	d	Function of D_{14}/XO and D_{15}/XI	Function of D_{14}/XO and D_{15}/XI latch
1	Unselectable crystal oscillation for timer (no internal halt)		short	open	open	short	discrete I/O (common terminal)	Output Latch
2	Selectable crystal oscillation for timer	with internal halt	open	short			Crystal Circuit Connecting Terminal	1-bit register
3		no internal halt						D_{14} ; 1-bit register D_{15} ; register for internal halt

(NOTE) Users can specify this mask option in "The format of I/O channels" at ROM order.

Discrete I/O is addressed by Y register, and the set/reset instruction is executed for the addressed latch. "0" and "1" level can be tested with the addressed terminal and 1-bit register against the I/O common pins and 1-bit register. The test is performed with the wired logic of the output latch and the pin input. Therefore, in the case of the I/O common pins, the output latch should be in the high impedance state when the test instruction is executed. In order to test the pin input, it is necessary the state that the output latch should not affect the pin input.

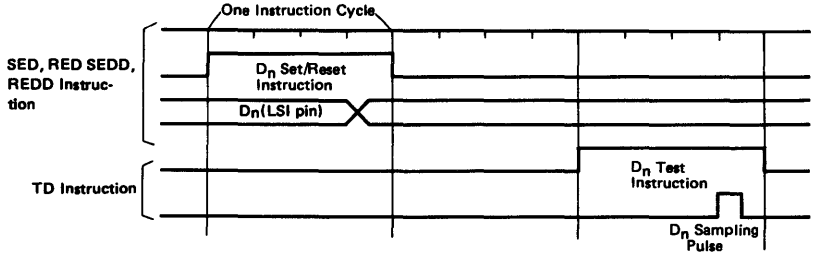


Figure 9 Timing Chart of Discrete I/O

- **Data I/O (R Terminal)**

Table 4 Data I/O for the LCD-III

I/O common channel	R1, R2 (2 channels)
Input channel	R0 (1 channel)
Output channel	R3 (1 channel)
Total	4 channels

(NOTE) In addition to the above, R4, R5 and R6 are provided as register setting liquid crystal display mode. In these registers, there is no terminal and exists only data I/O register each, which controls liquid crystal display mode. Data is transferred to R4, R5 and R6 by LRA or LRB instruction, same as data transfer to data I/O registers of R1, R2 and R3. For details of R4, R5 and R6, refer to LIQUID CRYSTAL DISPLAY.

4-bit register (data I/O register) each is attached to an I/O common channel and output channel. No register is attached to input channel. Addressing to all channels is performed by programs (addressed by operands in instructions).

Figure 10 shows the block diagram of each channel.

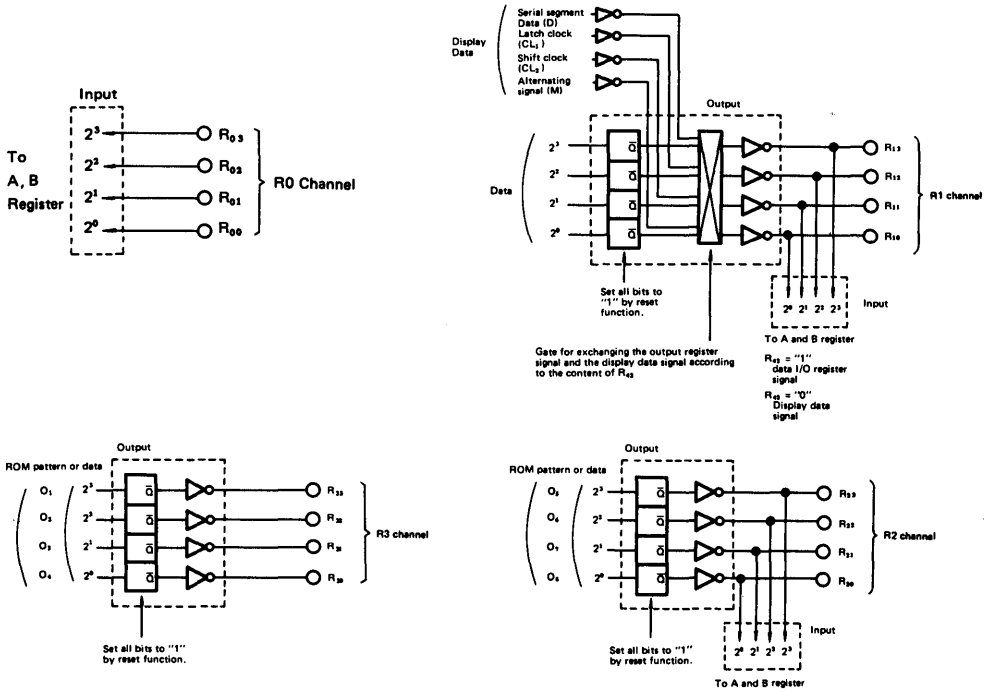


Figure 10 Data I/O Block Diagram

When expansion of segment signal for liquid crystal display is designated by a program (Register R_{42} = "0"), R1 is used as a display data output terminal. This prohibits R1 to be used as an I/O common channel by users (Refer to Figure 10, R1 channel).

If LRA or LRB instruction is executed at the time, data is transferred to data I/O register, but the content of data I/O register is not output from R1. If LAR or LBR instruction is executed, display data is inputted to accumulator (A register) or B register.

Data is transferred from the accumulator (A register) and B register to data I/O registers R1, R2, and R3 through the bus line. In addition, ROM bit patterns can be transferred to R2 and R3 by pattern generation instructions.

4-bit data can be inputted to the accumulator (A register) and B register from R0, R1 and R2 channels by input instructions. However, in the case of I/O common channels R2 and R3, since data I/O register outputs are connected to terminals, inputs are done to wired logic of register output and terminal input information. For this reason, to input terminal input signal, registers must be set to a state that would not affect the terminal input.

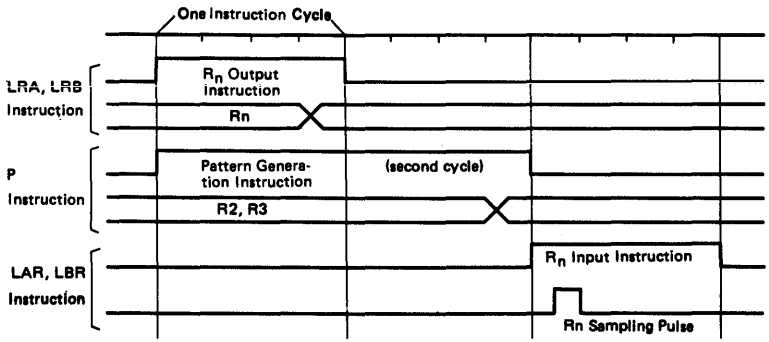
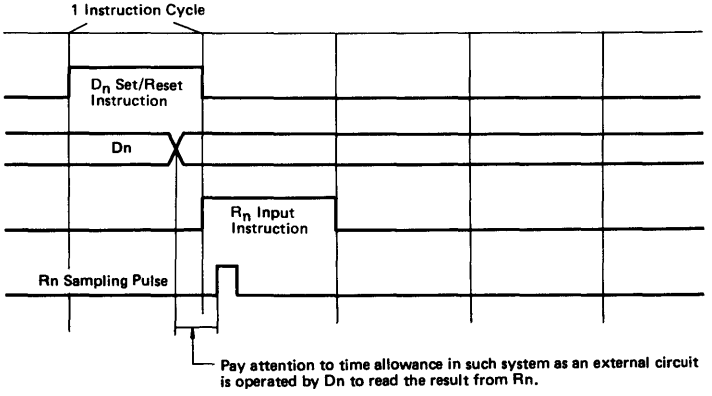


Figure 11 Data I/O Timing Chart

Pay attention: When executing an input instruction to output channel, the microcomputer reads unstabilized value causing malfunction of the program.

When executing an input instruction (LAR and LBR) from the data I/O, pay attention to time allowance after executing an output instruction. At the time, the input sampling pulse is generated during the first half of the instruction cycle.



Applied Pins: INT_0, INT_1, R_{00} to R_{03}

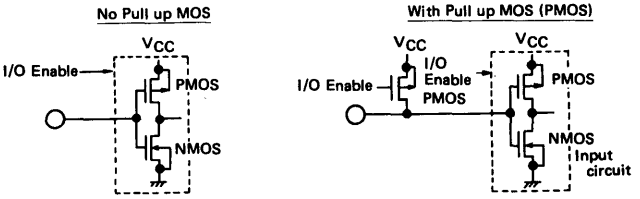


Figure 12 Configuration of Input Pins

Applied Pins: R_{30} to R_{33}

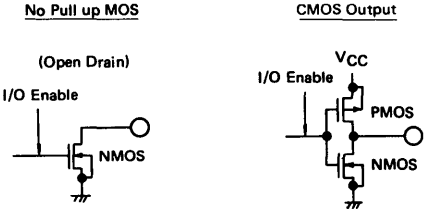
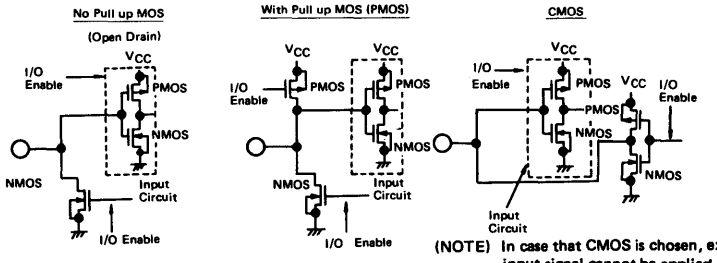


Figure 13 Configuration of Output Pins

Applied Pins: D_0 to D_{13}, D_{14}/XO, D_{15}/XI, R_{10} to R_{13}, R_{20} to R_{23}



(NOTE) In case that CMOS is chosen, external input signal cannot be applied.

Figure 14 Configuration of Input/Output Pins

■ TIMER/COUNTER

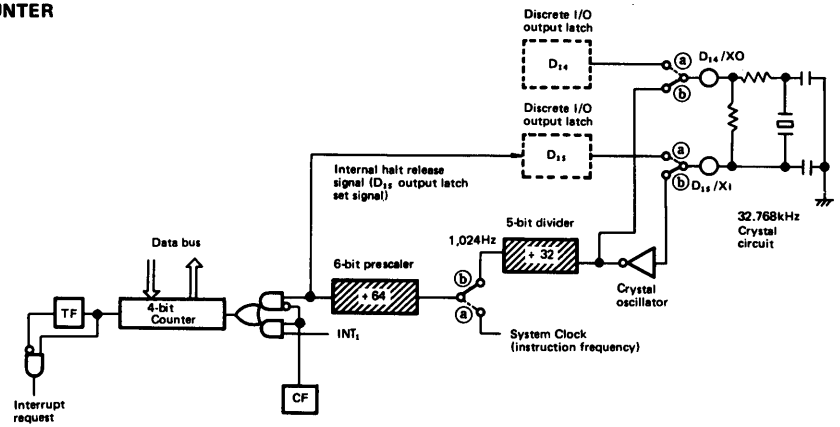


Figure 15 Timer/Counter Block Diagram

Timer/Counter Block Diagram is shown in Figure 15. 5-bit divider divides the crystal oscillation (32.768kHz) by 32 and generates clocks of 1,024Hz in the crystal oscillation mode. It does not stop in the halt state. Prescaler divides the system clock (instruction frequency) or 1,024Hz clock by 64 and generates overflow output pulse of "Instruction frequency/64Hz" or 16Hz. In the crystal oscillation mode, it does not stop during halt state. The input of the 4-bit counter is overflow output pulse of the prescaler or a pulse of INT_1 terminal. Input selection is determined by CF state. Data can be exchanged between the counter and bus by LTI, LTA or LAT instruction. TF is a flip-flop which masks the interrupt of timer/counter.

The timer is operable in 2 modes (timer mode and counter mode) depending on what to count, and the mode is selected by programs.

• Timer Mode

The 4-bit counter counts prescaler overflow output pulses. One of the following two can be selected as the prescaler count clock by the mask option.

1. System clock (Instruction frequency)
2. 1,024Hz clock (Crystal oscillation for timer is selected.) . . . Clock obtained by dividing the crystal oscillation (32.768kHz) for timer by 32. Crystal oscillator is constructed between D terminals of D_{14} and D_{15}:

Note 1) In this case, the overflow output pulses from the prescaler are 16Hz. These pulses are counted by the 4-bit counter to generate an interrupt from 16Hz to 1Hz.

Note 2) In this case, the part marked with ▨ in Figure 15 Timer/Counter does not stop even in halt state. When using "internal halt mode" among the halt function, internal halt state is generated by resetting the register for internal halt mode (D latch: D_{15}) by an instruction (D_{15} = "0": internal halt state, D_{15} = "1": operating state), and all the operation stop. In this case, overflow output pulses from the prescaler work as the signals releasing the internal halt state and set the D_{15} output latch. Therefore, if an overflow output pulse from the prescaler is generated, internal halt state is released, and the LSI starts to operate.
By utilizing this function, intermittent operation is possible, that is, program execution for necessary processing (for example, counting for clock function) starts after every 62.5 msec (16Hz) and the LSI stops after execution of this program by an instruction which makes the LSI into internal halt state. This reduces the time in which the LSI operates, resulting in power consumption in substance.

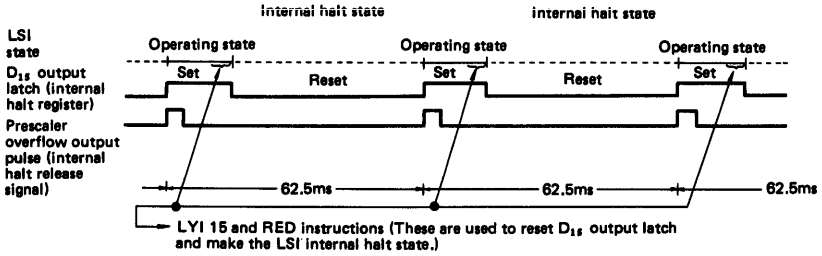


Figure 16 Set/Reset Operation Using Crystal Oscillator for Timer

- **Counter Mode**

Counts pulses of INT_1 terminal.

(Note) The width of INT_1 pulse in the counter mode must be at least 2-cycle time for both the "High" and "Low" levels.

Each block of timer/counter and the specified time of timer mode are explained in the followings.

■ INTERRUPT

There are interrupt caused by the timer/counter or the inputs. Each interrupt cause has the interrupt request F/F and the request is latched into this flip-flop when it is generated. If an interrupt request can be accepted, the interrupt is generated.

It is controlled by Interrupt Enable F/F (I/E F/F) whether an interrupt can be accepted or not.

Figure 17 shows the interrupt block diagram and Figure 18 shows the interrupt timing chart.

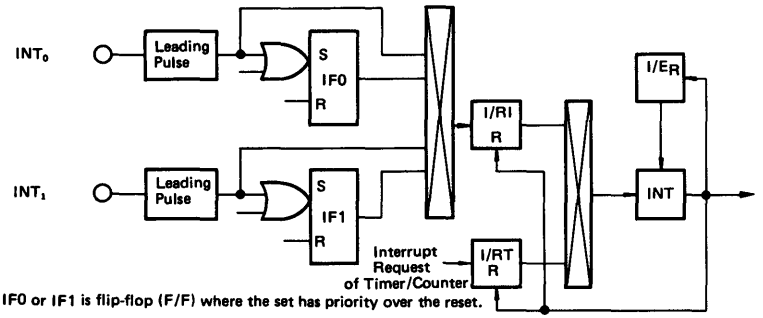


Figure 17 Interrupt Block Diagram

The status is unchanged. (The interrupt is different from general CAL in regard to this matter.)

Stacking of registers is performed by the program. Returning from the interrupt routine is performed in the same way as that from normal subroutine. But it is convenient to use RTNI (Return Interrupt) which sets the I/E simultaneously with RTN.

An interrupt is generated irrespectively of the condition of stack registers, so enough stack registers are needed.

TF, IF0, or IF1 is flip-flop where the set has priority over the reset. It is not reset when the reset instruction is issued simultaneously with OVF of the timer/counter or the leading edge of the input, though the interrupt request is generated and latched into I/RI or I/RT.

The interrupt processing caused by the interrupt generation is basically the subroutine jump and the jumping location in memory is fixed as:

Interrupt of the timer/counter 0 page 3F address (00–3F)
Interrupt of the inputs 1 page 3F address (01–3F)

In addition,

The saving operation of PC → ST1 → ST2 → ST3 → ST4.

I/E reset

- **Interrupt of the Inputs**

Two pins INT_0 and INT_1 have the interrupt request functions. They have the leading pulse generation circuit and the interrupt mask F/F (IF0, IF1). When IF0 or IF1 is reset, the interrupt request is able to generate interrupt mask release. When INT_0 or INT_1 changes from "0" to "1" ("Low" level → "High" level), the leading pulse is generated and generates the interrupt request. Then IF0 or IF1 is set, the interrupt is masked.

The interrupt request generated by the leading pulse is latched in the interrupt request F/F on the input side (I/RI). If interrupt Enable F/F (I/E) is "1", the interrupt is generated immediately and I/RI is reset. But if Interrupt Enable F/F (I/E) is "0", I/RI is held at "1" level until it gets into the Interrupt Enable state.

IF0, IF1, INT_0 and INT_1 can be tested by the program. Therefore, they can also be used as normal input terminals or latch terminals of momentary pulse input.

The interrupt pulse width (at both "High" and "Low" levels) should be more than two-cycle.

- **Interrupt of the Timer/Counter**

The interrupt request of the timer/counter is latched into the interrupt request F/F of the timer (I/RT). Then I/RT operates in the same way as I/RI, but the interrupt of the input has priority over that of the timer. Therefore, the input interrupt is processed when both of I/RI and I/RT are at "1" level (interrupt requests are simultaneously generated). During the input interrupt, I/RT remains set. Thus, after the input interrupt, the timer/counter interrupt can be processed.

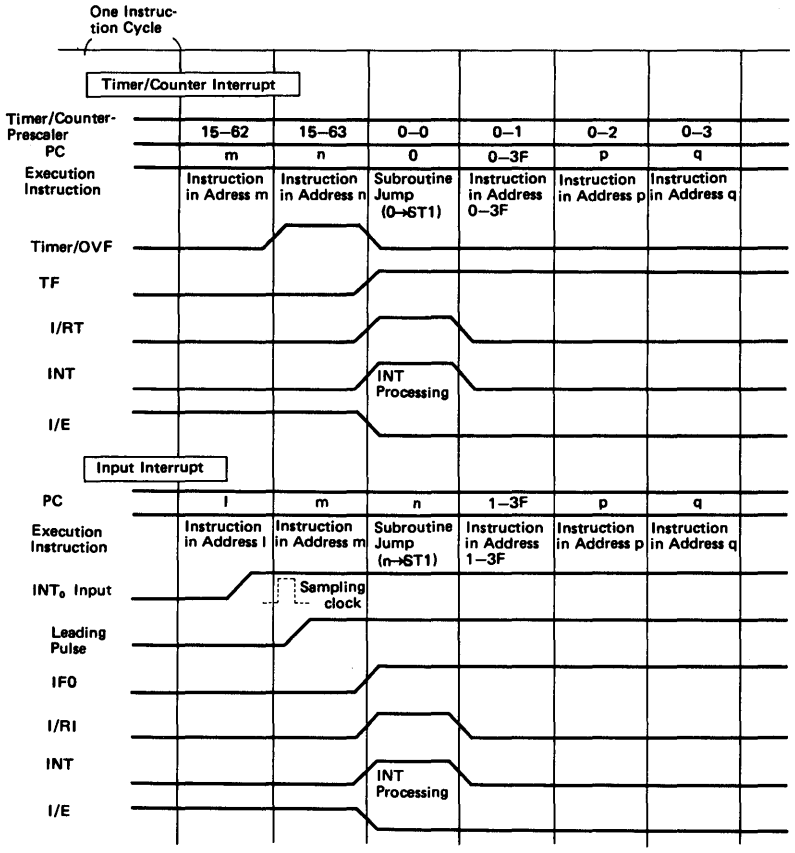


Figure 18 Interrupt Timing Chart

■ LIQUID CRYSTAL DISPLAY

• Liquid Crystal Display Circuit

The LCD-III can directly drive the liquid crystal display panel of static, 1/2 duty factor, 1/3 duty factor and 1/4 duty factor.

The LCD-III has 4 common signal terminals and 32 segment signal terminals. Further, if liquid crystal driver LSI(HD44100H) is connected to the LCD-III, up to 96 segment signal terminals can be extended externally. Thus, in addition to the internal 32 terminals, total 128 segment signal terminals can be driven.

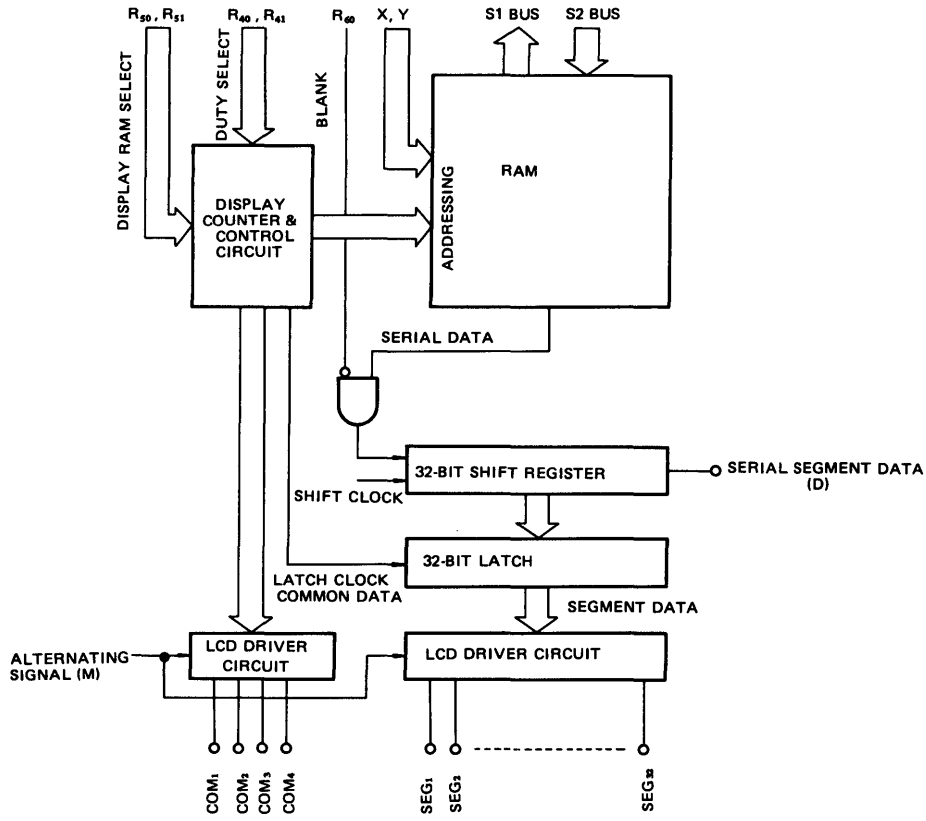


Figure 19 Liquid Crystal Display Circuit Block Diagram

Display is automatically executed by writing segment data into RAM for LCD. The RAM reads segment data bit by bit sequentially every one instruction cycle upon receiving address signal from the display counter and the control circuit. Every time common signal is scanned, the RAM reads 128-segment data (SEG_1 to SEG_{128}), which is correspond to common signal selected at the next time. In the HD44790, scan of common signal is executed every 256-instruction cycle. Therefore, the data which is correspond to 128-segment is read twice at the same time. And in the HD44795, scan of common signal is executed every 128-instruction cycle. Therefore, 128-segment data is read. The serial data read is converted to parallel data by the shift register and latch, converted to LCD drive signal by the liquid crystal driver and the outputted from a segment terminal. 32-segment (SEG_1 to SEG_{32}) out of 128-segment serial data is used within the LCD-III, and the rest (96-segment) is outputted to the liquid crystal driver LSI HD44100H which is connected to the LCD-III and is converted to the LCD drive signal in the HD44100H at the time of designation of with liquid crystal segment output extension. Cycle of the latch clock is 256-instruction cycle in the HD44790 and 128 instruction cycle in the HD44795. In the case of dynamic drive, data at the common side changes synchronously with the latch clock. These display operations are all executed regardless of program.

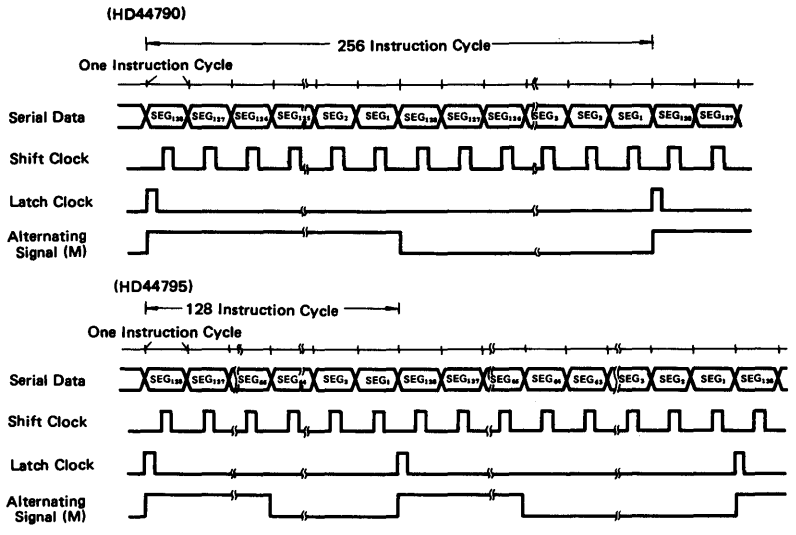


Figure 20 Liquid Crystal Display Circuit Time Chart (To be continued)

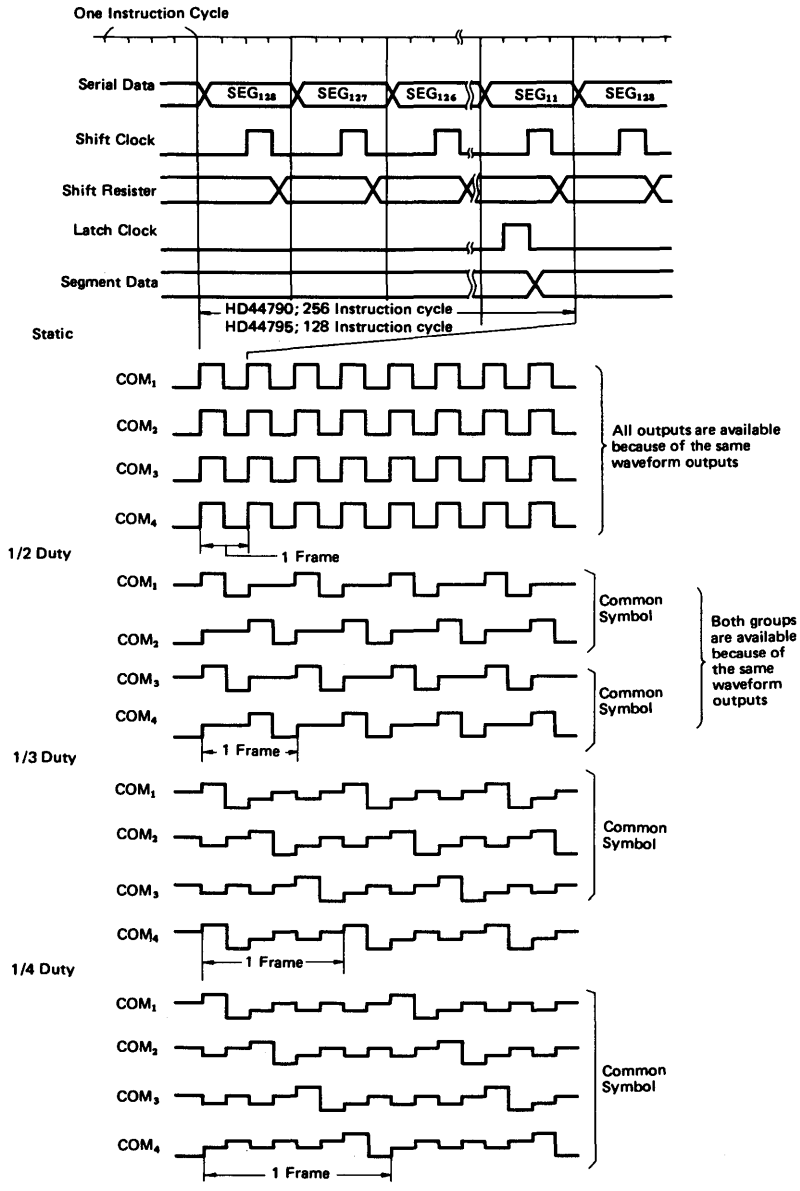


Figure 20 Liquid Crystal Display Circuit Time Chart

- **Liquid Crystal Display Mode Setting Registers**
  For selection of the liquid crystal display mode, data I/O registers of R4, R5 and R6 are used.

Table 5 Function of Liquid Crystal Display Mode Setting Registers

	R_{41}	R_{40}	Function
Selection of liquid crystal display duty factor (R_{40}, R_{41})	0	0	Static
	0	1	1/2 duty
	1	0	1/3 duty
	1	1	1/4 duty

	R_{42}	Function
Designation of with or without liquid crystal segment output extension (R_{42})	0	To be extended (Outputs display data from Channel R1)
	1	Not to be extended (Channel R1 becomes an ordinary 4-bit data I/O.)

	R_{60}	Function
Liquid crystal display blanking signal (R_{60})	0	Outputs RAM data for liquid crystal display as segment signals.
	1	Segment signals become non-selection status (blanking) regardless of RAM data for liquid crystal display.

	R_{51}	R_{50}	Function
RAM designation for liquid crystal display (R_{50}, R_{51})	Function varies with liquid crystal display duty factor.		

(NOTE) Liquid crystal display mode at resetting
Since all bits of registers R4, R5 and R6 are set to "1" by the reset function, display mode after resetting becomes as shown below:
Liquid crystal display duty factor: 1/4 duty (R_{40} = "1", R_{41} = "1")
Liquid crystal segment output extension: Not extended (R_{42} = "1")
Designation of liquid crystal display blanking: Display blanking (R_{60} = "1")

- **Relation between Display RAM and Segment Data**

In the LCD-III, 4 types of display duty factor (static, 1/2 duty, 1/3 duty, and 1/4 duty) can be selected by programs, and correspondence between RAM bits and segment data changes according to these duty factors.

RAM Address X				RAM Y	RAM 2^3	RAM 2^2	RAM 2^1	RAM 2^0
6	4	2	0	0	SEG_4	SEG_3	SEG_2	SEG_1
				1	SEG_8	SEG_7	SEG_6	SEG_5
				2	SEG_{12}	SEG_{11}	SEG_{10}	SEG_9
				3	SEG_{16}	SEG_{15}	SEG_{14}	SEG_{13}
				4	SEG_{20}	SEG_{19}	SEG_{18}	SEG_{17}
				5	SEG_{24}	SEG_{23}	SEG_{22}	SEG_{21}
				6	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}
				7	SEG_{32}	SEG_{31}	SEG_{30}	SEG_{29}
				8	SEG_{36}	SEG_{35}	SEG_{34}	SEG_{33}
				9	SEG_{40}	SEG_{39}	SEG_{38}	SEG_{37}
				10	SEG_{44}	SEG_{43}	SEG_{42}	SEG_{41}
				11	SEG_{48}	SEG_{47}	SEG_{46}	SEG_{45}
				12	SEG_{52}	SEG_{51}	SEG_{50}	SEG_{49}
				13	SEG_{56}	SEG_{55}	SEG_{54}	SEG_{53}
				14	SEG_{60}	SEG_{59}	SEG_{58}	SEG_{57}
				15	SEG_{64}	SEG_{63}	SEG_{62}	SEG_{61}
7	5	3	1	0	SEG_{68}	SEG_{67}	SEG_{66}	SEG_{65}
				1	SEG_{72}	SEG_{71}	SEG_{70}	SEG_{69}
				2	SEG_{76}	SEG_{75}	SEG_{74}	SEG_{73}
				3	SEG_{80}	SEG_{79}	SEG_{78}	SEG_{77}
				4	SEG_{84}	SEG_{83}	SEG_{82}	SEG_{81}
				5	SEG_{88}	SEG_{87}	SEG_{86}	SEG_{85}
				6	SEG_{92}	SEG_{91}	SEG_{90}	SEG_{89}
				7	SEG_{96}	SEG_{95}	SEG_{94}	SEG_{93}
				8	SEG_{100}	SEG_{99}	SEG_{98}	SEG_{97}
				9	SEG_{104}	SEG_{103}	SEG_{102}	SEG_{101}
				10	SEG_{108}	SEG_{107}	SEG_{106}	SEG_{105}
				11	SEG_{112}	SEG_{111}	SEG_{110}	SEG_{109}
				12	SEG_{116}	SEG_{115}	SEG_{114}	SEG_{113}
				13	SEG_{120}	SEG_{119}	SEG_{118}	SEG_{117}
				14	SEG_{124}	SEG_{123}	SEG_{122}	SEG_{121}
				15	SEG_{128}	SEG_{127}	SEG_{126}	SEG_{125}
R_{51}	0	0	1	1				
R_{50}	0	1	0	1				

(NOTE) The SEG_{33} to SEG_{128} are extended segments.

Figure 21 Relation between RAM for LCD & Segment Data (Static)

RAM Address					RAM				
X				Y	2^3	2^2	2^1	2^0	
6	4	2	0	0	SEG_4	SEG_3	SEG_2	SEG_1	COM_1
				1	SEG_4	SEG_3	SEG_2	SEG_1	COM_2
				2	SEG_8	SEG_7	SEG_6	SEG_5	COM_1
				3	SEG_8	SEG_7	SEG_6	SEG_5	COM_2
				4	SEG_{12}	SEG_{11}	SEG_{10}	SEG_9	COM_1
				5	SEG_{12}	SEG_{11}	SEG_{10}	SEG_9	COM_2
				6	SEG_{16}	SEG_{15}	SEG_{14}	SEG_{13}	COM_1
				7	SEG_{16}	SEG_{15}	SEG_{14}	SEG_{13}	COM_2
				8	SEG_{20}	SEG_{19}	SEG_{18}	SEG_{17}	COM_1
				9	SEG_{20}	SEG_{19}	SEG_{18}	SEG_{17}	COM_2
				10	SEG_{24}	SEG_{23}	SEG_{22}	SEG_{21}	COM_1
				11	SEG_{24}	SEG_{23}	SEG_{22}	SEG_{21}	COM_2
				12	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	COM_1
				13	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	COM_2
				14	SEG_{32}	SEG_{31}	SEG_{30}	SEG_{29}	COM_1
				15	SEG_{32}	SEG_{31}	SEG_{30}	SEG_{29}	COM_2
7	5	3	1	0	SEG_{36}	SEG_{35}	SEG_{34}	SEG_{33}	COM_1
				1	SEG_{36}	SEG_{35}	SEG_{34}	SEG_{33}	COM_2
				2	SEG_{40}	SEG_{39}	SEG_{38}	SEG_{37}	COM_1
				3	SEG_{40}	SEG_{39}	SEG_{38}	SEG_{37}	COM_2
				4	SEG_{44}	SEG_{43}	SEG_{42}	SEG_{41}	COM_1
				5	SEG_{44}	SEG_{43}	SEG_{42}	SEG_{41}	COM_2
				6	SEG_{48}	SEG_{47}	SEG_{46}	SEG_{45}	COM_1
				7	SEG_{48}	SEG_{47}	SEG_{46}	SEG_{45}	COM_2
				8	SEG_{52}	SEG_{51}	SEG_{50}	SEG_{49}	COM_1
				9	SEG_{52}	SEG_{51}	SEG_{50}	SEG_{49}	COM_2
				10	SEG_{56}	SEG_{55}	SEG_{54}	SEG_{53}	COM_1
				11	SEG_{56}	SEG_{55}	SEG_{54}	SEG_{53}	COM_2
				12	SEG_{60}	SEG_{59}	SEG_{58}	SEG_{57}	COM_1
				13	SEG_{60}	SEG_{59}	SEG_{58}	SEG_{57}	COM_2
				14	SEG_{64}	SEG_{63}	SEG_{62}	SEG_{61}	COM_1
				15	SEG_{64}	SEG_{63}	SEG_{62}	SEG_{61}	COM_2
4	6	0	2	0	SEG_{68}	SEG_{67}	SEG_{66}	SEG_{65}	COM_1
				1	SEG_{68}	SEG_{67}	SEG_{66}	SEG_{65}	COM_2
				2	SEG_{72}	SEG_{71}	SEG_{70}	SEG_{69}	COM_1
				3	SEG_{72}	SEG_{71}	SEG_{70}	SEG_{69}	COM_2
				4	SEG_{76}	SEG_{75}	SEG_{74}	SEG_{73}	COM_1
				5	SEG_{76}	SEG_{75}	SEG_{74}	SEG_{73}	COM_2
				6	SEG_{80}	SEG_{79}	SEG_{78}	SEG_{77}	COM_1
				7	SEG_{80}	SEG_{79}	SEG_{78}	SEG_{77}	COM_2
				8	SEG_{84}	SEG_{83}	SEG_{82}	SEG_{81}	COM_1
				9	SEG_{84}	SEG_{83}	SEG_{82}	SEG_{81}	COM_2
				10	SEG_{88}	SEG_{87}	SEG_{86}	SEG_{85}	COM_1
				11	SEG_{88}	SEG_{87}	SEG_{86}	SEG_{85}	COM_2
				12	SEG_{92}	SEG_{91}	SEG_{90}	SEG_{89}	COM_1
				13	SEG_{92}	SEG_{91}	SEG_{90}	SEG_{89}	COM_2
				14	SEG_{96}	SEG_{95}	SEG_{94}	SEG_{93}	COM_1
				15	SEG_{96}	SEG_{95}	SEG_{94}	SEG_{93}	COM_2
5	7	1	3	0	SEG_{100}	SEG_{99}	SEG_{98}	SEG_{97}	COM_1
				1	SEG_{100}	SEG_{99}	SEG_{98}	SEG_{97}	COM_2
				2	SEG_{104}	SEG_{103}	SEG_{102}	SEG_{101}	COM_1
				3	SEG_{104}	SEG_{103}	SEG_{102}	SEG_{101}	COM_2
				4	SEG_{108}	SEG_{107}	SEG_{106}	SEG_{105}	COM_1
				5	SEG_{108}	SEG_{107}	SEG_{106}	SEG_{105}	COM_2
				6	SEG_{112}	SEG_{111}	SEG_{110}	SEG_{109}	COM_1
				7	SEG_{112}	SEG_{111}	SEG_{110}	SEG_{109}	COM_2
				8	SEG_{116}	SEG_{115}	SEG_{114}	SEG_{113}	COM_1
				9	SEG_{116}	SEG_{115}	SEG_{114}	SEG_{113}	COM_2
				10	SEG_{120}	SEG_{119}	SEG_{118}	SEG_{117}	COM_1
				11	SEG_{120}	SEG_{119}	SEG_{118}	SEG_{117}	COM_2
				12	SEG_{124}	SEG_{123}	SEG_{122}	SEG_{121}	COM_1
				13	SEG_{124}	SEG_{123}	SEG_{122}	SEG_{121}	COM_2
				14	SEG_{128}	SEG_{127}	SEG_{126}	SEG_{125}	COM_1
				15	SEG_{128}	SEG_{127}	SEG_{126}	SEG_{125}	COM_2
R_{S1}	0	0	1	1					
R_{S0}	0	1	0	1					

(NOTE) The SEG_{33} to SEG_{128} are extended segments.

Figure 22 Relation between RAM for LCD & Segment Data (1/2 Duty, 1/2 Bias)

RAM Address					RAM			
X				Y	2^3	2^2	2^1	2^0
6	4	2	0	0		SEG_1	SEG_1	SEG_1
				1		SEG_2	SEG_2	SEG_2
				2		SEG_3	SEG_3	SEG_3
				3		SEG_4	SEG_4	SEG_4
				4		SEG_5	SEG_5	SEG_5
				5		SEG_6	SEG_6	SEG_6
				6		SEG_7	SEG_7	SEG_7
				7		SEG_8	SEG_8	SEG_8
				8		SEG_9	SEG_9	SEG_9
				9		SEG_{10}	SEG_{10}	SEG_{10}
				10		SEG_{11}	SEG_{11}	SEG_{11}
				11		SEG_{12}	SEG_{12}	SEG_{12}
				12		SEG_{13}	SEG_{13}	SEG_{13}
				13		SEG_{14}	SEG_{14}	SEG_{14}
				14		SEG_{15}	SEG_{15}	SEG_{15}
				15		SEG_{16}	SEG_{16}	SEG_{16}
7	5	3	1	0		SEG_{17}	SEG_{17}	SEG_{17}
				1		SEG_{18}	SEG_{18}	SEG_{18}
				2		SEG_{19}	SEG_{19}	SEG_{19}
				3		SEG_{20}	SEG_{20}	SEG_{20}
				4		SEG_{21}	SEG_{21}	SEG_{21}
				5		SEG_{22}	SEG_{22}	SEG_{22}
				6		SEG_{23}	SEG_{23}	SEG_{23}
				7		SEG_{24}	SEG_{24}	SEG_{24}
				8		SEG_{25}	SEG_{25}	SEG_{25}
				9		SEG_{26}	SEG_{26}	SEG_{26}
				10		SEG_{27}	SEG_{27}	SEG_{27}
				11		SEG_{28}	SEG_{28}	SEG_{28}
				12		SEG_{29}	SEG_{29}	SEG_{29}
				13		SEG_{30}	SEG_{30}	SEG_{30}
				14		SEG_{31}	SEG_{31}	SEG_{31}
				15		SEG_{32}	SEG_{32}	SEG_{32}
4	6	0	2	0		SEG_{33}	SEG_{33}	SEG_{33}
				1		SEG_{34}	SEG_{34}	SEG_{34}
				2		SEG_{35}	SEG_{35}	SEG_{35}
				3		SEG_{36}	SEG_{36}	SEG_{36}
				4		SEG_{37}	SEG_{37}	SEG_{37}
				5		SEG_{38}	SEG_{38}	SEG_{38}
				6		SEG_{39}	SEG_{39}	SEG_{39}
				7		SEG_{40}	SEG_{40}	SEG_{40}
				8		SEG_{41}	SEG_{41}	SEG_{41}
				9		SEG_{42}	SEG_{42}	SEG_{42}
				10		SEG_{43}	SEG_{43}	SEG_{43}
				11		SEG_{44}	SEG_{44}	SEG_{44}
				12		SEG_{45}	SEG_{45}	SEG_{45}
				13		SEG_{46}	SEG_{46}	SEG_{46}
				14		SEG_{47}	SEG_{47}	SEG_{47}
				15		SEG_{48}	SEG_{48}	SEG_{48}
5	7	1	3	0		SEG_{49}	SEG_{49}	SEG_{49}
				1		SEG_{50}	SEG_{50}	SEG_{50}
				2		SEG_{51}	SEG_{51}	SEG_{51}
				3		SEG_{52}	SEG_{52}	SEG_{52}
				4		SEG_{53}	SEG_{53}	SEG_{53}
				5		SEG_{54}	SEG_{54}	SEG_{54}
				6		SEG_{55}	SEG_{55}	SEG_{55}
				7		SEG_{56}	SEG_{56}	SEG_{56}
				8		SEG_{57}	SEG_{57}	SEG_{57}
				9		SEG_{58}	SEG_{58}	SEG_{58}
				10		SEG_{59}	SEG_{59}	SEG_{59}
				11		SEG_{60}	SEG_{60}	SEG_{60}
				12		SEG_{61}	SEG_{61}	SEG_{61}
				13		SEG_{62}	SEG_{62}	SEG_{62}
				14		SEG_{63}	SEG_{63}	SEG_{63}
				15		SEG_{64}	SEG_{64}	SEG_{64}
R_{51}	0	0	1	1				
R_{50}	0	1	0	1			COM_3	COM_2	COM_1

RAM Address					RAM			
X				Y	2^3	2^2	2^1	2^0
2	0	6	4	0		SEG_{65}	SEG_{65}	SEG_{65}
				1		SEG_{66}	SEG_{66}	SEG_{66}
				2		SEG_{67}	SEG_{67}	SEG_{67}
				3		SEG_{68}	SEG_{68}	SEG_{68}
				4		SEG_{69}	SEG_{69}	SEG_{69}
				5		SEG_{70}	SEG_{70}	SEG_{70}
				6		SEG_{71}	SEG_{71}	SEG_{71}
				7		SEG_{72}	SEG_{72}	SEG_{72}
				8		SEG_{73}	SEG_{73}	SEG_{73}
				9		SEG_{74}	SEG_{74}	SEG_{74}
				10		SEG_{75}	SEG_{75}	SEG_{75}
				11		SEG_{76}	SEG_{76}	SEG_{76}
				12		SEG_{77}	SEG_{77}	SEG_{77}
				13		SEG_{78}	SEG_{78}	SEG_{78}
				14		SEG_{79}	SEG_{79}	SEG_{79}
				15		SEG_{80}	SEG_{80}	SEG_{80}
3	1	7	5	0		SEG_{81}	SEG_{81}	SEG_{81}
				1		SEG_{82}	SEG_{82}	SEG_{82}
				2		SEG_{83}	SEG_{83}	SEG_{83}
				3		SEG_{84}	SEG_{84}	SEG_{84}
				4		SEG_{85}	SEG_{85}	SEG_{85}
				5		SEG_{86}	SEG_{86}	SEG_{86}
				6		SEG_{87}	SEG_{87}	SEG_{87}
				7		SEG_{88}	SEG_{88}	SEG_{88}
				8		SEG_{89}	SEG_{89}	SEG_{89}
				9		SEG_{90}	SEG_{90}	SEG_{90}
				10		SEG_{91}	SEG_{91}	SEG_{91}
				11		SEG_{92}	SEG_{92}	SEG_{92}
				12		SEG_{93}	SEG_{93}	SEG_{93}
				13		SEG_{94}	SEG_{94}	SEG_{94}
				14		SEG_{95}	SEG_{95}	SEG_{95}
				15		SEG_{96}	SEG_{96}	SEG_{96}
0	2	4	6	0		SEG_{97}	SEG_{97}	SEG_{97}
				1		SEG_{98}	SEG_{98}	SEG_{98}
				2		SEG_{99}	SEG_{99}	SEG_{99}
				3		SEG_{100}	SEG_{100}	SEG_{100}
				4		SEG_{101}	SEG_{101}	SEG_{101}
				5		SEG_{102}	SEG_{102}	SEG_{102}
				6		SEG_{103}	SEG_{103}	SEG_{103}
				7		SEG_{104}	SEG_{104}	SEG_{104}
				8		SEG_{105}	SEG_{105}	SEG_{105}
				9		SEG_{106}	SEG_{106}	SEG_{106}
				10		SEG_{107}	SEG_{107}	SEG_{107}
				11		SEG_{108}	SEG_{108}	SEG_{108}
				12		SEG_{109}	SEG_{109}	SEG_{109}
				13		SEG_{110}	SEG_{110}	SEG_{110}
				14		SEG_{111}	SEG_{111}	SEG_{111}
				15		SEG_{112}	SEG_{112}	SEG_{112}
1	3	5	7	0		SEG_{113}	SEG_{113}	SEG_{113}
				1		SEG_{114}	SEG_{114}	SEG_{114}
				2		SEG_{115}	SEG_{115}	SEG_{115}
				3		SEG_{116}	SEG_{116}	SEG_{116}
				4		SEG_{117}	SEG_{117}	SEG_{117}
				5		SEG_{118}	SEG_{118}	SEG_{118}
				6		SEG_{119}	SEG_{119}	SEG_{119}
				7		SEG_{120}	SEG_{120}	SEG_{120}
				8		SEG_{121}	SEG_{121}	SEG_{121}
				9		SEG_{122}	SEG_{122}	SEG_{122}
				10		SEG_{123}	SEG_{123}	SEG_{123}
				11		SEG_{124}	SEG_{124}	SEG_{124}
				12		SEG_{125}	SEG_{125}	SEG_{125}
				13		SEG_{126}	SEG_{126}	SEG_{126}
				14		SEG_{127}	SEG_{127}	SEG_{127}
				15		SEG_{128}	SEG_{128}	SEG_{128}
R_{50}	0	0	1	1				
R_{51}	0	1	0	1			COM_3	COM_2	COM_1

(NOTE) The SEG_{33} to SEG_{128} are extended segments.

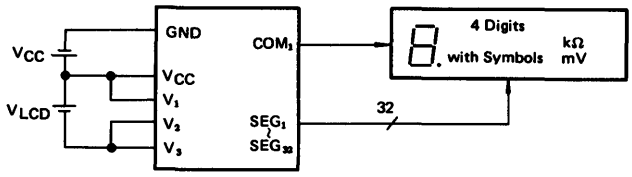
Figure 23 Relation between RAM for Liquid Crystal Display and Segment Data (1/3 Duty, 1/3 Bias Drive)

RAM Address X				Y	RAM 2^3	2^2	2^1	2^0
6	4	2	0	0	SEG_1	SEG_1	SEG_1	SEG_1
				1	SEG_2	SEG_2	SEG_2	SEG_2
				2	SEG_3	SEG_3	SEG_3	SEG_3
				3	SEG_4	SEG_4	SEG_4	SEG_4
				4	SEG_5	SEG_5	SEG_5	SEG_5
				5	SEG_6	SEG_6	SEG_6	SEG_6
				6	SEG_7	SEG_7	SEG_7	SEG_7
				7	SEG_8	SEG_8	SEG_8	SEG_8
				8	SEG_9	SEG_9	SEG_9	SEG_9
				9	SEG_{10}	SEG_{10}	SEG_{10}	SEG_{10}
				10	SEG_{11}	SEG_{11}	SEG_{11}	SEG_{11}
				11	SEG_{12}	SEG_{12}	SEG_{12}	SEG_{12}
				12	SEG_{13}	SEG_{13}	SEG_{13}	SEG_{13}
				13	SEG_{14}	SEG_{14}	SEG_{14}	SEG_{14}
				14	SEG_{15}	SEG_{15}	SEG_{15}	SEG_{15}
				15	SEG_{16}	SEG_{16}	SEG_{16}	SEG_{16}
7	5	3	1	0	SEG_{17}	SEG_{17}	SEG_{17}	SEG_{17}
				1	SEG_{18}	SEG_{18}	SEG_{18}	SEG_{18}
				2	SEG_{19}	SEG_{19}	SEG_{19}	SEG_{19}
				3	SEG_{20}	SEG_{20}	SEG_{20}	SEG_{20}
				4	SEG_{21}	SEG_{21}	SEG_{21}	SEG_{21}
				5	SEG_{22}	SEG_{22}	SEG_{22}	SEG_{22}
				6	SEG_{23}	SEG_{23}	SEG_{23}	SEG_{23}
				7	SEG_{24}	SEG_{24}	SEG_{24}	SEG_{24}
				8	SEG_{25}	SEG_{25}	SEG_{25}	SEG_{25}
				9	SEG_{26}	SEG_{26}	SEG_{26}	SEG_{26}
				10	SEG_{27}	SEG_{27}	SEG_{27}	SEG_{27}
				11	SEG_{28}	SEG_{28}	SEG_{28}	SEG_{28}
				12	SEG_{29}	SEG_{29}	SEG_{29}	SEG_{29}
				13	SEG_{30}	SEG_{30}	SEG_{30}	SEG_{30}
				14	SEG_{31}	SEG_{31}	SEG_{31}	SEG_{31}
				15	SEG_{32}	SEG_{32}	SEG_{32}	SEG_{32}
4	6	0	2	0	SEG_{33}	SEG_{33}	SEG_{33}	SEG_{33}
				1	SEG_{34}	SEG_{34}	SEG_{34}	SEG_{34}
				2	SEG_{35}	SEG_{35}	SEG_{35}	SEG_{35}
				3	SEG_{36}	SEG_{36}	SEG_{36}	SEG_{36}
				4	SEG_{37}	SEG_{37}	SEG_{37}	SEG_{37}
				5	SEG_{38}	SEG_{38}	SEG_{38}	SEG_{38}
				6	SEG_{39}	SEG_{39}	SEG_{39}	SEG_{39}
				7	SEG_{40}	SEG_{40}	SEG_{40}	SEG_{40}
				8	SEG_{41}	SEG_{41}	SEG_{41}	SEG_{41}
				9	SEG_{42}	SEG_{42}	SEG_{42}	SEG_{42}
				10	SEG_{43}	SEG_{43}	SEG_{43}	SEG_{43}
				11	SEG_{44}	SEG_{44}	SEG_{44}	SEG_{44}
				12	SEG_{45}	SEG_{45}	SEG_{45}	SEG_{45}
				13	SEG_{46}	SEG_{46}	SEG_{46}	SEG_{46}
				14	SEG_{47}	SEG_{47}	SEG_{47}	SEG_{47}
				15	SEG_{48}	SEG_{48}	SEG_{48}	SEG_{48}
5	7	1	3	0	SEG_{49}	SEG_{49}	SEG_{49}	SEG_{49}
				1	SEG_{50}	SEG_{50}	SEG_{50}	SEG_{50}
				2	SEG_{51}	SEG_{51}	SEG_{51}	SEG_{51}
				3	SEG_{52}	SEG_{52}	SEG_{52}	SEG_{52}
				4	SEG_{53}	SEG_{53}	SEG_{53}	SEG_{53}
				5	SEG_{54}	SEG_{54}	SEG_{54}	SEG_{54}
				6	SEG_{55}	SEG_{55}	SEG_{55}	SEG_{55}
				7	SEG_{56}	SEG_{56}	SEG_{56}	SEG_{56}
				8	SEG_{57}	SEG_{57}	SEG_{57}	SEG_{57}
				9	SEG_{58}	SEG_{58}	SEG_{58}	SEG_{58}
				10	SEG_{59}	SEG_{59}	SEG_{59}	SEG_{59}
				11	SEG_{60}	SEG_{60}	SEG_{60}	SEG_{60}
				12	SEG_{61}	SEG_{61}	SEG_{61}	SEG_{61}
				13	SEG_{62}	SEG_{62}	SEG_{62}	SEG_{62}
				14	SEG_{63}	SEG_{63}	SEG_{63}	SEG_{63}
				15	SEG_{64}	SEG_{64}	SEG_{64}	SEG_{64}
R_{S1}	0	0	1	1				
R_{S0}	0	1	0	1	COM_4	COM_3	COM_2	COM_1

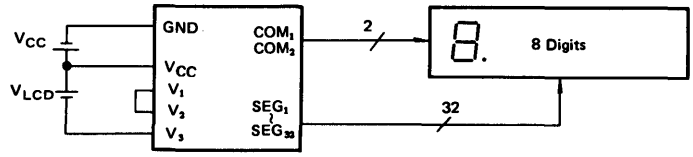
RAM Address X				Y	RAM 2^3	2^2	2^1	2^0
2	0	6	4	0	SEG_{65}	SEG_{65}	SEG_{65}	SEG_{65}
				1	SEG_{66}	SEG_{66}	SEG_{66}	SEG_{66}
				2	SEG_{67}	SEG_{67}	SEG_{67}	SEG_{67}
				3	SEG_{68}	SEG_{68}	SEG_{68}	SEG_{68}
				4	SEG_{69}	SEG_{69}	SEG_{69}	SEG_{69}
				5	SEG_{70}	SEG_{70}	SEG_{70}	SEG_{70}
				6	SEG_{71}	SEG_{71}	SEG_{71}	SEG_{71}
				7	SEG_{72}	SEG_{72}	SEG_{72}	SEG_{72}
				8	SEG_{73}	SEG_{73}	SEG_{73}	SEG_{73}
				9	SEG_{74}	SEG_{74}	SEG_{74}	SEG_{74}
				10	SEG_{75}	SEG_{75}	SEG_{75}	SEG_{75}
				11	SEG_{76}	SEG_{76}	SEG_{76}	SEG_{76}
				12	SEG_{77}	SEG_{77}	SEG_{77}	SEG_{77}
				13	SEG_{78}	SEG_{78}	SEG_{78}	SEG_{78}
				14	SEG_{79}	SEG_{79}	SEG_{79}	SEG_{79}
				15	SEG_{80}	SEG_{80}	SEG_{80}	SEG_{80}
3	1	7	5	0	SEG_{81}	SEG_{81}	SEG_{81}	SEG_{81}
				1	SEG_{82}	SEG_{82}	SEG_{82}	SEG_{82}
				2	SEG_{83}	SEG_{83}	SEG_{83}	SEG_{83}
				3	SEG_{84}	SEG_{84}	SEG_{84}	SEG_{84}
				4	SEG_{85}	SEG_{85}	SEG_{85}	SEG_{85}
				5	SEG_{86}	SEG_{86}	SEG_{86}	SEG_{86}
				6	SEG_{87}	SEG_{87}	SEG_{87}	SEG_{87}
				7	SEG_{88}	SEG_{88}	SEG_{88}	SEG_{88}
				8	SEG_{89}	SEG_{89}	SEG_{89}	SEG_{89}
				9	SEG_{90}	SEG_{90}	SEG_{90}	SEG_{90}
				10	SEG_{91}	SEG_{91}	SEG_{91}	SEG_{91}
				11	SEG_{92}	SEG_{92}	SEG_{92}	SEG_{92}
				12	SEG_{93}	SEG_{93}	SEG_{93}	SEG_{93}
				13	SEG_{94}	SEG_{94}	SEG_{94}	SEG_{94}
				14	SEG_{95}	SEG_{95}	SEG_{95}	SEG_{95}
				15	SEG_{96}	SEG_{96}	SEG_{96}	SEG_{96}
0	2	4	6	0	SEG_{97}	SEG_{97}	SEG_{97}	SEG_{97}
				1	SEG_{98}	SEG_{98}	SEG_{98}	SEG_{98}
				2	SEG_{99}	SEG_{99}	SEG_{99}	SEG_{99}
				3	SEG_{100}	SEG_{100}	SEG_{100}	SEG_{100}
				4	SEG_{101}	SEG_{101}	SEG_{101}	SEG_{101}
				5	SEG_{102}	SEG_{102}	SEG_{102}	SEG_{102}
				6	SEG_{103}	SEG_{103}	SEG_{103}	SEG_{103}
				7	SEG_{104}	SEG_{104}	SEG_{104}	SEG_{104}
				8	SEG_{105}	SEG_{105}	SEG_{105}	SEG_{105}
				9	SEG_{106}	SEG_{106}	SEG_{106}	SEG_{106}
				10	SEG_{107}	SEG_{107}	SEG_{107}	SEG_{107}
				11	SEG_{108}	SEG_{108}	SEG_{108}	SEG_{108}
				12	SEG_{109}	SEG_{109}	SEG_{109}	SEG_{109}
				13	SEG_{110}	SEG_{110}	SEG_{110}	SEG_{110}
				14	SEG_{111}	SEG_{111}	SEG_{111}	SEG_{111}
				15	SEG_{112}	SEG_{112}	SEG_{112}	SEG_{112}
1	3	5	7	0	SEG_{113}	SEG_{113}	SEG_{113}	SEG_{113}
				1	SEG_{114}	SEG_{114}	SEG_{114}	SEG_{114}
				2	SEG_{115}	SEG_{115}	SEG_{115}	SEG_{115}
				3	SEG_{116}	SEG_{116}	SEG_{116}	SEG_{116}
				4	SEG_{117}	SEG_{117}	SEG_{117}	SEG_{117}
				5	SEG_{118}	SEG_{118}	SEG_{118}	SEG_{118}
				6	SEG_{119}	SEG_{119}	SEG_{119}	SEG_{119}
				7	SEG_{120}	SEG_{120}	SEG_{120}	SEG_{120}
				8	SEG_{121}	SEG_{121}	SEG_{121}	SEG_{121}
				9	SEG_{122}	SEG_{122}	SEG_{122}	SEG_{122}
				10	SEG_{123}	SEG_{123}	SEG_{123}	SEG_{123}
				11	SEG_{124}	SEG_{124}	SEG_{124}	SEG_{124}
				12	SEG_{125}	SEG_{125}	SEG_{125}	SEG_{125}
				13	SEG_{126}	SEG_{126}	SEG_{126}	SEG_{126}
				14	SEG_{127}	SEG_{127}	SEG_{127}	SEG_{127}
				15	SEG_{128}	SEG_{128}	SEG_{128}	SEG_{128}
R_{S0}	0	0	1	1				
R_{S1}	0	1	0	1	COM_4	COM_3	COM_2	COM_1

(NOTE) The SEG_{33} to SEG_{128} are extended segments.

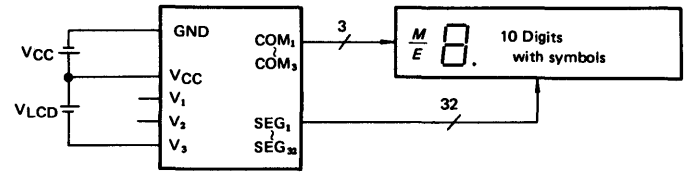
Figure 24 Relation between RAM for Liquid Crystal Display and Segment Data (1/4 Duty, 1/3 Bias Drive)



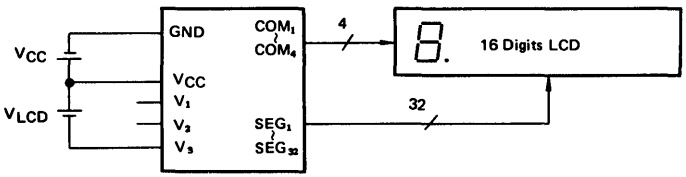
(Static)



(1/2 duty, 1/2 bias)



(1/3 duty, 1/3 bias)



(1/4 duty, 1/3 bias)

Figure 25 LCD Wiring Samples

- **Extension of Display Function**

Number of display digits can be increased by externally connecting an LCD driver LSI HD44100H to the LCD-III.

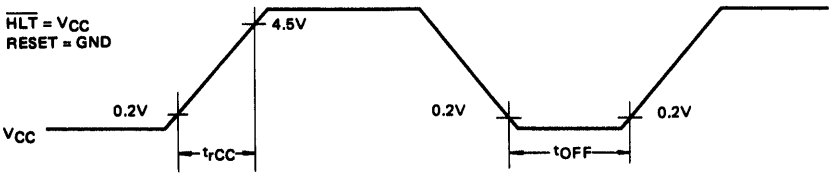
The HD44100H consists of shift registers and latch and liquid crystal drive circuit. When connected with the LCD-III, the HD44100H is used as a circuit for segment. In the LCD-III, display data for 128 segments is sent to the 32-bit shift register from RAM constantly. When R_{42} is set to "0", the R1 channel outputs the 32nd stage output D of the shift register, shift clock CL_2, latch clock CL_1 and AC signal M. Therefore, up to 96 segment terminals from SEG_{33} to SEG_{128} can be added by directly connecting the HD44100H.

■ RESET FUNCTION

The LCD-III can be reset by setting the reset terminal to "1" (High) and its operation starts when the terminal is set to "0" (Low). Also an automatic reset function (internal reset circuit) that operates when power is turned on is provided.

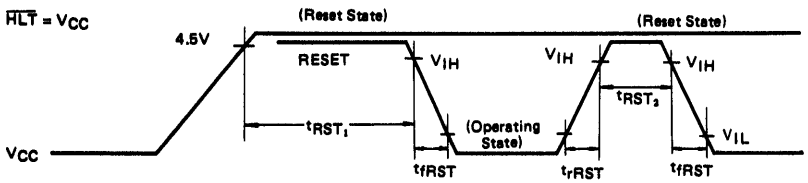
However, note that in the case of internal reset circuit the rise time of a power supply has a restriction. The LCD-III internal state is set as follows by the reset function:

The program counter is set to Address 3F of Page 31.
IR/I, IR/T, I/E and CF are reset to "0".
IF0, IF1 and TF are preset to "1".
All bits of data I/O register, discrete I/O output latches (R1, R2, R3 and D_0 to D_{15}) are preset to "1".
Liquid crystal display . . All bits of display mode setting registers (data I/O registers) R4, R5 and R6 are preset to "1".
RAM data is not retained after reset.



(NOTE) t_{OFF} specifies the period during the power supply is OFF, when a short break occurs or power supply ON/OFF is repeated.

Figure 26 Power Supply Condition Using the Built-in Reset Circuit



(NOTE) 1. t_{RST_1} includes the time required from the power ON until the operation gets into the constant state.

2. t_{RST_2} is applied when the operation is in the constant state.

Figure 27 Reset Input Condition Using an External Reset Circuit

■ HALT FUNCTION

The LCD-III is provided with half function. The halt function reduces power consumption in the halt state by temporarily stopping all status including RAM. When halt is released, operation restarts from the state immediately before the halt.

(Caution at the halt time)

When the LCD-III goes into halt state, segment terminals (SEG_1 to SEG_{32}) and common terminals (COM_1 to COM_4) become the same potential and display goes out. However, in order to reduce power consumption during halt, disconnect the voltage applied to liquid crystal power supply V_3. Since there are dividing resistors among V_1, V_2, and V_3, current of up to 50μA flows if voltage is applied between V_{CC} and V_3 in the same way as normal operation.

The user can select one of the following I/O status at the time of halt based on the "MASK OPTION LIST" when ordering ROM:

i) All I/O status is kept as the state immediately before the halt.
ii) All I/O status is held in the high impedance state (both PMOS and NMOS are off, and pull-up MOS is off).

There are the following two types of halt:

1) External Halt (Halt state generated by using $\overline{HLT}$ terminal)
All operations stop when the $\overline{HLT}$ terminal is set to the "0" level (Low). When the $\overline{HLT}$ terminal is set to the "1" level (High), operation restarts from the state immediately before the halt.
2) Internal Halt (Halt state generated by programs)
The user can select availability of internal halt at the time of ROM order based on the "MASK OPTION LIST". When internal halt is selected, timer crystal must be at-

tached externally. Therefore, the D_{14}/XO and D_{15}/XI terminals should not be used as general I/O's, but as XO and XI terminals for connecting cyrstal oscillator.

Resetting of the D_{15} latch by RED instruction generates internal halt state. Return from internal halt is effected by overflow signals of the prescaler. 16Hz overflow signals are output from the prescaler if a crystal oscillator of 32.768kHz is connected to the D_{14}/XO and D_{15}/XI terminals. When an overflow signal is issued, the D_{15} latch is set to "1" from "0", the LCD-III returns from halt state, adds 1 to the timer register, and execution restarts from the instruction next to the RED instruction.

Note that external halt caused by the $\overline{HLT}$ terminal cannot be released by prescaler overflow signals.

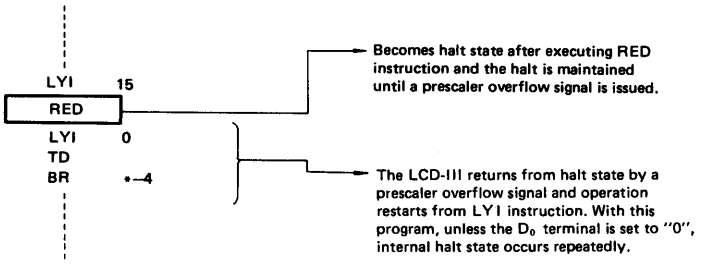


Figure 28 Program example in the Internal Halt Mode

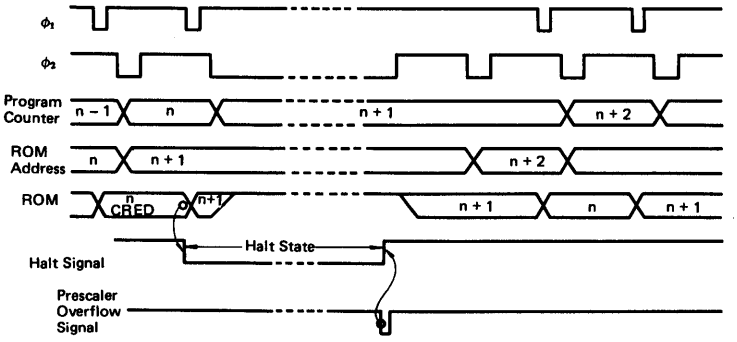


Figure 29 Internal Halt Timing Chart

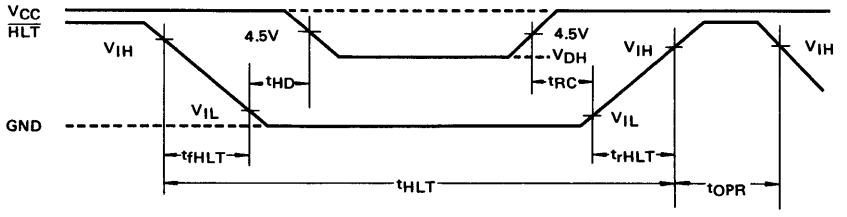
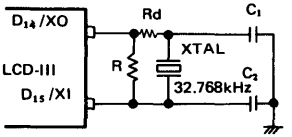


Figure 30 External Halt Timing Chart

■ CRYSTAL OSCILLATION CIRCUIT FOR TIMER

The user can specify by the "MASK OPTION LIST" whether or not the timer crystal should be externally attached. By externally attaching a crystal oscillator of 32.768 kHz to the D_{14}/XO and D_{15}/XI terminals, maximum 1 second of timer interruption cycle is possible setting the prescaler clock to 1,024Hz.

This circuit is the example of the typical use. As the oscillation characteristics is not guaranteed, please consider and examine the circuit constants carefully on your application.



$C_1 = C_2 = 20pF \pm 10\%$

$R = 10M\Omega \pm 10\%$

$Rd = 200k\Omega \pm 10\%$

(NOTE)
The crystal oscillator, resistor R, Rd and load capacitor C_1 and C_2 should be placed as close as possible to the LCD-III. Induction of external noise to D_{14}/XO and D_{15}/XI may disturb normal oscillation.

Figure 31 Crystal Oscillator Circuit

No.	Halt state	With or without timer crystal	D_{14}, D_{15} (XO, XI) terminals	Function
1	External halt	Externally attached crystal (32.768 kHz)	Terminals for attaching crystal. Cannot be used as general I/O.	Prescaler clock is set to 1,024 Hz and the overflow signal to 16 Hz. Up to 1 second can be set as the timer interruption cycle.
2	External halt	(Without crystal) Internal clock of LSI	Used as general I/O	The prescaler clock becomes 100 kHz type, and the timer interruption cycle can be set to maximum 97.66 Hz.
3	Internal and external halt	Externally attached crystal (32.768 kHz)	Terminals for attaching crystal. Cannot be used as general I/O.	Prescaler clock is set to 1,024 Hz and the overflow signal to 16 Hz. This signal performs the LCD-III return from internal halt. (Return from external halt is not possible by the prescaler overflow signal.)

■ MASK OPTION

The following type mask option is available.

- **I/O Terminal Format . . . . . Select one of A, B or C**
  A: Without pull-up MOS
  B: With pull-up MOS
  C: CMOS output

(Note) External input is not permitted if CMOS output is selected in the case of I/O common terminals.

- **I/O Status in the Halt State . . . . . Select Enable or Disable**

Enable
- Output . . . . Maintained in the status before halt.
- Pull-up MOS . . . ON
- Input . . . Unrelated to halt state

(Since Pull-up MOS is ON, if halt state occurs when output is "0" (Low) level (NMOS; ON), pull-up MOS current always flows. If input changes, transient current flows through the input circuit. Also, current flows through the input pull-up MOS. These currents are added to standby power supply current (or halt current).)

Disable
- Output . . . NMOS output; OFF
  CMOS output; High impedance
  (NMOS, PMOS; OFF)
- Pull-up MOS . . . OFF
- Input . . . Input circuit; OFF

(Both input and output become high impedance state. Since the input circuit is turned off, input change does not cause current other than the standby power supply current or halt current.)

- **With or without Externally Attached Timer Crystal**

Without timer crystal . . .
The D_{14} and D_{15} can be used as general I/O terminals. Select one of A, B or C in the D_{14}/D_{15} column of the I/O format specifications.

With timer crystal . . .
The D_{14} and D_{15} cannot be used as general I/O terminals.
Therefore, leave the D_{14}/D_{15} column in blank.
Since the D_{14} latch can be set, reset or tested, it can be used as a flag.
If no internal halt exists, the D_{15} latch can be used as a flag same as the D_{14} latch. If internal halt exists, it cannot be used as a general flag.

- **With or without Internal Halt**

With internal halt . . .
When internal halt is specified, the timer crystal must also be specified.

Without internal halt . . .
The D_{15} can be used as a general I/O terminal (when no timer crystal is used) or as a flag (when timer crystal is used).

■ INSTRUCTION

Instructions are listed according to their functions.
Each mnemonic code and function are shown in this table.

Group	Mnemonic code	Function	Status
Register to Register	LAB	B → A	
	LBA	A → B	
	LAY	Y → A	
	LASPX	SPX → A	
	LASPY	SPY → A	
	XAMR m	A ↔ MR (m)	
RAM Address	LXA	A → X	
	LYA	A → Y	
	LXI i	i → X	
	LYI i	i → Y	
	IY	Y+1 → Y	NZ
	DY	Y−1 → Y	NB
	AYY	Y+A → Y	C
	SYY	Y−A → Y	NB
	XSPX	X ↔ SPX	
	XSPY	Y ↔ SPY	
	XSPXY	X ↔ SPX, Y ↔ SPY	
Register RAM	LAM (XY)	M → A (XY ↔ SPXY)	
	LBM (XY)	M → B (XY ↔ SPXY)	
	XMA (XY)	M ↔ A (XY ↔ SPXY)	
	XMB (XY)	M ↔ B (XY ↔ SPXY)	
	LMAIY (X)	A → M, Y+1 → Y (X ↔ SPX)	NZ
	LMADY (X)	A → M, Y−1 → Y (X ↔ SPX)	NB
Immediate	LMIIY i	i → M, Y+1 → Y	NZ
	LAI i	i → A	
	LBI i	i → B	
Arithmetic	AI i	A + i → A	C
	IB	B+1 → B	NZ
	DB	B − 1 → B	NB
	AMC	M+A+C (F/F) → A	C
	SMC	M−A−$\overline{C}$ (F/F) → A	NB
	AM	M + A → A	C
	DAA	Decimal Adjustment (Addition)	
	DAS	Decimal Adjustment (Subtraction)	
	NEGA	$\overline{A}$ + 1 → A	
	COMB	$\overline{B}$ → B	
	SEC	1 → C (F / F)	
	REC	0 → C (F / F)	
	TC	Test C (F / F)	C (F / F)
	ROTL	Rotation Left	
	ROTR	Rotation Right	
	OR	A ∪ B → A	

(to be continued)

Group	Mnemonic code	Function	Status
Compare	MNEI i	M ≠ i	NZ
	YNEI i	Y ≠ i	NZ
	ANEM	A ≠ M	NZ
	BNEM	B ≠ M	NZ
	ALEI i	A ≦ i	NB
	ALEM	A ≦ M	NB
	BLEM	B ≦ M	NB
RAM bit Manipulation	SEM n	1 → M (n)	
	REM n	0 → M (n)	
	TM n	Test M (n)	M (n)
ROM Address	BR a	Branch on Status 1	1
	CAL a	Subroutine Jump on Status 1	1
	LPU u	Load Program Counter Upper on Status 1	
	TBR p	Table Branch	
	RTN	Return from Subroutine	
Interrupt	SEIE	1 → I/E	
	SEIF0	1 → IF0	
	SEIF1	1 → IF1	
	SETF	1 → TF	
	SECF	1 → CF	
	REIE	0 → I/E	
	REIF0	0 → IF0	
	REIF1	0 → IF1	
	RETF	0 → TF	
	RECF	0 → CF	
	TI0	Test INT_0	INT_0
	TI1	Test INT_1	INT_1
	TIF0	Test IF_0	IF_0
	TIF1	Test IF_1	IF_1
	TTF	Test TF	TF
	LTI	i → Timer/Counter	
	LTA	A → Timer/Counter	
	LAT	Timer/Counter → A	
	RTNI	Return Interrupt	
Input/Output (Display Control)	SED	1 → D (Y)	
	RED	0 → D (Y)	
	TD	Test D (Y)	D (Y)
	SEDD n	1 → D (n)	
	REDD n	0 → D (n)	
	LAR p	R (p) → A	
	LBR p	R (p) → B	
	LRA p	A → R (p)	
	LRB p	B → R (p)	
	Pp	Pattern Generation	
	NOP	No Operation	

(NOTE) 1. (XY) after a mnemonic code has four meanings as follows.

Mnemonic only	Instruction execution only
Mnemonic with X	Instruction execution, X ↔ SPX
Mnemonic with Y	Instruction execution, Y ↔ SPY
Mnemonic with XY	Instruction execution, X ↔ SPX, Y ↔ SPY

[Example]

LAM	M → A
LAMX	M → A, X ↔ SPX
LAMY	M → A, Y ↔ SPY
LAMXY	M → A, X ↔ SPX, Y ↔ SPY

2. Status column shows the factor which affects status by the instruction of status change.

NZ	ALU	Not Zeto
C	ALU	Overflow in Addition/Carry
NB	ALU	Overflow in Subtraction/No Borrow

except above .... Content of status column affects status directly.

3. Carry flip-flop is not always affected by executing the instruction which affects the Status.
Instructions which affect Carry flip-flop are eight as follows.

AMC	SEC
SMC	REC
DAA	ROTL
DAS	ROTR

4. All instructions except for P are executed in single cycle.
P is executed in 2-cycle.

Date	
Customer's Name	
ROM CODE ID	
Hitachi P/N	

LCD-III Mask Option List

(1) I/O Option

Pin Name	I/O	I/O Option A	I/O Option B	I/O Option C	Remarks	Pin Name	I/O	I/O Option A	I/O Option B	I/O Option C	Remarks
D_0	I/O					R_{00}	I				
D_1	I/O					R_{01}	I				
D_2	I/O					R_{02}	I				
D_3	I/O					R_{03}	I				
D_4	I/O					R_{10}	I/O				
D_5	I/O					R_{11}	I/O				
D_6	I/O					R_{12}	I/O				
D_7	I/O					R_{13}	I/O				
D_8	I/O					R_{20}	I/O				
D_9	I/O					R_{21}	I/O				
D_{10}	I/O					R_{22}	I/O				
D_{11}	I/O					R_{23}	I/O				
D_{12}	I/O					R_{30}	O				
D_{13}	I/O					R_{31}	O				
D_{14}	I/O					R_{32}	O				
D_{15}	I/O					R_{33}	O				
INT_0	I										
INT_1	I										

* Specify the I/O composition with a mark of "O" in the applicable composition column.
A: No pull up MOS B: With pull up MOS C: CMOS Output

(2) Oscillator & External Halt

External Halt / Oscillator	Not used	Used (Reset is applied when Halt release)	Used (Reset is not applied when Halt release)
Resistor			
Ceramic Resonator			
External Clock			

*Please check one section on the above chart.

(3) Oscillator & Internal Halt

Internal Halt / Oscillator	No (RAM contents are not kept by reset)	No (RAM contents are kept by reset)	Yes (It is provided only when the crystal for timer exists.)
Resistor			
Ceramic Resonator			
External Clock			

* Please check one section on the above chart.

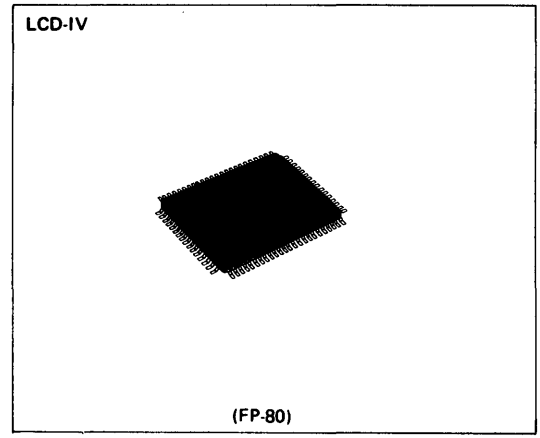
(4) Other Options

I/O State at Halt Mode	□ Enable □ Disable	
External Crystal for Timer	□ Yes □ No	If "Yes", D_{14} and D_{15} become XO and XI for connection of Crystal. Therefore, no I/O option can be selectable.
Supply Voltage	□ 5 ± 0.5V □ 2.7 to 5.5V	

* Mark "√" in "□" for the selected I/O state.

LCD—Ⅳ(HD613901)

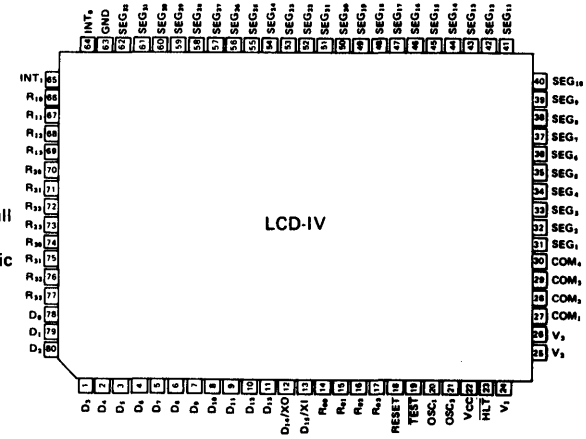
The LCD-IV is the CMOS 4-bit single chip microcomputer which contains ROM, RAM, I/O, Timer/Event Counter and Control Circuit, Direct Drive Circuit for LCD on single chip. The LCD-IV is designed to drive LCD directly and perform efficient controller function as well as arithmetic function for both binary and BCD data. With the on-chip crystal oscillator for timer, the clock function is easily realized. The CMOS technology of the LCD-IV provides the flexibility of microcomputers for battery powered and battery back-up applications in combination with low power consuming LCD.



■ FEATURES

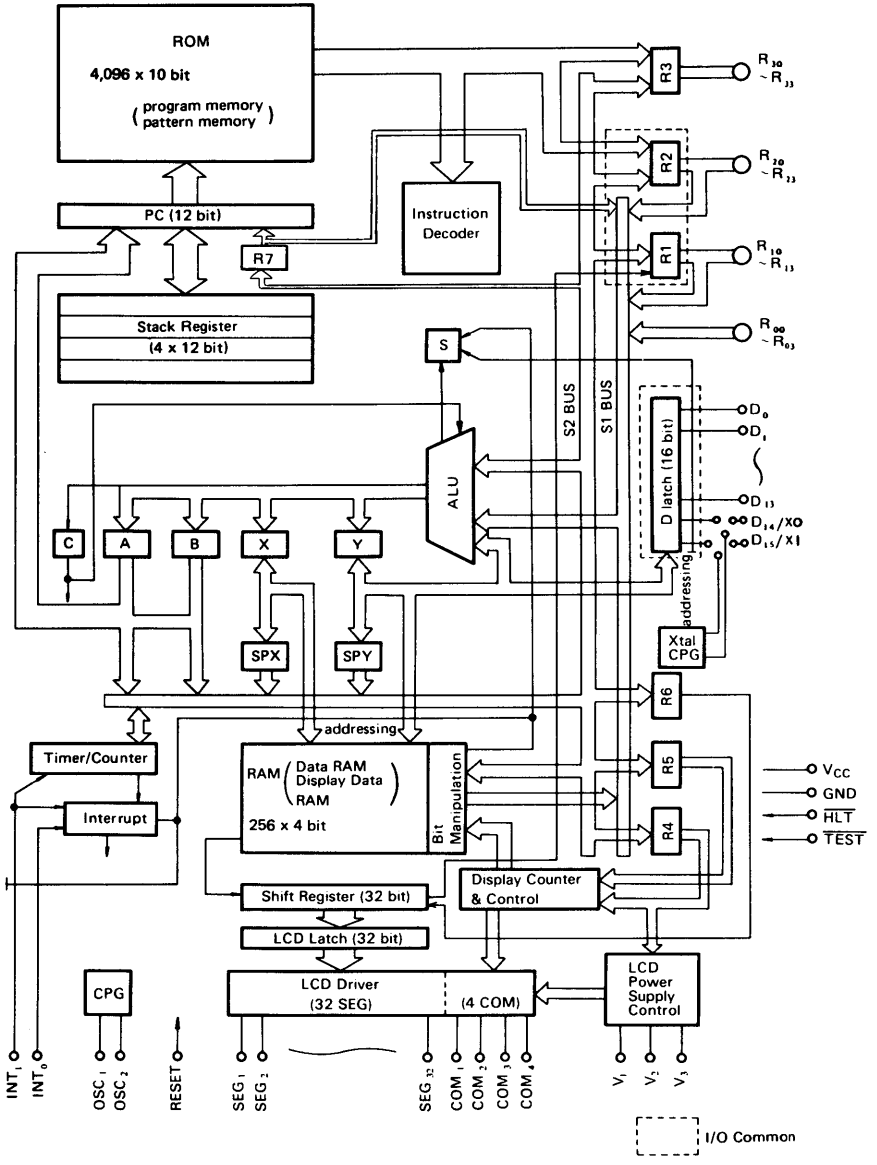
- 4-bit Architecture
- 4,096 Words of Program ROM (10 bits/Word)
- 256 Digits of Data RAM and Display Data RAM (4 bits/Digit)
- Control Circuit and Direct Drive Circuit for LCD
  - 4 Commons (Duty Ratio; Static, 1/2, 1/3, 1/4)
  - 32 Segments (Externally expandable up to 96 Segments using external Drivers HD44100Hs)
- 32 I/O Lines and 2 External Interrupt Lines
- Timer/Event Counter
- All Instructions except One Instruction; Single Word and Single Cycle
- BCD Arithmetic Instructions
- Pattern Generation Instruction
  – Table Look Up Capability –
- Powerful Interrupt Function
  - 3 Interrupt Sources
    - 2 External Interrupt Lines
    - Timer/Event Counter
  - Multiple Interrupt Capability
- Bit Manipulation Instructions for Both RAM and I/O
- Option of I/O Configuration Selectable on Each Pin; Pull Up MOS or CMOS or Open Drain
- Built-in Oscillator for System Clock (Resistor or Ceramic Filter)
- Built-in Crystal Oscillator for Timer
- Low Operating Power Dissipation
- Stand-by Mode (Halt Mode)
- 2 Versions;
  - V_{CC} = 5V ± 10%, 5 μs Instruction Cycle Time
  - V_{CC} = 2.5V to 5.5V, 20 μs Instruction Cycle Time

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%)

• ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	-0.3 to +7.0	V	
Terminal Voltage (1)	V_{T1}	-0.3 to V_{CC} +0.3	V	
Maximum Total Output Current (1)	$-\Sigma I_{O1}$	25	mA	(Note 3)
Maximum Total Output Current (2)	ΣI_{O2}	25	mA	(Note 3)
Operating Temperature	T_{opr}	-20 to +75	°C	
Storage Temperature	T_{stg}	-55 to +125	°C	

(NOTE) 1. Stresses above those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. Normal operation should be limited to those conditions specified under "ELECTRICAL CHARACTERISTICS -1" and "-2". The use beyond these conditions may cause LSI's malfunction and at the same time affects device reliability.
2. All voltages are with respect to GND.
3. Maximum Total Output Current is the total sum of output currents which can flow out or in simultaneously.
4. Power supply condition $V_{CC} \geqq V1 \geqq V2 \geqq V3 \geqq GND$ should be maintained.

- **ELECTRICAL CHARACTERISTICS – 1 (V_{CC} = 5V ± 10%, Ta = –20 to +75°C)**

Item	Symbol	Test Conditions	Value min.	Value max.	Unit	Note
Input "Low" Voltage	V_{IL}		–	1.0	V	
Input "High" Voltage	V_{IH}		V_{CC}–1.0	V_{CC}	V	(12)
Output "Low" Voltage	V_{OL}	I_{OL} = 1.6 mA	–	0.8	V	
Output "High" Voltage (1)	V_{OH1}	$-I_{OH}$ = 1.0 mA	2.4	–	V	(1)
Output "High" Voltage (2)	V_{OH2}	$-I_{OH}$ = 0.01 mA	V_{CC}–0.3	–	V	(2)
Driver Voltage Descending (COM)	Vd1	Id = 0.05 mA, V_{LCD} = 5 V	–	0.4	V	(16)
Driver Voltage Descending (SEG)	Vd2	Id = 0.01 mA, V_{LCD} = 5 V	–	0.4	V	(16)
Dividing Resistor of LCD Power Supply	Rwell		25	300	kΩ	
Interrupt Input Hold Time	t_{INT}		$2 \cdot T_{inst}$	–	μs	(14)
Output "High" Current	I_{OH}	V_{OH} = 10V	–	4	μA	(3)
Input Leakage Current	I_{IL}	V_{in} = 0 to V_{CC}	–	2	μA	(4),(12)
Pull up MOS Current	$-I_P$	V_{CC} = 5V	45	250	μA	
Supply Current (1)	I_{CC1}	V_{in} = V_{CC}, V_{CC} = 5V Ceramic Filter Oscillation (f_{osc} = 800 kHz)	–	3	mA	(5)
Supply Current (2)	I_{CC2}	V_{in} = V_{CC}, V_{CC} = 5V R_f Oscillation (f_{osc} = 800 kHz) External Clock Operation (f_{cp} = 800 kHz)	–	2	mA	(5)
Standby I/O Leakage Current	I_{LS}	$\overline{HLT}$ = 1.0V, V_{in} = 0 to V_{CC}	–	1.0	μA	(6),(12)
Standby Supply Current (1)	I_{CCS1}	V_{in} = V_{CC}, $\overline{HLT}$ = 0.2V	–	10	μA	(15)
Standby Supply Current (2)	I_{CCS2}	V_{in} = V_{CC}, $\overline{HLT}$ = 0.2V	–	120	μA	(7)
LCD Display Voltage	V_{LCD}	V_{CC}–V_3	2.5	V_{CC}	V	(11)
Frame Frequency of LCD Drive	f_F	n = 1 (static) n = 2 (1/2 Duty) n = 3 (1/3 Duty) n = 4 (1/4 Duty)	$\frac{1}{256 \times n \times T_{inst}}$		Hz	(13)
External Clock Operation; System Clock						
External Clock Frequency	f_{cp}		130	1,000	kHz	(8),(13)
External Clock Duty	Duty		45	55	%	(8)
External Clock Rise Time	t_{rcp}		0	0.2	μs	(8)
External Clock Fall Time	t_{fcp}		0	0.2	μs	(8)
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{cp}$	4.0	31.3	μs	(8)
Internal Clock Operation (R_f Oscillation); System Clock						
Clock Oscillation Frequency	f_{osc}	R_f = 62kΩ ± 2%	600	1,000	kHz	(9)
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{osc}$	4.0	6.7	μs	(9)
Internal Clock Operation (Ceramic Filter Oscillation); System Clock						
Clock Oscillation Frequency	f_{osc}	Ceramic Filter	784	816	kHz	(10)
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{osc}$	4.9	5.1	μs	(10)

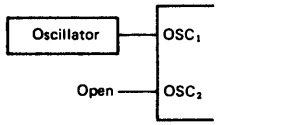
(NOTE) All voltages are with respect to GND.

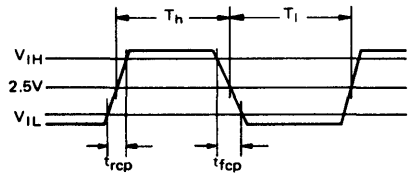
- **ELECTRICAL CHARACTERISTICS – 2 (Ta = –20 to +75°C)**

Item	Symbol	Test Conditions			Value min.	Value max.	Unit	Note
Halt Duration Voltage	V_{DH}	$\overline{HLT}$ = 0.2V			2.3	–	V	(17)
Halt Current	I_{DH}	V_{in} = V_{CC}, $\overline{HLT}$ = 0.2V, V_{DH} = 2.3V			–	4.0	μA	(17), (19)
Halt Delay Time	t_{HD}				100	–	μs	(17)
Operation Recovery Time	t_{RC}				100	–	μs	(17)
$\overline{HLT}$ Fall Time	t_{fHLT}				–	1000	μs	(17)
$\overline{HLT}$ Rise Time	t_{rHLT}				–	1000	μs	(17)
$\overline{HLT}$ "Low" Hold Time	t_{HLT}				400	–	μs	(17)
$\overline{HLT}$ "High" Hold Time	t_{OPR}	R_f Oscillation, External Clock Operation			100	–	μs	(17)
		Ceramic Filter Oscillation			4000	–		
RESET Pulse Width (1)	t_{RST1}	R_f Oscillation, External Clock Operation			5	–	ms	(18)
		Ceramic Filter Oscillation			20	–		
RESET Pulse Width (2)	t_{RST2}	External Reset, $\overline{HLT}$=V_{CC} V_{CC} = 4.5 to 5.5V	Prescaler Clock = System Clock		$2 \cdot T_{inst}$	–	μs	(18)
			Prescaler clock = D_{15}/XI clock (32×10^6/f_{oscx})	Not clear Prescaler with Reset signal	$2 \cdot T_{inst}$			
				Clear Prescaler with Reset signal	32×10^6/f_{oscx}	–		
RESET Rise Time	t_{rRST}	External Reset, $\overline{HLT}$ = V_{CC}, V_{CC} = 4.5 to 5.5V			–	100	μs	(18)
RESET Fall Time	t_{fRST}	External Reset, $\overline{HLT}$ = V_{CC}, V_{CC} = 4.5 to 5.5V			–	100	μs	(18)

(NOTE)
1. Applied to PMOS load of CMOS output pins and CMOS I/O common pins among D and R terminals.
2. Applied to CMOS output pins, CMOS I/O common pins, input pins with pull up MOS, and I/O common pins with pull up MOS among D and R terminals.
3. Applied to open-drain output pins and open-drain I/O common pins among D and R terminals.
4. Pull up MOS current is excluded.
5. Applied to the supply current when the LCD-IV is in the reset state and the crystal oscillation for timer doesn't operate. (Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded).
   Test Condition: RESET, $\overline{HLT}$, $\overline{TEST}$ = V_{CC} (Reset State)
   INT_0, INT_1, R_{00} to R_{33}, D_8 to D_{13} = V_{CC}
   D_{14}/XO, D_{15}/XI ——— D_{14}/XO, D_{15}/XI = V_{CC} (Crystal oscillation for timer is not selected).
   V_1, V_2, V_3 = V_{CC} ——— D_{14}/XO = Open, D_{15}/XI = V_{CC} (Crystal oscillation for timer is selected).
   COM_i to COM_4, SEG_1 to SEG_{32} = Open
   When the crystal oscillation for timer operates, the standby supply current (2) I_{CCS2} flows in addition to I_{CC1} or I_{CC2}. When the LCD-IV is installed in the user's system, and in operation current increases according to the external circuitry and devices. Those are connected to the LCD-IV. User should design the power supply in consideration of this point (The difference between the measured current in the above reset state and that measured in the operational state in the user's system is the increased part of the supply current).
6. Standby I/O leakage current is the leakage current of I/O pins in the "Halt" and "Disable" state.
7. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded. The standby supply current (2) is the supply current at V_{CC} = 5V ± 10% in "Halt" state in the case that the crystal oscillation for timer is selected (only the crystal oscillator for timer, 5-bit divider and 6-bit prescaler are in operation).

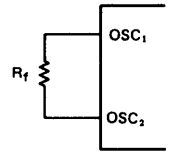
8. Applied to external clock operation (system clock).





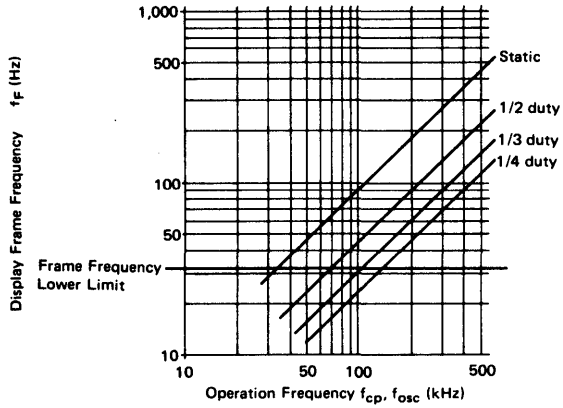
$$\text{Duty} = \frac{T_l}{T_h + T_l} \times 100\%$$

9. Applied to internal clock operation using resistor R_f. (system clock)

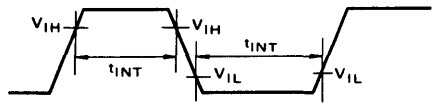


Wiring of OSC_1 and OSC_2 terminals should be as short as possible because the oscillation frequency is modified by capacitance of these terminals.

10. Applied to internal clock operation using ceramic filter. (system clock)
11. Power supply condition $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq GND$ should be maintained.
12. Applied to input pins, I/O common pins among D and R terminals, and RESET, $\overline{HLT}$, OSC_1, INT_0, INT_1 pins.
13. Lower limit of operation frequency is determined by liquid crystal display duty. Flutter occurs on liquid crystal display if frame frequency is under 32 Hz. Therefore operation frequency should be determined to prevent that frame frequency becomes under 32 Hz.
The following shows the relation between liquid crystal display frame frequency and operation frequency.

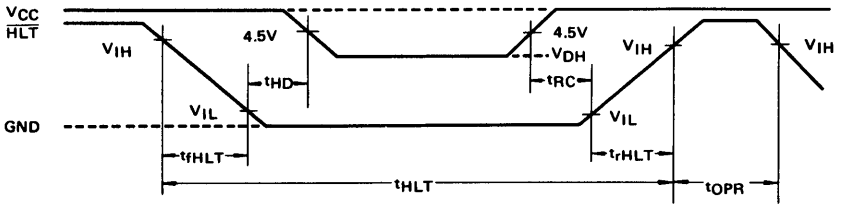


14. INT_0 and INT_1 inputs must be retained for two or more instruction cycle time at both "High" and "Low" levels.

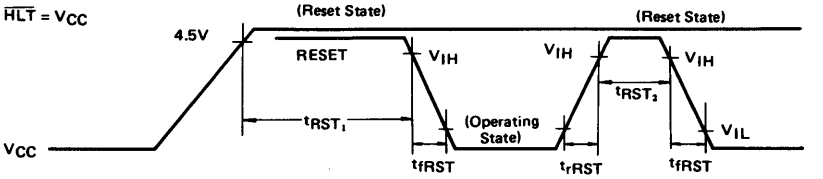


15. Power supply circuit for LCD is excluded. The standby supply current (1) is the supply at V_{CC} = 5V ± 10% in "Halt" state in the case that the crystal oscillation for timer is not selected. The supply current when supply voltage falls to the Halt Duration Voltage is called "Halt Current" (I_{DH}). (shown in ELECTRICAL CHARACTERISTICS–2)

16. The voltage that drops between the power supply terminals (V_{CC}, V_1, V_2, V_3) and each common or segment output terminal.
17. External Halt Timing Chart

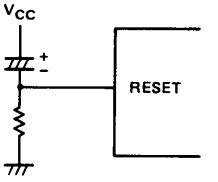


18. RESET Input Condition



- t_{RST_1} includes the time that required from the power ON until the operation gets into the constant state.
- t_{RST_2} is applied when the operation is in the constant state.

Reset circuit at power on is not installed. Simple reset circuit at power on is the following.



19. The supply current at $V_{CC} = V_{DH} = 2.3V$ in "Halt" state, in the case that the crystal oscillation for timer is not selected. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded.

■ ELECTRICAL CHARACTERISTICS (V_{CC} = 2.5 to 5.5V)

• ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	−0.3 to +7.0	V	
Terminal Voltage	V_{T1}	−0.3 to V_{CC} +0.3	V	
Maximum Total Output Current (1)	$-\Sigma I_{O1}$	25	mA	(Note 3)
Maximum Total Output Current (2)	ΣI_{O2}	25	mA	(Note 3)
Operating Temperature	T_{opr}	−20 to +75	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

(NOTE) 1. Stresses above those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. Normal operation should be limited to those conditions specified under "ELECTRICAL CHARACTERISTICS -1" and "-2". The use beyond these conditions may cause LSI's malfunction and at the same time affects device reliability.
2. All voltages are with respect to GND.
3. Maximum Total Output Current is the total sum of output currents which can flow out or in simultaneously.
4. Power supply condition $V_{CC} \geqq V1 \geqq V2 \geqq V3 \geqq$ GND should be maintained.

- **ELECTRICAL CHARACTERISTICS – 1 (V_{CC} = 2.5 to 5.5V, T_a = -20 to +75°C)**

Item	Symbol	Test Conditions	Value min.	Value max.	Unit	Note
Input "Low" Voltage	V_{IL}		–	0.15·V_{CC}	V	
Input "High" Voltage	V_{IH}		0.85·V_{CC}	V_{CC}	V	(11)
Output "Low" Voltage	V_{OL}	I_{OL} = 0.4 mA	–	0.4	V	
Output "High" Voltage (1)	V_{OH1}	$-I_{OH}$ = 0.08 mA	V_{CC}-0.5	–	V	(1)
Output "High" Voltage (2)	V_{OH2}	$-I_{OH}$ = 0.01 mA	V_{CC}-0.4	–	V	(2)
Driver Voltage Descending (COM)	Vd1	Id = 0.05 mA	–	0.5	V	(15)
Driver Voltage Descending (SEG)	Vd2	Id = 0.01 mA	–	0.5	V	(15)
Dividing Resistor of LCD Power Supply	Rwell		25	300	kΩ	
Interrupt Input Hold Time	tINT		2·T_{inst}	–	μs	(13)
Output "High" Current	I_{OH}	V_{OH} = V_{CC}	–	4	μA	(3)
Input Leakage Current	I_{IL}	V_{in} = 0 to V_{CC}	–	2	μA	(4), (11)
Pull up MOS Current	-Ip	V_{CC} = 3V	10	100	μA	
Supply Current	I_{CC}	V_{in} = V_{CC}, V_{CC} = 3V R_f Oscillation (f_{osc} = 200 kHz) External Clock Operation (f_{cp} = 200 kHz)	–	0.3	mA	(5)
Standby I/O Leakage Current	I_{LS}	$\overline{HLT}$ = 0.5V, Vin = 0 to V_{CC}	–	1	μA	(6), (11)
Standby Supply Current (1)	I_{CCS1}	Vin = V_{CC}, $\overline{HLT}$ = 0.1V, V_{CC} = 2.5 to 3.3V	–	6	μA	(14)
Standby Supply Current (2)	I_{CCS2}	Vin = V_{CC}, $\overline{HLT}$ = 0.1V, V_{CC} = 2.5 to 3.3V	–	50	μA	(7)
LCD Display Voltage	V_{LCD}	V_{CC}-V_3	2.5	V_{CC}	V	(10)
Frame Frequency of LCD Drive	f_F	n = 1 (static) n = 2 (1/2 Duty) n = 3 (1/3 Duty) n = 4 (1/4 Duty)	$\frac{1}{256 \times n \times T_{inst}}$		Hz	(12)
External Clock Operation; System Clock						
External Clock Frequency	f_{cp}		130	300	kHz	(8), (12)
External Clock Duty	Duty		45	55	%	(8)
External Clock Rise Time	t_{rcp}		0	0.2	μs	(8)
External Clock Fall Time	t_{fcp}		0	0.2	μs	(8)
Instruction Cycle Time	T_{inst}	T_{inst} = 4/f_{cp}	13.3	31.3	μs	(8)
Internal Clock Operation (R_f Oscillation); System Clock						
Clock Oscillation Frequency	f_{osc}	R_f=270kΩ±2%	V_{CC}=2.5 to 3.5V: 130	270	kHz	(9)
			V_{CC}=2.5 to 5.5V: 130	300		
Instruction Cycle Time	T_{inst}	T_{inst}=4/f_{osc}	V_{CC}=2.5 to 3.5V: 14.8	30.8	kHz	(9)
			V_{CC}=2.5 to 5.5V: 13.3	30.8		

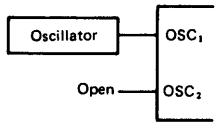
(NOTE) All voltages are with respect to GND.

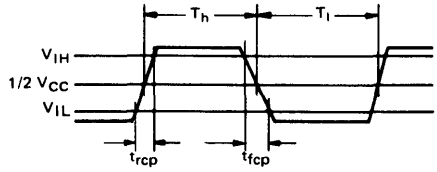
- **ELECTRICAL CHARACTERISTICS-2 (Ta = -20 to +75°C)**

Item	Symbol	Test Conditions			Value min.	Value max.	Unit	Note
Halt Duration Voltage	V_{DH}	$\overline{HLT}$ = 0.2V			2.3	–	V	(16)
Halt Current	I_{DH}	V_{in} = V_{CC}, $\overline{HLT}$ = 0.2V, V_{DH} = 2.3V			–	4.0	μA	(16), (18)
Halt Delay Time	t_{HD}				100	–	μs	(16)
Operation Recovery Time	t_{RC}				100	–	μs	(16)
$\overline{HLT}$ Fall Time	t_{fHLT}				–	1000	μs	(16)
$\overline{HLT}$ Rise Time	t_{rHLT}				–	1000	μs	(16)
$\overline{HLT}$ "Low" Hold Time	t_{HLT}				400	–	μs	(16)
$\overline{HLT}$ "High" Hold Time	t_{OPR}				100	–	μs	(16)
RESET Pulse Width (1)	t_{RST1}	External Reset, $\overline{HLT}$ = V_{CC}			10	–	ms	(17)
RESET Pulse Width (2)	t_{RST2}	External Reset, $\overline{HLT}$=V_{CC} V_{CC}=2.5V to 5.5V	Prescaler Clock = System Clock		2·Tinst	–	μs	(17)
			Prescaler Clock=D_{15} /XI Clock	Not Clear Prescaler with Reset Signal	2·Tinst			
				Clear Prescaler with Reset Signal	$\frac{32\times10^6}{foscx}$			
RESET Rise Time	t_{rRST}	External Reset, $\overline{HLT}$ = V_{CC} V_{CC} = 2.5 to 5.5V			–	100	μs	(17)
RESET Fall Time	t_{fRST}	External Reset, $\overline{HLT}$ = V_{CC} V_{CC} = 2.5 to 5.5V			–	100	μs	(17)

(NOTE) 1. Applied to PMOS load of CMOS output pins and CMOS I/O common pins among D and R terminals.
2. Applied to CMOS output pins, CMOS I/O common pins, input pins with pull up MOS, and I/O common pins with pull up MOS among D and R terminals.
3. Applied to open-drain output pins and open-drain I/O common pins among D and R terminals.
4. Pull up MOS current is excluded.
5. Applied to the supply current when the LCD-IV is in the reset state and the crystal oscillation for timer doesn't operate. (Current that flows in input/output circuit and in the power supply circuit for LCD is excluded).
   Test Condition: RESET, $\overline{HLT}$ = V_{CC} (Reset State)
   D_{14}/XO, D_{15}/XI — D_{14}/XO, D_{15}/XI = V_{CC} (Crystal oscillation for timer is not selected.)
   V_1, V_2, V_3 = V_{CC} — D_{14}/XO = Open, D_{15}/XI = V_{CC} (Crystal oscillation for timer is selected.)
   COM_1 to COM_4, SEG_1 to SEG_{32} = Open
   When the crystal oscillation for timer operates, the standby supply current (2) I_{CCS2} flows in addition to I_{CC}.
   When the LCD-IV is installed in the user's system, and in operation current increases according to the external circuitry and devices. Those are connected to the LCD-IV. User should design the power supply in consideration of this point. (The difference between the measured current in the above reset state and that measured in the operational state in the user's system is the increased part of the supply current).
6. Standby I/O leakage current is the leakage current of I/O pins in the "Halt" and "Disable" state.
7. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded. The standby supply current (2) is the supply current at V_{CC} = 2.5 to 3.3V in "Halt" state in the case that the crystal oscillation for timer is selected (only the crystal oscillator for timer, 5-bit divider and 6-bit prescaler are in operation).

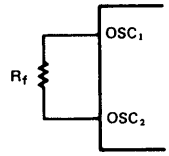
8. Applied to external clock operation. (system clock)





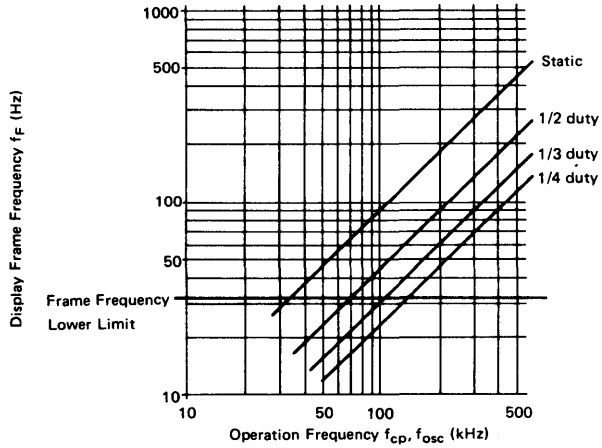
$$\text{Duty} = \frac{T_l}{T_h + T_l} \times 100\%$$

9. Applied to internal clock operation using resistor R_f. (System Clock)

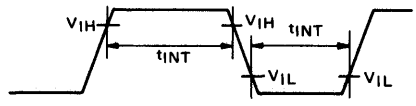


Wiring of OSC_1 and OSC_2 terminals should be as short as possible because the oscillation frequency is modified by capacitance of these terminals.

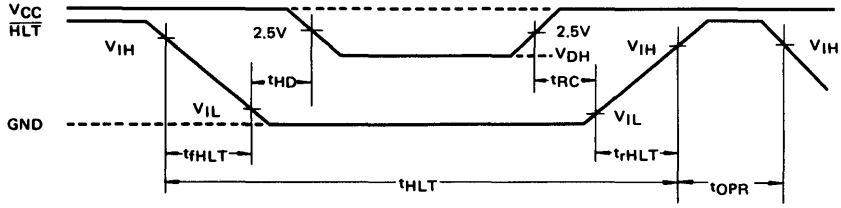
10. Power supply condition $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq GND$ should be maintained.
11. Applied to input pins, I/O common pins among D and R terminals, and RESET, $\overline{HLT}$, OSC_1, INT_0, INT_1 pins.
12. Lower limit of operation frequency is determined by liquid crystal display duty. Flutter occurs on liquid crystal display if frame frequency is under 32 Hz. Therefore operation frequency should be determined to prevent that frame frequency becomes under 32 Hz.
The following shows the relation between liquid crystal display frame frequency and operation frequency.



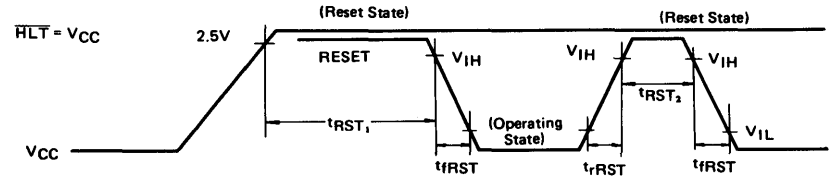
13. INT_0 and INT_1 inputs must be retained for two or more instruction cycle time at both "High" and "Low" levels.



14. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded. The standby supply current (1) is the supply at V_{CC} = 2.5 to 3.3V in "Halt" state in the case that the crystal oscillation for timer is not selected. The supply current when supply voltage fails to the Halt Duration Voltage is called "Halt Current" (I_{DH}). (shown in ELECTRICAL CHARACTERISTICS –2).
15. The voltage that drops between the power supply terminals (V_{CC}, V_1, V_2, V_3) and each common or segment output terminal.
16. External Halt Timing Chart

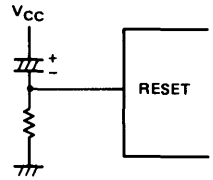


17. RESET Input Condition



- t_{RST_1} includes the time required from the power ON until the operation gets into the constant state.
- t_{RST_2} is applied when the operation is in the constant state.

Reset circuit at power on is not installed. Simple reset circuit at power on is the following.



18. The supply current at V_{CC} = V_{DH} = 2.3V in "Halt" state, in the case that the crystal oscillation for timer is not selected. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded.

■ SIGNAL DESCRIPTION

The input and output signals for the LCD-IV shown in PIN ARRANGEMENT are described in the following paragraphs.

• V_{CC} and GND

Power is supplied to the LCD-IV using these two pins. V_{CC} is power and GND is the ground connection.

• RESET

The LCD-IV can be reset by pulling RESET High.
Refer to RESET FUNCTION for additional information.

• OSC_1 and OSC_2

These pins provide control input for the on-chip clock oscillator circuit. A resistor, a ceramic filter circuit, or an external oscillator can be connected to these pins to provide a system clock with various degreeds of stability/cost trade-offs. Lead length and stray capacitance on these two pins should be minimized.

Refer to OSCILLATOR for recommendations about these pins.

• $\overline{HLT}$

This pin is used to place the LCD-IV in the HALT state (Stand-by Mode). The LCD-IV can be moved into the halt state by pulling $\overline{HLT}$ low.

In the halt state the internal clock stops and all the internal status (RAM, Registers, Carry, Status, Program Counter, and all the internal statuses) are maintained. Consequently power consumption is greatly reduced. By pulling $\overline{HLT}$ high, the LCD-IV starts operation from the status just before the halt state.

Refer to HALT FUNCTION for details of halt mode.

• $\overline{TEST}$

This pin is not for user application and must be connected to V_{CC}.

• INT_0 and INT_1

These pins provide the capability for asynchronously apply-

ing an external interrupt to the LCD-IV.
Refer to INTERRUPTS for additional information.

- **V_1, V_2 and V_3**

Power for liquid crystal display are supplied to the LCD-IV using these pins ($V_{CC} \geqq V_1 \geqq V_2 \geqq V_3 \geqq GND$).

- **R_{00} to R_{03}**

These 4 lines are a 4-bit input channel.
Refer to INPUT/OUTPUT for additional information.

- **R_{10} to R_{13}, R_{20} to R_{23}**

These 8 lines are arranged into two 4-bit Input/Output common channels.
The 4-bit register is attached to this channel. This channel is directly addressed by the operand of an instruction. I/O configuration of each pin can be specified among Open Drain and CMOS using a mask option.
Refer to INPUT/OUTPUT for additional information.

- **R_{30} to R_{33}**

These 4 lines are a 4-bit output channel.
4-bit register is attached to this channel. This channel is directly addressed by the operand of an instruction. I/O configuration of each pin can be specified among Open Drain and CMOS using a mask option.
Refer to INPUT/OUTPUT for additional information.

- **D_0 to D_{13}**

These are 14 discrete signals which can be configured as Input/Output lines.
Refer to INPUT/OUTPUT for additional information.

- **D_{14}/XO, D_{15}/XI**

D_{14}/XO and D_{15}/XI require a mask option in the following 3 types.

- Discrete I/O (common terminal)
- Crystal circuit connecting terminals (with internal halt)
- Crystal circuit connecting terminals (no internal halt)

Refer to INPUT/OUTPUT for additional information.

- **COM_1 to COM_4**

These pins are common terminals for liquid crystal display.
Refer to LIQUID CRYSTAL DISPLAY for additional information.

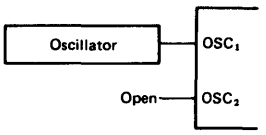
- **SEG_1 to SEG_{32}**

These pins are segment terminals for liquid crystal display.

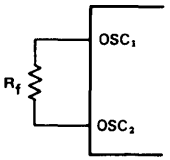
■ OSCILLATOR

The user can specify a resistor, or a ceramic filter circuit or an external oscillator by "MASK OPTION LIST".

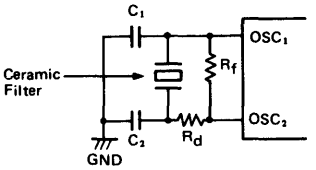
(1) External Clock



(2) Resistor



(3) Ceramic Filter (This is not applied to Low Voltage Operation Version.)



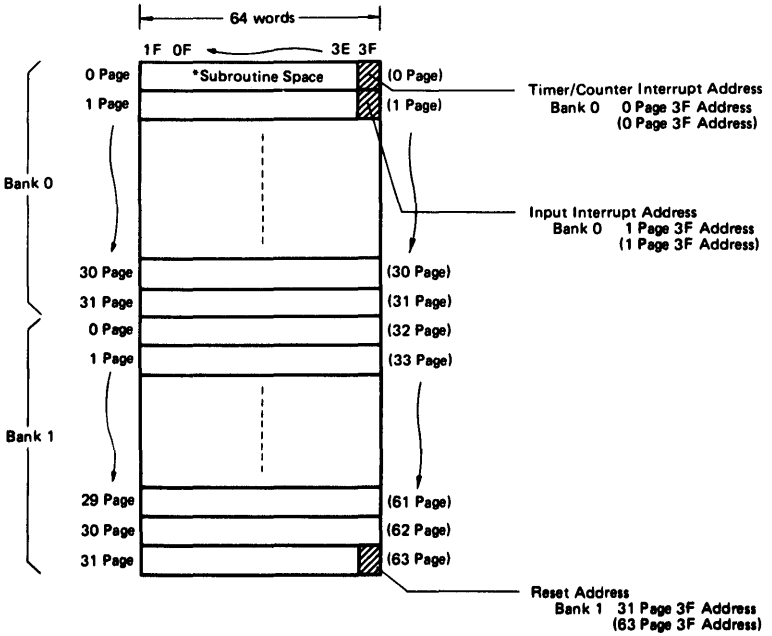
(NOTE) Configuration and constant of external parts are depend upon each applied ceramic filter.

The ceramic filter oscillation does not apply when using "Halt" and not resetting at time of "Halt" cancellation.
This circuit is the example of the typical use. As the oscillation characteristics is not guaranteed, please consider and examine the circuit constants carefully on your application.

■ ROM

- **ROM Address Space**

ROM is used as a memory for the instructions and the patterns (constants). The instruction used in the LCD-IV consists of 10 bits. These 10 bits are called "a word", which is a unit for writing into ROM
The ROM address has been split into two banks.
Each bank is composed of 32 pages (64 words/page).
The ROM capacity is 4,096 words (1 word = 10 bits) in all.
All addresses can contain both the instructions and the patterns (constants).
The ROM address space is shown in Figure 1.



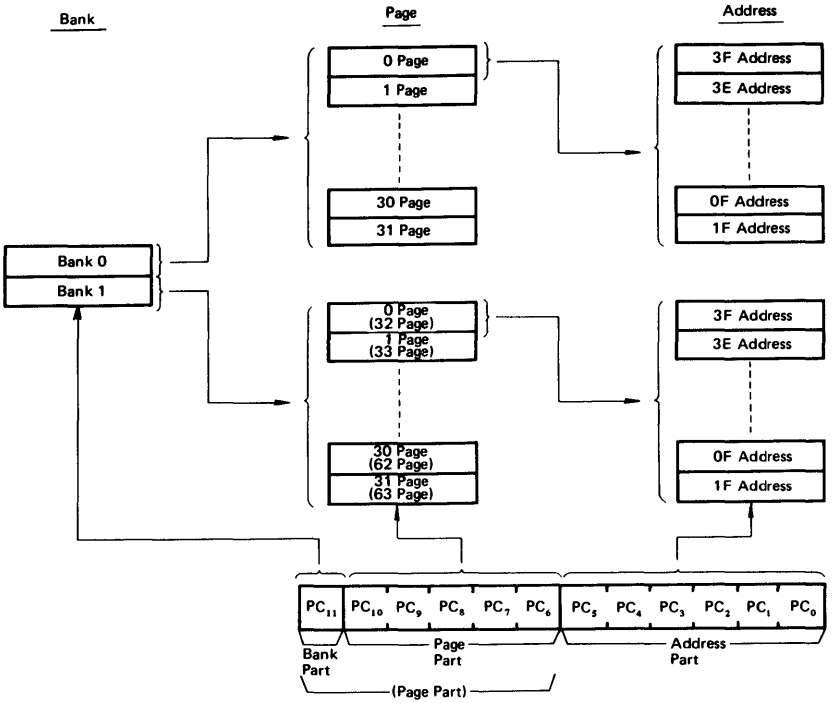
*Bank 0 0 Page (0 Page) is the Subroutine Space.

Note: The parenthesized contents are expressions of the Page, combining the bank part with the page part.

Figure 1 ROM Address Space

- **Program Counter (PC)**

The program counter is used for addressing of ROM. The program counter consists of the bank part, the page part, and the address part as shown in Figure 2.



Note: The parenthesized contents are expressions of the Page, combining the bank part with the page part.

Figure 2 Configuration of Program Counter

The bank part is a 1-bit register and the page part is a 5-bit register.

Once a certain value is loaded into the bank part or the page part, the content is unchanged until other value is loaded by a program.

The settable value is "0" (the Bank 0) or "1" (the Bank 1) for the bank part, and 0 to 31 for the page part.

The address part is a 6-bit polynomial counter and counts up for each instruction cycle time. The sequence in the decimal and hexa-decimal system is shown in Table 1. This sequence is circulating and has neither the starting nor ending point. It doesn't generate an overflow carry. Consequently, the program on a same page is executed in order unless the value of the bank part or the page part is changed.

Table 1 Program Counter Address Part Sequence

Decimal	Hexa-decimal	Decimal	Hexa-decimal	Decimal	Hexa-decimal
63	3F	5	05	9	09
62	3E	11	0B	19	13
61	3D	23	17	38	26
59	3B	46	2E	12	0C
55	37	28	1C	25	19
47	2F	56	38	50	32
30	1E	49	31	37	25
60	3C	35	23	10	0A
57	39	6	06	21	15
51	33	13	0D	42	2A
39	27	27	1B	20	14
14	0E	54	36	40	28
29	1D	45	2D	16	10
58	3A	26	1A	32	20
53	35	52	34	0	00
43	2B	41	29	1	01
22	16	18	12	3	03
44	2C	36	24	7	07
24	18	8	08	15	0F
48	30	17	11	31	1F
33	21	34	22		
2	02	4	04		

- **Designation of ROM Address and ROM Code**

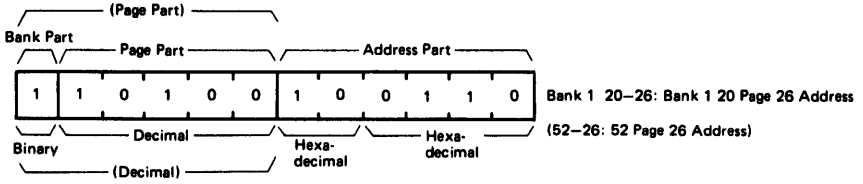
The bank part of the ROM address is shown in the binary system and the page part in the decimal system. The address part is divided into 2 bits and 4 bits, and shown in the hexa-decimal system.

It is possible to combine the bank part and the page part and show the combined part as the Page (in the decimal system). In this case, the 0 Page to the 31 Page in the Bank 1 are shown as the 32 Page to the 63 Page. The examples are shown in Figure 3.

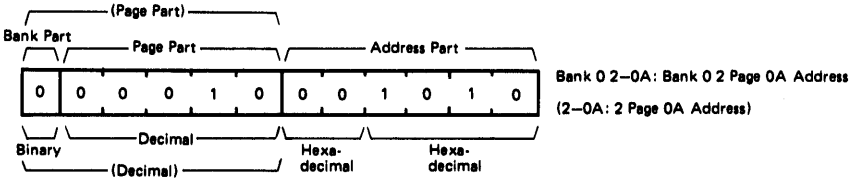
One word (10 bits) of ROM is divided into three parts (2 bits, 4 bits and 4 bits from the most significant bit O_{10} in order) shown in the hexa-decimal system. The examples are shown in Figure 3.

(a) ROM Address

(Example 1)

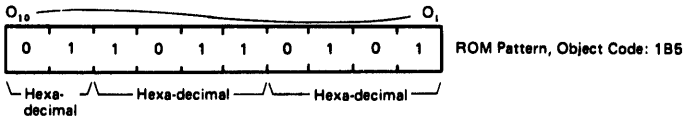


(Example 2)



(b) ROM Code

(Example 1)



(Example 2)

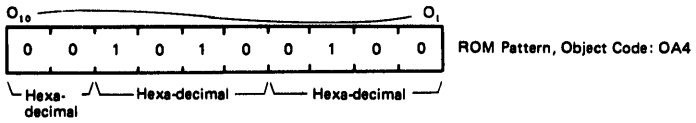


Figure 3 Designation of ROM Address and ROM Code

■ PATTERN GENERATION

The pattern (constant) can be accessed by the pattern instruction (P). The pattern can be written in any address of the ROM address space.

- **Reference**

ROM addressing for reference of the patterns is achieved by modifying the program counter with the accumulator, the B register, the Carry F/F and the operand p. Figure 4 shows how to modify the program counter. The address part is replaced with the accumulator and the lower 2 bits of B register, while the page part and the bank part are ORed with the upper 2 bits of B register, the Carry F/F and the operand p.

The value of the operand p (p_2, p_1, p_0) is 0 to 7 (decimal).

The bank part of the ROM address to be referenced to is determined by the logical equation: $PC_{11} + P_2$ (P_2 = the MSB of the operand p).

If the address where the pattern instruction exists is in the Bank 1, only the pattern of the Bank 1 can be referenced.

If the address where the pattern instruction exists is in the Bank 0, the pattern of the either Bank 1 or Bank 0 can be referenced depending on the value of p_2. The truth table of the bank part of the ROM address is shown in Table 2.

The value of the program counter is apparently modified and does not change actually. After execution of the pattern instruction, the program counter counts up and the next instruction is executed.

The pattern instruction is executed in 2-cycle time.

- **Generation**

The pattern of referred ROM address is generated as the following two ways:

(i) The pattern is loaded into the accumulator and B register.

(ii) The pattern is loaded into the Data I/O Registers R2 and R3.

Selection is determined by the command bits (O_9, O_{10}) in the pattern.

Mode (i) is performed when O_9 is "1" and mode (ii) is performed when O_{10} is "1".

Mode (i) and (ii) are simultaneously performed when both O_9 and O_{10} are "1". The correspondence of each bit of the pattern is shown in Figure 5.

Examples of the pattern instruction is shown in Table 3.

CAUTION

In the program execution, the pattern can not be distinguished from the instruction. When the program is executed at the addresses into which pattern is written, the instruction corresponding to the pattern bit is executed. Take care that a pattern is not executed as an instruction.

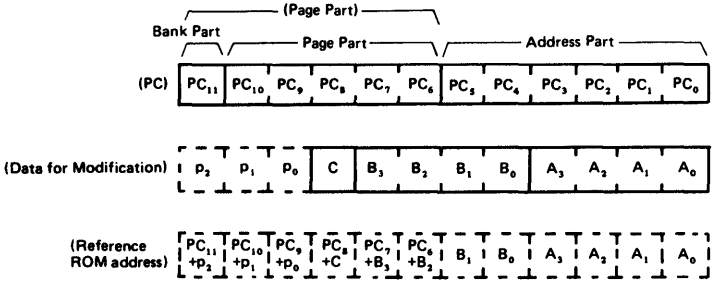


Figure 4 ROM Addressing for Pattern Generation

Table 2 Bank Part Truth Table of Pattern Generation

PC_{11}	P_2	Bank part of ROM address to be referenced to
1 (Bank 1)	1	1 (Bank 1)
	0	1 (Bank 1)
0 (Bank 0)	1	1 (Bank 1)
	0	0 (Bank 0)

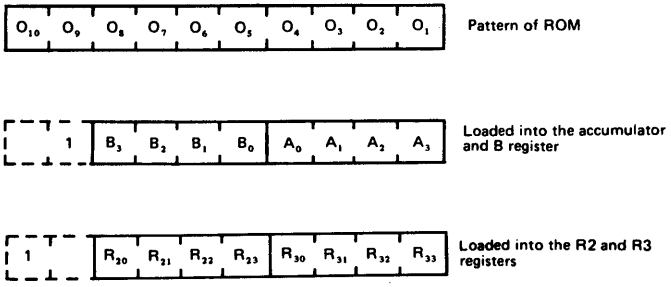


Figure 5 Correspondence of Each Bit of Pattern

Table 3 Example of Pattern Instructions

Before Execution					Referred ROM Address	ROM Pattern	After Execution			
PC	p	C	B	A			B	A	R2	R3
Bank 0 0-3F (0-3F)	1	0	A	0	Bank 0 10-20 (10-20)	12D	2	B	–	–*
Bank 0 0-3F (0-3F)	7	1	4	0	Bank 1 29-00 (61-00)	22D	–	–	4	B
Bank 1 30-00 (62-00)	4	0/1**	0	9	Bank 1 30-09 (62-09)	32D	2	B	4	B
Bank 1 30-00 (62-00)	1	0/1**	F	9	Bank 1 31-39 (63-39)	223	–	–	4	C

* "–" means that the value does not change after execution of the instruction.
** "0/1" means that either "0" or "1" may be selected.

■ **BRANCH**

ROM is accessed according to the program counter sequence and the program is executed. In order to jump to any address out of the sequence, there are four ways. They are explained in the following paragraphs.

● **BR**

By BR instruction, the program branches to an address in the current page.

The lower 6 bits of ROM Object Code (operand a, O_6 to O_1) are transferred to the address part of the program counter. This instruction is a conditional instruction and executed only when the Status F/F is "1". If it is "0", the instruction is skipped and the Status F/F becomes "1". The operation is shown in Figure 6.

● **LPU**

By LPU instruction, the jump of the bank and page is performed.

The lower 5 bits of the ROM Object Code (operand u, O_5 to O_1) are transferred to the page part of the program counter with a delay of 1 instruction cycle time. At the same time, the signal $\overline{R_{70}}$ (the reversed-phase signal of the Data I/O Register R_{70}) is transferred to the bank part of the program counter with a delay of 1 instruction cycle time. The operation is shown in Figure 7.

Consequently, the bank and page will remain unchanged in the cycle immediately following this instruction. In the next cycle, a jump of the bank and page is achieved.

This instruction (LPU) is conditional, and is executed only when the Status F/F is "1". Even after a skip, the Status F/F will remain unchanged ("0").

LPU instruction is used in combination with BR instruction or CAL instruction as the macro instruction of BRL or CALL instruction.

● **BRL**

By BRL instruction, the program branches to an address in any bank and page.

This instruction is a macro instruction of LPU and BR instructions, which is divided into two instructions as follows.

BRL a-b ⟶ LPU a
BR b

< Jump to Bank "$\overline{R_{70}}$", a Page – b Address >

BRL instruction is a conditional instruction because of characteristics of LPU and BR instructions, and is executed only when the Status F/F is "1". If the Status F/F is "0", the instruction is skipped and the Status F/F becomes "1". The examples of BRL instruction are shown in Figure 8.

● **TBR (Table Branch)**

By TBR instruction, the program branches by the table.

The program counter is modified with the accumulator, the B register, the Carry F/F and the operand p.

The method for modification is shown in Figure 9.

The bank part is determined by the logical equation: $PC_{11} + p_2$, as shown in Table 4.

If the address where TBR instruction exists is in the Bank 1,

it is possible to jump to an address only in the Bank 1, not to an address in the Bank 0.

If the address where TBR instruction exists is in the Bank 0, it is possible to jump to an address in either the Bank 1 or the Bank 0 depending on the value of the operand p_2.

TBR instruction is executed regardless of the Status F/F, and does not affect the Status F/F.

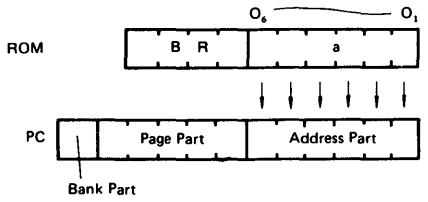


Figure 6 BR Operation

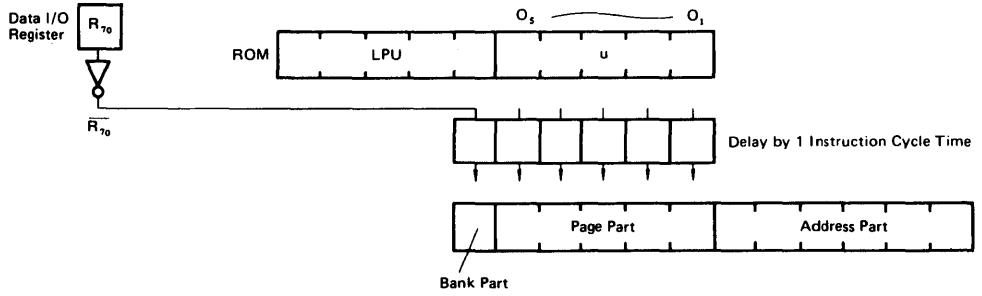


Figure 7 LPU Operation

```
Branch to Bank 0
  LAI   15
  LRA   7      R70 = "1" (R70 = "0")
  LPU   5      BRL 5-3F
  BR    3F     (Branch to Bank 0 5-3F (5-3F))

  LAI   15
  LBA
  LRA   7      R70 = "1" (R70 = "0")
  COMB
  LPU   31     BRL 31-3F
  BR    3F     (Branch to Bank 0 31-3F (31-3F))

Branch to Bank 1

  LAI   0
  LRA   7      R70 = "0" (R70 = "1")
  LPU   15     BRL 15-3F
  BR    3F     (Branch to Bank 1 15-3F (47-3F))

  LAI   0
  LTA
  LRA   7      R70 = "0" (R70 = "1")
  LYI   2
  XMA
  LPU   10     BRL 10-2E
  BR    2E     (Branch to Bank 1 10-2E (42-2E))
```

Figure 8 BRL Example

Table 4 Bank Part Truth Table of TBR Instruction

PC_{11}	P_2	Bank Part of PC after TBR
1 (Bank 1)	1	1 (Bank 1)
	0	1 (Bank 1)
0 (Bank 0)	1	1 (Bank 1)
	0	0 (Bank 0)

■ SUBROUTINE JUMP

There are two types of subroutine jumps. They are explained in the following paragraphs.

● CAL

By CAL instruction, subroutine jump to the Subroutine Space is performed.

The Subroutine Space is the Bank 0 0 Page (0 Page).

The address next to CAL instruction address is pushed onto the Stack ST1 and the contents of the stacks ST1, ST2 and ST3 are pushed onto the stacks ST2, ST3 and ST4 respectively as shown in Figure 10.

The bank part of the program counter becomes the Bank 0 and the page part becomes the 0 Page. The lower 6 bits (operand a, O_6 to O_1) of the ROM Object Code is transferred to the address part of the program counter.

The LCD-IV has 4 levels of stack (ST1, ST2, ST3 and ST4) which allows the programmer to use up to 4 levels of subroutine

jumps (including interrupts).

CAL is a conditional instruction and executed only when the Status F/F is "1". If the Status F/F is "0", it is skipped and the Status F/F changes to "1".

- **CALL**

By CALL instruction, subroutine jump to an address in any bank and page is performed.

Subroutine jump to any address can be implemented by the subroutine jump to the page specified by LPU instruction in the bank designated by the reversed-phase signal $\overline{R_{70}}$.

This instruction is a macro instruction of LPU and CAL instructions, which is divided into two instructions as follows.

```
CALL    a-b ----------> LPU  a
                        CAL  b
```

< Subroutine Jump to Bank "$\overline{R_{70}}$", a Page – b Address >

CALL instruction is conditional because of characteristics of LPU and CAL instructions and is executed when the Status F/F is "1". If the Status F/F is "0", the instruction is skipped and the Status F/F changes to "1". The examples of CALL instruction are shown in Figure 11.

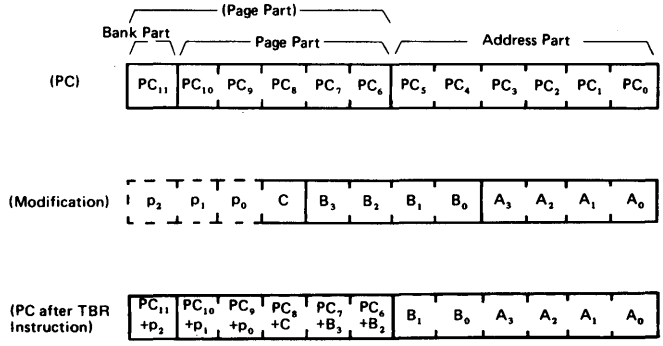


Figure 9 Modification of Program Counter by TBR Instruction

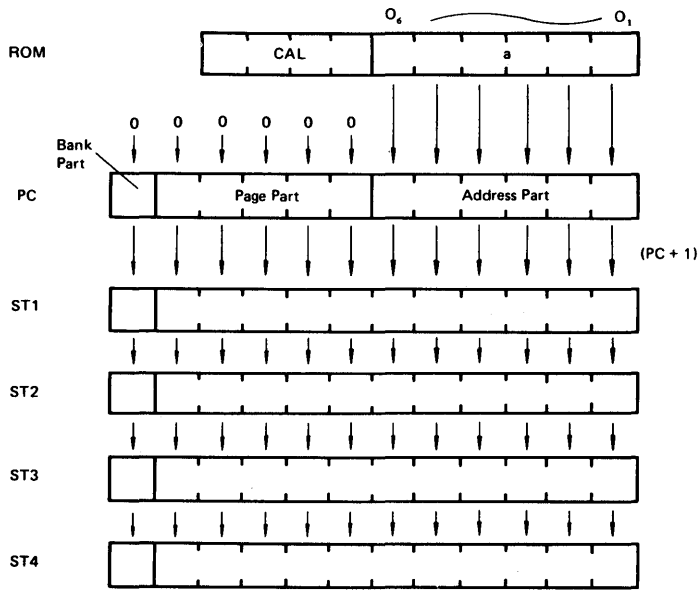


Figure 10 Subroutine Jump Stacking Order

```
Subroutine Jump to Bank 0
  LAI    15
  LRA    7        R70 = "1" (R70 = "0")
  LPU    5  }     CALL 5-3F
  CAL    3F }     (Subroutine Jump to Bank 0 5-3F (5-3F))

  LAI    15
  LBA
  LRA    7        R70 = "1" (R70 = "0")
  COMB
  LPU    31 }
  CAL    3F }     CALL 31-3F
                  (Subroutine Jump to Bank 0 31-3F (31-3F))
Subroutine Jump to Bank 1
  LAI    0
  LRA    7        R70 = "0" (R70 = "1")
  LPU    15 }
  CAL    3F }     CALL 15-3F
                  (Subroutine Jump to Bank 1 15-3F (47-3F))

  LAI    0
  LTA
  LRA    7        R70 = "0" (R70 = "1")
  LYI    3
  XMA
  LPU    10 }
  CAL    2E }     CALL 10-2E
                  (Subroutine Jump to Bank 1 10-2E (42-2E))
```

Figure 11 CALL Example

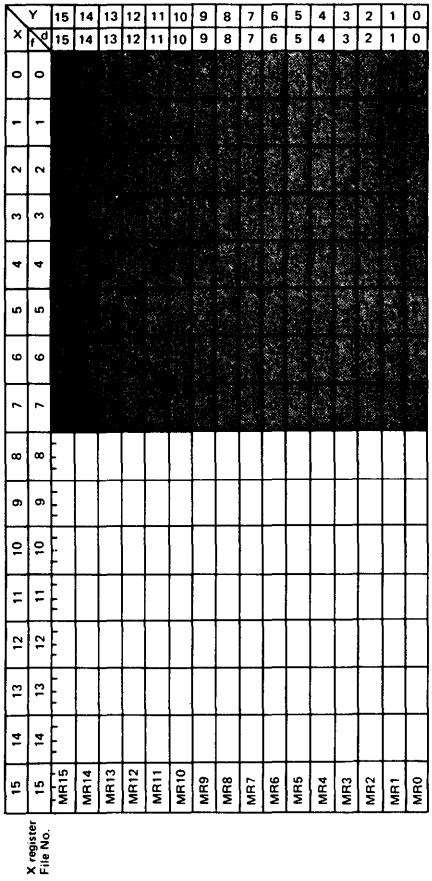
■ RAM

RAM is the memory used for data storage and register save (data RAM) and storage of segment data for liquid crystal display (display data RAM). Its capacity is 256 digits (1,024 bits) where one digit consists of 4 bits.

(Note 1) Capacity of display data RAM varies by contents of display, and capacity of data RAM changes corresponding to the former.

(Note 2) On the LCD-IV, RAM contents is not broken at system reset.

Addressing of RAM is performed by a matrix of the file No. and the digit No. Normally the file No. is set to X and the digit No. is set to Y, then the matrix of X and Y addresses RAM and performs the Read/Write operation. Special digits in RAM can be addressed without the use of X and Y. These digits are called as memory ragister (MR) and the number is 16 (MR0 ~ MR15). Memory register can be exchanged for A register by XAMR instruction. RAM address space is shown in Figure 12.

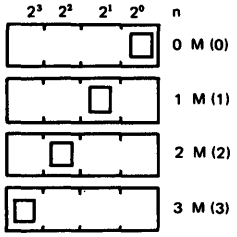


(NOTE) The area marked as ▭ is usable only for data.
The area marked as ▬ is usable for both liquid crystal display and data.

Figure 12 RAM Address Space

In case of the instructions which consists of a simultaneous Read/Write operations of RAM (exchange of RAM and a register), the writing data doesn't affect the reading data because the read operation is followed by the write operation.

RAM bit manipulation is usable, which performs any bit set (SEM), reset (REM) or test (TM) of the addressed RAM. Bit assignment is made by the program as shown below.



The bit test makes the status "1" when the assigned bit is "1" and makes it "0" when the assigned bit is "0"

■ REGISTERS

The LCD-IV has six 4-bit registers and two 1-bit registers available to the programmer. 1-bit registers are Carry F/F and Status F/F. They are explained in the following paragraphs.

• Accumulator (A; A Register) and Carry F/F (C)

The result of ALU operation (4 bits) and the overflow of the ALU are put into the accumulator and Carry F/F. Carry F/F can be set, reset or tested. Combination of the accumulator and Carry F/F can be right or left rotated. The accumulator is the main register for ALU operation and Carry F/F is used to store the overflow generated by ALU operation when the calculation of two or more digits (4 bits/digit) is performed.

• B Register (B)

The result of ALU operation (4 bits) is put into this register. B register is used as a sub-accumulator to stack the data temporarily and also used as a counter.

• X Register (X)

The result of ALU operation (4 bits) is put into this register. X register has exchangeability for SPX register. X register addresses the RAM file.

• SPX Register (SPX)

SPX register has exchangeability for X register.
SPX register is used to stack X register and expand the addressing system of RAM in combination with X register.

• Y Register (Y)

The result of ALU operation (4 bits) is put into this register. Y register has exchangeability for SPY register. Y register can calculate itself simultaneously with transferring the data by bus lines, which is usable for the calculation of two or more digits (4 bits/digit). Y register addresses the RAM digit and 1-bit discrete input/output common terminals.

• SPY Register (SPY)

SPY register has exchangeability for Y register. SPY register is used to stack Y register and expand the addressing system of RAM and 1-bit discrete input/output common terminals in combination with Y register.

• Status F/F (S)

Status F/F latches the result of logical or arithmetic operations (Not Zero, Overflow) and bit test operations. Status F/F affects conditional instructions (LPU, BR and CAL). These instructions are executed only when Status F/F is "1". If it is "0", these instructions are skipped and Status F/F becomes "1".

■ INPUT/OUTPUT

• Discrete I/O (D Terminal)

The discrete I/O is composed of 1-bit latch and I/O pin. Figure 13 shows the basic block diagram.

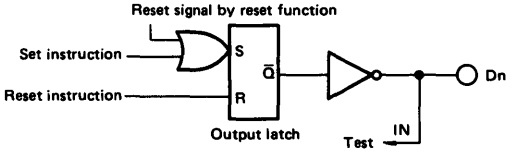


Figure 13 Discrete I/O Block Diagram

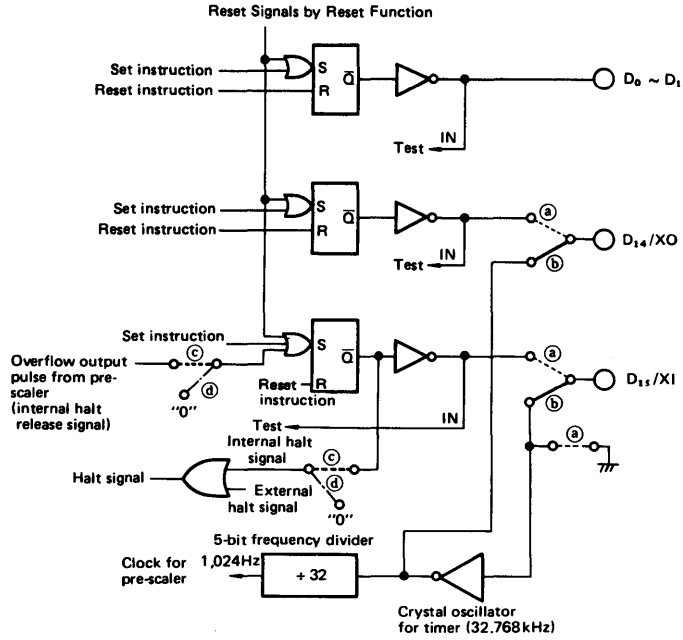


Figure 14 Mask Option of D_{14} and D_{15} Terminals

D_0 to D_{13} are discrete I/O's of common for input and output, D_{14} and D_{15} require a mask option in 3 types. When the crystal oscillation for timer is selected and the latches of D_{14} and D_{15} are not connected to the terminals, D_{14} and D_{15} can be used as 1-bit general purpose registers that can be set, reset and tested. Furthermore, if there is internal halt mode, latch of D_{15} is used as a register for internal halt mode specially.

In such case, since D_{15} means internal halt state and D_{15} = "1" means operating state, LSI can be in internal halt state by resetting D_{15} using an instruction. The prescaler keeps its operation in internal halt state. Therefore, D_{15} may be set by overflow output pulse from the prescaler to return to operating state. For details of internal halt mode, refer to HALT FUNCTION.

Table 5 Mask Option of D_{14}/XO and D_{15}/XI Terminals

Mask Option		a	b	c	d	Function of D_{14}/XO and D_{15}/XI	Function of D_{14}/XO and D_{15}/XI latch
1	Unselectable crystal oscillation for timer (no internal halt)	short	open	open	short	discrete I/O (common terminal)	Output Latch
2	Selectable crystal oscillation for timer — with internal halt	open	short	open	short	Crystal Circuit Connecting Terminal	1-bit register
3	Selectable crystal oscillation for timer — no internal halt	open	short	short	open	Crystal Circuit Connecting Terminal	D_{14} ; 1-bit register D_{15} ; register for internal halt

(NOTE) Users can specify this mask option in "The format of I/O channels" at ROM order.

Discrete I/O is addressed by Y register, and the set/reset instruction is executed for the addressed latch. "0" and "1" level can be tested with the addressed terminal and 1-bit register against the I/O common pins and 1-bit register. The test is performed with the wired logic of the output latch and the pin input. Therefore, in the case of the I/O common pins, the output latch should be in the high impedance state when the test instruction is executed. In order to test the pin input, it is necessary the state that the output latch should not affect the pin input.

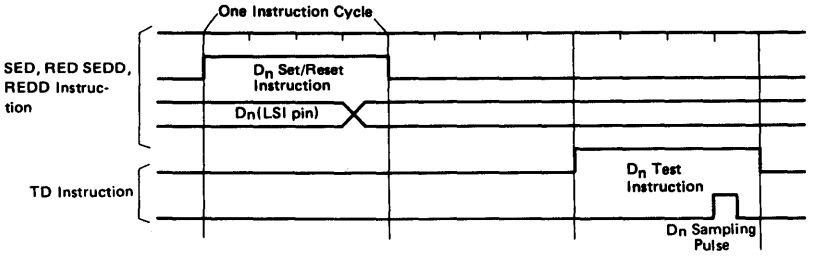


Figure 15 Timing Chart of Discrete I/O

- **Data I/O (R Terminal)**

Table 6 Data I/O for the LCD-IV

I/O common channel	R1, R2 (2 channels)
Input channel	R0 (1 channel)
Output channel	R3 (1 channel)
Total	4 channels

(NOTE) In addition to the above, R4, R5 and R6 are provided as register setting liquid crystal display mode. In these registers, there is no terminal and exists only data I/O register each, which controls liquid crystal display mode. Data is transferred to R4, R5 and R6 by LRA or LRB instruction, same as data transfer to data I/O registers of R1, R2 and R3. For details of R4, R5 and R6, refer to LIQUID CRYSTAL DISPLAY.

4-bit register (data I/O register) each is attached to an I/O common channel and output channel. No register is attached to input channel. Addressing to all channels is performed by programs (addressed by operands in instructions).

Figure 16 shows the block diagram of each channel.

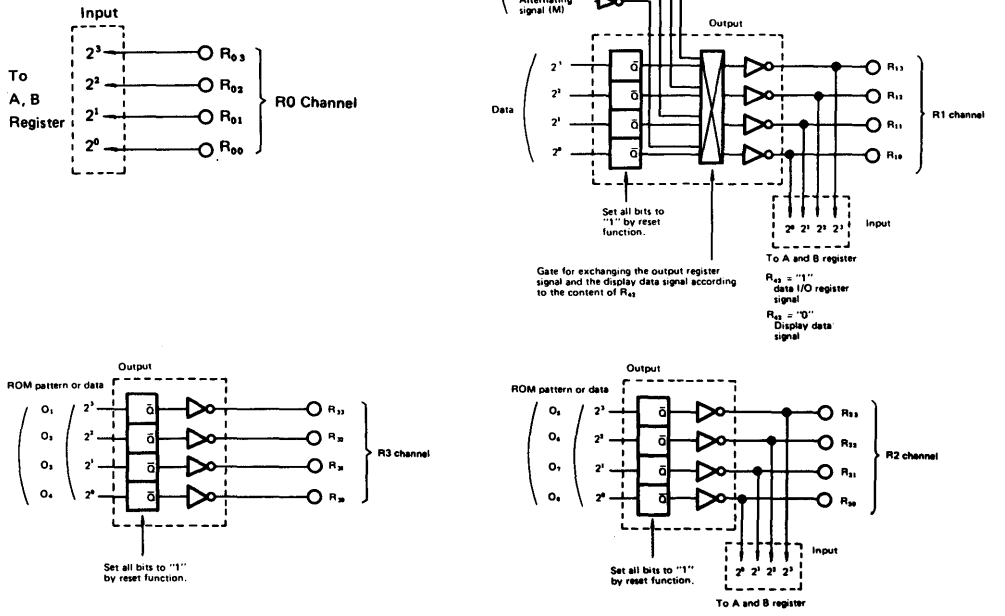


Figure 16 Data I/O Block Diagram

When expansion of segment signal for liquid crystal display is designated by a program (Register R_{42} = "0"), R1 is used as a display data output terminal. This prohibits R1 to be used as an I/O common channel by users (Refer to Figure 16, R1 channel).

If LRA or LRB instruction is executed at the time, data is transferred to data I/O register, but the content of data I/O register is not output from R1. If LAR or LBR instruction is executed, display data is inputted to accumulator (A register) or B register.

Data is transferred from the accumulator (A register) and B register to data I/O registers R1, R2, and R3 through the bus line. In addition, ROM bit patterns can be transferred to R2 and R3 by pattern generation instructions.

4-bit data can be inputted to the accumulator (A register) and B register from R0, R1 and R2 channels by input instructions. However, in the case of I/O common channels R2 and R3, since data I/O register outputs are connected to terminals, inputs are done to wired logic of register output and terminal input information. For this reason, to input terminal input signal, registers must be set to a state that would not affect the terminal input.

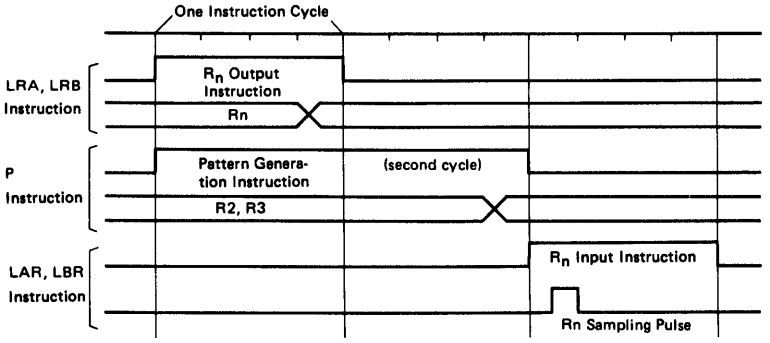
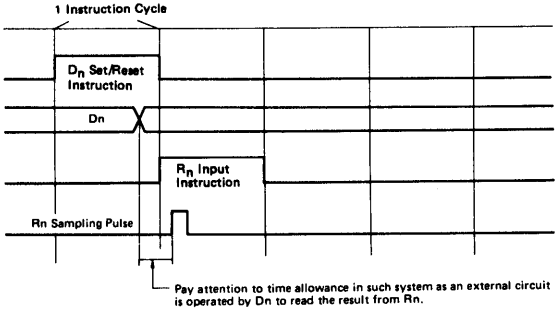


Figure 17 Data I/O Timing Chart

Pay attention: When executing an input instruction to output channel, the microcomputer reads unstabilized value causing malfunction of the program.

When executing an input instruction (LAR and LBR) from the data I/O, pay attention to time allowance after executing an output instruction. At the time, the input sampling pulse is generated during the first half of the instruction cycle.



Applied Pins: INT_0, INT_1, R_{00} to R_{03}

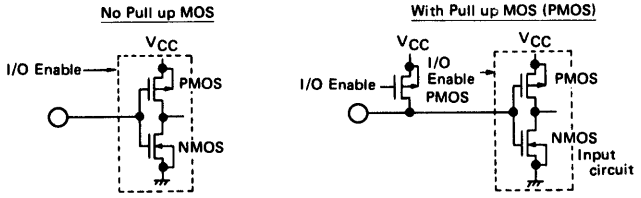


Figure 18 Configuration of Input Pins

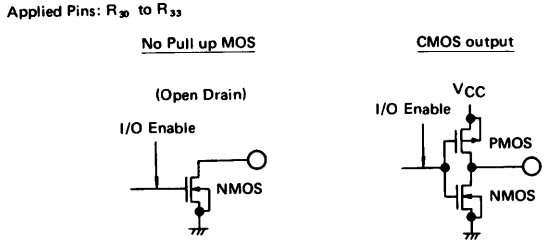


Figure 19 Configuration of Output Pins

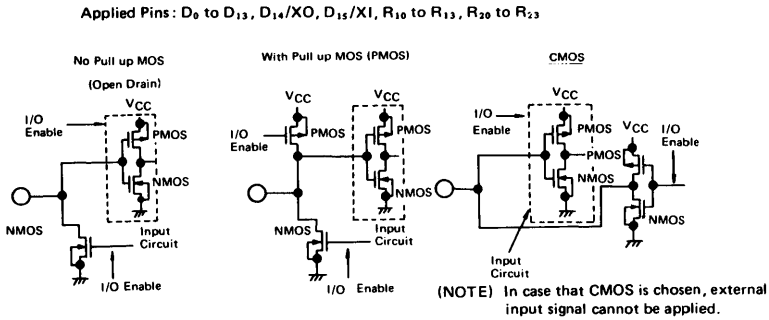


Figure 20 Configuration of Input/Output Pins

■ TIMER/COUNTER

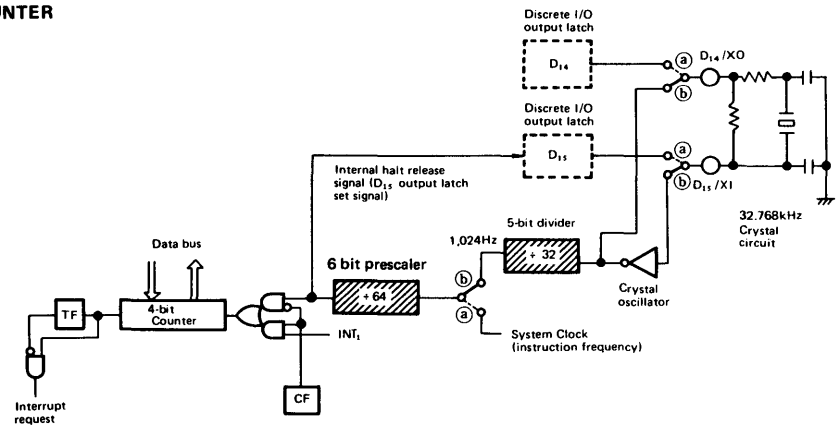


Figure 21 Timer/Counter Block Diagram

Timer/Counter Block Diagram is shown in Figure 21. 5-bit divider divides the crystal oscillation (32.768kHz) by 32 and generates clocks of 1,024Hz in the crystal oscillation mode. It does not stop in the halt state. Prescaler divides the system clock (instruction frequency) or 1,024Hz clock by 64 and generates overflow output pulse of "Instruction frequency/64Hz" or 16Hz. In the crystal oscillation mode, it does not stop during halt state. The input of the 4-bit counter is overflow output pulse of the prescaler or a pulse of INT_1 terminal. Input selection is determined by CF state. Data can be exchanged between the counter and bus by LTI, LTA or LAT instruction. TF is a flip-flop which masks the interrupt of timer/counter.

The timer is operable in 2 modes (timer mode and counter mode) depending on what to count, and the mode is selected by programs.

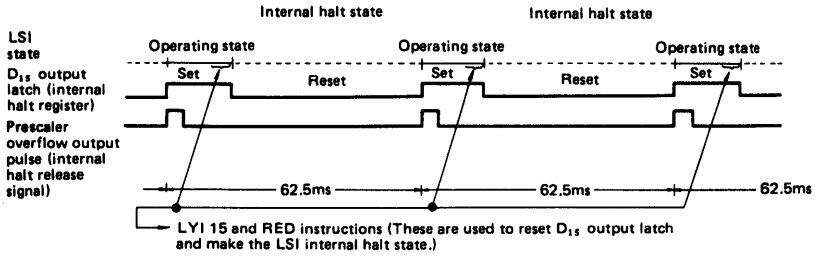
- **Timer Mode**

The 4-bit counter counts prescaler overflow output pulses. One of the following two can be selected as the prescaler count clock by the mask option.

1. System clock (Instruction frequency)
2. 1,024Hz clock (Crystal oscillation for timer is selected.) . . . Clock obtained by dividing the crystal oscillation (32.768kHz) for timer by 32. Crystal oscillator is constructed between D terminals of D_{14} and D_{15}:

Note 1) In this case, the overflow output pulses form the prescaler are 16Hz. These pulses are counted by the 4-bit counter to generate an interrupt from 16Hz to 1Hz.

Note 2) In this case, the part marked with ▨ in Figure 21 Timer/Counter does not stop even in halt state. When using "internal halt mode" among the halt function, internal halt state is generated by resetting the register for internal halt mode (D latch: D_{15}) by an instruction (D_{15} = "0": internal halt state, D_{15} = "1": operating state), and all the operation stop. In this case, overflow output pulses from the prescaler work as the signals releasing the internal halt state and set the D_{15} output latch. Therefore, if an overflow output pulse from the prescaler is generated, internal halt state is released, and the LSI starts to operate.
By utilizing this function, intermittent operation is possible, that is, program execution for necessary processing (for example, counting for clock function) starts after every 62.5 msec (16Hz) and the LSI stops after execution of this program by an instruction which makes the LSI into internal halt state. This reduces the time in which the LSI operates, resulting in power consumption in substance.



Figue 22 Set/Reset Operation Using Crystal Oscillator for Timer

- **Counter Mode**

Counts pulse of INT_1 terminal.

(Note) The width of INT_1 pulse in the counter mode must be at least 2-cycle time for both the "High" and "Low" levels.

The relation between the specified value of the counter and specified time in the Timer Mode are shown in Table 7 and 8.

Table 7 Timer Range (Prescaler clock: system clock)

Specified Value	Number of Cycles	*Time (ms)	Specified Value	Number of Cycles	*Time (ms)
0	1,024	5.12	8	512	2.56
1	960	4.80	9	448	2.24
2	896	4.48	10	384	1.92
3	832	4.16	11	320	1.60
4	768	3.84	12	256	1.28
5	704	3.52	13	192	0.96
6	640	3.20	14	128	0.64
7	576	2.88	15	64	0.32

* Time is based on instruction frequency 200kHz. (One Instruction Cycle Time (T_{inst}) = 5μs)

Table 8 Timer Range (Prescaler clock: 1,024 Hz)

Specified Value	* Time (ms)	Frequency (Hz)	Specified Value	* Time (ms)	Frequency
0	1,000	1	8	500	2
1	937.5	1.07	9	437.5	2.29
2	875	1.04	10	375	2.67
3	812.5	1.23	11	312.5	3.20
4	750	1.33	12	250	4
5	687.5	1.45	13	187.5	5.33
6	625	1.60	14	125	8
7	562.5	1.78	15	62.5	16

* Time is based on crystal oscillation for timer 32.768 kHz.

■ INTERRUPT

There are interrupt caused by the timer/counter or the inputs. Each interrupt cause has the interrupt request F/F and the request is latched into this flip-flop when it is generated. If an interrupt can be accepted, the interrupt is generated.

It is controlled by Interrupt Enable F/F (I/E F/F) whether an interrupt can be accepted or not.

Figure 23 shows the interrupt block diagram and Figure 24 shows the interrupt timing chart.

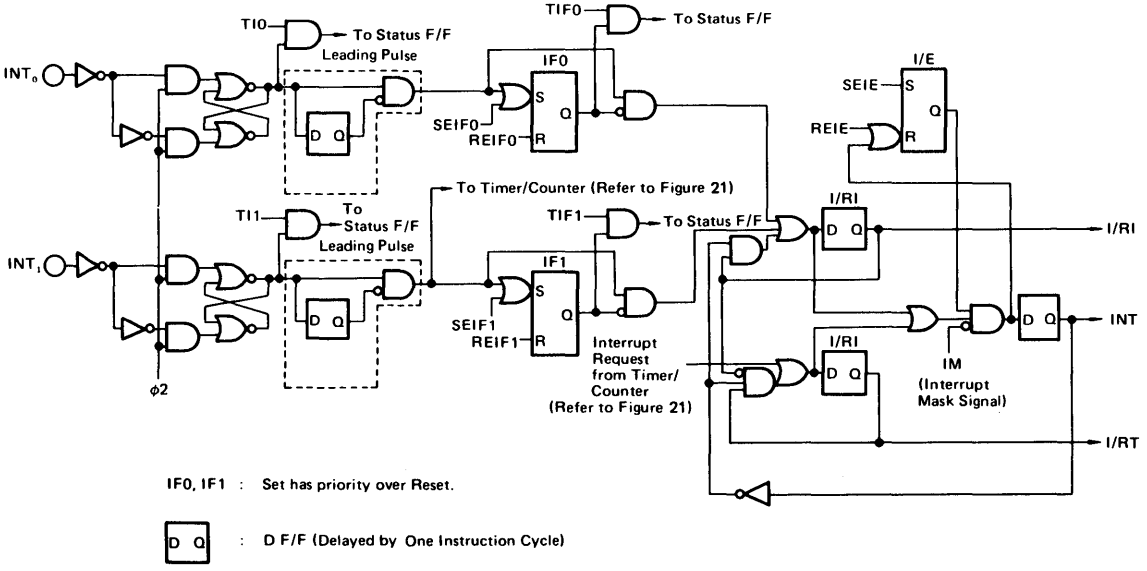


Figure 23 Interrupt Circuit Block Diagram

The status is unchanged. (The interrupt is different from general CAL in regard to this matter.)

Stacking of registers is performed by the program. Returning from the interrupt routine is performed in the same way as that from normal subroutine. But it is convenient to use RTNI (Return Interrupt) which sets the I/E simultaneously with RTN.

An interrupt is generated irrespectively of the condition of stack registers, so enough stack registers are needed.

TF, IF0, or IF1 is flip-flop where the set has priority over the reset. It is not reset when the reset instruction is issued simultaneously with OVF of the timer/counter or the leading edge of the input, though the interrupt request is generated and latched into I/RI or I/RT.

The interrupt processing caused by the interrupt generation is basically the subroutine jump and the jumping location in memory is fixed as:

Interrupt of the timer/counter
Bank 0 0 page 3F address (00–3F)

Interrupt of the inputs
Bank 0 1 page 3F address (01–3F)

In addition,
The saving operation of PC → ST1 → ST2 → ST3 → ST4.

I/E reset

- **Interrupt of the Inputs**

Two pins INT_0 and INT_1 have the interrupt request functions. They have the leading pulse generation circuit and the interrupt mask F/F (IF0, IF1). When IF0 or IF1 is reset, the interrupt request is able to generate interrupt mask release. When INT_0 or INT_1 changes from "0" to "1" ("Low" level → "High" level), the leading pulse is generated and generates the interrupt request. Then IF0 or IF1 is set, the interrupt is masked.

The interrupt request generated by the leading pulse is latched in the interrupt request F/F on the input side (I/RI). If interrupt Enable F/F (I/E) is "1", the interrupt is generated immediately and I/RI is reset. But if Interrupt Enable F/F (I/E) is "0", I/RI is held at "1" level until it gets into the Interrupt Enable state.

IF0, IF1, INT_0 and INT_1 can be tested by the program. Therefore, they can also be used as normal input terminals or latch terminals of momentary pulse input.

The interrupt pulse width (at both "High" and "Low" levels) should be more than two-cycle.

- **Interrupt of the Timer/Counter**

The interrupt request of the timer/counter is latched into the interrupt request F/F of the timer (I/RT). Then I/RT operates in the same way as I/RI, but the interrupt of the input has priority over that of the timer. Therefore, the input interrupt is processed when both of I/RI and I/RT are at "1" level (interrupt requests are simultaneously generated). During the input interrupt, I/RT remains set. Thus, after the input interrupt, the timer/counter interrupt can be processed.

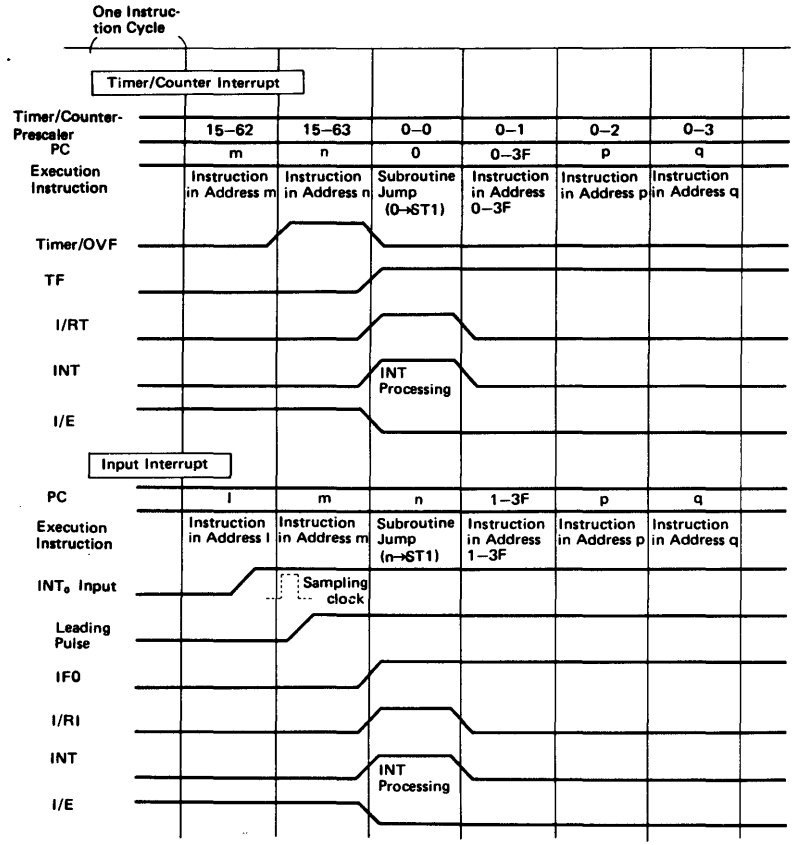


Figure 24 Interrupt Timing Chart

■ LIQUID CRYSTAL DISPLAY

● Liquid Crystal Display Circuit

The LCD-IV can directly drive the liquid crystal display panel of static, 1/2 duty factor, 1/3 duty factor and 1/4 duty factor.

The LCD-IV has 4 common signal terminals and 32 segment signal terminals. Further, if liquid crystal driver LSI (HD44100H) is connected to the LCD-IV, up to 96 segment signal terminals can be extended externally. Thus, in addition to the internal 32 terminals, total 128 segment signal terminals can be driven.

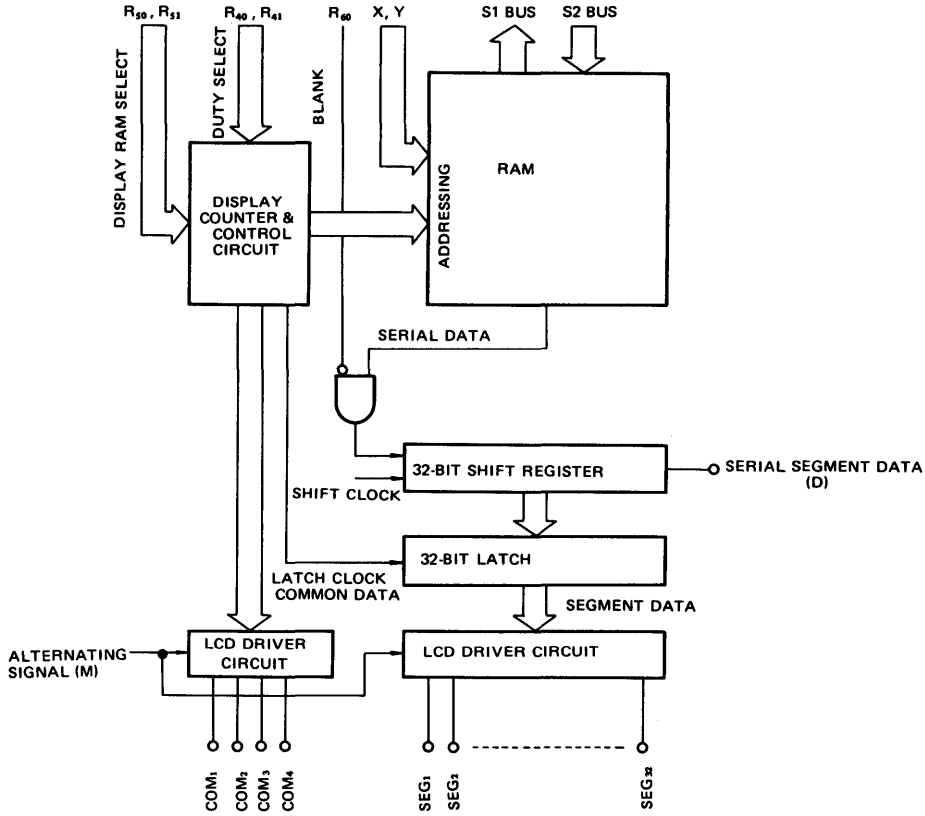


Figure 25 Liquid Crystal Display Circuit Block Diagram

Display is automatically executed by writing segment data into RAM for LCD. The RAM reads segment data bit by bit sequentially every one instruction cycle upon receiving address signal from the display counter and the control circuit. Every time common signal is scanned, the RAM reads 128-segment data (SEG_1 to SEG_{128}), which is correspond to common signal selected at the next time. Scan of common signal is executed every 256-instruction cycle. Therefore, the data which is correspond to 128-segment is read twice at the same time. The serial data read is converted to parallel data by the shift register and latch, converted to LCD drive signal by the liquid crystal driver and the outputted from a segment terminal. 32-segment (SEG_1 to SEG_{32}) out of 128-segment serial data is used within the LCD-IV, and the rest (96-segment) is outputted to liquid crystal driver LSI HD44100H which is connected to the LCD-IV and is converted to LCD drive signal in the HD44100H at the time of designation of with liquid crystal segment output extension. Cycle of the latch clock is 256-instruction cycle in the LCD-IV. In the case of dynamic drive, data at the common side changes synchronously with the latch clock. These display operations are all executed regardless of program.

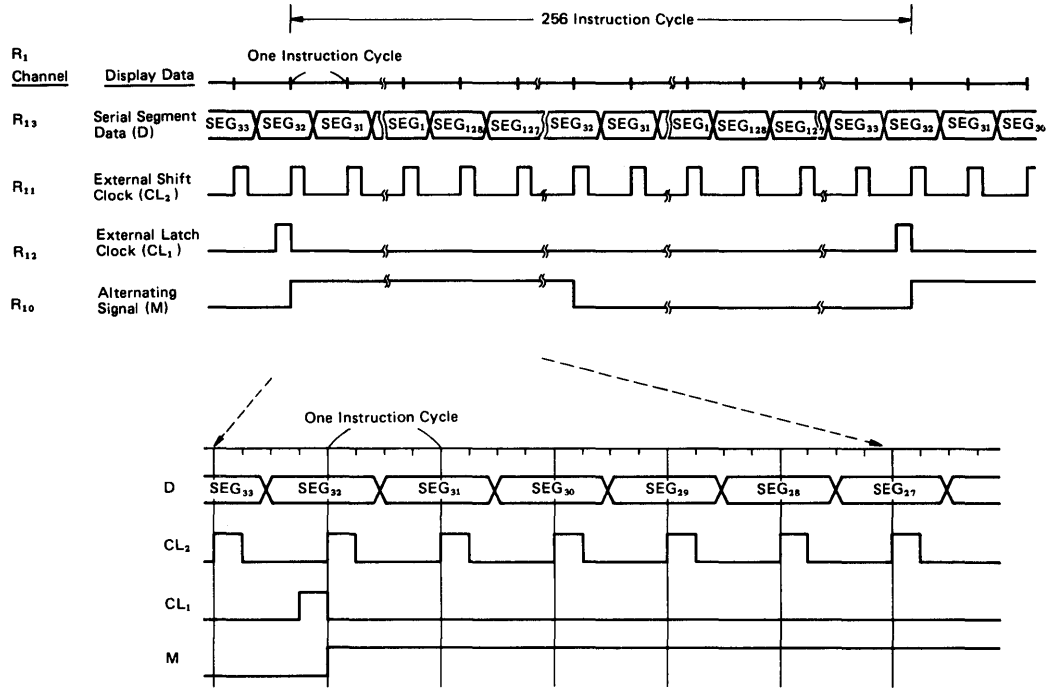


Figure 26 Display Data Timing Chart

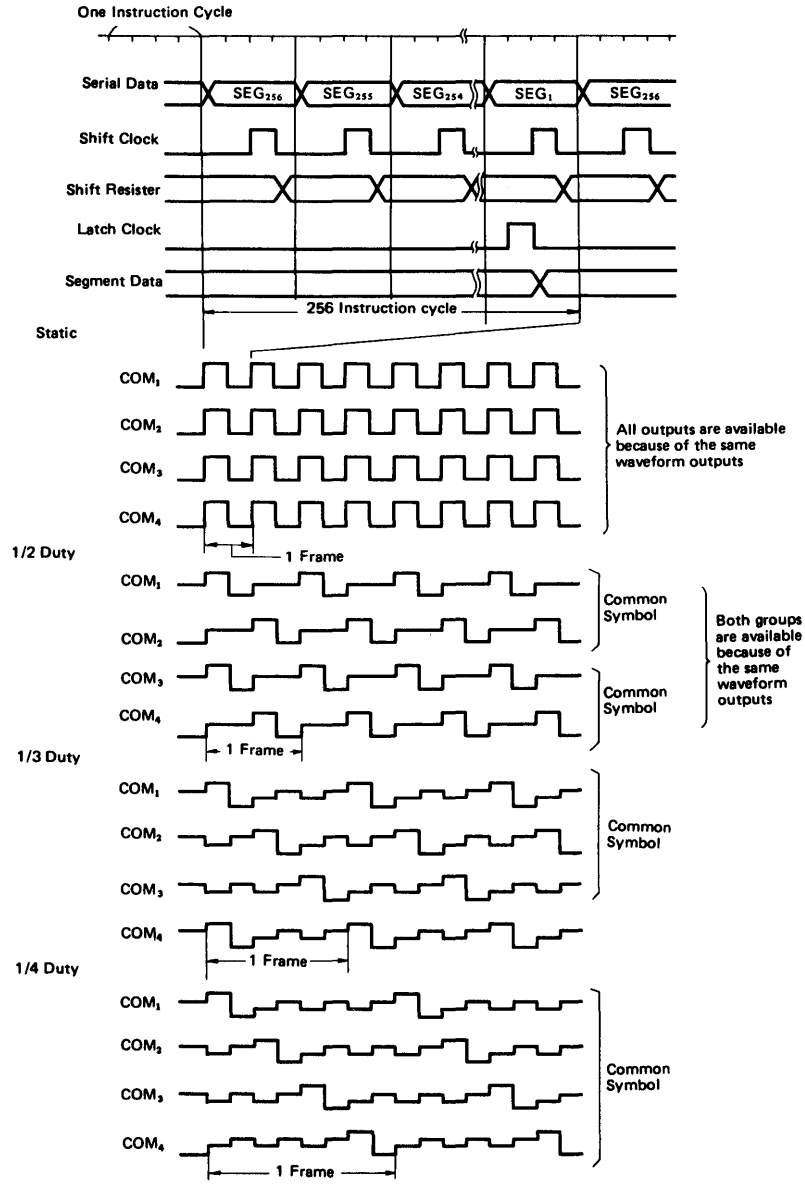


Figure 27 Liquid Crystal Display Circuit Timing Chart

- **Liquid Crystal Display Mode Setting Registers**
  For selection of the liquid crystal display mode, data I/O registers of R4, R5 and R6 are used.

Table 9 Function of Liquid Crystal Display Mode Setting Registers

	R_{41}	R_{40}	Function
Selection of liquid crystal display duty factor (R_{40}, R_{41})	0	0	Static
	0	1	1/2 duty
	1	0	1/3 duty
	1	1	1/4 duty

	R_{42}	Function
Designation of with or without liquid crystal segment output extension (R_{42})	0	To be extended (Outputs display data from Channel R1)
	1	Not to be extended (Channel R1 becomes an ordinary 4-bit data I/O.)

	R_{60}	Function
Liquid crystal display blanking signal (R_{60})	0	Outputs RAM data for liquid crystal display as segment signals.
	1	Segment signals become non-selection status (blanking) regardless of RAM data for liquid crystal display.

	R_{51}	R_{50}	Function
RAM designation for liquid crystal display (R_{50}, R_{51})	Function varies with liquid crystal display duty factor.		

	R_{63}	R_{62}	R_{61}	R_{60}	Function
Selection of halt function and oscillation circuit for timer		0	0		Do not set in this state.
		0	1		With crystal for timer, with internal halt, XI, XO
		1	0		Without crystal for timer, D_{14} and D_{15} are general I/O.
		1	1		With crystal for timer, without internal halt, XI, XO.
I/O state at halt	0				Enable:
	1				Disable:

(NOTE) Liquid crystal display mode at resetting.
Since all bits of registers R4, R5 and R6 are set to "1" by the reset function, display mode after resetting becomes as shown below:
Liquid crystal display duty factor: 1/4 duty (R_{40} = "1", R_{41} = "1")
Liquid crystal segment output extension: Not extended (R_{42} = "1")
Designation of liquid crystal display blanking: Display blanking (R_{60} = "1")
Designation of RAM for liquid crystal display: Varies correspond to each liquid crystal display duty factor. (R_{50} = "1", R_{51} = "1")
Designation of crystal for timer and internal halt: With crystal for timer, without internal halt (R_{61} = "1", R_{62} = "1").
I/O state at halt: I/O state at halt becomes disable (R_{63} = "1").

- **Relation between Display RAM and Segment Data**

In the LCD-IV, 4 types of display duty factor (static, 1/2 duty, 1/3 duty, and 1/4 duty) can be selected by programs, and correspondence between RAM bits and segment data changes according to these duty factors.

■ shows segment signal output from the LCD-IV.

RAM Address X				RAM Y	RAM 2^3	RAM 2^2	RAM 2^1	RAM 2^0
6	4	2	0	0				
				1				
				2				
				3				
				4				
				5				
				6				
				7				
				8	SEG_{36}	SEG_{35}	SEG_{34}	SEG_{33}
				9	SEG_{40}	SEG_{39}	SEG_{38}	SEG_{37}
				10	SEG_{44}	SEG_{43}	SEG_{42}	SEG_{41}
				11	SEG_{48}	SEG_{47}	SEG_{46}	SEG_{45}
				12	SEG_{52}	SEG_{51}	SEG_{50}	SEG_{49}
				13	SEG_{56}	SEG_{55}	SEG_{54}	SEG_{53}
				14	SEG_{60}	SEG_{59}	SEG_{58}	SEG_{57}
				15	SEG_{64}	SEG_{63}	SEG_{62}	SEG_{61}
7	5	3	1	0	SEG_{68}	SEG_{67}	SEG_{66}	SEG_{65}
				1	SEG_{72}	SEG_{71}	SEG_{70}	SEG_{69}
				2	SEG_{76}	SEG_{75}	SEG_{74}	SEG_{73}
				3	SEG_{80}	SEG_{79}	SEG_{78}	SEG_{77}
				4	SEG_{84}	SEG_{83}	SEG_{82}	SEG_{81}
				5	SEG_{88}	SEG_{87}	SEG_{86}	SEG_{85}
				6	SEG_{92}	SEG_{91}	SEG_{90}	SEG_{89}
				7	SEG_{96}	SEG_{95}	SEG_{94}	SEG_{93}
				8	SEG_{100}	SEG_{99}	SEG_{98}	SEG_{97}
				9	SEG_{104}	SEG_{103}	SEG_{102}	SEG_{101}
				10	SEG_{108}	SEG_{107}	SEG_{106}	SEG_{105}
				11	SEG_{112}	SEG_{111}	SEG_{110}	SEG_{109}
				12	SEG_{116}	SEG_{115}	SEG_{114}	SEG_{113}
				13	SEG_{120}	SEG_{119}	SEG_{118}	SEG_{117}
				14	SEG_{124}	SEG_{123}	SEG_{122}	SEG_{121}
				15	SEG_{128}	SEG_{127}	SEG_{126}	SEG_{125}
R_{S0}	0	1	0	1				
R_{S1}	0	0	1	1				

(NOTE) The SEG_{33} to SEG_{128} are extended segments.

Figure 28 Relation between RAM for LCD & Segment Data (Static)

RAM Address X				RAM Y	RAM 2^3	RAM 2^2	RAM 2^1	RAM 2^0	
6	4	2	0	0					COM_1
				1					COM_2
				2					COM_1
				3					COM_2
				4					COM_1
				5					COM_2
				6					COM_1
				7					COM_2
				8					COM_1
				9					COM_2
				10					COM_1
				11					COM_2
				12					COM_1
				13					COM_2
				14					COM_1
				15					COM_2
				0	SEG_{36}	SEG_{35}	SEG_{34}	SEG_{33}	COM_1
				1	SEG_{36}	SEG_{35}	SEG_{34}	SEG_{33}	COM_2
				2	SEG_{40}	SEG_{39}	SEG_{38}	SEG_{37}	COM_1
				3	SEG_{40}	SEG_{39}	SEG_{38}	SEG_{37}	COM_2
				4	SEG_{44}	SEG_{43}	SEG_{42}	SEG_{41}	COM_1
				5	SEG_{44}	SEG_{43}	SEG_{42}	SEG_{41}	COM_2
				6	SEG_{48}	SEG_{47}	SEG_{46}	SEG_{45}	COM_1
7	5	3	1	7	SEG_{48}	SEG_{47}	SEG_{46}	SEG_{45}	COM_2
				8	SEG_{52}	SEG_{51}	SEG_{50}	SEG_{49}	COM_1
				9	SEG_{52}	SEG_{51}	SEG_{50}	SEG_{49}	COM_2
				10	SEG_{56}	SEG_{55}	SEG_{54}	SEG_{53}	COM_1
				11	SEG_{56}	SEG_{55}	SEG_{54}	SEG_{53}	COM_2
				12	SEG_{60}	SEG_{59}	SEG_{58}	SEG_{57}	COM_1
				13	SEG_{60}	SEG_{59}	SEG_{58}	SEG_{57}	COM_2
				14	SEG_{64}	SEG_{63}	SEG_{62}	SEG_{61}	COM_1
				15	SEG_{64}	SEG_{63}	SEG_{62}	SEG_{61}	COM_2
				0	SEG_{68}	SEG_{67}	SEG_{66}	SEG_{65}	COM_1
				1	SEG_{68}	SEG_{67}	SEG_{66}	SEG_{65}	COM_2
				2	SEG_{72}	SEG_{71}	SEG_{70}	SEG_{69}	COM_1
				3	SEG_{72}	SEG_{71}	SEG_{70}	SEG_{69}	COM_2
				4	SEG_{76}	SEG_{75}	SEG_{74}	SEG_{73}	COM_1
				5	SEG_{76}	SEG_{75}	SEG_{74}	SEG_{73}	COM_2
				6	SEG_{80}	SEG_{79}	SEG_{78}	SEG_{77}	COM_1
4	6	0	2	7	SEG_{80}	SEG_{79}	SEG_{78}	SEG_{77}	COM_2
				8	SEG_{84}	SEG_{83}	SEG_{82}	SEG_{81}	COM_1
				9	SEG_{84}	SEG_{83}	SEG_{82}	SEG_{81}	COM_2
				10	SEG_{88}	SEG_{87}	SEG_{86}	SEG_{85}	COM_1
				11	SEG_{88}	SEG_{87}	SEG_{86}	SEG_{85}	COM_2
				12	SEG_{92}	SEG_{91}	SEG_{90}	SEG_{89}	COM_1
				13	SEG_{92}	SEG_{91}	SEG_{90}	SEG_{89}	COM_2
				14	SEG_{96}	SEG_{95}	SEG_{94}	SEG_{93}	COM_1
				15	SEG_{96}	SEG_{95}	SEG_{94}	SEG_{93}	COM_2
				0	SEG_{100}	SEG_{99}	SEG_{98}	SEG_{97}	COM_1
				1	SEG_{100}	SEG_{99}	SEG_{98}	SEG_{97}	COM_2
				2	SEG_{104}	SEG_{103}	SEG_{102}	SEG_{101}	COM_1
				3	SEG_{104}	SEG_{103}	SEG_{102}	SEG_{101}	COM_2
				4	SEG_{108}	SEG_{107}	SEG_{106}	SEG_{105}	COM_1
				5	SEG_{108}	SEG_{107}	SEG_{106}	SEG_{105}	COM_2
				6	SEG_{112}	SEG_{111}	SEG_{110}	SEG_{109}	COM_1
5	7	1	3	7	SEG_{112}	SEG_{111}	SEG_{110}	SEG_{109}	COM_2
				8	SEG_{116}	SEG_{115}	SEG_{114}	SEG_{113}	COM_1
				9	SEG_{116}	SEG_{115}	SEG_{114}	SEG_{113}	COM_2
				10	SEG_{120}	SEG_{119}	SEG_{118}	SEG_{117}	COM_1
				11	SEG_{120}	SEG_{119}	SEG_{118}	SEG_{117}	COM_2
				12	SEG_{124}	SEG_{123}	SEG_{122}	SEG_{121}	COM_1
				13	SEG_{124}	SEG_{123}	SEG_{122}	SEG_{121}	COM_2
				14	SEG_{128}	SEG_{127}	SEG_{126}	SEG_{125}	COM_1
				15	SEG_{128}	SEG_{127}	SEG_{126}	SEG_{125}	COM_2
R_{S0}	0	1	0	1					
R_{S1}	0	0	1	1					

Figure 29 Relation between RAM for LCD & Segment Data (1/2 Duty, 1/2 Bias)

RAM Address X				Y	RAM 2^3	2^2	2^1	2^0
6	4	2	0	0				
				1				
				2				
				3				
				4				
				5				
				6				
				7				
				8				
				9				
				10				
				11				
				12				
				13				
				14				
				15				
7	5	3	1	0				
				1				
				2				
				3				
				4				
				5				
				6				
				7				
				8				
				9				
				10				
				11				
				12				
				13				
				14				
				15				
4	6	0	2	0		SEG_{33}	SEG_{33}	SEG_{33}
				1		SEG_{34}	SEG_{34}	SEG_{34}
				2		SEG_{35}	SEG_{35}	SEG_{35}
				3		SEG_{36}	SEG_{36}	SEG_{36}
				4		SEG_{37}	SEG_{37}	SEG_{37}
				5		SEG_{38}	SEG_{38}	SEG_{38}
				6		SEG_{39}	SEG_{39}	SEG_{39}
				7		SEG_{40}	SEG_{40}	SEG_{40}
				8		SEG_{41}	SEG_{41}	SEG_{41}
				9		SEG_{42}	SEG_{42}	SEG_{42}
				10		SEG_{43}	SEG_{43}	SEG_{43}
				11		SEG_{44}	SEG_{44}	SEG_{44}
				12		SEG_{45}	SEG_{45}	SEG_{45}
				13		SEG_{46}	SEG_{46}	SEG_{46}
				14		SEG_{47}	SEG_{47}	SEG_{47}
				15		SEG_{48}	SEG_{48}	SEG_{48}
5	7	1	3	0		SEG_{49}	SEG_{49}	SEG_{49}
				1		SEG_{50}	SEG_{50}	SEG_{50}
				2		SEG_{51}	SEG_{51}	SEG_{51}
				3		SEG_{52}	SEG_{52}	SEG_{52}
				4		SEG_{53}	SEG_{53}	SEG_{53}
				5		SEG_{54}	SEG_{54}	SEG_{54}
				6		SEG_{55}	SEG_{55}	SEG_{55}
				7		SEG_{56}	SEG_{56}	SEG_{56}
				8		SEG_{57}	SEG_{57}	SEG_{57}
				9		SEG_{58}	SEG_{58}	SEG_{58}
				10		SEG_{59}	SEG_{59}	SEG_{59}
				11		SEG_{60}	SEG_{60}	SEG_{60}
				12		SEG_{61}	SEG_{61}	SEG_{61}
				13		SEG_{62}	SEG_{62}	SEG_{62}
				14		SEG_{63}	SEG_{63}	SEG_{63}
				15		SEG_{64}	SEG_{64}	SEG_{64}
R_{S0}	0	1	0	1				
R_{S1}	0	0	1	1		COM_3	COM_2	COM_1

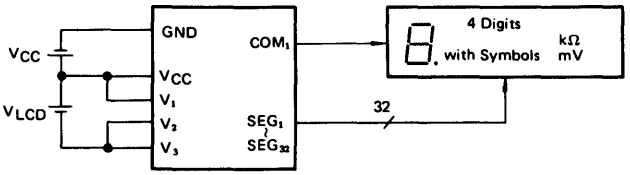
RAM Address X				Y	RAM 2^3	2^2	2^1	2^0
2	0	6	4	0		SEG_{65}	SEG_{65}	SEG_{65}
				1		SEG_{66}	SEG_{66}	SEG_{66}
				2		SEG_{67}	SEG_{67}	SEG_{67}
				3		SEG_{68}	SEG_{68}	SEG_{68}
				4		SEG_{69}	SEG_{69}	SEG_{69}
				5		SEG_{70}	SEG_{70}	SEG_{70}
				6		SEG_{71}	SEG_{71}	SEG_{71}
				7		SEG_{72}	SEG_{72}	SEG_{72}
				8		SEG_{73}	SEG_{73}	SEG_{73}
				9		SEG_{74}	SEG_{74}	SEG_{74}
				10		SEG_{75}	SEG_{75}	SEG_{75}
				11		SEG_{76}	SEG_{76}	SEG_{76}
				12		SEG_{77}	SEG_{77}	SEG_{77}
				13		SEG_{78}	SEG_{78}	SEG_{78}
				14		SEG_{79}	SEG_{79}	SEG_{79}
				15		SEG_{80}	SEG_{80}	SEG_{80}
3	1	7	5	0		SEG_{81}	SEG_{81}	SEG_{81}
				1		SEG_{82}	SEG_{82}	SEG_{82}
				2		SEG_{83}	SEG_{83}	SEG_{83}
				3		SEG_{84}	SEG_{84}	SEG_{84}
				4		SEG_{85}	SEG_{85}	SEG_{85}
				5		SEG_{86}	SEG_{86}	SEG_{86}
				6		SEG_{87}	SEG_{87}	SEG_{87}
				7		SEG_{88}	SEG_{88}	SEG_{88}
				8		SEG_{89}	SEG_{89}	SEG_{89}
				9		SEG_{90}	SEG_{90}	SEG_{90}
				10		SEG_{91}	SEG_{91}	SEG_{91}
				11		SEG_{92}	SEG_{92}	SEG_{92}
				12		SEG_{93}	SEG_{93}	SEG_{93}
				13		SEG_{94}	SEG_{94}	SEG_{94}
				14		SEG_{95}	SEG_{95}	SEG_{95}
				15		SEG_{96}	SEG_{96}	SEG_{96}
0	2	4	6	0		SEG_{97}	SEG_{97}	SEG_{97}
				1		SEG_{98}	SEG_{98}	SEG_{98}
				2		SEG_{99}	SEG_{99}	SEG_{99}
				3		SEG_{100}	SEG_{100}	SEG_{100}
				4		SEG_{101}	SEG_{101}	SEG_{101}
				5		SEG_{102}	SEG_{102}	SEG_{102}
				6		SEG_{103}	SEG_{103}	SEG_{103}
				7		SEG_{104}	SEG_{104}	SEG_{104}
				8		SEG_{105}	SEG_{105}	SEG_{105}
				9		SEG_{106}	SEG_{106}	SEG_{106}
				10		SEG_{107}	SEG_{107}	SEG_{107}
				11		SEG_{108}	SEG_{108}	SEG_{108}
				12		SEG_{109}	SEG_{109}	SEG_{109}
				13		SEG_{110}	SEG_{110}	SEG_{110}
				14		SEG_{111}	SEG_{111}	SEG_{111}
				15		SEG_{112}	SEG_{112}	SEG_{112}
1	3	5	7	0		SEG_{113}	SEG_{113}	SEG_{113}
				1		SEG_{114}	SEG_{114}	SEG_{114}
				2		SEG_{115}	SEG_{115}	SEG_{115}
				3		SEG_{116}	SEG_{116}	SEG_{116}
				4		SEG_{117}	SEG_{117}	SEG_{117}
				5		SEG_{118}	SEG_{118}	SEG_{118}
				6		SEG_{119}	SEG_{119}	SEG_{119}
				7		SEG_{120}	SEG_{120}	SEG_{120}
				8		SEG_{121}	SEG_{121}	SEG_{121}
				9		SEG_{122}	SEG_{122}	SEG_{122}
				10		SEG_{123}	SEG_{123}	SEG_{123}
				11		SEG_{124}	SEG_{124}	SEG_{124}
				12		SEG_{125}	SEG_{125}	SEG_{125}
				13		SEG_{126}	SEG_{126}	SEG_{126}
				14		SEG_{127}	SEG_{127}	SEG_{127}
				15		SEG_{128}	SEG_{128}	SEG_{128}
R_{S0}	0	1	0	1				
R_{S1}	0	0	1	1		COM_3	COM_2	COM_1

Figure 30 Relation between RAM for LCD & Segment Data (1/3 Duty, 1/3 Bias)

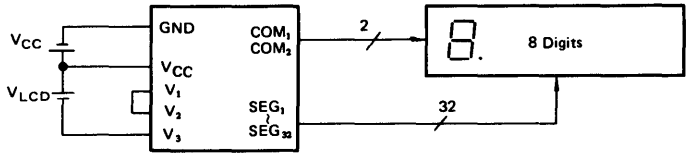
RAM Address X				Y	RAM 2^3	2^2	2^1	2^0
6	4	2	0	0				
				1				
				2				
				3				
				4				
				5				
				6				
				7				
				8				
				9				
				10				
				11				
				12				
				13				
				14				
				15				
7	5	3	1	0				
				1				
				2				
				3				
				4				
				5				
				6				
				7				
				8				
				9				
				10				
				11				
				12				
				13				
				14				
				15				
4	6	0	2	0	SEG_{33}	SEG_{33}	SEG_{33}	SEG_{33}
				1	SEG_{34}	SEG_{34}	SEG_{34}	SEG_{34}
				2	SEG_{35}	SEG_{35}	SEG_{35}	SEG_{35}
				3	SEG_{36}	SEG_{36}	SEG_{36}	SEG_{36}
				4	SEG_{37}	SEG_{37}	SEG_{37}	SEG_{37}
				5	SEG_{38}	SEG_{38}	SEG_{38}	SEG_{38}
				6	SEG_{39}	SEG_{39}	SEG_{39}	SEG_{39}
				7	SEG_{40}	SEG_{40}	SEG_{40}	SEG_{40}
				8	SEG_{41}	SEG_{41}	SEG_{41}	SEG_{41}
				9	SEG_{42}	SEG_{42}	SEG_{42}	SEG_{42}
				10	SEG_{43}	SEG_{43}	SEG_{43}	SEG_{43}
				11	SEG_{44}	SEG_{44}	SEG_{44}	SEG_{44}
				12	SEG_{45}	SEG_{45}	SEG_{45}	SEG_{45}
				13	SEG_{46}	SEG_{46}	SEG_{46}	SEG_{46}
				14	SEG_{47}	SEG_{47}	SEG_{47}	SEG_{47}
				15	SEG_{48}	SEG_{48}	SEG_{48}	SEG_{48}
5	7	1	3	0	SEG_{49}	SEG_{49}	SEG_{49}	SEG_{49}
				1	SEG_{50}	SEG_{50}	SEG_{50}	SEG_{50}
				2	SEG_{51}	SEG_{51}	SEG_{51}	SEG_{51}
				3	SEG_{52}	SEG_{52}	SEG_{52}	SEG_{52}
				4	SEG_{53}	SEG_{53}	SEG_{53}	SEG_{53}
				5	SEG_{54}	SEG_{54}	SEG_{54}	SEG_{54}
				6	SEG_{55}	SEG_{55}	SEG_{55}	SEG_{55}
				7	SEG_{56}	SEG_{56}	SEG_{56}	SEG_{56}
				8	SEG_{57}	SEG_{57}	SEG_{57}	SEG_{57}
				9	SEG_{58}	SEG_{58}	SEG_{58}	SEG_{58}
				10	SEG_{59}	SEG_{59}	SEG_{59}	SEG_{59}
				11	SEG_{60}	SEG_{60}	SEG_{60}	SEG_{60}
				12	SEG_{61}	SEG_{61}	SEG_{61}	SEG_{61}
				13	SEG_{62}	SEG_{62}	SEG_{62}	SEG_{62}
				14	SEG_{63}	SEG_{63}	SEG_{63}	SEG_{63}
				15	SEG_{64}	SEG_{64}	SEG_{64}	SEG_{64}
R_{S0}	0	1	0	1				
R_{S1}	0	0	1	1	COM_4	COM_3	COM_2	COM_1

RAM Address X				Y	RAM 2^3	2^2	2^1	2^0
2	0	6	4	0	SEG_{65}	SEG_{65}	SEG_{65}	SEG_{65}
				1	SEG_{66}	SEG_{66}	SEG_{66}	SEG_{66}
				2	SEG_{67}	SEG_{67}	SEG_{67}	SEG_{67}
				3	SEG_{68}	SEG_{68}	SEG_{68}	SEG_{68}
				4	SEG_{69}	SEG_{69}	SEG_{69}	SEG_{69}
				5	SEG_{70}	SEG_{70}	SEG_{70}	SEG_{70}
				6	SEG_{71}	SEG_{71}	SEG_{71}	SEG_{71}
				7	SEG_{72}	SEG_{72}	SEG_{72}	SEG_{72}
				8	SEG_{73}	SEG_{73}	SEG_{73}	SEG_{73}
				9	SEG_{74}	SEG_{74}	SEG_{74}	SEG_{74}
				10	SEG_{75}	SEG_{75}	SEG_{75}	SEG_{75}
				11	SEG_{76}	SEG_{76}	SEG_{76}	SEG_{76}
				12	SEG_{77}	SEG_{77}	SEG_{77}	SEG_{77}
				13	SEG_{78}	SEG_{78}	SEG_{78}	SEG_{78}
				14	SEG_{79}	SEG_{79}	SEG_{79}	SEG_{79}
				15	SEG_{80}	SEG_{80}	SEG_{80}	SEG_{80}
3	1	7	5	0	SEG_{81}	SEG_{81}	SEG_{81}	SEG_{81}
				1	SEG_{82}	SEG_{82}	SEG_{82}	SEG_{82}
				2	SEG_{83}	SEG_{83}	SEG_{83}	SEG_{83}
				3	SEG_{84}	SEG_{84}	SEG_{84}	SEG_{84}
				4	SEG_{85}	SEG_{85}	SEG_{85}	SEG_{85}
				5	SEG_{86}	SEG_{86}	SEG_{86}	SEG_{86}
				6	SEG_{87}	SEG_{87}	SEG_{87}	SEG_{87}
				7	SEG_{88}	SEG_{88}	SEG_{88}	SEG_{88}
				8	SEG_{89}	SEG_{89}	SEG_{89}	SEG_{89}
				9	SEG_{90}	SEG_{90}	SEG_{90}	SEG_{90}
				10	SEG_{91}	SEG_{91}	SEG_{91}	SEG_{91}
				11	SEG_{92}	SEG_{92}	SEG_{92}	SEG_{92}
				12	SEG_{93}	SEG_{93}	SEG_{93}	SEG_{93}
				13	SEG_{94}	SEG_{94}	SEG_{94}	SEG_{94}
				14	SEG_{95}	SEG_{95}	SEG_{95}	SEG_{95}
				15	SEG_{96}	SEG_{96}	SEG_{96}	SEG_{96}
0	2	4	6	0	SEG_{97}	SEG_{97}	SEG_{97}	SEG_{97}
				1	SEG_{98}	SEG_{98}	SEG_{98}	SEG_{98}
				2	SEG_{99}	SEG_{99}	SEG_{99}	SEG_{99}
				3	SEG_{100}	SEG_{100}	SEG_{100}	SEG_{100}
				4	SEG_{101}	SEG_{101}	SEG_{101}	SEG_{101}
				5	SEG_{102}	SEG_{102}	SEG_{102}	SEG_{102}
				6	SEG_{103}	SEG_{103}	SEG_{103}	SEG_{103}
				7	SEG_{104}	SEG_{104}	SEG_{104}	SEG_{104}
				8	SEG_{105}	SEG_{105}	SEG_{105}	SEG_{105}
				9	SEG_{106}	SEG_{106}	SEG_{106}	SEG_{106}
				10	SEG_{107}	SEG_{107}	SEG_{107}	SEG_{107}
				11	SEG_{108}	SEG_{108}	SEG_{108}	SEG_{108}
				12	SEG_{109}	SEG_{109}	SEG_{109}	SEG_{109}
				13	SEG_{110}	SEG_{110}	SEG_{110}	SEG_{110}
				14	SEG_{111}	SEG_{111}	SEG_{111}	SEG_{111}
				15	SEG_{112}	SEG_{112}	SEG_{112}	SEG_{112}
1	3	5	7	0	SEG_{113}	SEG_{113}	SEG_{113}	SEG_{113}
				1	SEG_{114}	SEG_{114}	SEG_{114}	SEG_{114}
				2	SEG_{115}	SEG_{115}	SEG_{115}	SEG_{115}
				3	SEG_{116}	SEG_{116}	SEG_{116}	SEG_{116}
				4	SEG_{117}	SEG_{117}	SEG_{117}	SEG_{117}
				5	SEG_{118}	SEG_{118}	SEG_{118}	SEG_{118}
				6	SEG_{119}	SEG_{119}	SEG_{119}	SEG_{119}
				7	SEG_{120}	SEG_{120}	SEG_{120}	SEG_{120}
				8	SEG_{121}	SEG_{121}	SEG_{121}	SEG_{121}
				9	SEG_{122}	SEG_{122}	SEG_{122}	SEG_{122}
				10	SEG_{123}	SEG_{123}	SEG_{123}	SEG_{123}
				11	SEG_{124}	SEG_{124}	SEG_{124}	SEG_{124}
				12	SEG_{125}	SEG_{125}	SEG_{125}	SEG_{125}
				13	SEG_{126}	SEG_{126}	SEG_{126}	SEG_{126}
				14	SEG_{127}	SEG_{127}	SEG_{127}	SEG_{127}
				15	SEG_{128}	SEG_{128}	SEG_{128}	SEG_{128}
R_{S0}	0	1	0	1				
R_{S1}	0	0	1	1	COM_4	COM_3	COM_2	COM_1

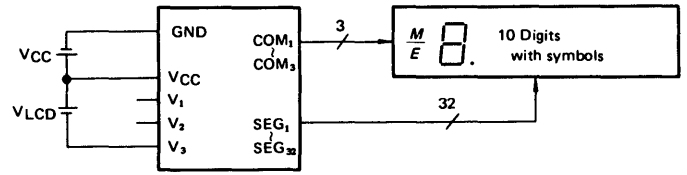
Figure 31 Relation between RAM for LCD & Segment Data (1/4 Duty, 1/3 Bias)



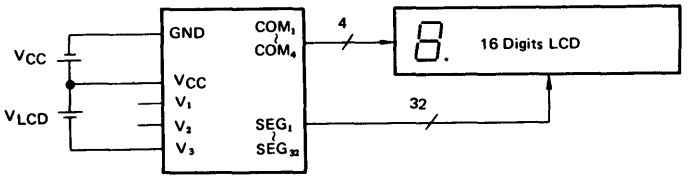
(Static)



(1/2 duty, 1/2 bias)



(1/3 duty, 1/3 bias)



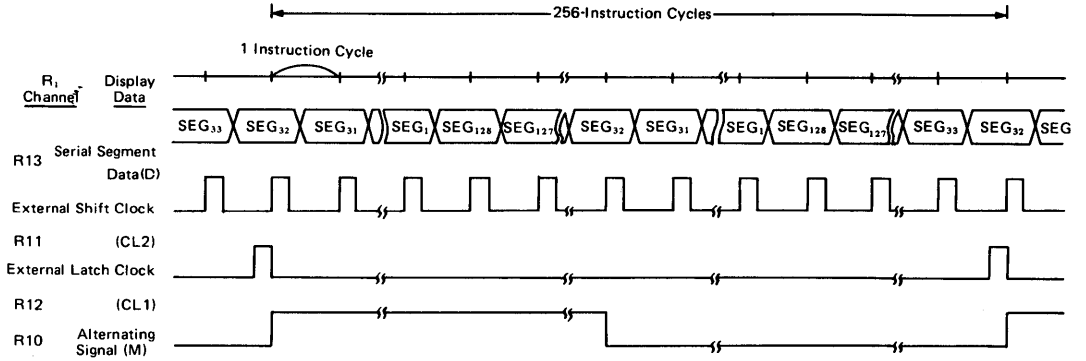
(1/4 duty, 1/3 bias)

Figure 32 LCD Wiring Samples

- **Extension of Display Function**

Number of display digits can be increased by externally connecting an LCD driver LSI HD44100H to the LCD-IV.

The HD44100H consists of shift registers and latch and liquid crystal drive circuit. When connected with the LCD-IV, the HD44100H is used as a circuit for segment. In the LCD-IV, display data for 128 segments is sent to the 32-bit shift register from RAM constantly. When R_{42} is set to "0", the R1 channel outputs the 32nd stage output D of the shift register, shift clock CL_2, latch clock CL_1 and AC signal M. Therefore, up to 96 segment terminals from SEG_{33} to SEG_{128} can be added by directly connecting the HD44100H.



■ RESET FUNCTION

The reset is performed by setting the RESET pin to "1" ("High" level) and the LCD-IV gets into operation by setting it to "0" ("Low" level).

Internal state of the LCD-IV are specified as follows by the reset function.

- Program Counter (PC) is set to Bank 1 63 Page 3F Address.
- IR/I, IR/T, I/E and CF are reset to "0".
- IF0, IF1 and TF are set to "1".
- Data I/O Registers and Discrete I/O Latches (R1, R2, R3, D_0 to D_{15}) are all set to "1".
- Bank Register R_{70} is set to "1" (Jumps to Bank 0 by execution of LPU instruction after the reset).
- Liquid Crystal Display ..... all bits of display mode setting register (Data I/O Register) R4, R5, R6 are set to "1".

(Note) All the other logic blocks (the Stack Registers, the Status F/F, the accumulator, the Carry F/F, the registers, the Timer/Counter, RAM) are not cleared by the reset function.

■ HALT FUNCTION

The LCD-IV is provided with halt function. The halt function reduces power consumption in the halt state by temporarily stopping all status including RAM. When halt is released, operation restarts from the state before the halt.

HALT state is kept 16-instruction after receiving halt releasing signal. (Internal, External)

The user can select one of the following I/O status at the time of halt based on the "MASK OPTION LIST" when ordering ROM:

i) All I/O status is kept as the state immediately before the halt.

ii) All I/O status is held in the high impedance state (both PMOS and NMOS are off, and pull-up MOS is off).

There are the following two types of halt:

1) External Halt (Halt state generated by using $\overline{HLT}$ terminal)

All operations stop when the $\overline{HLT}$ terminal is set to the "0" level (Low). When the $\overline{HLT}$ terminal is set to the "1" level (High), operation restarts from the state immediately before the halt.

2) Internal Halt (Halt state generated by programs)

The user can select availability of internal halt at the time of ROM order based on the "MASK OPTION LIST". When internal halt is selected, timer crystal must be attached externally. Therefore, the D_{14}/XO and D_{15}/XI terminals should not be used as general I/O's, but as XO and XI terminals for connecting crystal oscillator.

Resetting of the D_{15} latch by RED instruction generates internal halt state. Return from internal halt is effected by overflow signals of the prescaler. 16Hz overflow signals are output from the prescaler if a crystal oscillator of 32.768kHz is connected to the D_{14}/XO and D_{15}/XI terminals. When an overflow signal is issued, the D_{15} latch is set to "1" from "0", the LCD-IV returns from halt state, adds 1 to the timer register, and execution restarts from the instruction next to the RED instruction.

Note that external halt caused by the $\overline{HLT}$ terminal cannot be released by prescaler overflow signals.

(Caution at the halt time)

When the LCD-IV goes into halt state, segment terminals (SEG_1 to SEG_{32}) and common terminals (COM_1 to COM_4) become the same potential and display goes out. However, in order to reduce power consumption during halt, disconnect the voltage applied to liquid crystal power supply V_3. Since there are dividing resistors among V_1, V_2, and V_3, current of up to 50μA flows if voltage is applied between V_{CC} and V_3 in the same way as normal operation.

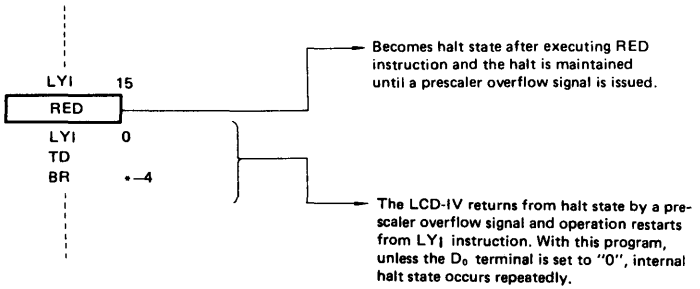


Figure 33 Program example in the Internal Halt Mode

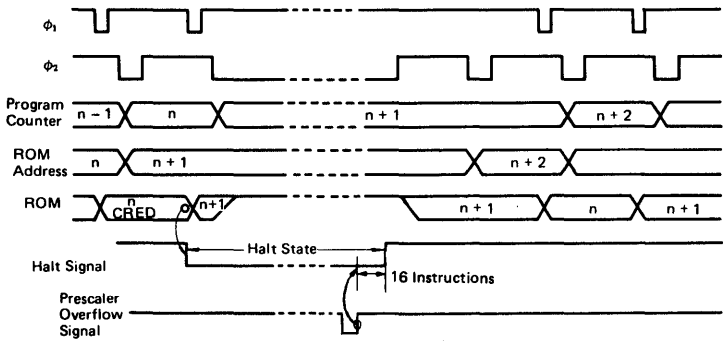
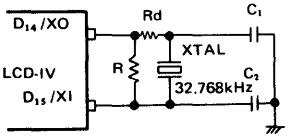


Figure 34 Internal Halt Timing Chart

■ CRYSTAL OSCILLATION CIRCUIT FOR TIMER

The user can specify by the "MASK OPTION LIST" whether or not the timer crystal should be externally attached. By externally attaching a crystal oscillator of 32.768kHz to the D_{14}/XO and D_{15}/XI terminals, maximum 1 second of timer interruption cycle is possible setting the prescaler clock to 1,024Hz.



(NOTE)
The crystal oscillator, resistor R, Rd and load capacitor C_1 and C_2 should be placed as close as possible to the LCD-IV. Induction of external noise to D_{14}/XO and D_{15}/XI may disturb normal oscillation.
This circuit is the example of the typical use. As the oscillation characteristics is not guaranteed, please consider and examine the circuit constants carefully on your application.

Figure 35 Crystal Oscillator Circuit

No.	Halt state	With or without timer crystal	D_{14}, D_{15} (XO, XI) terminals	Function
1	External halt	Externally attached crystal (32.768 kHz)	Terminals for attaching crystal. Cannot be used as general I/O.	Prescaler clock is set to 1,024 Hz and the overflow signal to 16 Hz. Up to 1 second can be set as the timer interruption cycle.
2	External halt	(Without crystal) Internal clock of LSI	Used as general I/O	The prescaler clock becomes 100 kHz type, and the timer interruption cycle can be set to maximum 97.66 Hz.
3	Internal and external halt	Externally attached crystal (32.768 kHz)	Terminals for attaching crystal. Cannot be used as general I/O.	Prescaler clock is set to 1,024 Hz and the overflow signal to 16 Hz. This signal performs the LCD-IV return from internal halt. (Return from external halt is not possible by the prescaler overflow signal.)

■ MASK OPTION

The following type mask option is available.

- **I/O Terminal Format . . . . . Select one of A, B or C.**
  A: Without pull-up MOS
  B: With pull-up MOS
  C: CMOS output

(Note) External input is not permitted if CMOS output is selected in the case of I/O common terminals.

- **I/O Status in the Halt State. . . . Select Enable or Disable.**

Enable
- Output . . . . Maintained in the status before halt.
- Pull-up MOS . . . ON
- Input . . . Unrelated to halt state

(Since Pull-up MOS is ON, if halt state occurs when output is "0" (Low) level (NMOS; ON), pull-up MOS current always flows. If input changes, transient current flows through the input circuit. Also, current flows through the input pull-up MOS. These currents are added to standby power supply current (or halt current).)

Disable
- Output . . . NMOS output; OFF
  CMOS output; High impedance (NMOS, PMOS; OFF)
- Pull-up MOS . . . OFF
- Input . . . Input circuit; OFF

(Both input and output become high impedance state. Since the input circuit is turned off, input change does not cause current other than the standby power supply current or halt current.)

- **With or without externally attached Timer Crystal**

Without timer crystal . . .

The D_{14} and D_{15} can be used as general I/O terminals. Select one of A, B or C in the D_{14}/D_{15} column of the I/O format specifications.

With timer crystal . . .

The D_{14} and D_{15} cannot be used as general I/O terminals.
Therefore, leave the D_{14}/D_{15} column in blank.
Since the D_{14} latch can be set, reset or tested, it can be used as a flag.
If no internal halt exists, the D_{15} latch can be used as a flag same as the D_{14} latch. If internal halt exists, it cannot be used as a general flag.

- **With or without Internal Halt**

With internal halt . . .

When internal halt is specified, the timer crystal must also be specified.

Without internal halt . . .

The D_{15} can be used as a general I/O terminal (when no timer crystal is used) or as a flag (when timer crystal is used).

- **OSCILLATION CIRCUIT**

The user can specify a resistor, or a ceramic filter or an external oscillator.

LSI Type Number	HD	(To be filled by Hitachi)
Customer's ROM Code Name		
Customer		

■ MASK OPTION LIST

(1) I/O Option

Pin Name	I/O	I/O Option			Remarks
		A	B	C	
D_0	I/O				
D_1	I/O				
D_2	I/O				
D_3	I/O				
D_4	I/O				
D_5	I/O				
D_6	I/O				
D_7	I/O				
D_8	I/O				
D_9	I/O				
D_{10}	I/O				
D_{11}	I/O				
D_{12}	I/O				
D_{13}	I/O				
D_{14}	I/O				
D_{15}	I/O				
R_{00}	I				
R_{01}	I				
R_{02}	I				
R_{03}	I				
R_{10}	I/O				
R_{11}	I/O				
R_{12}	I/O				
R_{13}	I/O				
R_{20}	I/O				
R_{21}	I/O				
R_{22}	I/O				
R_{23}	I/O				
R_{30}	O				
R_{31}	O				
R_{32}	O				
R_{33}	O				
INT_0	I				
INT_1	I				

(NOTE) Mark a selected composition with a circle (o).
A. No Pull up MOS
B. With Pull up MOS
C. CMOS Output

(2) I/O State at "Halt" State and Others

I/O State	□ Enable	□ Disable	
With or without externally attached crystal for timer	□ With	□ Without	With ..... D_{14} and D_{15} become XO, XI. Do not write anything the I/O Option space (A, B, C) of D_{14}, D_{15}.
With or without internal halt	□ With	□ Without	Internal halt is specified only when crystal for timer is specified.
Power-supply voltage	□ 5 ± 0.5V	□ 2.5 to 5.5V	
Oscillation circuit (system clock)	□ R_f Oscillation □ Ceramic filter □ External clock		Ceramic filter is specified only when power supply is V_{CC} = 5 ± 0.5V.
Halt function	□ Not use □ Use (Return by Reset) □ Use (Return by no Reset)		

(NOTE) Mark a selected I/O State or another with a check mark (√).

■ INSTRUCTION

Instructions are listed according to their functions.
Each mnemonic code and function are shown in this table.

Group	Mnemonic code	Function	Status
Register to Register	LAB	B → A	
	LBA	A → B	
	LAY	Y → A	
	LASPX	SPX → A	
	LASPY	SPY → A	
	XAMR m	A ↔ MR (m)	
RAM Address	LXA	A → X	
	LYA	A → Y	
	LXI i	i → X	
	LYI i	i → Y	
	IY	Y + 1 → Y	NZ
	DY	Y − 1 → Y	NB
	AYY	Y + A → Y	C
	SYY	Y − A → Y	NB
	XSPX	X ↔ SPX	
	XSPY	Y ↔ SPY	
	XSPXY	X ↔ SPX, Y ↔ SPY	
Register RAM	LAM (XY)	M → A (XY ↔ SPXY)	
	LBM (XY)	M → B (XY ↔ SPXY)	
	XMA (XY)	M ↔ A (XY ↔ SPXY)	
	XMB (XY)	M ↔ B (XY ↔ SPXY)	
	LMAIY (X)	A → M, Y + 1 → Y (X ↔ SPX)	NZ
	LMADY (X)	A → M, Y − 1 → Y (X ↔ SPX)	NB
Immediate	LMIIY i	i → M, Y + 1 → Y	NZ
	LAI i	i → A	
	LBI i	i → B	
Arithmetic	AI i	A + i → A	C
	IB	B + 1 → B	NZ
	DB	B − 1 → B	NB
	AMC	M + A + C (F/F) → A	C
	SMC	M − A − $\overline{C}$ (F/F) → A	NB
	AM	M + A → A	C
	DAA	Decimal Adjustment (Addition)	
	DAS	Decimal Adjustment (Subtruction)	
	NEGA	$\overline{A}$ + 1 → A	
	COMB	$\overline{B}$ → B	
	SEC	1 → C (F / F)	
	REC	0 → C (F / F)	
	TC	Test C (F / F)	C (F / F)
	ROTL	Rotation Left	
	ROTR	Rotation Right	
	OR	A ∪ B → A	

(to be continued)

Group	Mnemonic code	Function	Status
Compare	MNEI i	M ≠ i	NZ
	YNEI i	Y ≠ i	NZ
	ANEM	A ≠ M	NZ
	BNEM	B ≠ M	NZ
	ALEI i	A ≦ i	NB
	ALEM	A ≦ M	NB
	BLEM	B ≦ M	NB
RAM bit Manipulation	SEM n	1 → M (n)	
	REM n	0 → M (n)	
	TM n	Test M (n)	M (n)
ROM Address	BR a	Branch on Status 1	1
	CAL a	Subroutine Jump on Status 1	1
	LPU u	Load Program Counter Upper on Status 1	
	TBR p	Table Branch	
	RTN	Return from Subroutine	
Interrupt	SEIE	1 → I/E	
	SEIF0	1 → IF0	
	SEIF1	1 → IF1	
	SETF	1 → TF	
	SECF	1 → CF	
	REIE	0 → I/E	
	REIF0	0 → IF0	
	REIF1	0 → IF1	
	RETF	0 → TF	
	RECF	0 → CF	
	TI0	Test INT_0	INT_0
	TI1	Test INT_1	INT_1
	TIF0	Test IF_0	IF_0
	TIF1	Test IF_1	IF_1
	TTF	Test TF	TF
	LTI i	i → Timer/Counter	
	LTA	A → Timer/Counter	
	LAT	Timer/Counter → A	
	RTNI	Return Interrupt	
Input/Output (Display Control)	SED	1 → D (Y)	
	RED	0 → D (Y)	
	TD	Test D (Y)	D (Y)
	SEDD n	1 → D (n)	
	REDD n	0 → D (n)	
	LAR p	R (p) → A	
	LBR p	R (p) → B	
	LRA p	A → R (p)	
	LRB p	B → R (p)	
	Pp	Pattern Generation	
	NOP	No Operation	

(NOTE) 1. (XY) after a mnemonic code has four meanings as follows.

Mnemonic only	Instruction execution only
Mnemonic with X	Instruction execution, X ↔ SPX
Mnemonic with Y	Instruction execution, Y ↔ SPY
Mnemonic with XY	Instruction execution, X ↔ SPX, Y ↔ SPY

[Example]

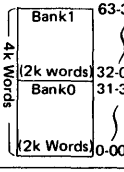
LAM	M → A
LAMX	M → A, X ↔ SPX
LAMY	M → A, Y ↔ SPY
LAMXY	M → A, X ↔ SPX, Y ↔ SPY

2. Status column shows the factor which affects status by the instruction of status change.
   NZ ..... ALU Not Zeto
   C ..... ALU Overflow in Addition/Carry
   NB ..... ALU Overflow in Subtraction/No Borrow
   except above .... Content of status column affects status directly.
3. Carry flip-flop is not always affected by executing the instruction which affects the Status.
   Instructions which affect Carry flip-flop are eight as follows.

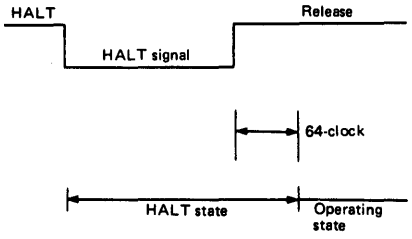
AMC	SEC
SMC	REC
DAA	ROTL
DAS	ROTR

4. All instructions except for P are executed in single cycle.
   P is executed in 2 cycles.

The Difference between LCD-III and LCD-IV

No.	Difference	LCD-III	LCD-IV
1	ROM	(Program Memory) 2,048 words (Pattern Memory) 128 words	(Program Memory) 4,096 words (Includes Pattern Memory)
2	RAM	160 digits	256 digits
3	Cycle Time (V_{CC} = 5V±10%)	10μs/cycle (f_{cp} = 400 kHz)	5μs/cycle (f_{cp} = 800 kHz)
4	Stored Reset Circuit (Power-on Reset)	Yes	No
5	Select Option	Selected by Mask Option List (Note) But when program evaluation with HD44797E, set up the option with the register as LCD-IV.	When ordering ROM, selected by Mask Option List or by program using internal register R6. (Mask Option List + Program)
	Crystal for Timer		R_{61} = 0 (No crystal for timer) R_{61} = 1 (With crystal for timer)
	Internal Halt		R_{62} = 0 (With internal halt) R_{62} = 1 (No internal halt)
	I/O Condition at "Halt" state		R_{63} = 0 (Enable) R_{63} = 1 (Disable)
6	Oscillator	Refer to the manual as for circuit constant of resistor oscillation and ceramic oscillation.	Circuit constants of resistor oscillation and ceramic oscillation are undecided. (As for low voltage operation board (V_{CC} = 2.5 to 5.5V), undecided that seramic filter can be used or not.)
7	Reset Address	31–3F	63–3F (Bank 1)
8	Bank Register (ROM Addressing)	No Bank Register	ROM is divided in 2 Banks.  When call or branch to other Bank, execute CALL or BRL after changing Bank Register (R7). R_7 = 0 (Bank 1 side) R_7 = 1 (Bank 0 side)
9	Absolute Maximum Rating V_{T2} for Terminal Voltage of Open Drain Configuration Output Pins and I/O Common Pins	–0.3 to +10.0V	–0.3 to V_{CC} + 0.3V (same as VT_1)

(to be continued)

<table>
<tr><th>No.</th><th>Difference</th><th>LCD-III</th><th>LCD-IV</th></tr>
<tr><td>10</td><td>Input "High" level Voltage V_{IHZ} of Open Drain Configuration Output Pins and I/O Common Pins.</td><td><table><tr><th>min.</th><th>typ.</th><th>max.</th></tr><tr><td>V_{CC}-1.0</td><td>–</td><td>10</td></tr></table></td><td><table><tr><th>min.</th><th>typ.</th><th>max.</th></tr><tr><td>V_{CC}-1.0</td><td>–</td><td>V_{CC}</td></tr></table></td></tr>
<tr><td>11</td><td>RAM Contents Destruction at Reset</td><td>With RAM destruction</td><td>No RAM destruction</td></tr>
<tr><td>12</td><td>HALT</td><td>Executes immediately after releasing HALT.</td><td>HALT state is released when system clock keeps it 64-clock after receiving halt release.
  </td></tr>
<tr><td>13</td><td>Maximum Total Output Current (1) $\cdot\Sigma I_{O1}$</td><td>45 mA</td><td>25 mA</td></tr>
<tr><td rowspan="2">14</td><td rowspan="2">Reset Pulse Width (1) t_{RST1}</td><td>V_{CC} = 5 ± 0.5V
R_f Oscillation 1 ms
External Clock Operation 4 ms</td><td>V_{CC} = 5 ± 0.5V
R_f Oscillation 10 ms
External Clock Operation 40 ms</td></tr>
<tr><td>V_{CC} = 2.5 to 5.5V
1 ms</td><td>V_{CC} = 2.5 to 5.5V
10 ms</td></tr>
</table>

4-BIT SINGLE-CHIP MICROCOMPUTER HMCS400 SERIES

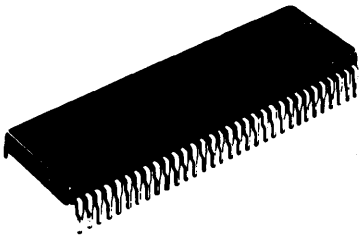
HMCS404C (HD614042)

The HMCS404C is a CMOS 4-bit single-chip microcomputer which is a member of the HMCS400 series.

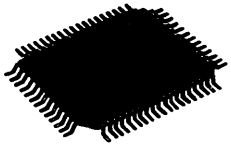
The HMCS404C has efficient and powerful architecture and its software is very similar to the HMCS40 series.

This microcomputer provides variety of on-chip resources such as ROM, RAM, I/O, two timer/counters and a serial interface to perform in wide users' applications.

The HMCS404C also has the characteristics of high speed and low power dissipation and which I/O pins are able to drive fluorescent display tube directly.



(DP-64S)



(FP-64)

■ HARDWARE FEATURES

- 4-bit Architecture
- 4,096 Words x 10-bit ROM
- 256 Digits x 4-bit RAM
- 58 I/O Pins, Including 26 High Voltage I/O Pins (40V Max)
- Two Timer/Counters
  - 11-bit Prescaler
  - 8-bit Free Running Timer
  - 8-bit Auto-Reload Timer/Event Counter
- Clock Synchronous 8-bit Serial Interface
- Five Interrupts

External	2
Timer/Counter	2
Serial Interface	1

- Subroutine Stack
  - Up to 16 Levels Including Interrupt
- Minimum Instruction Execution Time – 2 μs
- Two Low Power Dissipation Modes
  - Standby – Stops instruction execution while keeping clock oscillation and interrupt functions in operation
  - Stop – Stops instruction execution and clock oscillation while retaining RAM data
- On-Chip Oscillator
  - External Connection of Crystal, Ceramic Filter or Resistor (externally drivable)

■ SOFTWARE FEATURES

- Instruction Set Similar to and More Powerful than HMCS40 Series; 99 Instructions
- High Programming Efficiency with 10-bit ROM/Word; 79 instructions are single-word instructions
- Direct Branch to All ROM Area
- Direct or Indirect Addressing to All RAM Area
- Subroutine Nesting Up to 16 Levels Including Interrupts
- Binary and BCD Arithmetic Operation
- Powerful Logical Arithmetic Operation
- Pattern Generation – Table Look Up Capability –
- Bit Manipulation for Both RAM and I/O

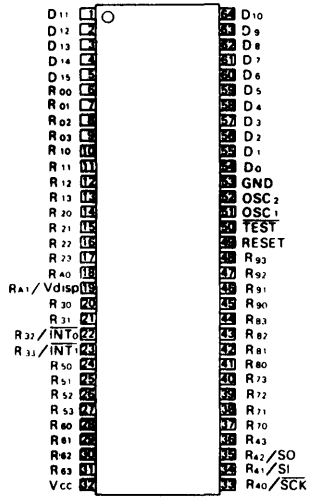
■ VERSATILE PROGRAM DEVELOPMENT SUPPORT TOOLS

- H68SD Series Macro Assembler
- H68SD5-use Emulator (With Real Time Trace Function)
- EPROM On Package Microcomputer

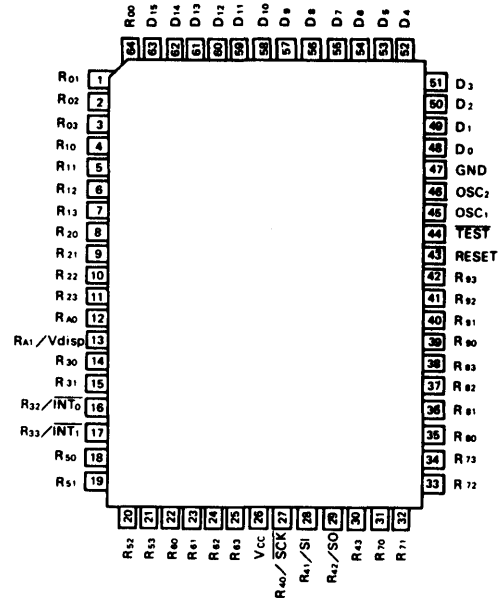
Mask options are fixed as follows:

- I/O pin : Open Drain
- Oscillator : Crystal Oscillator or Ceramic Filter Oscillator (externally drivable)
- Divider : Divide-by-8

■ PIN ARRANGEMENT

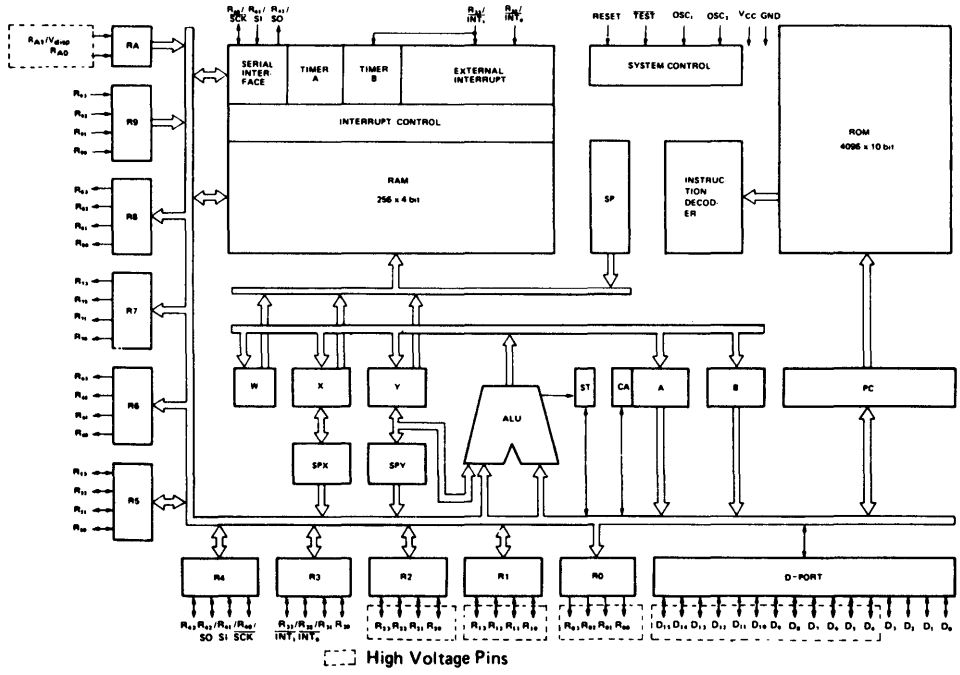


(Top View)



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	−0.3 to +7.0	V	
Terminal Voltage	V_T	−0.3 to V_{CC} +0.3	V	3
		V_{CC} −45 to V_{CC} +0.3	V	4
Total Allowance of Input Currents	ΣI_O	50	mA	5
Total Allowance of Output Currents	$-\Sigma I_O$	150	mA	6
Maximum Input Current	I_O	15	mA	7, 8
Maximum Output Current	$-I_O$	4	mA	9, 10
		6	mA	9, 11
		30	mA	9, 12
Operating Temperature	T_{opr}	−20 to +75	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

(Note 1) Permanent damage may occur if "Absolute Maximum Ratings" are exceeded. Normal operation should be under the conditions of "Electrical Characteristics". If these conditions are exceeded, it may cause the malfunction and affect the reliability of LSI.
(Note 2) All voltages are with respect to GND.
(Note 3) Applied to standard pins.
(Note 4) Applied to high voltage pins.
(Note 5) Total allowance of input current is the total sum of input current which flow in from all I/O pins to GND simultaneously.
(Note 6) Total allowance of output current is the total sum of the output current which flow out from V_{CC} to all I/O pins simultaneously.
(Note 7) Maximum input current is the maximum amount of input current from each I/O pin to GND.
(Note 8) Applied to $D_0 \sim D_3$ and R3 ~ R8.
(Note 9) Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
(Note 10) Applied to $D_0 \sim D_3$ and R3 ~ R8.
(Note 11) Applied to R0 ~ R2.
(Note 12) Applied to $D_4 \sim D_{15}$.

■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS (V_{CC} = 4V to 6V, GND = 0V, V_{disp} = V_{CC} −40V to V_{CC}, Ta = −20 to +75°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions		Value min	Value typ	Value max	Unit	Note
Input "High" Voltage	V_{IH}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$			0.7V_{CC}	–	V_{CC}+0.3	V	
		SI			0.7V_{CC}	–	V_{CC}+0.3	V	
		OSC_1			V_{CC}− 0.5	–	V_{CC}+0.3	V	
Input "Low" Voltage	V_{IL}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$			−0.3	–	0.22V_{CC}	V	
		SI			−0.3	–	0.22V_{CC}	V	
		OSC_1			−0.3	–	0.5	V	
Output "High" Voltage	V_{OH}	$\overline{SCK}$, SO	$-I_{OH}$ = 1.0 mA		V_{CC}−1.0	–	–	V	
			$-I_{OH}$ = 0.01 mA		V_{CC}−0.3	–	–	V	
Output "Low" Voltage	V_{OL}	$\overline{SCK}$, SO	I_{OL} = 1.6 mA		–	–	0.4	V	
Input/Output Leakage Current	$\|I_{IL}\|$	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$, SI, SO, OSC_1	V_{in} = 0V to V_{CC}		–	–	1	μA	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}	V_{CC}=5V	Crystal or Ceramic Filter Oscillator Option f_{osc} = 4MHz	–	–	2.0	mA	2, 6
				Resistor Oscillator Option f_{osc} = 4MHz	–	–	2.4	mA	2, 6
Current Dissipation in Standby Mode	I_{SBY1}	V_{CC}	Maximum Logic Operation V_{CC} = 5V	Crystal or Ceramic Filter Oscillator Option f_{osc} = 4MHz	–	–	1.2	mA	3, 6
				Resistor Oscillator Option f_{osc} = 4MHz	–	–	1.6	mA	3, 6
	I_{SBY2}	V_{CC}	Minimum Logic Operation V_{CC} = 5V	Crystal or Ceramic Filter Oscillator Option f_{osc} =4MHz	–	–	0.9	mA	4, 6
				Resistor Oscillator Option f_{osc} = 4MHz	–	–	1.3	mA	4, 6
Current Dissipation in Stop Mode	I_{stop}	V_{CC}	$V_{in}(\overline{TEST})$ = V_{CC}-0.3V to V_{CC} V_{in}(RESET) = 0V to 0.3V		–	–	10	μA	5
Stop Mode Retain Voltage	V_{stop}	V_{CC}			2	–	–	V	

(Note 1) Pull-up MOS current and output buffer current are excluded.
(Note 2) The MCU is in the reset state. The input/output current does not flow.
Test Conditions: MCU state; • Reset state in Operation Mode
Pin state; • RESET, $\overline{TEST}$ ... V_{CC} voltage
• $D_0 \sim D_3$, R3 ~ R9 ... V_{CC} voltage
• $D_4 \sim D_{15}$, R0 ~ R2, R_{A0}, R_{A1} ... V_{disp} voltage
(Note 3) The timer/counter operate with the fastest clock and input/output current does not flow.
Test Conditions: MCU state; • Standby Mode
• Input/Output; Reset state
• TIMER-A; ÷2 prescaler divide ratio
• TIMER-B; ÷2 prescaler divide ratio
• SERIAL Interface ; Stop
Pin state; • RESET ... GND voltage
• $\overline{TEST}$ ... V_{CC} voltage
• $D_0 \sim D_3$, R3 ~ R9 ... V_{CC} voltage
• $D_4 \sim D_{15}$, R0 ~ R2, R_{A0}, R_{A1} ... V_{disp} voltage
(Note 4) The timer/counter operate with the slowest clock and input/output current does not flow.
Test Conditions: MCU state; • Standby Mode
• Input/Output; Reset state
• TIMER-A; ÷2048 prescaler divide ratio
• TIMER-B; ÷2048 prescaler divide ratio
• SERIAL Interface ; Stop
Pin state; • RESET... GND voltage
• $\overline{TEST}$ ... V_{CC} voltage
• $D_0 \sim D_3$, R3 ~ R9 ... V_{CC} voltage
• $D_4 \sim D_{15}$, R0 ~ R2, R_{A0}, R_{A1} ... V_{disp} voltage
(Note 5) Pull-down MOS current is excluded.
(Note 6) When $f_{osc}=x$ [MHz], the Current Dissipation in Operation mode and Standby mode are estimated as follows:

$$\text{max. value } (f_{osc}=x\text{[MHz]}) = \frac{x}{4} \times \text{max. value } (f_{osc}=4\text{[MHz]})$$

• INPUT/OUTPUT CHARACTERISTICS FOR STANDARD PIN

(V_{CC} = 4V to 6V, GND = 0V, V_{disp} = V_{CC} −40V to V_{CC}, Ta = −20 to +75°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	$D_0 \sim D_3$, R3 ~ R5, R9		0.7V_{CC}	–	V_{CC}+0.3	V	
Input "Low" Voltage	V_{IL}	$D_0 \sim D_3$, R3 ~ R5, R9		−0.3	–	0.22V_{CC}	V	
Output "High" Voltage	V_{OH}	$D_0 \sim D_3$, R3 ~ R8	$-I_{OH}$ = 1.0 mA	V_{CC}−1.0	–	–	V	1
		$D_0 \sim D_3$, R3 ~ R8	$-I_{OH}$ = 0.01 mA	V_{CC}−0.3	–	–	V	1
Output "Low" Voltage	V_{OL}	$D_0 \sim D_3$, R3 ~ R8	I_{OL} = 1.6 mA	–	–	0.4	V	
Input/Output Leakage Current	$\|I_{IL}\|$	$D_0 \sim D_3$, R3 ~ R9	V_{in} = 0V to V_{CC}	–	–	1	μA	2
Pull-Up MOS Current	$-I_p$	$D_0 \sim D_3$, R3 ~ R9	V_{CC} = 5V, V_{in} = 0V	30	60	120	μA	3

(Note 1) Applied to I/O pins with "CMOS" Output selected by mask option.
(Note 2) Pull-up MOS current and output buffer current are excluded.
(Note 3) Applied to I/O pins with "with Pull-up MOS" selected by mask option.

- **INPUT/OUTPUT CHARACTERISTICS FOR HIGH VOLTAGE PIN**
  (V_{CC} = 4V to 6V, GND = 0V, V_{disp} = V_{CC} −40V to V_{CC}, Ta = −20 to +75°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	$D_4 \sim D_{15}$, R1 R2, R_{A0}, R_{A1}		0.7V_{CC}	–	V_{CC}+0.3	V	
Input "Low" Voltage	V_{IL}	$D_4 \sim D_{15}$, R1 R2, R_{A0}, R_{A1}		V_{CC}−40	–	0.22V_{CC}	V	
Output "High" Voltage	V_{OH}	$D_4 \sim D_{15}$	$-I_{OH}$=15mA, V_{CC}=5V±10%	V_{CC}−3.0	–	–	V	
			$-I_{OH}$=9 mA	V_{CC}−2.0	–	–	V	
		R0 ~ R2	$-I_{OH}$=3 mA, V_{CC}=5V±10%	V_{CC}−3.0	–	–	V	
			$-I_{OH}$=1.8 mA	V_{CC}−2.0	–	–	V	
Output "Low" Voltage	V_{OL}	$D_4 \sim D_{15}$ R0~R2	V_{disp} = V_{CC}−40V	–	–	V_{CC}−37	V	1
		$D_4 \sim D_{15}$ R0~R2	150kΩ to V_{CC}−40V	–	–	V_{CC}−37	V	2
Input/Output Leakage Current	$\|I_{IL}\|$	$D_4 \sim D_{15}$ R0~R2 R_{A0}, R_{A1}	V_{in} = V_{CC}−40V to V_{CC}	–	–	20	μA	3
Pull Down MOS Current	I_d	$D_4 \sim D_{15}$ R0~R2 R_{A0}, R_{A1}	V_{disp} = V_{CC}−35V V_{in} = V_{CC}	125	250	500	μA	4

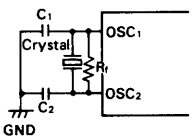
(Note 1) Applied to I/O pins with "with Pull-down MOS" selected by mask option.
(Note 2) Applied to I/O pins with "without Pull-down MOS (PMOS Open Drain)" selected by mask option.
(Note 3) Pull-down MOS current and output buffer current are excluded.
(Note 4) Applied to I/O pins with "with Pull-down MOS" selected by mask option.

● **AC CHARACTERISTICS (V_{CC} = 4V to 6V, GND = 0V, V_{disp} = V_{CC} −40V to V_{CC}, Ta = −20 to +75°C, if not specified.)**

	Item	Symbol	Pin Name	Test Conditions	Value min	Value typ	Value max	Unit	Note
Crystal or Ceramic Filter Oscillator	Oscillation Frequency	f_{osc}	OSC_1, OSC_2		0.4	4	4.5	MHz	
	Instruction Cycle Time	t_{cyc}			1.78	2	20	μs	
	Oscillator Stabilization Time	t_{RC}	OSC_1, OSC_2		–	–	20	ms	1
Resistor Oscillator	Oscillation Frequency	f_{osc}	OSC_1, OSC_2	R_f=20kΩ±2%	1.8	3.0	4.2	MHz	
	Instruction Cycle Time	t_{cyc}		R_f=20kΩ±2%	1.9	2.66	4.44	μs	
	Oscillator Stabilization Time	t_{RC}	OSC_1, OSC_2	R_f=20kΩ±2%	–	–	0.5	ms	1
External Clock	External Clock Frequency	f_{CP}	OSC_1		0.4	–	4.5	MHz	2
	External Clock "High" Level Width	t_{CPH}	OSC_1		100	–	–	ns	2
	External Clock "Low" Level Width	t_{CPL}	OSC_1		100	–	–	ns	2
	External Clock Rise Time	t_{CPr}	OSC_1		–	–	20	ns	2
	External Clock Fall Time	t_{CPf}	OSC_1		–	–	20	ns	2
	Instruction Cycle Time	t_{cyc}			1.78	–	20	μs	2
$\overline{INT_0}$ "High" Level Width		t_{I0H}	$\overline{INT_0}$		2	–	–	t_{cyc}	3
$\overline{INT_0}$ "Low" Level Width		t_{I0L}	$\overline{INT_0}$		2	–	–	t_{cyc}	3
$\overline{INT_1}$ "High" Level Width		t_{I1H}	$\overline{INT_1}$		2	–	–	t_{cyc}	3
$\overline{INT_1}$ "Low" Level Width		t_{I1L}	$\overline{INT_1}$		2	–	–	t_{cyc}	3
RESET "High" Level Width		t_{RSTH}	RESET		2	–	–	t_{cyc}	4
Input Capacitance		C_{in}	all pins	f=1MHz V_{in} = 0V	–	–	15	pF	
RESET Fall Time		t_{RSTf}			–	–	20	ms	4

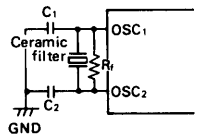
(Note 1) Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 4.0V at "Power-on", or after RESET input level goes to "High" by resetting to quit the stop mode by MCU reset on the circuits below. When using crystal or ceramic filter oscillator, please ask a crystal oscillator maker's or ceramic filter maker's advice because oscillator stabilization time depends on the circuit constant and stray capacity.

Crystal oscillator



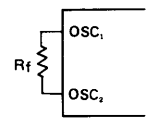
Crystal: 4.194304MHz NC-18C(Nihon Denpa Kogyo)
Rf : 1MΩ ±2%
C_1 : 22pF±20%
C_2 : 22pF±20%

Ceramic filter oscillator



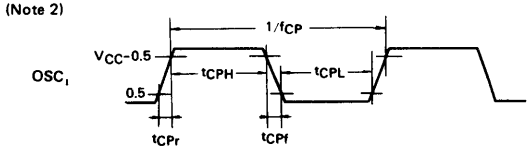
Ceramic filter: CSA4.00MG (Murata)
Rf : 1MHz±2%
C_1 : 30pF±20%
C_2 : 30pF±20%

Resistor oscillator

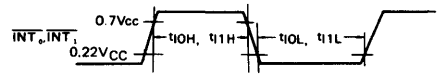


Rf : 20kΩ±2%

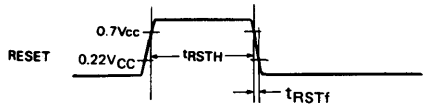
(Note 2)



(Note 3)



(Note 4)



- **SERIAL INTERFACE TIMING CHARACTERISTICS**
  (V_{CC} =4V to 6V, GND = 0V, V_{disp} = V_{CC} −40V to V_{CC}, Ta = −20 to +75°C, if not specified.)

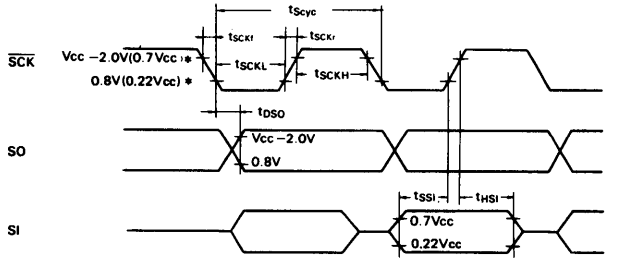
• At Transfer Clock Output

Item	Symbol	Pin Name	Test Conditions	Value min	Value typ	Value max	Unit	Note
Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$	(Note 2)	1	–	–	t_{cyc}	1, 2
Transfer Clock "High" Level Width	t_{SCKH}	$\overline{SCK}$	(Note 2)	0.5	–	–	t_{Scyc}	1, 2
Transfer Clock "Low" Level Width	t_{SCKL}	$\overline{SCK}$	(Note 2)	0.5	–	–	t_{Scyc}	1, 2
Transfer Clock Rise Time	t_{SCKr}	$\overline{SCK}$	(Note 2)	–	–	100	ns	1, 2
Transfer Clock Fall Time	t_{SCKf}	$\overline{SCK}$	(Note 2)	–	–	100	ns	1, 2
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	–	–	300	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		500	–	–	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		150	–	–	ns	1

• At Transfer Clock Input

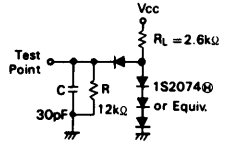
Item	Symbol	Pin Name	Test Conditions	Value min	Value typ	Value max	Unit	Note
Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$		1	–	–	t_{cyc}	1
Transfer Clock "High" Level Width	t_{SCKH}	$\overline{SCK}$		0.5	–	–	t_{Scyc}	1
Transfer Clock "Low" Level Width	t_{SCKL}	$\overline{SCK}$		0.5	–	–	t_{Scyc}	1
Transfer Clock Rise Time	t_{SCKr}	$\overline{SCK}$		–	–	100	ns	1
Transfer Clock Fall Time	t_{SCKf}	$\overline{SCK}$		–	–	100	ns	1
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	–	–	300	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		500	–	–	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		150	–	–	ns	1

(Note 1) Timing Diagram of Serial Interface

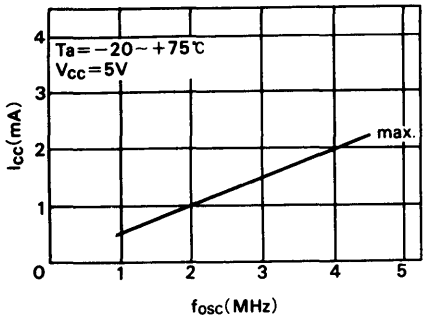


* V_{CC} − 2.0V and 0.8V are the threshold voltage for transfer clock output.
0.7 V_{CC} and 0.22 V_{CC} are the threshold voltage for transfer clock input.

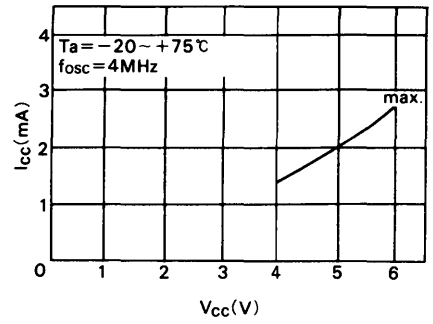
(Note 2) Timing Load Circuit



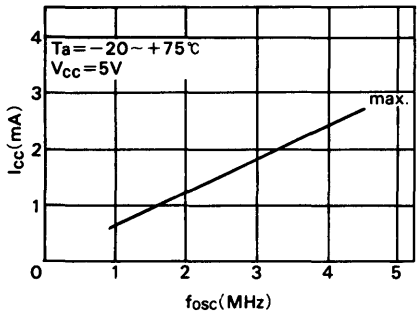
■ CHARACTERISTICS CURVE (REFERENCE DATA)



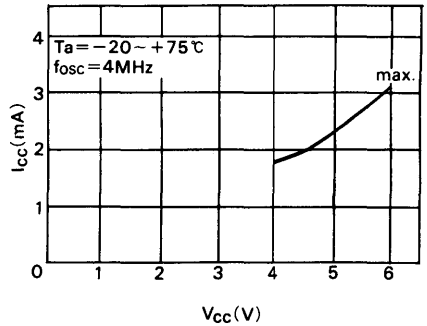
I_{CC} vs. f_{osc} Characteristics
(Crystal, Ceramic Filter Oscillator Option)



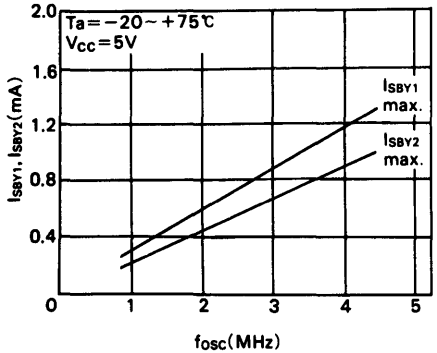
I_{CC} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator Option)



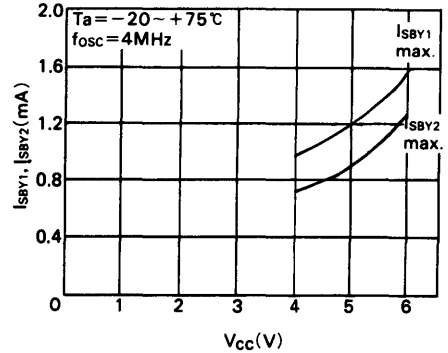
I_{CC} vs. f_{osc} Characteristics
(Resistor Oscillator Option)



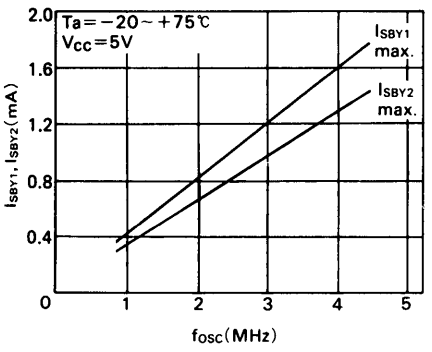
I_{CC} vs. V_{CC} Characteristics
(Resistor Oscillator Option)



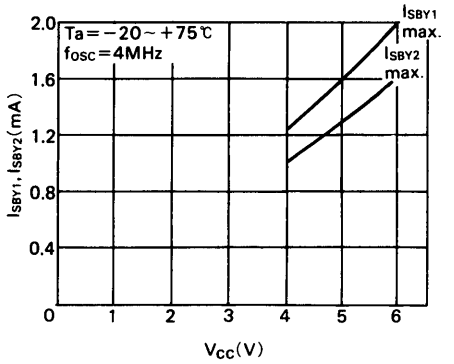
I_{SBY} vs. f_{osc} Characteristics
(Crystal, Ceramic Filter Oscillator Option)



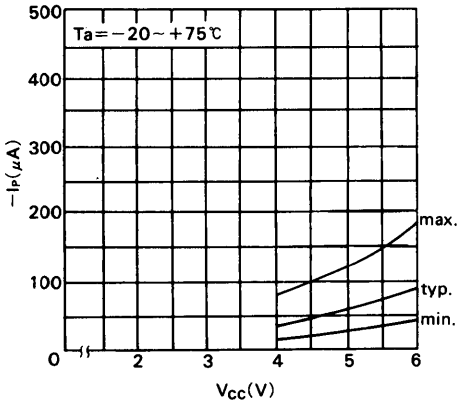
I_{SBY} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator Option)



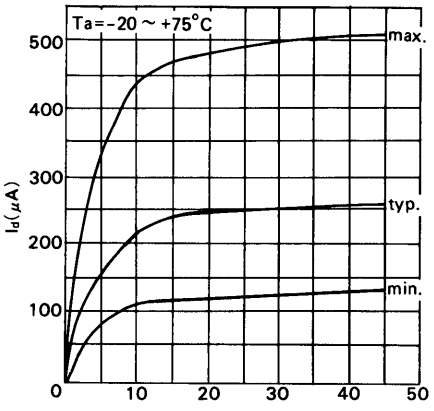
I_{SBY} vs. f_{osc} Characteristics
(Resistor Oscillator Option)



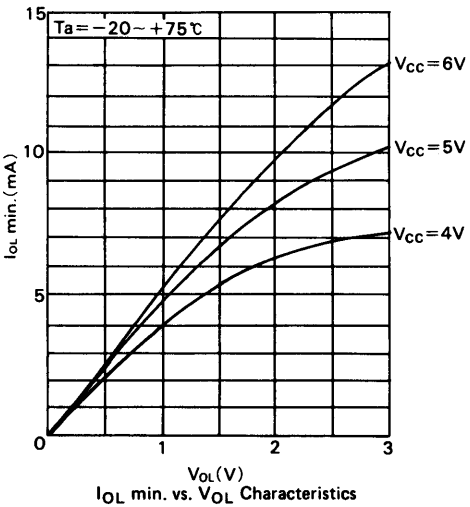
I_{SBY} vs. V_{CC} Characteristics
(Resistor Oscillator Option)



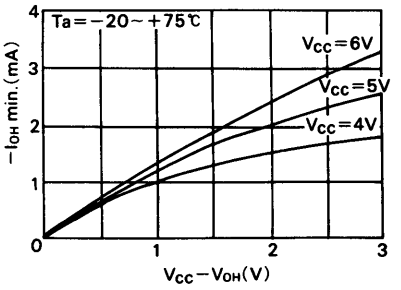
$-I_P$ (Pull-up MOS Current) vs.
V_{CC} Characteristics



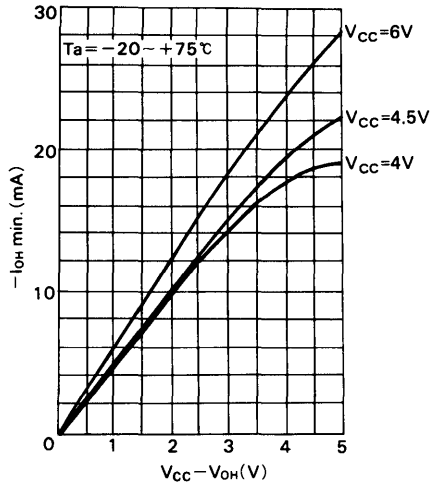
I_d (Pull-down MOS Current) vs.
(V_{CC} − V_{disp}) Characteristics



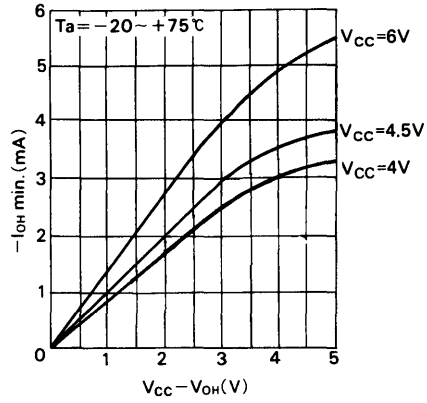
I_{OL} min. vs. V_{OL} Characteristics
(Standard Pin)



$-I_{OH}$ min vs. (V_{CC} − V_{OH}) Characteristics
(Standard Pin "CMOS")



$-I_{OH}$ min. vs. (V_{CC} − V_{OH}) Characteristics ($D_4 \sim D_{15}$ Pins)



$-I_{OH}$ min. vs. (V_{CC} − V_{OH}) Characteristics (RO ~ R2 Pins)

■ DESCRIPTION OF PIN FUNCTIONS

Input and output signals of MCU are described below.

• GND, V_{CC}, V_{disp}

These are Power Supply Pins. Connect GND pin to Earth (0V) and apply V_{CC} power supply voltage to V_{CC} pin. V_{disp} is an power supply for high voltage Input/Output pins with maximum voltage of V_{CC}-40V. V_{disp} pin can be also used as R_{A1} pin by mask option. For details, see "INPUT/OUTPUT".

• $\overline{TEST}$

$\overline{TEST}$ pin is not for user's application. $\overline{TEST}$ must be connected to V_{CC}.

• RESET

RESET pin is used to reset MCU. For details, see "RESET".

• OSC_1, OSC_2

These are Input pins to the internal oscillator circuit. They can be connected to crystal resonator, ceramic filter resonator, R_f oscillator, or external oscillator circuit. Select the circuit of MCU by mask option corresponding to the oscillator type. For details, see "INTERNAL OSCILLATOR CIRCUIT."

• D-port (D_0 to D_{15})

D-port is a 1-bit Input/Output common port. D_0 to D_3 are standard type, D_4 to D_{15} are for high voltage. Each pin has the mask option to select its circuit type. For details, See "INPUT/OUTPUT".

• R-port (R0 to RA)

R-port is a 4-bit Input/Output port. (only RA is 2-bit construction.) R0 and R6 to R8 are output ports, R9 to RA are input ports, and R1 to R5 are Input/Output common ports. R0 to R2 and RA are the high voltage ports, R3 to R9 are the standard ports. Each pin has the mask option to select its circuit type. R_{32}, R_{33}, R_{40}, R_{41} and R_{42} are also available as $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK}$, SI and SO respectively. For details, see "INPUT/OUTPUT".

• $\overline{INT_0}$, $\overline{INT_1}$

These are the input pins to interrupt MCU operation externally. $\overline{INT_1}$ can be used as an external event input pin for TIMER-B. $\overline{INT_0}$ and $\overline{INT_1}$ are also available as R_{32}, and R_{33} respectively. For details, See "INTERRUPT".

• $\overline{SCK}$, SI, SO

These are Transfer clock I/O pin ($\overline{SCK}$), serial data input pin (SI) and serial data output pin (SO) used for serial interface. $\overline{SCK}$, SI, and SO are also available as R_{40}, R_{41} and R_{42} respectively. For details, see "SERIAL INTERFACE".

■ ROM MEMORY MAP

MCU includes 4096 words × 10 bits ROM. ROM memory map is illustrated in Fig. 1 and described in the following paragraph.

• Vector Address Area ..... $0000 to $000F

When MCU is reset or an interrupt is serviced, the program is executed from the vector address. Program the JMPL instructions branching to the starting addresses of reset routine or of interrupt routines.

• Zero-Page Subroutine Area ..... $0000 to $003F

CAL instruction allows to branch to the subroutines in $0000 to $003F.

• Pattern Area ..... $0000 to $0FFF

P instruction allows referring to the ROM data in $0000 to $0FFF as a pattern.

• Program Area ..... $0000 to $0FFF

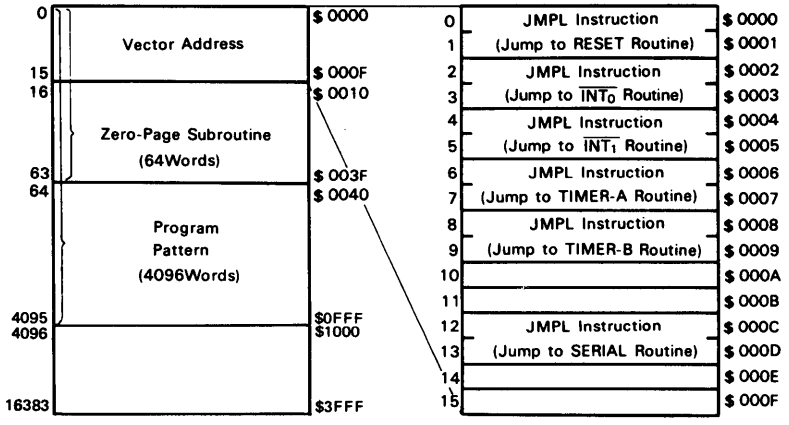
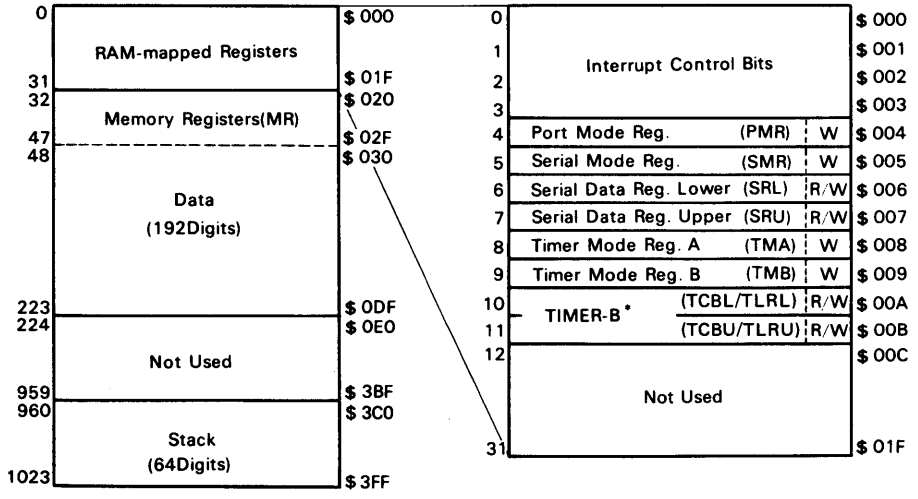


Fig. 1 ROM Memory Map

■ RAM MEMORY MAP

MCU includes 256 digits × 4 bits RAM as the data area and stack area. In addition to these areas, interrupt control bits and special registers are also mapped on the RAM memory space. RAM memory map is illustrated in Fig. 2 and described in the following paragraph.



* Two registers are mapped on same address.

R :Read Only
W :Write Only
R/W:Read/Write

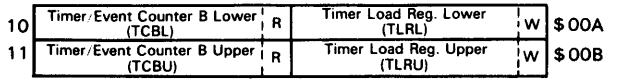


Fig. 2 RAM Memory Map

	bit 3	bit 2	bit 1	bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP Bit)	I/E (Interrupt Enable Flag)	$000
1	IMTA (IM of TIMER-A)	IFTA (IF of TIMER-A)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	Not Used	Not Used	IMTB (IM of TIMER-B)	IFTB (IF of TIMER-B)	$002
3	Not Used	Not Used	IMS (IM of SERIAL)	IFS (IF of SERIAL)	$003

IF : Interrupt Request Flag
IM : Interrupt Mask
I/E : Interrupt Enable Flag
SP : Stack Pointer

(Note) Each bit in Interrupt Control Bits Area is set by SEM/SEMD instruction, is reset by REM/REMD instruction and is tested by TM/TMD instruction. It is not affected by other instructions. Furthermore, Interrupt Request Flag is not affected by SEM/SEMD instruction. The content of Status becomes invarid when "Not Used" bit is tested.

Fig. 3 Configuration of Interrupt Control Bit Area

- **Interrupt Control Bit Area ..... $000 to $003**

This area is used for interrupt controls, and is illustrated in Fig.3. It is accessable only by RAM bit manipulation instruction. However, the interrupt request flag cannot be set by software.

- **Special Register Area ..... $004 to $00B**

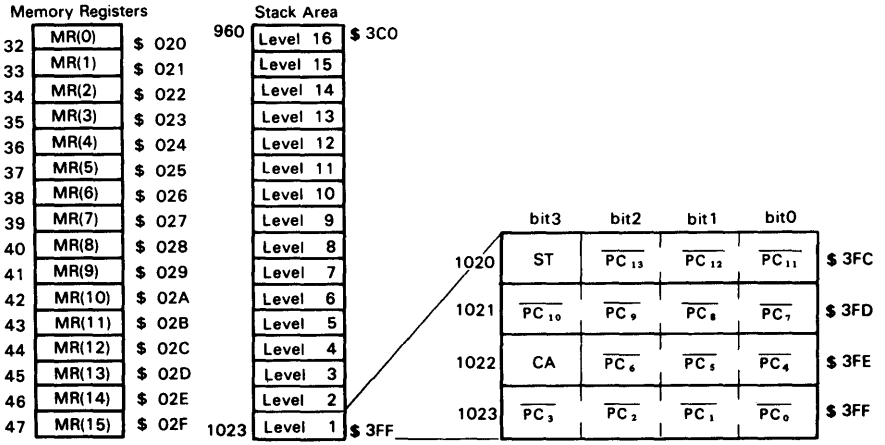
Special Register is a mode or a data register for the external interrupt, the serial interface, and the timer/counter. These registers are classified into 3 types: Write-only, Read-only, and Read/Write as shown in Fig. 2. These registers cannot be accessed by RAM bit manipulation instruction.

- **Data Area ..... $020 to $0DF**

16 digits of $020 to $02F are called memory register (MR) and accessable by LAMR and XMRA instructions.

- **Stack Area .... $3C0 to $3FF**

Stack Area is used for LIFO stacks with the contents of the program counter (PC), status (ST) and carry (CA) when processing subroutine call and interrupt. As 1 level requires 4 digits, this stack area is nested to 16 level-stack max. The data pushed in the stack and LIFO stack state are provided in Fig. 4. The program counter is restored by RTN and RTNI instructions. Status and Carry are restored only by RTNI instruction. The area, not used for stacking, is available as a data area.



PC_{13} to PC_0 ; Program Counter
ST; Status
CA; Carry

Fig. 4 Configuration of Memory Register, Stack Area and Stack Position

■ REGISTER AND FLAG

The MCU has nine registers and two flags for the CPU operations. They are illustrated in Fig. 5 and described in the following paragraphs.

• Accumulator (A), B Register (B)

Accumulator and B Register are 4-bit registers used to hold the results of Arithmetic Logic Unit (ALU), and to transfer data to/from memories, I/O and other registers.

• W Register (W), X Register (X), Y Register (Y)

W Register is 2-bit, and X and Y Register are 4-bit registers used for indirect addressing of RAM. Y register is also used for D-port addressing.

• SPX Register (SPX), SPY Register (SPY)

SPX and SPY Register are 4-bit registers used to assist X and Y Register respectively.

• Carry (CA)

Carry (CA) stores the overflow of ALU generated by the arithmetic operation. It is also affected by SEC, REC, ROTL and ROTR instructions.

During interrupt servicing, Carry is pushed onto the stack and restored back from the stack by RTNI instruction. (It's not affected by RTN instruction.)

• Status (ST)

Status (ST) holds the ALU overflow, ALU non-zero and the results of bit test instruction for the arithmetic or compare instruction. It is used for a branch condition of BR, BRL, CAL or CALL instructions. The value of the Status remains unchanged until the next arithmetic, compare or bit test instruction is executed. Status becomes "1" after the BR, BRL, CAL or CALL instruction has been executed (irrespective of its execution/skip). During the interrupt servicing, Status is pushed onto the stack and restored back from the stack by RTNI instruction. (It's not affected by RTN instruction.)

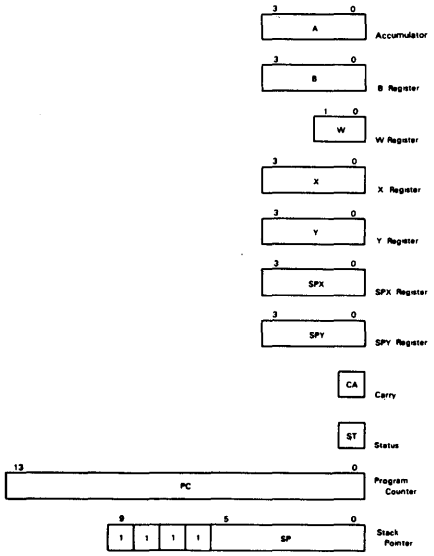


Fig. 5 Register and Flags

• Program Counter (PC)

Program Counter is a 14-bit binary counter for ROM addressing.

• Stack Pointer (SP)

Stack Pointer is used to point the address of the next stacking area up to 16 levels.

The Stack Pointer is initialized to locate $3FF on the RAM address, and is decremented by 4 as data pushed into the stack, and incremented by 4 as data restored back from the stack.

■ INTERRUPT

The MCU can be interrupted by five different sources: the external signals ($\overline{INT_0}$, $\overline{INT_1}$), timer/counter (TIMER-A, TIMER-B), and serial interface (SERIAL). In each sources, the Interrupt Request Flag, Interrupt Mask and interrupt vector address will be used to control and maintain the interrupt request. The Interrupt Enable Flag is also used to control the total interrupt operations.

• Interrupt Control Bit and Interrupt Service

The interrupt control bit is mapped on $000 to $003 of the RAM address and accessable by RAM bit manipulation instruction. (The Interrupt Request Flag (IF) cannot be set by software.) The Interrupt Enable Flag (I/E) and Interrupt Request Flag (IF) are set to "0", and the Interrupt Mask (IM) is set to "1" at the initialization by MCU reset.

Fig. 6 shows the interrupt block diagram. Table 1 shows the interrupt priority and vector addresses, and Table 2 shows the conditions that the interrupt service is executed by any one of the five interrupt sources.

The interrupt request is generated when the Interrupt Request Flag is set to "1" and the Interrupt Mask is "0". If the Interrupt Enable Flag is "1", then the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the five interrupt sources.

Fig. 7 shows the interrupt services sequence, and Fig. 8 shows the interrupt flowchart. If the interrupt is requested, the instruction finishes its execution in the first cycle. The Interrupt Enable Flag is reset in the second cycle. In the second and third cycles, the Carry, Status and Program Counter are pushed onto the stack. In the third cycle, the instruction is executed again after jumping to the vector address.

In each vector address, program JMPL instruction to branch to a starting address of the interrupt routine. The Interrupt Request Flag which caused the interrupt service has to be reset by software in the interrupt routine.

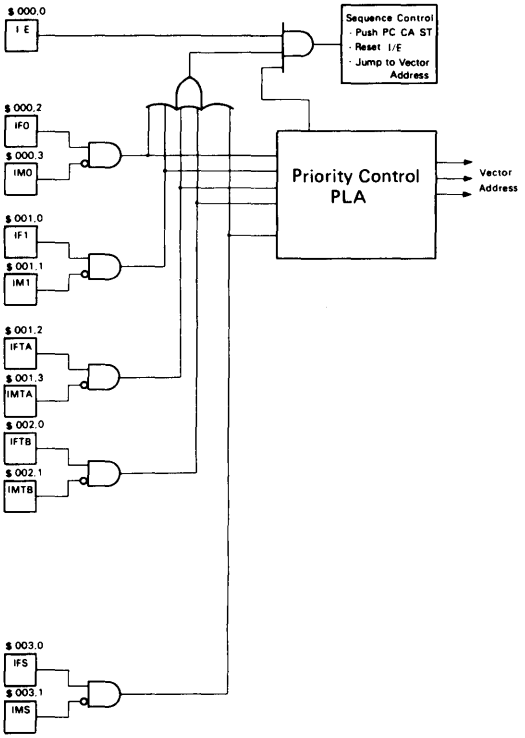


Fig. 6 Interrupt Circuit Block Diagram

Table 1. Vector Addresses and Interrupt Priority

Reset · Interrupt	Priority	Vector addresses
RESET	–	$0000
$\overline{INT_0}$	1	$0002
$\overline{INT_1}$	2	$0004
TIMER-A	3	$0006
TIMER-B	4	$0008
SERIAL	5	$000C

Table 2. Conditions of Interrupt Service

Interrupt source / Interrupt control bits	$\overline{INT_0}$	$\overline{INT_1}$	TIMER-A	TIMER-B	SERIAL
I/E	1	1	1	1	1
IF0·$\overline{IM0}$	1	0	0	0	0
IF1 · $\overline{IM1}$	*	1	0	0	0
IFTA · $\overline{IMTA}$	*	*	1	0	0
IFTB · $\overline{IMTB}$	*	*	*	1	0
IFS · $\overline{IMS}$	*	*	*	*	1

* Don't care

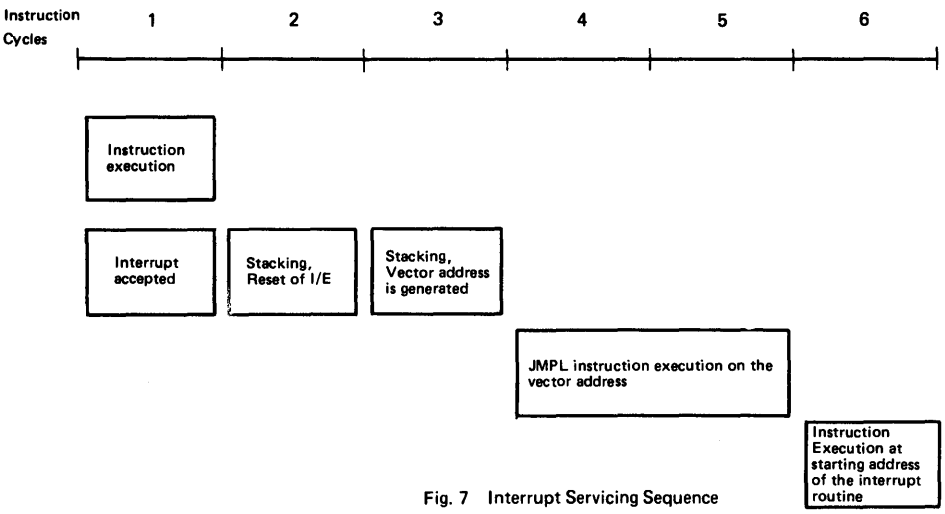


Fig. 7 Interrupt Servicing Sequence

- **Interrupt Enable Flag (I/E: $000,0)**

The Interrupt Enable Flag controls enable/disable of all interrupt requests as shown in Table 3. The Interrupt Enable Flag is reset by the interrupt servicing and set by RTNI instruction.

Table 3. Interrupt Enable Flag

Interrupt Enable Flag	Interrupt Enable/Disable
0	Disable
1	Enable

- **External Interrupt ($\overline{INT_0}$, $\overline{INT_1}$)**

To use external interrupt, select $R_{32}/\overline{INT_0}$, $R_{33}/\overline{INT_1}$ port for $\overline{INT_0}$, $\overline{INT_1}$ mode by setting the Port Mode Register (PMR: $004).

The External Interrupt Request Flags (IF0, IF1) are set at the falling edge of $\overline{INT_0}$, $\overline{INT_1}$ inputs.

$\overline{INT_1}$ input can be used as a clock signal input of TIMER-B. Then, TIMER-B counts up at each falling edge of input. When using $\overline{INT_1}$ as TIMER-B external event, an External Interrupt Mask (IM1) has to be set so that the interrupt request by $\overline{INT_1}$ will not be accepted.

- **External Interrupt Request Flag (IF0: $000,2, IF1: $001,0)**

The External Interrupt Request Flags (IF0, IF1) are set at the falling edges of $\overline{INT_0}$, $\overline{INT_1}$ inputs respectively.

- **External Interrupt Mask (IM0: $000,3, IM1: $001,1)**

The External Interrupt Mask is used to mask the external interrupt requests.

Table 4. External Interrupt Request Flag

External Interrupt Request Flags	Interrupt Requests
0	No
1	Yes

Table 5. External Interrupt Mask

External Interrupt Masks	Interrupt Requests
0	Enable
1	Disable (masks)

- **Port Mode Register (PMR: $004)**

The Port Mode Register is a 4-bit write-only register which controls the $R_{32}/\overline{INT_0}$ pin, $R_{33}/\overline{INT_1}$ pin, R_{41}/SI pin and R_{42}/SO pin as shown in Table 6. The Port Mode Register will be initialized to $0 by MCU reset, so that all these pins are set to a port mode.

Table 6. Port Mode Register

PMR bit 3	$R_{33}/\overline{INT_1}$ pin
0	Used as R_{33} port input/output pin
1	Used as $\overline{INT_1}$ input pin

PMR bit 2	$R_{32}/\overline{INT_0}$ pin
0	Used as R_{32} port input/output pin
1	Used as $\overline{INT_0}$ input pin

PMR bit 1	R_{41}/SI pin
0	Used as R_{41} port input/output pin
1	Used as SI input pin

PMR bit 0	R_{42}/SO pin
0	Used as R_{42} port input/output pin
1	Used as SO output pin

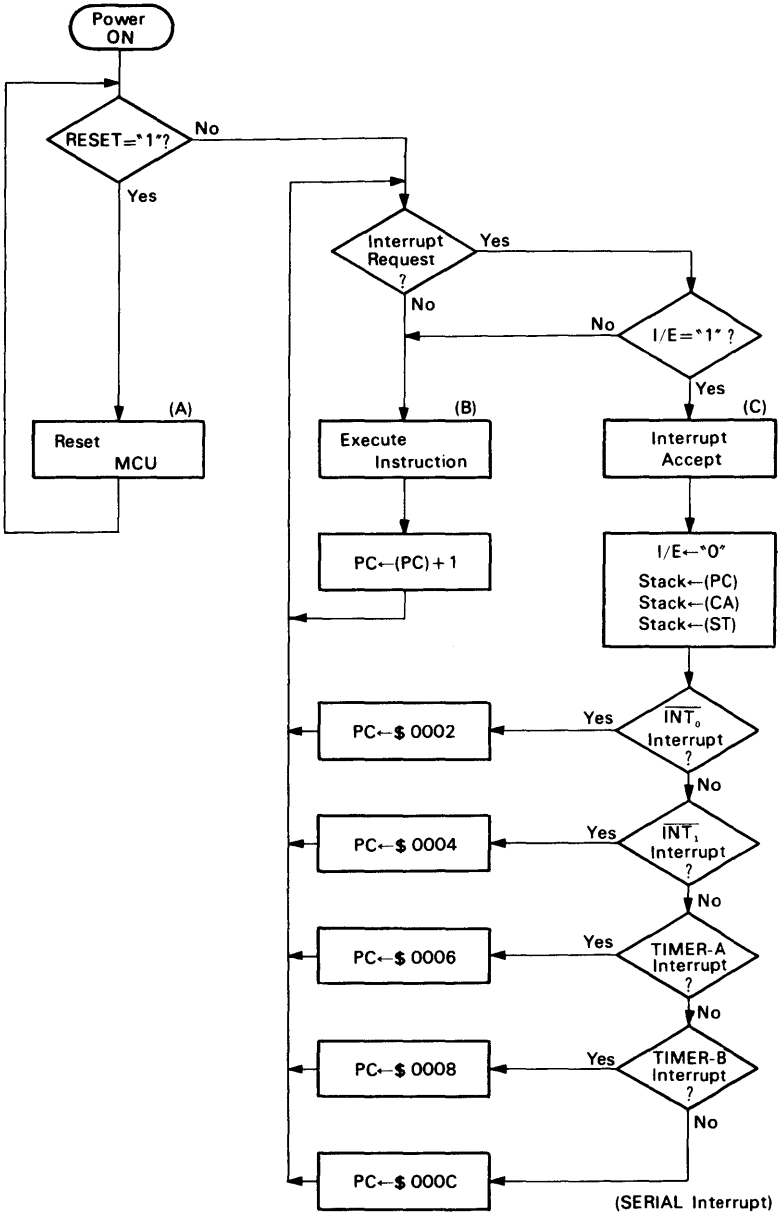


Fig. 8 Interrupt Servicing Flowchart

■ SERIAL INTERFACE

The serial interface is used to transmit/receive 8-bit data serially. This consists of the Serial Data Register, the Serial Mode Register, the Octal Counter and the multiplexer, as illustrated in Fig. 9. Pin $R_{40}/\overline{SCK}$ and the transfer clock signal are controlled by the Serial Mode Register. Contents of the Serial Data Register can be written into or read out by the software. The data in the Serial Data Register can be shifted synchronously with the transfer clock signal.

The serial interface operation is initiated with STS instruction. The Octal Counter is reset to $0 by STS instruction. It starts to count at the falling edge of the transfer clock ($\overline{SCK}$) signal and increments by one at the rising edge of the $\overline{SCK}$. When the Octal Counter is reset to $0 after eight transfer clock signals, or discontinued transmit/receive operation by resetting the Octal Counter, the SERIAL Interrupt Request Flag will be set.

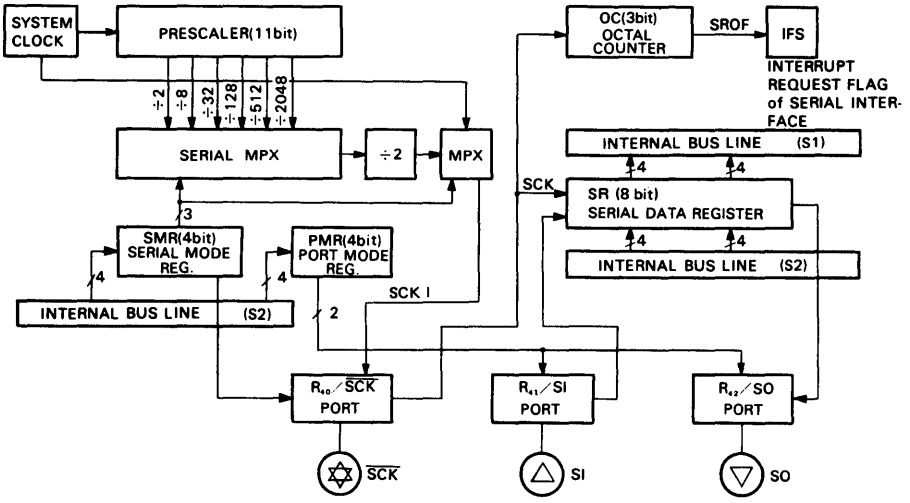


Fig. 9 Serial Interface Block Diagram

• Serial Mode Register (SMR: $005)

The Serial Mode Register is a 4-bit write-only register. This register controls the $R_{40}/\overline{SCK}$ and the prescaler divide ratio as the transfer clock source as shown in Table 7.

The Write Signal to the Serial Mode Register controls the operating state of serial interface.

The Write Signal to the Serial Mode Register stops the transfer clock applied to the Serial Data Register and the Octal Counter. And it also reset the Octal Counter to $0 simultaneously.

When the Serial Interface is in the "Transfer State", the Write Signal to the Serial Mode Register causes to quit the data transfer and to set the SERIAL Interrupt Request Flag.

Contents of the Serial Mode Register will be changed on the second instruction cycle after writing into the Serial Mode Register. Therefore, it will be necessary to execute the STS instruction after the data in the Serial Mode Register has been changed completely. The Serial Mode Register will be reset to $0 by MCU reset.

• Serial Data Register (SRL: $006, SRU: $007)

The Serial Data Register is an 8-bit read/write register. It consists of a low-order digit (SRL:$006) and a high-order digit (SRU: $007).

The data in the Serial Data Register will be output from the LSB side at SO pin synchronously with the falling edge of the transfer clock signal. At the same time, external data will be input from the LSB side at SI pin to the Serial Data Register synchronously with the rising edge of the transfer clock. Fig. 10 shows the I/O timing chart for the transfer clock signal and the data.

The writing into/reading from the Serial Data Register during its shifting causes the validity of the data.

Therefore complete data transmit/receive before writing into/reading from the serial data register.

Table 7. Serial Mode Register

SMR Bit 3	$R_{40}/\overline{SCK}$
0	Used as R_{40} port input/output pin
1	Used as $\overline{SCK}$ input/output pin

SMR			Transfer Clock			
Bit 2	Bit 1	Bit 0	$R_{40}/\overline{SCK}$ Port	Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio
0	0	0	$\overline{SCK}$ Output	Prescaler	÷ 2048	÷ 4096
0	0	1	$\overline{SCK}$ Output	Prescaler	÷ 512	÷ 1024
0	1	0	$\overline{SCK}$ Output	Prescaler	÷ 128	÷ 256
0	1	1	$\overline{SCK}$ Output	Prescaler	÷ 32	÷ 64
1	0	0	$\overline{SCK}$ Output	Prescaler	÷ 8	÷ 16
1	0	1	$\overline{SCK}$ Output	Prescaler	÷ 2	÷ 4
1	1	0	$\overline{SCK}$ Output	System Clock	–	÷ 1
1	1	1	$\overline{SCK}$ Input	External Clock	–	–

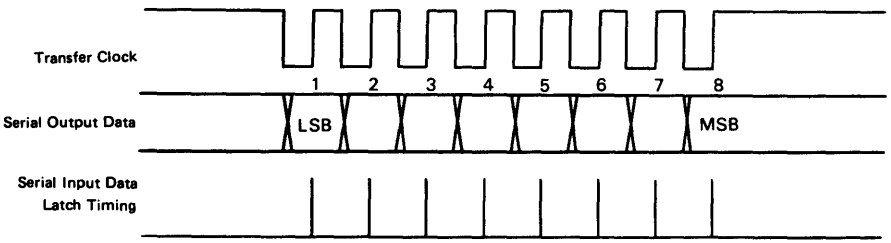


Fig. 10 Serial Interface I/O Timing Chart

- **SERIAL Interrupt Request Flag (IFS: $003, 0)**

The SERIAL Interrupt Request Flag will be set after the eight transfer clock signals or transmit/receive discontinued operation by resetting the Octal Counter.

- **SERIAL Interrupt Mask (IMS: $003, 1)**

The SERIAL Interrupt Mask masks the interrupt request.

Table 8. SERIAL Interrupt Request Flag

SERIAL Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 9. SERIAL Interrupt Mask

SERIAL Interrupt Mask	Interrupt Request
0	Enable
1	Disable (mask)

- **Selection of the Operation Mode**

Table 10 shows the operation mode of the serial interface. Select a combination of the value in the Port Mode Register and the Serial Mode Register according to Table 10.

Initialize the serial interface by the Write Signal to the Serial Mode Register, when the Operation Mode is changed.

- **Operating State of Serial Interface**

The serial interface has 3 operating states as shown in Fig. 11.

The serial interface gets into "STS waiting state" by 2 ways: one way is to change the operation mode by changing the data

in the Port Mode Register, the other is to write data into the Serial Mode Register. In this state, the serial interface does not operate although the transfer clock is applied. If STS instruction is executed, the serial interface changes its state to "SCK waiting state".

In the "SCK waiting state", the falling edge of first transfer clock affects the serial interface to get into "transfer state", while the Octal Counter counts-up and the Serial Data Register shifts simultaneously. As an exception, if the clock continuous output mode is selected, the serial interface stays in "SCK waiting state" while the transfer clock outputs continuously.

The Octal Counter becomes "000" again by 8 transfer clocks or execution of STS instruction, so that the serial interface gets back into the "SCK waiting state", and SERIAL Interrupt Request Flag is set simultaneously.

When the internal transfer clock is selected, the transfer clock output are triggered by the execution of STS instruction, and it stops after 8 clocks.

- **Example of Transfer Clock Error Detection**

The serial interface functions abnormally when the transfer clock was disturbed by external noises. In this case, the transfer clock error can be detected in the procedure shown in Fig. 12.

If more than 9 transfer clocks are applied by the external noises in the "SCK waiting state", the state of the serial interface shifts as the following sequence: first "transfer state" (while 1 to 7 transfer clocks), second "SCK waiting state" (at 8th transfer clock) and third "transfer state" again. Then reset the SERIAL Interrupt Request Flag, and make "STS waiting state" by writing to the Serial Mode Register. SERIAL Interrupt Request Flag is set again in this procedure, and it shows that the transfer clock was invalid and that the transmit/receive data were also invalid.

Table 10. Serial Interface Operation Mode

SMR	PMR		Serial Interface Operating Mode
Bit 3	Bit 1	Bit 0	
1	0	0	Clock Continuous Output Mode
1	0	1	Transmit Mode
1	1	0	Receive Mode
1	1	1	Transmit/Receive Mode

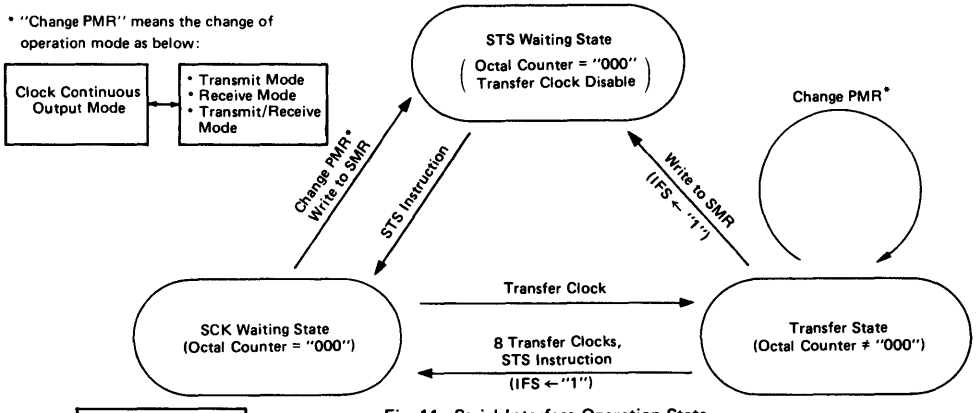


Fig. 11 Serial Interface Operation State

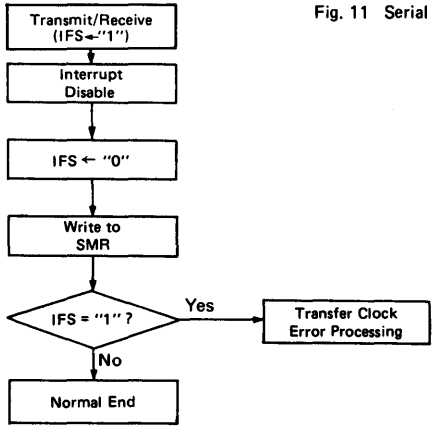


Fig. 12 Example of Transfer Clock Error Detection

- **TIMER**

The MCU contains a prescaler and two timer/counters (TIMER-A, TIMER-B), Fig. 13 shows the block diagram. The prescaler is an 11-bit binary counter. TIMER-A is an 8-bit free-running timer. TIMER-B is an 8-bit auto-reload timer/event counter.

- **Prescaler**

The input to the prescaler is a system clock signal. The prescaler is initialized to $000 by MCU reset, and the prescaler starts to count up the system clock signal as soon as RESET input goes to logic "0". The prescaler keeps counting up except MCU reset and stop mode. The prescaler provides clock signals to TIMER-A, TIMER-B and serial interface. The prescaler devide ratio of the clock signals are selected according to the content of the mode registers such as – Timer Mode Register A (TMA), Timer Mode Register B (TMB), Serial Mode Register (SMR).

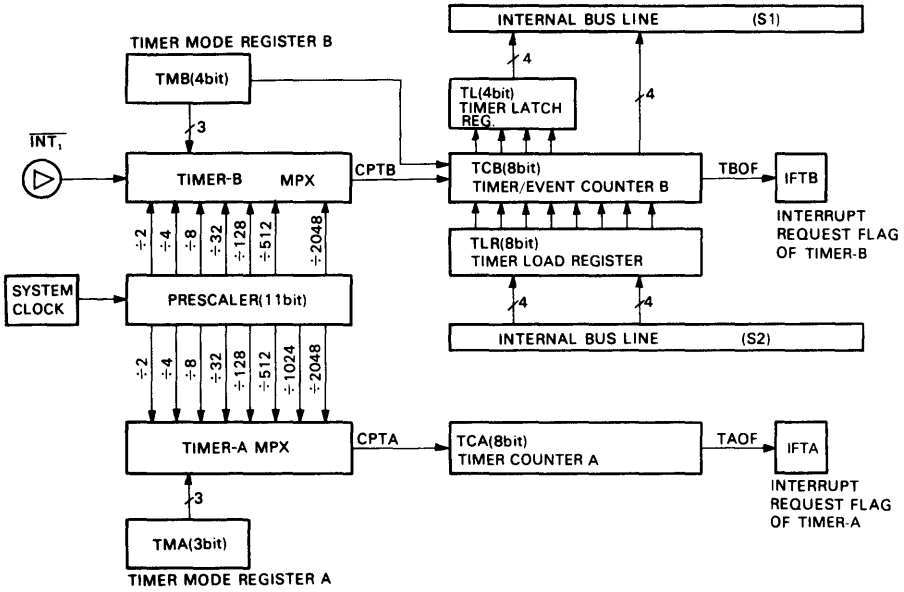


Fig. 13 Timer/Counter Block Diagram

- **TIMER-A Operation**

After TIMER-A is initialized to $00 by MCU reset, it counts up at every clock input signal. When the next clock signal is applied after TIMER-A is counted up to $FF, TIMER-A is set to $00 again, and generating overflow output. This leads to setting TIMER-A Interrupt Request Flag (IFTA: $001, 2) to "1". Therefore, this timer can function as an interval timer periodically generating overflow output at every 256th clock signal input.

The clock input signals to TIMER-A are selected by the Timer Mode Register A (TMA: $008).

- **TIMER-B Operation**

Timer Mode Register B (TMB: $009) is used to select the auto-reload function and the prescaler divide ratio of TIMER-B as the input clock source. When the external event input is used as an input clock signal to TIMER-B, select the $R_{33}/\overline{INT_1}$ as $\overline{INT_1}$ and set the External Interrupt Mask (IM1) to "1" to prevent the external interrupt request from occurring.

TIMER-B is initialized according to the value written into the Timer Load Register by software. TIMER-B counts up at every clock input signal. When the next clock signal is applied to TIMER-B after TIMER-B is set to $FF, TIMER-B will be initialized again and generate overflow output. In this case if the auto-reload function is selected. TIMER-B is initialized according to the value of the Timer Load Register. Else if the auto-reload function is not selected, TIMER-B goes to $00. TIMER-B Interrupt Request Flag (IFTB: $002,0) will be set at this overflow output.

- **Timer Mode Register A (TMA: $008)**

The Timer Mode Register A is a 3-bit write-only register. The TMA controls the prescaler divide ratio of TIMER-A clock input, as shown in Table 11.

The Timer Mode Register A is initialized to $0 by MCU reset.

- **Timer Mode Register B (TMB: $009)**

The Timer Mode Register B is a 4-bit write-only register. The Timer Mode Register B controls the selection for the auto-reload function of TIMER-B and the prescaler divide ratio, and the source of the clock input signal, as shown in Table 12.

The Timer Mode Register B is initialized to $0 by MCU reset.

The operation mode of TIMER-B is changed at the second instruction cycle after writing into the Timer Mode Register B. Therefore, it is necessary to program the write instruction to TLRU after the content of TMB is changed.

Table 11. Timer Mode Register A

TMA			Prescaler Divide Ratio
Bit 2	Bit 1	Bit 0	
0	0	0	÷2048
0	0	1	÷1024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	0	÷ 32
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2

Table 12. Timer Mode Register B

TMB Bit 3	Auto-reload Function
0	No
1	Yes

TMB Bit 2	TMB Bit 1	TMB Bit 0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	$\overline{INT_1}$ (External Event Input)

- **TIMER-B (TCBL: $00A, TCBU: $00B / TLRL: $00A, TLRU: $00B)**

TIMER-B consists of an 8-bit write-only Timer Load Register, and an 8-bit read-only Timer/Event Counter. Each of them has a low-order digit (TCBL: $00A, TLRL: $00A) and a high-order digit (TCBU: $00B, TLRU: $00B).

The Timer/Event Counter can be initialized by writing data into the Timer Load Register. In this case, write the low-order digit first, and then the high-order digit. The Timer/Event Counter is initialized at the time when the high-order digit is written. The Timer Load Register will be initialized to $00 by the MCU reset.

The counter value of TIMER-B can be obtained by reading the Timer/Event Counter. In this case, read the high-order digit first, and then the low-order digit. The count value of low-order digit is latched at the time when the high-order digit is read.

- **TIMER-A Interrupt Request Flag (IFTA: $001, 2)**

The TIMER-A Interrupt Request Flag is set by the overflow output of TIMER-A.

- **TIMER-A Interrupt Mask (IMTA: $001, 3)**

TIMER-A Interrupt Mask prevents an interrupt request generated by TIMER-A Interrupt Request Flag.

Table 13. TIMER-A Interrupt Request Flag

TIMER-A Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 14. TIMER-A Interrupt Mask

TIMER-A Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

- **TIMER-B Interrupt Request Flag (IFTB: $002, 0)**

The TIMER-B Interrupt Request Flag is set by the overflow output of TIMER-B.

- **TIMER-B Interrupt Mask (IMTB: $002, 1)**

TIMER-B Interrupt Mask prevents an interrupt request generated by TIMER-B Interrupt Request Flag.

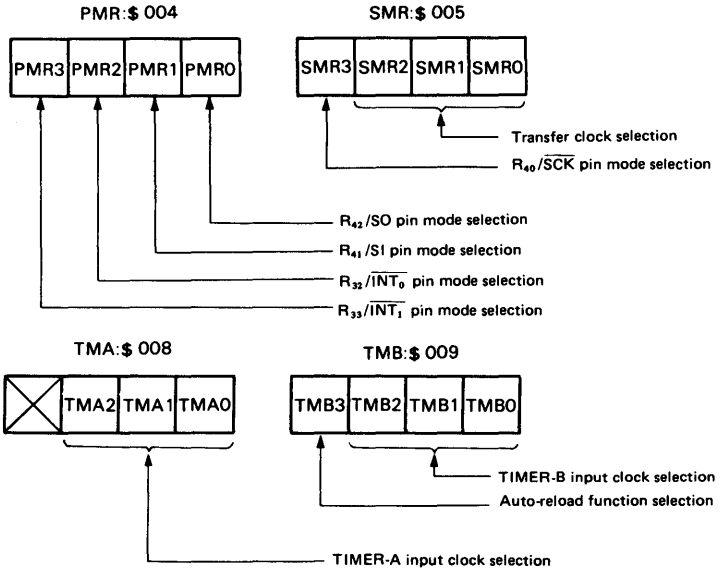


Fig. 14 Mode Register Configuration and Function

Table 15. TIMER-B Interrupt Request Flag

TIMER-B Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 16. TIMER-B Interrupt Mask

TIMER-B Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

■ INPUT/OUTPUT

The MCU provides 58 Input/Output pins, and they are consist of 32 standard pins and 26 high voltage pins. Each standard pin may have one of three mask options: (A) "Without pull-up MOS (NMOS open drain)", (B) "With pull-up MOS", or (C) "CMOS". And also each high voltage pin may have one of two mask options: (D) "Without pull-down MOS (PMOS open drain)", or (E) "With pull-down MOS". As pull-down MOS is connected to internal V_{disp} line, select R_{A1}/V_{disp} pin as V_{disp} with mask option when at least one high voltage pin is selected as "With pull-down MOS" option.

When any Input/Output common pin is used as input pin, it is necessary to select the mask option and output data as shown in Table 18.

• Output Circuit Operation of Standard Pins with "With pull-up MOS" Option

Fig. 15 shows the circuit used in the standard pins with "with pull-up MOS"option.

By execution of the output instruction, the write pulse will be generated, and be applied to the addressed port. This pulse will turn "ON" the PMOS (B) to make the transient time shorten to obtain "High level", if the output data is changed from "0" to "1". In this case, the "write pulse" allows the PMOS (B) to turn "ON" as long as 1/8 instruction cycle. While "write pulse" is "0", pull-up MOS (C) may retain the output in high level.

The $\overline{HLT}$ signal becomes "0" in stop mode, so that MOS (A) (B) (C) turn "OFF".

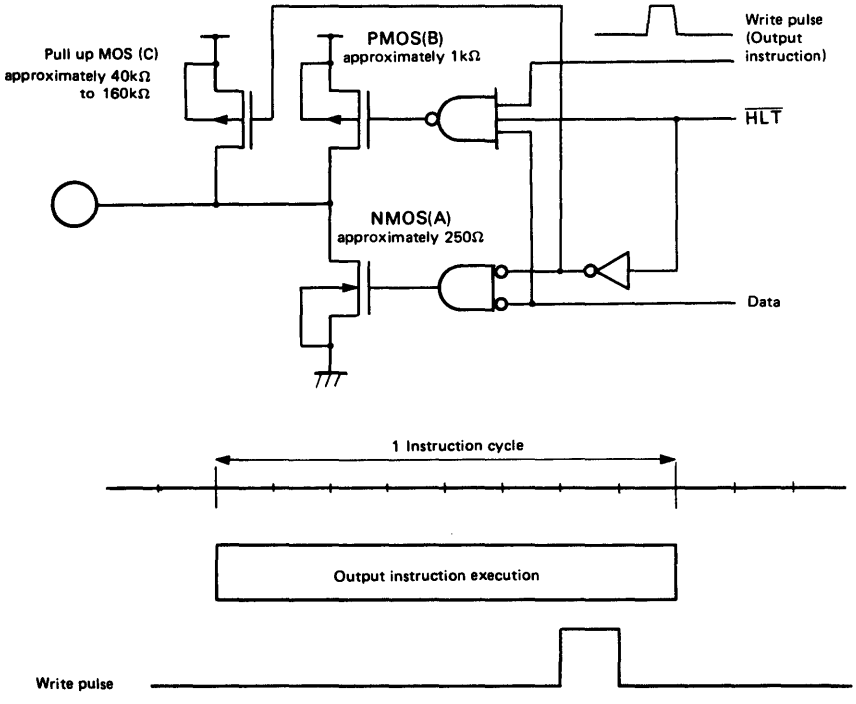
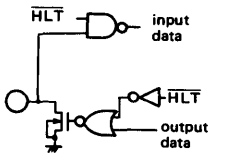
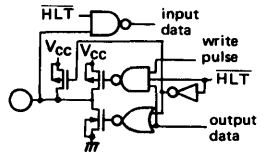
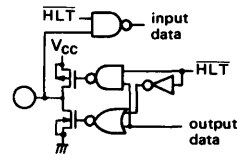
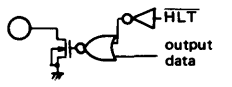
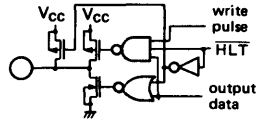
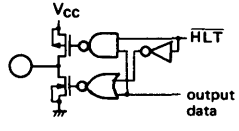
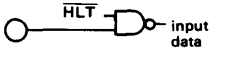
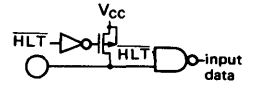
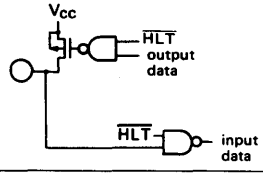
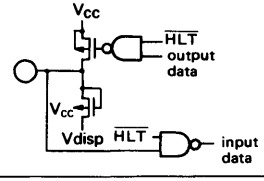
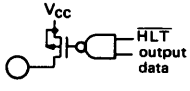
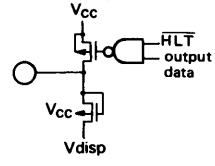
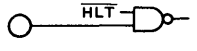
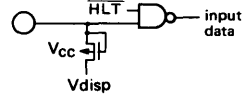


Fig. 15 Output Circuit Operation of Standard Pins with "with Pull-up MOS" Option

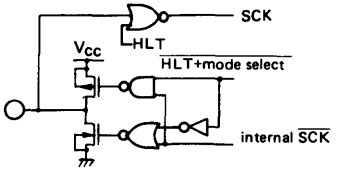
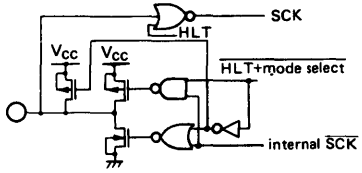
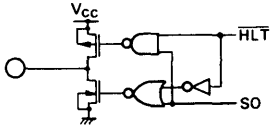
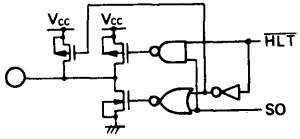
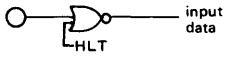
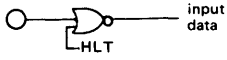
Table 17 I/O Pin Circuit Type

		Without pull-up MOS (NMOS open drain) (A)	With pull-up MOS (B)	CMOS (C)	Applied pins
Standard pins	I/O common pins				D0 ~D3, R30 ~R33, R40 ~R43, R50 ~R53
	Output pins				R60~R63, R70~R73, R80~R83
	Input pins				R90~R93

		Without pull-down MOS (PMOS open drain) (D)	With pull-down MOS (E)	Applied pins
High voltage pins	I/O common pins			D4~D15, R10~R13, R20~R23
	Output pins			R00~R03
	Input pins			RA0, RA1/Vdisp

(Note) In the stop mode, $\overline{HLT}$ signal is "0" and I/O pins are in high impedance state.

(to be continued)

		Without pull-up MOS (NMOS open drain) or CMOS (A or C)	With pull-up MOS (B)	Applied pins
Standard pins	I/O common pins			$\overline{SCK}$
	Output pins			SO
	Input pins			$\overline{INT_0}$, $\overline{INT_1}$, SI

(Note) In the stop mode, $\overline{HLT}$ signal is "0", HLT signal is "1" and I/O pins are in high impedance state.

Table 18 Data Input from Input/Output Common Pins

I/O pin circuit type		Possibility of Input	Available pin condition for input
Standard pins	CMOS	No	–
	Without pull-up MOS (NMOS open drain)	Yes	"1"
	With pull-up MOS	Yes	"1"
High voltage pins	Without pull-down MOS (PMOS open drain)	Yes	"0"
	With pull-down MOS	Yes	"0"

• **D-port**

D-port is 1-bit I/O port, and it has 16 Input/Output common pins. It can be set/reset by the SED/RED and SEDD/REDD instructions, and can be tested by the TD and TDD instructions. Table 17 shows the classification of standard pins, high voltage pins and the Input/Output pins circuit types.

• **R-port**

R-port is 4-bit I/O port. It provides 20 input/output common pins, 16 output-only pins, and 6 input-only pins. Data input is processed using the LAR and LBR instructions and data output is processed using the LRA and LRB instructions. The MCU will not be affected by writing into the input-only and/or non-existing ports, invalid data will be read by reading from the output-only and/or non-existing ports.

The R_{32}, R_{33}, R_{40}, R_{41} and R_{42} pins are also used as the $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK}$, SI and SO pins respectively. Table 17 shows the classification of standard pins, high voltage pins and Input/Output pins circuit types.

■ **RESET**

The MCU is reset by setting RESET pin to "1". At power ON or recovering from stop mode, apply RESET input more than t_{RC} to obtain the necessary time for oscillator stabilization. In other cases, the MCU reset requires at least two instructions cycle time of RESET input.

Table 19 shows initialized items by MCU reset and each status after reset.

Table 19 Initial Value by MCU Reset

Items			Initial value by MCU reset	Contents
Program counter (PC)			$0000	Execute program from the top of ROM address.
Status (ST)			"1"	Enable to branch with conditional branch instructions.
Stack pointer (SP)			$3FF	Stack level is 0.
I/O pin output register	Standard pin	(A) Without pull-up MOS	"1"	Enable to input.
		(B) With pull-up MOS	"1"	Enable to input
		(C) CMOS	"1"	–
	High voltage pin	(D) Without pull-down MOS	"0"	Enable to input.
		(E) With pull-down MOS	"0"	Enable to input.
Interrupt flag	Interrupt Enable Flag (I/E)		"0"	Inhibit all interrupts.
	Interrupt Request Flag (IF)		"0"	No interrupt request.
	Interrupt Mask (IM)		"1"	Mask interrupt request.
Mode register	Port Mode Register (PMR)		"0000"	See Item "Port Mode Register".
	Serial Mode Register (SMR)		"0000"	See Item "Serial Mode Register".
	Timer Mode Register A (TMA)		"000"	See Item "Timer Mode Register A".
	Timer Mode Register B (TMB)		"0000"	See Item "Timer Mode Register B".
Timer/Counter, Serial interface	Prescaler		$000	–
	Timer/Counter A (TCA)		$00	–
	Timer/Event Counter B (TCB)		$00	–
	Timer Load Register (TLR)		$00	–
	Octal Counter		"000"	–

(Note) MCU reset affects to the rest of registers as follows:

Item		After recovering from STOP mode by MCU reset	After MCU reset except for the left condition
Carry	(CA)	The contents of the items before MCU reset are not retained. It is necessary to intialize them by software again.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software again.
Accumulator	(A)		
B Register	(B)		
W Register	(W)		
X/SPX Registers	(X/SPX)		
Y/SPY Registers	(Y/SPY)		
Serial Data Register	(SR)	Same as above	Same as above
RAM		The contents of RAM before MCU reset (just before STOP instruction) are retained.	Same as above

■ INTERNAL OSCILLATOR CIRCUIT

Fig. 16 gives internal oscillator circuit. The oscillator type can be selected from the followings; crystal oscillator, ceramic filter oscillator, or resistor oscillator as shown in Table 20. In any cases, external clock operation is available.

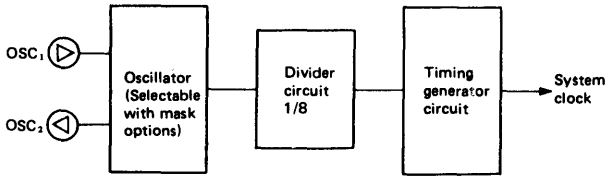


Fig. 16 Internal Oscillator Circuit

• Oscillator Circuit

Table 20 Examples of Oscillator Circuit

	Circuit configuration	Remarks
External clock operation	Oscillator OSC1 Open — OSC2	
Resistor oscillator	Rf OSC1 OSC2	Rf: 20kΩ±2%
Ceramic filter oscillator	C1 Ceramic filter OSC1 Rf OSC2 C2 GND	Ceramic filter CSA4.00MG (Murata) Rf : 1MΩ±2% C1 : 30pF±20% C2 : 30pF±20% • Wiring between these pins and elements should be as short as possible, and never cross the other wirings. (Refer to Fig. 17)
Crystal oscillator	C1 Crystal OSC1 Rf OSC2 C2 GND AT cut parallel resonance crystal OSC1 — L C1 Rs — OSC2 Co	Rf : 1MΩ±2% C1 : 10~22pF±20% C2 : 10~22pF±20% Crystal: AT cut parallel resonance crystal Co : 7pF max. Rs : 60Ω max. f : 2.0~4.5MHz • Wiring between these pins should be as short as possible, and never cross the other wirings. (Refer to Fig. 17)

Note) Please consult with the engineers of crystal or ceramic filter maker to determine the value of R_f, C_1 and C_2.

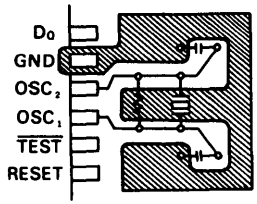


Fig. 17 Recommendable Layout of Crystal and Ceramic Filter

■ LOW POWER DISSIPATION MODE

The MCU provides two low power dissipation modes, that is, a Standby mode and a Stop mode. Table 21 shows the function of the low power dissipation mode, and Fig. 18 shows the diagram of the mode transition.

Table 21 Low Power Dissipation Mode Function

Low Power Dissipation Mode	Instruction	Condition							Recovering method
		Oscillator circuit	Instruction execution	Register, Flag	Interrupt function	RAM	Input/ Output pin	Timer/ Counter, Serial Interface	
Standby mode	SBY instruction	Active	Stop	Retained	Active	Retained	Retained*3)	Active	RESET Input, Interrupt request
Stop mode	STOP instruction	Stop	Stop	RESET*1)	Stop	Retained	High*2) impedance	Stop	RESET Input

*1) As the MCU recovers from STOP mode by RESET input, the contents of the flags and registers are initialized according to Table 19.
*2) A high voltage pin with a pull-down MOS option is pulled down to the V_{disp} power supply by the pull-down MOS. As the MOS is ON, a pull-down MOS current flows when a voltage difference between the pin and the V_{disp} voltage exists. This is the additional current to the current dissipation in Stop Mode (I_{stop}).
*3) As a I/O circuit is active, a I/O current possibly flows according the state of I/O pin. This is the additional current to the current dissipation in Standby Mode (I_{SBY1}, I_{SBY2}).

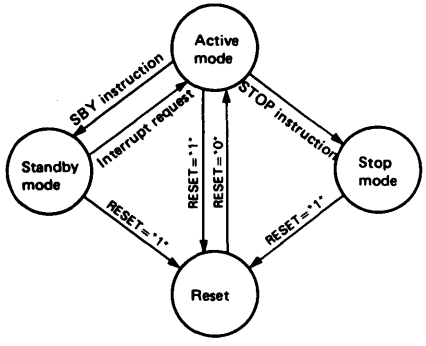


Fig. 18 MCU Operation Mode Transition

• Standby Mode

The SBY instruction puts the MCU into the Standby mode. In the Standby mode, the oscillator circuit is active and timer/counter and serial interface continue working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM and Input/Output pins retain the state they had just before going into the Standby mode.

The Standby mode is canceled by the MCU reset or interrupt request. When canceled by the interrupt request, the MCU becomes an active mode and executes the instruction next to the SBY instruction. At this time, if the Interrupt Enable Flag is "1", the interrupt is executed. If the Interrupt Enable Flag is "0", the interrupt request is held on and the normal instruction execution continues.

Fig. 19 shows the flowchart of the Standby Mode.

• Stop Mode

The STOP instruction brings the MCU into the Stop mode. In this mode the oscillator circuit and every function of the MCU stop.

The Stop mode is canceled by the MCU reset. At this time, as shown in Fig. 20, apply the RESET input for more than t_{RC} to get enough oscillator stabilization time. (Refer to the "AC CHARACTERISTICS".) After the Stop mode is canceled, RAM retains the state it had just before going into the Stop mode. The other hand, Accumulator, B Register, W Register, X/SPX Registers, Y/SPY Registers, Carry and Serial Data Register don't retain the contents.

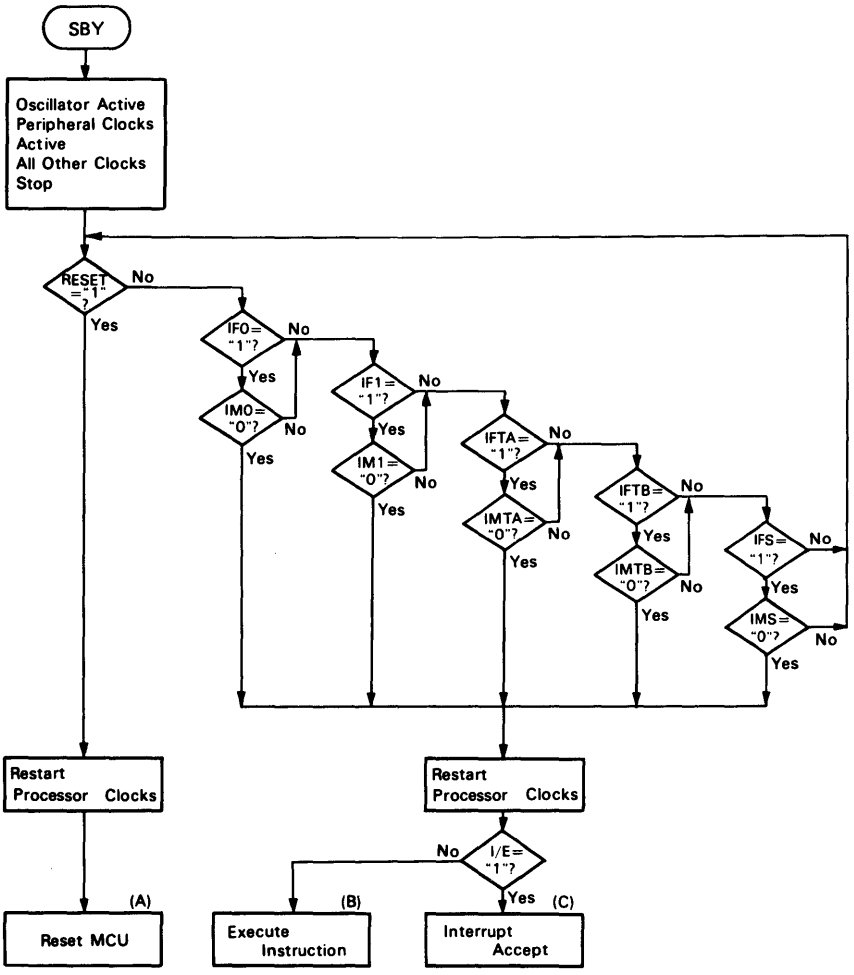


Fig. 19 MCU Operating Flowchart

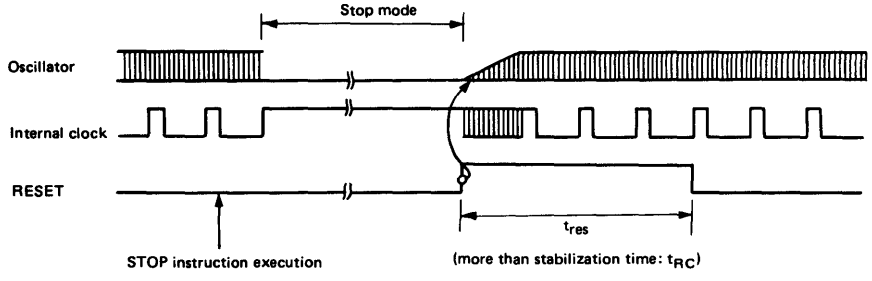


Fig. 20 Timing Chart of Recovering from Stop Mode

■ RAM ADDRESSING MODE

As shown in Fig. 21, the MCU provides three RAM addressing modes; Register Indirect Addressing, Direct Addressing and Memory Register Addressing.

• Register Indirect Addressing

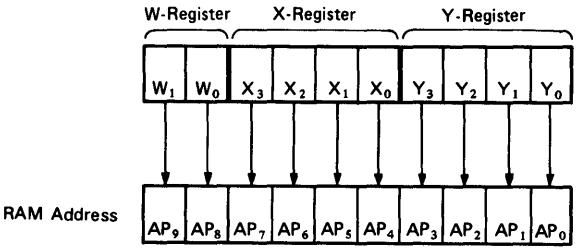
The combined 10-bit contents of W Register, X Register and Y Register is used as the RAM address in this mode.

• Direct Addressing

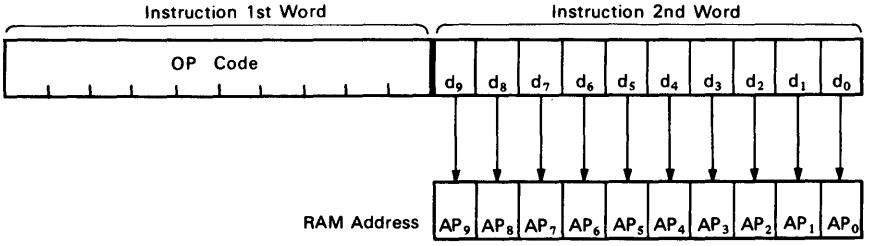
The direct addressing instruction consists of two words and the second word (10 bits) following Op-code (the first word) is used as the RAM address.

• Memory Register Addressing

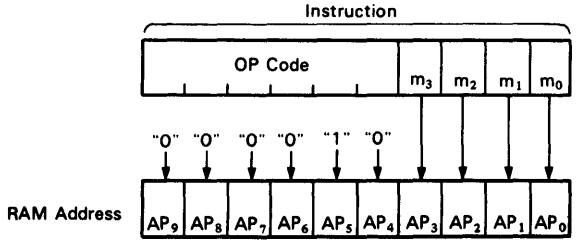
The Memory Register Addressing can access 16 digits (Memory Register: MR) from $020 to $02F by using the LAMR and XMRA instruction.



(a) Register Indirect Addressing



(b) Direct Addressing



(c) Memory Register Addressing

Fig. 21 RAM Addressing Mode

■ ROM ADDRESSING MODE AND P INSTRUCTION

The MCU has four kinds of ROM addressing modes as shown in Fig. 22.

• Direct Addressing Mode

The program can branch to any addresses in the ROM memory space by using JMPL, BRL or CALL instruction. These instruction replace 14-bit program counter (PC_{13} to PC_0) with 14-bit immediate data.

• Current Page Addressing Mode

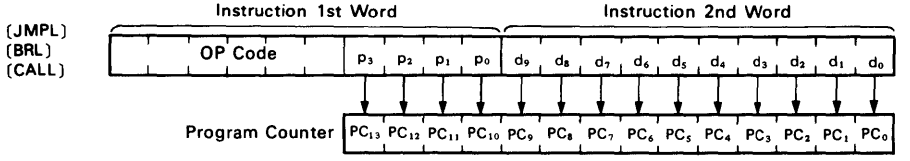
MCU has 8 pages of ROM(256 words in each page).The program branches to the address in the same page using BR instruction. This instruction replace the low-order eight bits of program counter (PC_7 to PC_0) with 8-bit immediate data.

• Zero Page Addressing Mode

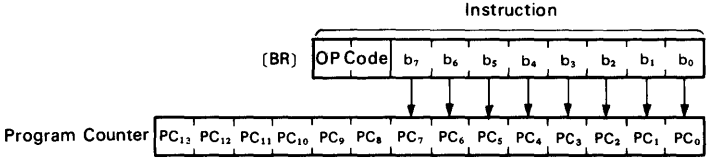
The program branches to the zero page subroutine area, which is located on the address from $0000 to $003F, using CAL instruction. When CAL instruction is executed, 6-bit immediate data is placed in low-order six bits of program counter (PC_5 to PC_0) and "0's" are placed in high-order eight bits (PC_{13} to PC_6). The branch destination by BR instruction on the broundary between pages is given in Fig. 24.

• Table Data Addressing

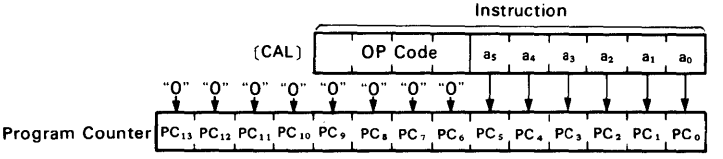
The program branches to the address determined by the contents of the 4-bit immediate data, accumulator and B register, using TBR instruction.



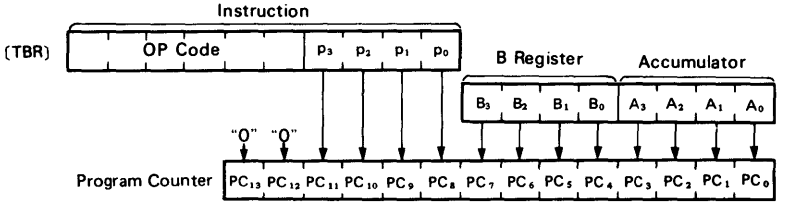
(a) Direct Addressing



(b) Current Page Addressing

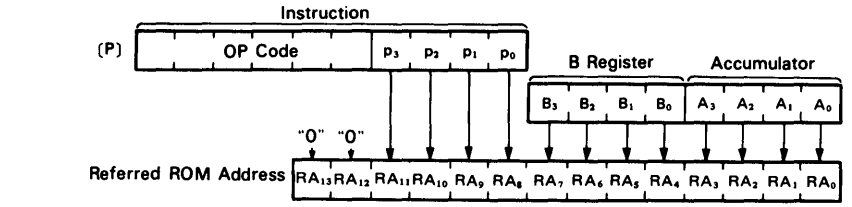


(c) Zero Page Addressing

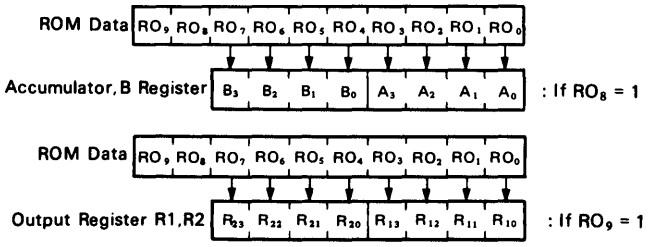


(d) Table Data Addressing

Fig. 22 ROM Addressing Mode



(a) Address Designation



(b) Pattern Output

Fig. 23 P Instruction

- **P Instruction**

The P instruction refers ROM data addressed by Table Data Addressing. ROM data addressed also determine its destination. When bit 8 in referred ROM data is "1", 8 bits of referred ROM data are written into the accumulator and B Register. When bit 9 is "1", 8 bits of referred ROM data are written into the R1 and R2 port output register. When both bit 8 and 9 are "1", ROM data are written into the accumulator and B Register and also to the R1 and R2 port output register at a same time.

The P instruction has no effect on the program counter.

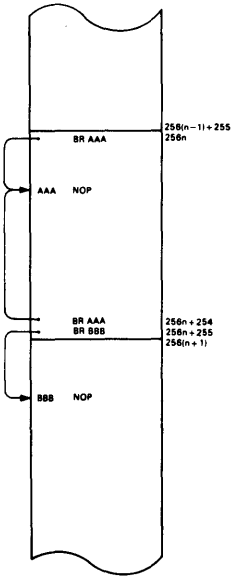


Fig. 24 The Branch Destination by BR Instruction on the Boundary between Pages

■ INSTRUCTION SET

The HMCS400 series provide 99 instructions. These instructions are classified into 10 groups as follows;

(1) Immediate Instruction
(2) Register-to-Register Instruction
(3) RAM Address Instruction
(4) RAM Register Instruction
(5) Arithmetic Instruction
(6) Compare Instruction
(7) RAM Bit Manipulation Instruction
(8) ROM Address Instruction
(9) Input/Output Instruction
(10) Control Instruction

Table 22. Immediate Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Load A from Immediate	LAI i	1 0 0 0 1 1 i_3 i_2 i_1 i_0	i⟶A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i_3 i_2 i_1 i_0	i⟶B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i⟶M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i_3 i_2 i_1 i_0	i→M,Y+1→Y	NZ	1/1

Table 23. Register-to-Register Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B→A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A→B		1/1
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y→A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX→A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY→A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m_3 m_2 m_1 m_0	MR(m)→A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m_3 m_2 m_1 m_0	MR(m)↔A		1/1

Table 24. RAM Address Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Load W from Immediate	LWI i	0 0 1 1 1 1 i_3 i_2 i_1 i_0	i⟶W		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i_3 i_2 i_1 i_0	i⟶X		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i_3 i_2 i_1 i_0	i⟶Y		1/1
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	A⟶X		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	A⟶Y		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	Y+1→Y	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	Y−1→Y	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	Y+A→Y	OVF	1/1
Subtract A from Y	SYY	0 0 1 1 0 1 0 1 0 0	Y−A→Y	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	X↔SPX		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	Y↔SPY		1/1
Exchange X and SPX,Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	X↔SPX,Y↔SPY		1/1

Table 25. RAM Register Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M→A, $\binom{X\leftrightarrow SPX}{Y\leftrightarrow SPY}$		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M→A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M→B, $\binom{X\leftrightarrow SPX}{Y\leftrightarrow SPY}$		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A→M, $\binom{X\leftrightarrow SPX}{Y\leftrightarrow SPY}$		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A→M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A→M,Y+1→Y(X↔SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A→M,Y−1→Y(X↔SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M↔A, $\binom{X\leftrightarrow SPX}{Y\leftrightarrow SPY}$		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M↔A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M↔B, $\binom{X\leftrightarrow SPX}{Y\leftrightarrow SPY}$		1/1

Note) (XY) and (x) have the meaning as follows:

(1) The instructions with (XY) have 4 mnemonics and 4 object codes for each. (example of LAM (XY) is given below.)

MNEMONIC	y	x	FUNCTION
LAM	0	0	
LAMX	0	1	X ↔ SPX
LAMY	1	0	Y ↔ SPY
LAMXY	1	1	X ↔ SPX, Y ↔ SPY

(2) The instructions with (x) have 2 mnemonics and 2 object codes for each. (example of LMAIY(X) is given below.)

MNEMONIC	x	FUNCTION
LMAIY	0	
LMAIYX	1	X ↔ SPX

Table 26. Arithmetic Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD / CYCLE
Add Immediate to A	AI i	1 0 1 0 0 0 i_3 i_2 i_1 i_0	A + i → A	OVF	1 / 1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	B + 1 → B	NZ	1 / 1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	B − 1 → B	NB	1 / 1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1 / 1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1 / 1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\overline{A}$ + 1 → A		1 / 1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\overline{B}$ → B		1 / 1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1 / 1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1 / 1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	1 → CA		1 / 1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	0 → CA		1 / 1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1 / 1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	M + A → A	OVF	1 / 1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M + A → A	OVF	2 / 2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	M + A + CA → A	OVF	1 / 1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M + A + CA → A	OVF	2 / 2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	M − A − $\overline{CA}$ → A	NB	1 / 1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M − A − $\overline{CA}$ → A	NB	2 / 2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	A ∪ B → A		1 / 1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	A ∩ M → A	NZ	1 / 1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ∩ M → A	NZ	2 / 2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	A ∪ M → A	NZ	1 / 1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ∪ M → A	NZ	2 / 2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	A ⊕ M → A	NZ	1 / 1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ⊕ M → A	NZ	2 / 2

Table 27. Compare Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i_3 i_2 i_1 i_0	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i_3 i_2 i_1 i_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	ANEMD d	0 1 0 0 0 0 0 1 0 0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i_3 i_2 i_1 i_0	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i_3 i_2 i_1 i_0	i ≦ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i_3 i_2 i_1 i_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i ≦ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≦ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ≦ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 0 1 0 0	B ≦ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i_3 i_2 i_1 i_0	A ≦ i	NB	1/1

Table 28. RAM Bit Manipulation Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n_1 n_0	1→M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n_1 n_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	1→M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n_1 n_0	0→M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n_1 n_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	0→M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n_1 n_0		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n_1 n_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		M(n)	2/2

Table 29. ROM Address Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Branch on Status 1	BR b	1 1 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p_3 p_2 p_1 p_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p_3 p_2 p_1 p_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a_5 a_4 a_3 a_2 a_1 a_0		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p_3 p_2 p_1 p_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p_3 p_2 p_1 p_0			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1→I/E		1/3

Table 30. Input/Output Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1→D(Y)		1/1
Set Discrete I/O Latch Direct	SEDD m	1 0 1 1 1 0 m_3 m_2 m_1 m_0	1→D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0→D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m_3 m_2 m_1 m_0	0→D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m_3 m_2 m_1 m_0		D(m)	1/1
Load A from R-Port Register	LAR m	1 0 0 1 0 1 m_3 m_2 m_1 m_0	R(m)→A		1/1
Load B from R-Port Register	LBR m	1 0 0 1 0 0 m_3 m_2 m_1 m_0	R(m)→B		1/1
Load R-Port Register from A	LRA m	1 0 1 1 0 1 m_3 m_2 m_1 m_0	A→R(m)		1/1
Load R-Port Register from B	LRB m	1 0 1 1 0 0 m_3 m_2 m_1 m_0	B→R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p_3 p_2 p_1 p_0			1/2

Table 31. Control Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD / CYCLE
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1 / 1
Start Serial	STS	0 1 0 1 0 0 1 0 0 0			1 / 1
Stand-by Mode	SBY	0 1 0 1 0 0 1 1 0 0			1 / 1
Stop Mode	STOP	0 1 0 1 0 0 1 1 0 1			1 / 1

Table 32. Op-Code Map

R9 \ RB, L / H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	NOP	XSPX	XSPY	XSP XY	AN EM			AM				ORM			
	1	RTN	RTNI			ALEM			AMC				EORM			
	2	INEM i(4)														
	3	ILEM i(4)														
	4	LBM(XY)			BNEM				LAB				IB			
	5	LMAIY(X)			AYY				LASPY				IY			
	6	NEGA			RED				LASPX							TC
	7	YNEI i(4)														
	8	XMA(XY)			SEM n(2)				REM n(2)				TM n(2)			
	9	LAM(XY)			LMA(XY)				SMC				ANM			
	A	ROTR	ROTL				DAA				DAS					LAY
	B	TBR p(4)														
	C	XMB(XY)			BLEM				LBA							DB
	D	LMADY(X)			SYY				LYA							DY
	E	TD			SED				LXA				REC			SEC
	F	LWI i(4)														
1	0	LBI i(4)														
	1	LYI i(4)														
	2	LXI i(4)														
	3	LAI i(4)														
	4	LBR m(4)														
	5	LAR m(4)														
	6	REDD m(4)														
	7	LAMR m(4)														
	8	AI i(4)														
	9	LMIIY i(4)														
	A	TDD m(4)														
	B	ALEI i(4)														
	C	LRB m(4)														
	D	LRA m(4)														
	E	SEDD m(4)														
	F	XMRA m(4)														

R9 \ RB, L / H	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0				ANEMD				AMD				ORMD			
				ALEMD				AMCD				EORMD			
	INEMD i(4)														
	ILEMD i(4)														
	COMB			OR				STS				SBY	STOP		
	JMPL p(4)														
	CALL p(4)														
	BRL p(4)														
	XMAD			SEMD n(2)				REMD n(2)				TMD n(2)			
	LAMD			LMAD				SMCD				ANMD			
	LMID i(4)														
	P p(4)														
	CAL a(6)														
1	BR b(8)														

... 1-word/2-cycle Instruction

... 1-word/3-cycle Instruction

... RAM Direct Address Instruction (2-word/2-cycle)

... 2-word/2-cycle Instruction

■ MASK OPTION LIST

- Family Name ■ HMCS404C
- Package □ DP-64S □ FP-64
- I/O Circuit Type A; Without Pull-up MOS (NMOS Open Drain)
  B; With Pull-up MOS
  C; CMOS
  D; Without Pull-down MOS (PMOS Open Drain)
  E; With Pull-down MOS

Date of Order	
Customer	
Dept.	
Name	
ROM Code Name	
LSI Type Number (Hitachi's entry)	

PIN			INPUT/OUTPUT	I/O OPTION A	B	C	D	E
D_0		Standard Pins	Input/Output					
D_1			Input/Output					
D_2			Input/Output					
D_3			Input/Output					
D_4		High Voltage Pins	Input/Output					
D_5			Input/Output					
D_6			Input/Output					
D_7			Input/Output					
D_8			Input/Output					
D_9			Input/Output					
D_{10}			Input/Output					
D_{11}			Input/Output					
D_{12}			Input/Output					
D_{13}			Input/Output					
D_{14}			Input/Output					
D_{15}			Input/Output					
R0	R_{00}		Output					
	R_{01}		Output					
	R_{02}		Output					
	R_{03}		Output					
R1	R_{10}		Input/Output					
	R_{11}		Input/Output					
	R_{12}		Input/Output					
	R_{13}		Input/Output					
R2	R_{20}		Input/Output					
	R_{21}		Input/Output					
	R_{22}		Input/Output					
	R_{23}		Input/Output					

PIN			INPUT/OUTPUT	I/O OPTION A	B	C	D	E
R3	R_{30}	Standard Pins	Input/Output					
	R_{31}		Input/Output					
	R_{32}		Input/Output					
	R_{33}		Input/Output					
R4	R_{40}		Input/Output					
	R_{41}		Input/Output					
	R_{42}		Input/Output					
	R_{43}		Input/Output					
R5	R_{50}		Input/Output					
	R_{51}		Input/Output					
	R_{52}		Input/Output					
	R_{53}		Input/Output					
R6	R_{60}		Output					
	R_{61}		Output					
	R_{62}		Output					
	R_{63}		Output					
R7	R_{70}		Output					
	R_{71}		Output					
	R_{72}		Output					
	R_{73}		Output					
R8	R_{80}		Output					
	R_{81}		Output					
	R_{82}		Output					
	R_{83}		Output					
R9	R_{90}		Input					
	R_{91}		Input					
	R_{92}		Input					
	R_{93}		Input					
RA	R_{A0}	High Voltage Pins	Input					
	R_{A1}		Input	Please Mark on R_{A1}/V_{disp}				

- R_{A1}/V_{disp} (RA1) □ R_{A1}: Without Pull-down MOS (D) □ V_{disp} (VDISP)
- Oscillator (OSC) □ Crystal or Ceramic Filter Oscillator (XTAL) □ Resistor Oscillator (RF)
- Divider (DIV) ■ Divide-by-8 (D-8)
- ROM Code Media □ EPROM: Emulator Type □ EPROM: EPROM On-Package Microcomputer Type

Note 1) I/O Options masked by ▨ are not available.
Note 2) R_{A1}/V_{disp} has to be selected as V_{disp} pin exept the case that all High Voltage Pins are option D.

HD614P080S

The HD614P080S is a 4-bit single chip microcomputer which has mounted a standard EPROM 2764/27128 for program memory.

The HD614P080S is pin-compatible with the mask ROM type HMCS404C/404AC, but has some differences with them as shown in Table 33. By modifying the program in the EPROM, it can be used for the evaluation of the HMCS404C/404AC, or for small-scale production.

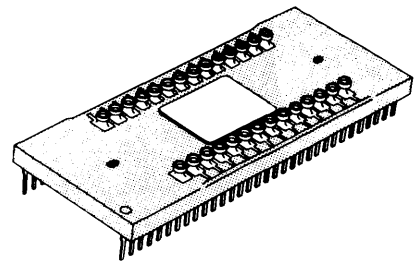
■ HARDWARE FEATURES

- 4-bit Architecture
- Applicable to 4k or 8k words x 10 bits of EPROM
  4096 words x 10 bits HN482764, HN27C64
  8192 words x 10 bits HN4827128
- Data Memory (RAM) Capacity . . . . . .576 digits x 4 bits
- 58 I/O Pins – 26 I/O pins are high voltage up to 40V (max).
- 2 Timer/Counters
  11-bit Prescaler
  8-bit Free Running Counter
  8-bit Auto-reload Timer/Event Counter
- Clocked Synchronous 8-bit Serial Interface
- 5 Interrupts
  External 2
  Timer/Counter 2
  Serial Interface 1
- Subroutine Stack
  Up to 16 levels including interrupts
- Minimum Instruction Execution Time; 1.33 μs
- 2 Low Power Modes
  Standby – Stops instruction execution while keeping clock generator and interrupt functions included Timer/Counter and Serial Interface in operation
  Stop – Stops instruction execution and clock generation while retaining RAM data
- Clock Generator
  External Connection of Crystal Resonator or Ceramic Filter Resonator (externally drivable)
- Power Voltage Range; 5V ± 10%
- I/O Pin Circuit Form
  All standard pins are "without pull-up MOS".
  All high voltage pins are "without pull-down MOS".
- Shrink Type 64 Pin EPROM On-package

■ SOFTWARE FEATURES

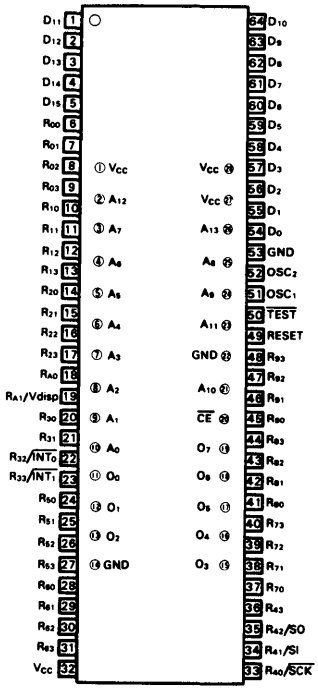
- Software Compatible with HMCS404C/404AC
- Instruction Set Similar to and More Powerful than HMCS40 Series; 99 Instructions
- High Programming Efficiency with 10-bit ROM/Word; 79 instructions are single word instructions.
- Direct Branch to All ROM Area
- Direct or Indirect Addressing to All RAM Area
- Subroutine Nesting Up to 16 Levels Including Interrupts

HD614P080S



(DC-64SP)

■ PIN ARRANGEMENT



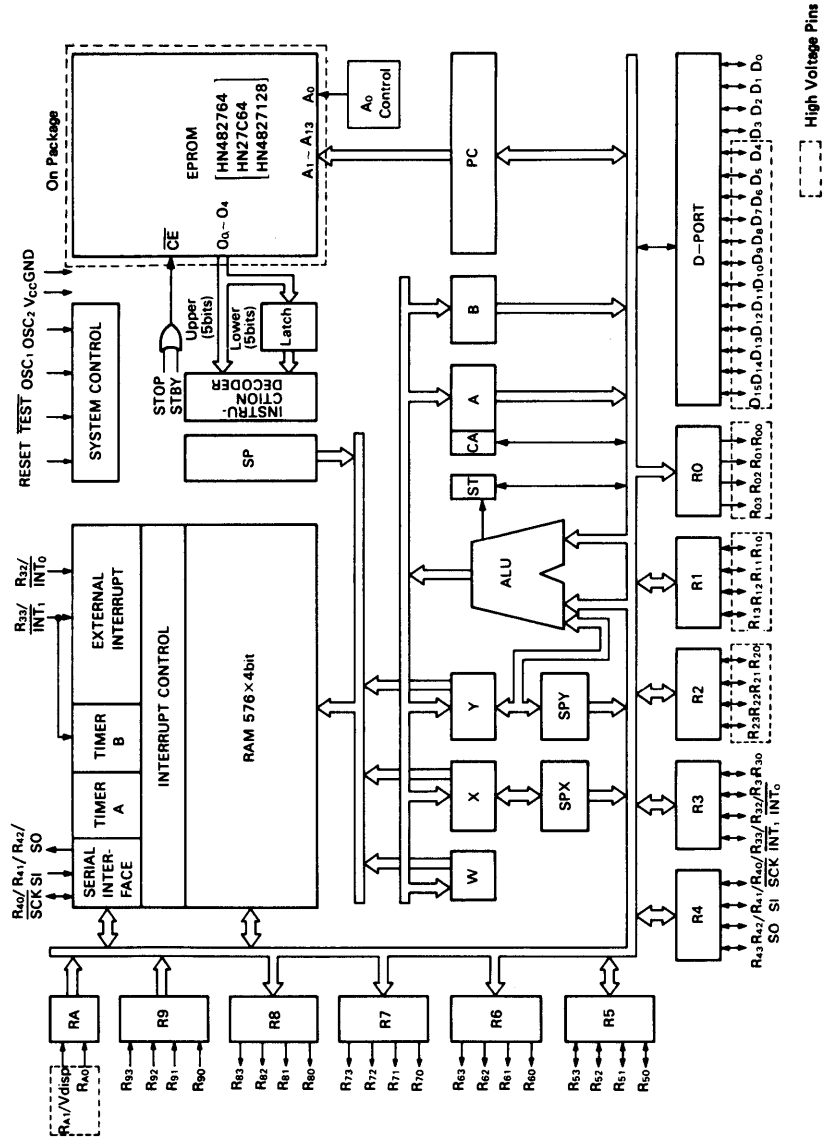
(Top View)

- Binary and BCD Arithmetic Operation
- Powerful Logic Arithmetic Operation
- Pattern Generation – Table Look Up Capability –
- Bit Manipulation for Both RAM and I/O

■ VERSATILE PROGRAM DEVELOPMENT SUPPORT TOOLS

- H68SD Series Macro Assembler
- H68SD5-use Emulator (With Real Time Trace Function)

■ **BLOCK DIAGRAM**



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	−0.3 to +7.0	V	
Pin Voltage	V_T	−0.3 to V_{CC} +0.3	V	3
		V_{CC} −45 to V_{CC} +0.3	V	4
Total Allowance of Input Currents	ΣI_O	50	mA	5
Total Allowance of Output Currents	$-\Sigma I_O$	150	mA	6
Maximum Input Current	I_O	15	mA	7, 8
Maximum Output Current	$-I_O$	4	mA	9, 10
		6	mA	9, 11
		30	mA	9, 12
Operating Temperature	T_{opr}	−20 to +75	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

(Note 1) Permanent damage may occur if "Absolute Maximum Ratings"of the LSI or the EPROM are exceeded. Normal operation should be under the conditions of "Electrical Characteristics". If these conditions are exceeded, it may cause the malfunction and affect the reliability of LSI.
(Note 2) All voltages are with respect to GND.
(Note 3) Applied to standard pins.
(Note 4) Applied to high voltage I/O pins.
(Note 5) Total allowance of input current is the total sum of input current which flow in from all I/O pins to GND simultaneously.
(Note 6) Total allowance of output current is the total sum of the output current which flow out from V_{CC} to all I/O pins simultaneously.
(Note 7) Maximum input current is the maximum amount of input current from each I/O pin to GND.
(Note 8) Applied to $D_0 \sim D_3$ and R3 ~ R8.
(Note 9) Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
(Note 10) Applied to $D_0 \sim D_3$ and R3 ~ R8.
(Note 11) Applied to R0 ~ R2.
(Note 12) Applied to $D_4 \sim D_{15}$.

■ RECOMMENDED APPLICABLE EPROM

Type No.	Program Memory Capacity	f_{osc} (MHz)	EPROM Type No.
HD614P080S	4096 words	4	HN27C64-30 HN482764-3
		6	HN27C64-25 HN482764
	8192 words	4	HN4827128-45
		6	HN4827128-25

■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS (V_{CC} = 4.5V to 5.5V, GND = 0V, Ta = -20 to +75°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value min	Value typ	Value max	Unit	Note
Input "High" Voltage	V_{IH}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$		0.7V_{CC}	–	V_{CC}+0.3	V	
		SI		0.7V_{CC}	–	V_{CC}+0.3	V	
		OSC_1		V_{CC}-0.5	–	V_{CC}+0.3	V	
Input "Low" Voltage	V_{IL}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$		-0.3	–	0.22V_{CC}	V	
		SI		-0.3	–	0.22V_{CC}	V	
		OSC_1		-0.3	–	0.5	V	
Output "High" Voltage	V_{OH}	$\overline{SCK}$, SO	$-I_{OH}$ = 1.0 mA	V_{CC}-1.0	–	–	V	
			$-I_{OH}$ = 0.01 mA	V_{CC}-0.3	–	–	V	
Output "Low" Voltage	V_{OL}	$\overline{SCK}$, SO	I_{OL} = 1.6 mA	–	–	0.4	V	
Input/Output Leakage Current	$\|I_{IL}\|$	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$, SI, SO, OSC_1	V_{in} = 0V to V_{CC}	–	–	1	μA	1
Current Dissipation in Operation Mode	I_{CC}	V_{CC}	V_{CC} = 5V, Crystal or Ceramic Filter Resonator f_{osc} = 4MHz	–	–	2.0	mA	2, 5
Current Dissipation in Standby Mode	I_{SBY1}	V_{CC}	Maximum Logic Operation V_{CC} = 5V, Crystal or Ceramic Filter Resonator f_{osc} = 4MHz	–	–	1.2	mA	3, 5
	I_{SBY2}	V_{CC}	Minimum Logic Operation V_{CC} = 5V, Crystal or Ceramic Filter Resonator f_{osc} = 4MHz	–	–	0.9	mA	4, 5
Current Dissipation in Stop Mode	I_{stop}	V_{CC}	V_{in} ($\overline{TEST}$) = V_{CC} ~ V_{CC}-0.3V, V_{in} (RESET) = 0 ~ 0.3V	–	–	10	μA	
Stop Mode Retain Voltage	V_{stop}	V_{CC}		2.0	–	–	V	

(Note 1) Output buffer current are excluded.

(Note 2) The MCU is in the reset state. The input/output current does not flow.
Test Conditions: MCU state; • Reset state in Operation Mode
Pin state; • RESET, $\overline{TEST}$ – V_{CC} voltage
• D_0~D_3, R3~R9 – V_{CC} voltage
• D_4~D_{15}, R0~R2, R_{A0}, R_{A1} – V_{CC} ~V_{CC}-40V

(Note 3) The timer/counter with the fastest clock and input/output current does not flow.
Test Conditions: MCU state; • Standby Mode
• Input/Output; Reset state
• TIMER-A; ÷2 prescaler divide ratio
• TIMER-B; ÷2 prescaler divide ratio
• SERIAL; Stop
Pin state; • RESET – GND voltage
• $\overline{TEST}$ – V_{CC} voltage
• D_0~D_3, R3~R9 – V_{CC} voltage
• D_4~D_{15}, R0~R2, R_{A0}, R_{A1} – V_{CC} ~ V_{CC}-40V

(Note 4) The timer/counter with the slowest clock and input/output current does not flow.
Test Conditions: MCU state; • Standby Mode
• Input/Output; Reset state
• TIMER-A; ÷2048 prescaler divide ratio
• TIMER-B; ÷2048 prescaler divide ratio
• SERIAL; Stop

Pin state;
- $\overline{RESET}$ – GND voltage
- $\overline{TEST}$ – V_{CC} voltage
- $D_0 \sim D_3$, R3 ~ R9 – V_{CC} voltage
- $D_4 \sim D_{15}$, R0 ~ R2, R_{A0}, R_{A1} – $V_{CC} \sim V_{CC}$-40V

(Note 5) The consumption of current in operation and standby mode is proportional to f_{osc}. When $f_{osc} = x$ [MHz], the value of each current is calculated as follows.

max. value ($f_{osc} = x$) = $\frac{x}{4}$ x max. value (f_{osc} = 4 [MHz]).

• INPUT/OUTPUT CHARACTERISTICS FOR STANDARD PIN

(V_{CC} = 4.5V to 5.5V, GND = 0V, Ta = -20 to +75°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	$D_0 \sim D_3$, R3 ~ R5, R9		0.7V_{CC}	–	V_{CC}+0.3	V	
Input "Low" Voltage	V_{IL}	$D_0 \sim D_3$, R3 ~ R5, R9		–0.3	–	0.22V_{CC}	V	
Output "Low" Voltage	V_{OL}	$D_0 \sim D_3$, R3 ~ R8	I_{OL} = 1.6 mA	–	–	0.4	V	
Input/Output Leakage Current	$\lvert I_{IL} \rvert$	$D_0 \sim D_3$, R3 ~ R9	V_{in} = 0V–V_{CC}	–	–	1	μA	1

(Note 1) Output buffer current are excluded.

• INPUT/OUTPUT CHARACTERISTICS FOR HIGH VOLTAGE PIN

(V_{CC} = 4.5V to 5.5V, GND = 0V, Ta = -20 to +75°C, if not specified.)

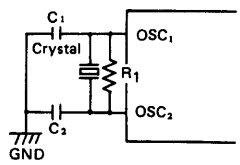
Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	$D_4 \sim D_{15}$, R1 R2, R_{A0}, R_{A1}		0.7V_{CC}	–	V_{CC}+0.3	V	
Input "Low" Voltage	V_{IL}	$D_4 \sim D_{15}$, R1 R2, R_{A0}, R_{A1}		V_{CC}-40	–	0.22V_{CC}	V	
Output "High" Voltage	V_{OH}	$D_4 \sim D_{15}$	$-I_{OH}$ = 15mA	V_{CC}-3.0	–	–	V	
			$-I_{OH}$ = 9mA	V_{CC}-2.0				
		R0 ~ R2	$-I_{OH}$ = 3mA	V_{CC}-3.0	–	–	V	
			$-I_{OH}$ = 1.8 mA	V_{CC}-2.0				
Output "Low" Voltage	V_{OL}	$D_4 \sim D_{15}$ R0 ~ R2	150kΩ to V_{CC}-40V	–	–	V_{CC}-37	V	
Input/Output Leakage Current	$\lvert I_{IL} \rvert$	$D_4 \sim D_{15}$ R0 ~ R2 R_{A0}, R_{A1}	V_{in} = V_{CC}-40V to V_{CC}	–	–	20	μA	1

(Note 1) Output buffer current are excluded.

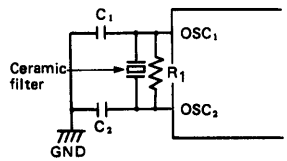
• AC CHARACTERISTICS (V_{CC} = 4.5V to 5.5V, GND = 0V, Ta= -20 to +75°C, if not specified.)

	Item	Symbol	Pin Name	Test Conditions	Value min	Value typ	Value max	Unit	Note
Crystal Resonator	Oscillation Frequency	f_{osc}	OSC_1, OSC_2		0.4	–	6.2	MHz	
	Instruction Cycle Time	t_{cyc}			1.29	–	20	μs	
	Oscillator Stabilization Time	t_{RC}	OSC_1, OSC_2		–	–	20	ms	1
Ceramic Filter Resonator	Oscillation Frequency	f_{osc}	OSC_1, OSC_2		0.4	–	6.2	MHz	
	Instruction Cycle Time	t_{cyc}			1.29	–	20	μs	
	Oscillator Stabilization Time	t_{RC}	OSC_1, OSC_2		–	–	20	ms	1
External Clock	External Clock Frequency	f_{CP}	OSC_1		0.4	–	6.2	MHz	2
	External Clock "High" Level Width	t_{CPH}	OSC_1		70	–	–	ns	2
	External Clock "Low" Level Width	t_{CPL}	OSC_1		70	–	–	ns	2
	External Clock Rise Time	t_{CPr}	OSC_1		–	–	20	ns	2
	External Clock Fall Time	t_{CPf}	OSC_1		–	–	20	ns	2
	Instruction Cycle Time	t_{cyc}			1.29	–	20	μs	2
$\overline{INT_0}$ "High" Level Width		t_{I0H}	$\overline{INT_0}$		2	–	–	t_{cyc}	3
$\overline{INT_0}$ "Low" Level Width		t_{I0L}	$\overline{INT_0}$		2	–	–	t_{cyc}	3
$\overline{INT_1}$ "High" Level Width		t_{I1H}	$\overline{INT_1}$		2	–	–	t_{cyc}	3
$\overline{INT_1}$ "Low" Level Width		t_{I1L}	$\overline{INT_1}$		2	–	–	t_{cyc}	3
RESET "High" Level Width		t_{RSTH}	RESET		2	–	–	t_{cyc}	4
Input Capacitance		C_{in}	all pins	f=1MHz V_{in} = 0V	–	–	15	pF	
Reset Fall Time		t_{RSTf}			–	–	20	ms	4

(Note 1) Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 4.5V at "Power-on", or after RESET input level goes to "High" by resetting to quit the stop mode by MCU reset on the circuits below. When using crystal or ceramic filter oscillator, please ask a crystal oscillator maker's or ceramic filter maker's advice because oscillator stabilization time depends on the circuit constant and stray capacity.

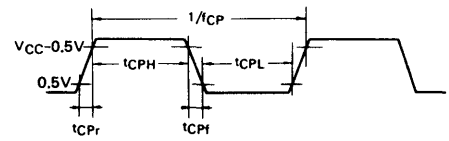


Crystal: 6.0 [MHz]
NC-18C (Nihon Denpa Kogyo)
R_f = 1 [MΩ] ± 2%, C_1 = C_2 = 20 [pF] ±20%

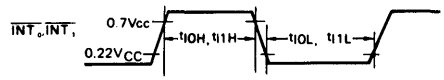


Ceramic filter: CSA6.00MG (Murata)
R_f = 1 [MΩ] ±2%, C_1 = C_2 = 30 [pF] ± 20%

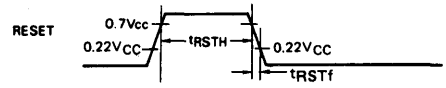
(Note 2)



(Note 3)



(Note 4)



• SERIAL INTERFACE TIMING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, GND = 0V, Ta = -20 to +75°C, if not specified.)

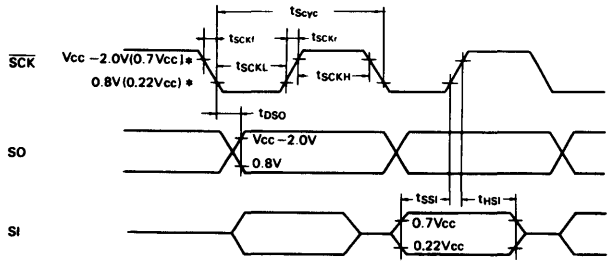
• At Transfer Clock Output

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$	(Note 2)	1	–	–	t_{cyc}	1, 2
Transfer Clock "High" Level Width	t_{SCKH}	$\overline{SCK}$	(Note 2)	0.5	–	–	t_{Scyc}	1, 2
Transfer Clock "Low" Level Width	t_{SCKL}	$\overline{SCK}$	(Note 2)	0.5	–	–	t_{Scyc}	1, 2
Transfer Clock Rise Time	t_{SCKr}	$\overline{SCK}$	(Note 2)	–	–	100	ns	1, 2
Transfer Clock Fall Time	t_{SCKf}	$\overline{SCK}$	(Note 2)	–	–	100	ns	1, 2
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	–	–	250	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		300	–	–	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		150	–	–	ns	1

• At Transfer Clock Input

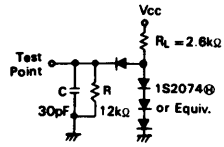
Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$		1	–	–	t_{cyc}	1
Transfer Clock "High" Level Width	t_{SCKH}	$\overline{SCK}$		0.5	–	–	t_{Scyc}	1
Transfer Clock "Low" Level Width	t_{SCKL}	$\overline{SCK}$		0.5	–	–	t_{Scyc}	1
Transfer Clock Rise Time	t_{SCKr}	$\overline{SCK}$		–	–	100	ns	1
Transfer Clock Fall Time	t_{SCKf}	$\overline{SCK}$		–	–	100	ns	1
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	–	–	250	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		300	–	–	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		150	–	–	ns	1

(Note 1) Timing Diagram of Serial Interface

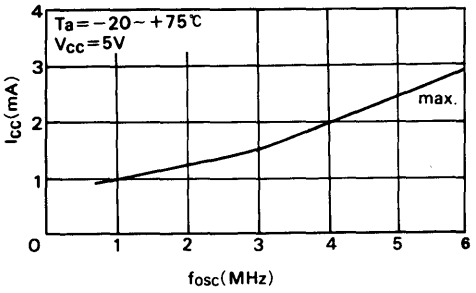


* V_{CC}-2.0V and 0.8V are the threshold voltage for transfer clock output.
0.7V_{CC} and 0.22 V_{CC} are the threshold voltage for transfer clock input.

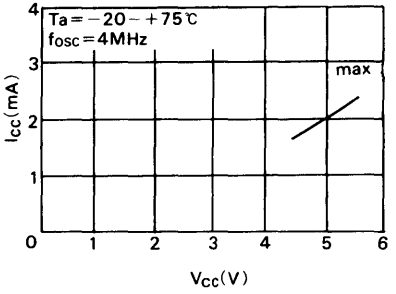
(Note 2) Timing Load Circuit



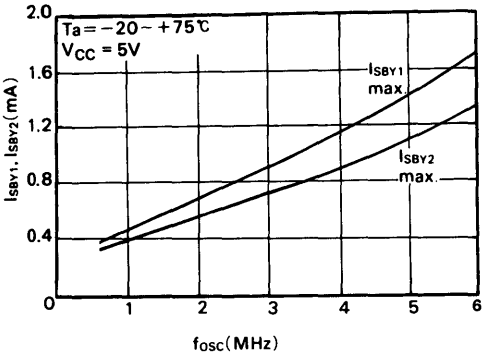
■ CHARACTERISTICS CURVE (REFERENCE DATA)



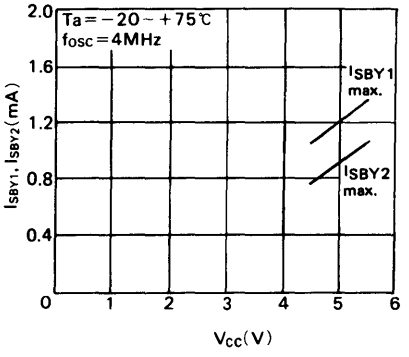
I_{CC} vs. f_{osc} characteristic
(crystal, ceramic resonator)



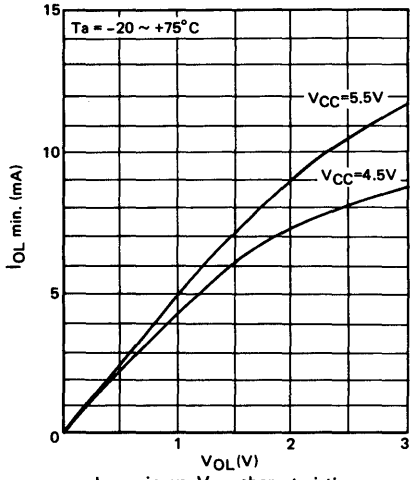
I_{CC} vs. V_{CC} characteristic
(crystal, ceramic resonator)



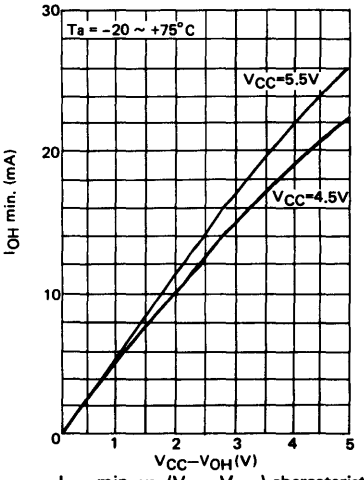
I_{SBY} vs. f_{osc} characteristics
(crystal, ceramic resonator)



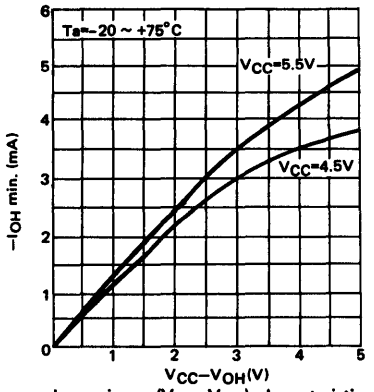
I_{SBY} vs. V_{CC} characteristics
(crystal, ceramic resonator)



I_{OL} min. vs. V_{OL} characteristics
(Standard Pin)



$-I_{OH}$ min. vs. ($V_{CC}-V_{OH}$) characteristics
(D_4 ~ D_{15} pins)



$-I_{OH}$ min. vs. ($V_{CC}-V_{OH}$) characteristics (R0 ~ R2 pins)

■ DESCRIPTION OF PIN FUNCTIONS

Input and output signals of MCU are described below.

• GND, V_{CC}, V_{disp}

These are power supply pins. Connect GND pin to Earth (0V) and apply V_{CC} power supply voltage to V_{CC} pin. R_{A1}/V_{disp} pins are used for R_{A1} as all high voltage pins are "without pull-down MOS" (PMOS open drain).

• $\overline{TEST}$

$\overline{TEST}$ pin is not for users application. Connect it to V_{CC}.

• RESET

RESET pin is used to reset MCU. For details, see "RESET".

• OSC_1, OSC_2

These are input pins to the internal clock generator circuit. They can be connected to crystal resonator, ceramic filter resonator, or external oscillator circuit. For details, see "INTERNAL OSCILLATOR CIRCUIT."

• D-port (D_0 to D_{15})

D-port is a 1-bit Input/Output common port. D_0 to D_3 are standard type, D_4 to D_{15} are for high voltage. For details, see "INPUT/OUTPUT".

• R-port (R0 to RA)

R-port is a 4-bit Input/Output port. (only RA is 2-bit construction.) R0 and R6 to R8 are output ports, R9 to RA are input ports, and R1 to R5 are Input/Output common ports. R0 to R2 and RA are the high voltage ports, R3 to R9 are the standard ports. R_{32}, R_{33}, R_{40}, R_{41}, and R_{42} are also available as $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK}$, SI and SO respectively. For details, see "INPUT/OUTPUT".

• $\overline{INT_0}$, $\overline{INT_1}$

These are the input pins to interrupt MCU operation externally. $\overline{INT_1}$ can be used as an external event input pin for TIMER-B. $\overline{INT_0}$ and $\overline{INT_1}$ are also available as R_{32}, and R_{33} respectively. For details, see "INTERRUPT".

• $\overline{SCK}$, SI, SO

These are transfer clock I/O pin ($\overline{SCK}$), serial data input pin (SI) and serial data output pin (SO) used for serial interface. $\overline{SCK}$, SI and SO are also available as R_{40}, R_{41}, and R_{42} respectively. For details, see "SERIAL INTERFACE".

■ ROM MEMORY MAP

ROM memory map is illustrated in Fig. 1 and described in the following paragraph.

• Vector Address Area ..... $0000 to $000F

When MCU reset or an interrupt is serviced, the program is executed from the vector address. Program the JMPL instructions branching to the starting addresses of reset routine or of interrupt routines.

• Zero-Page Subroutine Area ..... $0000 to $003F

CAL instruction allows to branch to the subroutines in $0000 to $003F.

• Pattern Area ..... $0000 to $0FFF

P instruction allows referring to the ROM data in $0000 to $0FFF as a pattern.

• Program Area ..... $0000 to $1FFF

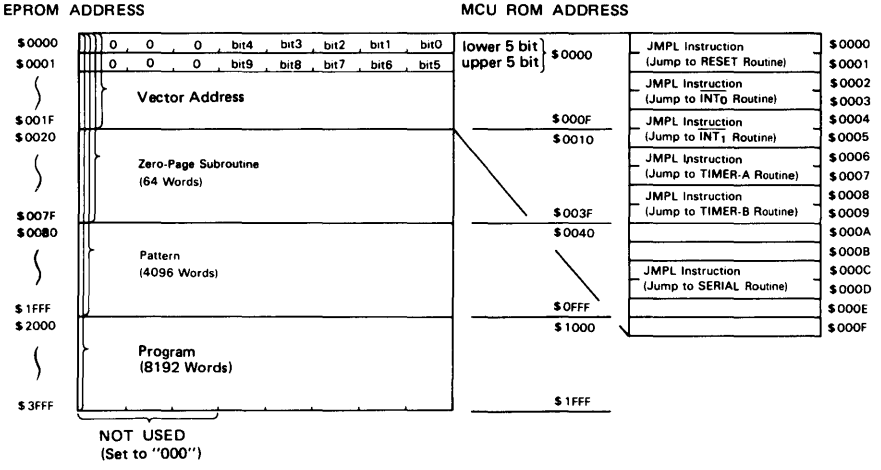


Fig. 1 ROM Memory Map

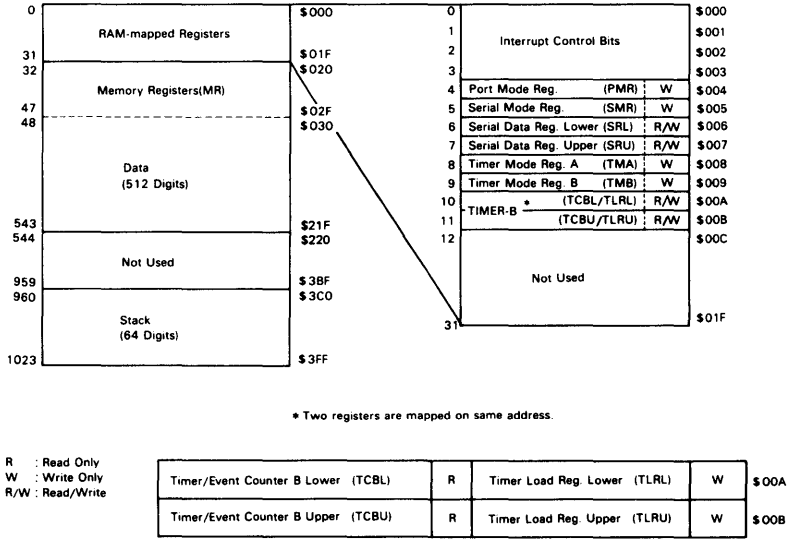


Fig. 2 RAM Memory Map

■ RAM MEMORY MAP

The MCU includes 576 digits x 4 bits RAM as the data area and stack area. In addition to these areas, interrupt control bits and special registers are also mapped on the RAM memory space. RAM memory map is illustrated in Fig. 2 and described in the following paragraph.

	bit 3	bit 2	bit 1	bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP Bit)	I/E (Interrupt Enable Flag)	$000
1	IMTA (IM of TIMER-A)	IFTA (IF of TIMER-A)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	Not Used	Not Used	IMTB (IM of TIMER-B)	IFTB (IF of TIMER-B)	$002
3	Not Used	Not Used	IMS (IM of SERIAL)	IFS (IF of SERIAL)	$003

IF : Interrupt Request Flag
IM : Interrupt Mask
I/E : Interrupt Enable Flag
SP : Stack Pointer
(Note) Each bit in Interrupt Control Bits Area is set by SEM/SEMD instruction, is reset by REM/REMD instruction and is tested by TM/TMD instruction. It is not affected by other instructions. Furthermore, Interrupt Request Flag is not affected by SEM/SEMD instruction. The content of Status becomes invarid when "RSP" bit and "Not Used" bit is tested.

Fig. 3 Configuration of Interrupt Control Bit Area

- **Interrupt Control Bit Area ..... $000 to $003**

This area is used for interrupt controls, and is illustrated in Fig. 3. It is accessable only by RAM bit manipulation instruction. However, the interrupt request flag cannot be set by software. The RSP bit is only used to reset the SP.

- **Special Register Area ..... $004 to $00B**

Special Register is a mode or a data register for the external interrupt, the serial interface, and the timer/counter. These registers are classified into 3 types: Write-only, Read-only, and Read/Write as shown in Fig. 2. These registers cannot be accessed by RAM bit manipulation instruction.

- **Data Area ..... $020 to $21F**

16 digits of $020 to $02F are called memory register (MR) and accessable by LAMR and XMRA instructions.

- **Stack Area .... $3C0 to $3FF**

Stack Area is used for LIFO stacks with the contents of the program counter (PC), status (ST) and carry (CA) when processing subroutine call and interrupt. As 1 level requires 4 digits, this stack area is nested to 16 level-stack max. The data pushed in the stack and LIFO stack state are provided in Fig. 4. The program counter is restored by RTN and RTNI instructions. Status and Carry are restored only by RTNI instruction, and not affected by RTN instruction. The area, not used for stacking, is available as a data area.

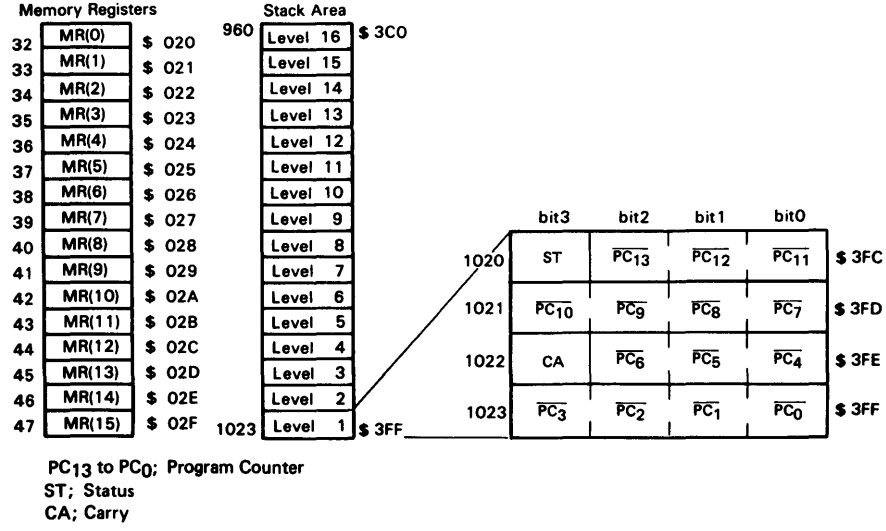


Fig. 4 Configuration of Memory Register, Stack Area and Stack Position

■ REGISTER AND FLAG

The MCU has nine registers and two flags for the CPU operations. They are illustrated in Fig. 5 and described in the following paragraphs.

• Accumulator (A), B Register (B)

Accumulator and B Register are 4-bit registers used to hold the results of Arithmetic Logic Unit (ALU), and to transfer data to/from memories, I/O and other registers.

• W Register (W), X Register (X), Y Register (Y)

W Register is 2-bit, and X and Y Register are 4-bit registers used for indirect addressing of RAM. Y register is also used for D-port addressing.

• SPX Register (SPX), SPY Register (SPY)

SPX and SPY Register are 4-bit registers used to assist X and Y Register respectively.

• Carry (CA)

Carry (CA) stores the overflow of ALU generated by the arithmetic operation. It is also affected by SEC, REC, ROTL and ROTR instructions.

During interrupt servicing, Carry is pushed onto the stack and restored back from the stack by RTNI instruction. (It's not affected by RTN instruction.)

• Status (ST)

Status (ST) holds the ALU overflow, ALU non-zero and the results of bit test instruction for the arithmetic or compare instruction. It is used for a branch condition of BR, BRL, CAL or CALL instructions. The value of the Status remains unchanged until the next arithmetic, compare or bit test instruction is executed. Status becomes "1" after the BR, BRL, CAL or CALL instruction has been executed (irrespective of its execution/skip). During the interrupt servicing, Status is pushed onto the stack and restored back from the stack by RTNI instruction. (It's not affected by RTN instruction.)

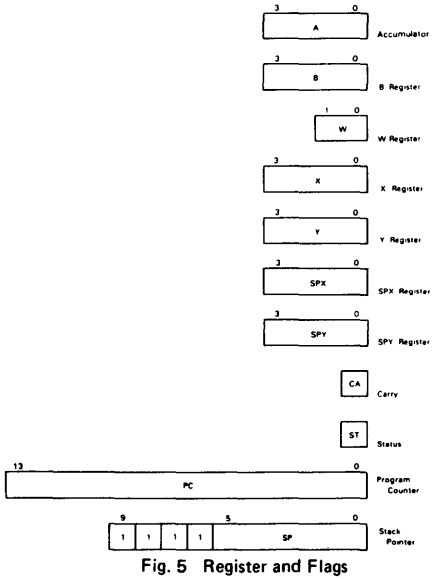


Fig. 5 Register and Flags

• Program Counter (PC)

Program Counter is a 14-bit binary counter for ROM addressing.

• Stack Pointer (SP)

Stack Pointer is used to point the address of the next stacking area up to 16 levels.

The Stack Pointer is initialized to locate $3FF on the RAM address, and is decremented by 4 as data pushed into the stack, and incremented by 4 as data restored back from the stack.

■ INTERRUPT

The MCU can be interrupted by five different sources: the external signals ($\overline{INT_0}$, $\overline{INT_1}$), timer/counter (TIMER-A, TIMER-B), and serial interface (SERIAL). In each sources, the Interrupt Request Flag, Interrupt Mask and interrupt vector address will be used to control and maintain the interrupt request. The Interrupt Enable Flag is also used to control the total interrupt operations.

• Interrupt Control Bit and Interrupt Service

The interrupt control bit is mapped on $000 to $003 of the RAM address and accessable by RAM bit manipulation instruction. (The Interrupt Request Flag (IF) cannot be set by software.) The Interrupt Enable Flag (I/E) and Interrupt Request Flag (IF) are set to "0", and the Interrupt Mask (IM) is set to "1" at the initialization by MCU reset.

Fig. 6 shows the interrupt block diagram. Table 1 shows the interrupt priority and vector addresses, and Table 2 shows the conditions that the interrupt service is executed by any one of the five interrupt sources.

The interrupt request is generated when the Interrupt Request Flag is set to "1" and the Interrupt Mask is "0". If the Interrupt Enable Flag is "1", then the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the five interrupt sources.

Fig. 7 shows the interrupt services sequence, and Fig. 8 shows the interrupt flowchart. If the interrupt is requested, the instruction finishes its execution in the first cycle. The Interrupt Enable Flag is reset in the second cycle. In the second and third cycles, the Carry, Status and Program Counter are pushed onto the stack. In the third cycle, the instruction is executed again after jumping to the vector address.

In each vector address, program JMPL instruction to branch to a starting address of the interrupt routine. The Interrupt Request Flag which caused the interrupt service has to be reset by software in the interrupt routine.

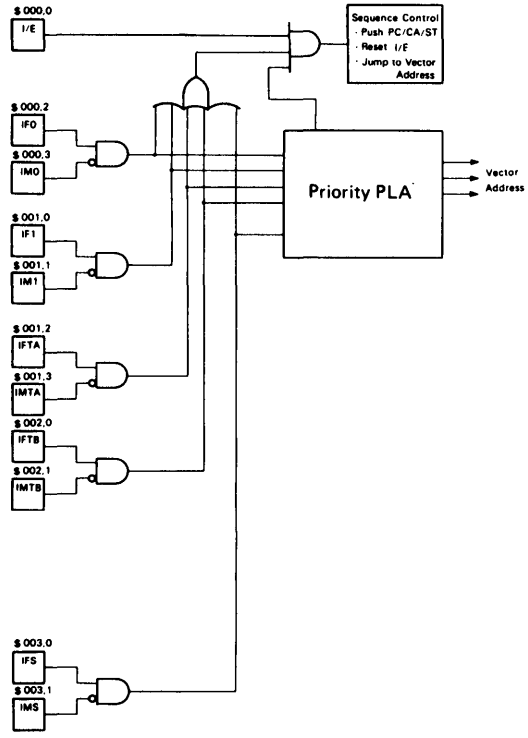


Fig. 6 Interrupt Circuit Block Diagram

Table 1. Vector Addresses and Interrupt Priority

Reset , Interrupt	Priority	Vector addresses
RESET	–	$0000
$\overline{INT_0}$	1	$0002
$\overline{INT_1}$	2	$0004
TIMER-A	3	$0006
TIMER-B	4	$0008
SERIAL	5	$000C

Table 2. Conditions of Interrupt Service

Interrupt source / Interrupt control bits	$\overline{INT_0}$	$\overline{INT_1}$	TIMER-A	TIMER-B	SERIAL
I/E	1	1	1	1	1
IF0·$\overline{IM0}$	1	0	0	0	0
IF1 · $\overline{IM1}$	*	1	0	0	0
IFTA · $\overline{IMTA}$	*	*	1	0	0
IFTB · $\overline{IMTB}$	*	*	*	1	0
IFS · $\overline{IMS}$	*	*	*	*	1

* Don't care

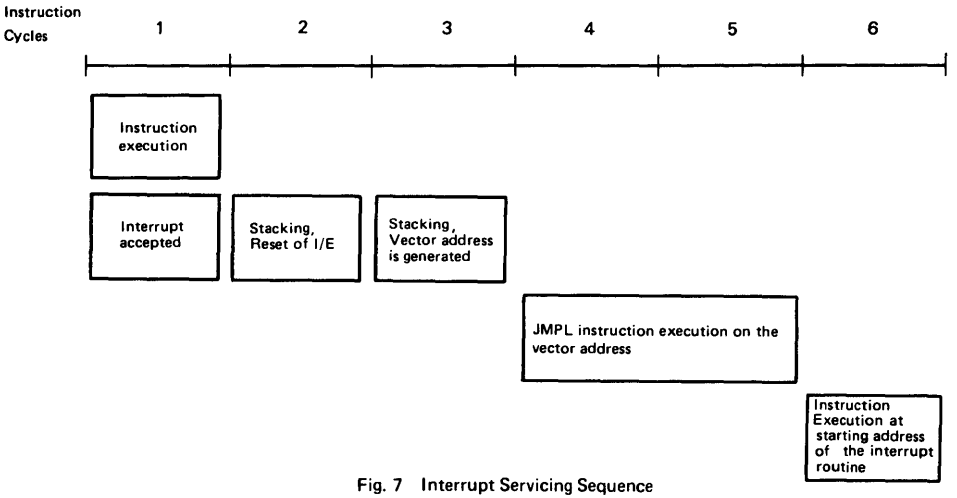


Fig. 7 Interrupt Servicing Sequence

- **Interrupt Enable Flag (I/E: $000,0)**

The Interrupt Enable Flag controls enable/disable of all interrupt requests as shown in Table 3. The Interrupt Enable Flag is reset by the interrupt servicing and set by RTNI instruction.

Table 3. Interrupt Enable Flag

Interrupt Enable Flag	Interrupt Enable/Disable
0	Disable
1	Enable

- **External Interrupt ($\overline{INT_0}$, $\overline{INT_1}$)**

To use external interrupt, select $R_{32}/\overline{INT_0}$, $R_{33}/\overline{INT_1}$ port for $\overline{INT_0}$, $\overline{INT_1}$ mode by setting the Port Mode Register (PMR: $004).

The External Interrupt Request Flags (IF0, IF1) are set at the falling edge of $\overline{INT_0}$, $\overline{INT_1}$ inputs.

$\overline{INT_1}$ input can be used as a clock signal input of TIMER-B. Then, TIMER-B counts up at each falling edge of input. When using $\overline{INT_1}$ as TIMER-B external event, an External Interrupt Mask (IM1) has to be set so that the interrupt request by $\overline{INT_1}$ will not be accepted.

- **External Interrupt Request Flag (IF0: $000,2, IF1: $001,0)**

The External Interrupt Request Flags (IF0, IF1) are set at the falling edges of $\overline{INT_0}$, $\overline{INT_1}$ inputs respectively.

- **External Interrupt Mask (IM0: $000,3, IM1: $001,1)**

The External Interrupt Mask is used to mask the external interrupt requests.

Table 4. External Interrupt Request Flag

External Interrupt Request Flags	Interrupt Requests
0	No
1	Yes

Table 5. External Interrupt Mask

External Interrupt Masks	Interrupt Requests
0	Enable
1	Disable (masks)

- **Port Mode Register (PMR: $004)**

The Port Mode Register is a 4-bit write-only register which controls the $R_{32}/\overline{INT_0}$ pin, $R_{33}/\overline{INT_1}$ pin, R_{41}/SI pin and R_{42}/SO pin as shown in Table 6. The Port Mode Register will be initialized to $0 by MCU reset, so that all these pins are set to a port mode.

Table 6. Port Mode Register

PMR bit 3	$R_{33}/\overline{INT_1}$ pin
0	Used as R_{33} port input/output pin
1	Used as $\overline{INT_1}$ input pin

PMR bit 2	$R_{32}/\overline{INT_0}$ pin
0	Used as R_{32} port input/output pin
1	Used as $\overline{INT_0}$ input pin

PMR bit 1	R_{41}/SI pin
0	Used as R_{41} port input/output pin
1	Used as SI input pin

PMR bit 0	R_{42}/SO pin
0	Used as R_{42} port input/output pin
1	Used as SO output pin

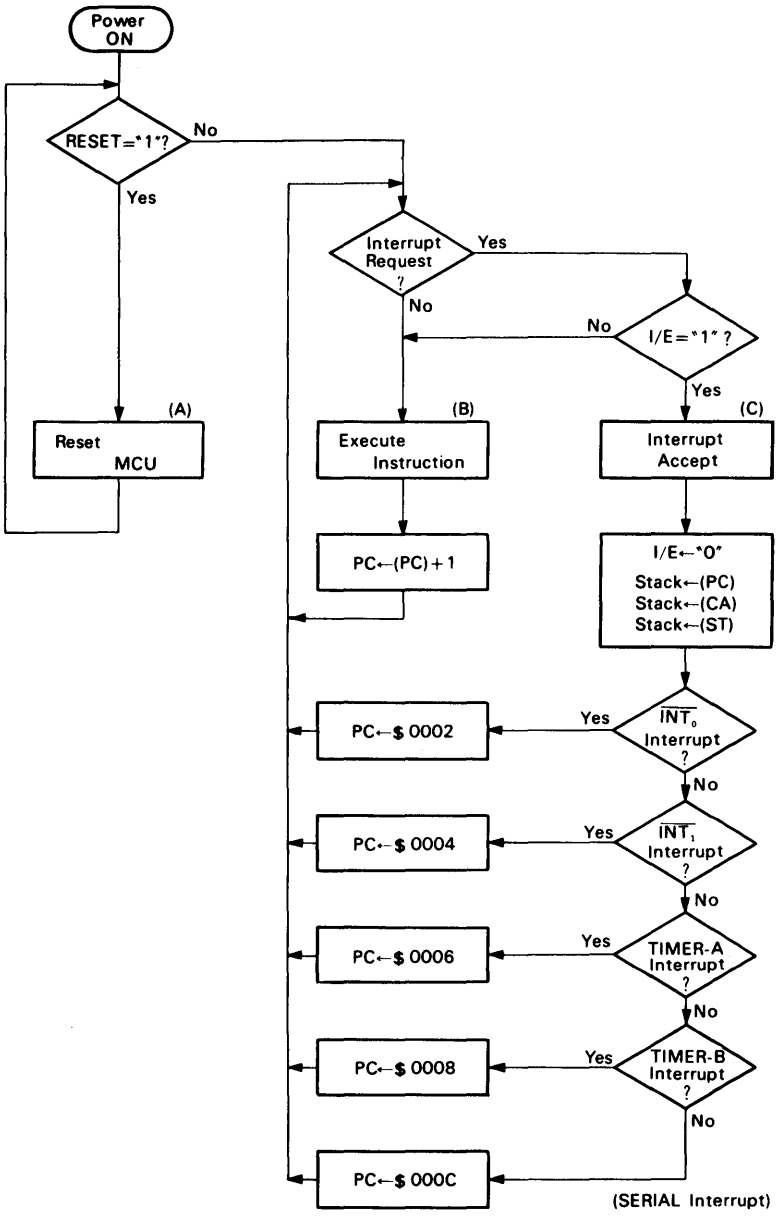


Fig. 8 Interrupt Servicing Flowchart

■ SERIAL INTERFACE

The serial interface is used to transmit/receive 8-bit data serially. This consists of the Serial Data Register, the Serial Mode Register, the Octal Counter and the multiplexer, as illustrated in Fig. 9. Pin $R_{40}/\overline{SCK}$ and the transfer clock signal are controlled by the Serial Mode Register. Contents of the Serial Data Register can be written into or read out by the software. The data in the Serial Data Register can be shifted synchronously with the transfer clock signal.

The serial interface operation is initiated with STS instruction. The Octal Counter is reset to $0 by STS instruction. It starts to count at the falling edge of the transfer clock ($\overline{SCK}$) signal and increments by one at the rising edge of the $\overline{SCK}$. When the Octal Counter is reset to $0 after eight transfer clock signals, or discontinued transmit/receive operation by resetting the Octal Counter, the SERIAL Interrupt Request Flag will be set.

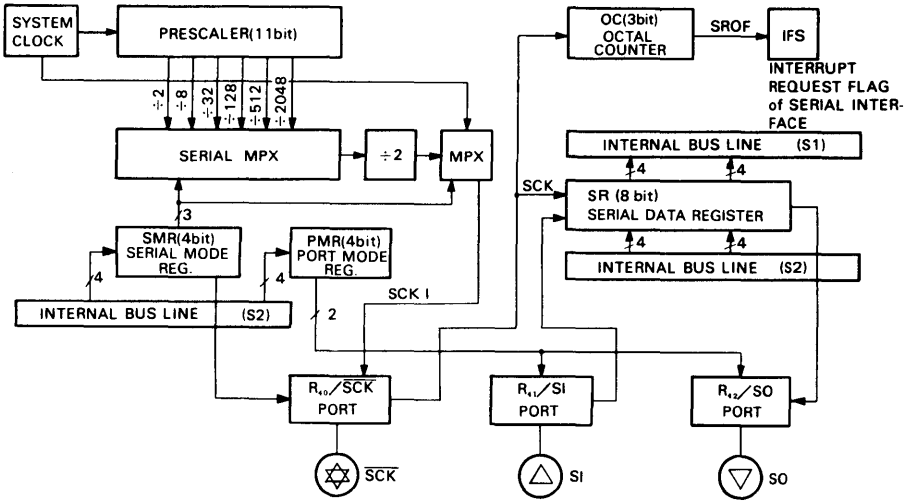


Fig. 9 Serial Interface Block Diagram

• Serial Mode Register (SMR: $005)

The Serial Mode Register is a 4-bit write-only register. This register controls the $R_{40}/\overline{SCK}$ and the prescaler divide ratio as the transfer clock source as shown in Table 7.

The Write Signal to the Serial Mode Register controls the operating state of serial interface.

The Write Signal to the Serial Mode Register stops the transfer clock applied to the Serial Data Register and the Octal Counter. And it also reset the Octal Counter to $0 simultaneously.

When the Serial Interface is in the "Transfer State", the Write Signal to the Serial Mode Register causes to quit the data transfer and to set the SERIAL Interrupt Request Flag.

Contents of the Serial Mode Register will be changed on the second instruction cycle after writing into the Serial Mode Register. Therefore, it will be necessary to execute the STS instruction after the data in the Serial Mode Register has been changed completely. The Serial Mode Register will be reset to $0 by MCU reset.

• Serial Data Register (SRL: $006, SRU: $007)

The Serial Data Register is an 8-bit read/write register. It consists of a low-order digit (SRL:$006) and a high-order digit (SRU: $007).

The data in the Serial Data Register will be output from the LSB side at SO pin synchronously with the falling edge of the transfer clock signal. At the same time, external data will be input from the LSB side at SI pin to the Serial Data Register synchronously with the rising edge of the transfer clock. Fig. 10 shows the I/O timing chart for the transfer clock signal and the data.

The writing into/reading from the Serial Data Register during its shifting causes the validity of the data.

Therefore complete data transmit/receive before writing into/reading from the serial data register.

Table 7. Serial Mode Register

SMR Bit 3	$R_{40}/\overline{SCK}$
0	Used as R_{40} port input/output pin
1	Used as $\overline{SCK}$ input/output pin

SMR			Transfer Clock			
Bit 2	Bit 1	Bit 0	$R_{40}/\overline{SCK}$ Port	Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio
0	0	0	$\overline{SCK}$ Output	Prescaler	÷ 2048	÷ 4096
0	0	1	$\overline{SCK}$ Output	Prescaler	÷ 512	÷ 1024
0	1	0	$\overline{SCK}$ Output	Prescaler	÷ 128	÷ 256
0	1	1	$\overline{SCK}$ Output	Prescaler	÷ 32	÷ 64
1	0	0	$\overline{SCK}$ Output	Prescaler	÷ 8	÷ 16
1	0	1	$\overline{SCK}$ Output	Prescaler	÷ 2	÷ 4
1	1	0	$\overline{SCK}$ Output	System Clock	–	÷ 1
1	1	1	$\overline{SCK}$ Input	External Clock	–	–

(In the case of SMR Bit 3 = 1)

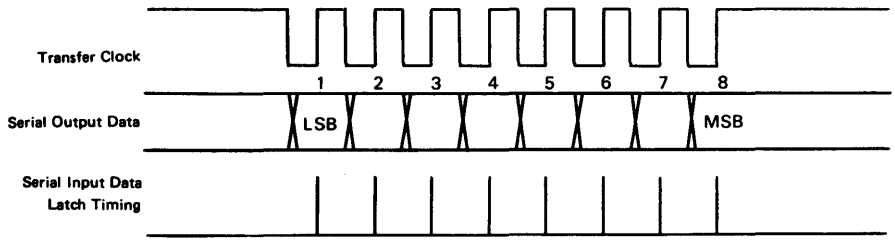


Fig. 10 Serial Interface I/O Timing Chart

- **SERIAL Interrupt Request Flag (IFS: $003, 0)**

The SERIAL Interrupt Request Flag will be set after the eight transfer clock signals or transmit/receive discontinued operation by resetting the Octal Counter.

- **SERIAL Interrupt Mask (IMS: $003, 1)**

The SERIAL Interrupt Mask masks the interrupt request.

Table 8. SERIAL Interrupt Request Flag

SERIAL Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 9. SERIAL Interrupt Mask

SERIAL Interrupt Mask	Interrupt Request
0	Enable
1	Disable (masks)

- **Selection of the Operation Mode**

Table 10 shows the operation mode of the serial interface. Select a combination of the value in the Port Mode Register and the Serial Mode Register according to Table 10.

Initialize the serial interface by the Write Signal to the Serial Mode Register, when the Operation Mode is changed.

- **Operating State of Serial Interface**

The serial interface has 3 operating states as shown in Fig. 11.

The serial interface gets into "STS waiting state" by 2 ways: one way is to change the operation mode by changing the data

in the Port Mode Register, the other is to write data into the Serial Mode Register. In this state, the serial interface does not operate although the transfer clock is applied. If STS instruction is executed, the serial interface changes its state to "SCK waiting state".

In the "SCK waiting state", the falling edge of first transfer clock affects the serial interface to get into "transfer state", while the Octal Counter counts-up and the Serial Data Register shifts simultaneously. As an exception, if the clock continuous output mode is selected, the serial interface stays in "SCK waiting state" while the transfer clock outputs continuously.

The Octal Counter becomes "000" again by 8 transfer clocks or execution of STS instruction, so that the serial interface gets back into the "SCK waiting state", and SERIAL Interrupt Request Flag is set simultaneously.

When the internal transfer clock is selected, the transfer clock output are triggered by the execution of STS instruction, and it stops after 8 clocks.

- **Example of Transfer Clock Error Detection**

The serial interface functions abnormally when the transfer clock was disturbed by external noises. In this case, the transfer clock error can be detected in the procedure shown in Fig. 12.

If more than 9 transfer clocks are applied by the external noises in the "SCK waiting state", the state of the serial interface shifts as the following sequence: first "transfer state" (while 1 to 7 transfer clocks), second "SCK waiting state" (at 8th transfer clock) and third "transfer state" again. Then reset the SERIAL Interrupt Request Flag, and make "STS waiting state" by writing to the Serial Mode Register. SERIAL Interrupt Request Flag is set again in this procedure, and it shows that the transfer clock was invalid and that the transmit/receive data were also invalid.

Table 10. Serial Interface Operation Mode

SMR	PMR		Serial Interface Operating Mode
Bit 3	Bit 1	Bit 0	
1	0	0	Clock Continuous Output Mode
1	0	1	Transmit Mode
1	1	0	Receive Mode
1	1	1	Transmit/Receive Mode

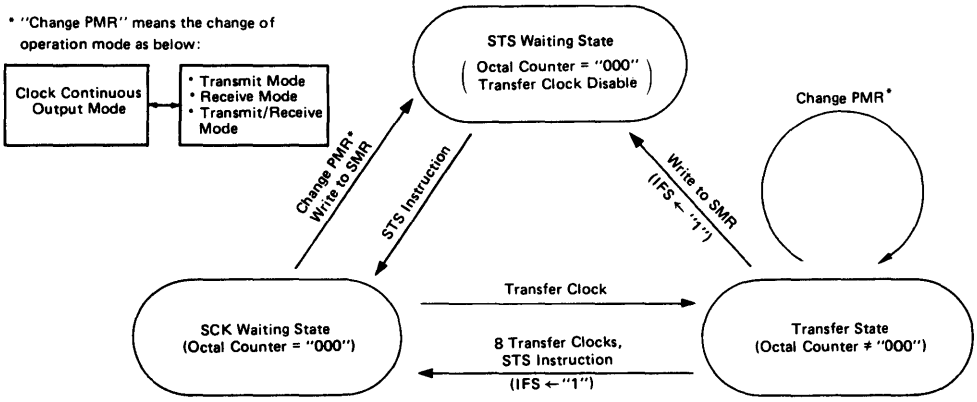


Fig. 11 Serial Interface Operation State

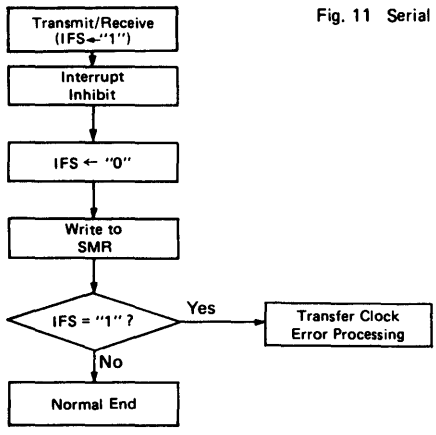


Fig. 12 Example of Transfer Clock Error Detection

■ TIMER

The MCU contains a prescaler and two timer/counters (TIMER-A, TIMER-B), Fig. 13 shows the block diagram. The prescaler is an 11-bit binary counter. TIMER-A is an 8-bit free-run timer. TIMER-B is an 8-bit auto-reload timer/event counter.

- **Prescaler**

The input to the prescaler is a system clock signal. The prescaler is initialized to $000 by MCU reset, and the prescaler starts to count up the system clock signal as soon as RESET input goes to logic "0". The prescaler keeps counting up except MCU reset and stop mode. The prescaler provides clock signals to TIMER-A, TIMER-B and serial interface. The prescaler divide ratio of the clock signals are selected according to the content of the mode registers such as – Timer Mode Register A (TMA), Timer Mode Register B (TMB), Serial Mode Register (SMR).

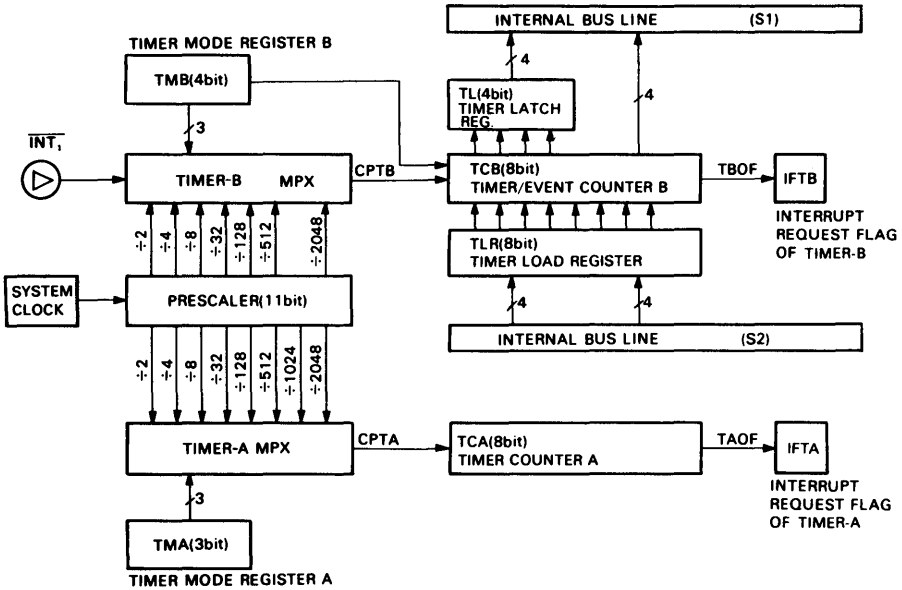


Fig. 13 Timer/Counter Block Diagram

- **TIMER-A Operation**

After TIMER-A is initialized to $00 by MCU reset, it counts up at every clock input signal. When the next clock signal is applied after TIMER-A is counted up to $FF, TIMER-A is set to $00 again, and generating overflow output. This leads to setting TIMER-A Interrupt Request Flag (IFTA: $001, 2) to "1". Therefore, this timer can function as an interval timer periodically generating overflow output at every 256th clock signal input.

The clock input signals to TIMER-A are selected by the Timer Mode Register A (TMA: $008).

- **TIMER-B Operation**

Timer Mode Register B (TMB: $009) is used to select the auto-reload function and the prescaler divide ratio of TIMER-B as the input clock source. When the external event input is used as an input clock signal to TIMER-B, select the $R_{33}/\overline{INT_1}$ as $\overline{INT_1}$ and set the External Interrupt Mask (IM1) to "1" to prevent the external interrupt request from occurring.

TIMER-B is initialized according to the value written into the Timer Load Register by software. TIMER-B counts up at every clock input signal. When the next clock signal is applied to TIMER-B after TIMER-B is set to $FF, TIMER-B will be initialized again and generate overflow output. In this case if the auto-reload function is selected. TIMER-B is initialized according to the value of the Timer Load Register. Else if the auto-reload function is not selected, TIMER-B goes to $00. TIMER-B Interrupt Request Flag (IFTB: $002,0) will be set at this overflow output.

- **Timer Mode Register A (TMA: $008)**

The Timer Mode Register A is a 3-bit write-only register. The TMA controls the prescaler divide ratio of TIMER-A clock input, as shown in Table 11.

The Timer Mode Register A is initialized to $0 by MCU reset.

- **Timer Mode Register B (TMB: $009)**

The Timer Mode Register B is a 4-bit write-only register. The Timer Mode Register B controls the selection for the auto-reload function of TIMER-B and the prescaler divide ratio, and the source of the clock input signal, as shown in Table 12.

The Timer Mode Register B is initialized to $00 by MCU reset.

The operation mode of TIMER–B is changed at the second instruction cycle after writing into the Timer Mode Register B.

Therefore, it is necessary to program the write instruction to TLRU after the content of TMB is changed.

Table 11. Timer Mode Register A

TMA			Prescaler Divide Ratio
Bit 2	Bit 1	Bit 0	
0	0	0	÷2048
0	0	1	÷1024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	0	÷ 32
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2

Table 12. Timer Mode Register B

TMB Bit 3	Auto-reload Function
0	No
1	Yes

TMB Bit 2	TMB Bit 1	TMB Bit 0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	$\overline{INT_1}$ (External Event Input)

- **TIMER-B (TCBL: $00A, TCBU: $00B / TLRL: $00A, TLRU: $00B)**

TIMER-B consists of an 8-bit write-only Timer Load Register, and an 8-bit read-only Timer/Event Counter. Each of them has a low-order digit (TCBL: $00A, TLRL: $00A) and a high-order digit (TCBU: $00B, TLRU: $00B).

The Timer/Event Counter can be initialized by writing data into the Timer Load Register. In this case, write the low-order digit first, and then the high-order digit. The Timer/Event Counter is initialized at the time when the high-order digit is written. The Timer Load Register will be initialized to $00 by the MCU reset.

The counter value of TIMER-B can be obtained by reading the Timer/Event Counter. In this case, read the high-order digit first, and then the low-order digit. The count value of low-order digit is latched at the time when the high-order digit is read.

- **TIMER-A Interrupt Request Flag (IFTA: $001, 2)**

The TIMER-A Interrupt Request Flag is set by the overflow output of TIMER-A.

- **TIMER-A Interrupt Mask (IMTA: $001, 3)**

TIMER-A Interrupt Mask prevents an interrupt request generated by TIMER-A Interrupt Request Flag.

Table 13. TIMER-A Interrupt Request Flag

TIMER-A Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 14. TIMER-A Interrupt Mask

TIMER-A Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

- **TIMER-B Interrupt Request Flag (IFTB: $002, 0)**

The TIMER-B Interrupt Request Flag is set by the overflow output of TIMER-B.

- **TIMER-B Interrupt Mask (IMTB: $002, 1)**

TIMER-B Interrupt Mask prevents an interrupt request generated by TIMER-B Interrupt Request Flag.

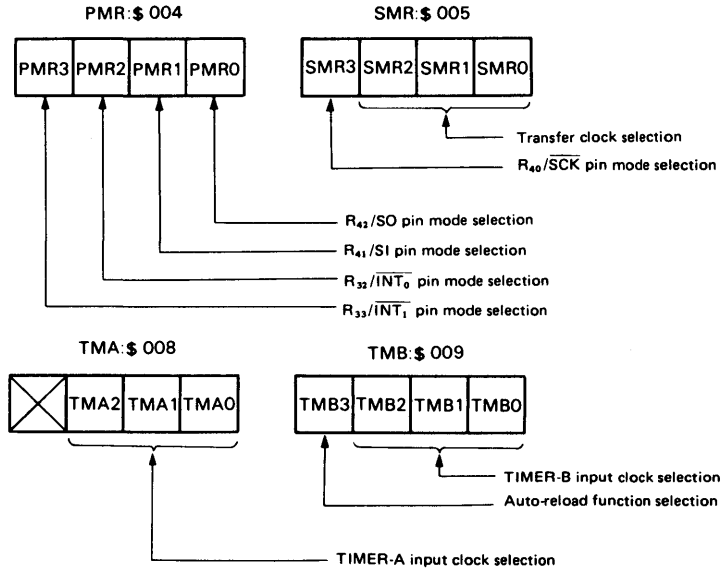


Fig. 14 Mode Register Configuration and Function

Table 15. TIMER-B Interrupt Request Flag

TIMER-B Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 16. TIMER-B Interrupt Mask

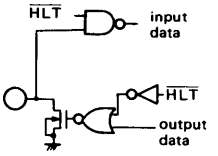
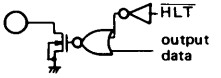
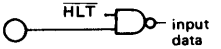
TIMER-B Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

■ INPUT/OUTPUT

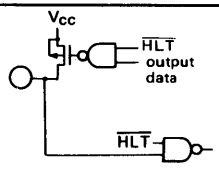
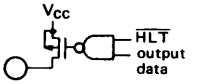
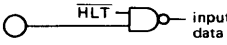
The MCU provides 58 Input/Output pins, and they are consist of 32 standard pins of "Without pull-up MOS (NMOS open drain)" and 26 high voltage pins of "Without pull-down MOS (PMOS open drain)".

When any input/output common pin is used as input pin, it is necessary to set the output data as shown in Table 18.

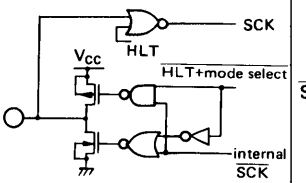
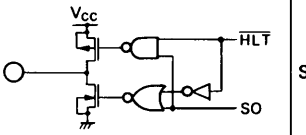
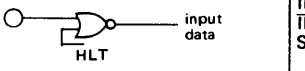
Table 17 I/O Pin Circuit Forms

		Without pull-up MOS (NMOS open drain)	Applied pins
Standard pins	I/O common pins		$D_0 \sim D_3$, $R_{30} \sim R_{33}$, $R_{40} \sim R_{43}$, $R_{50} \sim R_{53}$
	Output pins		$R_{60} \sim R_{63}$, $R_{70} \sim R_{73}$, $R_{80} \sim R_{83}$
	Input pins		$R_{90} \sim R_{93}$

(Continued)

		Without pull-down MOS (PMOS open drain)	Applied pins
High voltage pins	I/O common pins		$D_4 \sim D_{15}$, $R_{10} \sim R_{13}$, $R_{20} \sim R_{23}$
	Output pins		$R_{00} \sim R_{03}$
	Input pins		R_{A0}, R_{A1}/V_{disp}

(Note) In the stop mode, $\overline{HLT}$ signal is "0", HLT signal is "1" and I/O pins are in high impedance.

		Without pull-up MOS (NMOS open drain)	Applied pins
Standard pins	I/O common pins		$\overline{SCK}$
	Output pins		SO
	Input pins		$\overline{INT_0}$, $\overline{INT_1}$, SI

(Note) In the stop mode, $\overline{HLT}$ signal is "0", HLT signal is "1" and I/O pins are in high impedance.

Table 18 Data Input from Input/Output Common Pins

I/O circuit type	Available pin condition for input
For Standard pins "Without pull-up MOS (NMOS open drain)"	"1"
For High voltage pins "Without pull-down MOS (PMOS open drain)"	"0"

- **D-port**

D-port is 1-bit I/O port, and it has 16 Input/Output common pins. It can be set/reset by the SED/RED and SEDD/REDD instructions, and can be tested by the TD and TDD instructions. Table 17 shows the classification of standard pins, high voltage pins and the Input/Output pins circuit types.

- **R-port**

R-port is 4-bit I/O port. It provides 20 input/output common pins, 16 output-only pins, and 6 input-only pins. Data input is processed using the LAR and LBR instructions and data output is processed using the LRA and LRB instructions. The MCU will not be affected by writing into the input-only and/or non-existing ports, invalid data will be read by reading from the output-only and/or non-existing ports.

The R_{32}, R_{33}, R_{40}, R_{41} and R_{42} pins are also used as the $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK}$, SI and SO pins respectively. Table 17 shows the classification of standard pins, high voltage pins and Input/Output pins circuit types.

- **RESET**

The MCU is reset by setting RESET pin to "1". At power

Table 19 MCU Initial Value by Reset

Items			Initial value by MCU reset	Contents
Program counter (PC)			$0000	Execute program from the top of ROM address.
Status (ST)			"1"	Enable to branch with conditional branch instructions.
Stack pointer (SP)			$3FF	Stack level is 0.
I/O output register	Standard pin	Without pull-up MOS	"1"	Enable to input.
	High voltage pin	Without pull-down MOS	"0"	Enable to input.
Interrupt flag	Interrupt Enable Flag (I/E)		"0"	Inhibit all interrupts.
	Interrupt Request Flag (IF)		"0"	No interrupt request.
	Interrupt Mask (IM)		"1"	Mask interrupt request.
Mode register	Port Mode Register (PMR)		"0000"	See Item "Port Mode Register".
	Serial Mode Register (SMR)		"0000"	See Item "Serial Mode Register".
	Timer Mode Register A (TMA)		"000"	See Item "Timer Mode Register A".
	Timer Mode Register B (TMB)		"0000"	See Item "Timer Mode Register B".
Timer/Counter, Serial Interface	Prescaler		$000	–
	Timer/Counter A (TCA)		$00	–
	Timer/Event Counter B (TCB)		$00	–
	Timer Load Register (TLR)		$00	–
	Octal Counter		"000"	–

(Note) The values of registers and flags which are not described on above table will become as follows.

Item	After releasing stop mode by MCU Reset	After MCU Reset except the left
Carry (CA) Accumulator (A) B register (B) W register (W) X/SPX register (X/SPX) Y/SPY register (Y/SPY)	The value immediately before MCU reset is not guaranteed. Initialization by the program should be required.	The value immediately before MCU Reset is not guaranteed. Initialization by the program should be required.
Serial data register (SR)	– ditto –	– ditto –
RAM	The value immediately before MCU reset (the value immediately before executing stop instruction) is retained.	– ditto –

ON or recovering from stop mode, apply RESET input more than t_{RC} to obtain the necessary time for oscillator stabilization. In other cases, the MCU reset requires at least two instructions cycle time of RESET input.

Table 19 shows initialized items by MCU reset and each status after reset.

■ INTERNAL OSCILLATOR CIRCUIT

Fig. 15 gives internal oscillator circuit. The oscillator type can be selected from the followings; crystal resonator, or ceramic filter resonator as shown in Table 20. In any cases, external clock operation is available.

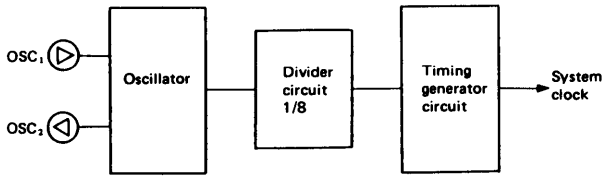
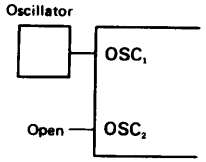
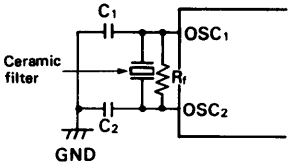
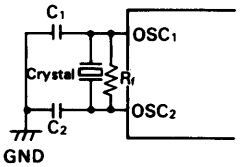
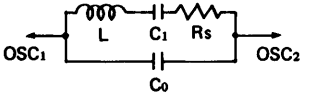


Fig. 15 Internal Oscillator Circuit

Table 20 Oscillator Circuit Example

	Circuit configuration	Remarks
External clock operation		
Ceramic filter resonator		Ceramic filter: CSA 4.00MG (Murata) R_f: 1MΩ ± 2% C_1: 33pF ± 20% C_2: 33pF ± 20% Ceramic filter: CSA 6.00MG (Murata) R_f: 1MΩ ±2% C_1: 30pF ± 20% C_2: 30pF ± 20% ● Wiring between these pins and elements should be as short as possible, and never cross the other wirings. (Refer to Fig. 16)
Crystal resonator	 	Crystal: 4.194304 (MHz) NC-18C (Nihon Denpa Kogyo) R_f: 1MΩ ± 2% C_1: 22pF ± 20% C_2: 22pF ± 20% Crystal: 6.0 (MHz) NC-18C (Nihon Denpa Kogyo) R_f: 1MΩ ± 2% C_1: 20pF ±20% C_2: 20pF ± 20% Crystal: ATcut parallel resonance crystal C_0: 7pF max. R_S: 100Ω max. f: 2.0 ~6.2MHz ● Wiring between these pins and elements should be as short as possible, and never cross the other wirings. (Refer to Fig. 16)

* Please consult with the engineers of crystal or ceramic filter resonator maker to determine the value of R_f, C_1 and C_2.

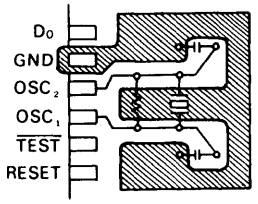


Fig. 16 Recommendable Layout of Crystal and Ceramic Filter

■ LOW POWER DISSIPATION MODE

The MCU provides two low power dissipation modes, that is, a Standby mode and a Stop mode. Table 21 shows the function of the low power dissipation mode, and Fig. 17 shows the diagram of the mode transition.

Table 21 Low Power Dissipation Mode Function

Low Power Dissipation Mode	Instruction	Condition							Recovering method
		Oscillator circuit	Instruction execution	Register Flag	Interrupt function	RAM	Input/ Output pin	Timer/ Counter, Serial Interface	
Standby mode	SBY instruction	Active	Stop	Retained	Active	Retained	Retained*2)	Active	RESET Input, Interrupt request
Stop mode	STOP instruction	Stop	Stop	RESET*1)	Stop	Retained	High impedance	Stop	RESET Input

*1) STOP mode is released only by MCU Reset. Refer to Table 19 as for the values of the registers and flags after releasing stop mode.
*2) Current flows in I/O Circuit by I/O pin state at stand-by mode, because I/O circuit is active.
This current is an addition to stand-by mode power dissipation.

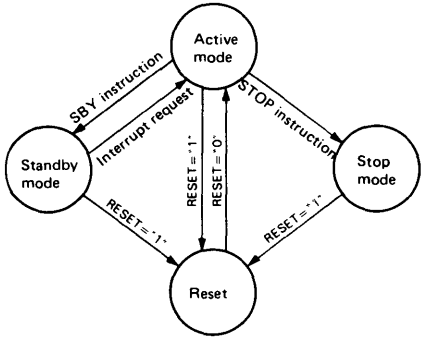


Fig. 17 MCU Operation Mode Transition

• Standby Mode

The SBY instruction puts the MCU into the Standby mode. In the Standby mode, the oscillator circuit is active and timer/counter and serial interface continue working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM and Input/Output pins retain the state they had just before going into the Standby mode.

The Standby mode is canceled by the MCU reset or interrupt request. When canceled by the interrupt request, the MCU becomes an active mode and executes the instruction next to the SBY instruction. At this time, if the Interrupt Enable Flag is "1", the interrupt is executed. If the Interrupt Enable Flag is "0", the interrupt request is held on and the normal instruction execution continues.

Fig. 18 shows the flowchart of the Standby Mode.

• Stop Mode

The STOP instruction brings the MCU into the Stop mode. In this mode the oscillator circuit and every function of the MCU stop.

The Stop mode is canceled by the MCU reset. At this time, as shown in Fig. 19, apply the RESET input for more than t_{RC} to get enough oscillator stabilization time. (Refer to the "AC CHARACTERISTICS".) After the Stop mode is canceled, RAM retains the state it had just before going into the Stop mode after releasing stop mode by MCU reset, the values of the B register, W register, X/SPX register, Y/SPY register, carry and serial data register are not guaranteed.

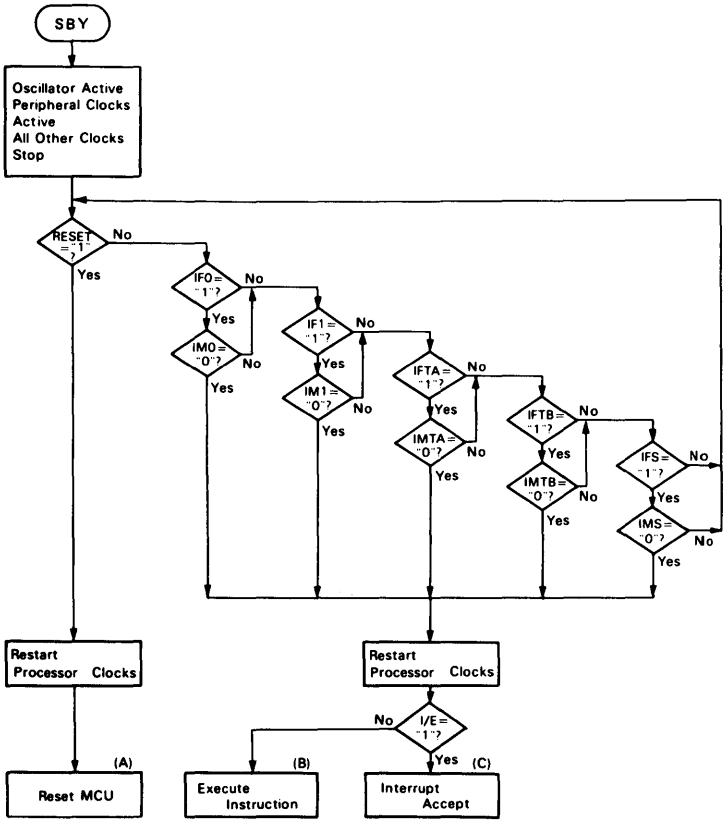


Fig. 18 MCU Operating Flowchart

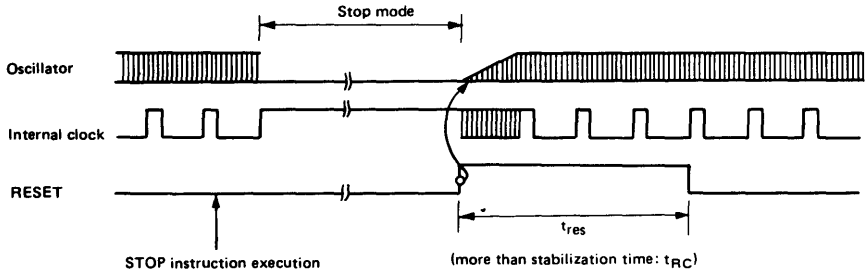


Fig. 19 Stop Mode Cancel Timing Chart

■ RAM ADDRESSING MODE

As shown in Fig. 20, the MCU provides three RAM addressing modes; Register Indirect Addressing, Direct Addressing and Memory Register Addressing.

• Register Indirect Addressing

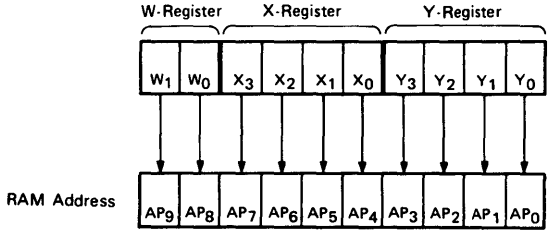
The combined 10-bit contents of W Register, X Register and Y Register is used as the RAM address in this mode.

• Direct Addressing

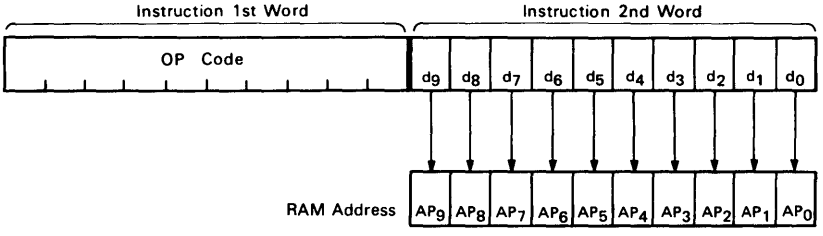
The direct addressing instruction consists of two words and the second word (10 bits) following Op-code (the first word) is used as the RAM address.

• Memory Register Addressing

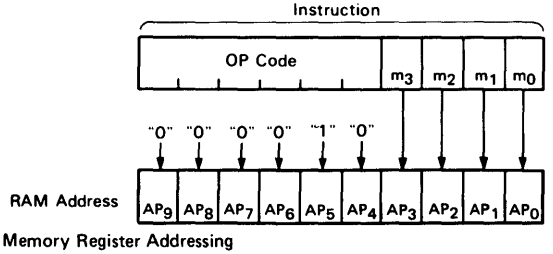
The Memory Register Addressing can access 16 digits (Memory Register: MR) from $020 to $02F by using the LAMR and XMRA instruction.



(a) Register Indirect Addressing



(b) Direct Addressing



(c) Memory Register Addressing

Fig. 20 RAM Addressing Mode

■ ROM ADDRESSING MODE AND P INSTRUCTION

The MCU has four kinds of ROM addressing modes as shown in Fig. 21.

• Direct Addressing Mode

The program can branch to any addresses in the ROM memory space by using JMPL, BRL or CALL instruction. These instructions replace 14-bit program counter (PC13 to PC0) with 14-bit immediate data.

• Current Page Addressing Mode

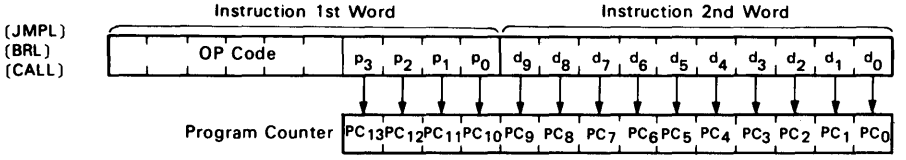
ROM memory space is divided into 256 words in each page starting from $0000. The program branches to the address in the same page using BR instruction. This instruction replace the low-order eight bits of program counter (PC7 to PC0) with 8-bit immediate data.

• Zero Page Addressing Mode

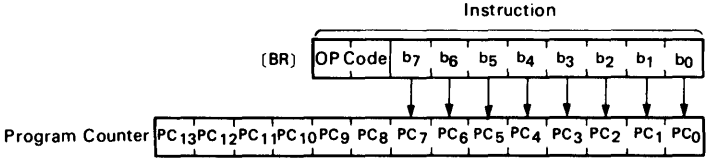
The program branches to the zero page subroutine area, which is located on the address from $0000 to $003F, using CAL instruction. When CAL instruction is executed, 6-bit immediate data is placed in low-order six bits of program counter (PC5 to PC0) and "0's" are placed in high-order eight bits (PC13 to PC6). The branch destination by BR instruction on the boundary between pages is given in Fig. 23.

• Table Data Addressing

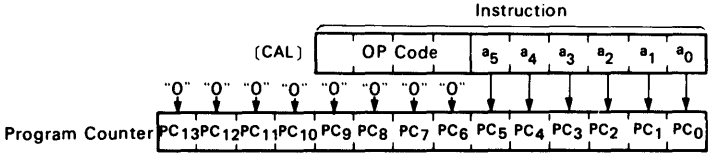
The program branches to the address determined by the contents of the 4-bit immediate data, accumulator and B register, using TBR instruction.



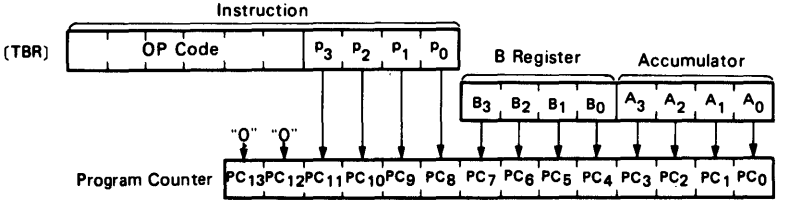
(a) Direct Addressing



(b) Current Page Addressing

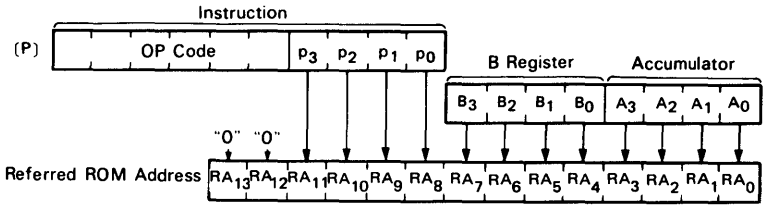


(c) Zero Page Addressing

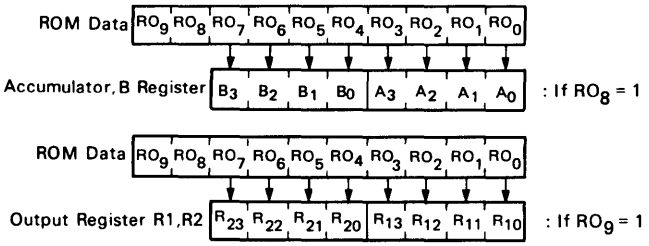


(d) Table Data Addressing

Fig. 21 ROM Addressing Mode



(a) Address Designation



(b) Pattern Output

Fig. 22 P Instruction

- **P Instruction (Pattern Instruction)**

By P instruction, the ROM data determined by Table Data addressing is referred. When bit 8 in referred ROM data is "1", 8 bits of referred ROM data are written into the accumulator and B Register. When bit 9 is "1", 8 bits of referred ROM data are written into the R1 and R2 port output register. When both bit 8 and 9 are "1", ROM data are written into the accumulator and B register and also to the R1 and R2 port output register at a same time.

The P instruction has no effect on the program counter.

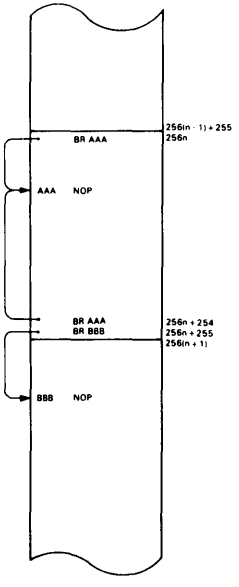


Fig. 23 The Branch Destination by BR Instruction on the Boundary between Pages

■ INSTRUCTION SET

The HMCS400 series provide 99 instructions. These instructions are classified into 10 groups as follows;

(1) Immediate Instruction
(2) Register-to-Register Instruction
(3) RAM Address Instruction
(4) RAM Register Instruction
(5) Arithmetic Instruction
(6) Compare Instruction
(7) RAM Bit Manipulation Instruction
(8) ROM Address Instruction
(9) Input/Output Instruction
(10) Control Instruction

Table 22. Immediate Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD / CYCLE
Load A from Immediate	LAI i	1 0 0 0 1 1 i_3 i_2 i_1 i_0	i→A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i_3 i_2 i_1 i_0	i→B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i→M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i_3 i_2 i_1 i_0	i→M,Y+1→Y	NZ	1/1

Table 23. Register-to-Register Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD / CYCLE
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B→A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A→B		1/1
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y→A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX→A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY→A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m_3 m_2 m_1 m_0	MR(m)→A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m_3 m_2 m_1 m_0	MR(m)↔A		1/1

Table 24. RAM Address Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD / CYCLE
Load W from Immediate	LWI i	0 0 1 1 1 1 i_3 i_2 i_1 i_0	i→W		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i_3 i_2 i_1 i_0	i→X		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i_3 i_2 i_1 i_0	i→Y		1/1
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	A→X		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	A→Y		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	Y+1→Y	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	Y−1→Y	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	Y+A→Y	OVF	1/1
Subtract A from Y	SYY	0 0 1 1 0 1 0 1 0 0	Y−A→Y	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	X↔SPX		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	Y↔SPY		1/1
Exchange X and SPX,Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	X↔SPX,Y↔SPY		1/1

Table 25. RAM Register Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD / CYCLE
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M→A, (X↔SPX / Y↔SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M→A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M→B, (X↔SPX / Y↔SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A→M, (X↔SPX / Y↔SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A→M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A→M,Y+1→Y(X↔SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A→M,Y−1→Y(X↔SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M↔A, (X↔SPX / Y↔SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M↔A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M↔B, (X↔SPX / Y↔SPY)		1/1

Note) (XY) and (x) have the meaning as follows:

(1) The instructions with (XY) have 4 mnemonics and 4 object codes for each. (example of LAM (XY) is given below.)

MNEMONIC	y	x	FUNCTION
LAM	0	0	
LAMX	0	1	X↔SPX
LAMY	1	0	Y↔SPY
LAMXY	1	1	X↔SPX, Y↔SPY

(2) The instructions with (x) have 2 mnemonics and 2 object codes for each. (example of LMAIY(X) is given below.)

MNEMONIC	x	FUNCTION
LMAIY	0	
LMAIYX	1	X↔SPX

Table 26. Arithmetic Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Add Immediate to A	AI i	1 0 1 0 0 0 i_3 i_2 i_1 i_0	A+i→A	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	B+1→B	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	B−1→B	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\overline{A}$+1→A		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\overline{B}$→B		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	1→CA		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	0→CA		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	M+A→A	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M+A→A	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	M+A+CA→A	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M+A+CA→A	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	M−A−$\overline{CA}$→A	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M−A−$\overline{CA}$→A	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	A∪B →A		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	A∩M→A	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A∩M→A	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	A∪M→A	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A∪M→A	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	A⊕M→A	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A⊕M→A	NZ	2/2

Table 27. Compare Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i_3 i_2 i_1 i_0	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	ANEMD d	0 1 0 0 0 0 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i_3 i_2 i_1 i_0	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i_3 i_2 i_1 i_0	i ≦ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i ≦ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≦ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ≦ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≦ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i_3 i_2 i_1 i_0	A ≦ i	NB	1/1

Table 28. RAM Bit Manipulation Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n_1 n_0	1→M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	1→M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n_1 n_0	0→M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	0→M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n_1 n_0		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		M(n)	2/2

Table 29. ROM Address Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Branch on Status 1	BR b	1 1 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a_5 a_4 a_3 a_2 a_1 a_0		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p_3 p_2 p_1 p_0			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1→I/E		1/3

Table 30. Input/Output Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1→D(Y)		1/1
Set Discrete I/O Latch Direct	SEDD m	1 0 1 1 1 0 m_3 m_2 m_1 m_0	1→D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0→D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m_3 m_2 m_1 m_0	0→D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m_3 m_2 m_1 m_0		D(m)	1/1
Load A from R-Port Register	LAR m	1 0 0 1 0 1 m_3 m_2 m_1 m_0	R(m)→A		1/1
Load B from R-Port Register	LBR m	1 0 0 1 0 0 m_3 m_2 m_1 m_0	R(m)→B		1/1
Load R-Port Register from A	LRA m	1 0 1 1 0 1 m_3 m_2 m_1 m_0	A→R(m)		1/1
Load R-Port Register from B	LRB m	1 0 1 1 0 0 m_3 m_2 m_1 m_0	B→R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p_3 p_2 p_1 p_0			1/2

Table 31. Control Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD / CYCLE
No Operation	NOP	0000000000			1/1
Start Serial	STS	0101001000			1/1
Stand-by Mode	SBY	0101001100			1/1
Stop Mode	STOP	0101001101			1/1

Table 32. Op-Code Map

R9 H \ R8 L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	NOP	XSPX	XSPY	XSP XY	AN EM			AM				ORM			
	1	RTN	RTNI			ALEM			AMC				EORM			
	2	INEM i(4)														
	3	ILEM i(4)														
	4	LBM(XY)			BNEM				LAB				IB			
	5	LMAIY(X)			AYY				LASPY				IY			
	6	NEGA			RED				LASPX							TC
	7	YNEI i(4)														
	8	XMA(XY)			SEM n(2)				REM n(2)				TM n(2)			
	9	LAM(XY)			LMA(XY)				SMC				ANM			
	A	ROTR	ROTL			DAA				DAS						LAY
	B	TBR p(4)														
	C	XMB(XY)			BLEM				LBA							DB
	D	LMADY(X)			SYY				LYA							DY
	E	TD			SED				LXA				REC			SEC
	F	LWI i(4)														
1	0	LBI i(4)														
	1	LYI i(4)														
	2	LXI i(4)														
	3	LAI i(4)														
	4	LBR m(4)														
	5	LAR m(4)														
	6	REDD m(4)														
	7	LAMR m(4)														
	8	AI i(4)														
	9	LMIIY i(4)														
	A	TDD m(4)														
	B	ALEI i(4)														
	C	LRB m(4)														
	D	LRA m(4)														
	E	SEDD m(4)														
	F	XMRA m(4)														

R9 H \ R8 L	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0				ANEMD				AMD				ORMD			
				ALEMD				AMCD				EORMD			
	INEMD i(4)														
	ILEMD i(4)														
	COMB			OR				STS				SBY	STOP		
	JMPL p(4)														
	CALL p(4)														
	BRL p(4)														
	XMAD			SEMD n(2)				REMD n(2)				TMD n(2)			
	LAMD			LMAD				SMCD				ANMD			
	LMID i(4)														
	P p(4)														
	CAL a(6)														
1	BR b(8)														

... 1 word/2 cycle Instruction

... 1 word/3 cycle Instruction

... RAM Direct Address Instruction (2 word/2 cycle)

... 2 word/2 cycle Instruction

■ **PRECAUTION TO USE THE EPROM ON-PACKAGE 4 BIT SINGLE CHIP MICROCOMPUTER**

Please pay attention to the followings, since this MCU has special structure with pin socket on the package.

(1) Don't apply high static voltage or surge voltage over MAXIMUM RATINGS to the socket pins as well as the LSI pins.
If not, that may cause permanent damage to the device.

(2) When using this in production like mask ROM type single chip microcomputer, pay attention to the followings to keep the good contact between the EPROM pins and socket pins.
(a) When soldering the LSI on a print circuit board, the recommended condition is
Temperature: lower than 250°C
Time : within 10 sec.
Over time/temperature may cause the bonding solder of socket pin to melt and the socket pin may drop.
(b) Note that the detergent or coating will not get in the socket during flux washing or board coating after soldering, because that may cause bad effect on socket contact.
(c) Avoid permanent application of this under the condition of vibratory place and system.
(d) The socket, inserted and pulled repeatedly loses its contactability. It is recommended to use new one when applied in production.

Table 33 Difference between the HD614P080S and HMCS404C/HMCS404AC

Item \ Type name		HD614P080S	HMCS404C		HMCS404AC	
Minimum instruction execution time		1.33 μs	2 μs		1.33 μs	
Power supply voltage		4.5 to 5.5 V	4 to 6 V		4.5 to 6 V	
ROM		∘ 4,096 words x 10 bits (using standard EPROM 2764) ∘ 8,192 words x 10 bits (using standard EPROM 27128)	4,096 words x 10 bits Mask ROM			
RAM		576 digits x 4 bits	256 digits x 4 bits			
I/O pin circuit	Standard pins	All pins are "without pull-up MOS (NMOS open drain)".	Each pin selects "without pull-up MOS (NMOS open drain)", "with pull-up MOS", or "CMOS".			
	High voltage pins	All pins are "without pull-down MOS (PMOS open drain)"	Each pin selects "without pull-down MOS (PMOS open drain)" or "with pull-down MOS."			
Clock generator		Crystal resonator or ceramic filter resonator	Crystal resonator, ceramic filter resonator, or resistance oscillator			
Package		Shrink type 64-pin EPROM on package (DC-64SP). The base chip pins are compatible with those of the HMCS404C/HMCS404AC.	Shrink type 64-pin dual-in-line plastic package (DP-64S) or 64-pin flat plastic package (FP-64).			
	Type	DC-64SP	DP-64S	FP-64	DP-64S	FP-64
	Occupied area (mm)	23 x 57.3	17 x 58	19.6 x 25.6	17 x 58	19.6 x 25.6
	High from stand-off	7.5 (max.) EPROM on package	5.1 (max)	2.9 (max)	5.1 (max.)	2.9 (max.)

EVALUATION CHIP FOR 4-BIT SINGLE-CHIP MICROCOMPUTERS

HD44850E

The HD44850E is an evaluation chip for 4-bit single-chip microcomputer, HMCS40 series. Its function is equivalent to HMCS45C except that it doesn't contain ROM. Instead, it has the function to address external memory (ROM or RAM). User can handle this evaluation chip by writing program into external program memory as well as the HMCS40 series chip in which program has been written. User program and system can be debugged by connecting this evaluation chip with external program memory in which user program is written to user systems.

The HD44850E provides 12-bit address outputs (A_0 to A_{11} terminals) and 10-bit instruction input pins (O_1 to O_{10} terminals) for the external program memory. ϕ and TSTP pins are required for debugging programs, and H43, CMOS and D/E pins for selecting applicable chips.

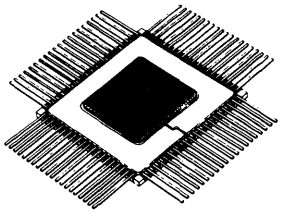
■ APPLICABLE CHIPS

HMCS42C, 43C, 44C, 45C

■ FUNCTION

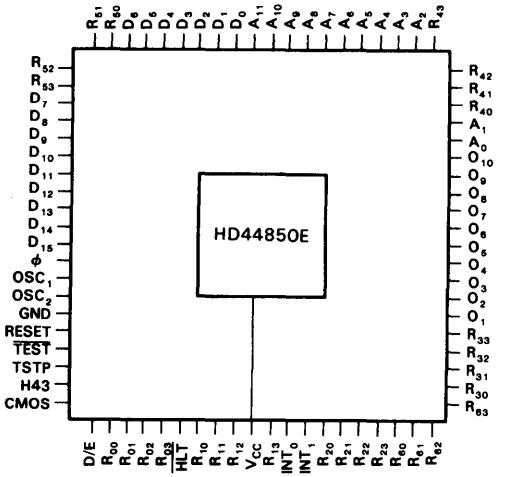
- Instruction Characteristics etc.; Same as the HMCS45C
- Address External ROM (2k)
- Address Output; Direct interface with EPROM (A_0 to A_{11})
- Instruction Input; EPROM or CMOS RAM or NMOS RAM (O_1 to O_{10})
  Direct interface with TTL
- CMOS/PMOS Selecting Input Pin
- Timer Halt Input
- I/O Enable/Disable Selecting Pin at Halt
- Output Pins except Address Output and Clock Open Drain Output
- Address Output, Clock; CMOS Output
- Input Pins; Inputs with no Pull up MOS

HD44850E



(FC-80)

■ PIN ARRANGEMENT



(Top View)

■ PIN NAME

A_0 to A_{11}	: Address Output
O_1 to O_{10}	: Instruction Input
ϕ	: Word Timing
TSTP	: Timer Stop Input
H43	: HMCS43/45A Selection
CMOS	: CMOS/PMOS Selection
D/E	: I/O Enable/Disable Selection Input in the Halt Mode
R_{00} to R_{53}	: I/O Common Port
R_{60} to R_{83}	: Output Port
D_0 to D_{15}	: I/O Common Port
OSC_1, OSC_2	: Oscillator
INT_0, INT_1	: Interrupt
RESET	: External Reset
$\overline{HLT}$	: Halt Pin
V_{CC}	: Power Supply
GND	: Ground

HD44857E

The HD44857E is an evaluation chip for 4-bit single-chip microcomputer, HMCS40 series. Its function is equivalent to HMCS47C except that it doesn't contain ROM and RAM. Instead, it has the function to address external memory, program memory (ROM or RAM) and data memory (RAM).

User can handle this evaluation chip by writing program into external program memory as well as the HMCS40 series chip in which program has been written.

The HD44857E provides address/instruction pins (A_0/O_1 to A_9/O_{10}, A_{10}/A_{11} terminals) for the external program memory, and address/bus pins (Y_1/S_{11} to Y_4/S_{14}, X_1/S_{21} to X_4/S_{24}), timing signal ϕ_1, ϕ_2 pins for accessing data RAM.

ϕ and TSTP pins are required for debugging programs, and CMOS and D/E pins for selecting applicable chips.

■ APPLICABLE CHIPS

HMCS42C, 43C, 44C, 45C, 46C, 47C

■ FUNCTION

- Instruction Characteristics etc.; Same as the HMCS47C
- Address External ROM (max; 4k words)
- Access External Data RAM (max; 256 digits)
- CMOS/PMOS Selecting Input Pin for evaluating PMOS
- Timer Stop Input
- I/O Enable/Disable Selecting Input Pin at Halt
- External ROM/RAM Access Pin; CMOS Pin
  All Output Pins except these are Open Drain Output.
- Input Pin; Input with no Pull up MOS

■ PIN NAME

(1) A_0/O_1 to A_9/O_{10} : Access pins for user program external memory. Divide 1 instruction cycle by two. The first half is the address from A_0 to A_9 and the latter half is instruction inputs from O_1 to O_{10}.

(2) A_{10}/A_{11} : Access pins for external user program memory. Divide 1 instruction cycle by two. The first half is A_{10} and the latter half is A_{11}.

(3) A_{11}* : Unusable. Be "open" always.

(4) X_1/S_{21} to X_4/S_{24} : Access pins for data RAM. Divide 1 instruction cycle by two. The first half (X_1 to X_4) is for selecting RAM file and the latter half (S_{21} to S_{24}) is bus signal for writing data into RAM.

(5) Y_1/S_{11} to Y_4/S_{14} : Access pins for data RAM. Divide 1 instruction cycle by two. The first half (Y_1 to Y_4) is for selecting RAM digit and the latter half (S_{11} to S_{14}) is bus signal for reading data from RAM to evaluation chip.

(6) ϕ, ϕ_1, ϕ_2 : Clock signal

(7) TSTP : Timer stops with timer stop input or "H" level, and operates with "L" level.

(8) CMOS : CMOS/PMOS selecting pin

(9) D/E : Selecting I/O state at halt

(10) R_{00} to R_{53} : I/O common pins (I/O pins)

(11) R_{60} to R_{63} : Output pins (I/O pins)

(12) D_0 to D_{15} : I/O common pins (I/O pins)

(13) OSC_1 : Oscillator (input)

(14) OSC_2 : Oscillator (output)

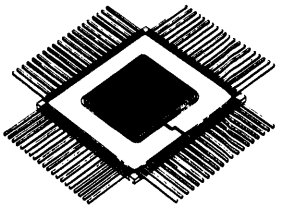
(15) $\overline{INT_0}$, $\overline{INT_1}$: Interrupt input pin

(16) $\overline{RESET}$: External reset input

(17) $\overline{HLT}$: Halt pin

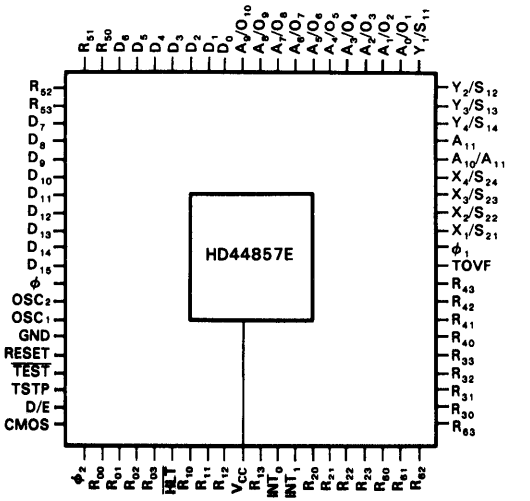
(18) $\overline{TEST}$: "H" level always

HD44857E



(FC-80)

■ PIN ARRANGEMENT



(Top View)

(19) TOVF : Time overflow. Not use usually. Be "open".

(20) V_{CC} : Power supply

(21) GND : Ground

HD44797E

The HD44797E is an evaluation chip for 4-bit single-chip microcomputer LCD-III/IV. The HD44797E has the same logical functions as LCD-III/IV except that its ROM is external. All I/O pins are open drain.

The HD44797E provides 12-bit address outputs (A_0 to A_{11} terminals) and 5-bit instruction input pins (O_1/O_5 to O_6/O_{10} pins) for the external program memory. ϕ and TSTP pins are required for debugging programs, and SELECT pin for selecting applicable chips.

■ APPLICABLE CHIPS

LCD-III, LCD-IV

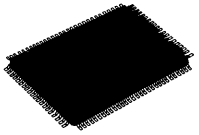
■ FUNCTION

- Instruction Characteristics etc.; Same as LCD-III, LCD-IV
- Address External ROM (4k)
- I/O Pins (D, R, INT_0, INT_1); Open Drain

■ PIN NAME

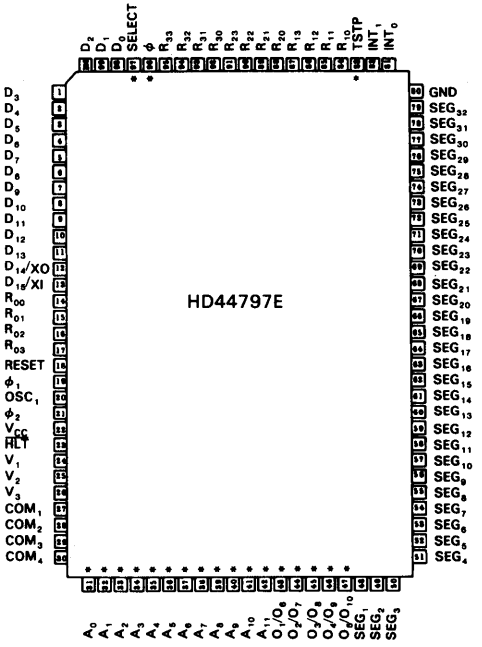
V_1, V_2, V_3	: Power Supply for LCD
OSC_1	: External Clock Input Pin
$\overline{HLT}$	: Halt Pin
R_{00} to R_{03}	: Input Port
R_{10} to R_{23}	: I/O Port
R_{30} to R_{33}	: Output Port
D_0 to D_{13}	: I/O Port
D_{14}/XO, D_{15}/XI	: I/O Port or Clock Input Pin for Timer
INT_0, INT_1	: Interrupt
COM_1 to COM_4	: Common Signal Pin
SEG_1 to SEG_{32}	: Segment Signal Pin
A_0 to A_{11}	: Program Memory Access Pin
O_1/O_6 to O_5/O_{10}	: Instruction Input Pin
ϕ, ϕ_1, ϕ_2	: Clock Signal
TSTP	: Timer/Prescaler Stop Signal Pin
SELECT	: Applicable Chips Selecting Pin

HD44797E



(FP-100)

■ PIN ARRANGEMENT



(Note) * : Additional pin for evaluation chip.

(Top View)

NEW DEVICES

HMCS404AC (HD614048)

The HMCS404AC is a CMOS 4-bit single-chip microcomputer which is a member of the HMCS400 series.

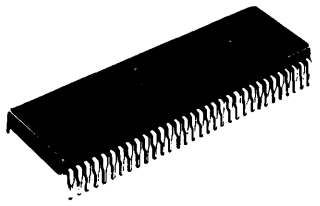
The HMCS404AC is a high speed version of the HMCS404C.

The HMCS404AC has efficient and powerful architecture and its software is very similar to the HMCS40 series.

This microcomputer provides variety of on-chip resources such as ROM, RAM, I/O, two timer/counters and a serial interface to perform in wide users' applications.

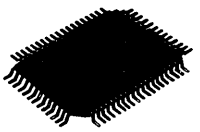
The HMCS404AC also has the characteristics of high speed and low power dissipation and which I/O pins are able to drive fluorescent display tube directly.

HMCS404AC



(DP-64S)

HMCS404AC



(FP-64)

■ HARDWARE FEATURES

- 4-bit Architecture
- 4,096 Words x 10-bit ROM
- 256 Digits x 4-bit RAM
- 58 I/O Pins, including 26 high voltage I/O pins (40V Max)
- Two Timer/Counters
  - 11-bit Prescaler
  - 8-bit Free Running Timer
  - 8-bit Auto-Reload Timer/Event Counter
- Clock Synchronous 8-bit Serial Interface
- Five Interrupt Sources

External	2
Timer/Counter	2
Serial Interface	1

- Subroutine Stack
  - Up to 16 levels including interrupts
- High Speed Operation
  - Minimum Instruction Execution Time — 1.33 μs
- Two Low Power Dissipation Modes
  - Standby — Stops instruction execution while keeping clock oscillation and interrupt functions in operation.
  - Stop — Stops instruction execution and clock oscillation while retaining RAM data
- On-Chip Oscillator
  - External Connection of Crystal or Ceramic Filter (externally drivable)

■ SOFTWARE FEATURES

- Instruction Set Similar to and More Powerful than HMCS40 Series; 99 Instructions
- High Programming Efficiency with 10-bit ROM/Word; 79 instructions are single word instructions
- Direct Branch to All ROM Area
- Direct or Indirect Addressing to All RAM Area
- Subroutine Nesting Up to 16 Levels Including Interrupts
- Binary and BCD Arithmetic Operation
- Powerful Logical Arithmetic Operation
- Pattern Generation — Table Look Up Capability —
- Bit Manipulation for Both RAM and I/O

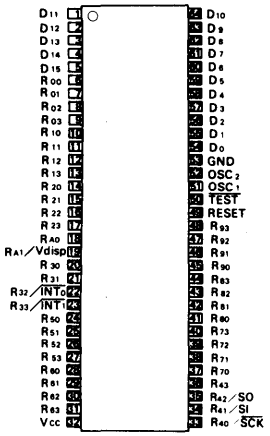
■ VERSATILE PROGRAM DEVELOPMENT SUPPORT TOOLS

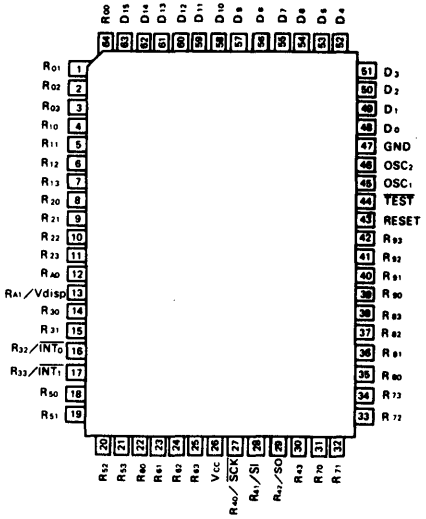
- H68SD Series Macro Assembler
- H68SD5-use Emulator (With Real Time Trace Function)
- EPROM On Package Microcomputer

Mask options are fixed as follows:

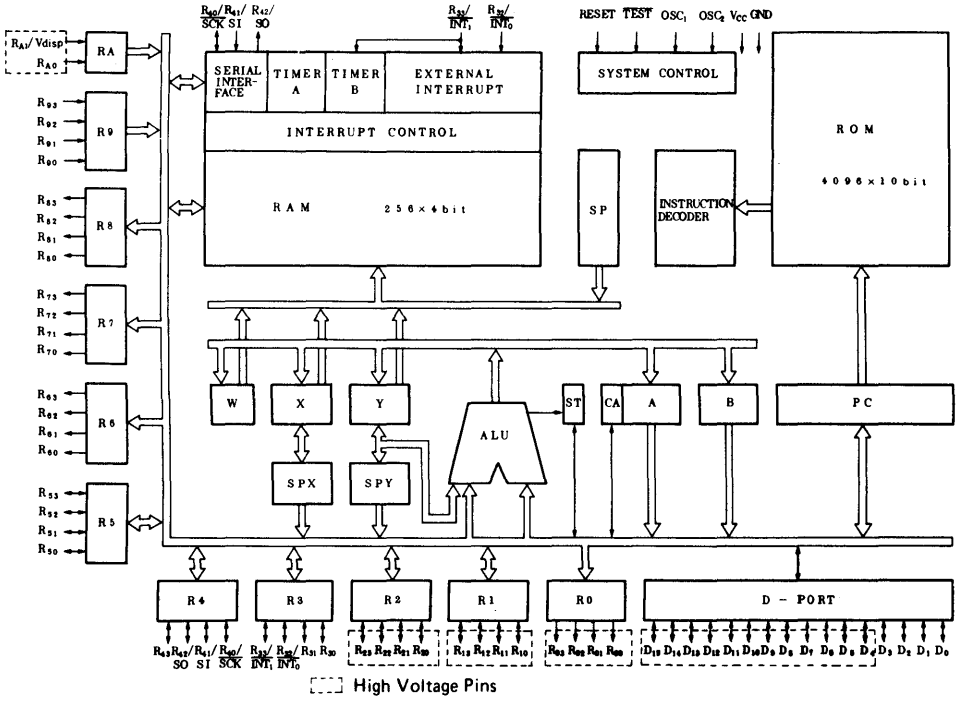
- I/O pin : Open drain
- Oscillator : Crystal Oscillator or Ceramic Filter Oscillator (externally drivable)
- Divider : Divided-by-8

■ PIN ARRANGEMENT (Top View)





■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	−0.3 to +7.0	V	
Terminal Voltage	V_T	−0.3 to V_{CC} +0.3	V	3
		V_{CC} −45 to V_{CC} +0.3	V	4
Total Allowance of Input Currents	ΣI_O	50	mA	5
Total Allowance of Output Currents	$-\Sigma I_O$	150	mA	6
Maximum Input Current	I_O	15	mA	7, 8
Maximum Output Current	$-I_O$	4	mA	9, 10
		6	mA	9, 11
		30	mA	9, 12
Operating Temperature	T_{opr}	−20 to +75	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

(Note 1) Permanent damage may occur if "Absolute Maximum Ratings" are exceeded. Normal operation should be under the conditions of "Electrical Characteristics". If these conditions are exceeded, it may cause the malfunction and affect the reliability of LSI.
(Note 2) All voltages are with respect to GND.
(Note 3) Applied to standard pins.
(Note 4) Applied to high voltage pins.
(Note 5) Total allowance of input current is the total sum of input current which flow in from all I/O pins to GND simultaneously.
(Note 6) Total allowance of output current is the total sum of the output current which flow out from V_{CC} to all I/O pins simultaneously.
(Note 7) Maximum input current is the maximum amount of input current from each I/O pin to GND.
(Note 8) Applied to $D_0 \sim D_3$ and R3 ~ R8.
(Note 9) Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
(Note 10) Applied to $D_0 \sim D_3$ and R3 ~ R8.
(Note 11) Applied to R0 ~ R2.
(Note 12) Applied to $D_4 \sim D_{15}$.

■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS (V_{CC} = 4.5V to 6V, GND = 0V, V_{disp} = V_{CC}−40V to V_{CC}, Ta = −20 to +75°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$		0.7V_{CC}	–	V_{CC}+0.3	V	
		SI		0.7V_{CC}	–	V_{CC}+0.3	V	
		OSC_1		V_{CC}−0.5	–	V_{CC}+0.3	V	
Input "Low" Voltage	V_{IL}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$		-0.3	–	0.22V_{CC}	V	
		SI		-0.3	–	0.22V_{CC}	V	
		OSC_1		-0.3	–	0.5	V	
Output "High" Voltage	V_{OH}	$\overline{SCK}$, SO	$-I_{OH}$ = 1.0 mA	V_{CC}−1.0	–	–	V	
			$-I_{OH}$ = 0.01 mA	V_{CC}−0.3	–	–	V	
Output "Low" Voltage	V_{OL}	$\overline{SCK}$, SO	I_{OL} = 1.6 mA	–	–	0.4	V	
Input/Output Leakage Current	$\|I_{IL}\|$	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$ SI, SO, OSC_1	V_{in} = 0 V to V_{CC}	–	–	1	μA	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}	V_{CC} = 5 V f_{osc} = 6 MHz	–	–	3.0	mA	2, 6
Current Dissipation in Standby Mode	I_{SBY1}	V_{CC}	Maximum Logic Operation V_{CC} = 5 V f_{osc} = 6 MHz	–	–	1.8	mA	3, 6
	I_{SBY2}	V_{CC}	Minimum Logic Operation V_{CC} = 5 V f_{osc} = 6MHz	–	–	1.35	mA	4, 6
Current Dissipation in Stop Mode	I_{stop}	V_{CC}	V_{in} ($\overline{TEST}$) = V_{CC} −0.3 V to V_{CC} V_{in} (RESET) = 0V to 0.3 V	–	–	10	μA	5
Stop Mode Retain Voltage	V_{stop}	V_{CC}		2	–	–	V	

(Note 1) Pull-up MOS current and output buffer current are excluded.
(Note 2) The MCU is in the reset state. The input/output current does not flow.
Test Conditions: MCU state; • Reset state in Operation Mode
Pin state; • RESET, $\overline{TEST}$ ··· V_{CC} voltage
• D_0~D_3, R3~R9 ··· V_{CC} voltage
• D_4~D_{15}, R0~R2, R_{A0}, R_{A1} ··· V_{disp} voltage
(Note 3) The timer/counter operate with the fastest clock and input/output current does not flow.
Test Conditions: MCU state; • Standby Mode
• Input/Output; Reset state
• TIMER-A; ÷2 prescaler divide ratio
• TIMER-B; ÷2 prescaler divide ratio
• SERIAL Interface ; Stop
Pin state; • RESET ···GND voltage
• $\overline{TEST}$ ··· V_{CC} voltage
• D_0~D_3, R3~R9 ··· V_{CC} voltage
• D_4~D_{15}, R0~R2, R_{A0}, R_{A1} ··· V_{disp} voltage
(Note 4) The timer/counter operate with the slowest clock and input/output current does not flow.
Test Conditions: MCU state; • Standby Mode
• Input/Output; Reset state
• TIMER-A; ÷2048 prescaler divide ratio
• TIMER-B; ÷2048 prescaler divide ratio
• SERIAL Interface ; Stop
Pin state; • RESET ··· GND voltage
• $\overline{TEST}$ ··· V_{CC} voltage
• D_0~D_3, R3~R9 ··· V_{CC} voltage
• D_4~D_{15}, R0~R2, R_{A0}, R_{A1} ··· V_{disp} voltage
(Note 5) Pull-down MOS current is excluded.
(Note 6) When $f_{osc}=x$ [MHz], the Current Dissipation in Operation mode and Standby mode are estimated as follows:

$$\text{max. value } (f_{osc}=x\,[\text{MHz}]) = \frac{x}{6} \times \text{max. value } (f_{osc}=6\,[\text{MHz}])$$

• INPUT/OUTPUT CHARACTERISTICS FOR STANDARD PIN

(V_{CC} = 4.5V to 6V, GND = 0V, V_{disp} = V_{CC}−40V to V_{CC}, Ta = −20 to +75°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	D_0 ~ D_3, R3 ~ R5, R9		0.7V_{CC}	–	V_{CC}+0.3	V	
Input "Low" Voltage	V_{IL}	D_0 ~ D_3, R3 ~ R5, R9		−0.3	–	0.22V_{CC}	V	
Output "High" Voltage	V_{OH}	D_0 ~ D_3, R3 ~ R8	$-I_{OH}$ = 1.0 mA	V_{CC}−1.0	–	–	V	1
		D_0 ~ D_3, R3 ~ R8	$-I_{OH}$ = 0.01 mA	V_{CC}−0.3	–	–	V	1
Output "Low" Voltage	V_{OL}	D_0 ~ D_3, R3 ~ R8	I_{OL} = 1.6 mA	–	–	0.4	V	
Input/Output Leakage Current	$\|I_{IL}\|$	D_0 ~ D_3, R3 ~ R9	V_{in} = 0V to V_{CC}	–	–	1	μA	2
Pull-Up MOS Current	$-I_p$	D_0 ~ D_3, R3 ~ R9	V_{CC} = 5V, V_{in} = 0V	30	60	120	μA	3

(Note 1) Applied to I/O pins with "CMOS" Output selected by mask option.
(Note 2) Pull-up MOS current and output buffer current are excluded.
(Note 3) Applied to I/O pins "with Pull-up MOS" selected by mask option.

- **INPUT/OUTPUT CHARACTERISTICS FOR HIGH VOLTAGE PIN**
  (V_{CC} = 4.5V to 6V, GND = 0V, V_{disp} = V_{CC}−40V to V_{CC}, Ta = −20 to +75°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	D_4 ~ D_{15}, R1 R2, R_{A0}, R_{A1}		0.7V_{CC}	–	V_{CC}+0.3	V	
Input "Low" Voltage	V_{IL}	D_4~D_{15} , R1 R2, R_{A0}, R_{A1}		V_{CC}−40	–	0.22V_{CC}	V	
Output "High" Voltage	V_{OH}	D_4 ~ D_{15}	$-I_{OH}$=15mA, V_{CC}=5V ± 10%	V_{CC}−3.0	–	–	V	
			$-I_{OH}$=9mA	V_{CC}−2.0	–	–	V	
		R0 ~ R2	$-I_{OH}$=3mA, V_{CC}=5V ± 10%	V_{CC}−3.0	–	–	V	
			$-I_{OH}$=1.8 mA	V_{CC}−2.0	–	–	V	
Output "Low" Voltage	V_{OL}	D_4~D_{15} R0~R2	V_{disp} = V_{CC}−40V	–	–	V_{CC}−37	V	1
		D_4~D_{15} R0~R2	150kΩ to V_{CC}−40V	–	–	V_{CC}−37	V	2
Input/Output Leakage Current	$\|I_{IL}\|$	D_4~D_{15} R0~R2 R_{A0}, R_{A1}	V_{in} = V_{CC}−40V to V_{CC}	–	–	20	μA	3
Pull Down MOS Current	I_d	D_4~D_{15} R0~R2 R_{A0}, R_{A1}	V_{disp} = V_{CC}−35V V_{in} = V_{CC}	125	250	500	μA	4

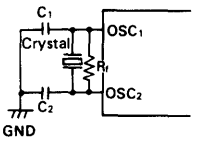
(Note 1) Applied to I/O pins "with Pull-down MOS" selected by mask option.
(Note 2) Applied to I/O pins "without Pull-down MOS (PMOS Open Drain)" selected by mask option.
(Note 3) Pull-down MOS current and output buffer current are excluded.
(Note 4) Applied to I/O pins "with Pull-down MOS" selected by mask option.

- **AC CHARACTERISTICS (V_{CC}=4.5V to 6V, GND = 0V, V_{disp} = V_{CC}−40V to V_{CC}, Ta = −20 to +75°C, if not specified.)**

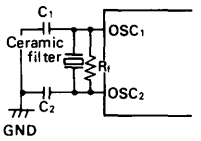
Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Oscillation Frequency	f_{osc}	OSC_1, OSC_2		0.4	6	6.2	MHz	
Instruction Cycle Time	t_{cyc}			1.29	1.33	20	μs	
Oscillator Stabilization Time	t_{RC}	OSC_1, OSC_2		–	–	20	ms	1
External Clock "High" Level Width	t_{CPH}	OSC_1		70	–	–	ns	2
External Clock "Low" Level Width	t_{CPL}	OSC_1		70	–	–	ns	2
External Clock Rise Time	t_{CPr}	OSC_1		–	–	20	ns	2
External Clock Fall Time	t_{CPf}	OSC_1		–	–	20	ns	2
$\overline{INT_0}$ "High" Level Width	t_{I0H}	$\overline{INT_0}$		2	–	–	t_{cyc}	3
$\overline{INT_0}$ "Low" Level Width	t_{I0L}	$\overline{INT_0}$		2	–	–	t_{cyc}	3
$\overline{INT_1}$ "High" Level Width	t_{I1H}	$\overline{INT_1}$		2	–	–	t_{cyc}	3
$\overline{INT_1}$ "Low" Level Width	t_{I1L}	$\overline{INT_1}$		2	–	–	t_{cyc}	3
RESET "High" Level Width	t_{RSTH}	RESET		2	–	–	t_{cyc}	4
Input Capacitance	C_{in}	all pins	f = 1 MHz V_{in} = 0 V	–	–	15	pF	
RESET Fall Time	t_{RSTf}			–	–	20	ms	4

(Note 1) Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 4.5V at "Power-on", or after RESET input level goes "High" by resetting to quit the stop mode by MCU reset. The circuits used to measure the value are described below. When using crystal or ceramic filter oscillator, please ask a crystal oscillator maker's or ceramic filter maker's advice because oscillator stabilization time depends on the circuit constant and stray capacity.

Crystal oscillator



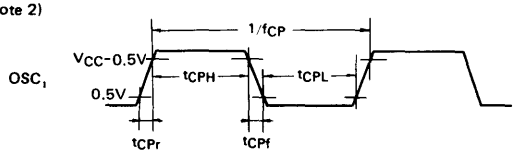
Ceramic filter oscillator



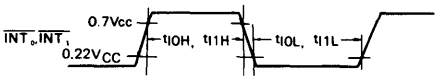
Crystal: 6.0MHz NC-18C (Nihon Denpa Kogyo)
Rf : 1MΩ ±2%
C_1 : 20pF ±20%
C_2 : 20pF ±20%

Ceramic filter : CSA6.00MG (Murata)
Rf : 1MΩ ±2%
C_1 : 30pF ±20%
C_2 : 30pF ±20%

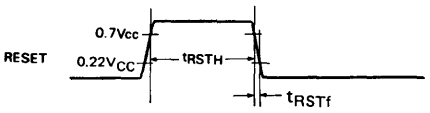
(Note 2)



(Note 3)



(Note 4)



• SERIAL INTERFACE TIMING CHARACTERISTICS

(V_{CC}=4.5V to 6V, GND = 0V, V_{disp} = V_{CC}−40V to V_{CC}, Ta = −20 to +75°C, if not specified.)

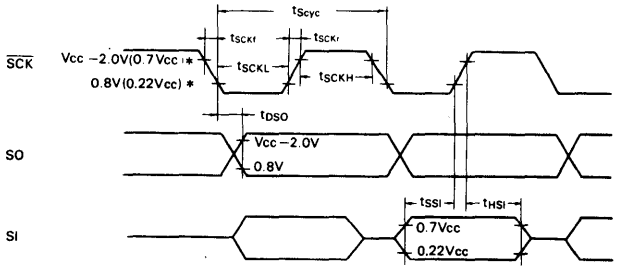
- At Transfer Clock Output

Item	Symbol	Pin Name	Test Conditions	Value min	Value typ	Value max	Unit	Note
Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$	(Note 2)	1	–	–	t_{cyc}	1, 2
Transfer Clock "High" Level Width	t_{SCKH}	$\overline{SCK}$	(Note 2)	0.5	–	–	t_{Scyc}	1, 2
Transfer Clock "Low" Level Width	t_{SCKL}	$\overline{SCK}$	(Note 2)	0.5	–	–	t_{Scyc}	1, 2
Transfer Clock Rise Time	t_{SCKr}	$\overline{SCK}$	(Note 2)	–	–	100	ns	1, 2
Transfer Clock Fall Time	t_{SCKf}	$\overline{SCK}$	(Note 2)	–	–	100	ns	1, 2
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	–	–	250	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		300	–	–	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		150	–	–	ns	1

- At Transfer Clock Input

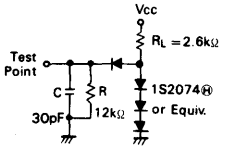
Item	Symbol	Pin Name	Test Conditions	Value min	Value typ	Value max	Unit	Note
Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$		1	–	–	t_{cyc}	1
Transfer Clock "High" Level Width	t_{SCKH}	$\overline{SCK}$		0.5	–	–	t_{Scyc}	1
Transfer Clock "Low" Level Width	t_{SCKL}	$\overline{SCK}$		0.5	–	–	t_{Scyc}	1
Transfer Clock Rise Time	t_{SCKr}	$\overline{SCK}$		–	–	100	ns	1
Transfer Clock Fall Time	t_{SCKf}	$\overline{SCK}$		–	–	100	ns	1
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	–	–	250	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		300	–	–	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		150	–	–	ns	1

(Note 1) Timing Diagram of Serial Interface

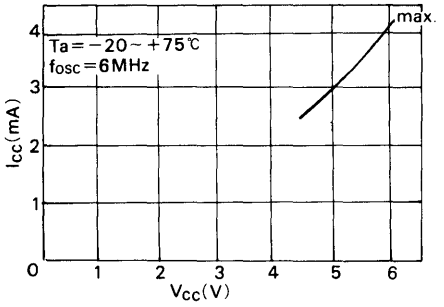


* V_{CC} − 2.0V and 0.8V are the threshold voltage for transfer clock output.
0.7 V_{CC} and 0.22 V_{CC} are the threshold voltage for transfer clock input.

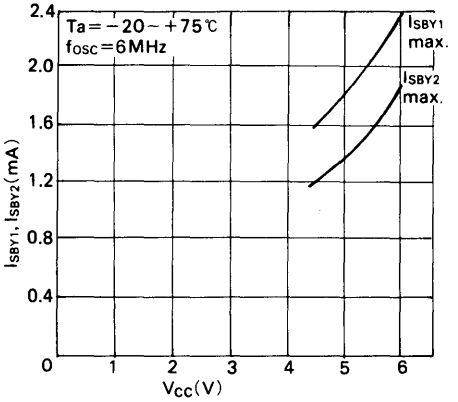
(Note 2) Timing Load Circuit



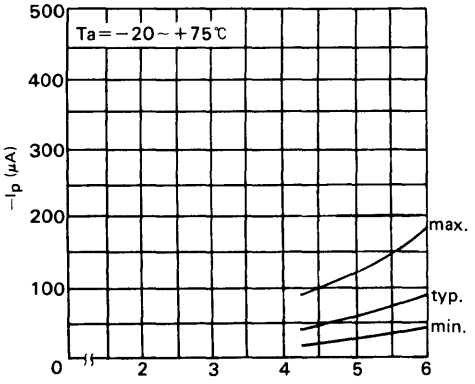
■ CHARACTERISTICS CURVE (REFERENCE DATA)



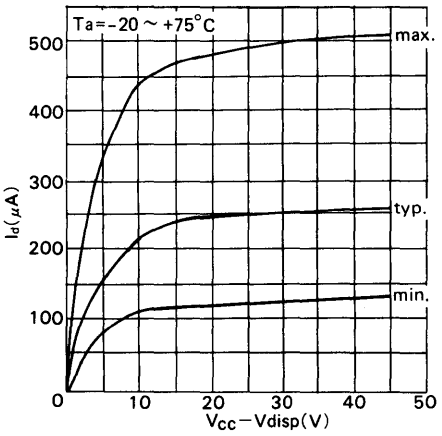
I_{CC} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator)



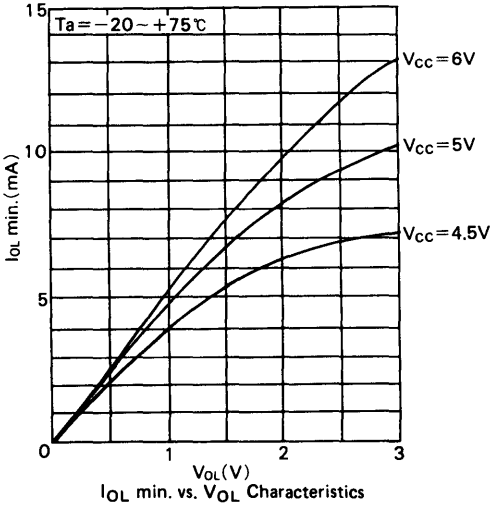
I_{SBY} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator)



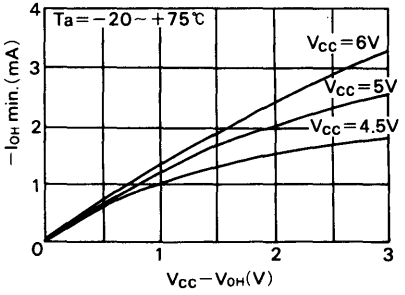
$-I_p$ (Pull-up MOS Current) vs.
V_{CC} Characteristics



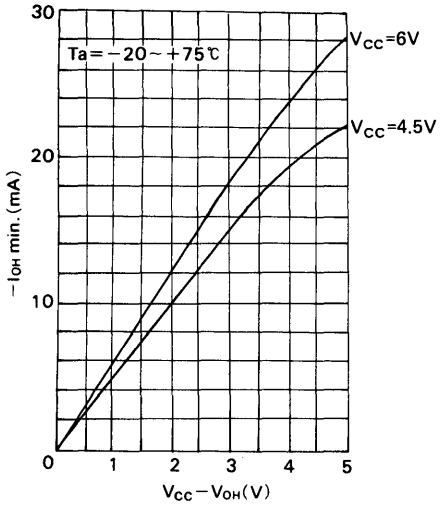
I_d (Pull-down MOS Current) vs.
(V_{CC} − V_{disp}) Characteristics



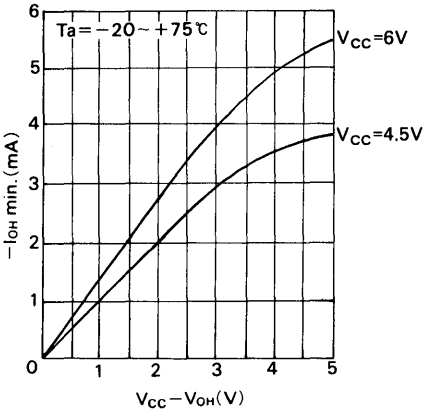
I_{OL} min. vs. V_{OL} Characteristics
(Standard Pin)



$-I_{OH}$ min vs. (V_{CC} − V_{OH}) Characteristics
(Standard Pin "CMOS")



$-I_{OH}$ min. vs. (V_{CC} − V_{OH}) Characteristics (D_4 ~ D_{15} Pins)



$-I_{OH}$ min. vs. (V_{CC} − V_{OH}) Characteristics (RO ~ R2 Pins)

■ DESCRIPTION OF PIN FUNCTIONS

Input and output signals of MCU are described below.

• GND, V_{CC}, V_{disp}

These are Power Supply Pins. Connect GND pin to Earth (0V) and apply V_{CC} power supply voltage to V_{CC} pin. V_{disp} is an power supply for high voltage Input/Output pins with maximum voltage of V_{CC}-40V. V_{disp} pin can be also used as R_{A1} pin by mask option. For details, see "INPUT/OUTPUT".

• $\overline{TEST}$

$\overline{TEST}$ pin is not for user's application. $\overline{TEST}$ must be connected to V_{CC}.

• RESET

RESET pin is used to reset MCU. For details, see "RESET".

• OSC_1, OSC_2

These are Input pins to the internal oscillator circuit. They can be connected to crystal, or ceramic filter resonator. For details, see "INTERNAL OSCILLATOR CIRCUIT."

• D-port (D_0 to D_{15})

D-port is a 1-bit Input/Output common port. D_0 to D_3 are standard type, D_4 to D_{15} are for high voltage. Each pin has the mask option to select its circuit type. For details, See "INPUT/OUTPUT".

• R-port (R0 to RA)

R-port is a 4-bit Input/Output port. (only RA is 2-bit construction.) R0 and R6 to R8 are output ports, R9 to RA are input ports, and R1 to R5 are Input/Output common ports. R0 to R2 and RA are the high voltage ports, R3 to R9 are the standard ports. Each pin has the mask option to select its circuit type. R_{32}, R_{33}, R_{40}, R_{41} and R_{42} are also available as $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK}$, SI and SO respectively. For details, see "INPUT/OUTPUT".

• $\overline{INT_0}$, $\overline{INT_1}$

These are the input pins to interrupt MCU operation externally. $\overline{INT_1}$ can be used as an external event input pin for TIMER-B. $\overline{INT_0}$ and $\overline{INT_1}$ are also available as R_{32}, and R_{33} respectively. For details, See "INTERRUPT".

• $\overline{SCK}$, SI, SO

These are Transfer clock I/O pin ($\overline{SCK}$), serial data input pin (SI) and serial data output pin (SO) used for serial interface. $\overline{SCK}$, SI, and SO are also available as R_{40}, R_{41} and R_{42} respectively. For details, see "SERIAL INTERFACE".

■ ROM MEMORY MAP

MCU includes 4096 words × 10 bits ROM. ROM memory map is illustrated in Fig. 1 and described in the following paragraph.

• Vector Address Area ..... $0000 to $000F

When MCU is reset or an interrupt is serviced, the program is executed from the vector address. Program the JMPL instructions branching to the starting addresses of reset routine or of interrupt routines.

• Zero-Page Subroutine Area ..... $0000 to $003F

CAL instruction allows to branch to the subroutines in $0000 to $003F.

• Pattern Area ..... $0000 to $0FFF

P instruction allows referring to the ROM data in $0000 to $0FFF as a pattern.

• Program Area ..... $0000 to $0FFF

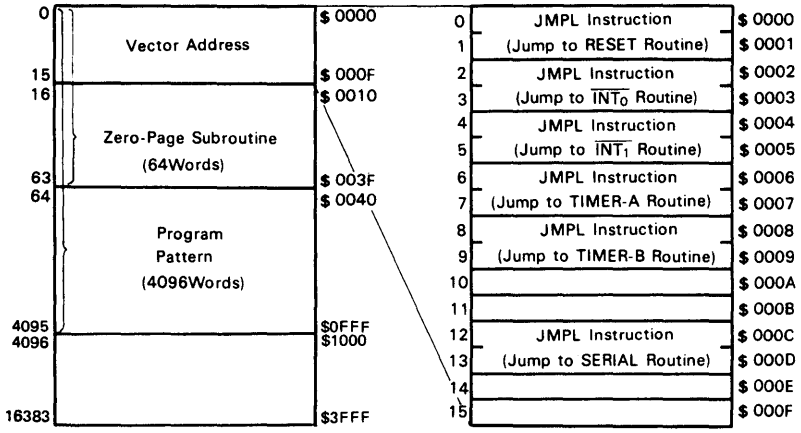
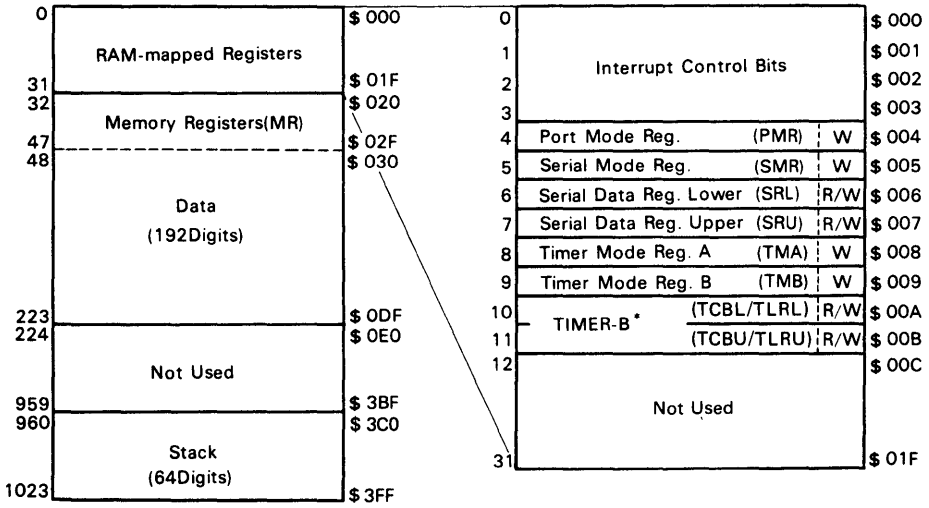


Fig. 1 ROM Memory Map

■ RAM MEMORY MAP

MCU includes 256 digits × 4 bits RAM as the data area and stack area. In addition to these areas, interrupt control bits and special registers are also mapped on the RAM memory space. RAM memory map is illustrated in Fig. 2 and described in the following paragraph.



* Two registers are mapped on same address.

R :Read Only
W :Write Only
R/W:Read/Write

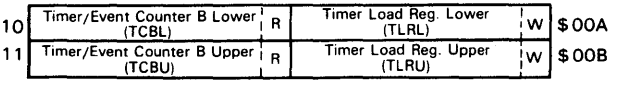


Fig. 2 RAM Memory Map

	bit 3	bit 2	bit 1	bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP Bit)	I/E (Interrupt Enable Flag)	$000
1	IMTA (IM of TIMER-A)	IFTA (IF of TIMER-A)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	Not Used	Not Used	IMTB (IM of TIMER-B)	IFTB (IF of TIMER-B)	$002
3	Not Used	Not Used	IMS (IM of SERIAL)	IFS (IF of SERIAL)	$003

IF : Interrupt Request Flag
IM : Interrupt Mask
I/E : Interrupt Enable Flag
SP : Stack Pointer

(Note) Each bit in Interrupt Control Bits Area is set by SEM/SEMD instruction, is reset by REM/REMD instruction and is tested by TM/TMD instruction. It is not affected by other instructions. Furthermore, Interrupt Request Flag is not affected by SEM/SEMD instruction. The content of Status becomes invarid when "Not Used" bit is tested.

Fig. 3 Configuration of Interrupt Control Bit Area

- **Interrupt Control Bit Area ..... $000 to $003**

This area is used for interrupt controls, and is illustrated in Fig.3. It is accessable only by RAM bit manipulation instruction. However, the interrupt request flag cannot be set by software.

- **Special Register Area ..... $004 to $00B**

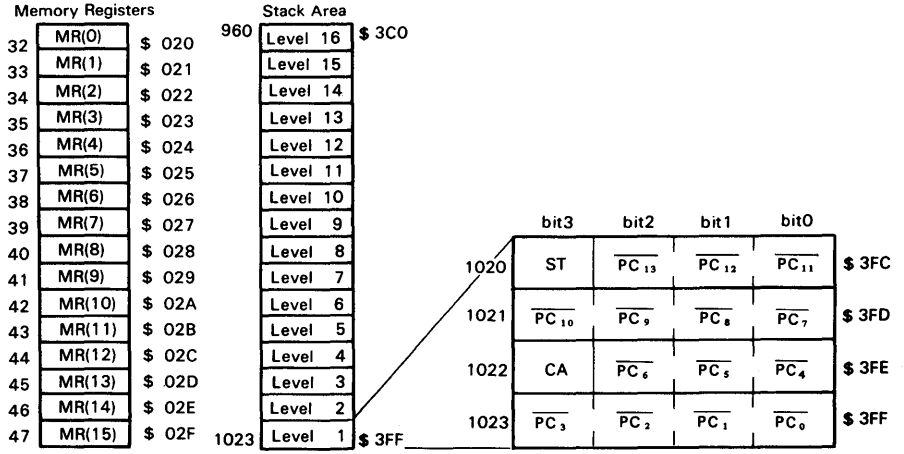
Special Register is a mode or a data register for the external interrupt, the serial interface, and the timer/counter. These registers are classified into 3 types: Write-only, Read-only, and Read/Write as shown in Fig. 2. These registers cannot be accessed by RAM bit manipulation instruction.

- **Data Area ..... $020 to $0DF**

16 digits of $020 to $02F are called memory register (MR) and accessable by LAMR and XMRA instructions.

- **Stack Area .... $3C0 to $3FF**

Stack Area is used for LIFO stacks with the contents of the program counter (PC), status (ST) and carry (CA) when processing subroutine call and interrupt. As 1 level requires 4 digits, this stack area is nested to 16 level-stack max. The data pushed in the stack and LIFO stack state are provided in Fig. 4. The program counter is restored by RTN and RTNI instructions. Status and Carry are restored only by RTNI instruction. The area, not used for stacking, is available as a data area.



PC_{13} to PC_0 ; Program Counter
ST; Status
CA; Carry

Fig. 4 Configuration of Memory Register, Stack Area and Stack Position

■ REGISTER AND FLAG

The MCU has nine registers and two flags for the CPU operations. They are illustrated in Fig. 5 and described in the following paragraphs.

- **Accumulator (A), B Register (B)**

Accumulator and B Register are 4-bit registers used to hold the results of Arithmetic Logic Unit (ALU), and to transfer data to/from memories, I/O and other registers.

- **W Register (W), X Register (X), Y Register (Y)**

W Register is 2-bit, and X and Y Register are 4-bit registers used for indirect addressing of RAM. Y register is also used for D-port addressing.

- **SPX Register (SPX), SPY Register (SPY)**

SPX and SPY Register are 4-bit registers used to assist X and Y Register respectively.

- **Carry (CA)**

Carry (CA) stores the overflow of ALU generated by the arithmetic operation. It is also affected by SEC, REC, ROTL and ROTR instructions.

During interrupt servicing, Carry is pushed onto the stack and restored back from the stack by RTNI instruction. (It's not affected by RTN instruction.)

- **Status (ST)**

Status (ST) holds the ALU overflow, ALU non-zero and the results of bit test instruction for the arithmetic or compare instruction. It is used for a branch condition of BR, BRL, CAL or CALL instructions. The value of the Status remains unchanged until the next arithmetic, compare or bit test instruction is executed. Status becomes "1" after the BR, BRL, CAL or CALL instruction has been executed (irrespective of its execution/skip). During the interrupt servicing, Status is pushed onto the stack and restored back from the stack by RTNI instruction. (It's not affected by RTN instruction.)

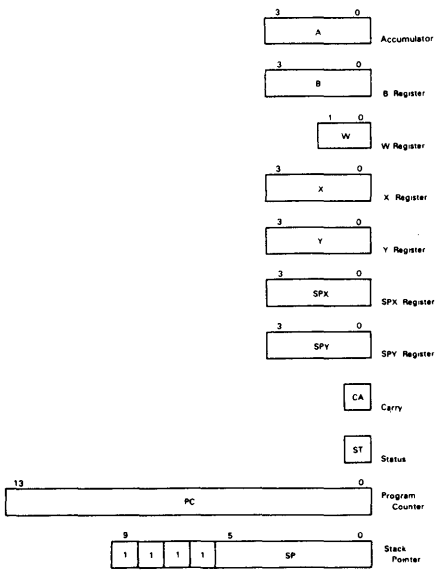


Fig. 5 Register and Flags

- **Program Counter (PC)**

Program Counter is a 14-bit binary counter for ROM addressing.

- **Stack Pointer (SP)**

Stack Pointer is used to point the address of the next stacking area up to 16 levels.

The Stack Pointer is initialized to locate $3FF on the RAM address, and is decremented by 4 as data pushed into the stack, and incremented by 4 as data restored back from the stack.

■ INTERRUPT

The MCU can be interrupted by five different sources: the external signals ($\overline{INT_0}$, $\overline{INT_1}$), timer/counter (TIMER-A, TIMER-B), and serial interface (SERIAL). In each sources, the Interrupt Request Flag, Interrupt Mask and interrupt vector address will be used to control and maintain the interrupt request. The Interrupt Enable Flag is also used to control the total interrupt operations.

- **Interrupt Control Bit and Interrupt Service**

The interrupt control bit is mapped on $000 to $003 of the RAM address and accessable by RAM bit manipulation instruction. (The Interrupt Request Flag (IF) cannot be set by software.) The Interrupt Enable Flag (I/E) and Interrupt Request Flag (IF) are set to "0", and the Interrupt Mask (IM) is set to "1" at the initialization by MCU reset.

Fig. 6 shows the interrupt block diagram. Table 1 shows the interrupt priority and vector addresses, and Table 2 shows the conditions that the interrupt service is executed by any one of the five interrupt sources.

The interrupt request is generated when the Interrupt Request Flag is set to "1" and the Interrupt Mask is "0". If the Interrupt Enable Flag is "1", then the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the five interrupt sources.

Fig. 7 shows the interrupt services sequence, and Fig. 8 shows the interrupt flowchart. If the interrupt is requested, the instruction finishes its execution in the first cycle. The Interrupt Enable Flag is reset in the second cycle. In the second and third cycles, the Carry, Status and Program Counter are pushed onto the stack. In the third cycle, the instruction is executed again after jumping to the vector address.

In each vector address, program JMPL instruction to branch to a starting address of the interrupt routine. The Interrupt Request Flag which caused the interrupt service has to be reset by software in the interrupt routine.

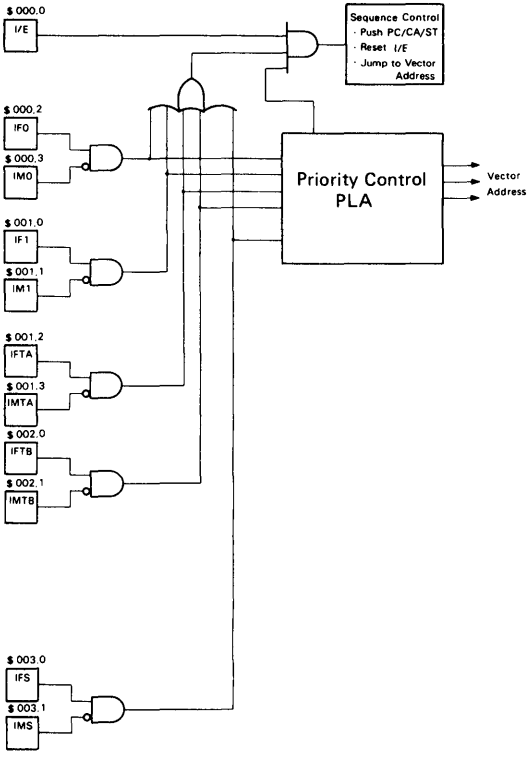


Fig. 6 Interrupt Circuit Block Diagram

Table 1. Vector Addresses and Interrupt Priority

Reset · Interrupt	Priority	Vector addresses
RESET	–	$0000
$\overline{INT_0}$	1	$0002
$\overline{INT_1}$	2	$0004
TIMER-A	3	$0006
TIMER-B	4	$0008
SERIAL	5	$000C

Table 2. Conditions of Interrupt Service

Interrupt source / Interrupt control bits	$\overline{INT_0}$	$\overline{INT_1}$	TIMER-A	TIMER-B	SERIAL
I/E	1	1	1	1	1
IF0·$\overline{IM0}$	1	0	0	0	0
IF1 · $\overline{IM1}$	*	1	0	0	0
IFTA · $\overline{IMTA}$	*	*	1	0	0
IFTB · $\overline{IMTB}$	*	*	*	1	0
IFS · $\overline{IMS}$	*	*	*	*	1

* Don't care

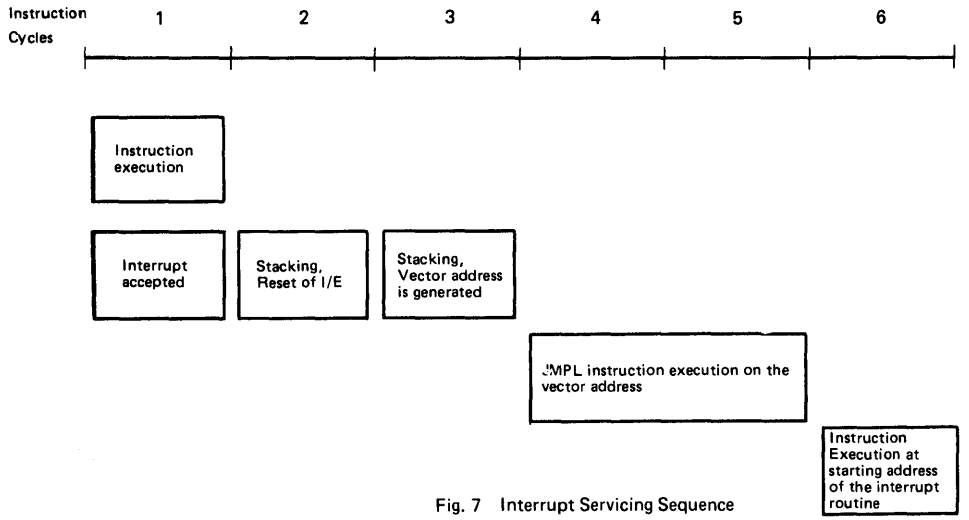


Fig. 7 Interrupt Servicing Sequence

- **Interrupt Enable Flag (I/E: $000,0)**

The Interrupt Enable Flag controls enable/disable of all interrupt requests as shown in Table 3. The Interrupt Enable Flag is reset by the interrupt servicing and set by RTNI instruction.

Table 3. Interrupt Enable Flag

Interrupt Enable Flag	Interrupt Enable/Disable
0	Disable
1	Enable

- **External Interrupt ($\overline{INT_0}$, $\overline{INT_1}$)**

To use external interrupt, select $R_{32}/\overline{INT_0}$, $R_{33}/\overline{INT_1}$ port for $\overline{INT_0}$, $\overline{INT_1}$ mode by setting the Port Mode Register (PMR: $004).

The External Interrupt Request Flags (IF0, IF1) are set at the falling edge of $\overline{INT_0}$, $\overline{INT_1}$ inputs.

$\overline{INT_1}$ input can be used as a clock signal input of TIMER-B. Then, TIMER-B counts up at each falling edge of input. When using $\overline{INT_1}$ as TIMER-B external event, an External Interrupt Mask (IM1) has to be set so that the interrupt request by $\overline{INT_1}$ will not be accepted.

- **External Interrupt Request Flag (IF0: $000,2, IF1: $001,0)**

The External Interrupt Request Flags (IF0, IF1) are set at the falling edges of $\overline{INT_0}$, $\overline{INT_1}$ inputs respectively.

- **External Interrupt Mask (IM0: $000,3, IM1: $001,1)**

The External Interrupt Mask is used to mask the external interrupt requests.

Table 4. External Interrupt Request Flag

External Interrupt Request Flags	Interrupt Requests
0	No
1	Yes

Table 5. External Interrupt Mask

External Interrupt Masks	Interrupt Requests
0	Enable
1	Disable (masks)

- **Port Mode Register (PMR: $004)**

The Port Mode Register is a 4-bit write-only register which controls the $R_{32}/\overline{INT_0}$ pin, $R_{33}/\overline{INT_1}$ pin, R_{41}/SI pin and R_{42}/SO pin as shown in Table 6. The Port Mode Register will be initialized to $0 by MCU reset, so that all these pins are set to a port mode.

Table 6. Port Mode Register

PMR bit 3	$R_{33}/\overline{INT_1}$ pin
0	Used as R_{33} port input/output pin
1	Used as $\overline{INT_1}$ input pin

PMR bit 2	$R_{32}/\overline{INT_0}$ pin
0	Used as R_{32} port input/output pin
1	Used as $\overline{INT_0}$ input pin

PMR bit 1	R_{41}/SI pin
0	Used as R_{41} port input/output pin
1	Used as SI input pin

PMR bit 0	R_{42}/SO pin
0	Used as R_{42} port input/output pin
1	Used as SO output pin

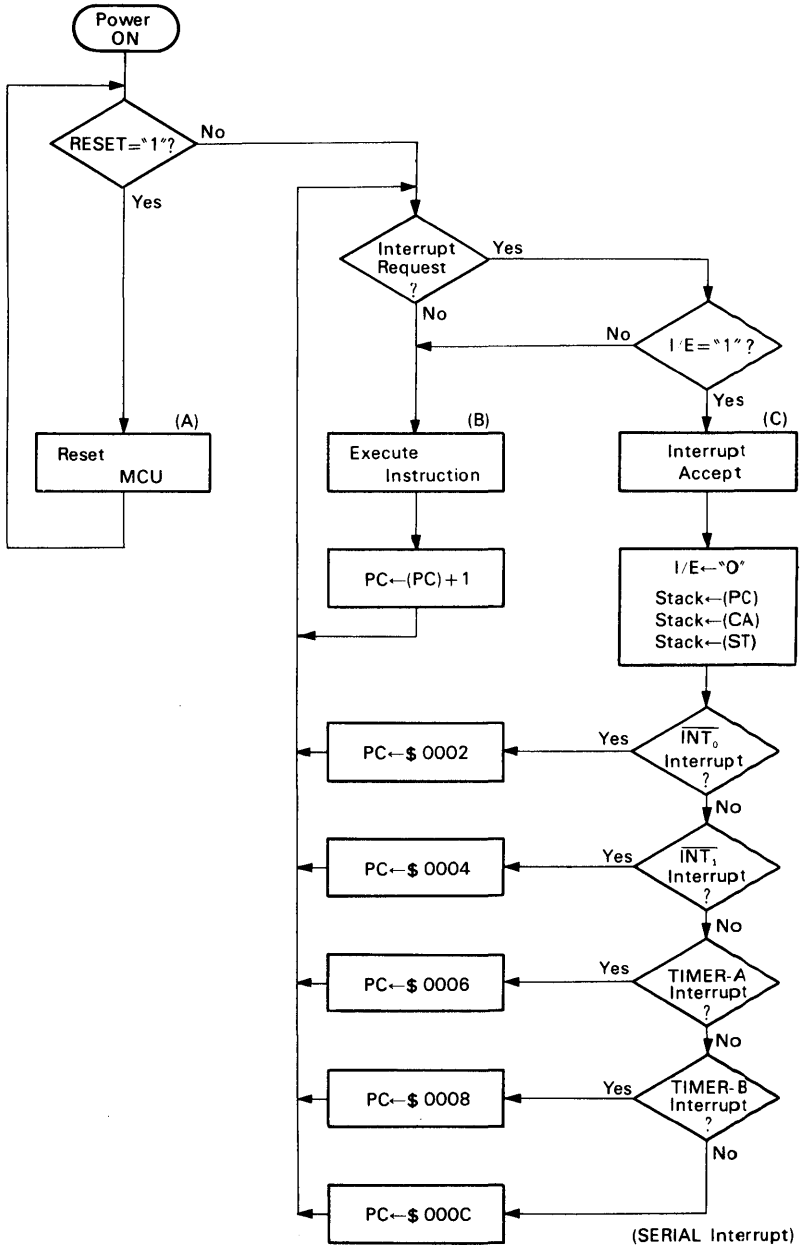


Fig. 8 Interrupt Servicing Flowchart

■ SERIAL INTERFACE

The serial interface is used to transmit/receive 8-bit data serially. This consists of the Serial Data Register, the Serial Mode Register, the Octal Counter and the multiplexer, as illustrated in Fig. 9. Pin $R_{40}/\overline{SCK}$ and the transfer clock signal are controlled by the Serial Mode Register. Contents of the Serial Data Register can be written into or read out by the software. The data in the Serial Data Register can be shifted synchronously with the transfer clock signal.

The serial interface operation is initiated with STS instruction. The Octal Counter is reset to $0 by STS instruction. It starts to count at the falling edge of the transfer clock ($\overline{SCK}$) signal and increments by one at the rising edge of the $\overline{SCK}$. When the Octal Counter is reset to $0 after eight transfer clock signals, or discontinued transmit/receive operation by resetting the Octal Counter, the SERIAL Interrupt Request Flag will be set.

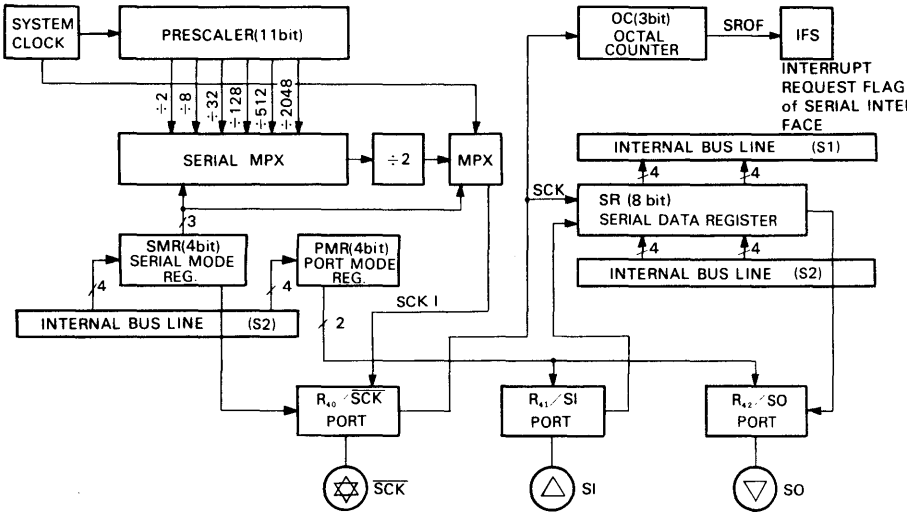


Fig. 9 Serial Interface Block Diagram

• Serial Mode Register (SMR: $005)

The Serial Mode Register is a 4-bit write-only register. This register controls the $R_{40}/\overline{SCK}$ and the prescaler divide ratio as the transfer clock source as shown in Table 7.

The Write Signal to the Serial Mode Register controls the operating state of serial interface.

The Write Signal to the Serial Mode Register stops the transfer clock applied to the Serial Data Register and the Octal Counter. And it also reset the Octal Counter to $0 simultaneously.

When the Serial Interface is in the "Transfer State", the Write Signal to the Serial Mode Register causes to quit the data transfer and to set the SERIAL Interrupt Request Flag.

Contents of the Serial Mode Register will be changed on the second instruction cycle after writing into the Serial Mode Register. Therefore, it will be necessary to execute the STS instruction after the data in the Serial Mode Register has been changed completely. The Serial Mode Register will be reset to $0 by MCU reset.

• Serial Data Register (SRL: $006, SRU: $007)

The Serial Data Register is an 8-bit read/write register. It consists of a low-order digit (SRL:$006) and a high-order digit (SRU: $007).

The data in the Serial Data Register will be output from the LSB side at SO pin synchronously with the falling edge of the transfer clock signal. At the same time, external data will be input from the LSB side at SI pin to the Serial Data Register synchronously with the rising edge of the transfer clock. Fig. 10 shows the I/O timing chart for the transfer clock signal and the data.

The writing into/reading from the Serial Data Register during its shifting causes the validity of the data.

Therefore complete data transmit/receive before writing into/reading from the serial data register.

Table 7. Serial Mode Register

SMR Bit 3	$R_{40}/\overline{SCK}$
0	Used as R_{40} port input/output pin
1	Used as $\overline{SCK}$ input/output pin

SMR			Transfer Clock			
Bit 2	Bit 1	Bit 0	$R_{40}/\overline{SCK}$ Port	Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio
0	0	0	$\overline{SCK}$ Output	Prescaler	÷ 2048	÷ 4096
0	0	1	$\overline{SCK}$ Output	Prescaler	÷ 512	÷ 1024
0	1	0	$\overline{SCK}$ Output	Prescaler	÷ 128	÷ 256
0	1	1	$\overline{SCK}$ Output	Prescaler	÷ 32	÷ 64
1	0	0	$\overline{SCK}$ Output	Prescaler	÷ 8	÷ 16
1	0	1	$\overline{SCK}$ Output	Prescaler	÷ 2	÷ 4
1	1	0	$\overline{SCK}$ Output	System Clock	–	÷ 1
1	1	1	$\overline{SCK}$ Input	External Clock	–	–

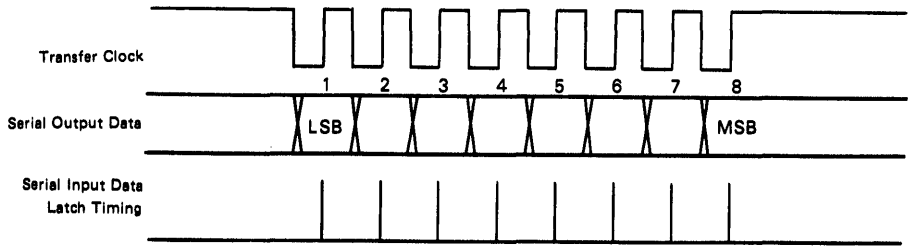


Fig. 10 Serial Interface I/O Timing Chart

- **SERIAL Interrupt Request Flag (IFS: $003, 0)**

The SERIAL Interrupt Request Flag will be set after the eight transfer clock signals or transmit/receive discontinued operation by resetting the Octal Counter.

- **SERIAL Interrupt Mask (IMS: $003, 1)**

The SERIAL Interrupt Mask masks the interrupt request.

Table 8. SERIAL Interrupt Request Flag

SERIAL Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 9. SERIAL Interrupt Mask

SERIAL Interrupt Mask	Interrupt Request
0	Enable
1	Disable (mask)

- **Selection of the Operation Mode**

Table 10 shows the operation mode of the serial interface. Select a combination of the value in the Port Mode Register and the Serial Mode Register according to Table 10.

Initialize the serial interface by the Write Signal to the Serial Mode Register, when the Operation Mode is changed.

- **Operating State of Serial Interface**

The serial interface has 3 operating states as shown in Fig. 11.

The serial interface gets into "STS waiting state" by 2 ways: one way is to change the operation mode by changing the data

in the Port Mode Register, the other is to write data into the Serial Mode Register. In this state, the serial interface does not operate although the transfer clock is applied. If STS instruction is executed, the serial interface changes its state to "SCK waiting state".

In the "SCK waiting state", the falling edge of first transfer clock affects the serial interface to get into "transfer state", while the Octal Counter counts-up and the Serial Data Register shifts simultaneously. As an exception, if the clock continuous output mode is selected, the serial interface stays in "SCK waiting state" while the transfer clock outputs continuously.

The Octal Counter becomes "000" again by 8 transfer clocks or execution of STS instruction, so that the serial interface gets back into the "SCK waiting state", and SERIAL Interrupt Request Flag is set simultaneously.

When the internal transfer clock is selected, the transfer clock output are triggered by the execution of STS instruction, and it stops after 8 clocks.

- **Example of Transfer Clock Error Detection**

The serial interface functions abnormally when the transfer clock was disturbed by external noises. In this case, the transfer clock error can be detected in the procedure shown in Fig. 12.

If more than 9 transfer clocks are applied by the external noises in the "SCK waiting state", the state of the serial interface shifts as the following sequence: first "transfer state" (while 1 to 7 transfer clocks), second "SCK waiting state" (at 8th transfer clock) and third "transfer state" again. Then reset the SERIAL Interrupt Request Flag, and make "STS waiting state" by writing to the Serial Mode Register. SERIAL Interrupt Request Flag is set again in this procedure, and it shows that the transfer clock was invalid and that the transmit/receive data were also invalid.

Table 10. Serial Interface Operation Mode

SMR	PMR		Serial Interface Operating Mode
Bit 3	Bit 1	Bit 0	
1	0	0	Clock Continuous Output Mode
1	0	1	Transmit Mode
1	1	0	Receive Mode
1	1	1	Transmit/Receive Mode

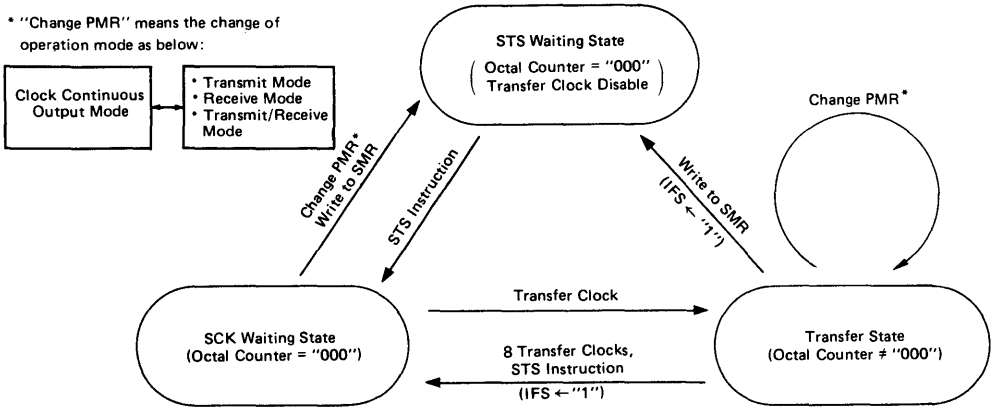


Fig. 11 Serial Interface Operation State

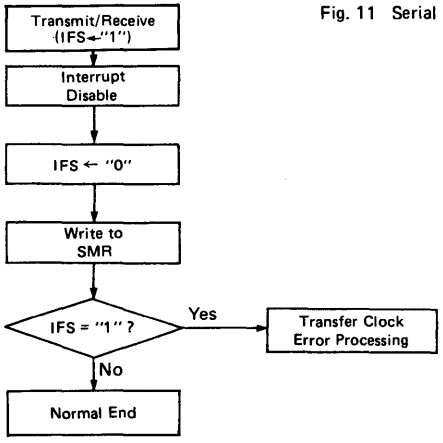


Fig. 12 Example of Transfer Clock Error Detection

■ TIMER

The MCU contains a prescaler and two timer/counters (TIMER-A, TIMER-B), Fig. 13 shows the block diagram. The prescaler is an 11-bit binary counter. TIMER-A is an 8-bit free-running timer. TIMER-B is an 8-bit auto-reload timer/event counter.

- **Prescaler**

The input to the prescaler is a system clock signal. The prescaler is initialized to $000 by MCU reset, and the prescaler starts to count up the system clock signal as soon as RESET input goes to logic "0". The prescaler keeps counting up except MCU reset and stop mode. The prescaler provides clock signals to TIMER-A, TIMER-B and serial interface. The prescaler devide ratio of the clock signals are selected according to the content of the mode registers such as – Timer Mode Register A (TMA), Timer Mode Register B (TMB), Serial Mode Register (SMR).

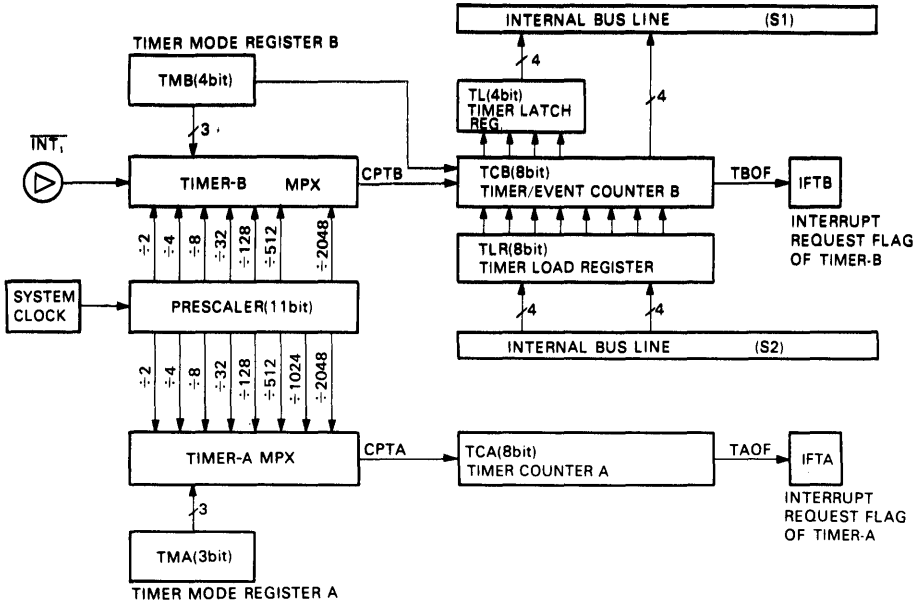


Fig. 13 Timer/Counter Block Diagram

- **TIMER-A Operation**

After TIMER-A is initialized to $00 by MCU reset, it counts up at every clock input signal. When the next clock signal is applied after TIMER-A is counted up to $FF, TIMER-A is set to $00 again, and generating overflow output. This leads to setting TIMER-A Interrupt Request Flag (IFTA: $001, 2) to "1". Therefore, this timer can function as an interval timer periodically generating overflow output at every 256th clock signal input.

The clock input signals to TIMER-A are selected by the Timer Mode Register A (TMA: $008).

- **TIMER-B Operation**

Timer Mode Register B (TMB: $009) is used to select the auto-reload function and the prescaler divide ratio of TIMER-B as the input clock source. When the external event input is used as an input clock signal to TIMER-B, select the $R_{33}/\overline{INT_1}$ as $\overline{INT_1}$ and set the External Interrupt Mask (IM1) to "1" to prevent the external interrupt request from occurring.

TIMER-B is initialized according to the value written into the Timer Load Register by software. TIMER-B counts up at every clock input signal. When the next clock signal is applied to TIMER-B after TIMER-B is set to $FF, TIMER-B will be initialized again and generate overflow output. In this case if the auto-reload function is selected. TIMER-B is initialized according to the value of the Timer Load Register. Else if the auto-reload function is not selected, TIMER-B goes to $00. TIMER-B Interrupt Request Flag (IFTB: $002,0) will be set at this overflow output.

- **Timer Mode Register A (TMA: $008)**

The Timer Mode Register A is a 3-bit write-only register. The TMA controls the prescaler divide ratio of TIMER-A clock input, as shown in Table 11.

The Timer Mode Register A is initialized to $0 by MCU reset.

- **Timer Mode Register B (TMB: $009)**

The Timer Mode Register B is a 4-bit write-only register. The Timer Mode Register B controls the selection for the auto-reload function of TIMER-B and the prescaler divide ratio, and the source of the clock input signal, as shown in Table 12.

The Timer Mode Register B is initialized to $0 by MCU reset.

The operation mode of TIMER-B is changed at the second instruction cycle after writing into the Timer Mode Register B.

Therefore, it is necessary to program the write instruction to TLRU after the content of TMB is changed.

Table 11. Timer Mode Register A

TMA			Prescaler Divide Ratio
Bit 2	Bit 1	Bit 0	
0	0	0	÷2048
0	0	1	÷1024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	0	÷ 32
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2

Table 12. Timer Mode Register B

TMB Bit 3	Auto-reload Function
0	No
1	Yes

TMB Bit 2	TMB Bit 1	TMB Bit 0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	$\overline{INT_1}$ (External Event Input)

- **TIMER-B (TCBL: $00A, TCBU: $00B / TLRL: $00A, TLRU: $00B)**

TIMER-B consists of an 8-bit write-only Timer Load Register, and an 8-bit read-only Timer/Event Counter. Each of them has a low-order digit (TCBL: $00A, TLRL: $00A) and a high-order digit (TCBU: $00B, TLRU: $00B).

The Timer/Event Counter can be initialized by writing data into the Timer Load Register. In this case, write the low-order digit first, and then the high-order digit. The Timer/Event Counter is initialized at the time when the high-order digit is written. The Timer Load Register will be initialized to $00 by the MCU reset.

The counter value of TIMER-B can be obtained by reading the Timer/Event Counter. In this case, read the high-order digit first, and then the low-order digit. The count value of low-order digit is latched at the time when the high-order digit is read.

- **TIMER-A Interrupt Request Flag (IFTA: $001, 2)**

The TIMER-A Interrupt Request Flag is set by the overflow output of TIMER-A.

- **TIMER-A Interrupt Mask (IMTA: $001, 3)**

TIMER-A Interrupt Mask prevents an interrupt request generated by TIMER-A Interrupt Request Flag.

Table 13. TIMER-A Interrupt Request Flag

TIMER-A Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 14. TIMER-A Interrupt Mask

TIMER-A Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

- **TIMER-B Interrupt Request Flag (IFTB: $002, 0)**

The TIMER-B Interrupt Request Flag is set by the overflow output of TIMER-B.

- **TIMER-B Interrupt Mask (IMTB: $002, 1)**

TIMER-B Interrupt Mask prevents an interrupt request generated by TIMER-B Interrupt Request Flag.

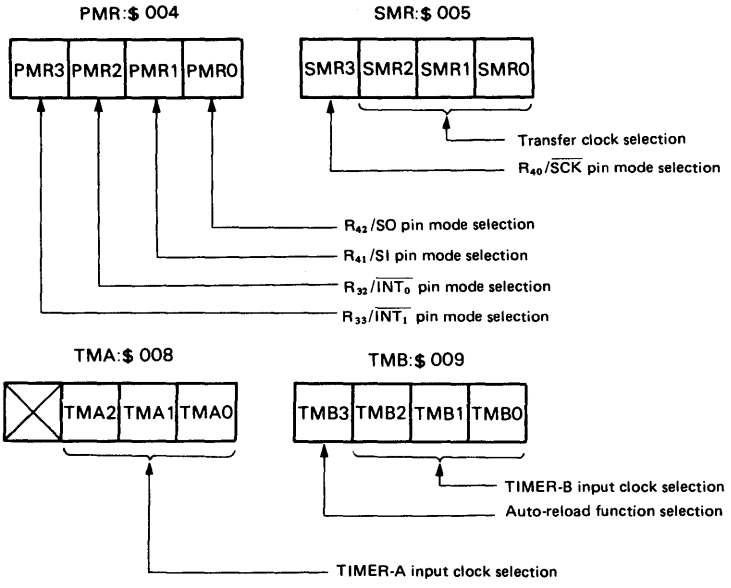


Fig. 14 Mode Register Configuration and Function

Table 15. TIMER-B Interrupt Request Flag

TIMER-B Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 16. TIMER-B Interrupt Mask

TIMER-B Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

■ INPUT/OUTPUT

The MCU provides 58 Input/Output pins, and they are consist of 32 standard pins and 26 high voltage pins. Each standard pin may have one of three mask options: (A) "Without pull-up MOS (NMOS open drain)", (B) "With pull-up MOS", or (C) "CMOS". And also each high voltage pin may have one of two mask options: (D) "Without pull-down MOS (PMOS open drain)", or (E) "With pull-down MOS". As pull-down MOS is connected to internal V_{disp} line, select R_{A1}/V_{disp} pin as V_{disp} with mask option when at least one high voltage pin is selected as "With pull-down MOS" option.

When any Input/Output common pin is used as input pin, it is necessary to select the mask option and output data as shown in Table 18.

• Output Circuit Operation of Standard Pins with "With pull-up MOS" Option

Fig. 15 shows the circuit used in the standard pins with "with pull-up MOS"option.

By execution of the output instruction, the write pulse will be generated, and be applied to the addressed port. This pulse will turn "ON" the PMOS (B) to make the transient time shorten to obtain "High level", if the output data is changed from "0" to "1". In this case, the "write pulse" allows the PMOS (B) to turn "ON" as long as 1/8 instruction cycle. While "write pulse" is "0", pull-up MOS (C) may retain the output in high level.

The $\overline{HLT}$ signal becomes "0" in stop mode, so that MOS (A) (B) (C) turn "OFF".

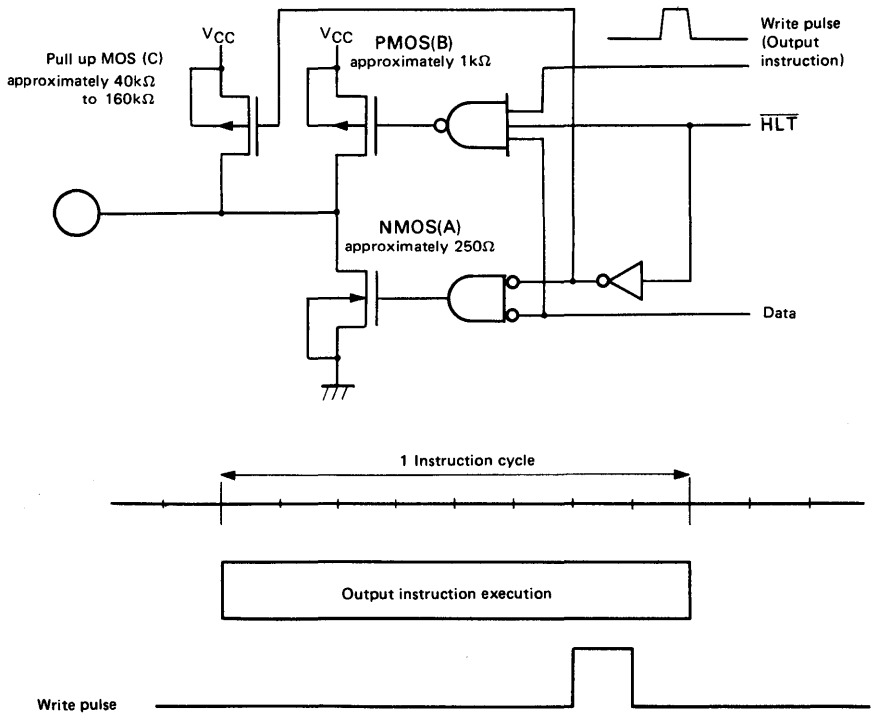
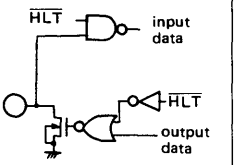
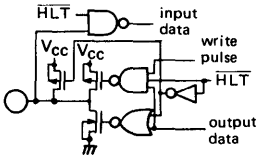
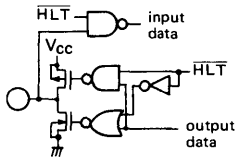
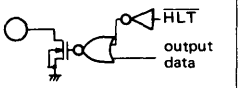
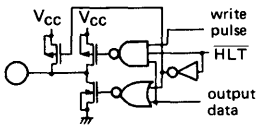
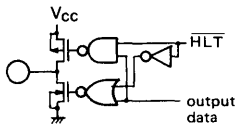
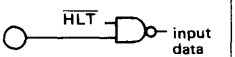
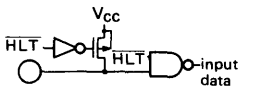
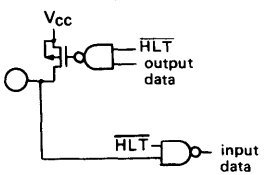
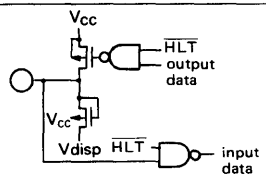
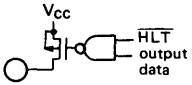
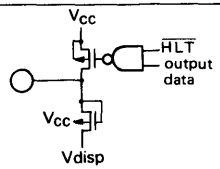
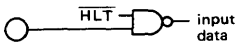
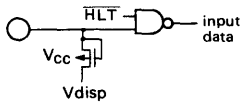


Fig. 15 Output Circuit Operation of Standard Pins with "with Pull-up MOS" Option

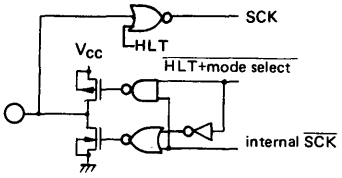
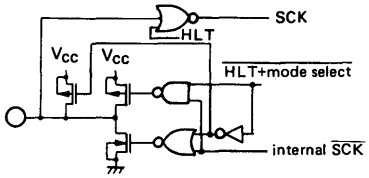
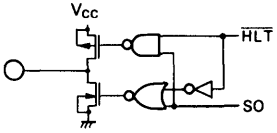
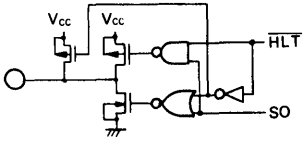
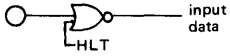
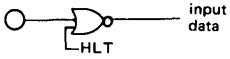
Table 17 I/O Pin Circuit Type

		Without pull-up MOS (NMOS open drain) (A)	With pull-up MOS (B)	CMOS (C)	Applied pins
Standard pins	I/O common pins				$D_0 \sim D_3$, $R_{30} \sim R_{33}$, $R_{40} \sim R_{43}$, $R_{50} \sim R_{53}$
	Output pins				$R_{60} \sim R_{63}$, $R_{70} \sim R_{73}$, $R_{80} \sim R_{83}$
	Input pins				$R_{90} \sim R_{93}$

		Without pull-down MOS (PMOS open drain) (D)	With pull-down MOS (E)	Applied pins
High voltage pins	I/O common pins			$D_4 \sim D_{15}$, $R_{10} \sim R_{13}$, $R_{20} \sim R_{23}$
	Output pins			$R_{00} \sim R_{03}$
	Input pins			R_{A0}, R_{A1}/V_{disp}

(Note) In the stop mode, $\overline{HLT}$ signal is "0" and I/O pins are in high impedance state.

(to be continued)

		Without pull-up MOS (NMOS open drain) or CMOS (A or C)	With pull-up MOS (B)	Applied pins
Standard pins	I/O common pins			$\overline{SCK}$
	Output pins			SO
	Input pins			$\overline{INT_0}$, $\overline{INT_1}$, SI

(Note) In the stop mode, $\overline{HLT}$ signal is "0", HLT signal is "1" and I/O pins are in high impedance state.

Table 18 Data Input from Input/Output Common Pins

I/O pin circuit type		Possibility of Input	Available pin condition for input
Standard pins	CMOS	No	–
	Without pull-up MOS (NMOS open drain)	Yes	"1"
	With pull-up MOS	Yes	"1"
High voltage pins	Without pull-down MOS (PMOS open drain)	Yes	"0"
	With pull-down MOS	Yes	"0"

- **D-port**

D-port is 1-bit I/O port, and it has 16 Input/Output common pins. It can be set/reset by the SED/RED and SEDD/REDD instructions, and can be tested by the TD and TDD instructions. Table 17 shows the classification of standard pins, high voltage pins and the Input/Output pins circuit types.

- **R-port**

R-port is 4-bit I/O port. It provides 20 input/output common pins, 16 output-only pins, and 6 input-only pins. Data input is processed using the LAR and LBR instructions and data output is processed using the LRA and LRB instructions. The MCU will not be affected by writing into the input-only and/or non-existing ports, invalid data will be read by reading from the output-only and/or non-existing ports.

The R_{32}, R_{33}, R_{40}, R_{41} and R_{42} pins are also used as the $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK}$, SI and SO pins respectively. Table 17 shows the classification of standard pins, high voltage pins and Input/Output pins circuit types.

- **RESET**

The MCU is reset by setting RESET pin to "1". At power ON or recovering from stop mode, apply RESET input more than t_{RC} to obtain the necessary time for oscillator stabilization. In other cases, the MCU reset requires at least two instructions cycle time of RESET input.

Table 19 shows initialized items by MCU reset and each status after reset.

Table 19 Initial Value by MCU Reset

Items			Initial value by MCU reset	Contents
Program counter (PC)			$0000	Execute program from the top of ROM address.
Status (ST)			"1"	Enable to branch with conditional branch instructions.
Stack pointer (SP)			$3FF	Stack level is 0.
I/O pin output register	Standard pin	(A) Without pull-up MOS	"1"	Enable to input.
		(B) With pull-up MOS	"1"	Enable to input
		(C) CMOS	"1"	–
	High voltage pin	(D) Without pull-down MOS	"0"	Enable to input.
		(E) With pull-down MOS	"0"	Enable to input.
Interrupt flag	Interrupt Enable Flag (I/E)		"0"	Inhibit all interrupts.
	Interrupt Request Flag (IF)		"0"	No interrupt request.
	Interrupt Mask (IM)		"1"	Mask interrupt request.
Mode register	Port Mode Register (PMR)		"0000"	See Item "Port Mode Register".
	Serial Mode Register (SMR)		"0000"	See Item "Serial Mode Register".
	Timer Mode Register A (TMA)		"000"	See Item "Timer Mode Register A".
	Timer Mode Register B (TMB)		"0000"	See Item "Timer Mode Register B".
Timer/Counter, Serial interface	Prescaler		$000	–
	Timer/Counter A (TCA)		$00	–
	Timer/Event Counter B (TCB)		$00	–
	Timer Load Register (TLR)		$00	–
	Octal Counter		"000"	–

(Note) MCU reset affects to the rest of registers as follows:

Item		After recovering from STOP mode by MCU reset	After MCU reset except for the left condition
Carry	(CA)	The contents of the items before MCU reset are not retained. It is necessary to intialize them by software again.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software again.
Accumulator	(A)		
B Register	(B)		
W Register	(W)		
X/SPX Registers	(X/SPX)		
Y/SPY Registers	(Y/SPY)		
Serial Data Register	(SR)	Same as above	Same as above
RAM		The contents of RAM before MCU reset (just before STOP instruction) are retained.	Same as above

■ INTERNAL OSCILLATOR CIRCUIT

Fig. 16 gives internal oscillator circuit. The oscillator type can be selected from a crystal oscillator or a ceramic filter oscillator without mask option. In any cases, external clock operation is available.

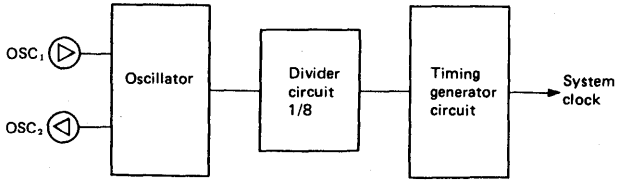


Fig. 16 Internal Oscillator Circuit

- **Oscillator Circuit**

Table 20 Examples of Oscillator Circuit

	Circuit configuration	Remarks
External clock operation	Oscillator OSC1 Open — OSC2	
Ceramic filter oscillator	Ceramic filter C1, OSC1, Rf, OSC2, C2 GND	Ceramic filter CSA6.00MG (Murata) Rf : 1MΩ±2% C1 : 30pF±20% C2 : 30pF±20% • Wiring between these pins and elements should be as short as possible, and never cross the other wirings. (Refer to Fig. 17)
Crystal oscillator	C1, Crystal, OSC1, Rf, OSC2, C2 GND AT cut parallel resonance crystal OSC1 — L — C1 — Rs — OSC2 C0	Rf : 1MΩ±2% C1 : 10~22pF±20% C2 : 10~22pF±20% Crystal: AT cut parallel resonance crystal C0 : 7pF max. Rs : 100Ω max. f : 2.0~6.2MHz • Wiring between these pins should be as short as possible, and never cross the other wirings. (Refer to Fig. 17)

Note) Please consult with the engineers of crystal or ceramic filter maker to determine the value of R_f, C_1 and C_2.

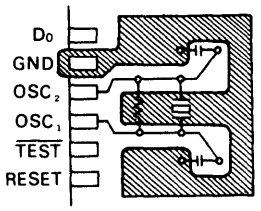


Fig. 17 Recommendable Layout of Crystal and Ceramic Filter

■ LOW POWER DISSIPATION MODE

The MCU provides two low power dissipation modes, that is, a Standby mode and a Stop mode. Table 21 shows the function of the low power dissipation mode, and Fig. 18 shows the diagram of the mode transition.

Table 21 Low Power Dissipation Mode Function

Low Power Dissipation Mode	Instruction	Condition							Recovering method
		Oscillator circuit	Instruction execution	Register, Flag	Interrupt function	RAM	Input/ Output pin	Timer/ Counter, Serial Interface	
Standby mode	SBY instruction	Active	Stop	Retained	Active	Retained	Retained*3)	Active	RESET Input, Interrupt request
Stop mode	STOP instruction	Stop	Stop	RESET*1)	Stop	Retained	High*2) impedance	Stop	RESET Input

*1) As the MCU recovers from STOP mode by RESET input, the contents of the flags and registers are initialized according to Table 19.
*2) A high voltage pin with a pull-down MOS option is pulled down to the V_{disp} power supply by the pull-down MOS. As the MOS is ON, a pull-down MOS current flows when a voltage difference between the pin and the V_{disp} voltage exists. This is the additional current to the current dissipation in Stop Mode (I_{stop}).
*3) As a I/O circuit is active, a I/O current possibly flows according the state of I/O pin. This is the additional current to the current dissipation in Standby Mode (I_{SBY1}, I_{SBY2}).

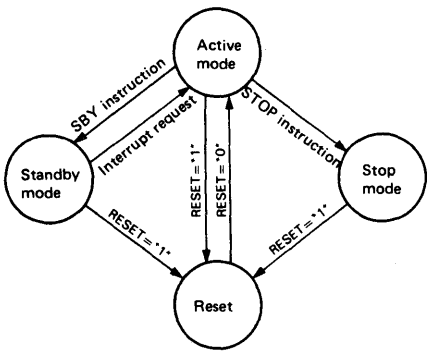


Fig. 18 MCU Operation Mode Transition

• Standby Mode

The SBY instruction puts the MCU into the Standby mode. In the Standby mode, the oscillator circuit is active and timer/counter and serial interface continue working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM and Input/Output pins retain the state they had just before going into the Standby mode.

The Standby mode is canceled by the MCU reset or interrupt request. When canceled by the interrupt request, the MCU becomes an active mode and executes the instruction next to the SBY instruction. At this time, if the Interrupt Enable Flag is "1", the interrupt is executed. If the Interrupt Enable Flag is "0", the interrupt request is held on and the normal instruction execution continues.

Fig. 19 shows the flowchart of the Standby Mode.

• Stop Mode

The STOP instruction brings the MCU into the Stop mode. In this mode the oscillator circuit and every function of the MCU stop.

The Stop mode is canceled by the MCU reset. At this time, as shown in Fig. 20, apply the RESET input for more than t_{RC} to get enough oscillator stabilization time. (Refer to the "AC CHARACTERISTICS".) After the Stop mode is canceled, RAM retains the state it had just before going into the Stop mode. The other hand, Accumulator, B Register, W Register, X/SPX Registers, Y/SPY Registers, Carry and Serial Data Register don't retain the contents.

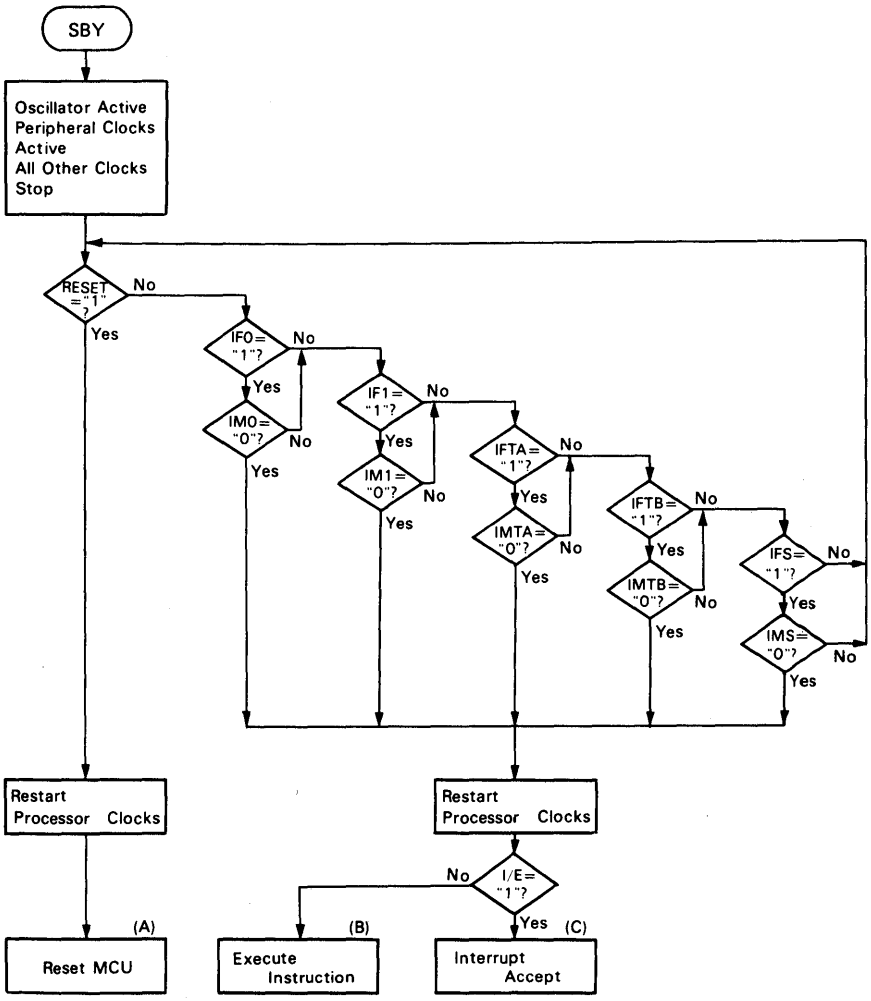


Fig. 19 MCU Operating Flowchart

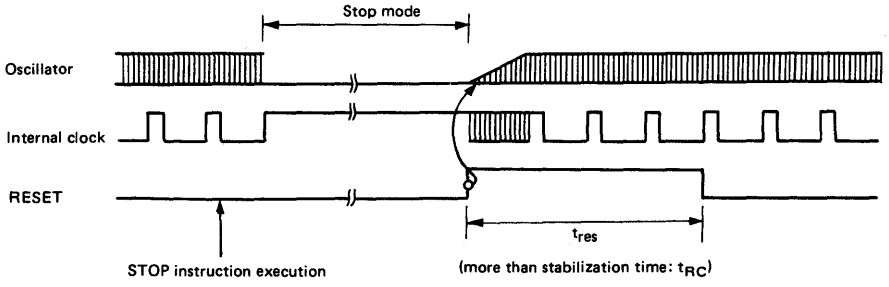


Fig. 20 Timing Chart of Recovering from Stop Mode

■ RAM ADDRESSING MODE

As shown in Fig. 21, the MCU provides three RAM addressing modes; Register Indirect Addressing, Direct Addressing and Memory Register Addressing.

• Register Indirect Addressing

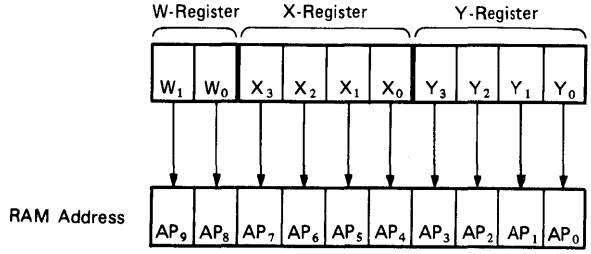
The combined 10-bit contents of W Register, X Register and Y Register is used as the RAM address in this mode.

• Direct Addressing

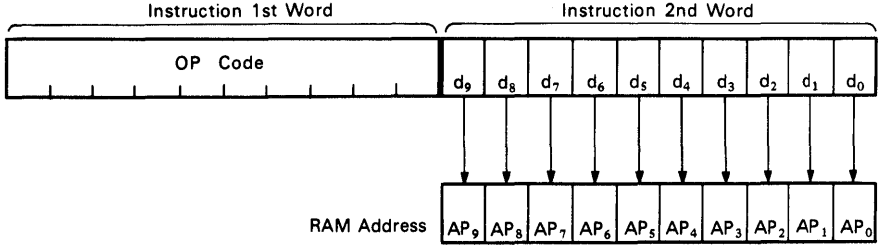
The direct addressing instruction consists of two words and the second word (10 bits) following Op-code (the first word) is used as the RAM address.

• Memory Register Addressing

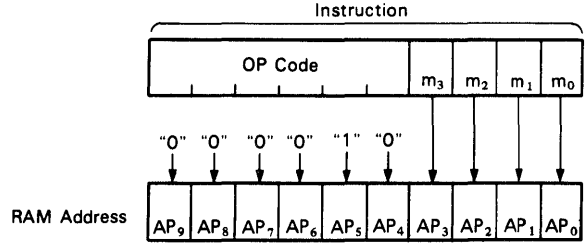
The Memory Register Addressing can access 16 digits (Memory Register: MR) from $020 to $02F by using the LAMR and XMRA instruction.



(a) Register Indirect Addressing



(b) Direct Addressing



(c) Memory Register Addressing

Fig. 21 RAM Addressing Mode

■ ROM ADDRESSING MODE AND P INSTRUCTION

The MCU has four kinds of ROM addressing modes as shown in Fig. 22.

• Direct Addressing Mode

The program can branch to any addresses in the ROM memory space by using JMPL, BRL or CALL instruction. These instruction replace 14-bit program counter (PC_{13} to PC_0) with 14-bit immediate data.

• Current Page Addressing Mode

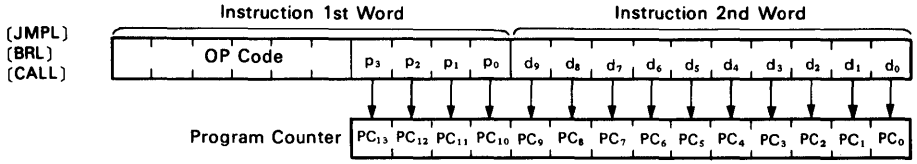
ROM memory space is divided into 256 words in each page starting from $0000. The program branches to the address in the same page using BR instruction. This instruction replace the lower-order eight bits of program counter (PC_7 to PC_0) with 8-bit immediate data. The branch destination by BR instruction on the boundary between pages is in the next page. Refer to Fig. 24.

• Zero Page Addressing Mode

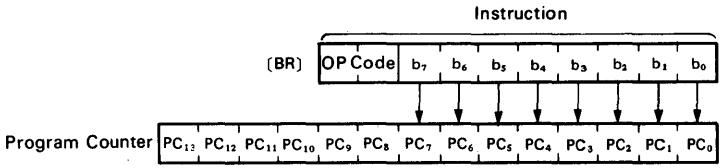
The program branches to the zero page subroutine area, which is located on the address from $0000 to $003F, using CAL instruction. When CAL instruction is executed, 6-bit immediate data is placed in low-order six bits of program counter (PC_5 to PC_0) and "0's" are placed in high-order eight bits (PC_{13} to PC_6).

• Table Data Addressing

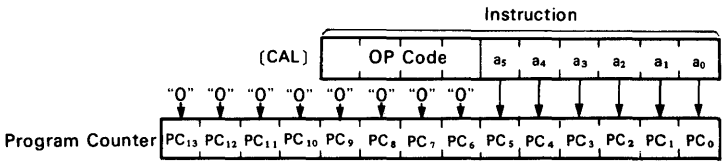
The program branches to the address determined by the contents of the 4-bit immediate data, accumulator and B register, using TBR instruction.



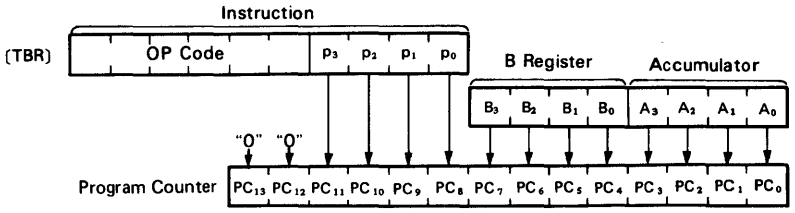
(a) Direct Addressing



(b) Current Page Addressing

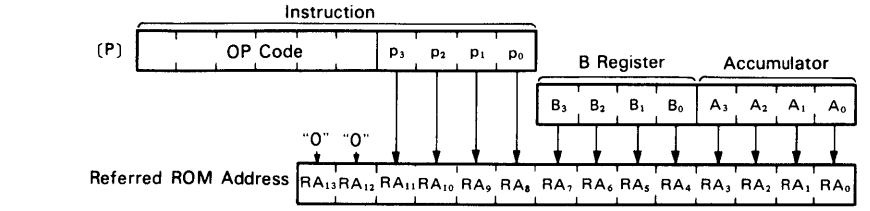


(c) Zero Page Addressing

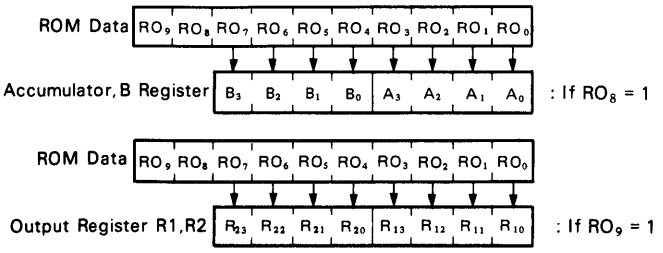


(d) Table Data Addressing

Fig. 22 ROM Addressing Mode



(a) Address Designation



(b) Pattern Output

Fig. 23 P Instruction

- **P Instruction**

The P instruction refers ROM data addressed by Table Data Addressing. ROM data addressed also determine its destination. When bit 8 in referred ROM data is "1", 8 bits of referred ROM data are written into the accumulator and B Register. When bit 9 is "1", 8 bits of referred ROM data are written into the R1 and R2 port output register. When both bit 8 and 9 are "1", ROM data are written into the accumulator and B Register and also to the R1 and R2 port output register at a same time.

The P instruction has no effect on the program counter.

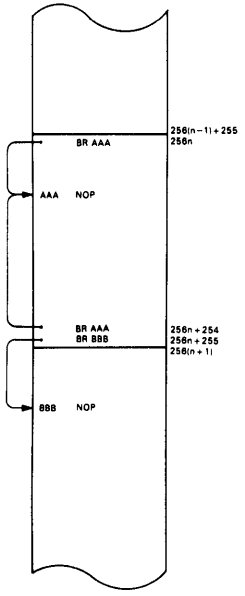


Fig. 24 The Branch Destination by BR Instruction on the Boundary between Pages

■ INSTRUCTION SET

The HMCS400 series provide 99 instructions. These instructions are classified into 10 groups as follows;

(1) Immediate Instruction
(2) Register-to-Register Instruction
(3) RAM Address Instruction
(4) RAM Register Instruction
(5) Arithmetic Instruction
(6) Compare Instruction
(7) RAM Bit Manipulation Instruction
(8) ROM Address Instruction
(9) Input/Output Instruction
(10) Control Instruction

Table 22. Immediate Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD / CYCLE
Load A from Immediate	LAI i	1 0 0 0 1 1 i_3 i_2 i_1 i_0	i⟶A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i_3 i_2 i_1 i_0	i⟶B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i⟶M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i_3 i_2 i_1 i_0	i⟶M,Y+1⟶Y	NZ	1/1

Table 23. Register-to-Register Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD / CYCLE
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B→A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A→B		1/1
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y→A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX→A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY→A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m_3 m_2 m_1 m_0	MR(m)→A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m_3 m_2 m_1 m_0	MR(m)↔A		1/1

Table 24. RAM Address Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD / CYCLE
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i_1 i_0	i⟶W		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i_3 i_2 i_1 i_0	i⟶X		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i_3 i_2 i_1 i_0	i⟶Y		1/1
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	A⟶X		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	A⟶Y		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	Y+1→Y	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	Y−1→Y	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	Y+A→Y	OVF	1/1
Subtract A from Y	SYY	0 0 1 1 0 1 0 1 0 0	Y−A→Y	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	X↔SPX		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	Y↔SPY		1/1
Exchange X and SPX,Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	X↔SPX,Y↔SPY		1/1

Table 25. RAM Register Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD / CYCLE
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M→A, $(^{X\leftrightarrow SPX}_{Y\leftrightarrow SPY})$		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M→A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M→B, $(^{X\leftrightarrow SPX}_{Y\leftrightarrow SPY})$		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A→M, $(^{X\leftrightarrow SPX}_{Y\leftrightarrow SPY})$		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A→M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A→M,Y+1→Y(X↔SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A→M,Y−1→Y(X↔SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M↔A, $(^{X\leftrightarrow SPX}_{Y\leftrightarrow SPY})$		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M↔A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M↔B, $(^{X\leftrightarrow SPX}_{Y\leftrightarrow SPY})$		1/1

Note) (XY) and (x) have the meaning as follows:

(1) The instructions with (XY) have 4 mnemonics and 4 object codes for each. (example of LAM (XY) is given below.)

MNEMONIC	y	x	FUNCTION
LAM	0	0	
LAMX	0	1	X↔SPX
LAMY	1	0	Y↔SPY
LAMXY	1	1	X↔SPX, Y↔SPY

(2) The instructions with (x) have 2 mnemonics and 2 object codes for each. (example of LMAIY(X) is given below.)

MNEMONIC	x	FUNCTION
LMAIY	0	
LMAIYX	1	X↔SPX

Table 26. Arithmetic Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Add Immediate to A	AI i	1 0 1 0 0 0 i_3 i_2 i_1 i_0	A+i→A	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	B+1→B	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	B−1→B	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\bar{A}$+1→A		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\bar{B}$→B		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	1→CA		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	0→CA		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 0 1 0 0 0	M+A→A	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M+A→A	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	M+A+CA→A	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M+A+CA→A	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	M−A−$\overline{CA}$→A	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M−A−$\overline{CA}$→A	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	A∪B →A		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	A∩M→A	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A∩M→A	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	A∪M→A	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A∪M→A	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	A⊕M→A	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A⊕M→A	NZ	2/2

Table 27. Compare Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i_3 i_2 i_1 i_0	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i_3 i_2 i_1 i_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	ANEMD d	0 1 0 0 0 0 0 1 0 0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i_3 i_2 i_1 i_0	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i_3 i_2 i_1 i_0	i ≦ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i_3 i_2 i_1 i_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i ≦ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≦ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ≦ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≦ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i_3 i_2 i_1 i_0	A ≦ i	NB	1/1

Table 28. RAM Bit Manipulation Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n_1 n_0	1→M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n_1 n_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	1→M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n_1 n_0	0→M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n_1 n_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	0→M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n_1 n_0		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n_1 n_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		M(n)	2/2

Table 29. ROM Address Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Branch on Status 1	BR b	1 1 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p_3 p_2 p_1 p_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p_3 p_2 p_1 p_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a_5 a_4 a_3 a_2 a_1 a_0		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p_3 p_2 p_1 p_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p_3 p_2 p_1 p_0			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1→I/E		1/3

Table 30. Input/Output Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1→D(Y)		1/1
Set Discrete I/O Latch Direct	SEDD m	1 0 1 1 1 0 m_3 m_2 m_1 m_0	1→D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0→D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m_3 m_2 m_1 m_0	0→D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m_3 m_2 m_1 m_0		D(m)	1/1
Load A from R-Port Register	LAR m	1 0 0 1 0 1 m_3 m_2 m_1 m_0	R(m)→A		1/1
Load B from R-Port Register	LBR m	1 0 0 1 0 0 m_3 m_2 m_1 m_0	R(m)→B		1/1
Load R-Port Register from A	LRA m	1 0 1 1 0 1 m_3 m_2 m_1 m_0	A→R(m)		1/1
Load R-Port Register from B	LRB m	1 0 1 1 0 0 m_3 m_2 m_1 m_0	B→R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p_3 p_2 p_1 p_0			1/2

Table 31. Control Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD / CYCLE
No Operation	NOP	0000000000			1/1
Start Serial	STS	0101001000			1/1
Stand-by Mode	SBY	0101001100			1/1
Stop Mode	STOP	0101001101			1/1

Table 32. Op-Code Map

R9 \ R8	0																1													
H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	XSPX	XSPY	XSP XY	AN EM				AM				ORM								ANEMD				AMD				ORMD			
1	RTN	RTNI			ALEM				AMC				EORM								ALEMD				AMCD				EORMD			
2	INEM i(4)																INEMD i(4)															
3	ILEM i(4)																ILEMD i(4)															
4	LBM(XY)				BNEM				LAB				IB				COMB				OR				STS				SBY	STOP		
5	LMAIY(X)				AYY				LASPY				IY				JMPL p(4)															
6	NEGA				RED				LASPX							TC	CALL p(4)															
7	YNEI i(4)																BRL p(4)															
8	XMA(XY)				SEM n(2)				REM n(2)				TM n(2)				XMAD				SEMD n(2)				REMD n(2)				TMD n(2)			
9	LAM(XY)				LMA(XY)				SMC				ANM				LAMD				LMAD				SMCD				ANMD			
A	ROTR	ROTL					DAA				DAS					LAY	LMID i(4)															
B	TBR p(4)																P p(4)															
C	XMB(XY)				BLEM				LBA							DB	CAL a(6)															
D	LMADY(X)				SYY				LYA							DY																
E	TD				SED				LXA				REC			SEC																
F	LWI i (2)																															
1	BR b(8)																															
0	LBI i(4)																															
1	LYI i(4)																															
2	LXI i(4)																															
3	LAI i(4)																															
4	LBR m(4)																															
5	LAR m(4)																															
6	REDD m(4)																															
7	LAMR m(4)																															
8	AI i(4)																															
9	LMIIY i(4)																															
A	TDD m(4)																															
B	ALEI i(4)																															
C	LRB m(4)																															
D	LRA m(4)																															
E	SEDD m(4)																															
F	XMRA m(4)																															

... 1-word/2-cycle Instruction

... 1-word/3-cycle Instruction

... RAM Direct Address Instruction (2-word/2-cycle)

... 2-word/2-cycle Instruction

■ MASK OPTION LIST

- Family Name ■ HMCS404AC
- Package □ DP-64S □ FP-64
- I/O Circuit Type A; Without Pull-up MOS (NMOS Open Drain)
  B; With Pull-up MOS
  C; CMOS
  D; Without Pull-down MOS (PMOS Open Drain)
  E; With Pull-down MOS

Date of Order	
Customer	
Dept.	
Name	
ROM Code Name	
LSI Type Number (Hitachi's entry)	

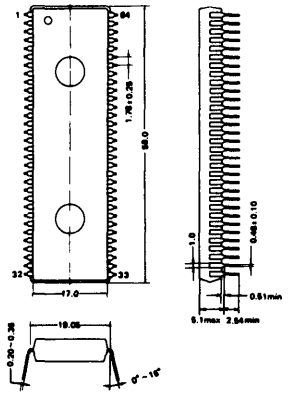
PIN		INPUT/OUTPUT		I/O OPTION A	B	C	D	E
D_0	Standard Pins	Input/Output						
D_1		Input/Output						
D_2		Input/Output						
D_3		Input/Output						
D_4	High Voltage Pins	Input/Output						
D_5		Input/Output						
D_6		Input/Output						
D_7		Input/Output						
D_8		Input/Output						
D_9		Input/Output						
D_{10}		Input/Output						
D_{11}		Input/Output						
D_{12}		Input/Output						
D_{13}		Input/Output						
D_{14}		Input/Output						
D_{15}		Input/Output						
R0	R_{00}	High Voltage Pins	Output					
	R_{01}		Output					
	R_{02}		Output					
	R_{03}		Output					
R1	R_{10}		Input/Output					
	R_{11}		Input/Output					
	R_{12}		Input/Output					
	R_{13}		Input/Output					
R2	R_{20}		Input/Output					
	R_{21}		Input/Output					
	R_{22}		Input/Output					
	R_{23}		Input/Output					

PIN		INPUT/OUTPUT		I/O OPTION A	B	C	D	E
R3	R_{30}	Standard Pins	Input/Output					
	R_{31}		Input/Output					
	R_{32}		Input/Output					
	R_{33}		Input/Output					
R4	R_{40}		Input/Output					
	R_{41}		Input/Output					
	R_{42}		Input/Output					
	R_{43}		Input/Output					
R5	R_{50}		Input/Output					
	R_{51}		Input/Output					
	R_{52}		Input/Output					
	R_{53}		Input/Output					
R6	R_{60}		Output					
	R_{61}		Output					
	R_{62}		Output					
	R_{63}		Output					
R7	R_{70}		Output					
	R_{71}		Output					
	R_{72}		Output					
	R_{73}		Output					
R8	R_{80}		Output					
	R_{81}		Output					
	R_{82}		Output					
	R_{83}		Output					
R9	R_{90}		Input					
	R_{91}		Input					
	R_{92}		Input					
	R_{93}		Input					
RA	R_{A0}	High Voltage Pins	Input					
	R_{A1}		Input	Please Mark on R_{A1}/V_{disp}				

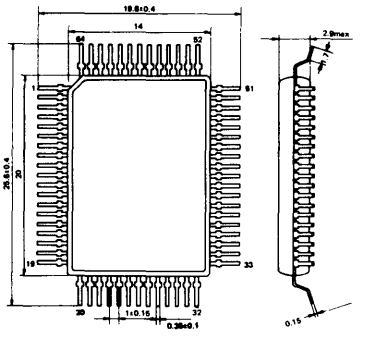
- R_{A1}/V_{disp} (RA1) □ R_{A1}: Without Pull-down MOS (D) □ V_{disp} (VDISP)
- Oscillator (OSC) ■ Crystal or Ceramic Filter Oscillator (XTAL)
- Divider (DIV) ■ Divide-by-8 (D-8)
- ROM Code Media □ EPROM: Emulator Type □ EPROM: EPROM On-Package Microcomputer Type

Note 1) I/O Options masked by ▨ are not available.
Note 2) R_{A1}/V_{disp} has to be selected as V_{disp} pin exept the case that all High Voltage Pins are option D.

■ **PACKAGE DIMENSIONS (Unit: mm)**



(DP-64S)



(FP-64)

HMCS404CL (HD614045)

The HMCS404CL is a CMOS 4-bit single-chip microcomputer which is a member of the HMCS400 series.

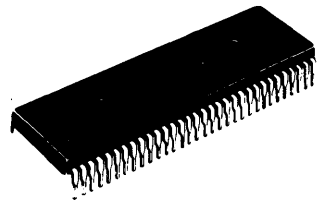
The HMCS404CL is a 3V operation version of the HMCS-404C.

The HMCS404CL has efficient and powerful architecture and its software is very similar to the HMCS40 series.

This microcomputer provides variety of on-chip resources such as ROM, RAM, I/O, two timer/counters and a serial interface to perform in wide users' applications.

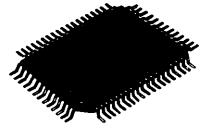
The HMCS404CL also has the characteristics of high speed and low power dissipation and which I/O pins are able to drive fluorescent display tube directly.

HMCS404CL



(DP-64S)

HMCS404CL



(FP-64)

■ HARDWARE FEATURES

- 4-bit Architecture
- 4,096 Words x 10-bit ROM
- 256 Digits x 4-bit RAM
- 58 I/O Pins, including 26 high voltage I/O pins (40V Max)
- Two Timer/Counters
  - 11-bit Prescaler
  - 8-bit Free Running Timer
  - 8-bit Auto-Reload Timer/Event Counter
- Clock Synchronous 8-bit Serial Interface
- Five Interrupt Sources

External	2
Timer/Counter	2
Serial Interface	1

- Subroutine Stack
  - Up to 16 levels including interrupts
- Wide V_{CC} Supply Voltage Range — 2.7V to 6V
- Minimum Instruction Execution Time — 4 μs
- Two Low Power Dissipation Modes
  - Standby — Stops instruction execution while keeping clock oscillation and interrupt functions in operation.
  - Stop — Stops instruction execution and clock oscillation while retaining RAM data
- On-Chip Oscillator
  - External Connection of Crystal or Ceramic Filter (externally drivable)

■ SOFTWARE FEATURES

- Instruction Set Similar to and More Powerful than HMCS40 Series; 99 Instructions
- High Programming Efficiency with 10-bit ROM/Word; 79 instructions are single word instructions
- Direct Branch to All ROM Area
- Direct or Indirect Addressing to All RAM Area
- Subroutine Nesting Up to 16 Levels Including Interrupts
- Binary and BCD Arithmetic Operation
- Powerful Logical Arithmetic Operation
- Pattern Generation — Table Look Up Capability —
- Bit Manipulation for Both RAM and I/O

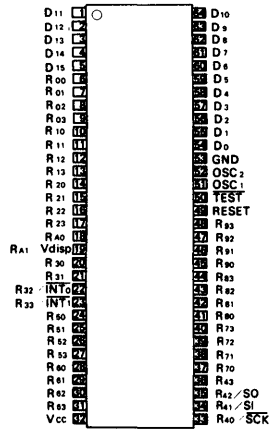
■ VERSATILE PROGRAM DEVELOPMENT SUPPORT TOOLS

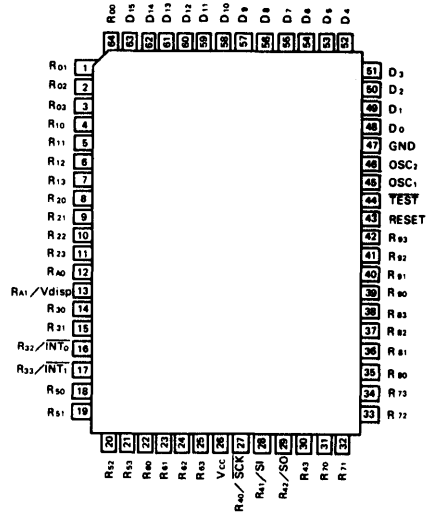
- H68SD Series Macro Assembler
- H68SD5-use Emulator (With Real Time Trace Function)
- EPROM On Package Microcomputer

Mask options are fixed as follows:

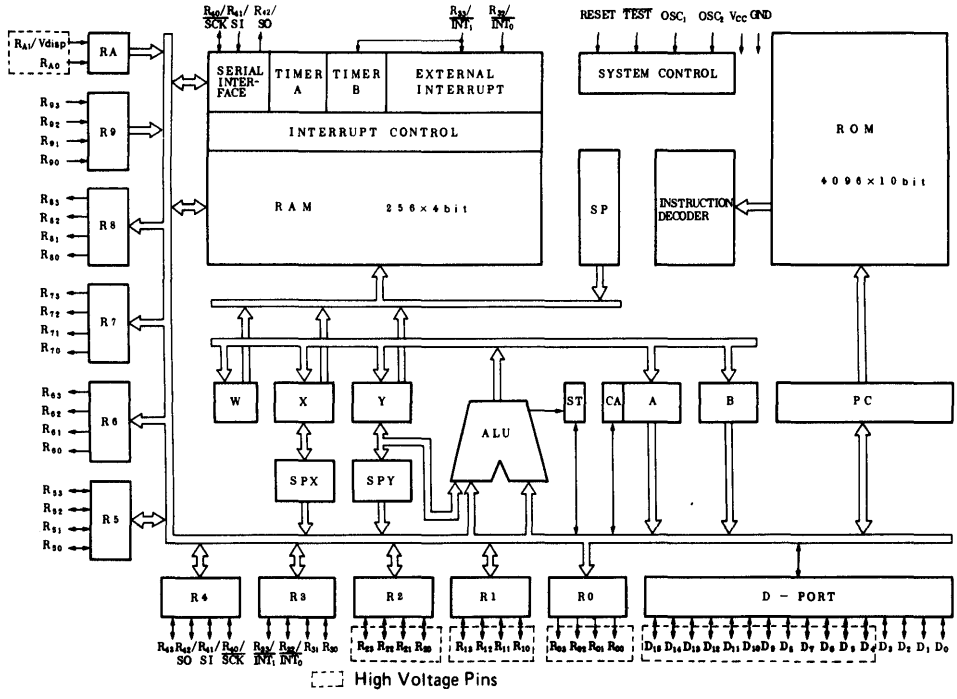
- I/O pin : Open drain
- **Oscillator** : **Crystal Oscillator or Ceramic Filter Oscillator (externally drivable)**
- **Divider** : Divided-by-8

■ PIN ARRANGEMENT (Top View)





■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	−0.3 to +7.0	V	
Terminal Voltage	V_T	−0.3 to V_{CC} +0.3	V	3
		V_{CC} −45 to V_{CC} +0.3	V	4
Total Allowance of Input Currents	ΣI_O	50	mA	5
Total Allowance of Output Currents	$-\Sigma I_O$	150	mA	6
Maximum Input Current	I_O	15	mA	7, 8
Maximum Output Current	$-I_O$	4	mA	9, 10
		6	mA	9, 11
		30	mA	9, 12
Operating Temperature	T_{opr}	−20 to +75	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

(Note 1) Permanent damage may occur if "Absolute Maximum Ratings" are exceeded. Normal operation should be under the conditions of "Electrical Characteristics". If these conditions are exceeded, it may cause the malfunction and affect the reliability of LSI.
(Note 2) All voltages are with respect to GND.
(Note 3) Applied to standard pins.
(Note 4) Applied to high voltage pins.
(Note 5) Total allowance of input current is the total sum of input current which flow in from all I/O pins to GND simultaneously.
(Note 6) Total allowance of output current is the total sum of the output current which flow out from V_{CC} to all I/O pins simultaneously.
(Note 7) Maximum input current is the maximum amount of input current from each I/O pin to GND.
(Note 8) Applied to $D_0 \sim D_3$ and R3 ~ R8.
(Note 9) Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
(Note 10) Applied to $D_0 \sim D_3$ and R3 ~ R8.
(Note 11) Applied to R0 ~ R2.
(Note 12) Applied to $D_4 \sim D_{15}$.

- **ELECTRICAL CHARACTERISTICS**
- **DC CHARACTERISTICS (V_{CC}=2.7V to 6V, GND = 0V, V_{disp} = V_{CC}−40V to V_{CC}, Ta = −20 to +75°C, if not specified.)**

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	RESET, SCK, INT0, INT1		0.85V_{CC}	–	V_{CC}+0.3	V	
		SI		0.85V_{CC}	–	V_{CC}+0.3	V	
		OSC1		V_{CC}−0.3	–	V_{CC}+0.3	V	
Input "Low" Voltage	V_{IL}	RESET, SCK, INT0, INT1		-0.3	–	0.15V_{CC}	V	
		SI		-0.3	–	0.15V_{CC}	V	
		OSC1		-0.3	–	0.3	V	
Output "High" Voltage	V_{OH}	SCK, SO	$-I_{OH}$ = 0.1 mA	V_{CC}−0.5	–	–	V	
Output "Low" Voltage	V_{OL}	SCK, SO	I_{OL} = 0.4mA	–	–	0.4	V	
Input/Output Leakage Current	$\|I_{IL}\|$	RESET, SCK, INT0, INT1, SI, SO, OSC1	V_{in} = 0 V to V_{CC}	–	–	1	μA	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}	V_{CC} = 3 V f_{osc} = 2 MHz	–	–	0.6	mA	2, 6
Current Dissipation in Standby Mode	I_{SBY1}	V_{CC}	Maximum Logic Operation V_{CC} = 3 V f_{osc} = 2 MHz	–	–	0.5	mA	3, 6
	I_{SBY2}	V_{CC}	Minimum Logic Operation V_{CC} = 3 V f_{osc} = 2MHz	–	–	0.4	mA	4, 6
Current Dissipation in Stop Mode	I_{stop}	V_{CC}	V_{in} ($\overline{TEST}$) = V_{CC}-0.2V to V_{CC} V_{in} (RESET) = 0V to 0.2 V	–	–	10	μA	5
Stop Mode Retain Voltage	V_{stop}	V_{CC}		2	–	–	V	

(Note 1) Pull-up MOS current and output buffer current are excluded.
(Note 2) The MCU is in the reset state. The input/output current does not flow.
Test Conditions: MCU state; • Reset state in Operation Mode
Pin state; • RESET, $\overline{TEST}$ ... V_{CC} voltage
• $D_0 \sim D_3$, R3 ~ R9 ... V_{CC} voltage
• $D_4 \sim D_{15}$, R0 ~ R2, R_{A0}, R_{A1} ... V_{disp} voltage
(Note 3) The timer/counter operate with the fastest clock and input/output current does not flow.
Test Conditions: MCU state; • Standby Mode
• Input/Output; Reset state
• TIMER-A; ÷2 prescaler divide ratio
• TIMER-B; ÷2 prescaler divide ratio
• SERIAL Interface ; Stop
Pin state; • RESET ... GND voltage
• $\overline{TEST}$ ... V_{CC} voltage
• $D_0 \sim D_3$, R3 ~ R9 ... V_{CC} voltage
• $D_4 \sim D_{15}$, R0 ~ R2, R_{A0}, R_{A1} ... V_{disp} voltage
(Note 4) The timer/counter operate with the slowest clock and input/output current does not flow.
Test Conditions: MCU state; • Standby Mode
• Input/Output; Reset state
• TIMER-A; ÷2048 prescaler divide ratio
• TIMER-B; ÷2048 prescaler divide ratio
• SERIAL Interface ; Stop
Pin state; • RESET ... GND voltage
• $\overline{TEST}$ ... V_{CC} voltage
• $D_0 \sim D_3$, R3 ~ R9 ... V_{CC} voltage
• $D_4 \sim D_{15}$, R0 ~ R2, R_{A0}, R_{A1} ... V_{disp} voltage
(Note 5) Pull-down MOS current is excluded.
(Note 6) When $f_{osc}=x$ [MHz], the Current Dissipation in Operation mode and Standby mode are estimated as follows:

[When Divide-by-8 (D-8) option is selected.] max. value ($f_{osc}=x$ [MHz]) = $\frac{x}{2}$ x max. value (f_{osc}=2 [MHz])

• INPUT/OUTPUT CHARACTERISTICS FOR STANDARD PIN

(V_{CC} = 2.7V to 6V, GND = 0V, V_{disp} = V_{CC} −40V to V_{CC}, Ta = −20 to +75°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	$D_0 \sim D_3$, R3 ~ R5, R9		0.85V_{CC}	–	V_{CC}+0.3	V	
Input "Low" Voltage	V_{IL}	$D_0 \sim D_3$, R3 ~ R5, R9		-0.3	–	0.15 V_{CC}	V	
Output "High" Voltage	V_{OH}	$D_0 \sim D_3$, R3 ~ R8	$-I_{OH}$ = 0.1 mA	V_{CC}−0.5	–	–	V	1
Output "Low" Voltage	V_{OL}	$D_0 \sim D_3$, R3 ~ R8	I_{OL} = 0.4 mA	–	–	0.4	V	
Input/Output Leakage Current	$\|I_{IL}\|$	$D_0 \sim D_3$, R3 ~ R9	V_{in}= 0V to V_{CC}	–	–	1	μA	2
Pull-Up MOS Current	$-I_p$	$D_0 \sim D_3$, R3 ~ R9	V_{CC} = 3V, V_{in}= 0V	3	15	40	μA	3
		$D_0 \sim D_3$, R3 ~ R9	V_{CC} = 5V, V_{in} = 0V	30	60	120	μA	3

(Note 1) Applied to I/O pins with "CMOS" output selected by mask option.
(Note 2) Pull-up MOS current and output buffer current are excluded.
(Note 3) Applied to I/O pins "with Pull-up MOS" selected by mask option.

- **INPUT/OUTPUT CHARACTERISTICS FOR HIGH VOLTAGE PIN**
  (V_{CC} = 2.7V to 6V, GND = 0V, V_{disp} = V_{CC} −40V to V_{CC}, Ta = −20 to +75°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	$D_4 \sim D_{15}$, R1 R2, R_{A0}, R_{A1}		0.85V_{CC}	–	V_{CC}+0.3	V	
Input "Low" Voltage	V_{IL}	$D_4 \sim D_{15}$, R1 R2, R_{A0}, R_{A1}		V_{CC}−40	–	0.15V_{CC}	V	
Output "High" Voltage	V_{OH}	$D_4 \sim D_{15}$	$-I_{OH}$=15mA, V_{CC}=5V±10%	V_{CC}−3.0	–	–	V	
			$-I_{OH}$=2.5mA	V_{CC}−1.0	–	–	V	
		R0 ~ R2	$-I_{OH}$=3 mA, V_{CC}=5V±10%	V_{CC}−3.0	–	–	V	
			$-I_{OH}$=0.5 mA	V_{CC}−1.0	–	–	V	
Output "Low" Voltage	V_{OL}	$D_4 \sim D_{15}$ R0~R2	V_{disp} = V_{CC}−40V	–	–	V_{CC}−37	V	1
		$D_4 \sim D_{15}$ R0~R2	150kΩ to V_{CC}−40V	–	–	V_{CC}−37	V	2
Input/Output Leakage Current	$\|I_{IL}\|$	$D_4 \sim D_{15}$ R0~R2 R_{A0}, R_{A1}	V_{in} = V_{CC}−40V to V_{CC}	–	–	20	μA	3
Pull Down MOS Current	I_d	$D_4 \sim D_{15}$ R0~R2 R_{A0}, R_{A1}	V_{disp} = V_{CC}−35V V_{in} = V_{CC}	125	250	500	μA	4

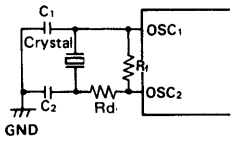
(Note 1) Applied to I/O pins "with Pull-down MOS" selected by mask option.
(Note 2) Applied to I/O pins "without Pull-down MOS (PMOS Open Drain)" selected by mask option.
(Note 3) Pull-down MOS current and output buffer current are excluded.
(Note 4) Applied to I/O pins "with Pull-down MOS" selected by mask option.

• AC CHARACTERISTICS (V_{CC}=2.7V to 6V, GND = 0V, V_{disp} = V_{CC}−40V to V_{CC}, Ta = −20 to +75°C, if not specified.)

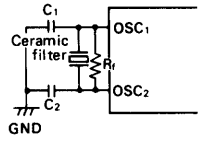
Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Oscillation Frequency	f_{osc}	OSC_1, OSC_2		0.4	2	2.25	MHz	
Instruction Cycle Time	t_{cyc}			3.55	4	20	μs	
Oscillator Stabilization Time	t_{RC}	OSC_1, OSC_2		–	–	60	ms	1
External Clock "High" Level Width	t_{CPH}	OSC_1		205	–	–	ns	2
External Clock "Low" Level Width	t_{CPL}	OSC_1		205	–	–	ns	2
External Clock Rise Time	t_{CPr}	OSC_1		–	–	20	ns	2
External Clock Fall Time	t_{CPf}	OSC_1		–	–	20	ns	2
$\overline{INT_0}$ "High" Level Width	t_{I0H}	$\overline{INT_0}$		2	–	–	t_{cyc}	3
$\overline{INT_0}$ "Low" Level Width	t_{I0L}	$\overline{INT_0}$		2	–	–	t_{cyc}	3
$\overline{INT_1}$ "High" Level Width	t_{I1H}	$\overline{INT_1}$		2	–	–	t_{cyc}	3
$\overline{INT_1}$ "Low" Level Width	t_{I1L}	$\overline{INT_1}$		2	–	–	t_{cyc}	3
RESET "High" Level Width	t_{RSTH}	RESET		2	–	–	t_{cyc}	4
Input Capacitance	C_{in}	all pins	f = 1 MHz V_{in} = 0 V	–	–	15	pF	
RESET Fall Time	t_{RSTf}			–	–	15	ms	4

(Note 1) Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 2.7V at "Power-on", or after RESET input level goes "High" by resetting to quit the stop mode by MCU reset. The circuits used to measure the value are described below. When using crystal or ceramic filter oscillator, please ask a crystal oscillator maker's or ceramic filter maker's advice because oscillator stabilization time depends on the circuit constant and stray capacity.

Crystal oscillator



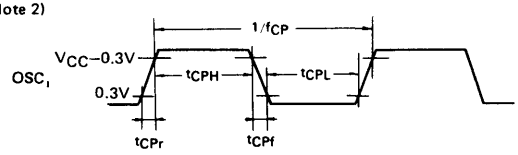
Ceramic filter oscillator



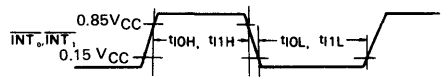
Crystal: 2.097152MHz DS-MGQ308 (Seiko Denshi)
Rf = 2MΩ ± 2%, Rd = 2.2kΩ ± 2%
C_1 = 10pF ± 20%
C_2 = 10pF ± 20%

Ceramic filter: CSA2.000MK (Murata)
Rf = 1MΩ ± 2%, C_1 = C_2 = 30pF ± 20%

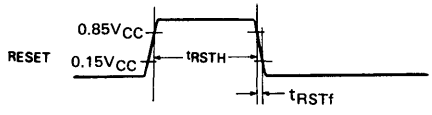
(Note 2)



(Note 3)



(Note 4)



• SERIAL INTERFACE TIMING CHARACTERISTICS

(V_{CC}=2.7V to 6V, GND = 0V, V_{disp} = V_{CC}−40V to V_{CC}, Ta = −20 to +75°C, if not specified.)

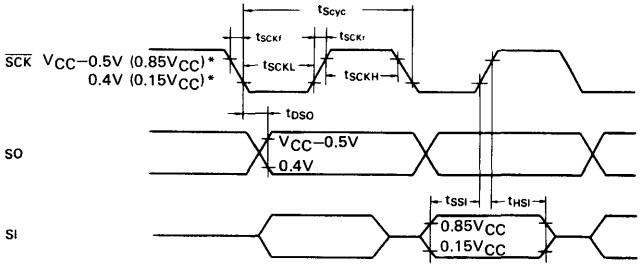
- At Transfer Clock Output

Item	Symbol	Pin Name	Test Conditions	Value min	Value typ	Value max	Unit	Note
Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$	(Note 2)	1	–	–	t_{cyc}	1, 2
Transfer Clock "High" Level Width	t_{SCKH}	$\overline{SCK}$	(Note 2)	0.5	–	–	t_{Scyc}	1, 2
Transfer Clock "Low" Level Width	t_{SCKL}	$\overline{SCK}$	(Note 2)	0.5	–	–	t_{Scyc}	1, 2
Transfer Clock Rise Time	t_{SCKr}	$\overline{SCK}$	(Note 2)	–	–	300	ns	1, 2
Transfer Clock Fall Time	t_{SCKf}	$\overline{SCK}$	(Note 2)	–	–	300	ns	1, 2
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	–	–	600	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		1000	–	–	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		500	–	–	ns	1

- At Transfer Clock Input

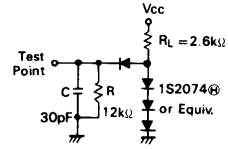
Item	Symbol	Pin Name	Test Conditions	Value min	Value typ	Value max	Unit	Note
Transfer Clock Cycle Time	t_{Scyc}	$\overline{SCK}$		1	–	–	t_{cyc}	1
Transfer Clock "High" Level Width	t_{SCKH}	$\overline{SCK}$		0.5	–	–	t_{Scyc}	1
Transfer Clock "Low" Level Width	t_{SCKL}	$\overline{SCK}$		0.5	–	–	t_{Scyc}	1
Transfer Clock Rise Time	t_{SCKr}	$\overline{SCK}$		–	–	300	ns	1
Transfer Clock Fall Time	t_{SCKf}	$\overline{SCK}$		–	–	300	ns	1
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	–	–	600	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		1000	–	–	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		500	–	–	ns	1

(Note 1) Timing Diagram of Serial Interface

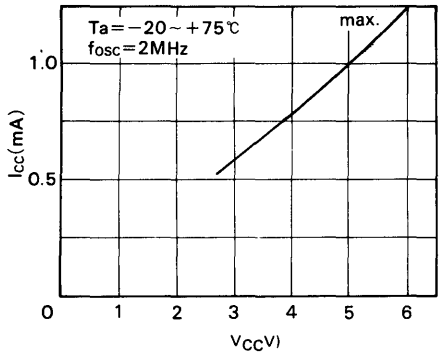


*V_{CC}−0.5V and 0.4V are the threshold voltage for transfer clock output.
0.85V_{CC} and 0.15V_{CC} are the threshold voltage for transfer clock input.

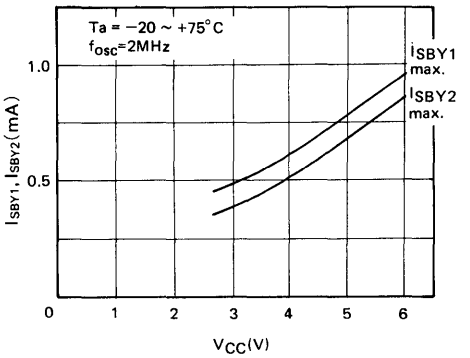
(Note 2) Timing Load Circuit



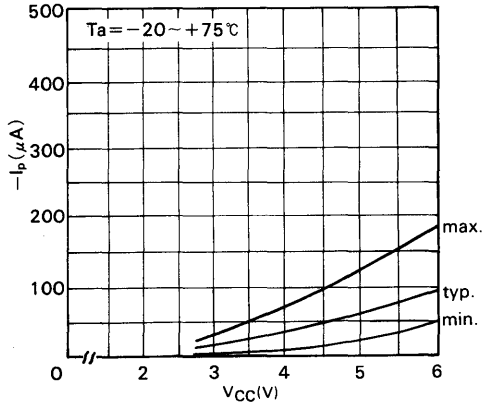
■ CHARACTERISTICS CURVE (REFERENCE DATA)



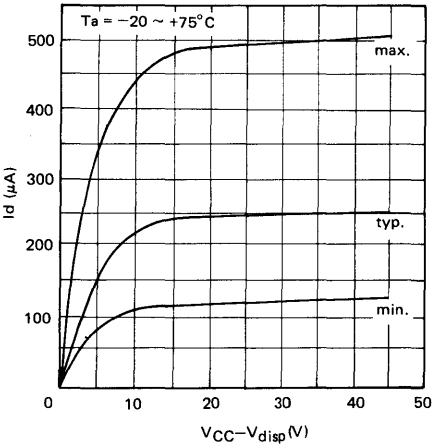
I_{CC} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator)



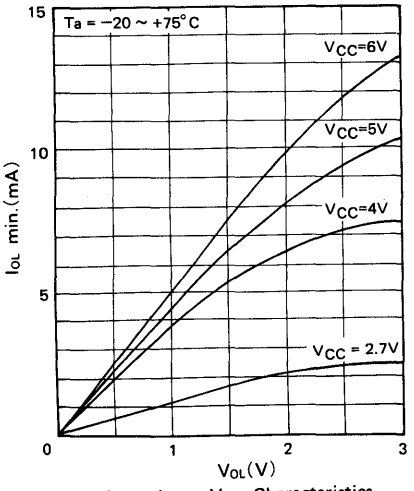
I_{SBY} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator)



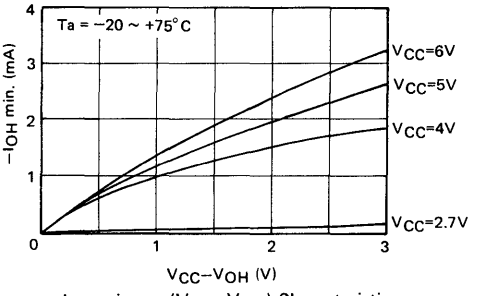
$-I_p$ (Pull-up MOS Current) vs.
V_{CC} Characteristics



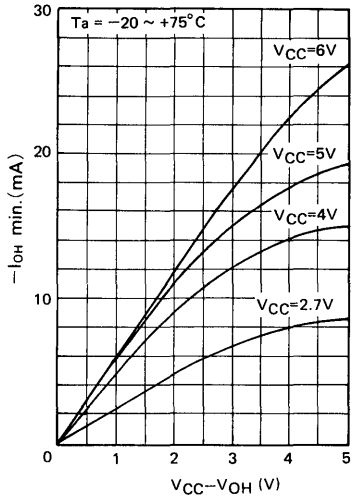
I_d (Pull-down MOS Current) vs.
($V_{CC}-V_{disp}$) Characteristics



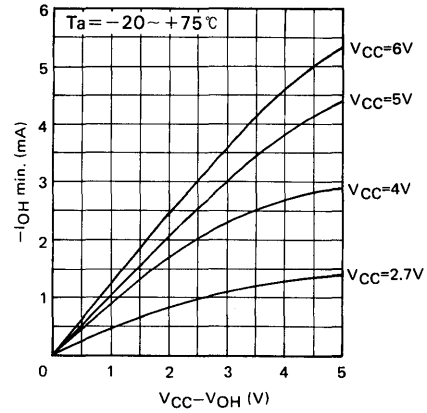
I_{OL} min. vs. V_{OL} Characteristics
(Standard Pin)



$-I_{OH}$ min. vs. ($V_{CC}-V_{OH}$) Characteristics
(Standard Pin "CMOS")



$-I_{OH}$ min. vs. ($V_{CC}-V_{OH}$) Characteristics
($D_4 \sim D_{15}$ Pins)



$-I_{OH}$ min. vs. ($V_{CC}-V_{OH}$) Characteristics
(R0 ~ R2 Pins)

■ DESCRIPTION OF PIN FUNCTIONS

Input and output signals of MCU are described below.

- **GND, V_{CC}, V_{disp}**

These are Power Supply Pins. Connect GND pin to Earth (0V) and apply V_{CC} power supply voltage to V_{CC} pin. V_{disp} is an power supply for high voltage Input/Output pins with maximum voltage of V_{CC}-40V. V_{disp} pin can be also used as R_{A1} pin by mask option. For details, see "INPUT/OUTPUT".

- **$\overline{TEST}$**

$\overline{TEST}$ pin is not for user's application. $\overline{TEST}$ must be connected to V_{CC}.

- **RESET**

RESET pin is used to reset MCU. For details, see "RESET".

- **OSC_1, OSC_2**

These are Input pins to the internal oscillator circuit. They can be connected to crystal, or ceramic filter resonator. For details, see "INTERNAL OSCILLATOR CIRCUIT."

- **D-port (D_0 to D_{15})**

D-port is a 1-bit Input/Output common port. D_0 to D_3 are standard type, D_4 to D_{15} are for high voltage. Each pin has the mask option to select its circuit type. For details, See "INPUT/OUTPUT".

- **R-port (R0 to RA)**

R-port is a 4-bit Input/Output port. (only RA is 2-bit construction.) R0 and R6 to R8 are output ports, R9 to RA are input ports, and R1 to R5 are Input/Output common ports. R0 to R2 and RA are the high voltage ports, R3 to R9 are the standard ports. Each pin has the mask option to select its circuit type. R_{32}, R_{33}, R_{40}, R_{41} and R_{42} are also available as $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK}$, SI and SO respectively. For details, see "INPUT/OUTPUT".

- **$\overline{INT_0}$, $\overline{INT_1}$**

These are the input pins to interrupt MCU operation externally. $\overline{INT_1}$ can be used as an external event input pin for TIMER-B. $\overline{INT_0}$ and $\overline{INT_1}$ are also available as R_{32}, and R_{33} respectively. For details, See "INTERRUPT".

- **$\overline{SCK}$, SI, SO**

These are Transfer clock I/O pin ($\overline{SCK}$), serial data input pin (SI) and serial data output pin (SO) used for serial interface. $\overline{SCK}$, SI, and SO are also available as R_{40}, R_{41} and R_{42} respectively. For details, see "SERIAL INTERFACE".

■ ROM MEMORY MAP

MCU includes 4096 words × 10 bits ROM. ROM memory map is illustrated in Fig. 1 and described in the following paragraph.

- **Vector Address Area ..... $0000 to $000F**

When MCU is reset or an interrupt is serviced, the program is executed from the vector address. Program the JMPL instructions branching to the starting addresses of reset routine or of interrupt routines.

- **Zero-Page Subroutine Area ..... $0000 to $003F**

CAL instruction allows to branch to the subroutines in $0000 to $003F.

- **Pattern Area ..... $0000 to $0FFF**

P instruction allows referring to the ROM data in $0000 to $0FFF as a pattern.

- **Program Area ..... $0000 to $0FFF**

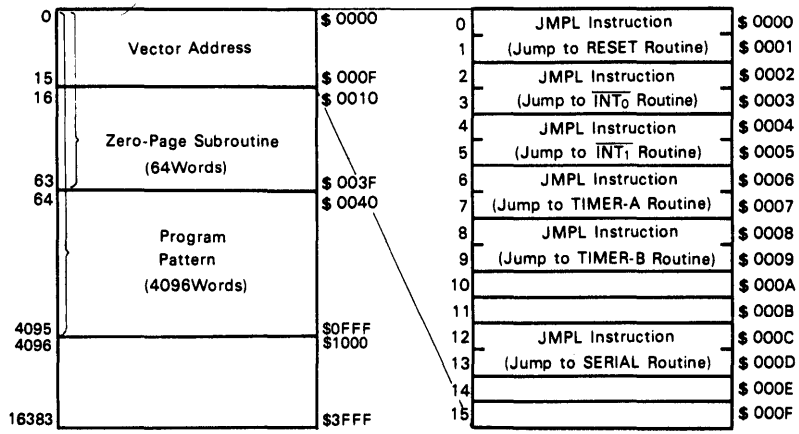
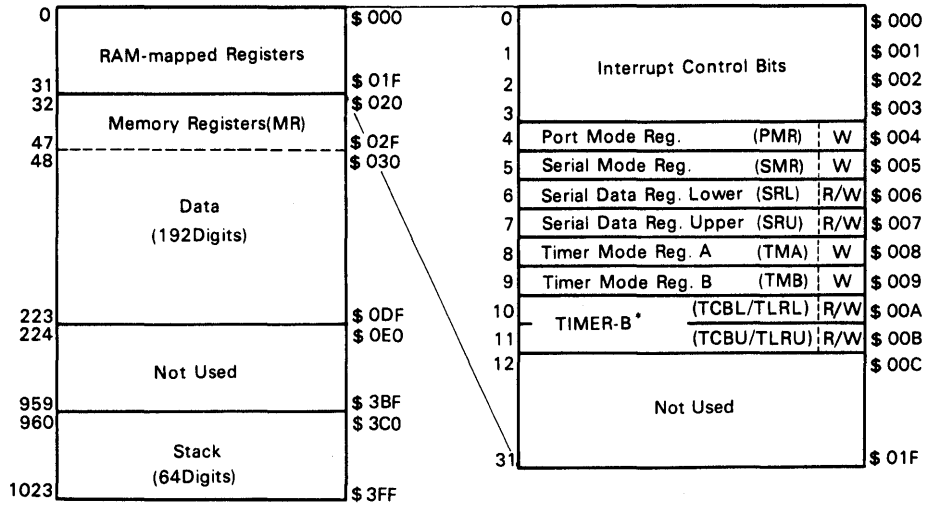


Fig. 1 ROM Memory Map

■ RAM MEMORY MAP

MCU includes 256 digits × 4 bits RAM as the data area and stack area. In addition to these areas, interrupt control bits and special registers are also mapped on the RAM memory space. RAM memory map is illustrated in Fig. 2 and described in the following paragraph.



* Two registers are mapped on same address.

R :Read Only
W :Write Only
R/W:Read/Write

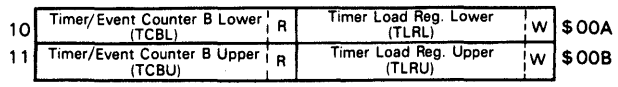


Fig. 2 RAM Memory Map

	bit 3	bit 2	bit 1	bit 0	
0	IMO (IM of $\overline{INT_0}$)	IFO (IF of $\overline{INT_0}$)	RSP (Reset SP Bit)	I/E (Interrupt Enable Flag)	$000
1	IMTA (IM of TIMER-A)	IFTA (IF of TIMER-A)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	Not Used	Not Used	IMTB (IM of TIMER-B)	IFTB (IF of TIMER-B)	$002
3	Not Used	Not Used	IMS (IM of SERIAL)	IFS (IF of SERIAL)	$003

IF : Interrupt Request Flag
IM : Interrupt Mask
I/E : Interrupt Enable Flag
SP : Stack Pointer
(Note) Each bit in Interrupt Control Bits Area is set by SEM/SEMD instruction, is reset by REM/REMD instruction and is tested by TM/TMD instruction. It is not affected by other instructions. Furthermore, Interrupt Request Flag is not affected by SEM/SEMD instruction. The content of Status becomes invarid when "Not Used" bit is tested.

Fig. 3 Configuration of Interrupt Control Bit Area

- **Interrupt Control Bit Area ..... $000 to $003**

This area is used for interrupt controls, and is illustrated in Fig.3. It is accessable only by RAM bit manipulation instruction. However, the interrupt request flag cannot be set by software.

- **Special Register Area ..... $004 to $00B**

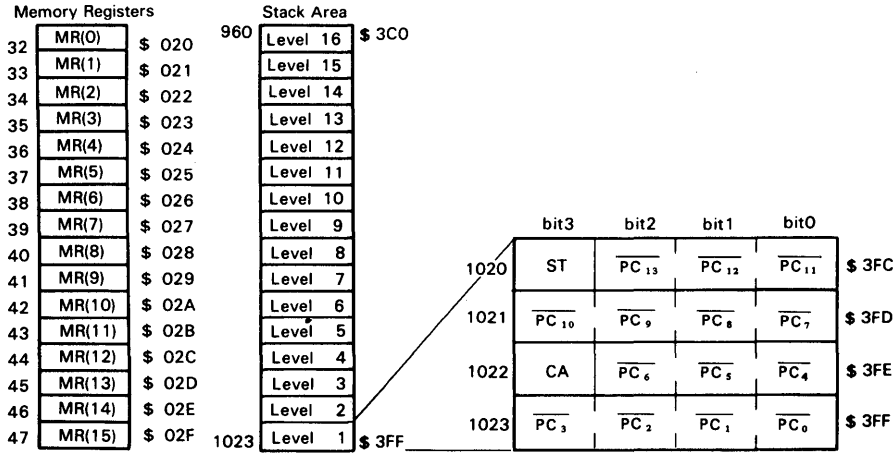
Special Register is a mode or a data register for the external interrupt, the serial interface, and the timer/counter. These registers are classified into 3 types: Write-only, Read-only, and Read/Write as shown in Fig. 2. These registers cannot be accessed by RAM bit manipulation instruction.

- **Data Area ..... $020 to $0DF**

16 digits of $020 to $02F are called memory register (MR) and accessable by LAMR and XMRA instructions.

- **Stack Area .... $3C0 to $3FF**

Stack Area is used for LIFO stacks with the contents of the program counter (PC), status (ST) and carry (CA) when processing subroutine call and interrupt. As 1 level requires 4 digits, this stack area is nested to 16 level-stack max. The data pushed in the stack and LIFO stack state are provided in Fig. 4. The program counter is restored by RTN and RTNI instructions. Status and Carry are restored only by RTNI instruction. The area, not used for stacking, is available as a data area.



PC_{13} to PC_0 ; Program Counter
ST; Status
CA; Carry

Fig. 4 Configuration of Memory Register, Stack Area and Stack Position

■ REGISTER AND FLAG

The MCU has nine registers and two flags for the CPU operations. They are illustrated in Fig. 5 and described in the following paragraphs.

• Accumulator (A), B Register (B)

Accumulator and B Register are 4-bit registers used to hold the results of Arithmetic Logic Unit (ALU), and to transfer data to/from memories, I/O and other registers.

• W Register (W), X Register (X), Y Register (Y)

W Register is 2-bit, and X and Y Register are 4-bit registers used for indirect addressing of RAM. Y register is also used for D-port addressing.

• SPX Register (SPX), SPY Register (SPY)

SPX and SPY Register are 4-bit registers used to assist X and Y Register respectively.

• Carry (CA)

Carry (CA) stores the overflow of ALU generated by the arithmetic operation. It is also affected by SEC, REC, ROTL and ROTR instructions.

During interrupt servicing, Carry is pushed onto the stack and restored back from the stack by RTNI instruction. (It's not affected by RTN instruction.)

• Status (ST)

Status (ST) holds the ALU overflow, ALU non-zero and the results of bit test instruction for the arithmetic or compare instruction. It is used for a branch condition of BR, BRL, CAL or CALL instructions. The value of the Status remains unchanged until the next arithmetic, compare or bit test instruction is executed. Status becomes "1" after the BR, BRL, CAL or CALL instruction has been executed (irrespective of its execution/skip). During the interrupt servicing, Status is pushed onto the stack and restored back from the stack by RTNI instruction. (It's not affected by RTN instruction.)

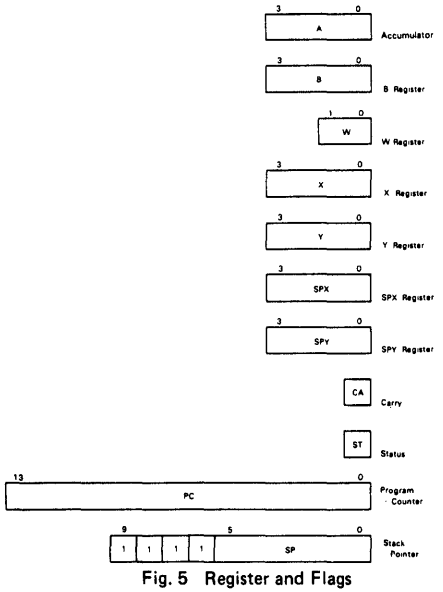


Fig. 5 Register and Flags

• Program Counter (PC)

Program Counter is a 14-bit binary counter for ROM addressing.

• Stack Pointer (SP)

Stack Pointer is used to point the address of the next stacking area up to 16 levels.

The Stack Pointer is initialized to locate $3FF on the RAM address, and is decremented by 4 as data pushed into the stack, and incremented by 4 as data restored back from the stack.

■ INTERRUPT

The MCU can be interrupted by five different sources: the external signals ($\overline{INT_0}$, $\overline{INT_1}$), timer/counter (TIMER-A, TIMER-B), and serial interface (SERIAL). In each sources, the Interrupt Request Flag, Interrupt Mask and interrupt vector address will be used to control and maintain the interrupt request. The Interrupt Enable Flag is also used to control the total interrupt operations.

• Interrupt Control Bit and Interrupt Service

The interrupt control bit is mapped on $000 to $003 of the RAM address and accessable by RAM bit manipulation instruction. (The Interrupt Request Flag (IF) cannot be set by software.) The Interrupt Enable Flag (I/E) and Interrupt Request Flag (IF) are set to "0", and the Interrupt Mask (IM) is set to "1" at the initialization by MCU reset.

Fig. 6 shows the interrupt block diagram. Table 1 shows the interrupt priority and vector addresses, and Table 2 shows the conditions that the interrupt service is executed by any one of the five interrupt sources.

The interrupt request is generated when the Interrupt Request Flag is set to "1" and the Interrupt Mask is "0". If the Interrupt Enable Flag is "1", then the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the five interrupt sources.

Fig. 7 shows the interrupt services sequence, and Fig. 8 shows the interrupt flowchart. If the interrupt is requested, the instruction finishes its execution in the first cycle. The Interrupt Enable Flag is reset in the second cycle. In the second and third cycles, the Carry, Status and Program Counter are pushed onto the stack. In the third cycle, the instruction is executed again after jumping to the vector address.

In each vector address, program JMPL instruction to branch to a starting address of the interrupt routine. The Interrupt Request Flag which caused the interrupt service has to be reset by software in the interrupt routine.

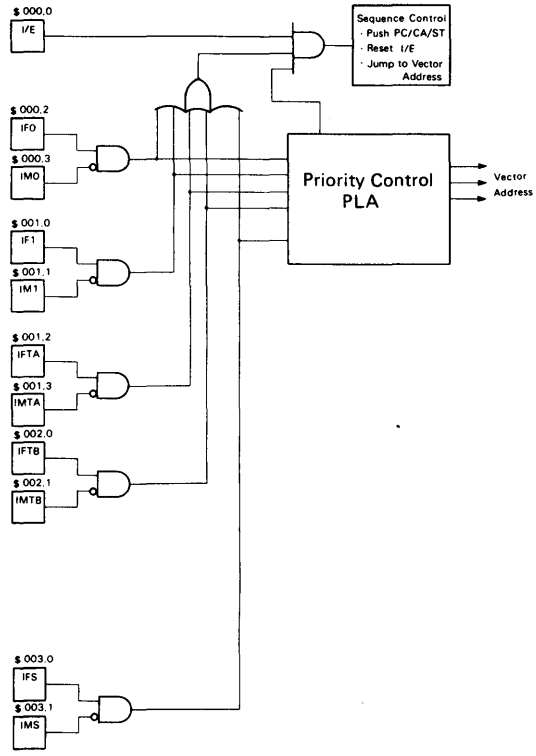


Fig. 6 Interrupt Circuit Block Diagram

Table 1. Vector Addresses and Interrupt Priority

Reset · Interrupt	Priority	Vector addresses
RESET	–	$0000
$\overline{INT_0}$	1	$0002
$\overline{INT_1}$	2	$0004
TIMER-A	3	$0006
TIMER-B	4	$0008
SERIAL	5	$000C

Table 2. Conditions of Interrupt Service

Interrupt control bits \ Interrupt source	$\overline{INT_0}$	$\overline{INT_1}$	TIMER-A	TIMER-B	SERIAL
I/E	1	1	1	1	1
IF0·$\overline{IM0}$	1	0	0	0	0
IF1 · $\overline{IM1}$	*	1	0	0	0
IFTA · $\overline{IMTA}$	*	*	1	0	0
IFTB · $\overline{IMTB}$	*	*	*	1	0
IFS · $\overline{IMS}$	*	*	*	*	1

* Don't care

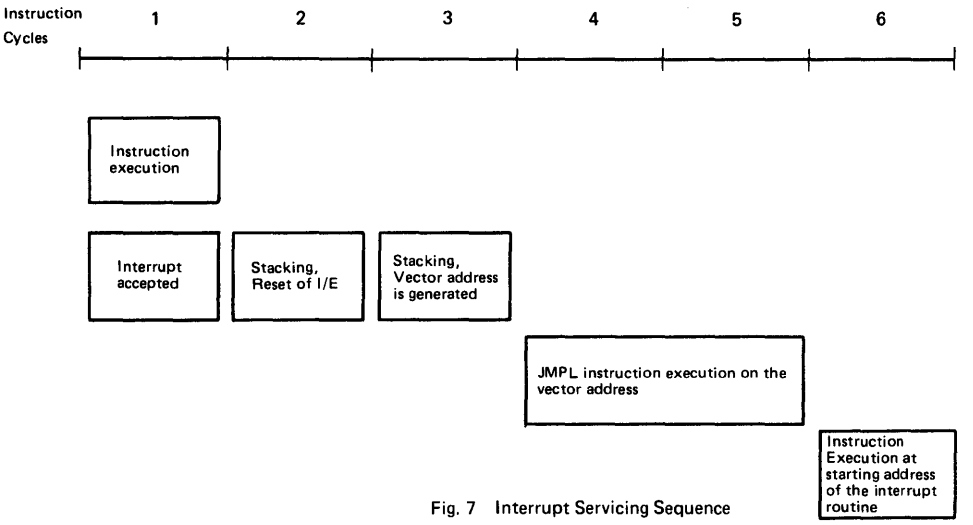


Fig. 7 Interrupt Servicing Sequence

- **Interrupt Enable Flag (I/E: $000,0)**

The Interrupt Enable Flag controls enable/disable of all interrupt requests as shown in Table 3. The Interrupt Enable Flag is reset by the interrupt servicing and set by RTNI instruction.

Table 3. Interrupt Enable Flag

Interrupt Enable Flag	Interrupt Enable/Disable
0	Disable
1	Enable

- **External Interrupt ($\overline{INT_0}$, $\overline{INT_1}$)**

To use external interrupt, select $R_{32}/\overline{INT_0}$, $R_{33}/\overline{INT_1}$ port for $\overline{INT_0}$, $\overline{INT_1}$ mode by setting the Port Mode Register (PMR: $004).

The External Interrupt Request Flags (IF0, IF1) are set at the falling edge of $\overline{INT_0}$, $\overline{INT_1}$ inputs.

$\overline{INT_1}$ input can be used as a clock signal input of TIMER-B. Then, TIMER-B counts up at each falling edge of input. When using $\overline{INT_1}$ as TIMER-B external event, an External Interrupt Mask (IM1) has to be set so that the interrupt request by $\overline{INT_1}$ will not be accepted.

- **External Interrupt Request Flag (IF0: $000,2, IF1: $001,0)**

The External Interrupt Request Flags (IF0, IF1) are set at the falling edges of $\overline{INT_0}$, $\overline{INT_1}$ inputs respectively.

- **External Interrupt Mask (IM0: $000,3, IM1: $001,1)**

The External Interrupt Mask is used to mask the external interrupt requests.

Table 4. External Interrupt Request Flag

External Interrupt Request Flags	Interrupt Requests
0	No
1	Yes

Table 5. External Interrupt Mask

External Interrupt Masks	Interrupt Requests
0	Enable
1	Disable (masks)

- **Port Mode Register (PMR: $004)**

The Port Mode Register is a 4-bit write-only register which controls the $R_{32}/\overline{INT_0}$ pin, $R_{33}/\overline{INT_1}$ pin, R_{41}/SI pin and R_{42}/SO pin as shown in Table 6. The Port Mode Register will be initialized to $0 by MCU reset, so that all these pins are set to a port mode.

Table 6. Port Mode Register

PMR bit 3	$R_{33}/\overline{INT_1}$ pin
0	Used as R_{33} port input/output pin
1	Used as $\overline{INT_1}$ input pin

PMR bit 2	$R_{32}/\overline{INT_0}$ pin
0	Used as R_{32} port input/output pin
1	Used as $\overline{INT_0}$ input pin

PMR bit 1	R_{41}/SI pin
0	Used as R_{41} port input/output pin
1	Used as SI input pin

PMR bit 0	R_{42}/SO pin
0	Used as R_{42} port input/output pin
1	Used as SO output pin

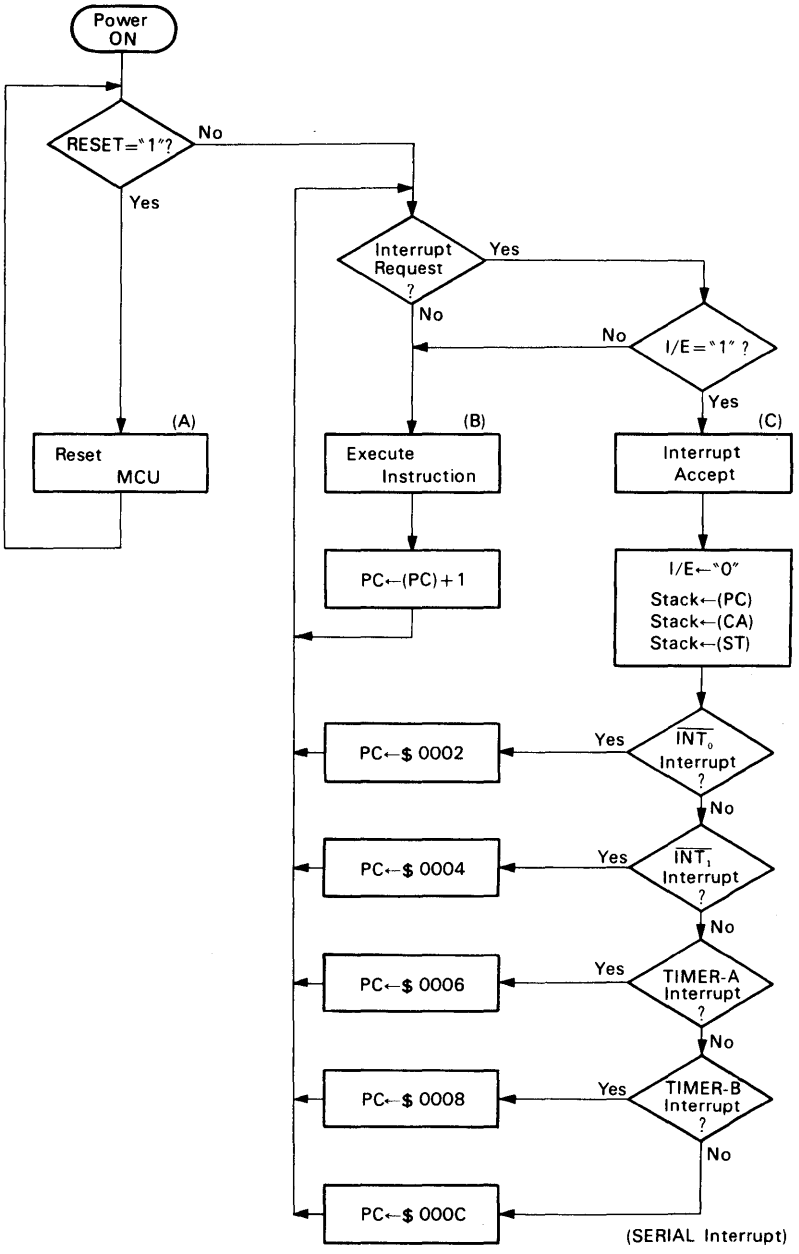


Fig. 8 Interrupt Servicing Flowchart

■ SERIAL INTERFACE

The serial interface is used to transmit/receive 8-bit data serially. This consists of the Serial Data Register, the Serial Mode Register, the Octal Counter and the multiplexer, as illustrated in Fig. 9. Pin $R_{40}/\overline{SCK}$ and the transfer clock signal are controlled by the Serial Mode Register. Contents of the Serial Data Register can be written into or read out by the software. The data in the Serial Data Register can be shifted synchronously with the transfer clock signal.

The serial interface operation is initiated with STS instruction. The Octal Counter is reset to $0 by STS instruction. It starts to count at the falling edge of the transfer clock ($\overline{SCK}$) signal and increments by one at the rising edge of the $\overline{SCK}$. When the Octal Counter is reset to $0 after eight transfer clock signals, or discontinued transmit/receive operation by resetting the Octal Counter, the SERIAL Interrupt Request Flag will be set.

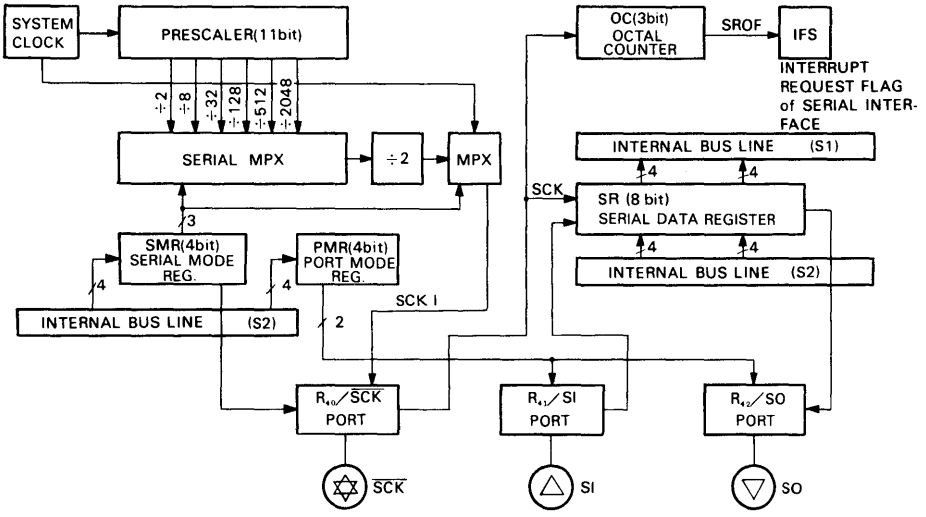


Fig. 9 Serial Interface Block Diagram

• Serial Mode Register (SMR: $005)

The Serial Mode Register is a 4-bit write-only register. This register controls the $R_{40}/\overline{SCK}$ and the prescaler divide ratio as the transfer clock source as shown in Table 7.

The Write Signal to the Serial Mode Register controls the operating state of serial interface.

The Write Signal to the Serial Mode Register stops the transfer clock applied to the Serial Data Register and the Octal Counter. And it also reset the Octal Counter to $0 simultaneously.

When the Serial Interface is in the "Transfer State", the Write Signal to the Serial Mode Register causes to quit the data transfer and to set the SERIAL Interrupt Request Flag.

Contents of the Serial Mode Register will be changed on the second instruction cycle after writing into the Serial Mode Register. Therefore, it will be necessary to execute the STS instruction after the data in the Serial Mode Register has been changed completely. The Serial Mode Register will be reset to $0 by MCU reset.

• Serial Data Register (SRL: $006, SRU: $007)

The Serial Data Register is an 8-bit read/write register. It consists of a low-order digit (SRL:$006) and a high-order digit (SRU: $007).

The data in the Serial Data Register will be output from the LSB side at SO pin synchronously with the falling edge of the transfer clock signal. At the same time, external data will be input from the LSB side at SI pin to the Serial Data Register synchronously with the rising edge of the transfer clock. Fig. 10 shows the I/O timing chart for the transfer clock signal and the data.

The writing into/reading from the Serial Data Register during its shifting causes the validity of the data.

Therefore complete data transmit/receive before writing into/reading from the serial data register.

Table 7. Serial Mode Register

SMR Bit 3	$R_{40}/\overline{SCK}$
0	Used as R_{40} port input/output pin
1	Used as $\overline{SCK}$ input/output pin

SMR			Transfer Clock			
Bit 2	Bit 1	Bit 0	$R_{40}/\overline{SCK}$ Port	Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio
0	0	0	$\overline{SCK}$ Output	Prescaler	÷ 2048	÷ 4096
0	0	1	$\overline{SCK}$ Output	Prescaler	÷ 512	÷ 1024
0	1	0	$\overline{SCK}$ Output	Prescaler	÷ 128	÷ 256
0	1	1	$\overline{SCK}$ Output	Prescaler	÷ 32	÷ 64
1	0	0	$\overline{SCK}$ Output	Prescaler	÷ 8	÷ 16
1	0	1	$\overline{SCK}$ Output	Prescaler	÷ 2	÷ 4
1	1	0	$\overline{SCK}$ Output	System Clock	–	÷ 1
1	1	1	$\overline{SCK}$ Input	External Clock	–	–

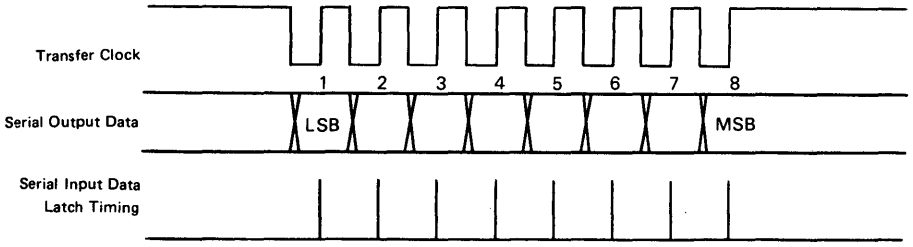


Fig. 10 Serial Interface I/O Timing Chart

- **SERIAL Interrupt Request Flag (IFS: $003, 0)**

The SERIAL Interrupt Request Flag will be set after the eight transfer clock signals or transmit/receive discontinued operation by resetting the Octal Counter.

- **SERIAL Interrupt Mask (IMS: $003, 1)**

The SERIAL Interrupt Mask masks the interrupt request.

Table 8. SERIAL Interrupt Request Flag

SERIAL Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 9. SERIAL Interrupt Mask

SERIAL Interrupt Mask	Interrupt Request
0	Enable
1	Disable (mask)

- **Selection of the Operation Mode**

Table 10 shows the operation mode of the serial interface. Select a combination of the value in the Port Mode Register and the Serial Mode Register according to Table 10.

Initialize the serial interface by the Write Signal to the Serial Mode Register, when the Operation Mode is changed.

- **Operating State of Serial Interface**

The serial interface has 3 operating states as shown in Fig. 11.

The serial interface gets into "STS waiting state" by 2 ways: one way is to change the operation mode by changing the data

in the Port Mode Register, the other is to write data into the Serial Mode Register. In this state, the serial interface does not operate although the transfer clock is applied. If STS instruction is executed, the serial interface changes its state to "SCK waiting state".

In the "SCK waiting state", the falling edge of first transfer clock affects the serial interface to get into "transfer state", while the Octal Counter counts-up and the Serial Data Register shifts simultaneously. As an exception, if the clock continuous output mode is selected, the serial interface stays in "SCK waiting state" while the transfer clock outputs continuously.

The Octal Counter becomes "000" again by 8 transfer clocks or execution of STS instruction, so that the serial interface gets back into the "SCK waiting state", and SERIAL Interrupt Request Flag is set simultaneously.

When the internal transfer clock is selected, the transfer clock output are triggered by the execution of STS instruction, and it stops after 8 clocks.

- **Example of Transfer Clock Error Detection**

The serial interface functions abnormally when the transfer clock was disturbed by external noises. In this case, the transfer clock error can be detected in the procedure shown in Fig. 12.

If more than 9 transfer clocks are applied by the external noises in the "SCK waiting state", the state of the serial interface shifts as the following sequence: first "transfer state" (while 1 to 7 transfer clocks), second "SCK waiting state" (at 8th transfer clock) and third "transfer state" again. Then reset the SERIAL Interrupt Request Flag, and make "STS waiting state" by writing to the Serial Mode Register. SERIAL Interrupt Request Flag is set again in this procedure, and it shows that the transfer clock was invalid and that the transmit/receive data were also invalid.

Table 10. Serial Interface Operation Mode

SMR	PMR		Serial Interface Operating Mode
Bit 3	Bit 1	Bit 0	
1	0	0	Clock Continuous Output Mode
1	0	1	Transmit Mode
1	1	0	Receive Mode
1	1	1	Transmit/Receive Mode

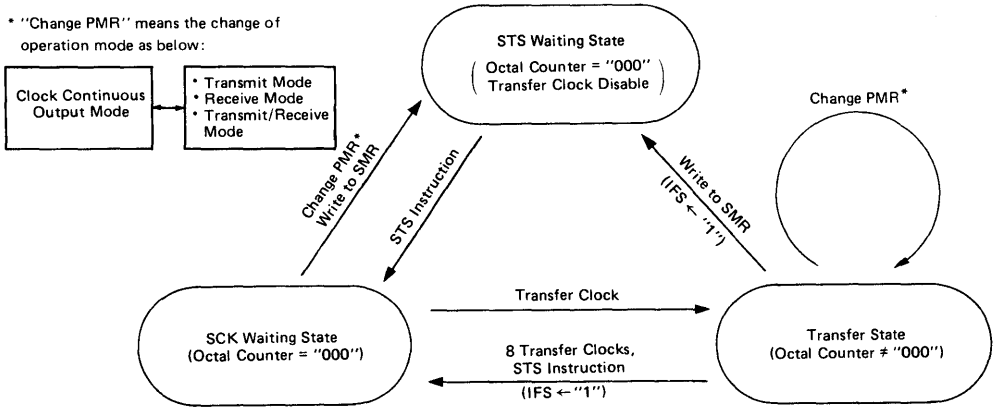


Fig. 11 Serial Interface Operation State

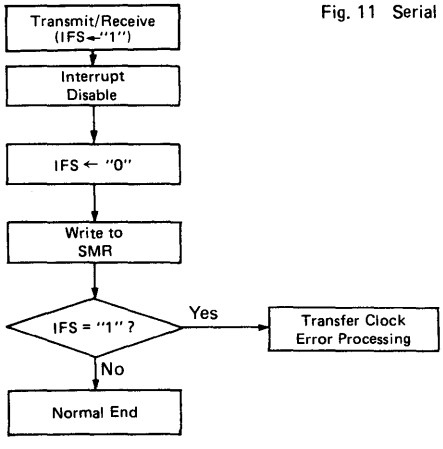


Fig. 12 Example of Transfer Clock Error Detection

- **TIMER**

The MCU contains a prescaler and two timer/counters (TIMER-A, TIMER-B), Fig. 13 shows the block diagram. The prescaler is an 11-bit binary counter. TIMER-A is an 8-bit free-running timer. TIMER-B is an 8-bit auto-reload timer/event counter.

- **Prescaler**

The input to the prescaler is a system clock signal. The prescaler is initialized to $000 by MCU reset, and the prescaler starts to count up the system clock signal as soon as RESET input goes to logic "0". The prescaler keeps counting up except MCU reset and stop mode. The prescaler provides clock signals to TIMER-A, TIMER-B and serial interface. The prescaler devide ratio of the clock signals are selected according to the content of the mode registers such as – Timer Mode Register A (TMA), Timer Mode Register B (TMB), Serial Mode Register (SMR).

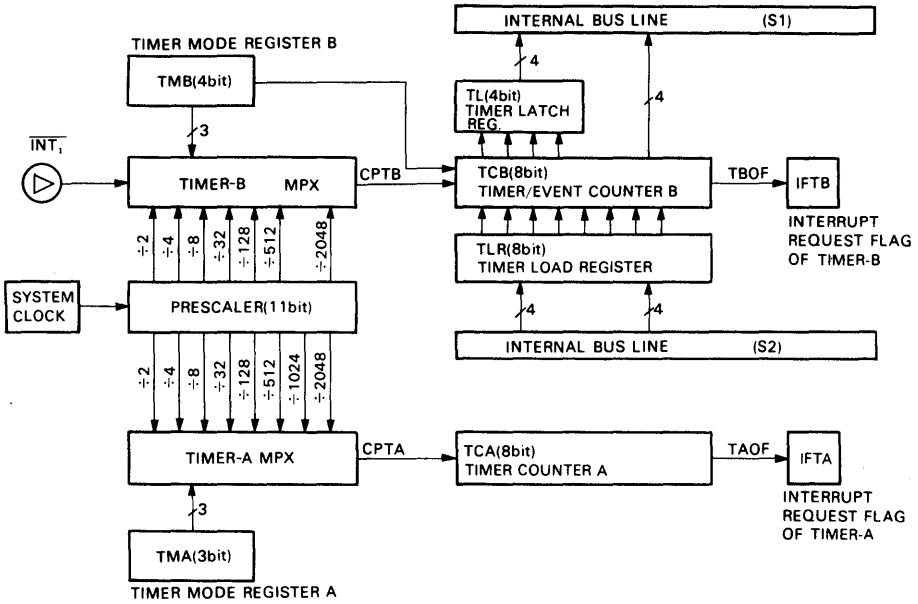


Fig. 13 Timer/Counter Block Diagram

- **TIMER-A Operation**

After TIMER-A is initialized to $00 by MCU reset, it counts up at every clock input signal. When the next clock signal is applied after TIMER-A is counted up to $FF, TIMER-A is set to $00 again, and generating overflow output. This leads to setting TIMER-A Interrupt Request Flag (IFTA: $001, 2) to "1". Therefore, this timer can function as an interval timer periodically generating overflow output at every 256th clock signal input.

The clock input signals to TIMER-A are selected by the Timer Mode Register A (TMA: $008).

- **TIMER-B Operation**

Timer Mode Register B (TMB: $009) is used to select the auto-reload function and the prescaler divide ratio of TIMER-B as the input clock source. When the external event input is used as an input clock signal to TIMER-B, select the $R_{33}/\overline{INT_1}$ as $\overline{INT_1}$ and set the External Interrupt Mask (IM1) to "1" to prevent the external interrupt request from occurring.

TIMER-B is initialized according to the value written into the Timer Load Register by software. TIMER-B counts up at every clock input signal. When the next clock signal is applied to TIMER-B after TIMER-B is set to $FF, TIMER-B will be initialized again and generate overflow output. In this case if the auto-reload function is selected. TIMER-B is initialized according to the value of the Timer Load Register. Else if the auto-reload function is not selected, TIMER-B goes to $00. TIMER-B Interrupt Request Flag (IFTB: $002,0) will be set at this overflow output.

- **Timer Mode Register A (TMA: $008)**

The Timer Mode Register A is a 3-bit write-only register. The TMA controls the prescaler divide ratio of TIMER-A clock input, as shown in Table 11.

The Timer Mode Register A is initialized to $0 by MCU reset.

- **Timer Mode Register B (TMB: $009)**

The Timer Mode Register B is a 4-bit write-only register. The Timer Mode Register B controls the selection for the auto-reload function of TIMER-B and the prescaler divide ratio, and the source of the clock input signal, as shown in Table 12.

The Timer Mode Register B is initialized to $0 by MCU reset.

The operation mode of TIMER-B is changed at the second instruction cycle after writing into the Timer Mode Register B.

Therefore, it is necessary to program the write instruction to TLRU after the content of TMB is changed.

Table 11. Timer Mode Register A

TMA			Prescaler Divide Ratio
Bit 2	Bit 1	Bit 0	
0	0	0	÷2048
0	0	1	÷1024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	0	÷ 32
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2

Table 12. Timer Mode Register B

TMB Bit 3	Auto-reload Function
0	No
1	Yes

TMB Bit 2	TMB Bit 1	TMB Bit 0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	$\overline{INT_1}$ (External Event Input)

- **TIMER-B (TCBL: $00A, TCBU: $00B / TLRL: $00A, TLRU: $00B)**

TIMER-B consists of an 8-bit write-only Timer Load Register, and an 8-bit read-only Timer/Event Counter. Each of them has a low-order digit (TCBL: $00A, TLRL: $00A) and a high-order digit (TCBU: $00B, TLRU: $00B).

The Timer/Event Counter can be initialized by writing data into the Timer Load Register. In this case, write the low-order digit first, and then the high-order digit. The Timer/Event Counter is initialized at the time when the high-order digit is written. The Timer Load Register will be initialized to $00 by the MCU reset.

The counter value of TIMER-B can be obtained by reading the Timer/Event Counter. In this case, read the high-order digit first, and then the low-order digit. The count value of low-order digit is latched at the time when the high-order digit is read.

- **TIMER-A Interrupt Request Flag (IFTA: $001, 2)**

The TIMER-A Interrupt Request Flag is set by the overflow output of TIMER-A.

- **TIMER-A Interrupt Mask (IMTA: $001, 3)**

TIMER-A Interrupt Mask prevents an interrupt request generated by TIMER-A Interrupt Request Flag.

Table 13. TIMER-A Interrupt Request Flag

TIMER-A Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 14. TIMER-A Interrupt Mask

TIMER-A Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

- **TIMER-B Interrupt Request Flag (IFTB: $002, 0)**

The TIMER-B Interrupt Request Flag is set by the overflow output of TIMER-B.

- **TIMER-B Interrupt Mask (IMTB: $002, 1)**

TIMER-B Interrupt Mask prevents an interrupt request generated by TIMER-B Interrupt Request Flag.

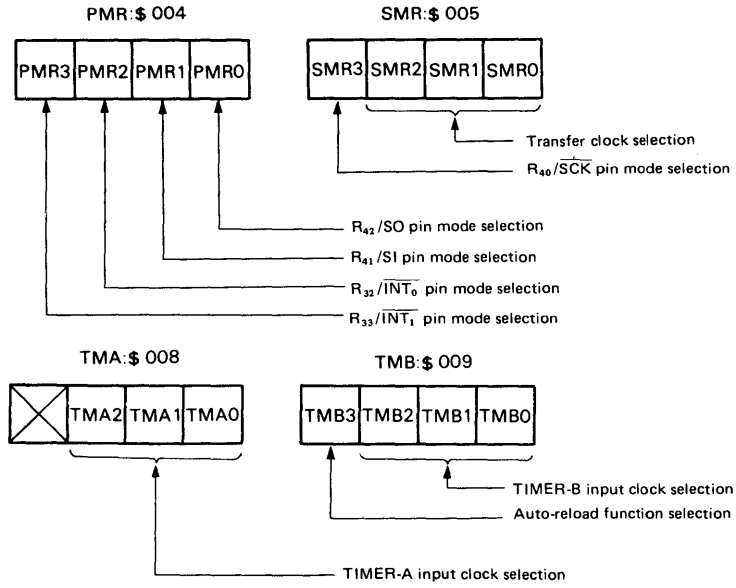


Fig. 14 Mode Register Configuration and Function

Table 15. TIMER-B Interrupt Request Flag

TIMER-B Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 16. TIMER-B Interrupt Mask

TIMER-B Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

■ INPUT/OUTPUT

The MCU provides 58 Input/Output pins, and they are consist of 32 standard pins and 26 high voltage pins. Each standard pin may have one of three mask options: (A) "Without pull-up MOS (NMOS open drain)", (B) "With pull-up MOS", or (C) "CMOS". And also each high voltage pin may have one of two mask options: (D) "Without pull-down MOS (PMOS open drain)", or (E) "With pull-down MOS". As pull-down MOS is connected to internal V_{disp} line, select R_{A1}/V_{disp} pin as V_{disp} with mask option when at least one high voltage pin is selected as "With pull-down MOS" option.

When any Input/Output common pin is used as input pin, it is necessary to select the mask option and output data as shown in Table 18.

• Output Circuit Operation of Standard Pins with "With pull-up MOS" Option

Fig. 15 shows the circuit used in the standard pins with "with pull-up MOS"option.

By execution of the output instruction, the write pulse will be generated, and be applied to the addressed port. This pulse will turn "ON" the PMOS (B) to make the transient time shorten to obtain "High level", if the output data is changed from "0" to "1". In this case, the "write pulse" allows the PMOS (B) to turn "ON" as long as 1/8 instruction cycle. While "write pulse" is "0", pull-up MOS (C) may retain the output in high level.

The $\overline{HLT}$ signal becomes "0" in stop mode, so that MOS (A) (B) (C) turn "OFF".

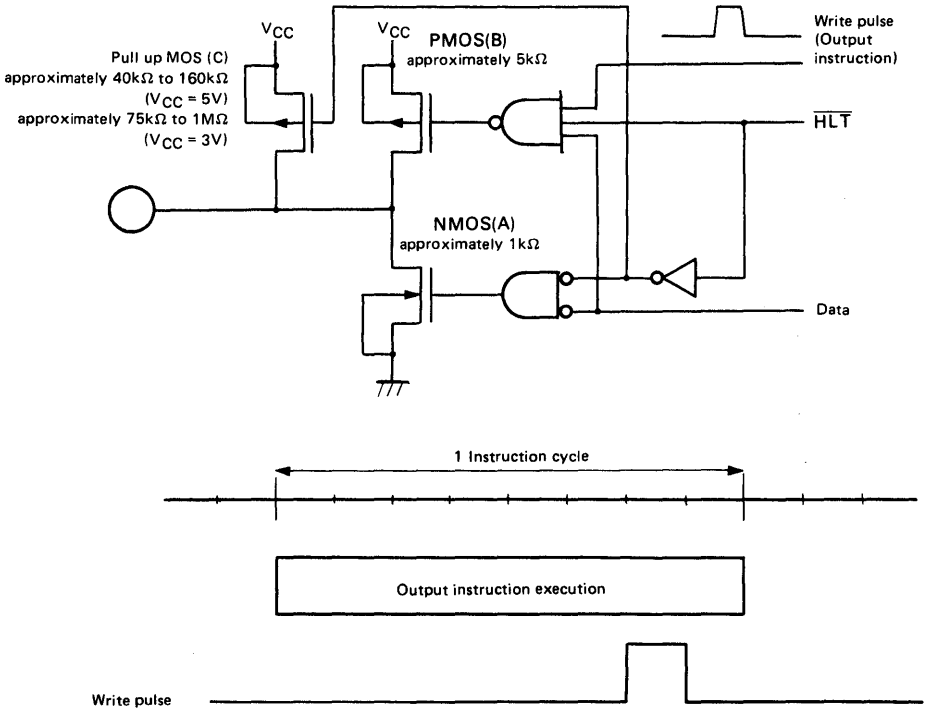
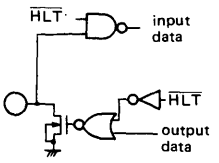
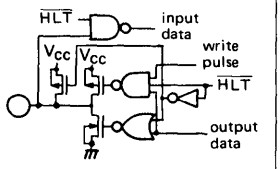
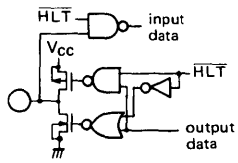
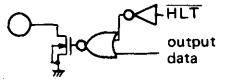
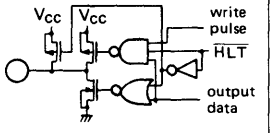
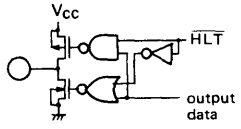
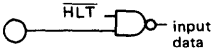
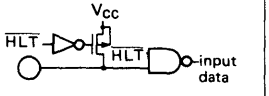
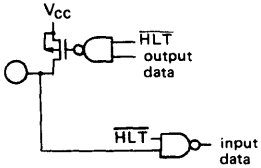
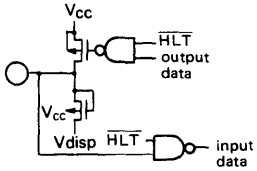
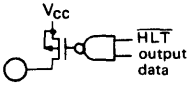
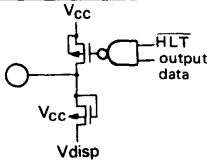
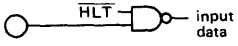
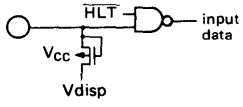


Fig. 15 Output Circuit Operation of Standard Pins with "with Pull-up MOS" Option

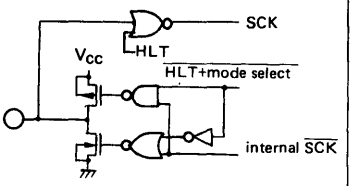
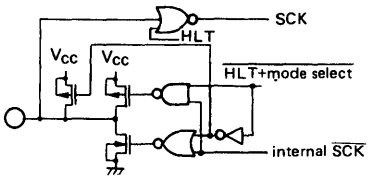
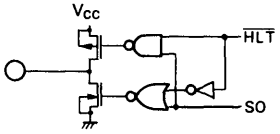
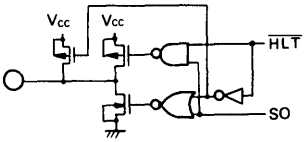
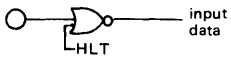
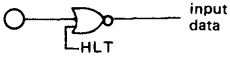
Table 17 I/O Pin Circuit Type

		Without pull-up MOS (NMOS open drain) (A)	With pull-up MOS (B)	CMOS (C)	Applied pins
Standard pins	I/O common pins				$D_0 \sim D_3$, $R_{30} \sim R_{33}$, $R_{40} \sim R_{43}$, $R_{50} \sim R_{53}$
	Output pins				$R_{60} \sim R_{63}$, $R_{70} \sim R_{73}$, $R_{80} \sim R_{83}$
	Input pins				$R_{90} \sim R_{93}$

		Without pull-down MOS (PMOS open drain) (D)	With pull-down MOS (E)	Applied pins
High voltage pins	I/O common pins			$D_4 \sim D_{15}$, $R_{10} \sim R_{13}$, $R_{20} \sim R_{23}$
	Output pins			$R_{00} \sim R_{03}$
	Input pins			R_{A0}, R_{A1}/V_{disp}

(Note) In the stop mode, $\overline{HLT}$ signal is "0" and I/O pins are in high impedance state.

(to be continued)

		Without pull-up MOS (NMOS open drain) or CMOS (A or C)	With pull-up MOS (B)	Applied pins
Standard pins	I/O common pins			$\overline{SCK}$
	Output pins			SO
	Input pins			$\overline{INT_0}$, $\overline{INT_1}$, SI

(Note) In the stop mode, $\overline{HLT}$ signal is "0", HLT signal is "1" and I/O pins are in high impedance state.

Table 18 Data Input from Input/Output Common Pins

I/O pin circuit type		Possibility of Input	Available pin condition for input
Standard pins	CMOS	No	–
	Without pull-up MOS (NMOS open drain)	Yes	"1"
	With pull-up MOS	Yes	"1"
High voltage pins	Without pull-down MOS (PMOS open drain)	Yes	"0"
	With pull-down MOS	Yes	"0"

• D-port

D-port is 1-bit I/O port, and it has 16 Input/Output common pins. It can be set/reset by the SED/RED and SEDD/REDD instructions, and can be tested by the TD and TDD instructions. Table 17 shows the classification of standard pins, high voltage pins and the Input/Output pins circuit types.

• R-port

R-port is 4-bit I/O port. It provides 20 input/output common pins, 16 output-only pins, and 6 input-only pins. Data input is processed using the LAR and LBR instructions and data output is processed using the LRA and LRB instructions. The MCU will not be affected by writing into the input-only and/or non-existing ports, invalid data will be read by reading from the output-only and/or non-existing ports.

The R_{32}, R_{33}, R_{40}, R_{41} and R_{42} pins are also used as the $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK}$, SI and SO pins respectively. Table 17 shows the classification of standard pins, high voltage pins and Input/Output pins circuit types.

■ RESET

The MCU is reset by setting RESET pin to "1". At power ON or recovering from stop mode, apply RESET input more than t_{RC} to obtain the necessary time for oscillator stabilization. In other cases, the MCU reset requires at least two instructions cycle time of RESET input.

Table 19 shows initialized items by MCU reset and each status after reset.

Table 19 Initial Value by MCU Reset

Items			Initial value by MCU reset	Contents
Program counter (PC)			$0000	Execute program from the top of ROM address.
Status (ST)			"1"	Enable to branch with conditional branch instructions.
Stack pointer (SP)			$3FF	Stack level is 0.
I/O pin output register	Standard pin	(A) Without pull-up MOS	"1"	Enable to input.
		(B) With pull-up MOS	"1"	Enable to input
		(C) CMOS	"1"	–
	High voltage pin	(D) Without pull-down MOS	"0"	Enable to input.
		(E) With pull-down MOS	"0"	Enable to input.
Interrupt flag	Interrupt Enable Flag (I/E)		"0"	Inhibit all interrupts.
	Interrupt Request Flag (IF)		"0"	No interrupt request.
	Interrupt Mask (IM)		"1"	Mask interrupt request.
Mode register	Port Mode Register (PMR)		"0000"	See Item "Port Mode Register".
	Serial Mode Register (SMR)		"0000"	See Item "Serial Mode Register".
	Timer Mode Register A (TMA)		"000"	See Item "Timer Mode Register A".
	Timer Mode Register B (TMB)		"0000"	See Item "Timer Mode Register B".
Timer/Counter, Serial interface	Prescaler		$000	–
	Timer/Counter A (TCA)		$00	–
	Timer/Event Counter B (TCB)		$00	–
	Timer Load Register (TLR)		$00	–
	Octal Counter		"000"	–

(Note) MCU reset affects to the rest of registers as follows:

Item		After recovering from STOP mode by MCU reset	After MCU reset except for the left condition
Carry	(CA)	The contents of the items before MCU reset are not retained. It is necessary to intialize them by software again.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software again.
Accumulator	(A)		
B Register	(B)		
W Register	(W)		
X/SPX Registers	(X/SPX)		
Y/SPY Registers	(Y/SPY)		
Serial Data Register	(SR)	Same as above	Same as above
RAM		The contents of RAM before MCU reset (just before STOP instruction) are retained.	Same as above

■ INTERNAL OSCILLATOR CIRCUIT

Fig. 16 gives internal oscillator circuit. The oscillator type can be selected from a crystal oscillator or a ceramic filter oscillator. In any cases, external clock operation is available.

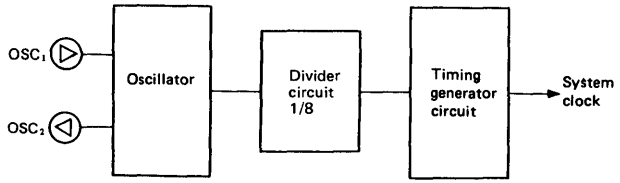
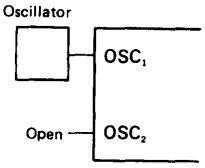
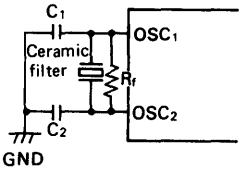
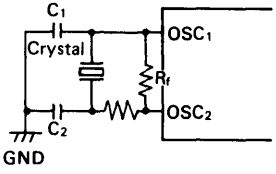
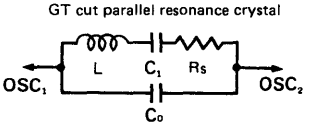


Fig. 16 Internal Oscillator Circuit

• Oscillator Circuit

Table 20 Examples of Oscillator Circuit

	Circuit configuration	Remarks
External clock operation		
Ceramic filter oscillator		Ceramic filter CSA2.000MK (Murata) Rf : 1MΩ ±2% C1 : 30pF ±20% C2 : 30pF ±20% • Wiring between these pins and elements should be as short as possible, and never cross the other wirings. (Refer to Fig. 17)
Crystal oscillator	 	Rf : 2MΩ±2% C1 : 10~22pF±20% C2 : 10~22pF±20% Crystal: GT cut parallel resonance crystal C0 : 7pF max. Rs : 100Ω max. f : 2.0 ~ 2.25MHz • Wiring between these pins should be as short as possible, and never cross the other wirings. (Refer to Fig. 17)

Note) Please consult with the engineers of crystal or ceramic filter maker to determine the value of R_f, C_1 and C_2.

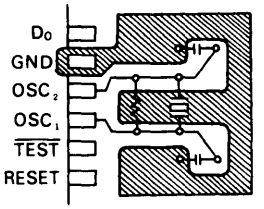


Fig. 17 Recommendable Layout of Crystal and Ceramic Filter

■ LOW POWER DISSIPATION MODE

The MCU provides two low power dissipation modes, that is, a Standby mode and a Stop mode. Table 21 shows the function of the low power dissipation mode, and Fig. 18 shows the diagram of the mode transition.

Table 21 Low Power Dissipation Mode Function

Low Power Dissipation Mode	Instruction	Condition							Recovering method
		Oscillator circuit	Instruction execution	Register, Flag	Interrupt function	RAM	Input/ Output pin	Timer/ Counter, Serial Interface	
Standby mode	SBY instruction	Active	Stop	Retained	Active	Retained	Retained*3)	Active	RESET Input, Interrupt request
Stop mode	STOP instruction	Stop	Stop	RESET*1)	Stop	Retained	High*2) impedance	Stop	RESET Input

*1) As the MCU recovers from STOP mode by RESET input, the contents of the flags and registers are initialized according to Table 19.
*2) A high voltage pin with a pull-down MOS option is pulled down to the V_{disp} power supply by the pull-down MOS. As the MOS is ON, a pull-down MOS current flows when a voltage difference between the pin and the V_{disp} voltage exists. This is the additional current to the current dissipation in Stop Mode (I_{stop}).
*3) As a I/O circuit is active, a I/O current possibly flows according the state of I/O pin. This is the additional current to the current dissipation in Standby Mode (I_{SBY1}, I_{SBY2}).

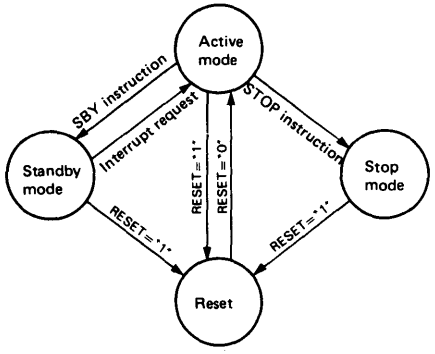


Fig. 18 MCU Operation Mode Transition

• Standby Mode

The SBY instruction puts the MCU into the Standby mode. In the Standby mode, the oscillator circuit is active and timer/counter and serial interface continue working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM and Input/Output pins retain the state they had just before going into the Standby mode.

The Standby mode is canceled by the MCU reset or interrupt request. When canceled by the interrupt request, the MCU becomes an active mode and executes the instruction next to the SBY instruction. At this time, if the Interrupt Enable Flag is "1", the interrupt is executed. If the Interrupt Enable Flag is "0", the interrupt request is held on and the normal instruction execution continues.

Fig. 19 shows the flowchart of the Standby Mode.

• Stop Mode

The STOP instruction brings the MCU into the Stop mode. In this mode the oscillator circuit and every function of the MCU stop.

The Stop mode is canceled by the MCU reset. At this time, as shown in Fig. 20, apply the RESET input for more than t_{RC} to get enough oscillator stabilization time. (Refer to the "AC CHARACTERISTICS".) After the Stop mode is canceled, RAM retains the state it had just before going into the Stop mode. The other hand, Accumulator, B Register, W Register, X/SPX Registers, Y/SPY Registers, Carry and Serial Data Register don't retain the contents.

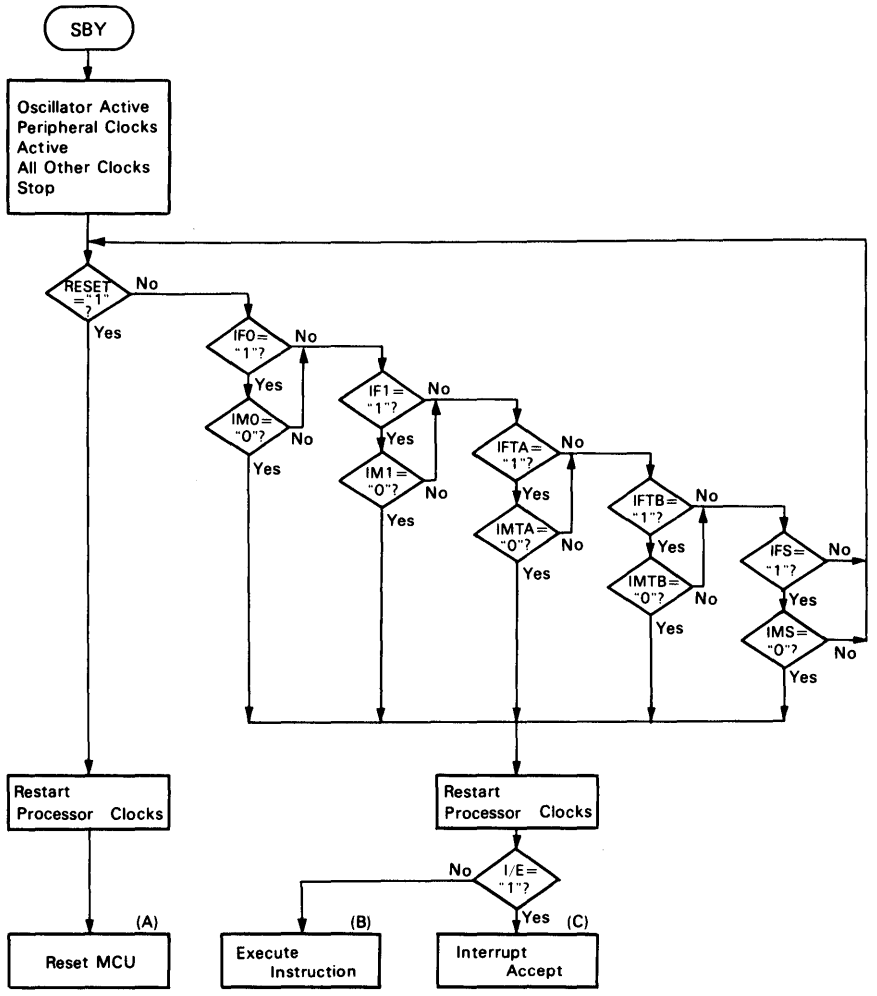


Fig. 19 MCU Operating Flowchart

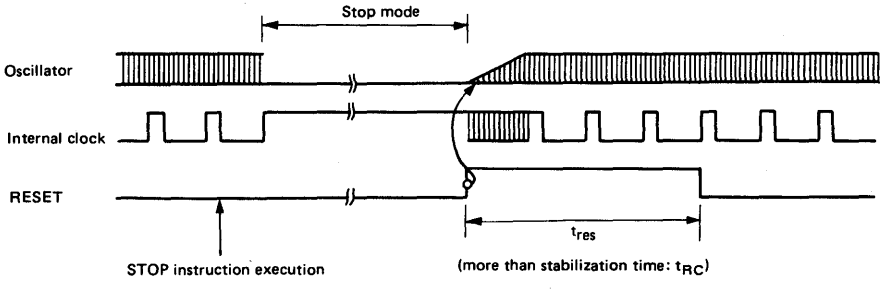


Fig. 20 Timing Chart of Recovering from Stop Mode

■ RAM ADDRESSING MODE

As shown in Fig. 21, the MCU provides three RAM addressing modes; Register Indirect Addressing, Direct Addressing and Memory Register Addressing.

• Register Indirect Addressing

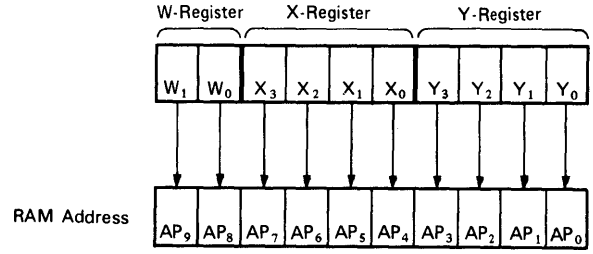
The combined 10-bit contents of W Register, X Register and Y Register is used as the RAM address in this mode.

• Direct Addressing

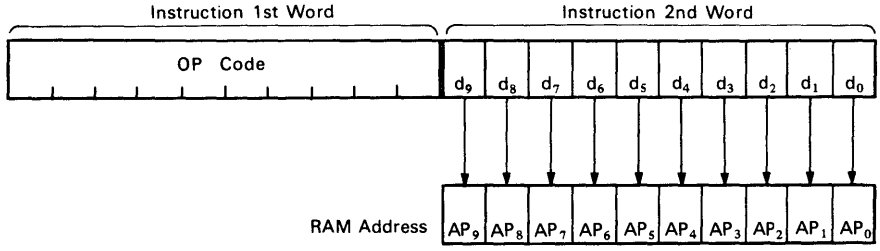
The direct addressing instruction consists of two words and the second word (10 bits) following Op-code (the first word) is used as the RAM address.

• Memory Register Addressing

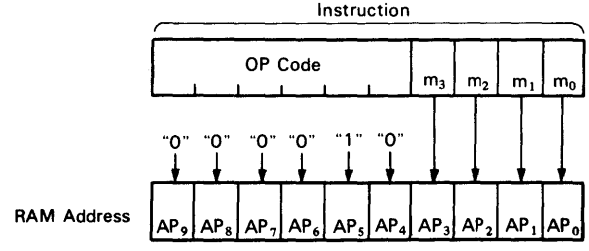
The Memory Register Addressing can access 16 digits (Memory Register: MR) from $020 to $02F by using the LAMR and XMRA instruction.



(a) Register Indirect Addressing



(b) Direct Addressing



(c) Memory Register Addressing

Fig. 21 RAM Addressing Mode

■ ROM ADDRESSING MODE AND P INSTRUCTION

The MCU has four kinds of ROM addressing modes as shown in Fig. 22.

• Direct Addressing Mode

The program can branch to any addresses in the ROM memory space by using JMPL, BRL or CALL instruction. These instruction replace 14-bit program counter (PC_{13} to PC_0) with 14-bit immediate data.

• Current Page Addressing Mode

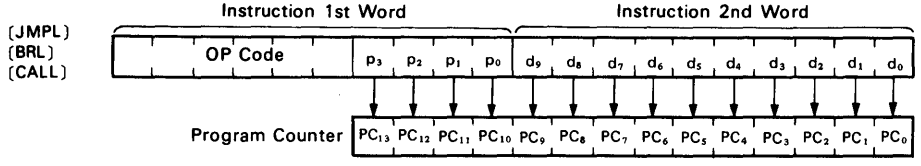
ROM memory space is divided into 256 words in each page starting from $0000. The program branches to the address in the same page using BR instruction. This instruction replace the low-order eight bits of program counter (PC_7 to PC_0) with 8-bit immediate data. The branch destination by BR instruction on the boundary between pages is in the next page. Refer to Fig. 24.

• Zero Page Addressing Mode

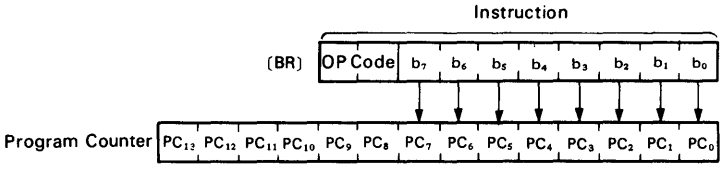
The program branches to the zero page subroutine area, which is located on the address from $0000 to $003F, using CAL instruction. When CAL instruction is executed, 6-bit immediate data is placed in low-order six bits of program counter (PC_5 to PC_0) and "0's" are placed in high-order eight bits (PC_{13} to PC_6).

• Table Data Addressing

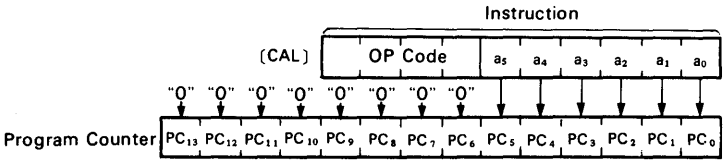
The program branches to the address determined by the contents of the 4-bit immediate data, accumulator and B register, using TBR instruction.



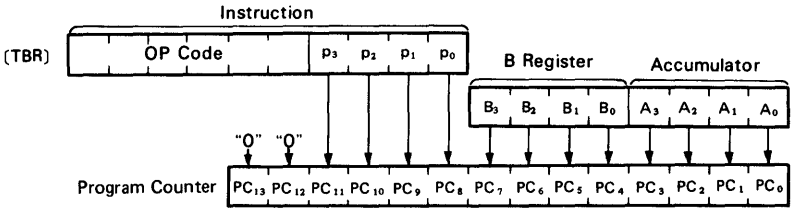
(a) Direct Addressing



(b) Current Page Addressing

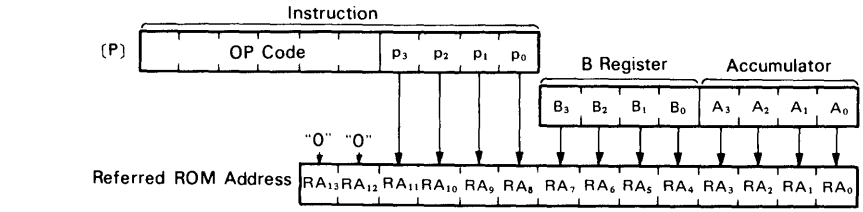


(c) Zero Page Addressing

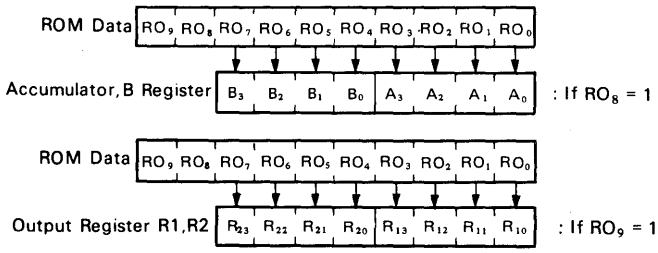


(d) Table Data Addressing

Fig. 22 ROM Addressing Mode



(a) Address Designation



(b) Pattern Output

Fig. 23 P Instruction

- **P Instruction**

The P instruction refers ROM data addressed by Table Data Addressing. ROM data addressed also determine its destination. When bit 8 in referred ROM data is "1", 8 bits of referred ROM data are written into the accumulator and B Register. When bit 9 is "1", 8 bits of referred ROM data are written into the R1 and R2 port output register. When both bit 8 and 9 are "1", ROM data are written into the accumulator and B Register and also to the R1 and R2 port output register at a same time.

The P instruction has no effect on the program counter.

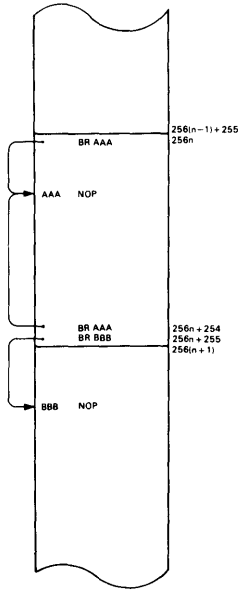


Fig. 24 The Branch Destination by BR Instruction on the Boundary between Pages

■ INSTRUCTION SET

The HMCS400 series provide 99 instructions. These instructions are classified into 10 groups as follows;

(1) Immediate Instruction
(2) Register-to-Register Instruction
(3) RAM Address Instruction
(4) RAM Register Instruction
(5) Arithmetic Instruction
(6) Compare Instruction
(7) RAM Bit Manipulation Instruction
(8) ROM Address Instruction
(9) Input/Output Instruction
(10) Control Instruction

Table 22. Immediate Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Load A from Immediate	LAI i	1 0 0 0 1 1 i_3 i_2 i_1 i_0	i⟶A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i_3 i_2 i_1 i_0	i⟶B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i⟶M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i_3 i_2 i_1 i_0	i→M,Y+1→Y	NZ	1/1

Table 23. Register-to-Register Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B→A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A→B		1/1
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y→A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX→A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY→A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m_3 m_2 m_1 m_0	MR(m)→A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m_3 m_2 m_1 m_0	MR(m)↔A		1/1

Table 24. RAM Address Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i_1 i_0	i⟶W		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i_3 i_2 i_1 i_0	i⟶X		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i_3 i_2 i_1 i_0	i⟶Y		1/1
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	A⟶X		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	A⟶Y		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	Y+1→Y	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	Y−1→Y	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	Y+A→Y	OVF	1/1
Subtract A from Y	SYY	0 0 1 1 0 1 0 1 0 0	Y−A→Y	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	X↔SPX		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	Y↔SPY		1/1
Exchange X and SPX,Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	X↔SPX,Y↔SPY		1/1

Table 25. RAM Register Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M→A, (X↔SPX, Y↔SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M→A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M→B, (X↔SPX, Y↔SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A→M, (X↔SPX, Y↔SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A→M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A→M,Y+1→Y(X↔SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A→M,Y−1→Y(X↔SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M↔A, (X↔SPX, Y↔SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M↔A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M↔B, (X↔SPX, Y↔SPY)		1/1

Note) (XY) and (x) have the meaning as follows:

(1) The instructions with (XY) have 4 mnemonics and 4 object codes for each. (example of LAM (XY) is given below.)

MNEMONIC	y	x	FUNCTION
LAM	0	0	
LAMX	0	1	X↔SPX
LAMY	1	0	Y↔SPY
LAMXY	1	1	X↔SPX, Y↔SPY

(2) The instructions with (x) have 2 mnemonics and 2 object codes for each. (example of LMAIY(X) is given below.)

MNEMONIC	x	FUNCTION
LMAIY	0	
LMAIYX	1	X↔SPX

Table 26. Arithmetic Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Add Immediate to A	AI i	1 0 1 0 0 0 i_3 i_2 i_1 i_0	A+i→A	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	B+1→B	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	B−1→B	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\bar{A}$+1→A		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\bar{B}$→B		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	1→CA		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	0→CA		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	M+A→A	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M+A→A	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	M+A+CA→A	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M+A+CA→A	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	M−A−$\overline{CA}$→A	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M−A−$\overline{CA}$→A	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	A∪B →A		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	A∩M→A	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A∩M→A	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	A∪M→A	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A∪M→A	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	A⊕M→A	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A⊕M→A	NZ	2/2

Table 27. Compare Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i_3 i_2 i_1 i_0	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i_3 i_2 i_1 i_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	ANEMD d	0 1 0 0 0 0 0 1 0 0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i_3 i_2 i_1 i_0	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i_3 i_2 i_1 i_0	i ≦ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i_3 i_2 i_1 i_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i ≦ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≦ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ≦ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≦ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i_3 i_2 i_1 i_0	A ≦ i	NB	1/1

Table 28. RAM Bit Manipulation Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n_1 n_0	1→M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n_1 n_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	1→M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n_1 n_0	0→M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n_1 n_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	0→M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n_1 n_0		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n_1 n_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		M(n)	2/2

Table 29. ROM Address Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Branch on Status 1	BR b	1 1 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p_3 p_2 p_1 p_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p_3 p_2 p_1 p_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a_5 a_4 a_3 a_2 a_1 a_0		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p_3 p_2 p_1 p_0 / d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p_3 p_2 p_1 p_0			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1→I/E		1/3

Table 30. Input/Output Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/CYCLE
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1→D(Y)		1/1
Set Discrete I/O Latch Direct	SEDD m	1 0 1 1 1 0 m_3 m_2 m_1 m_0	1→D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0→D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m_3 m_2 m_1 m_0	0→D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m_3 m_2 m_1 m_0		D(m)	1/1
Load A from R-Port Register	LAR m	1 0 0 1 0 1 m_3 m_2 m_1 m_0	R(m)→A		1/1
Load B from R-Port Register	LBR m	1 0 0 1 0 0 m_3 m_2 m_1 m_0	R(m)→B		1/1
Load R-Port Register from A	LRA m	1 0 1 1 0 1 m_3 m_2 m_1 m_0	A→R(m)		1/1
Load R-Port Register from B	LRB m	1 0 1 1 0 0 m_3 m_2 m_1 m_0	B→R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p_3 p_2 p_1 p_0			1/2

Table 31. Control Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD / CYCLE
No Operation	NOP	0000000000			1 / 1
Start Serial	STS	0101001000			1 / 1
Stand-by Mode	SBY	0101001100			1 / 1
Stop Mode	STOP	0101001101			1 / 1

Table 32. Op-Code Map

R9 (H) \ R8 (L)	0	1
0	NOP, XSPX, XSPY, XSP XY, AN EM, AM, ORM	ANEMD, AMD, ORMD
1	RTN, RTNI, ALEM, AMC, EORM	ALEMD, AMCD, EORMD
2	INEM i(4)	INEMD i(4)
3	ILEM i(4)	ILEMD i(4)
4	LBM(XY), BNEM, LAB, IB	COMB, OR, STS, SBY, STOP
5	LMAIY(X), AYY, LASPY, IY	JMPL p(4)
6	NEGA, RED, LASPX, TC	CALL p(4)
7	YNEI i(4)	BRL p(4)
8	XMA(XY), SEM n(2), REM n(2), TM n(2)	XMAD, SEMD n(2), REMD n(2), TMD n(2)
9	LAM(XY), LMA(XY), SMC, ANM	LAMD, LMAD, SMCD, ANMD
A	ROTR, ROTL, DAA, DAS, LAY	LMID i(4)
B	TBR p(4)	P p(4)
C	XMB(XY), BLEM, LBA, DB	CAL a(6)
D	LMADY(X), SYY, LYA, DY	
E	TD, SED, LXA, REC, SEC	
F	LWI i(2)	
0	LBI i(4)	BR b(8)
1	LYI i(4)	
2	LXI i(4)	
3	LAI i(4)	
4	LBR m(4)	
5	LAR m(4)	
6	REDD m(4)	
7	LAMR m(4)	
8	AI i(4)	
9	LMIIY i(4)	
A	TDD m(4)	
B	ALEI i(4)	
C	LRB m(4)	
D	LRA m(4)	
E	SEDD m(4)	
F	XMRA m(4)	

... 1-word/2-cycle Instruction

... 1-word/3-cycle Instruction

... RAM Direct Address Instruction (2-word/2-cycle)

... 2-word/2-cycle Instruction

■ MASK OPTION LIST

- Family Name ■ HMCS404CL
- Package □ DP-64S □ FP-64
- I/O Circuit Type A; Without Pull-up MOS (NMOS Open Drain)
  B; With Pull-up MOS
  C; CMOS
  D; Without Pull-down MOS (PMOS Open Drain)
  E; With Pull-down MOS

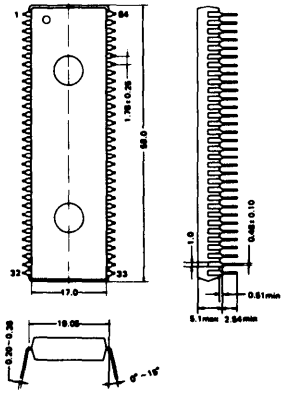
Date of Order	
Customer	
Dept.	
Name	
ROM Code Name	
LSI Type Number (Hitachi's entry)	

PIN			INPUT/OUTPUT	I/O OPTION A	B	C	D	E
D_0		Standard Pins	Input/Output					
D_1			Input/Output					
D_2			Input/Output					
D_3			Input/Output					
D_4		High Voltage Pins	Input/Output					
D_5			Input/Output					
D_6			Input/Output					
D_7			Input/Output					
D_8			Input/Output					
D_9			Input/Output					
D_{10}			Input/Output					
D_{11}			Input/Output					
D_{12}			Input/Output					
D_{13}			Input/Output					
D_{14}			Input/Output					
D_{15}			Input/Output					
R0	R_{00}	High Voltage Pins	Output					
	R_{01}		Output					
	R_{02}		Output					
	R_{03}		Output					
R1	R_{10}		Input/Output					
	R_{11}		Input/Output					
	R_{12}		Input/Output					
	R_{13}		Input/Output					
R2	R_{20}		Input/Output					
	R_{21}		Input/Output					
	R_{22}		Input/Output					
	R_{23}		Input/Output					
R3	R_{30}	Standard Pins	Input/Output					
	R_{31}		Input/Output					
	R_{32}		Input/Output					
	R_{33}		Input/Output					
R4	R_{40}		Input/Output					
	R_{41}		Input/Output					
	R_{42}		Input/Output					
	R_{43}		Input/Output					
R5	R_{50}		Input/Output					
	R_{51}		Input/Output					
	R_{52}		Input/Output					
	R_{53}		Input/Output					
R6	R_{60}		Output					
	R_{61}		Output					
	R_{62}		Output					
	R_{63}		Output					
R7	R_{70}		Output					
	R_{71}		Output					
	R_{72}		Output					
	R_{73}		Output					
R8	R_{80}		Output					
	R_{81}		Output					
	R_{82}		Output					
	R_{83}		Output					
R9	R_{90}		Input					
	R_{91}		Input					
	R_{92}		Input					
	R_{93}		Input					
RA	R_{A0}	High Voltage Pins	Input					
	R_{A1}		Input	Please Mark on R_{A1}/V_{disp}				

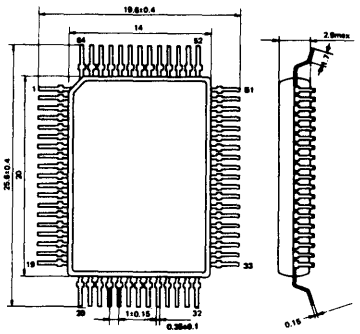
- R_{A1}/V_{disp} (R_{A1}) □ R_{A1}: Without Pull-down MOS (D) □ V_{disp} (VDISP)
- Oscillator (OSC) ■ Crystal or Ceramic Filter Oscillator (XTAL)
- Divider (DIV) ■ Divide-by-8 (D-8)
- ROM Code Media □ EPROM: Emulator Type □ EPROM: EPROM On-Package Microcomputer Type

Note 1) I/O Options masked by ▨ are not available.
Note 2) R_{A1}/V_{disp} has to be selected as V_{disp} pin exept the case that all High Voltage Pins are option D.

■ **PACKAGE DIMENSIONS (Unit: mm)**



(DP-64S)



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