SPARClite

MB86860 Series Data Sheet

Rev.1.2 July 27, 1999

Fujitsu

This material is preliminary and is subject to change without notice.

860 Series 32-bit RISC Embedded Processor

1. Features

1.1. CPU Core Part

- Conforms to SPARC V8
- Internal operating frequency maximum 200MHz
- 2-issue super-scalar architecture
- 16KB 4-way instruction cache
- 16KB 4-way data cache
- Power Down Mode
- Bi-endian support

1.2. Debug Support Functions

- Break Function (Instruction Address / External pins / Software / Single Step)
- 16-depth Address Trace Buffer
- Single Step Operation

1.3. Data Buffer Module

- 4 Column Instruction Buffer
- 4 Column X 2 Read Buffer
- 16 Column Write Buffer

1.4. SDRAM Interface

- 64 bit Data Bus Widths
- Maximum 100MHz Operation
- Auto / Self-Refresh Support
- Parity Function Support

1.5. SPARClite Bus Interface

- 8 / 16 / 32 / 64-bit Data Bus
- Burst Mode Support
- Parity Function Support

1.6. Bus-bridge DMA

- DMA 2 channels. Simultaneous operation 1 channel

1.7. Power Supply

- Internal: 2.5V
- I/O Pins: 3.3V

1.8. MB86860 Block Diagram

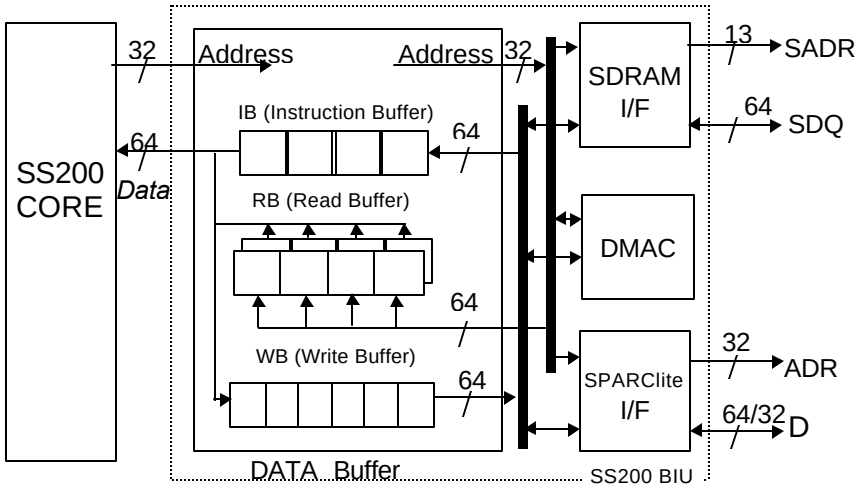


Figure 1.1 SS200 BIU Block Diagram

1.9 MB86860 Pin Overview

1.9.1 Package

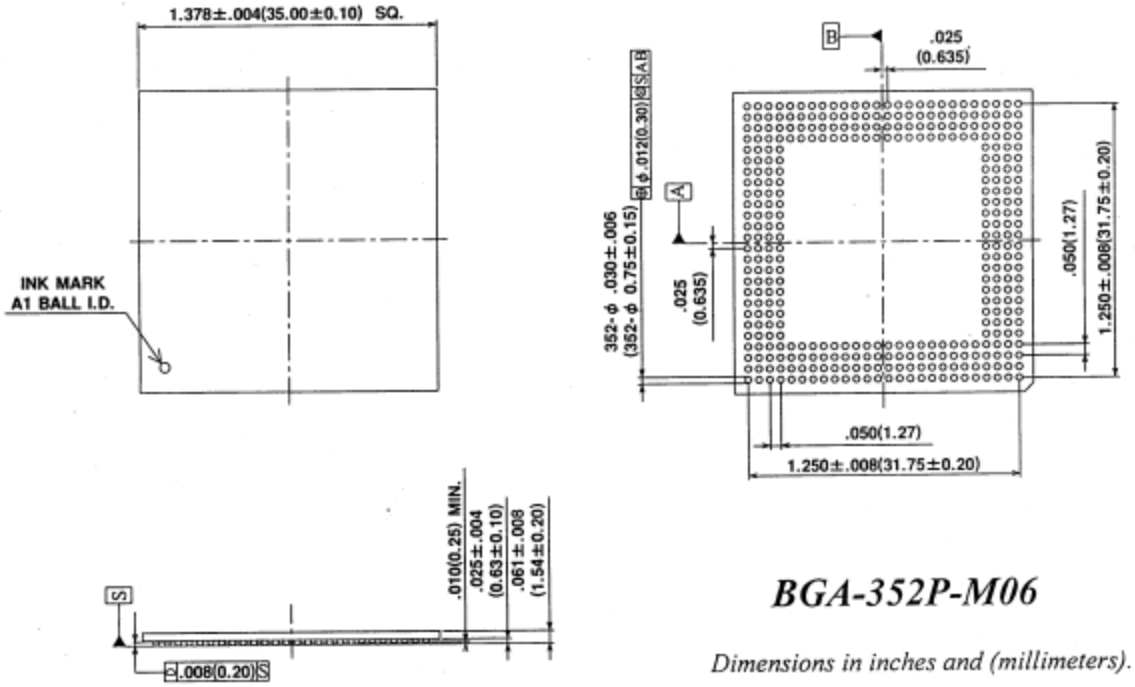


Figure 1.2 Package Dimension

1.9.2 MB86860 signal list

Table 1.1 Pin Assignment

PKG Pin No.			Left		PKG Pin No.			Bottom		PKG Pin No.			Right		PKG Pin No.			Top	
(FJ)	(JEDEC)		Signal	Att.	(FJ)	(JEDEC)		Signal	Att.	(FJ)	(JEDEC)		Signal	Att.	(FJ)	(JEDEC)		Signal	Att.
1	A	1	VSS	VSS	76	A	26	VSS	VSS	51	AF	26	VSS	VSS	26	AF	1	VSSP	VSS
277	D	4	VDDI	VDDI	334	D	23	VDDI	VDDI	315	AC	23	VDDI	VDDI	296	AC	4	VDDI	VDDI
276	C	4	D<23>	I/O	255	D	24	SDQ<15>	I/O	234	AD	23	SDQ<45>	I/O	213	AC	3	TRST#	I
352	D	5	VDDE	VDDE	333	E	23	VDDE	VDDE	314	AC	22	VDDE	VDDE	295	AB	4	TD1	I
99	A	3	D<24>	I/O	74	C	26	SDQ<16>	I/O	49	AF	24	SDQ<46>	I/O	24	AD	1	TMS	I
191	B	4	D<25>	I/O	168	D	25	SDQ<17>	I/O	145	AE	23	SDQ<47>	I/O	122	AC	2	TD0	O
275	C	5	D<26>	I/O	254	E	24	SDQ<18>	I/O	233	AD	22	SDQ<48>	I/O	212	AB	3	TCLK	I
351	D	8	DP4	I/O	332	F	23	ADP5	I/O	313	AC	21	SDP1	I/O	294	AA	4	VDDP	VDDP
101	B	2	VDDI	VDDI	170	B	25	VDDI	VDDI	147	AE	25	VDDI	VDDI	124	AE	2	VDDI	VDDI
98	A	4	D<27>	I/O	73	D	26	SDQ<19>	I/O	48	AF	23	SDQ<49>	I/O	23	AC	1	TEST1	I
190	B	5	D<28>	I/O	167	E	25	SDQ<20>	I/O	144	AE	22	SDQ<50>	I/O	121	AB	2	TEST2	I
274	C	6	D<29>	I/O	253	F	24	SDQ<21>	I/O	232	AD	21	SDQ<51>	I/O	211	AA	3	VDDP	VDDP
350	D	7	DP3	I/O	331	G	23	SDP4	I/O	312	AC	20	SDP0	I/O	293	Y	4	VSSP	VSSP
192	B	3	VSS	VSS	169	C	25	VSS	VSS	146	AE	24	VSS	VSS	123	AD	2	VSSP	VSS
97	A	5	D<30>	I/O	72	E	26	SDQ<22>	I/O	47	AF	22	SDQ<52>	I/O	22	AB	1	CLKSEL1	I
348	D	9	VDDI	VDDI	329	J	23	VDDI	VDDI	310	AC	18	VDDI	VDDI	291	V	4	VDDI	VDDI
189	B	6	D<31>	I/O	166	F	25	SDQ<23>	I/O	143	AE	21	SDQ<53>	I/O	120	AA	2	CLKIN	I
273	C	7	D<32>	I/O	252	G	24	SDQ<24>	I/O	231	AD	20	SDQ<54>	I/O	210	Y	3	VSSP	VSSP
349	D	8	VDDE	VDDE	330	H	23	VDDE	VDDE	311	AC	19	VDDE	VDDE	292	W	4	VDDE	VDDE
96	A	6	D<33>	I/O	71	F	26	SDQ<25>	I/O	46	AF	21	SDQ<55>	I/O	21	AA	1	CLKSEL0	I
188	B	7	D<34>	I/O	165	G	25	SDQ<26>	I/O	142	AE	20	SDQ<56>	I/O	119	Y	2	RESET#	I
100	A	2	VSS	VSS	75	B	26	VSS	VSS	50	AF	25	VSS	VSS	25	AE	1	VSSP	VSS
272	C	8	D<35>	I/O	251	H	24	SDQ<27>	I/O	230	AD	19	SDQ<57>	I/O	209	W	3	BCLK	I
95	A	7	D<36>	I/O	70	G	26	SDQ<28>	I/O	45	AF	20	SDQ<58>	I/O	20	Y	1	PLLCEN	I
187	B	8	D<37>	I/O	164	H	25	SDQ<29>	I/O	141	AE	19	SDQ<59>	I/O	118	W	2	STOP#	I
271	C	9	D<38>	I/O	250	J	24	SDQ<30>	I/O	229	AD	18	SDQ<60>	I/O	208	V	3	BEN#	I
347	D	10	NC	NC	328	K	23	NC ***1**	NC	309	AC	17	NC	NC	290	U	4	NC	NC
94	A	8	D<39>	I/O	69	H	26	SDQ<31>	I/O	44	AF	19	I/O	I/O	19	W	1	ILR<0>	I
186	B	9	D<40>	I/O	163	J	25	SDQM0	O	140	AE	18	I/O	I/O	117	V	2	IRL<1>	I
270	C	10	D<41>	I/O	249	K	24	SDQM1	O	228	AD	17	I/O	I/O	207	U	3	IRL<2>	I
93	A	9	D<42>	I/O	68	J	26	SDQM2	O	43	AF	18	O	O	18	V	1	IRL<3>	I
346	D	11	DP2	I/O	327	L	23	FLOAT#	I	308	AC	16	O	O	289	T	4	DBREAK#	I
185	B	10	D<43>	I/O	162	K	25	SDQM3	O	139	AE	17	O	O	116	U	2	BRKEN#	I
269	C	11	D<44>	I/O	248	L	24	SDQM4	O	227	AD	16	O	O	206	T	3	BRKG0	O
92	A	10	D<45>	I/O	67	K	26	SDQM5	O	42	AF	17	O	O	17	U	1	BREQ#	I
343	D	14	VDDI	VDDI	324	P	23	VDDI	VDDI	305	AC	13	VDDI	VDDI	286	N	4	VDDI	VDDI
184	B	11	D<46>	I/O	161	L	25	SDQM6	O	138	AE	16	ADR<7>	O	115	T	2	BGRNT#	O
345	D	12	VDDE	VDDE	326	M	23	VDDE	VDDE	307	AC	15	VDDE	VDDE	288	R	4	VDDE	VDDE
91	A	11	D<47>	I/O	66	L	26	SDQM7	O	41	AF	16	ADR<8>	O	16	T	1	PBREQ#	O
268	C	12	D<48>	I/O	247	M	24	SADR<0>	O	226	AD	15	ADR<9>	O	205	R	3	BE0#	O
183	B	12	D<49>	I/O	160	M	25	SADR<1>	O	137	AE	15	ADR<10>	O	114	R	2	BE1#	O
89	A	13	VSS	VSS	64	N	26	VSS	VSS	39	AF	14	VSS	VSS	14	P	1	VSS	VSS
90	A	12	D<50>	I/O	65	M	26	SADR<2>	O	40	AF	15	ADR<11>	O	15	R	1	BE2#	O
344	D	13	DP1	I/O	325	N	23	SADR<3>	O	306	AC	14	ADR<12>	O	287	P	4	BE3#	O

VDDI: VDD for Internal Logic --- 2.5V
VDDE: VDD for I/O Pad ---------- 3.3V
VDDP: VDD for built-in PLL ----- 2.5V

Table 1.2 Pin Assignment (continued)

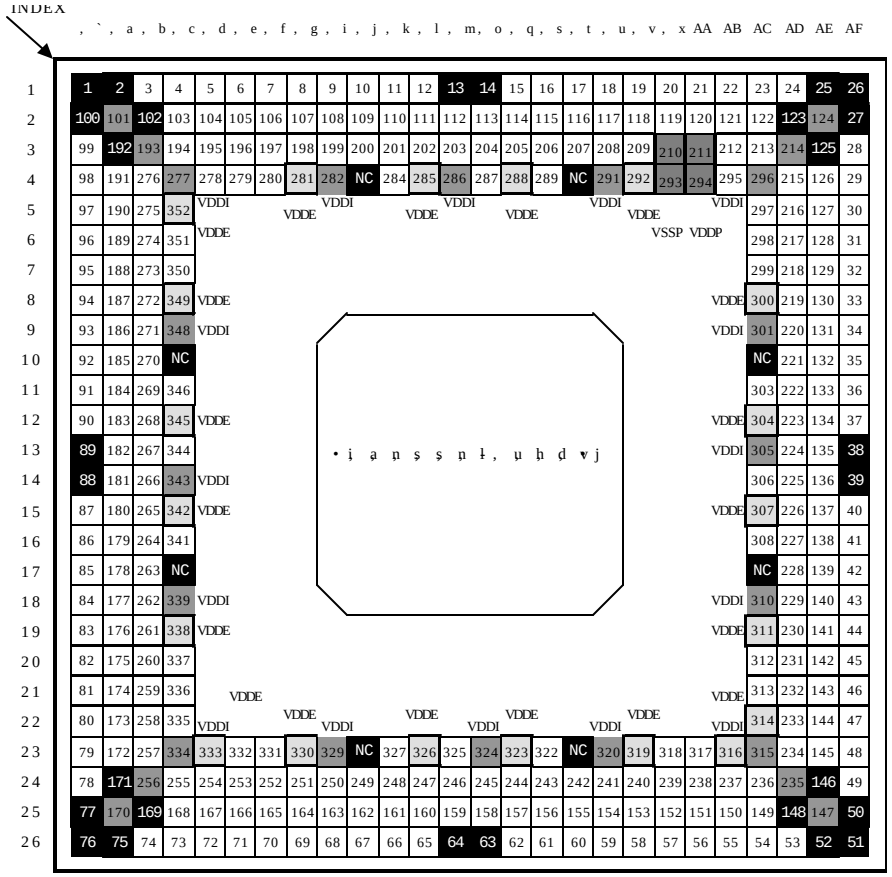
PKG Pin No.		Left		PKG Pin No.		Bottom		PKG Pin No.		Right		PKG Pin No.		Top	
(FJ)	(JEDEC)	Signal	Att.	(FJ)	(JEDEC)	Signal	Att.	(FJ)	(JEDEC)	Signal	Att.	(FJ)	(JEDEC)	Signal	Att.
267	C 13	D<51>	I/O	246	N 24	SADR<4>	O	225	AD 14	ADR<13>	O	204	P 3	BE4#	O
182	B 13	D<52>	I/O	159	N 25	SADR<5>	O	136	AE 14	ADR<14>	O	113	P 2	BE5#	O
181	B 14	S<53>	I/O	158	P 25	SADR<6>	O	135	AE 13	ADR<15>	O	112	N 2	BE6#	O
266	C 14	D<54>	I/O	245	P 24	SADR<7>	O	224	AD 13	ADR<16>	O	203	N 3	BE7#	O
87	A 15	D<55>	I/O	62	R 26	SADR<8>	O	37	AF 12	ADR<17>	O	12	M 1	WKUP#	I
88	A 14	VSS	VSS	63	P 26	VSS	VSS	38	AF 13	VSS	VSS	13	N 1	VSS	VSS
180	B 15	D<56>	I/O	157	R 25	SADR<9>	O	134	AE 12	ADR<18>	O	111	M 2	PDWN#	O
265	C 15	D<57>	I/O	244.	R 24	SADR<10>	O	223	AE 11	ADR<19>	O	202	M 3	AS#	O
86	A 16	D<58>	I/O	61	T 26	SADR<11>	O	36	AF 11	ADR<20>	O	11	L 1	RD#	O
342	D 15	VDDE	VDDE	323	R 23	VDDE	VDDE	304	AC 12	VDDE	VDDE	285	M 4	VDDE	VDDE
179	B 16	D<59>	I/O	156	T 25	SADR<12>	O	133	AE 11	ADR<21>	O	110	L 2	RDWR#	O
85	A 17	D<60>	I/O	60	U 26	SRAS#	O	35	AF 10	ADR<22>	O	10	K 1	LOCK#	O
264	C 16	D<61>	I/O	243	T 24	SCKE#	O	222	AD 11	ADR<23>	O	201	L 3	D<0>	I/O
178	B 17	D<62>	I/O	155	U 25	SCAS#	O	132	AE 10	ADR<24>	O	109	K 2	D<1>	I/O
341	D 16	DP0	I/O	322	T 23	SCLK	O	303	AC 11	ADR>25>	O	284	L 4	D<2>	I/O
84	A 18	D<63>	I/O	59	V 26	SWE#	O	34	AF 9	ADR<26>	O	9	J 1	D<3>	I/O
263	C 17	MEXC#	I	242	U 24	SCS0#	O	221	AD 10	ADR<27>	O	200	K 3	D<4>	I/O
339	D 18	VDDI	VDDI	320	V 23	VDDI	VDDI	301	AC 9	VDDI	VDDI	282	J 4	VDDI	VDDI
177	B 18	READY#	I	154	V 25	SCS1#	O	131	AE 9	SDR<28>	O	108	J 2	D<5>	I/O
83	A 19	RDYOUT#	O	58	W 26	SCS2#	O	33	AF 8	ADR<29>	O	8	H 1	D<6>	I/O
340	D 17	NC	NC	321	U 23	NC	NC	302	AC 10	NC ***2**	NC	283	K 4	NC	NC
262	C 19	BMODE32#	I	241	V 24	SCS3#	O	220	AD 9	ADR<30>	O	199	J 3	D<7>	I/O
176	B 19	BMODE16#	I	153	W 25	SBA<0>	O	130	AE 8	ADR<31>	O	107	H 2	D<8>	I/O
82	A 20	SDQ<0>	I/O	57	Y 26	SBA<1>	O	32	AF 7	DTYP<1>	O	7	G 1	D<9>	I/O
261	C 19	SDQ<1>	I/O	240	W 24	SDQ<32>	I/O	219	AD 8	DTYP<0>	O	198	H 3	D<10>	I/O
171	B 24	VSS	VSS	148	AD 25	VSS	VSS	27	AF 2	VSS	VSS	2	B 1	VSS	VSS
175	B 20	SDQ<2>	I/O	152	Y 25	SDQ<33>	I/O	129	AE 7	BMACK#	I	106	G 2	D<11>	I/O
81	A 21	SDQ<3>	I/O	56	AA 26	SDQ<34>	I/O	31	AF 6	BMREQ#	O	6	F 1	D<12>	I/O
338	D 19	VDDE	VDDE	319	W 23	VDDE	VDDE	300	AC 8	VDDE	VDDE	281	H 4	VDDE	VDDE
260	C 20	SDQ<4>	I/O	239	Y 24	SDQ<35>	I/O	218	AD 7	ERROR#	O	197	G 3	D<13>	I/O
174	B 21	ADQ<5>	I/O	151	AA 25	SDQ<36>	I/O	128	AE 6	EOP#	O	105	F 2	D<14>	I/O
80	A 22	SDQ<6>	I/O	55	AB 26	SDQ<37>	I/O	30	AF 5	CS0#	O	5	E 1	D<15>	I/O
337	D 20	SDQ<7>	I/O	318	Y 23	SDP3	I/O	299	AC 7	CS1#	O	280	G 4	DP7	I/O
259	C 21	SDQ<8>	I/O	238	AA 24	SDQ<38>	I/O	217	AD 6	CS2#	O	196	F 3	D<16>	I/O
173	B 22	SDQ<9>	I/O	150	AB 25	SDQ<39>	I/O	127	AE 5	CS3#	O	104	E 2	D<17>	I/O
79	A 23	SDQ<10>	I/O	54	AC 26	SDQ<40>	I/O	29	AF 4	CS4#	O	4	D 1	D<18>	I/O
256	C 24	VDDI	VDDI	235	AD 24	VDDI	VDDI	214	AD 3	VDDI	VDDI	193	C 3	VDDI	VDDI
336	D 21	SDP7	I/O	317	AA 23	SDP2	I/O	298	AC 6	CS5#	O	279	F 4	DP6	I/O
77	A 25	VSS	VSS	52	AE 26	VSS	VSS	125	AE 3	VSS	VSS	102	C 2	VSS	VSS
258	C 22	SDQ<11>	I/O	237	AB 24	SDQ<41>	I/O	216	AD 5	ASI<0>	O	195	E 3	D<19>\	I/O
172	B 23	SDQ<12>	I/O	149	AC 25	SDQ<42>	I/O	126	AE 4	ASI<1>	O	103	D 2	D<20>	I/O
78	A 24	SDQ<13>	I/O	53	AD 26	SDQ<43>	I/O	28	AF 3	ASI<2>	O	3	C 1	D<21>	I/O
335	D 22	SDP6	I/O	316	.AB 23	VDDE	VDDE	297	AC 5	ASI<3>	O	278	E 4	DP5	IO
257	C 23	SDQ<14>	I/O	236	AC 24	SDQ<44>	I/O	215	AD 4	NCTEST#	I	194	D 3	D<22>	I/O

VDDI: VDD for Internal Logic ---- 2.5V
VDDE: VDD for I/O Pad ---------- 3.3V
VDDP: VDD for built-in PLL ------ 2.5V

Note *1) Pin 328 (NC) is reserved OUTPUT(SDC) MB86862.
Note *2) Pin 302 (NC) is reserved INPUT (BLEN8#) for MB86861 and MB86862.
Note *3) Pin 215 (NCTEST#) is changed to SDSEL# (input) for MB86861 and MB86862.

1.9.3 Package Pin Assignment (Power, GND)

***1) Pin 302(NC) is reserved input for MB86861 and MB86862**
***2) Pin 328(NC) is reserved output for MB86862.**



: SIGNALS (268)

:	VDDI(24) VDD for interna	101, 124, 147, 170, 193, 214, 235, 256, 277, 282, 286, 291, 296, 301, 305, 310, 315, 320, 324, 329, 334, 339, 343, 348
:	VDDE(20) VDD for I/O pac	281, 285, 288, 292, 300, 304, 307, 311, 319, 323, 326, 330, 338, 342, 345, 349
:	VSS (28)	1, 2, 13, 14, 25, 26, 27, 38, 39, 50, 51, 52, 63, 64, 75, 76, 77, 88, 89, 100, 102, 123, 125, 146, 148, 169, 171, 192
	NC (8)	283,290 302(*1) ,309 321,328(*2) 340,347
	VDDP	211, 294
	VSSP	210, 293

Figure 1.3 Package Pin Assignments

2. Programmers Model

2.1. ASI Assignments

MB86860 ASI assignments are as shown below.

Table 2.1

ASI	Function
0h	reserved
1h	special regs.
2h	reserved
3h	reserved for TLB probe
4h	internal regs. / user I/O ***1**
5h-6h	reserved
7h	user I/O regs.
8h	user inst.
9h	supervisor inst.
ah	user data
bh	supervisor data
ch	I-Cache TAG diagnostic
dh	I-Cache Set Diagnostic
eh-fh	reserved
10h-14h	reserved (I-Cache/D-Cache line flush) ***2**
15h-17h	reserved
18h-1bh	I-Cache line flush
1ch	D-Cache TAG diagnostic
1dh	D-Cache Set diagnostic
1eh-30h	reserve
31h	Flush entire I-Cache/D-cache
32h-ffh	reserved

Note *1) 0x00000000~0x7FFFFFFF of ASI=4 is a USER area, and since 0x80000000~0xFFFFFFFF is a reserved area it cannot be used.

Note *2) I-cache/D-cache line flush function is not implemented.

2.2. Register Overview

The following is an overview of the registers located in the SS200 memory spaces.

Table 2.2 Register Overview

ASI	Address	Register
0x01	0x00002004	Sleep mode register
0x01	0x0000FF00	Instruction Address Descriptor Register1 (ADR1)
0x01	0x0000FF04	Instruction Address Descriptor Register2 (ADR2)
0x01	0x0000FF18	Debug Control Register (DCR)
0x01	0x0000FF1C	Debug Status Register (DSR)
0x01	0x0000FF40 | 0x0000FF7C	PC Trace Buffer (TB)
0x04	0x80000000	Buffer Control Register (BCR)
0x04	0x80000100	Address Range Specifier Register0 (ARSR0)
0x04	0x80000108	Address Range Specifier Register1 (ARSR1)
0x04	0x80000110	Address Range Specifier Register2 (ARSR2)
0x04	0x80000118	Address Range Specifier Register3 (ARSR3)
0x04	0x80000120	Address Range Specifier Register4 (ARSR4)
0x04	0x80000128	Address Range Specifier Register5 (ARSR5)
0x04	0x80000130	SDRAM Address Range Specifier Register0 (SDARS0)
0x04	0x80000138	SDRAM Address Range Specifier Register1 (SDARS1)
0x04	0x80000200	Address Mask Register0 (AMR0)
0x04	0x80000208	Address Mask Register1 (AMR1)
0x04	0x80000210	Address Mask Register2 (AMR2)
0x04	0x80000218	Address Mask Register3 (AMR3)
0x04	0x80000220	Address Mask Register4 (AMR4)
0x04	0x80000228	Address Mask Register5 (AMR5)
0x04	0x80000230	SDRAM Address Mask Register0 (SDAM0)
0x04	0x80000238	SDRAM Address Mask Register1 (SDAM1)
0x04	0x80000400	Wait State Specifier Register0 (WSSR0)
0x04	0x80000408	Wait State Specifier Register1 (WSSR1)
0x04	0x80000410	Wait State Specifier Register2 (WSSR2)
0x04	0x80000418	Wait State Specifier Register3 (WSSR3)
0x04	0x80000420	Wait State Specifier Register4 (WSSR4)
0x04	0x80000428	Wait State Specifier Register5 (WSSR5)
0x04	0x80000430	MEXC Parity Error Flag Register (MXPEF)
0x04	0x80000438	MEXC Parity Error Control Register (MXPECR)
0x04	0x80000440	Idle Cycle Control Register (IDCCR)
0x04	0x80000800	SDRAM Configuration Register (SDCFG)
0x04	0x80000808	Auto Refresh Timer Register (ART)
0x04	0x80000810	SDRAM Status Register (SSR)
0x04	0x80000C00	DMA Control Register0 (DMCR0)
0x04	0x80000C08	DMA Source Address Register0 (DMSAR0)
0x04	0x80000C10	DMA Destination Address Register0 (DMDAR0)
0x04	0x80000C18	DMA Word Length Register0 (DMWL0)
0x04	0x80000C20	DMA Control Register1 (DMCR1)
0x04	0x80000C28	DMA Source Address Register1 (DMSAR1)
0x04	0x80000C30	DMA Destination Address Register1 (DMDAR1)
0x04	0x80000C38	DMA Word Length Register1 (DMWL1)
00x04	0x80000FF0	ID Register (IDR)

Note: Those registers listed above should be accessed as word data. In access other than word size (32 bits), register settings and data are not guaranteed.

Table 2.2 Register Overview (continued)

ASI	Address	Register	Symbol	Class
0x0c	0x00000000 | 0x00000FE0	I-Cache Tag Diagnostics set 0	I-CTAG0	I-Cache
0x0c	0x00001000 | 0x00001FE0	I-Cache Tag Diagnostics set 1	I-CTAG1	I-Cache
0x0c	0x00001000 | 0x00001FE0	I-Cache Tag Diagnostics set 2	I-CTAG2	I-Cache
0x0c	0x00001000 | 0x00001FE0	I-Cache Tag Diagnostics set 3	I-CTAG3	I-Cache
0x0d	0x00001000 | 0x00001FF8	I-Cache Data Diagnostics set 0	I-CDATA0	I-Cache
0x0d	0x00002000 | 0x00002FF8	I-Cache Data Diagnostics set 1	I-CDATA1	I-Cache
0x0d	0x00003000 | 0x00003FF8	I-Cache Data Diagnostics set 2	I-CDATA2	I-Cache
0x0d	0x00004000 | 0x00004FF8	I-Cache Data Diagnostics set 3	I-CDATA3	I-Cache
0x1c	0x00000000 | 0x00000FE0	D-Cache Tag Diagnostics set 0	D-CTAG0	D-Cache
0x1c	0x00001000 | 0x00001FE0	D-Cache Tag Diagnostics set 1	D-CTAG1	D-Cache
0x1c	0x00001000 | 0x00001FE0	D-Cache Tag Diagnostics set 2	D-CTAG2	D-Cache
0x1c	0x00001000 | 0x00001FE0	D-Cache Tag Diagnostics set 3	D-CTAG3	D-Cache
0x1d	0x00001000 | 0x00001FF8	D-Cache Data Diagnostics set 0	D-CDATA0	D-Cache
0x1d	0x00002000 | 0x00002FF8	D-Cache Data Diagnostics set 1	D-DATA1	D-Cache
0x1d	0x00003000 | 0x00003FF8	D-Cache Data Diagnostics set 2	D-CDATA2	D-Cache
0x1d	0x00004000 | 0x00004FF8	D-Cache Data Diagnostics set 3	D-CDATA3	D-Cache

3. Register Maps

Access to registers should be as word data.

3.1. BCR: Buffer Control Register

WDDP sets the number of columns (depth) of write buffers. MCE enables Merge and Collapse. All buffers are cleared by writing 1 to ICL and RCL. Upon completion of a clear operation, they return to 0. Write buffers have no bit for clears. IR, RE and WE enable all buffer operations.

31 ... 6	5	4	3	2	1	0
Reserved	MCE	ICL	RCL	IE	RE	WE

Address: 0x80000000 (ASI=0x4)
Reset State: 0x00000000

Figure 3-1 BCR Register

bit31-6: Reserved
bit8-6: Write Buffer Depth [WBDP]
bit5: Merge & Collapse Enable [MCE]
bit4: Instruction Buffer Clear [ICL]
bit3: Read Buffer Clear [RCL]
bit2: Instruction Buffer Enable [IE]
bit1: Read Buffer Enable [RE]
bit0: Write Buffer Enable [WE]

Table 3-1

MCE	Merge & Collapse
0	Merge & Collapse Collapse is disabled
1	Merge & Collapse is enabled

Table 3-2 Buffer Clear

ICL	Instruction buffer clear	RCL	Read Buffer Clear
0	No operation	0	No operation
1	Buffer Clear	1	Buffer Clear

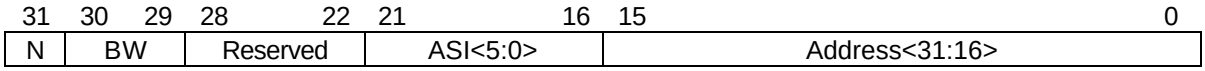
Table 3-3 Buffer Enable

IE	Instruction Buffer Enable	RE	Read Buffer Enable	WE	Write Buffer Enable
0	Disable	0	Disable	0	Disable
1	Enable	1	Enable	1	Enable

3.2. ARSR : Address Range Specifier Register

This register is for setting SPARClite bus address ranges from CS0# To CS5#. Start addresses of address ranges are set in this register. Bits which do not make address comparisons are set in the AMR register. If N bit is 1, its range is set as a non-cache area. ARSR0-5 set SPARClite bus areas. BW decides SPARClite area bus widths specified in CS#1~CS#5. CS0# is for ROM area exclusive use. The start address of CS0# is 0. ARSR and CS# correspond as shown below. CS area settings must not overlap. CS1#~CS5# are not asserted unless both their ARSR and AMR corresponding areas are set (CS# is not asserted when only ARSR or AMR is set).

ARSR0 (0x80000100) for setting SPARC area CS0# (0x80080000 on reset)
ARSR1 (0x80000108) for setting SPARC area CS1# (Undefined on reset)
ARSR2 (0x80000110) for setting SPARC area CS2# (Undefined on reset)
ARSR3 (0x80000118) for setting SPARC area CS3# (Undefined on reset)
ARSR4 (0x80000120) for setting SPARC area CS4# (Undefined on reset)
ARSR5 (0x80000128) for setting SPARC area CS5# (Undefined on reset)



Address: 0x80000100 (ASI=0x4)-0x8000128
Reset State: Undefined (ARSR0=0x80080000)

Figure 3-2 ARSR Register

bit31: Non-cache [N]
bit30-29: Bus width [BW] (Reserved for CS#0)
bit29-22: Reserved
bit21-16: ASI<5:0> (Reserved for CS#0)
bit15-0: Address<31:16> (Reserved for CS#0)

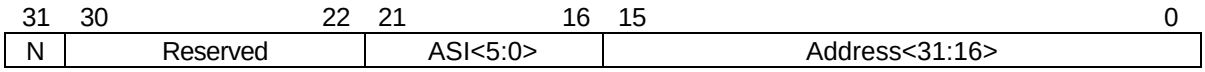
BW	Bus width
00	64 bit
01	32 bit
10	16 bit
11	8 bit

Table 3-4 Bus

3.3. SDARS : SDRAM Address Range Specifier Register

This register is for setting SDRAM bus areas. Address ranges of starting addresses are set in this register. Bits which do not make address comparisons are set in the SDAM Register. When N bit is 1, its range is set as a non-cache area. All area settings must be set so as not to overlap. (CS0#~CS5# areas must also be set so as not to overlap).

SDARS0 (0x80000130) for setting SDRAM area no corresponding CS# (Undefined on reset)
SDARS1 (0x80000138) for setting SDRAM area no corresponding CS# (Undefined on reset)



Address: 0x80000130 (ASI=0x4)-0x8000138
Reset State: Undefined

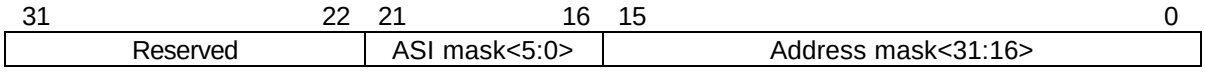
Figure 3-3 SDARS Register

bit31: Non-cache [N]
bit30-22: Reserved
bit21-16: ASI<5:0>
bit15-0: Address<31:16>

3.4. AMR : Address Mask Register

This is the register for setting CS0#~CS5# address ranges. It sets address ranges in combination with the ARSR Register. Bits which are set 1 in the AMR Register do not compare addresses with the ARSR Register. Only AMR Register bits set to 0 compare memory addresses with the ARSR Register and assert CS# if they agree. AMR and CS# correspond as follows:

AMR0 (0x80000200) for setting SPARC area CS0# (ROM area exclusive use. 0x00030001 on reset)
AMR1 (0x80000208) for setting SPARC area CS1# (Undefined on reset)
AMR2 (0x80000210) for setting SPARC area CS2# (Undefined on reset)
AMR3 (0x80000218) for setting SPARC area CS3# (Undefined on reset)
AMR4 (0x80000220) for setting SPARC area CS4# (Undefined on reset)
AMR5 (0x80000228) for setting SPARC area CS5# (Undefined on reset)



Address: 0x80000200 (ASI=0x4)-0x8000228
Reset State: Undefined (AMR0=0x00030001)

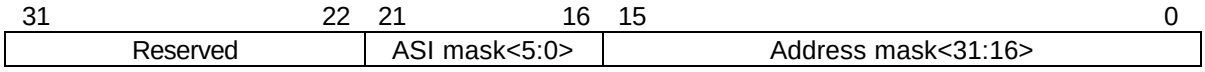
Figure 3-4 AMR Register

bit31-22: Reserved
bit21-16: ASI<5:0>
bit15-0: Address<31:16>

3.5. SDAM : SDRAM Address Mask Register

This register is for setting SDRAM address ranges. It sets address ranges in combination with the SDARS Register. Bits which are set 1 in the AMR Register do not compare addresses with the SDARS Register. Only SDAM Register bits set to 0 compare memory addresses with the SDARS Register, and if they agree regard this as access to SDRAM.

SDAMR0 (0x80000230) for setting SDRAM area no corresponding CS# (Undefined on reset)
SDAMR1 (0x80000238) for setting SDRAM area no corresponding CS# (Undefined on reset)



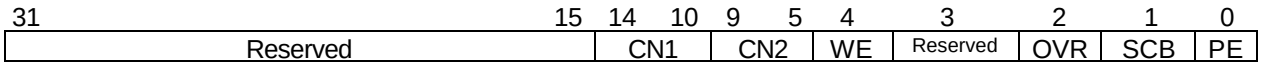
Address: 0x80000230 (ASI=0x4)-0x8000238
Reset State: Undefined

Figure 3-5 SDAM Register

bit31-22: Reserved
bit21-16: ASI<5:0>
bit15-0: Address<31:16>

3.6. WSSR : Wait State Specifier Register

Sets wait state generation for all CS# areas.



Address: 0x80000400 (ASI=0x4): CS0# Reset State: 0x00007ff4
Address: 0x80000408 (ASI=0x4): CS1# Reset State: 0x00000000
Address: 0x80000410 (ASI=0x4): CS2# Reset State: 0x00000000
Address: 0x80000418 (ASI=0x4): CS3# Reset State: 0x00000000
Address: 0x80000420 (ASI=0x4): CS4# Reset State: 0x00000000
Address: 0x80000428 (ASI=0x4): CS5# Reset State: 0x00000000
Reset State: 0x00000000

Figure 3-6 WSSR Register

bit31-15: Reserved
bit14-10: count1 [CN1]
bit9-5: count2 [CN2]
bit4: wait enable [WE]
bit3: Reserved
bit2: override [OVR
bit1: single cycle burst mode [SCB]
bit0: parity enable [PE]

Table 3-5

wait enable	[WE]	Enables internal wait state generation for corresponding CS areas. [OVR], [CN1], [CN2] and [SCB] functions all become valid when [WE] is "1".
override	[OVR]	When this bit is "1", external READY# is also received. (The READY# which comes first is given priority), When this bit is "0", READY# from the exterior is masked and received. However, the mask function does not work for READY# which is input in the same cycle as AS#, in other words for READY# which is input by 0wait. This bit becomes valid when [WE] is "1". Thus this bit should be set together with [WE].

		Note: When [WE] is “0”, READY# input from c w exterior is always valid.
count1	[CN1]	Specifies the number of waits for the first cycle of non-burst and burst transfers. The number of waits is the value specified for this field + 1, These bits are valid when [WE] is “1”.
count2	[CN2]	Specifies the number of waits for the 2nd cycle of burst transfers and thereafter. Thus when 0 is specified, it is 1 wait. These bits are valid when [WE] is “1”.
single cycle burst mode	[SCB]	If this bit is set to “1”, transfers from the 2nd cycle on of a burst transfer are performed with 0wait. This bit is valid when set to “1”. Thus this bit should be set together with [WE].
parity enable	[PE]	Enables and disables Parity functions for access to the corresponding CS# areas.

Note: When READY# returns in the same cycle as AS#, 0wait is set and when READY# returns in the next cycle 1wait is set.

3.7. MXPEF : MEXC Parity Error Flag Register

Flags are set when a MEXC or parity error occurs during reads and writes. To clear a Flag, write “0” or perform a reset.

31 7	6	5	4	3	2	1	0
Reserved	DMXRE	DMXWE	DPRE	Reserved	MXRE	MXWE	PRE

Address: 0x80000430 (ASI=04)
Reset State: 0x00000000

Figure 3-7 MXPEF Register

bit31-7: Reserved
bit6: DMA MEXC Read Error [DMXRE]
bit5: DMA MEXC Write Error [DMXWE]
bit4: DMA Parity Read Error [DPRE]
bit3: Reserved
bit2: CPU MEXC Read Error [MXRE]
bit1: CPU MEXC Write Error [MXWE]
bit0: CPU Parity Read Error [PRE]

3.8. MXPECR : MEXC Parity Error Control Register

Performs Return Mode Enable/Disable settings and Parity Check Odd/Even settings during the next Data Read from the CPU when MEXC flags are set during data writes.

31 2	1	0
Reserved	PAR	MXWEE

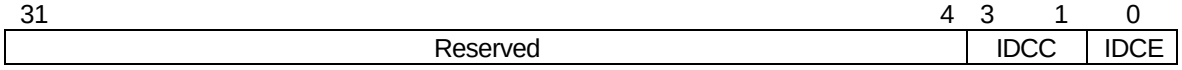
Address: 0x80000438 (ASI=04)
Reset State: 0x00000000

Figure 3-10 MXPECR Register

bit31-2: Reserved
bit1: Parity bit (Odd Priority=0, Even Priority=1) [PAR]
bit2: MEXC Write Error Enable [MXWEE]

3.9. IDCCR : Idle Cycle Control Register

Performs automatic Idle Cycle insertion settings for CS0# area access.



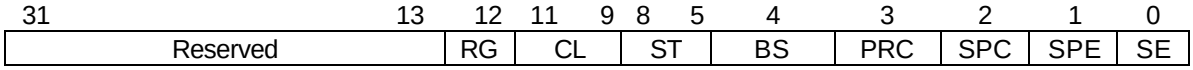
Address: 0x80000440 (ASI=04)
Reset State: 0x00000000

Figure 3-11 IDCCR Register

bit31-4: Reserved
bit3-1: Idle Cycle Count [IDCC]
bit0: Idle Cycle Enable [IDCE]

3.10. SDCFG : SDRAM Configuration Register

This register decides such SDRAM operating modes as CAS Latency, SDRAM Type, Bus Size etc.



Address: 0x80000800 (ASI=04)
Reset State: 0x00000400

Figure 3-12 SDCFG Register

*Burst Type is sequential fixed.
bit31-13: Reserved
bit12: Registered Mode [RG] ---- This bit is WRITE ONLY. i.e., the bit can not be read out.
bit1-9: CAS Latency [CL]
bit8-5: SDRAM Type [ST]
bit4: Bus Size [BS]
bit3: Precharge Control [PRC
bit2: SDRAM Parity Control [SPC
bit1: SDRAM Parity Enable [SPE]
bit0: SDRAM Enable [SE]

Table 3-6 CAS Latency

CL	CAS Latency
000	Reserved
001	1
010	2
011	3
100	Reserved
101	Reserved
110	Reserved
111	Reserved

Table 3-7 Bus Size

BS	Bus Size
0	32bit
1	64bit

Table 3-8 SDRAM Type

ST	SDRAM Type
0000	Reserved
0001	16Mbit 2bank x 1M x 8bit
0010	16Mbit 2bank x 512k x 16bit
0011	Reserved
0100	Reserved
0101	64Mbit 4bank x 2M x 8bit
0110	64Mbit 4bank x 1M x 16bit
0111	64Mbit 4bank x 512k x 32bit
1000	Reserved
1001	Reserved(128Mbit 4bank x 4M x 8bit)
1010	Reserved(128Mbit 4bank x 2M x 16bit)
1011	Reserved
1100	Reserved
1101	Reserved(256Mbit 4bank x 8M x 8bit)
1110	Reserved(256Mbit 4bank x 4M x 16bit)
1111	Reserved

Table 3-9 Precharge Control

PRC	Precharge Control
0	All banks
1	Each bank

Table3-10 SDRAM Parity Control

SPC	SDRAM Parity Control
0	Odd Parity
1	Even Parity

Table 3-11 SDRAM Parity Enable

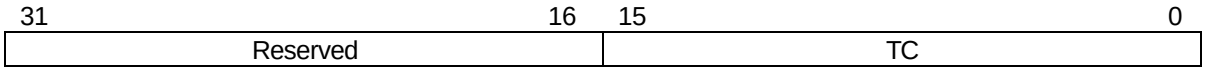
SPE	SDRAM Parity Enable
0	Disable
1	Enable

Table 3-12 SDRAM Enable

SE	SDRAM Enable
0	Disable
1	Enable

3.11. ART : Auto Refresh Timer Register

SDRAM refresh spaces are decided by the values written to auto refresh timers. Clock input is the same as the BIU unit clock. (CLKIN X frequency multiplier setting)



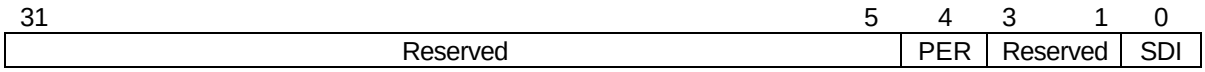
Address: 0x80000808 (ASI=0x4)
Reset State: 0x0000FFFF

Figure 3-13 ART Register

bit31-16: Reserved
bit15-0: Timer count [TC]

3.12. SSR : SDRAM Status Register

Shows the status of the SDRAM I/F Unit. Access to this register is read only. Writes are invalid. All bit settings are done automatically by the hardware. When parity errors occur in SDRAM data reads, the value "1" is set to the PER bit. The PER bit is reset (set to "0") during read access to this register. The SDI bit value is preserved.



Address: 0x80000810 (ASI=0x4)
Reset State: 0x00000000

Figure 3-14 SSR

bit31-5: Reserved
bit4: Parity Error Flag [PER]
bit3-1: Reserved
bit0: SDRAM Initial Wait Indicator

Table 3-13 Parity Error

PER	Parity Error
0	No Error
1	Parity Error

Table 3-14 SDRAM Initial Wait Indicator

SDI	SDRAM Initial Wait Indicator
0	In initial process
1	Initialization finished

3.13. DMCR[0:1] : DMA Control Register

The DMA Control Register performs all DMA operating mode settings and start/stop controls. Whether a source address range is SDRAM or a SPARClite bus is specified by the SBSn bit. The SIOn bit indicates that a source address range is I/O. When an SIOn bit is set to "1" (when the source address is an I/O area), the address becomes fixed and is not incremented. The SCSNn bit specifies in which CS range a source address is located. The SBWn bit specifies source data bus width. The DBSn bit specifies whether a destination address range is SDRAM or SPARClite. The DCSn bit specifies in which CS range a destination address is located. The DBWn bit specifies destination data bus widths. The TCn bit controls EOP signals. If this bit is set to "1", EOP signals are output upon completion of transfers. The SBn bit controls DMA operations. If "1" is set to this bit, DMA operation starts. Even if an SB bit is set in the same channel during a DMA operation, the DMA operation is not affected. Also, if an SB bit I set in another channel during a DMA operation in one direction, a DMA transfer in the other direction is activated after the DMA transfer in progress has ended. SIOn, SCSn and SDSn bits become valid when the SBSn bit is set. Likewise, DCSNn and DDSn bits become valid when the DBSn bit is set. If the SB0 bit is cleared to "0" during a DMA transfer, the DMA is aborted and the ABTn bit is set. If a parity error or MEXC is detected during a DMA transfer, DMA stops, and the ERRn bit is set. All DMACR bit settings and operations should be performed at the same time.

31	30	29	28 26	25 24	23	22	21	20 18	17 16	15 9	8	7	6	5 1	0
SBS0	R	SIO0	SCSN0	SBW0	DBS 0	R	DIO0	DCSN0	DBW0	reserved	TC0	ERR0	ABT0	reserved	SB 0

Address: .0x80000C00 (ASI=0x4)
Reset State: 0x00000000

Figure 3-15 DMCR0 Register

31	30	29	28 26	25 24	23	22	21	20 18	17 16	15 9	8	7	6	5 1	0
SBS1	R	SIO1	SCSN1	SBW1	DBS 1	R	DIO1	DCSN1	DBW1	reserved	TC1	ERR1	ABT1	reserved	SB 1

Address: .0x80000C00 (ASI=0x4)
Reset State: 0x00000000

Figure 3-16 DMCR1 Register

bit31: Source Bus Select [SBS]
bit30: Reserved
bit29: Source I/O Select [SIO]
bit28-26: Source CS Number [SCSN]
bit25-24: Source Bus Width [SBW]
bit23: Destination Bus Select [DBS]
bit22: Reserved
bit21: Destination I/O Select [DIO]
bit20-18: Destination CS Number [DCSN]
bit17-16: Destination Bus Width [DBW]
bit15-9: Reserved
bit8: Transfer Complete Out [TC]
bit7: Error [ERR]
bit6: Abort [ABT]
bit5-1: Reserved
bit0: Start Bit [SB]

Table 3-15 Source Bus Select

SBS	Source Bus Select
0	SPARClite region
1	SDRAM region

Table 3-16 Source I/O Select

SIO	Source I/O Select
0	Address is incremented
1	Address is not incremented

Table 3-17 Source CS Select

SCSN	Source CS Select
000	assert CS0
001	assert CS1
010	assert CS2
011	assert CS3
100	assert CS4
101	assert CS5
11-	Any CS is not asserted

Table 3-18 Source Bus Width

SBW	Source Bus Width
00	Double word (64 bit)
01	Word (32 bit)
10	Half word (16bit)
11	Byte (8 bit)

Table 3-19 Destination Bus Select

DBS	Destination Bus Select
0	SPARClite region
1	SDRAM region

Table 3-20 Destination I/O Select

DIO	Destination I/O Select
0	Address is incremented
1	Address is not incremented

Table 3-21 Destination CS Select

DCSN	Destination CS Select
000	assert CS0
001	assert CS1
010	assert CS2
011	assert CS3
100	assert CS4
101	assert CS5
11-	Any CS is not asserted

Table 3-22 Destination Bus Width

DBW	Destination Bus Width
00	Double word (64 bit)
01	Word (32 bit)
10	Half word (16bit)
11	Byte (8 bit)

Table 3-23 Transfer Complete Out

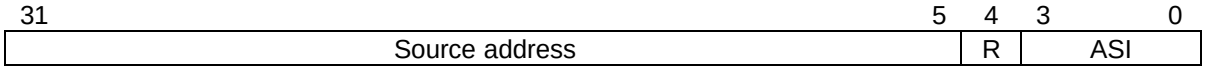
TC	Transfer complete out
0	EOP output is disabled
1	EOP output is enabled

Table 3-24 Start Bit

SB	Start Bit
0	Stop
1	Start

3.14. DMSAR[0:1] : DMA Source Address Register

DMA source address registers are used to specify DMA transfer source addresses. These registers are assigned to 0x80000c08 (DMSA0 for Channel 0) and 0x80000c28 (DMSA1 for Channel 1). The setting unit is burst length (32 bytes). Transfer source ASI is specified by the lower order 4 bits.



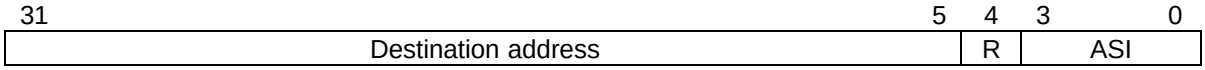
Address: 0x80000C08 (ASI=0x4) DMSAR0
Address: 0x80000C28 (ASI=0x4) DMSAR1
Reset State: 0x00000000

Figure 3-17 DMSAR Register

bit31-5: Source address
bit4: Reserved
bit3-0: ASI<3:0>

3.15. DMDAR[0:1] : DMA Destination Address Register

DMA destination address registers are used to specify DMA transfer destination addresses. These registers are assigned to 0x80000c10 (DMDA0 for Channel 0) and 0x80000c30 (DMDA1 for Channel 1). The setting unit is burst length (32 bytes). Transfer destination ASI is specified by the lower order 4 bits.



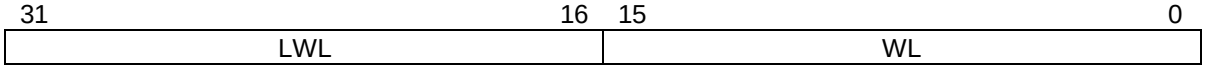
Address: 0x80000C10 (ASI=0x4) DMDAR0
Address: 0x80000C30 (ASI=0x4) DMDAR1
Reset State: 0x00000000

Figure 3-18 DMDAR Register

bit31-5: Destination address
bit4: Reserved
bit3-0: ASI<3:0>

3.16. DMWL[0:1] : DMA Word Length Register

DMA word length registers specify the number of DMA transfer data. These registers are assigned to 0x80000c18 (DMWL0 for Channel 0) and 0x80000c38 (DMWL1 for Channel 1). The setting unit is burst length (32 bytes).



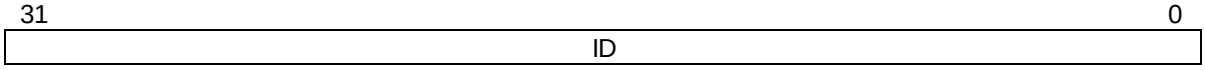
Address: 0x80000C18 (ASI=0x4) DMWL0
Address: 0x80000C38 (ASI=0x4) DMWL1
Reset State: 0x00000000

Figure 3-19 DMWL Register

bit31-16: Left Word Length [LWL]
bit15-0: Word Length [WL]

3.17. IDR : ID Register

ID registers store ID numbers for identifying processors. Read values are “0x0860XXXX”, and the lower order 16 bits are undefined. This register is Read Only.



Address: 0x80000ff0 (ASI=0x4) IDR
Reset State: 0x0860XXXX

Figure 3-20 IDR Register

bit31-0: ID (Value is 0x0860XXXX)

4. CPU Core

4.1. Overview

The SS200 is a High-end embedded SPARC core developed for installation with the ROSS Technology Company hyperSPARC (RT6xx) as a base. The SS200 Core consists of an IU Part having 2-issue superscalar architecture, a 16KB/4-way instruction cache, a write-through system 16KB/4-way data cache and a IMB (Intra-Module Bus) Bus Interface which is the internal bus of the SS200 chip. The SS200 Core conforms to SPARC V8 architecture. Instruction types, execution cycle numbers and comparisons with the old SPARClite core are shown separately. The SS200 Core simultaneously fetches two 32-bit instructions using a 64-bit instruction bus and simultaneously executes 2 instructions using 2 ALUs. (Instructions which can be simultaneously executed are partially restricted).

Internal caches control both instructions and data using 16KB/4-way with 64 bits as 1 unit. Data caches are write-through systems. The SS200 is connected to external modules by IMB buses. IMB buses have a 32-bit address bus, a 64-bit data bus and bus control signals. Because of the internal buses, SS200 external pins have no IMB buses. IMB bus data buses support Bi-endian. Little-endian data can be directly accessed using Core register settings. The SS200 Core operates at a clock of 2 X the IMB bus interface. It operates at a maximum of 200mhz.

4.2. Power Down Mode

The SS200 can be set to any of 4 modes- Cache OFF Mode, Normal Mode, Sleep Mode and Stop Mode. In Sleep Mode, since the PLL is operating, a return to normal mode can be made by the external pins. In Stop Mode, however, the PLL is also stopped, and a reset is therefore required for a return to Normal Mode.

4.3. Debug Support Function

The SS200 supports a break function, address trace buffer and step operation function as debug functions. Selection of Debug Mode and Normal mode is performed in accordance with external pin status on reset. 3 types of break function are supported: external pin breaks, address conveyor breaks and software breaks. Address trace buffers store program count values immediately preceding breaks in 16 columns. By reading this register after breaks, operation immediately preceding a break can be confirmed. Traps can be made to occur in 1-step units by setting internal register step execution flags.

4.4. Non-cache

Data handled as Non-cache by the SS200 is area access specified as Non-cache by the ARSR and AMR registers.

4.5. CPU Core Block Diagram

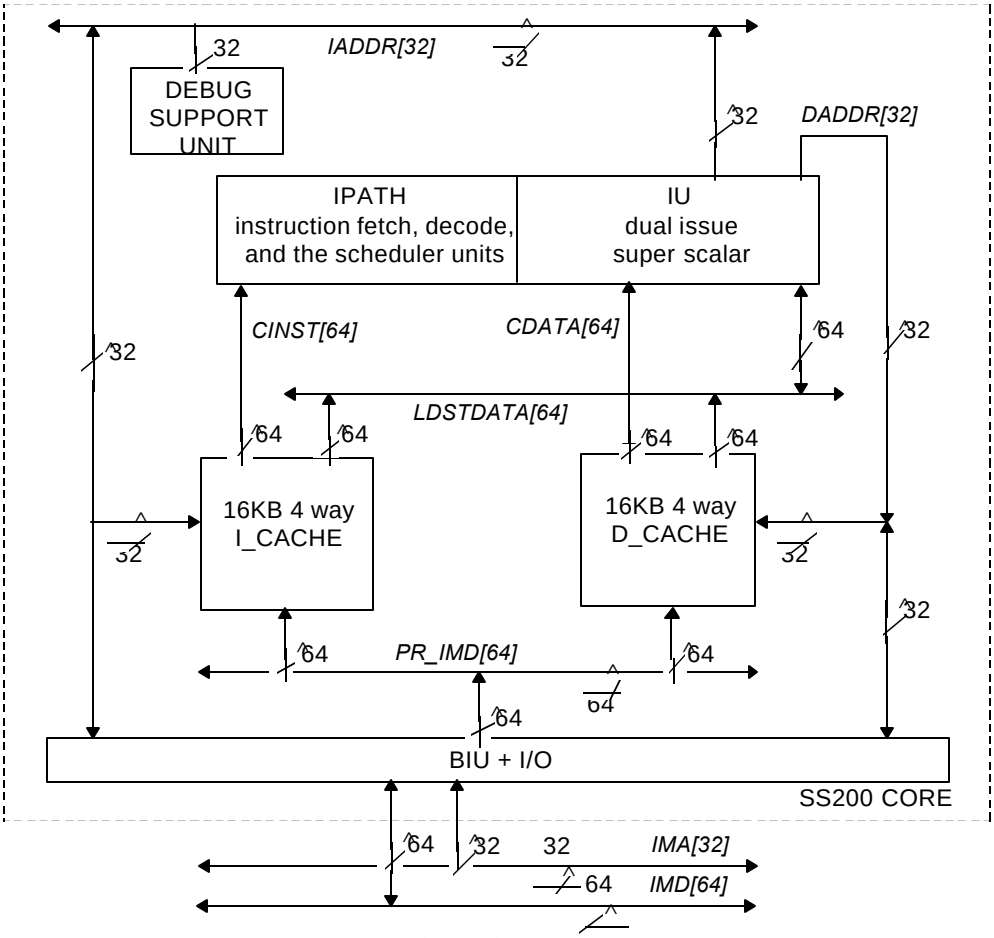


Figure 4-1 CPU Core Block Diagram

4.6. MB8686X IU Block Diagram

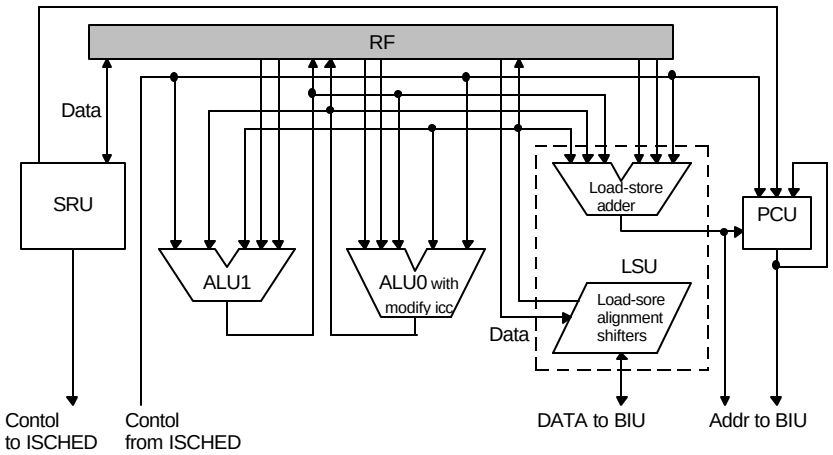


Figure 4-2 SS200 Core IU Block Diagram

5. MB86860 BIU

The MB86860 Bus Unit (BIU) functions as an interface with the SS200 Core and external chip circuits. It operates at frequency multiples (X2, X3, X4) of the external input clock, with a maximum of 100MHz. It consists of 3 modules: a Data Buffer, an SDRAM Interface and a SPARClite Interface.

5.1. Data Buffer (DBU)

5.1.1. Instruction Buffer (IB)

- Has valid-bits indicating that a 64-bit 4-column buffer, buffer data address-tag and data are valid. There are 4 valid-bits.
- Reads 4 double-word data using burst transfers in addresses in sequence from requested addresses when there is a miss in instruction buffer tags. Also outputs appropriate address double word data to IMB buses.
- Outputs data corresponding to the appropriate addresses to IMB buses when there is a tag hit.
- Instruction fetches from non-cache areas bypass buffers. Invalidates when there is a tag hit. Invalidates valid bits when a MEXC signal is asserted.
- Cache target areas are ASI=8 and ASI=9. Double word loads for these areas are regarded as instruction fetches.
- Invalidates if there is a hit to an Atomic-load/Store instruction for ASI=8 and ASI=9 (handles as non-cache).
- When FLUSH instructions are executed the IB is also flushed.

5.1.2. Read Buffer (RB)

- Has two 64-bit 4-column buffers. Each buffer has a valid-bit which indicates that buffer data address tags and data are valid. Has 1 tag and 1 valid-bit for double-words.
- When buffer replacement is required, replacement is by means of an LRU algorithm.
- Outputs data corresponding to the appropriate address to an IMB bus when an address in a load instruction hits a tag.
- Reads 4 double-word data from external memory by addresses in sequence from the requested address and outputs data corresponding to the appropriate addresses to IMB buses when an address in a load instruction misses all RB tags.
- Bypasses buffers during execution of load instructions from non-cache areas. Invalidates when a tag is hit.
- Handles Atomic-load/Store instructions as non-cache in all areas.

5.1.3. Write Buffer (WB)

- Outputs Store data via FIFO. BIU-BUS output is single transfers. FIFO is 64-bit X (16 columns-6 columns change possible).
- Overwrites to valid locations when, in case of bytes, half words and words, Store instructions are the same address as the immediately preceding data (a FIFO input column tag is hit). (when Merge & Collapse is enabled).
- Controls WB data with valid bits in byte units and reflects to the Byte Enable pin upon output.
- Handles Atomic-load/Store instructions as non-cache in all areas.

5.1.4. Buffering Policy

- The IB and RB are accessed in the order of instruction execution.
- When Store Data hits in the first column of a WB, that data is rewritten. (when Merge and Collapse is enabled).
- When Atomic-load/Store instructions are executed, WB contents is first written to memory, and the data is then read from memory to the RB. If there is a hit in the RB, it is invalidated. Stores are handled as non-cache. After that, Stores are then executed. Data is then handled as non-cache.

The order of data access between Read Buffers (RB) and Write Buffers (WB) is as shown below.

Table 5-1 Access Order between RB and WB

Access Type		hit judgment	Operation	Burst Access
Cache Area (Data Access)	Store ASI==a,b & NC==0	RB: miss & WB: miss	Writes data to WB	OFF
		RB: hit & WB: miss	Writes data to WB	OFF
		RB: miss & WB: hit	Merges with that data when there is a hit to initial WB data. Otherwise, writes data to WB.	OFF
		RB: hit & WB: hit	Merges with that data when there is a hit to initial WB data. Otherwise, writes data to WB.	OFF
	Load ASI==a, b & NC==0	RB: miss & WB: miss	Reads 4 double words from external memory and writes them to the RB. Simultaneously sends 1 double word to the CPU Core. Updates or replaces RB tags.	ON
		RB: miss & WB: hit	Writes the hit data to external memory when there are multiple hits or a single hit to the WB and then reads 4 double words from external memory to the RB. Simultaneously sends 1 double word to the CPU Core. Updates or replaces RB tags.	ON
		RB: hit & WB: miss	Sends 1 double word from the RB to the CPU Core	NA
		RB: hit & WB: hit	Writes the hit data to external memory while updating the RB when there are multiple hits or a single hit to the WB. Thereafter sends 1 double word to the CPU Core.	NA
Cache Area (instruction)	Load/Fetch ASI==8, 9 & NC==0	IB: miss	Reads 4 double words from external memory and writes them to the IB. Simultaneously sends 1 double word to the CPU Core. Replaces tags	ON
		IB: hit	Sends 1 double word to the CPU Core.	NA

Table 5-2 Access Order between RB and WB (continued)

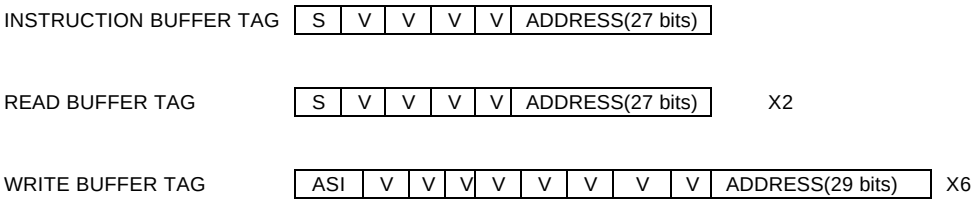
Access Type		hit judgment	Operation	Burst Access
Non-cache area (data access)	Store ASI==8, 9	IB: hit	First writes the WB, then writes data to external memory.	OFF
		IB: miss		
	Store ASI==a, b & NC==1	RB: hit	First writes the WB, then writes data to external memory. Invalidates tags if there is a hit to the RB.	OFF
		RB: miss		
	Store ASI != 8,9,a, b	DON'T CARE	First writes the WB, then writes data to external memory.	OFF
	Load ASI==a, b & NC==1	RB: hit	First writes the WB to external memory, then reads data from external memory or I/O and sends it to the CPU Core. Basically, RB tags are not updated but are invalidated if there is a hit to the RB. Data size is decided at IMSIZE<1: 0>.	OFF
		RB: miss		
	Load ASI != 8,9,a, b	RB: hit	First writes the WB to external memory, then reads data from external memory or I/O and sends it to the CPU Core. Data is not written to the RB. Data size is decided at IMSIZE<1: 0>.	OFF
		RB: miss		
Non-cache area (instruction)	Load/Fetch ASI==8, 9 & NC==1	IB: miss	First writes the WB to external memory, then reads data from external memory or I/O and sends it to the CPU Core. Data size is decided at IMSIZE<1: 0>.	OFF
		IB: hit		

Table 5-3 Access Order between RB and WB (continued)

Access Type		hit judgment	Operation	Burst Access
Cache Area (Data Access)	ASI==8, 9	IB: hit	First writes the WB to external memory, then reads data from external memory or I/O and sends it to the CPU Core. Continu-	OFF
		IB: miss	ously stores data to external memory or I/O.	
	ASI==a, b	RB: hit	First writes the WB to external memory, then reads data from external memory or I/O and sends it to the CPU Core. Continu-	OFF
		RB: miss	ously stores data to external memory or I/O. Invalidates the RB if there is a hit to the RB.	
	ASI != 8,9,a, b	DON'T CARE	First writes the WB to external memory, then reads data from external memory or I/O and sends it to the CPU Core. Continu- ously stores data to external memory or I/O.	OFF

5.2. Data Buffer Tag Format

The following shows instruction buffer, read bufer and write buffer format.



S: Supervisor bit
V: Valid bit

Figure 5-1

5.3. SDRAM Interface (SDB)

5.3.1. Summary

The SDRAM I/F Unit is a module belonging to the Bus Interface Unit (BIU) which functions as the interface between the SS200 Core and external chip circuits, and it has the following functions:

(1) Has dedicated 64-bit data bus and 13-bit address bus pins.
(2) Performs external SDRAM address control, data transfer control, command control etc.
(3) Performs SDRAM transfers in 64-bit buses with burst length 4. Moreover, performs them wih burst length 8 in 32-bit buses.
(4) CAS latency can be set from 1 to 3. Uses sequential burst type.
(5) Outputs 4 SCS (SDRAM Chip Select) signals.
(6) Auto-refresh and self-refresh settings supported.
(7) Performs SDRAM read and write operations in Burst Mode.

5.3.2. Block Diagram

The following is a Block Diagram of the SDRAM Interface Part.

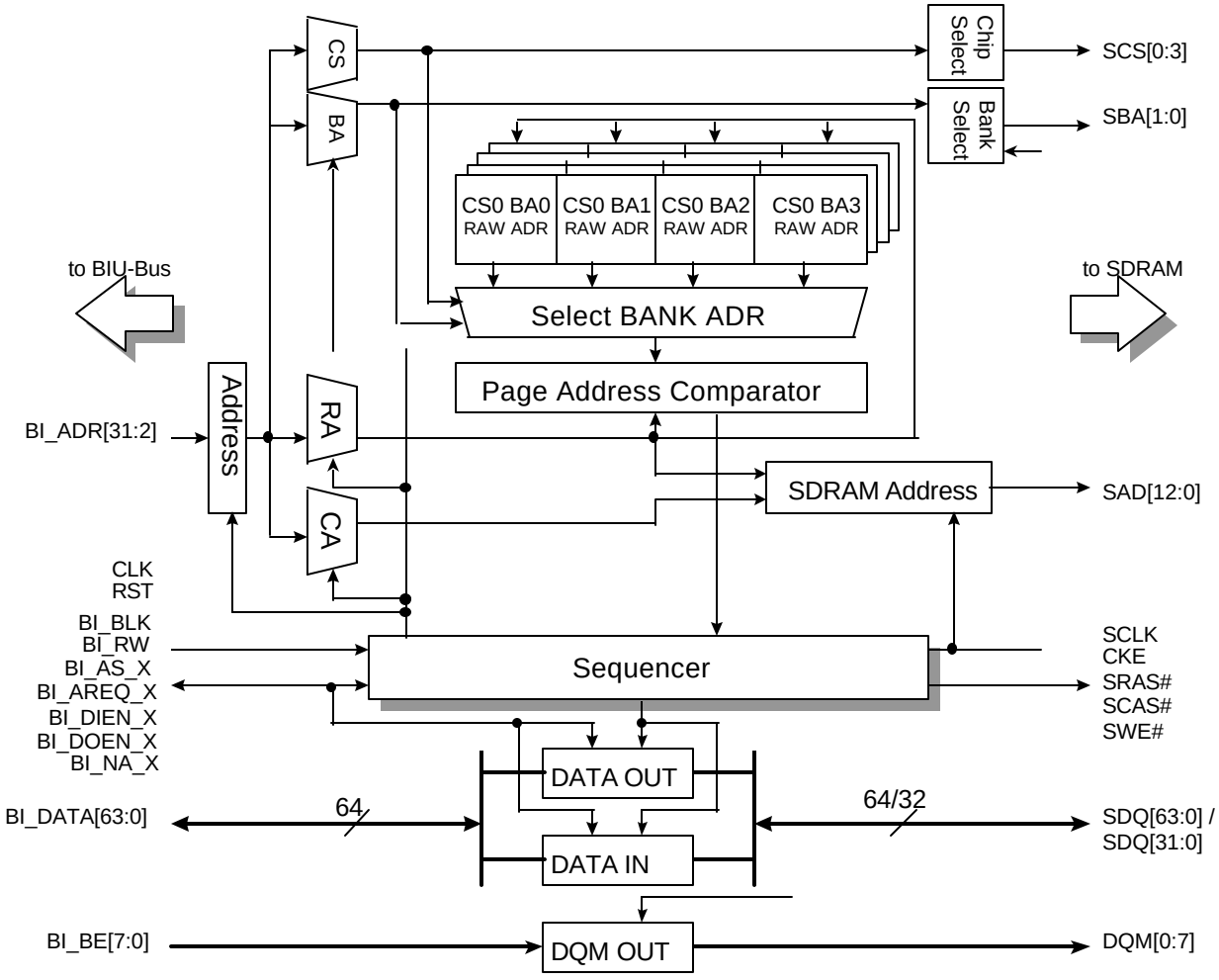


Figure 5-2 SDRAM I/F Block Diagram

5.3.3. Signals

SDRAM bus signals are explained below. Signal direction takes the BIU Unit as the standard.

Table 5-4

SCLK (output)	SDRAM clock signal. Should be linked to SDRAM clock input. Clock frequency is the same as internal IMB bus frequency.
CKE (ouput)	SDRAM Clock Enable signal.
SRAS# (output)	SDRAM RAS signal.
SCAS# (output)	SDRAM CAS signal.
SWE# (output)	SDRAM Write Enable signal.
SCS3# - SCS0# (output)	SDRAM Chip Select signals.
SBA[1:0] (output)	SDRAM Bank Select signal.
SADR[12:0] (output)	SDRAM Address signal. Addresses are multiplexed.
SDQ[63:0] (I/O)	SDRAM Data Bus.
SDQM[0:7] (output)	SDRAM Input Mask (Output Enable signal).
SDP[0:7] (I/O)	SDRAM Parity signal.

5.3.4. Parity Generation Check Functions

Parity checks during SDRAM reads and Parity Generation during SDRAM writes are performed by setting 1 to bit1(SPE) of the SDRAM Configuration Register (SDCFG). The SDRAM I/F Unit performs each odd/even parity generation and check in the SDQ signal byte in accordance with the setting of SDCFG bit2(SPC).

5.3.5. SDRAM Bus Connections with SDRAM

5.3.5.1. Addresses

SS200 address output pin connections with SDRAM address input pins for each operating mode are shown here.

Table 5-5 SDRAM Addresses

SDRAM		S200 Pin Names				
		SBA1	SBA0	SAD12	SAD11	SAD10-0
256Mbit (T.B.D.)	8Mwordx8bitx4bank	A14	A13	A12	A11	A10-0
	4Mwordx16bitx4bank	A14	A13	A12	A11	A10-0
	2Mwordx32bitx4bank	A13	A12	-	A11	A10-0
128Mbit (T.B.D.)	4Mwordx8bitx4bank	A13	A12	-	A11	A10-0
	2Mwordx16bitx4bank	A13	A12	-	A11	A10-0
	1Mwordx32bitx4bank	A12	A11	-	-	A10-0
64Mbit	2Mwordx8bitx4bank	A13	A12	-	A11	A10-0
	1Mwordx16bitx4bank	A13	A12	-	A11	A10-0
	512Kwordx32bitx4bank	A12	A11	-	-	A10-0
16Mbit	1Mwordx8bitx4bank	-	A11	-	-	A10-0
	512Kwordx16bitx2bank	-	A11	-	-	A10-0

This feature are reserved for future expansion.

5.3.5.2. SDRAM Data Mask (SDQM)

Correspondence of each SDRAM data mask (SDQM) with SDRAM data is shown here.

Table 5-6 SDRAM Data Mask

Bus Size	SDQ							
	<63:56>	<55:48>	<47:40>	<39:32>	<31:24>	<23:16>	<15:8>	<7:0>
64bit mode	SDQM0	SDQM1	SDQM2	SDQM3	SDQM4	SDQM5	SDQM6	SDQM7
32bit mode	NC	NC	NC	NC	SDQM4	SDQM5	SDQM6	SDQM7

5.3.5.3. SDRAM Parity

Correspondence of each SDRAM parity bit with SDRAM data is shown here.

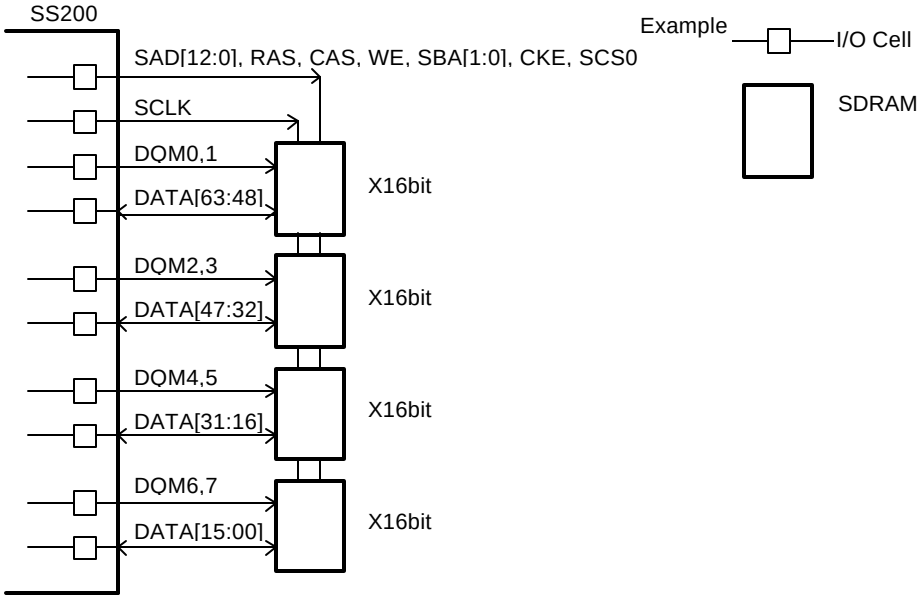
Table 5-7 SDRAM Parity

Bus Size	SDQ							
	<63:56>	<55:48>	<47:40>	<39:32>	<31:24>	<23:16>	<15:8>	<7:0>
64bit mode	SDP0	SDP1	SDP2	SDP3	SDP4	SDP5	SDP6	SDP7
32bit mode	NC	NC	NC	NC	SDP4	SDP5	SDP6	SDP7

5.3.5.4. Examples of SDRAM Connections

Here we discuss connections between SDRAM buses and SDRAM. Please note that there are restrictions on addresses assigned to SDRAM areas because of connection configurations. Examples of this are shown below.

A 64Mbit 16bit-width SDRAM is used, and in the following connection configuration using 1 SCS# signal (SCS0#) 32M bytes of SDRAM space is configured.



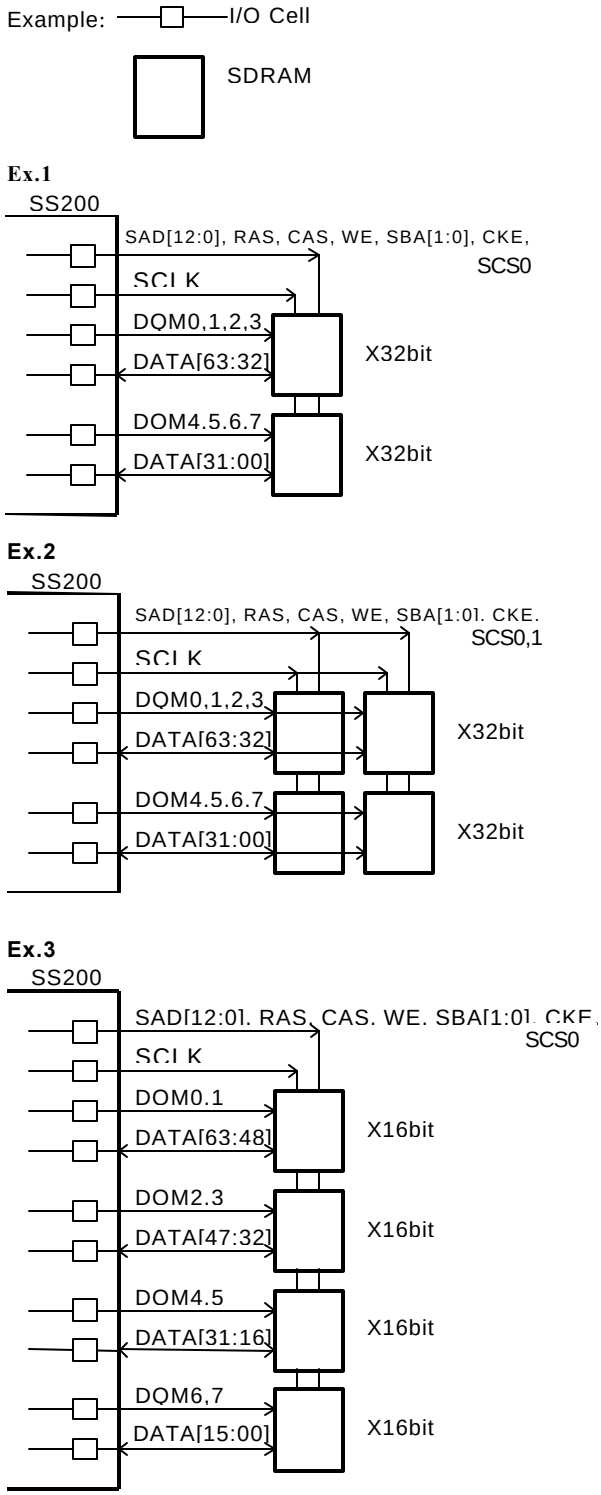
Addresses which can be assigned to the SDRAM spaces in this example are in the ranges shown below.

	Start Address	End Address	Capacity
Area 1	0x0000 0000	0x01FF FFFF	32Mbyte
Area 2	0x0800 0000	0x09FF FFFF	32Mbyte
Area 3	0x1000 0000	0X11FF FFFF	32Mbyte
:	:	:	:
Area n	(32Mbyte X 4) X (n-1)	Start address + 32Mbyte	32Mbyte

All areas are physically assigned to the same SDRAM spaces. Start addresses of the respective areas when used up to all SCS# signals (SCS0#~3#) are multiples of the configured SDRAM spaces. Thus, if in the above example there is a connction configuration which uses 4 SCS# signals (SCS0#~3#), SDRAM area start address is a multiple of 128M bytes because there is a 128M byte (32M byte X 4) SDRAM space configuration. Moreover, end addresses depend on the actual capacity of connected SDRAM, and in the above example they become addresses which add actual SDRAM capacity of 32M bytes to the start address.

The following material shows examples of possible SDRAM connection configurations in the light of the I/O drive capacity restrictions of the SDRAM I/F. In these respective configurations SDRAM area address ranges are shown in accordance with the SDRAM type used, but only Area 1 is described. Please note that address ranges up to areas 2~n which show physically identical spaces also exist.

SDRAM Connection Examples (64-bit Bus Mode)



Example

SDRAM	SCS	Start Address	End Address	Capacity
16Mbit	SCS0	0x0000 0000	0x003F FFFF	4Mbyte
64Mbit	SCS0	0x0000 0000	0x00FF FFFF	16Mbyte
128Mbit	SCS0	0x0000 0000	0x01FF FFFF	32Mbyte
256Mbit	SCS0	0x0000 0000	0x03FF FFFF	64Mbyte

Note: Hatched function are reserved for future expansion.

Example

SDRAM	SCS	Start Address	End Address	Capacity
16Mbit	SCS0	0x0000 0000	0x003F FFFF	8Mbyte
	SCS1	0x0040 0000	0x007F FFFF	
64Mbit	SCS0	0x0000 0000	0x00FF FFFF	32Mbyte
	SCS1	0x0100 0000	0x01FF FFFF	
128Mbit	SCS0	0x0000 0000	0x01FF FFFF	64Mbyte
	SCS1	0x0200 0000	0x03FF FFFF	
256Mbit	SCS0	0x0000 0000	0x03FF FFFF	128Mbyte
	SCS1	0x0400 0000	0x07FF FFFF	

Note: Hatched function are reserved for future expansion.

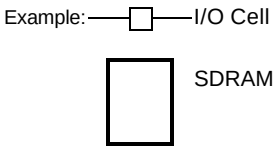
Example

SDRAM	SCS	Start Address	End Address	Capacity
16Mbit	SCS0	0x0000 0000	0x007F FFFF	8Mbyte
64Mbit	SCS0	0x0000 0000	0x01FF FFFF	32Mbyte
128Mbit	SCS0	0x0000 0000	0x03FF FFFF	64Mbyte
256Mbit	SCS0	0x0000 0000	0x07FF FFFF	128Mbyte

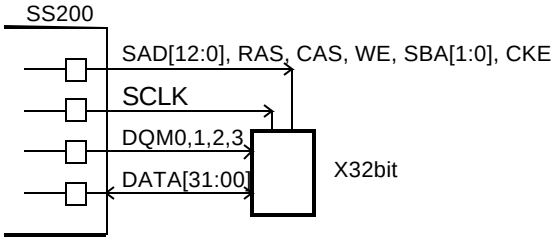
Note: Hatched function are reserved for future expansion.

Figure 5-3 Connect with DRAM Data (64-bit Bus Mode)

SDRAM Connection Examples - 32-bit Bus Mode.



EX.4

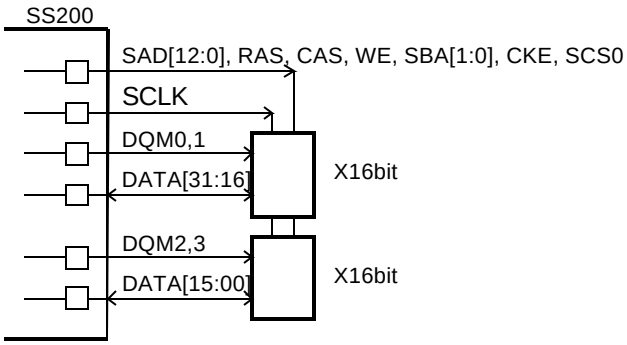


Example

SDRAM	SCS	Start Address	End Address	Capacity
16Mbit	SCS0	0x0000 0000	0x001F FFFF	2Mbyte
64Mbit	SCS0	0x0000 0000	0x007F FFFF	8Mbyte
128Mbit	SCS0	0x0000 0000	0x00FF FFFF	16Mbyte
Example	CS0	0x0000 0000	0x01FF FFFF	32Mbyte

EX.5

SCS0

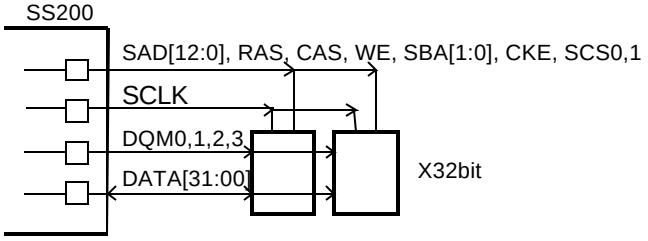


SDRAM	SCS	Start Address	End Address	Capacity
16Mbit	SCS0	0x0000 0000	0x003F FFFF	4Mbyte
64Mbit	SCS0	0x0000 0000	0x00FF FFFF	16Mbyte
128Mbit	SCS0	0x0000 0000	0x01FF FFFF	32Mbyte
256Mbit	SCS0	0x0000 0000	0x03FF FFFF	64Mbyte

EX.6

SCS0,1

Example



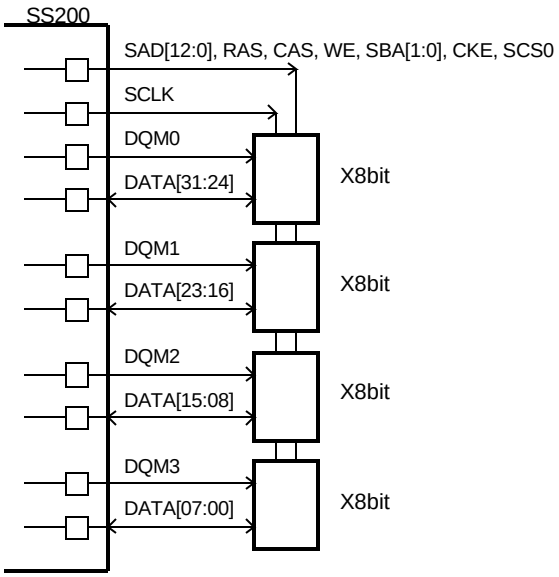
SDRAM	SCS	Start Address	End Address	Capacity
16Mbit	SCS0	0x0000 0000	0x001F FFFF	4Mbyte
	SCS1	0x0020 0000	0x003F FFFF	
64Mbit	SCS0	0x0000 0000	0x007F FFFF	16Mbyte
	SCS1	0x0080 0000	0x00FF FFFF	
128Mbit	SCS0	0x0000 0000	0x00FF FFFF	32Mbyte
	SCS1	0x0100 0000	0x01FF FFFF	
256Mbit	SCS0	0x0000 0000	0x01FF FFFF	64Mbyte
	SCS1	0x0200 0000	0x03FF FFFF	

Figure 5-3 Connect with SDRAM Data (32-bit Bus Mode)

Note: 32bit bus width of SDRAM are reserved for future expansion.

SDRAM Connection Examples - 32-bit Bus Mode - continued.

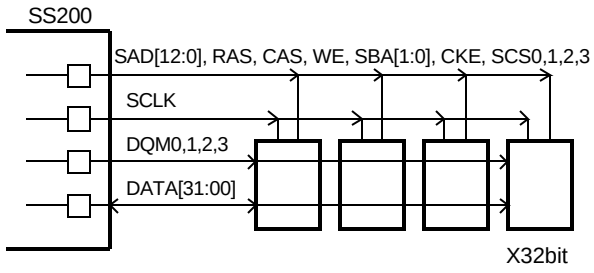
EX.7



Example 7

SDRAM	SCS	Start Address	End Address	Capacity
16Mbit	SCS0	0x0000 0000	0x007F FFFF	8Mbyte
64Mbit	SCS0	0x0000 0000	0x01FF FFFF	32Mbyte
128Mbit	SCS0	0x0000 0000	0x03FF FFFF	64Mbyte
256Mbit	SCS0	0x0000 0000	0x07FF FFFF	128Mbyte

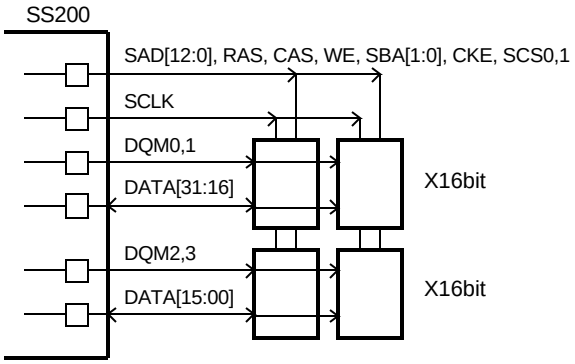
EX.8



Example 8

SDRAM	SCS	Start Address	End Address	Capacity
16Mbit	SCS0	0x0000 0000	0x001F FFFF	8Mbyte
	SCS1	0x0020 0000	0x003F FFFF	
	SCS2	0x0040 0000	0x005F FFFF	
	SCS3	0x0060 0000	0x007F FFFF	
64Mbit	SCS0	0x0000 0000	0x007F FFFF	32Mbyte
	SCS1	0x0080 0000	0x00FF FFFF	
	SCS2	0x0100 0000	0x017F FFFF	
	SCS3	0x0180 0000	0x01FF FFFF	
128Mbit	SCS0	0x0000 0000	0x00FF FFFF	64Mbyte
	SCS1	0x0100 0000	0x01FF FFFF	
	SCS2	0x0200 0000	0x02FF FFFF	
	SCS3	0x0300 0000	0x03FF FFFF	
256Mbit	SCS0	0x0000 0000	0x01FF FFFF	128Mbyte
	SCS1	0x0200 0000	0x03FF FFFF	
	SCS2	0x0400 0000	0x05FF FFFF	
	SCS3	0x0600 0000	0x07FF FFFF	

EX.9



Example 9

SDRAM	SCS	Start Address	End Address	Capacity
16Mbit	SCS0	0x0000 0000	0x003F FFFF	8Mbyte
	SCS1	0x0040 0000	0x007F FFFF	
64Mbit	SCS0	0x0000 0000	0x00FF FFFF	32Mbyte
	SCS1	0x0100 0000	0x01FF FFFF	
128Mbit	SCS0	0x0000 0000	0x01FF FFFF	64Mbyte
	SCS1	0x0200 0000	0x03FF FFFF	
256Mbit	SCS0	0x0000 0000	0x03FF FFFF	128Mbyte
	SCS1	0x0400 0000	0x07FF FFFF	

Figure 5-5 (CONT) Connect with SDRAM Data (32-bit Bus Mode)

Note: 32bit bus width of SDRAM are reserved for future expansion.

SDRAM DIMM Connection Examples (under consideration)

An example of connections using SDRAM DIMM as a technique for achieving large capacity is shown here. SDRAM DIMM which can be connected to the SS200 is limited to products in which PLL logic and register buffers are loaded.

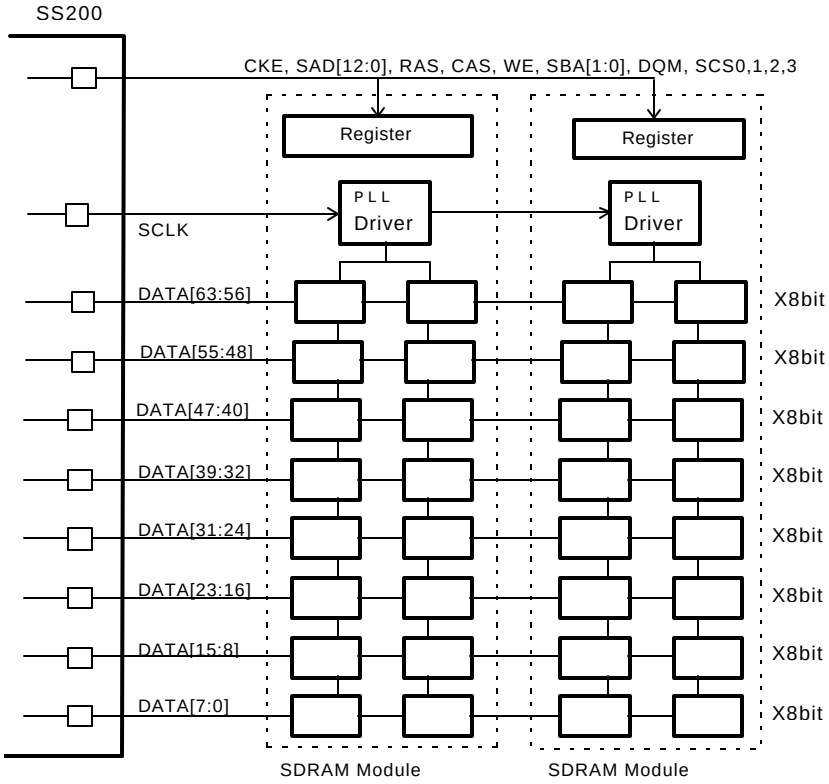
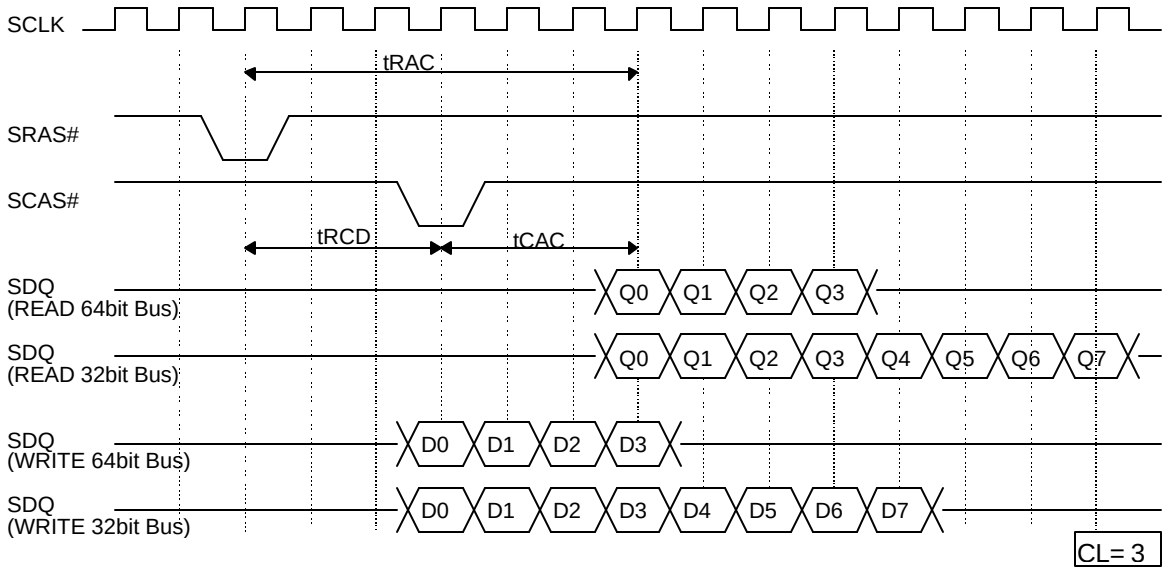


Figure 5-6 Connect with SDRAM DIMM Data

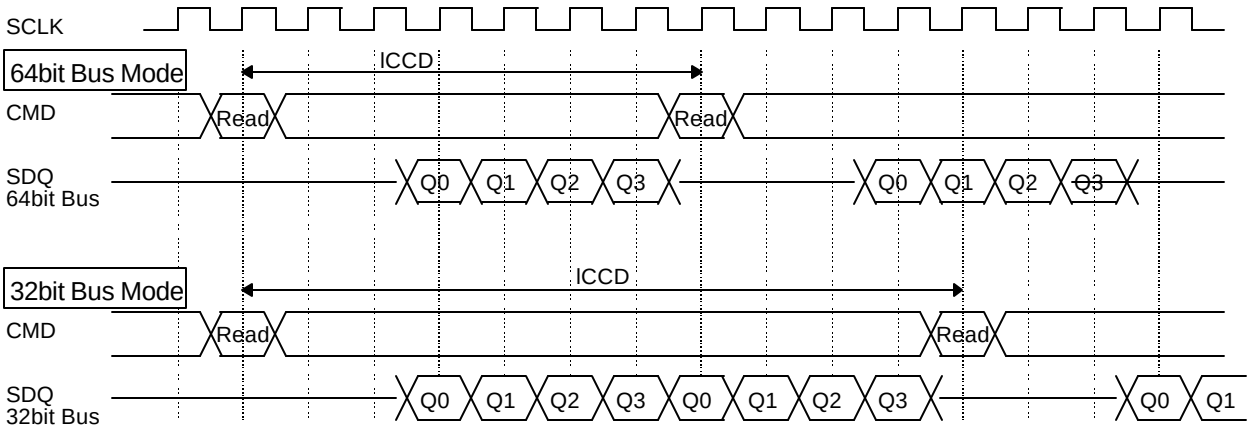
5.3.6. Timing Diagram

5.3.6.1. Access Time



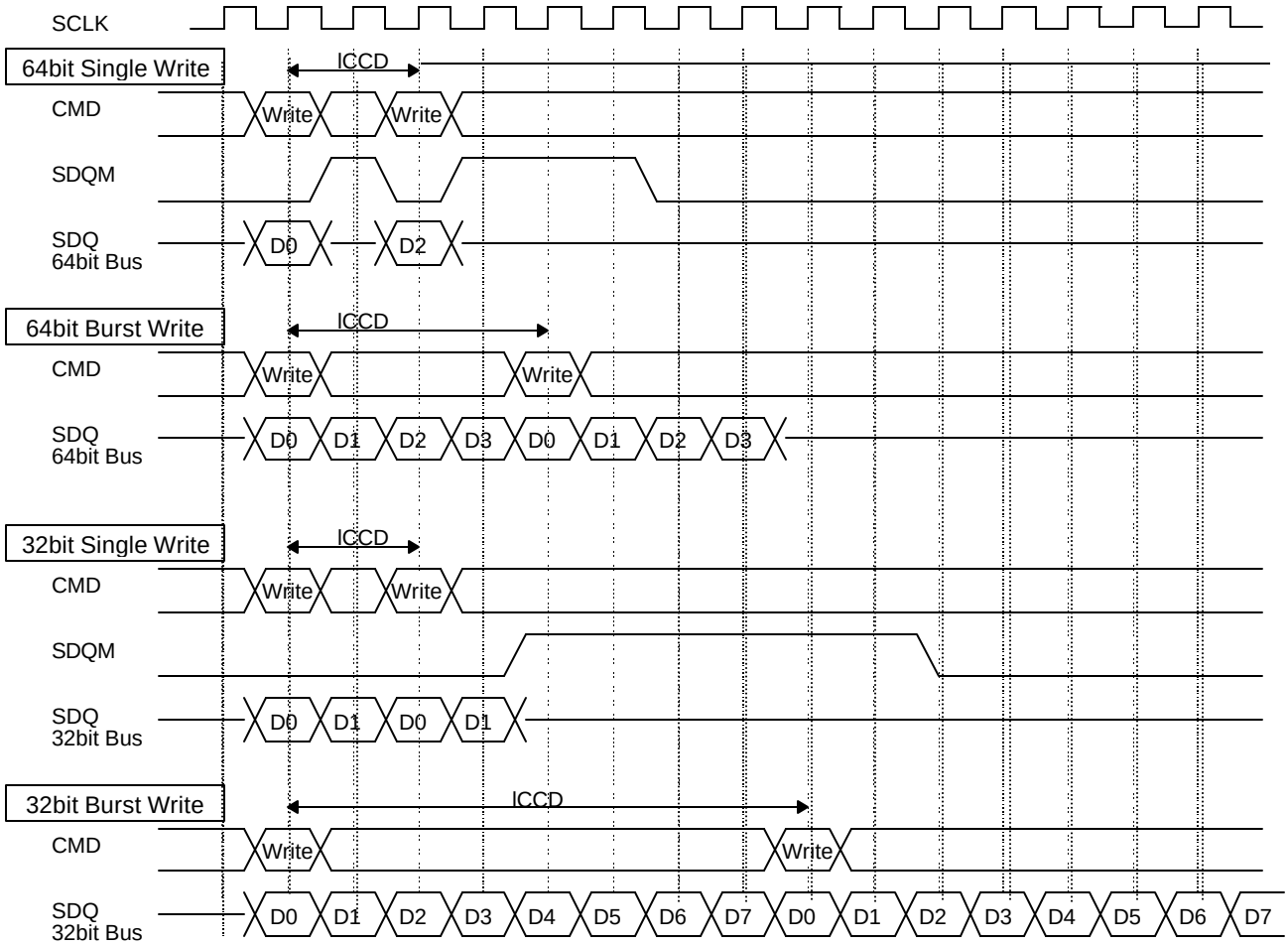
5.3.6.2. CAS Output Spaces

(1) Same Bank Access (Read)

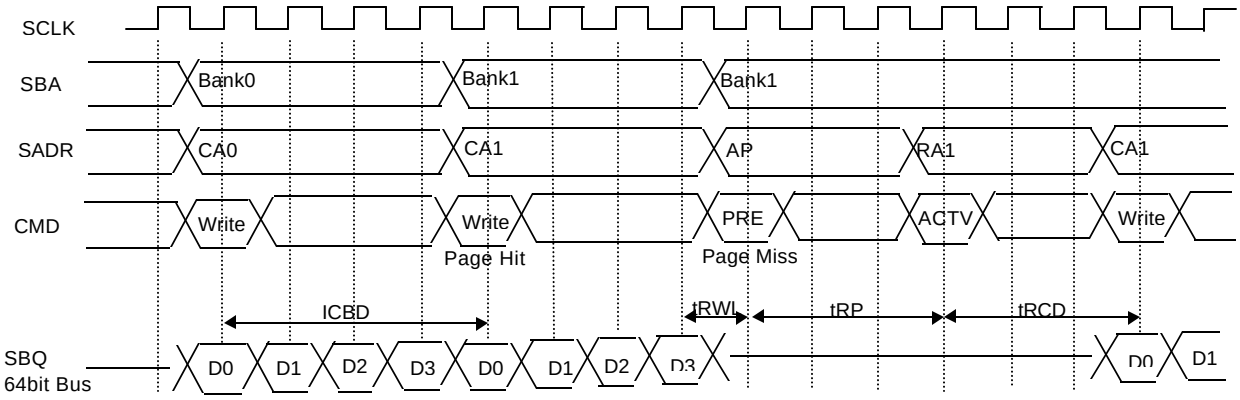


(2) Mask by Same Bank Access (Write) and DQM

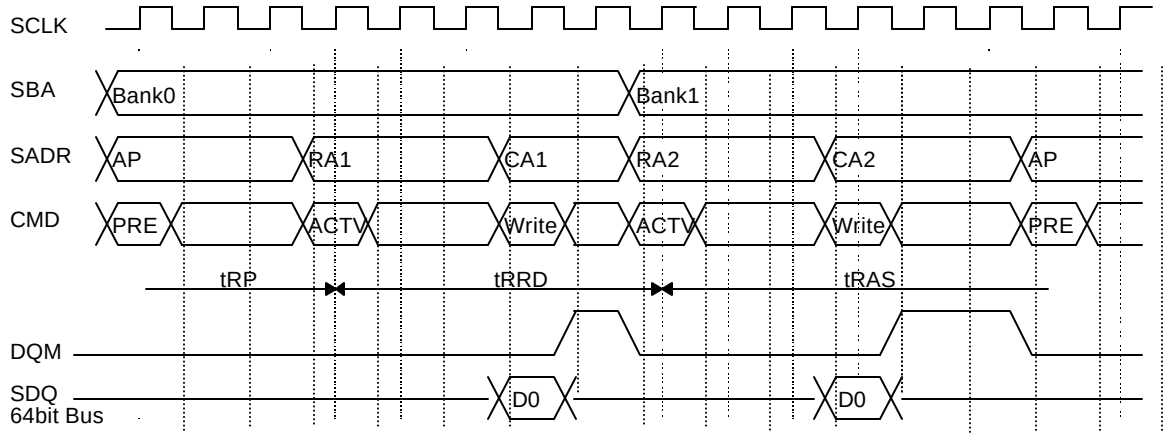
Data mask control by DQM is performed only for data written to SDRAM.



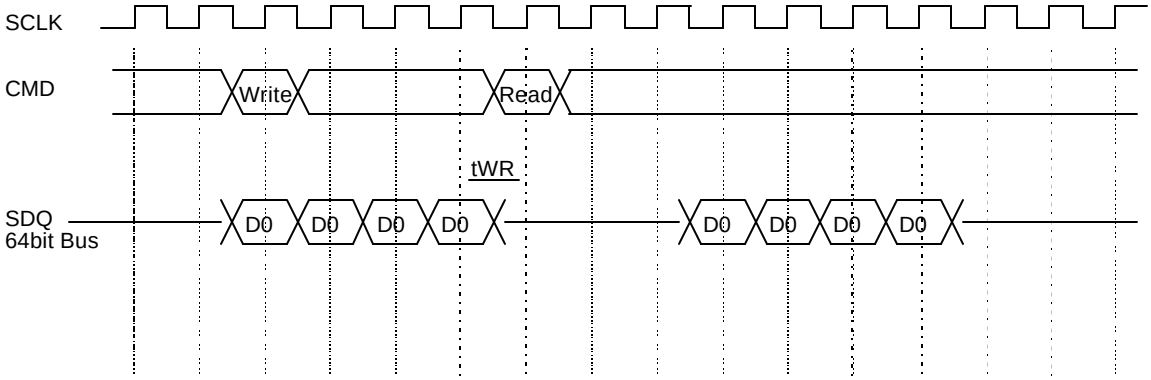
(3) Different Bank Access (Read)



5.3.6.3. RAS Output Spaces



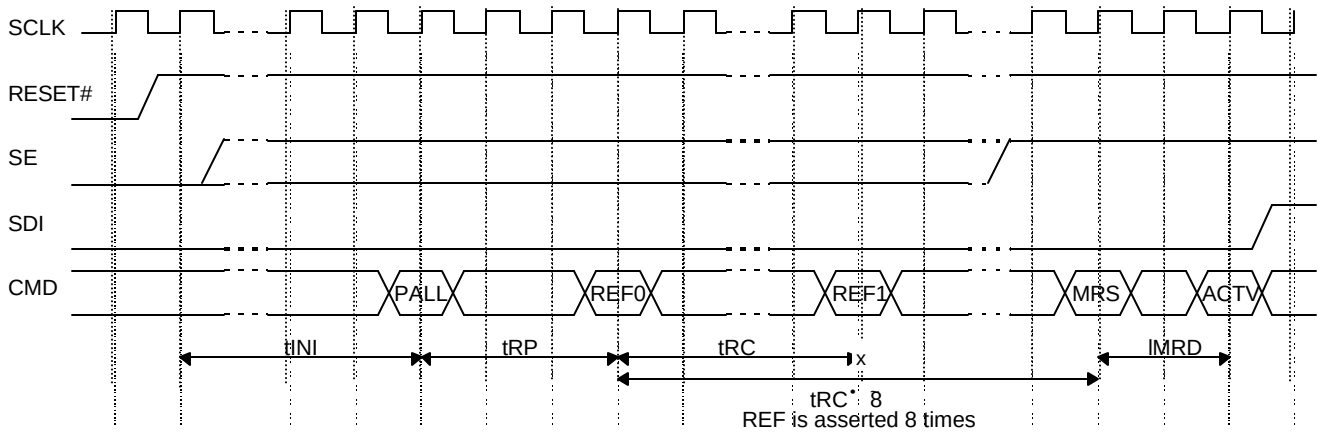
5.3.6.4. Timing from Write to Read



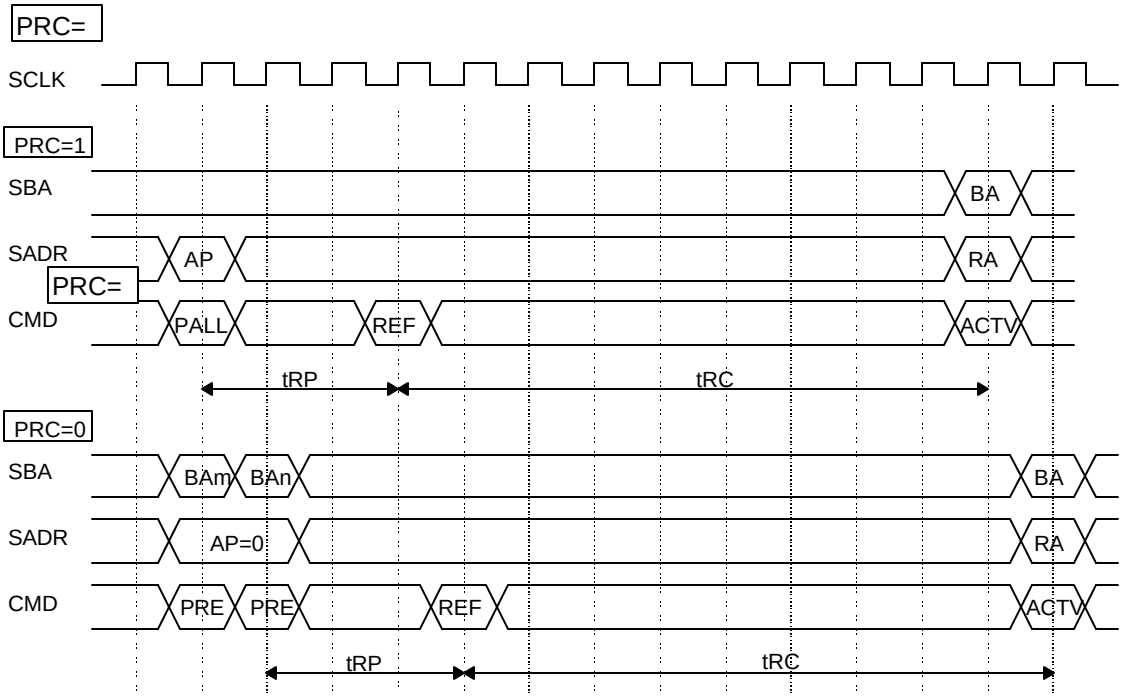
5.3.6.5. Initialization

The SDRAM I/F performs the following operations following cancellation of a RESET signal to the SS200.

(1) Transmits a nop to SDRAM in an interval of 200μs (at 100mhz).
(2) Issues a PALL command to SDRAM and precharges all SDRAM banks.
(3) Issues an auto-refresh command (REF) to SDRAM.
(4) Performs (2)~(3) for all CS.
(5) Recognizes that a write operation to the SDRAM Configuration Register (SDCFG) has been performed and issues a Mode Register Set (MRS) command to SDRAM.
(6) Sets “1” to the SDRAM Initial Wait Indicator (SDI) of the SDRAM Status Register (SSR).



5.3.6.6. Refresh



5.3.6.7. Values Predetermined by Number of SDRAM I/F Cycles

Parameter	Symbol	MIN	unit	notes
RAS# Access Time	tRAC	6	cycle	
RAS#-CAS# Delay Time	tRCD	3	cycle	
CAS# Access Time	tCAC	3	cycle	
CAS# to CAS# Delay	CCD	2	cycle	
CAS# Bank Delay	CBD	2	cycle	
RAS# Cycle Time	tRC	9	cycle	
RAS# Precharge Time	tRP	3	cycle	
RAS# Active Time	tRAS	6	cycle	

Write Recovery Time	tWR	1	cycle	
Last Write to Precharge Lead Time	tRWL	1	cycle	
RAS# -RAS# Bank Active Delay Time	tRRD	5	cycle	
MRS to Active Delay	MRD	2	cycle	
SDRAM Initialization Time	tINI	200	µs	

5.4. SPARClite Interface (SPB)

5.4.1. Functions as the basic interface connecting the SS200 to the SPARClite bus and has dedicated 32-bit address bus and 64-bit data bus pins. Supports Burst Mode and Non-burst Transfer Mode. The SPARClite bus interface operates at input clock frequency.

5.4.1.1. Overview of SPARClite Interface Operations

operation	bus master	cache/ non-cache region	data type	case		access times(burst/non-burst) SPARClite bus width 64bit	32bit	16bit	8bit
read	data buffer	cache	byte half word word double word	BMREQ# assert	BMACK# reply	4 (burst)	8 (burst)	16 (burst)	32 (burst)
					BMACK# not reply	4 (non-burst)	8 (non-burst)	16 (non-burst)	32 (non-burst)
		non-cache	byte	BMREQ# not assert		1 (non-burst)	1 (non-burst)	1 (non-burst)	1 (non-burst)
			half word			1 (non-burst)	1 (non-burst)	1 (non-burst)	2 (non-burst)
			word			1 (non-burst)	1 (non-burst)	2 (non-burst)	4 (non-burst)
			double word			1 (non-burst)	2 (non-burst)	4 (non-burst)	8 (non-burst)
	dmac	non-cache	double word	BMREQ# assert	BMACK# reply	4 (burst)	8 (burst)	16 (burst)	32 (burst)
					BMACK# not reply	4 (non-burst)	8 (non-burst)	16 (non-burst)	32 (non-burst)
write	data buffer	cache	double word+BE# *1	BMREQ# not assert		1 (non-burst)	2 (non-burst)	4 (non-burst)	8 (non-burst)
		non-cache	byte	BMREQ# not assert		1 (non-burst)	1 (non-burst)	1 (non-burst)	1 (non-burst)
			half word			1 (non-burst)	1 (non-burst)	1 (non-burst)	2 (non-burst)
			word			1 (non-burst)	1 (non-burst)	2 (non-burst)	4 (non-burst)
			double word			1 (non-burst)	2 (non-burst)	4 (non-burst)	8 (non-burst)
	dmac	non-cache	double word	BMREQ# assert	BMACK# reply	4 (burst)	8 (burst)	16 (burst)	32 (burst)
					BMACK# not reply	4 (non-burst)	8 (non-burst)	16 (non-burst)	32 (non-burst)

*1 Data merge and collapse happens. Therefore the data type cannot be decided

5.4.1.2. Burst Mode/Non-burst Mode

- Read operations by Cache area reads and DMAC are basically processed as burst transfers. Thus, if BMREQ# is asserted at the same time as AS# and BMACK# is returned in READY# timing for the initial access, a burst transfer corresponding to the bus width is performed in Burst Mode. If BMACK# is not returned, a number of non-burst transfers which corresponds to the bus width is performed.
- In Burst Mode AS# is only asserted once, but the address changes sequentially every time READY# is returned, and the address pin indicates the access destination address.
- (1) Write operations to cache areas, (2) Atomic Load/Store operations and (3) Reads other than ASI=8,9,a,b are handled as non-burst, and BMREQ# is therefore not asserted.
- Since caches perform data valid/invalid control in double word units, the data read unit from cache areas is double words regardless of the data type requested by the CPU. In a 64-bit bus, burst length is 4. BMREQ# is then output, and if BMACK# is returned together with READY#, burst mode materializes, and burst transfers of the lengths shown in the above table are performed. If BMACK# is not returned, burst transfers do not take place, and the required number of single transfers as shown in the above table is performed. Burst length is 8 in 32-bit bus, 16 in 16-bit bus and 32 in 8-bit bus. When burst transfers do not take place, the required number of single transfers is performed as shown in the above table.

- Cache Area Write Operations
  Write operations to cache areas are processed by single transfers in double word units.
- DMAC Write Operations
  DMAC write operations are performed in 4 X double word burst transfers. (when BMACK# responds to BMREQ#). If BMACK# does not respond, 4 double word single transfers are performed..
- Writes outside of cache areas and other than DMAC
  The required number of single transfers is performed as shown in the above table.

5.4.1.3. SPARClite Bus Width

- SPARClite Bus Width is set for each CS#.
  - CS0# Area Bus Width
    CS0# is assigned to ROM space. CS0# area bus width is set by the BMODE16# and BMODE32# pins as shown below. BMODE16# and BMODE32# values are sampled during reset periods.

5.4.1.4. Table 5.9 SPARClite Bus Width

BMODE16#	BMODE32#	CS0# Area Bus Width
0	0	8bit
0	1	16bit
1	0	32bit
1	1	64bit

  - CS1#~CS5# Area Bus Width

CS1#~CS5# Area bus Width is set by registers.
[See explanations of ARSR(Reg.) and AMR(Reg.)]

5.4.1.5. Idle Cycles between Accesses

- Idle cycles between accesses are set by settings in the IDCCR (Reg.).
- When IDCCR (Reg,) bit0 is 0 and a write operation continues following a read operation, an idle cycle of 1 external clock is guaranteed from when the read operation READY# is returned to when the write operation AS# is output.
- When IDCCR (Reg.) bit0 is 1, the space (idle cycle) from READY# for the CS0# read operation to the next access (regardless of CS0# and read/write) is guaranteed to be the number of external clocks set to IDCCR (Reg.) bit3~bit1.

Table 5-10 Idle Cycle Settings

IDCCR[3:1]	No. of Idle Cycles
3'b000	1
3'b001	2
3'b010	3
3'b011	4
3'b100	5
3'b101	6
3'b110	7
3'b111	8

5.4.1.6. Internal READY Generator Function

Has the function of internally generating READY# in timing which differs from CS# to CS# in accordance with register settings. [See the explanation of the WSPR (Reg.)]

5.4.1.7. Bus Grant Timing (BREQ# and BGRNT#)

- Reads from Cache Areas (burst)
  Release bus after burst transfers end.
- Reads from Cache Areas (non-burst : BMACK# does not return)
  Release bus after required number of single transfers.
- Reads from Non-cache Areas (except ASI=8,9,a,b)
  Release bus after required number of single transfers.
- Atomic Load/Store
  The CPU does not release external buses between Load and Store instructions of Atomic Load/Store instructions. The CPU release a bus after a store operation (in response to an Atomic Load/Store instruction) ends. Also, LOCK# signals are asserted during this period.

5.4.1.8. Memory Exceptions

- Even though a MEXC may occur during a data transfer, the data transfer continues without pause.

MEXC# during reads

- Cache Areas
  Data read operations to cache areas are performed by burst transfer. If a MEXC occurs during a burst transfer and that MEXC occurs for the first double word data of the burst transfer (data requested by the CPU -double word, word, half word, byte- will definitely be included in the first double word access), 1 is set as a flag to bit2 of the MXPEF (Reg.). The CPU then generates a trap as an instruction access exception or a data access exception when the burst transfer ends. MEXC occurring for the 2nd, 3rd and so forth double word data are neither transmitted to the CPU nor stored in buffers, nor do they generate traps. However, 1 is set as a flag to bit2 of the MXPEF (Reg.). Also, users can verify that MEXC have occurred for read operations from the CPU or read operations from the DMAC by verifying the MXPEF (Reg.) with a trap routine.
- In 32-bit, 16-bit and 8-bit Buses
  MEXC# is handled in double word units for cache areas, and for other than cache areas in data type units (double word, word, half word, byte) requested by the CPU. Thus, when a word data read is performed for 8-bit bus width, access is performed 4 times, and if for the 1st to the 4th access MEXC# is returned together with READY# for at least one of those accesses the CPU is notified that MEXC# has occurred for that word data and a trap occurs.
- During DMA Transfers (reads from SPARClite Bus)
  When MEXC# occurs in the middle of a data read operation from a SPARClite bus while using the DMAC, 1 is set as a flag to bit5 of the MXPEF (Reg.). A flag is also set to the ERR bit (bit7) of the MCR (Reg.). See the item regarding DMAC Exception Processing Errors.

MEXC# during Writes

If MEXC# occur during writes, 1 is set as a flag to bit1 of the MXPEF (Reg.) for writes from the CPU and to bit5 of the MXPEF (Reg.) for writes from the DMAC. Write MEXC# are not transmitted to the CPU at the point in time at which they occur. If 1 is set to bit0 of the MXPECR (Reg.), this is transmitted to the CPU as a MEXC during the next read access from the CPU, and a trap occurs. If 0 (0 after Reset cancel) is set to bit0 of the MXPECR (Reg.), MEXC is not transmitted to the CPU and no trap occurs. Accordingly, in this case the external circuits inform the CPU of irregularities by means of interrupts. Users can verify that MEXC has occurred for a write operation preceding a read operation by verifying the MXPEF (Reg.) with a trap routine.

5.4.1.9. Parity

- Performs a Parity Check for access to the corresponding CS# areas if 1 is set to bit0 of the WSPR (Reg.).
- 0: Even Parity and 1: Odd Parity respectiveley depend on the value of bit1 of the MXPECR.
- Bus Width and DP Pins Used

Bus Width and the corresponding DP Signal bits are as shown below

Table 5-11 Bus Width and DP Pins Used

SP-bus	DATA							
width	<63:56>	<55:48>	<47:40>	<39:32>	<31:24>	<23:16>	<15:8>	<7:0>
64bit	DP0	DP1	DP2	DP3	DP4	DP5	DP6	DP7
32bit					DP4	DP5	DP6	DP7
16bit							DP6	DP7
8bit								----

- Data Reads
  If 1 is set to bit0 of the WSPR (Reg.), a Parity Check is performed, and if a Parity Error occurs, 1 is set as a flag to bit0 of the MXPEF. It is also transmited to the CPU as MEXC. Users can verify that a Parity Error has occured during a read by verifying bit0 of the MXPEF (Reg.) with a trap routine.
- Data Writes
  If 1 is set to bit0 of the WSPR (Reg.), data supporting the Parity information is output at the same time to the DP pins during data writes.

5.4.1.10. SPARClite Bus Width and BE0#~7#

Shows data locations indicated by SPARClite Bus Width and BE0#~BE7#.

Table 6-10 Bus Width and BE0#-7#

SP-bus	DATA							
width	BE0#	BE1#	BE2#	BE3#	BE4#	BE5#	BE6#	BE7#
64bit	D<63:56>	D<55:48>	D<47:40>	DE<39:32>	D<31:24>	D<23:16>	D<15:8>	D<7:0>
32bit	----------	----------	----------	----------	D<31:24>	D<23:16>	D<15:8>	D<7:0>
16bit	----------	----------	----------	----------	*1 ADR<1>	*1 ADR<0>	D<15:8>	D<7:0>
8bit	----------	----------	----------	----------	*1 ADR<1>	*1 ADR<0>	----------	D<7:0>

- During reads from cache areas and DMAC read operations, BE0#~7# are all asserted.
- Only BE is asserted to valid bytes during read operations other than the above.
- Only BE is asserted to valid bytes during writes.
- The above support is the same in both Big-Endian and Little-Endian operations.

NOTE *1： In 16-bit and 8-bit Bus Width ADR<1:0> is output to BE4# and BE5#.

5.4.2. SPARClite Bus Operations

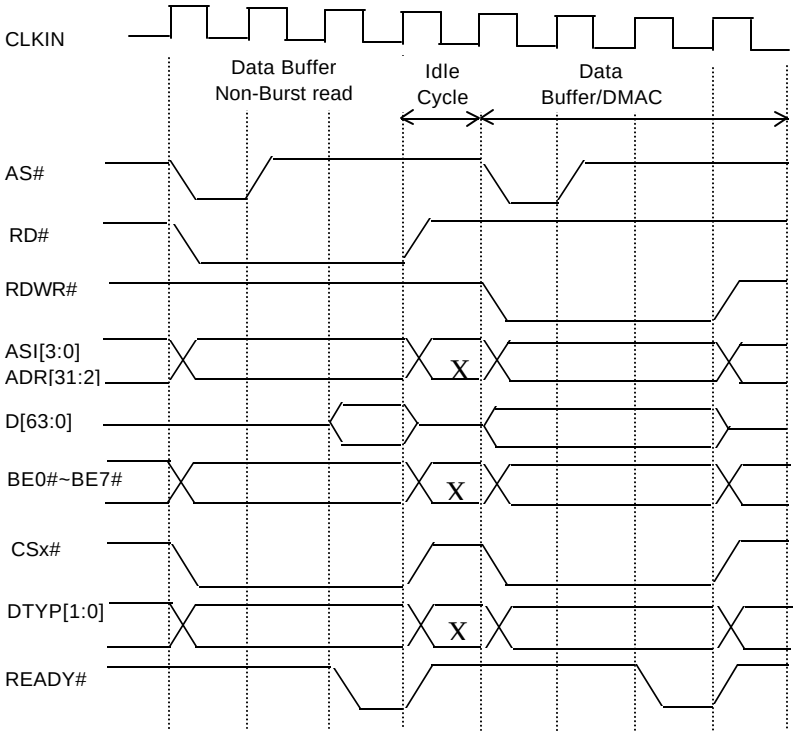


Figure 5-1 SPARClite Non-Burst Read/Write Operations

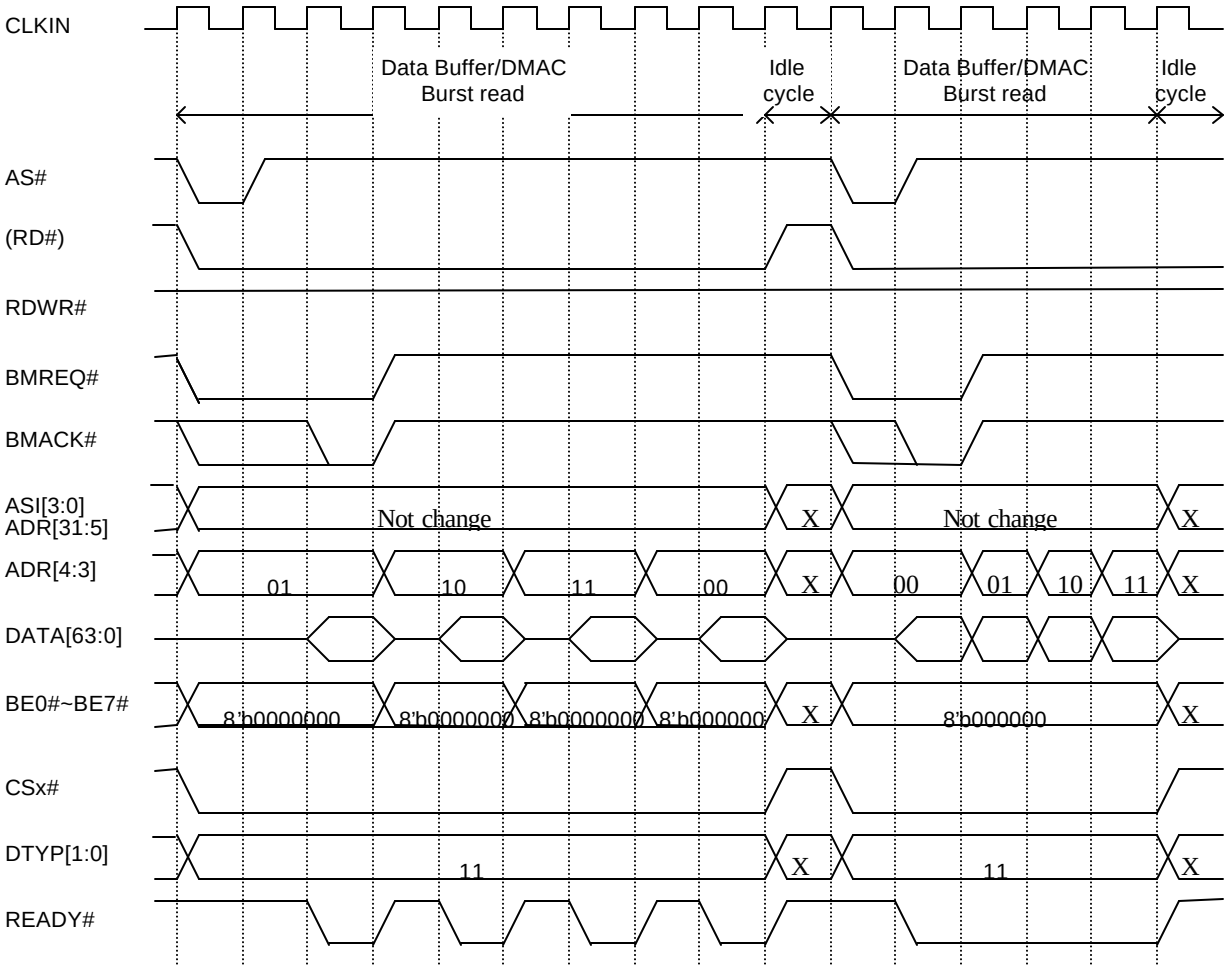


Figure 5-2 SPARClite Bus Burst Read Operation

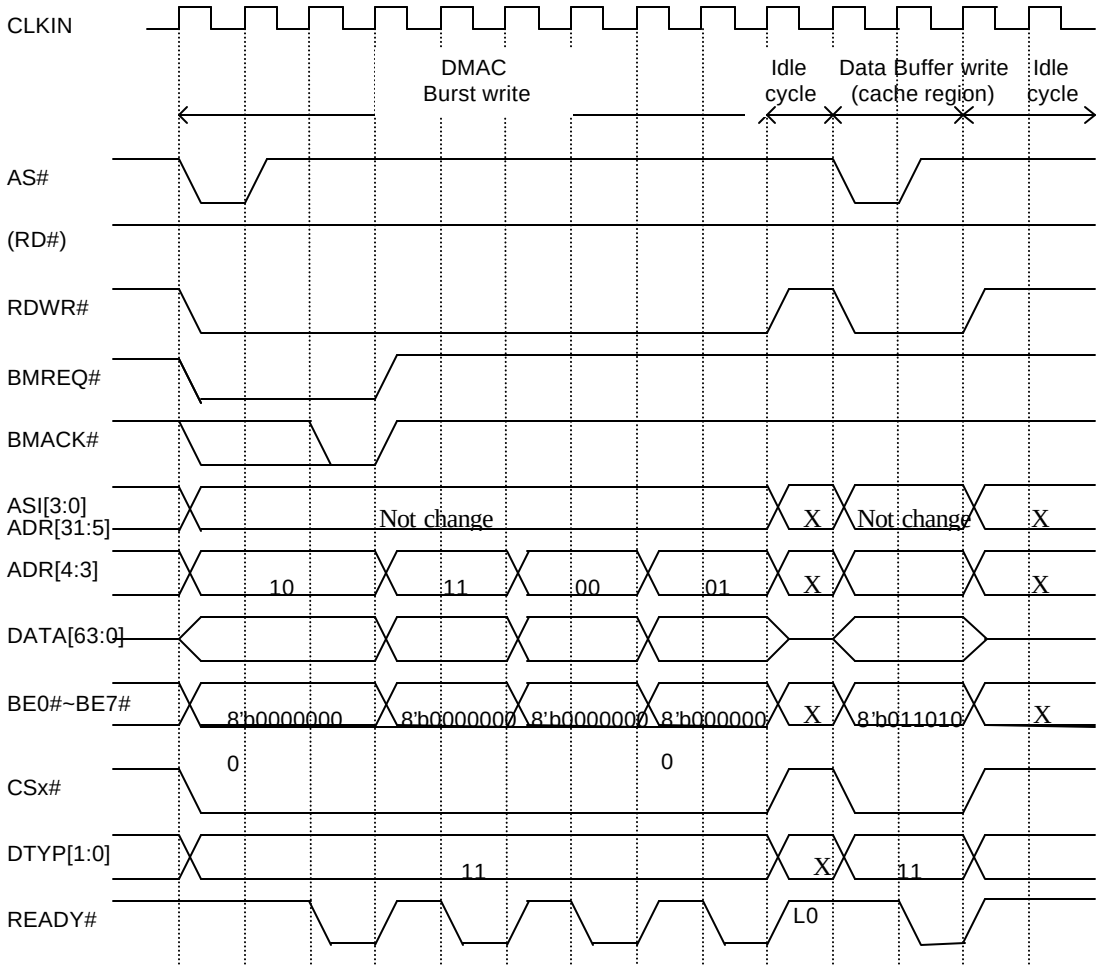


Figure 5-3 SPARClite Bus Burst WRITE Operation (DMA transfer)

5.5. SS200 Bus-bridge DMAC

5.5.1. Summary

- The DMAC supports flow-through transfers between SPARClite buses (SPB) and SDRAM buses. Each set register has 2 channels. Simultaneous operation is only 1 channel.

- Flow-through Transfers
  SDRAM–bus <> SPARC–bus
  SDRAM–bus <> SDRAM–bus
  SPARC–bus <> SPARC–bus

- Burst Transfer Support
- Transfer Number Burst Unit (32 bytes) / set maximum 64k times (2 Mbyte)

5.5.1.1. Internal Bus Priority Order

The DMAC is connected to the chip internal BIU bus. The CPU core has BIU bus right priority. DMA transfers are activated by setting activation bits SB of the DMA Control Registers (DMCR0, 1) to 1. When CPU Core access requests occur during DMA operations, DMA opens a bus right in burst transfer units, and the CPU continues operating after the bus right is opened.

5.5.1.2. Transfer Systems

The DMAC has a 64-bit 4-column FIFO and makes burst transfers of transfer length 4 (bus width 8 bytes X 4 times = 32 bytes) the basic bus cycle. It reads 4 consecutive burst transfer data from memory spaces which indicate source addresses and outputs 4 consecutive data in burst transfers to memory spaces indicating destination addresses. The basic unit for transfer number settings, bus arbitration, error processing and the like is also 32 bytes. DMA transfers basically assume non-cache space access. Since the SS200 does not support snoop functions, cache area DMA transfers should not be performed. Memory coherency is not guaranteed during transfers.

5.5.1.3. Register Summary

Selection of respective buses for source and destination spaces, I/O area selection and CS area selection are set in the MCR Register. I/O areas and CS areas are valid only when bus selection is specified to the SPB. CS area settings must be set to agree with ARSR and AMR Register settings. Addresses are not updated when set to I/O areas.
Source and destination addresses are set respectively in the DMSAR and DMDAR registers. Address settings are in 32-byte units. ASI is specified by the 4 lower order register bits. Transfer numbers are set in the DMWL Register. Transfer numbers are set in units of 32 bytes (1 burst) to the lower order 16 bits (WL) of the register. WL indicates a 1-burst (32 bytes) transfer when 1, and transfers are possible up to a maximum of 64k bursts (2 Mbyte) at 0xf f f f. The upper order 16 bits (L WL) of the DME WL indicate the remaining number of transfers during DMA transfers or when an exception occurs.

5.5.1.4. Activation / Termination

2 Channels can be set independently for each set DMA register. DMA activates when the start bits of all MCR Register channels are set. Then, after the number of transfers set to the Transfer Number Register has been executed, it automatically clears the the Control Register start bit and stops. DMA transfers operate simultaneously in either channel in 1 direction only. If a start bit is set in the other direction while a channel is activated in 1 direction, continuous transfers are started in the other direction after the set number of transfers in the first direction is completed. EOP is output upon completion of the transfers. Whether or not to output it can be specified by register settings.

5.5.1.5 Exception Processing

- **Aborts**

If the activation bit of the MCR Register is cleared (1—> 0) during DMA transfer, DMA transfers in that channel are aborted. Abort timing is timing in which an MCR Register clear write cycle is inserted at a break in the burst unit bus.

After a stop because of an abort, the MCR abort bit (bit6) is set, but EOP is not output.

- When the activation bit of a channel in the other direction is set, the channel in the first direction stops and a transfer is automatically started. After the channel in the first direction has been aborted, in order not to activate a channel in the other direction whose activation bit has been set, it is necessary to clear the activation bits of both channels. Abort bits should be cleared by an MCR write.

- **Errors**

- If a MEXC or parity error is detected during a source data read, the DMA stops writing to destination address spaces, and the MCR activation bit (bit0) clears both channels and stops. Also during the stop EOP is output and the ERR bit (bit7) of the MCR is set. The ERR bit is not cleared by an MCR write. It is automatically cleared when both channels are activated.

5.5.2. Block Diagram

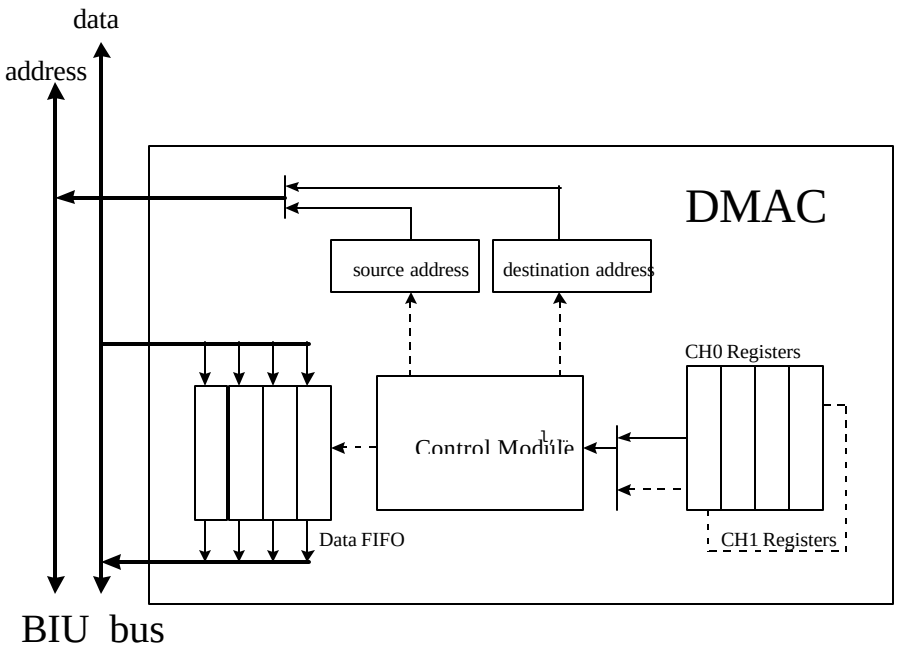


Figure 5-8 SS200 DMA Block Diagram

5.6. Operating Frequencies

The SS200 has an internal clock frequency multiplier circuit which operates at 2X, 3X and 4X the external input clock. The following shows examples of mode settings, input clocks and internal operating frequencies (maximum).

Table 5-17 Operational Frequency

Multiple Mode	External Clock	SPARClite Bus	SDRAM Bus	SS200 Core
x2	50MHz	50MHz	100MHz	200MHz
x3	33MHz	33MHz	100MHz	200MHz
x4	25MHz	25MHz	100MHz	200MHz

6. Debug Support Unit (DSU)

6.1. DSU Features

- The 3 Types of Debug Trap Conditions
  Items which depend on external input (DBREAK#) (asynchronous)
  — Internal hardware break points (instruction address conveyors, single step mode)
  — Software break points (**TA255**)
- Debug Mode by sampling when resetting the BRKEN# pin
- Debug Support Registers
  2 instruction • address • descriptor • registers (IADR1, IADR2)
  — Debug • control • registers (DCR)
  — Debug • status • registers (DSR)
- SPARClite and Program Models are identical
  Debug • Support Register addresses are the same as SPARClite
  — All SPARClite DSR and DCR bits are not implemented, but those which are implemented are the same.
- Debugging is possible only in Supervisor Mode.
- Debug Trap Features
  — All debug trap types are 255, and TBA is ignored.
  >Debug traps always start at address 0x00000ff0.
  — Debug trap priority is 2 (highest rank except for reset)
  — Debug traps are not masked by PSR ET=0.
  — Flags exclusively for new debug routines (pET, pPS)
- ROM (or FLASH ROM) for debug trap routines can be selected by external pin (BRKGO) which indicates debug status.
- The Debug Support Unit stops operating in Normal Mode to reduce power consumption.
- The PC trace function has a 16-column buffer, and it saves instruction addresses from the program counter.

6.2. DSU Functions

6.2.1. Move to Debug Mode

The CPU has 2 statuses: Debug Mode and Normal Mode. The EN_BRK_ bit of the DSR Register indicates the current mode.

EN_BRK_ = 0 . . . Debug Mode
EN_BRK_ = 1 . . . Normal Mode

The mode is decided by BRKEN# pin status when a reset signal is canceled. Values at this time are stored in the EN_BRK_ pin and cannot be rewritten by the software until the next reset. In Normal Mode all breaks are disabled and debug traps are not activated. In addition, the DSU stops functioning in order to reduce power consumption.

Upon reset, if the DBREAK# and BRKEN# pins are asserted simultaneously, instead of fetching instructions from CPU0 addresses they jump immediately to a debug trap routine (0x00000FF0). In this way the boot ROM can be replaced by a debug monitor. By using the SWF bit (in the DCR Register), the software can decide whether or not that debug trap routine was activated immediately following a reset. Since the SWF bit is “0” immediately following a reset, if “1” is written at that time, and this bit is read when the next debug routine is activated, it becomes clear that the routine was not activated immediately following a reset if that bit is “1”.

6.2.2. Debug Trap Activation

There are 3 ways of activating debug traps:

1. Activation by External Break Pins
   The EB bit of the DSR Register is set by DREAK# fall input, and an asynchronous debug trap activates. This input is ignored between Normal Mode and debug trap routines.

2. Activation by Internal Hardware Breaks
   These break points are handled as synchronous traps. The following 2 conditions obtain for activating these traps:

   A. The PC address matches IADR1/2, the PSR user/supervisor bits match the US1/2 bits (DSR Register) which correspond to IADR, and the EIA1/2 bits of the DSR Register which correspond to these are set. Accordingly, the EIA bit of the DCR Register, the IADR Register and the US bits must be set beforehand in order to activate these break points. Instruction address breaks are before-type break points. Thus debug traps occur before instructions with matching addresses are executed.

   B. When the SSE bit of the DCR Register is set to "1", the CPU is in Single Step Mode, and debug traps occur following execution of each instruction without regard to PC or IADR values (there are several exceptions such as RETT, WRPSR etc.). To activate this mode, the SSE bit of the DCR Register must be set.

3. Software Breaks
   The TA255 instruction (Trap always with tt=255) is a software debug trap instruction. This instruction activates debug traps when the EN_BRK_ bit of the DSR Register is "0".

6.2.3. Debug Trap Features

- Debug trap priority is 2. It takes the highest priority when a reset is deleted.
- All debug traps are trap type tt=225, and the trap address is 0x00000FF0. Trap base addresses (TBA) are ignored.
- When the TDBP bit of the DCR Register is "1", debug traps occur even during traps (ET=0).
- When the TDBP bit of the DCR Register is "0", ET=0 and hardware breaks and external breaks are ignored. Software breaks (TA255) are activated even when ET=0.
- Debug traps are activated only in Supervisor Mode.
- Debug traps cannot be nested. Debug traps cannot again be activated during a debug trap. When the BG bit of the DCR Register is "1", break conditions other than TA255 are ignored, and traps are not activated. Software breaks (TA255) during debug traps are abnormal, and the results are unpredictable. Try not to use TA255 instructions in debug trap routines.
- When debug trap routines are entered, condition codes (PSR CC fields) are not automatically saved by the hardware. When the possibility exists that a debug trap routine may rewrite these, they must be saved and restored by the softeware.

6.2.4. Debug Trap Operations

In addition to ordinary trap operations, the following operations are activated in debug traps:

- ET –> pET . . . ET bit saved to pET
- PS –> pPS . . . PS bit returned to pPS
- 1 –> DCR.BG . . . DCR Register bit is "1"
- 255 –> TBR.tt . . . (TBR tt field set to 255 only in software debug traps. tt fields are not rewritten by software breaks and external breaks.

When there is again a return from a debug trap (JMPL+RETT is executed when DCR.BG is "1"), the next operation is performed.

- 0 –> DCR.BG . . . DCR Register BG bit is "0"
- pPS –> PS . . . pPS bit returned to PS
- pET –> ET . . . pET bit returned to ET

pPS and pET are new bits for debug traps. They are assigned to bits 9 and 8 of the DSR Register.

6.2.5. BRKGO Output Pin

The MB86860 has a BRKGO output pin. This always reflects the DCR Register BG bit. When this bit is "1", it indicates that instruction fetches and data access are for debug trap routines. This pin can be used for debug trap routines in

ROM chip select. Instructions and data indicated by BRKGO are not cached.

6.2.6. Register Files

Handling of debug trap register files is the same as for ordinary traps, and CWP is decremented. Handling of debug trap routine register files is left entirely to the software.

6.2.7. PC Trace Features

PC trace information is stored in 16-column cyclic registers mapped in the one ASI=0x01 memory space. In Debug Mode, as instructions are fetched their addresses are stored in this register until a break is activated. If the trace register is full before a break is activated, the new address is written over the oldest register (cyclic operation).

Break trap routines can read those registers in which ASI=0x01 addresses 0x0000FF40~0x0000FF7C are mapped. The TBPTR Field of the DSR Register holds the register addresses which are the PC addresses stored last. The newest register addresses can be obtained by shifting the TBPTR field to bits 5~2 and doing 0x0FF40 and OR. For example, if TBPTR is 5 and it is shifted, it becomes 0x14, and if 0x0FF40 and OR is done, 0xFF54 is obtained. The nearest traces are stored in this register, and under it Reg4, Reg3, . . .Reg0, Reg15, Reg 14, . . . becomes effective.

7. Bi-endian Function

The SS200 uses the load/store instruction to select access data byte address endian- Big endian or Little endian. Endian is specified by the DE (Default Endian) bit of the SS200 Core PSR Register. “0” indicates big endian and “1” indicates little endian. After a reset, big endian (DE : 0) is effective. Bi-endian specification is valid only for data access. Please note that instruction fetches are fixed to big endian and have no relation to DE bit settings. In the SS200, internal registers mapped in memory spaces should be accessed as word data. During word access, register address bit positions in these specifications are guaranteed without regard to DE bit settings.

When changes are made to little endian after a reset, the DE bit must be set before executing load/store instructions. Also, for DE bit changes, set data caches while off, or flush data cache contents after setting. The following indicates the correspondences between data and addresses specified by load/store instructions of each access type.

		bit63←			64bit bus				→bit0
Addresses in case of Big Endian	=>	0	1	2	3	4	5	6	7
	00	a	b	c	d	e	f	g	h
Addresses in case of Little Endian	=>	7	6	5	4	3	2	1	0

Figure 7-1

1. Byte Access (ldub,ldsb,stb)

Table 7-1

Instruction	Address	little	BIG
ldb	0	h	a
	1	g	b
	2	f	c
	3	e	d
	4	d	e
	5	c	f
	6	b	g
	7	a	h

2. Half word Access (iduh,ldsh,sth)

Table 7-2

Instruction	Address	little	BIG
ldh	0	gh	ab
	2	ef	cd
	4	cd	ef
	6	ab	gh

3. Word Access (ld, st)

Table 7-3

Instruction	Address	little	BIG
ld	0	efgh	abcd
	4	abcd	efgh

4. Double word Access (ldd, std)

Table 7-4

Instruction	Address	little	BIG
ldd	0	abcdefgh	abcdefgh

8. Low Power Consumption Mode

The SS200 has 2 modes for low power consumption- Sleep Mode and Stop Mode. Sleep Mode stops the clocks provided by Core and peripheral functions while the PLL is operating. Continuous normal operation is possible after Sleep Mode cancellation. Stop Mode stops the PLL, and all internal clocks stop. A reset must be input in order to restart. Caches must be in OFF status when converting to low power consumption mode. Relationships between all modes when in Cache OFF Mode and caches in OFF status and operations in Normal Mode which use caches are shown below.

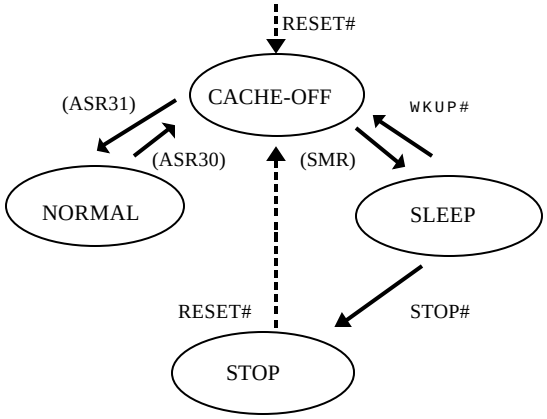


Figure 8-1 Power Save State Diagram

1. CACHE-OFF
   - Converts to this Mode after reset
   - Sensamp also stops in cache OFF
   - Converts to Normal Mode by setting ICCR Register
   - Converts to SLEEP Mode by setting Sleep Mode Register

2. NORMAL Mode
   - Conversion only possible from CACHE-OFF Mode
   - Converts to CACHE-OFF Mode by setting ICCR Register

3. SLEEP Mode
   - Conversion only possible froim CACHE-OFF Mode.
   - Except for PLL, clocks stop.
   - PDOWN Pin is asserted during Sleep Mode period.
   - During Sleep Mode conversion the SDRAM I/F issues a self-refresh command to SDRAM.
   - SPARClite bus right open.
   - Returns to CACHE-OFF Mode if WKUP# Pin is asserted.
   - Converts to STOP Mode if STOP# Pin is asserted.

4. STOP Mode
   - Conversion only possible from SLEEP Mode.
   - Stops PLL and all internal clocks.
   - Restart only possible by reset.

   #When converting from CACHE-OFF Mode to NORMAL Mode, a cache flush (access to ASI0X31space) before the ICCR Register settings is required.

9. APPENDIX A [SPARClite Instruction Sets and CPI]

Name		Operation		MB8686X[1]	SPARClite[4] MB8683X
Load and Store Instructions					
LDSB	(LDSBA)	Load Signed Byte	(from Alternate Space)	1[2]	1
LDSH	(LDSHA)	Load Signed Halfword	(from Alternate Space)	1[2]	1
LDUB	(LDUBA)	Load Unsigned Byte	(from Alternate Space)	1[2]	1
LDUH	(LDUHA)	Load Unsigned Halfword	(from Alternate Space)	1[2]	1
LD	(LDA)	Load word	(from Alternate Space)	1[2]	1
LDD	(LDDA)	Load Doubleword	(from Alternate Space)	1[2]	2
LDF		Load Floating Point		not supported	not supported
LDFF		Load Double Floating Point		not supported	not supported
LDFSR		Load Floating-Point State Register		not supported	not supported
LDC		Load Coprocessor		not supported	not supported
LDDC		Load Double Coprocessor		not supported	not supported
LDCSR		Load Coprocessor State Register		not supported	not supported
STB	(STBA)	Store Byte	(into Alternate Space)	1 or 2[6]	1
STH	(STHA)	Store Harfword	(into Alternate Space)	1 or 2[6]	1
ST	(STA)	Store Word	(into Alternate Space)	1 or 2[6]	1
STD	(STDA)	Store Doubleword	(into Alternate Space)	1 or 2[6]	2
STF		Store Floating-Point		not supported	not supported
STDF		Store Double Floating-Point		not supported	not supported
STFSR		Store Floating-Point State Register		not supported	not supported
STDFQ		Store Double Floating-Point Queue		not supported	not supported
STC		Store Coprocessor		not supported	not supported
STDC		Store Double Coprocessor		not supported	not supported
STCSR		Store Coprocessor State Register		not supported	not supported
STDCQ		Store Double Coprocessor Queue		not supported	not supported
LDSTUB	(LDSTUBA)	Atomic Load-Store Unsigned Byte	(in Alternate Space)	3	3
SWAP	(SWAPA)	Swap r-register with Memory	(in Alternate Space)	3	3
Arithmetic/Logical/Shift					
ADD	(ADDcc)	Add	(and modify icc)	1	1
ADDX	(ADDXcc)	Add with Carry	(and modify icc)	1	1
SUB	(SUBcc)	Subtract	(and modify icc)	1	1
SUBX	(SUBXcc)	Subtract with Carry	(and modify icc)	1	1
TADDcc	(TADDccTV)	Tagged Add and Modify icc	(and Trap on overflow)	1	1
TSUBcc	(TSUBccTV)	Tagged Subtract and Modify icc	(and Trap on overflow)	1	1
DIVSCC		Divide Step		not supported	1
SCAN		Scan for MSB		not supported	1
SDIV	(SDIVcc)	Integer Divide	(and modify icc)	37	not supported
SMUL	(SMULcc)	Integer Multiply	(and modify icc)	6	max5[5]
MULScc		Multiply Step and Modify icc		1	1
UDIV	(UDIVcc)	Unsigned Divide (integer)		37	not supported
UMUL	(UMULcc)	Unsigned Multiply (integer)		6	max5[5]
AND	(ANDcc)	And	(and modify icc)	1	1
ANDN	(ANDNcc)	And Not	(and modify icc)	1	1
OR	(Orcc)	Inclusive Or	(and modify icc)	1	1
ORN	(ORNcc)	Inclusive Or Not	(and modify icc)	1	1
XOR	(XORcc)	Exclusive Or	(and modify icc)	1	1
XNOR	(XNORcc)	Exclusive Nor	(and modify icc)	1	1
SLL		Shift Left Logical		1	1
SRL		Shift Right Logical		1	1
SRA		Shift Right Arithmetic		1	1
SETHI		Set High 22 Bit of r-register		1	1
SAVE		Save Caller's Window		1	1
RESTORE		Restore Caller's Window		1	1

Control Transfer			
Bicc	Branch on Integer Condition Codes	1[3]	1[3]
Fbicc	Branch on Floating-Point Condition Codes	not supported	not supported
CBccc	Branch on Coprocessor Condition Codes	not supported	not supported
CALL	Call	1[3]	1[3]
JMPL	Jump and Link	1[3]	2[3]
RETT	Return from Trap	1[3]	2[3]
Ticc	Trap on Integer Condition Codes	1	3
Read/Write Control Registers			
RDASR	Read Ancillary Register	1	1
RDY	Read Y Register	1	1
RDPSR	Read Processor State Register	1	1
RDWIM	Read Window Invalid Mask	1	1
RDTBR	Read Trap Base Register	1	1
WRASR	Write Ancillary State Register	1	1
WRY	Write Y Register	1	1
WRPSR	Write Processor State Register	1	1
WRWIM	Write Window Invalid Mask	1	1
WRTBR	Write Trap Base Register	1	1
UNIMP	Unimplemented Instruction	1	3
FLUSH	Instruction Cache Flash	4	not supported
FP(CP) Operations			
Fpop	Floating-Point Unit Operations	not supported	not supported
Cpop	Coprocessor Operations	not supported	not supported

Notes:
1. MB8686X CPI assume Worst Case in 1 command execution.
2. For ASI=0xc, 0xd, 0x10-0x18, 0x31access, the CPI changes.
3. Assumes that delay slots are buried in usable instructions
4. Assumes that all CPI hit to I-cache and d-cache
5. 32bit x 0bit 1cycle
   32bit x 8bit 2cycle
   32bit x 16bit 3cycle
   32bit x 32bit 5cycle
6. Execution of stores in IMB odd clock cycles takes 2 clocks and in even cycles 1 clock.

10. APPENDIX B (Instruction Grouping in MB8686X)

Group B is divided into Group B#0 and Group B#1. Group B#0 instructions affect condition codes, while Group B#1 does not. FPU instructions are not supported, and there is therefore no Group C.

Group ID		Group Name	Instructions
A		Load/Store	LDSB, LDSH, LD, LDUB, LDUH, LD, LDD, ST, STB, STH, STD, SWAP, LDSTUB
B	B#0	ALU (arithmetic/logic which affects condition codes)	ADDcc, ADDXcc, SUBcc, SUBXcc, TADDcc, TSUBcc, MULScc, ANDcc, ANDNcc, ORcc, ORNcc, XORcc, XNORcc,
	B#1	ALU (arithmetic/logic which does not affect condition codes)	ADD, ADDX, SUB, SUBX AND, ANDN, OR, ORN, XOR, XNOR SLL, SRL, SRA, SETHI
C		FP instruction (FP add/multiply)	not supported
D		(reserved)	(reserved)
E		Bcc (Branch control transfer)	Bicc
F		Single-step	CALL, JMPL, RETT, SAVE, RESTORE, TADDccTV, TSUBccTV, UMUL, UMULcc, SUML, SMULcc, UDIV, UDIVcc, SDIV, SDIVcc, RDY, RDPSR, RDWIM, RDTBR, WRY, WRPSR, WRWIM, WRTBR, LDSBA, LDSHA, LDA, LDUBA, LDUHA, LDDA, STA, STBA, STHA, STDA, SWAPA, LDSTUBA Ticc, FLUSH.

Simultaneously executable instruction combinations

Through the addition of a 2nd ALU to the MB8686X, it has become possible to execute 2 ALU instructions at the same time. The 2nd ALU can only execute instructions which do not affect condition codes.

Slot-a	***Slot-b***
group A	group B
group A	group E
group B	group A
group B	group B#1

Slot-a	***Slot-b***
group B#1	group B
group B	group E
group E	group A
group E	group B

11. MB86860 Signals

Table 11-1 SPARClite Bus Signals (1/3)

Pin Names (Attribute)	Pin Status		Explanation
	Sleep Mode	Bus Grant	
RESET# (input)	--------	--------	**System Reset**. Asserting RESET# for at least 10 CLKIN cycles after the clock has stabilized, causes the MB8686X to be initialized.
CLKIN (input)	--------	--------	**Clock Input**. This clock determine execution rate of SPARClite bus and timing of MB8686X processor.
CLKSEL0 CLKSEL1 (input)	--------	--------	**Clock multiply mode select**. These pins determine the clock multiply mode. Internal operating frequency is determined by CLKIN and combination of CLKSEL1 and CLKSEL0. (CLKSEL1, CLKSEL0) == (0,0): Reserved, (0,1): X2 mode, (1,0): X3 mode, (1,1): X4 mode.
AS# (output)	O(Z)	O(Z)	**Address Strobe** . In the beginning of bus cycle, one clock period "L" is output. Basically, a bus cycle starts with an assertion of AS# and terminated by an assertion of READY# or RDYOUT#.
ASI<3:0> (output)	O(Z)	O(Z)	**ASI output** . During a bus cycle, ASI<3:0> are valid similar to address signal.
ADR<31:2> (output)	O(Z)	O(Z)	**Address output**. ADR<31:2> are signal for identifying instruction addresses or data addresses. This signal are valid during bus cycle periods. Output values during Idle cycles are not guaranteed. During burst transfers, address signal switch (incremented) at assertion of READY#. Note: In case of 860 series, address are updated by wrap-round while in 830 series address are updated by toggle mode. In 16-bit and 8-bit bus widths, ADR<1:0> information are output on BE4# and BE5# pins.
D<63:0> (input/output)	I(Z)	I(Z)	**Data Bus**. It is a bi-directional data bus used for instruction fetches, data loads and data stores. Double word data types must be aligned in addresses which are multiples of 8, word data types in addresses which are multiples of 4 and half word data types in addresses which are multiples of 2 respectively. D<7:0> are used in 8-bit bus mode, D<15:0> in 16-bit bus mode and D<31:0> in 32-bit bus mode. Pull up resistance should be attached to unused data bus pins if entire address space are assigned to 8 or 16 or 32bit bus width.
DP0~DP7 (input/output)	I (Z)	I(Z)	**Data Parity**. These signals are parity input during reads and parity output during writes. DP0 correspond to parity of D<63:56>. DP1 to DP7 correspond to D<55:48> to D<7:0> respectively. In 32-bit bus mode, DP4~DP7 are used, in 16-bit bus mode DP6 and DP7, and in 8-bit bus mode DP7 is used. Pull up resistance should be attached if unused DP signals exist.
RD# (output)	O(Z)	O(Z)	**Read Signal**. When the current bus cycle is a READ cycle, "L" is output, and in WRITE cycle or IDLE cycle periods "H" is output. Output level is maintained from the beginning to the end of a bus cycle. This signal has been added to the SPARClite -830 Series. In order to maintain design compatibility with the 830 Series, use only RDWR# signals when doing your designing.
RDWR# (output)	O(Z)	O(Z)	**Read/write signal**. When the current bus cycle is a WRITE cycle "L" is output, and in READ cycle or IDLE cycle periods "H" is output. Output level is maintained from the beginning to the end of a bus cycle.

SPARClite Bus Signals (2/3)

Pin Names	Pin Status		Explanation
	Sleep Mode	Bus Grant	
BE0#~BE7# (output)	O(Z)	O(Z)	**Byte Enable signals**. In both READ and WRITE cycle, "L" is output according to valid byte data. In 16-bit and 8-bit bus modes, ADR<1> and ADR<0> are output respectively to BE4# and BE5# pin. These signals are valid during bus cycle periods.
CS0#~CS5# (output)	O(H)	O(H)	**Chip Select**. One of these signals are asserted when address area are accessed. Corresponding address area are determined by the value of ARSR and AMR registers. For detail usage, see the explanation of ARSR/AMR Registers. In DMAC operations, CS# signals determined by DMCR Register setting. Also, these signals are irrelevant during access to SDRAM areas.
DTYP< 1: 0> (output)	O(X)	O(X)	**DATA TYPE**. Indicates data access type (double-word, word, half-word, byte). The output level of DTYP<1> means 11:double word, 10:word, 01:half-word and 00: byte. However, during burst transfers and cache area writes, 11 are asserted regardless of access type.
READY# (input)	--------	--------	**READY Input**. Input "L" to this pin terminates a bus cycle. In burst transfers, READY must be asserted a prescribed number of times for each address strobe assert.
RDYOUT# (output)	O(H)	O(H)	**Internal READY Output Signal**. RDYOUT# indicates termination of bus cycle. RDYOUT# is generated by internal wait state generator.
MEXC# (input)	--------	--------	**Memory Access Exception**. When "L" is input to this pin in the same cycle as a READY# input, the CPU handles it as an instruction access exception or a data access exception and generates a trap. Operations in which this signal is asserted in timing other than the same cycle as a READY#, input are not guaranteed (Cases where an exception occurs when the ET bit of the PSR is "0" result in error status). For MEXC# in burst transfers, see the MEXC explanation.
BREQ# (input)	--------	--------	**Bus Request**. When this signal are asserted by an external bus master, CPU release bus ownership to external bus master when a bunch of bus cycle are completed. Bus release timing is as follows. 1) Burst read/write : after completion of burst access. 2) Single write/read to or from non-cache area: completion of the bus cycle. 3) Atomic LD/ST: after completion of Atomic LoadStore cycle. 4) Read/Write from 8/16/32 bit bus: after required number of single transfers.
BGRNT# (output)	O(V)	O(L)	**Bus Grant Signal**. When a bus request (BREQ#) is accepted, this signal is asserted, and external devices are notified that bus are released.
PBREQ# (output)	O(H)	O(V)	**Processor Bus Request**. This signal is asserted by the processor to indicate to an external bus arbiter on SPARClite bus that it needs to regain control of the SPARClite bus. This provides a handshake between the arbiter and the processor to allow the bus to allocate based on demand.
BMREQ# (output)	O(H)	O(H)	**Burst Mode Request**. This signal is asserted by the processor to indicate to the external system that the current transaction can be a burst. If the external system supports burst mode, it asserts BMACK# is concurrently with READY# to begin the burst mode transfer.
BMACK# (input)	--------		**Burst Mode Acknowledge**. This signal is asserted by the system to indicate that it can support burst mode for the address currently on the bus. The system asserts BMACK# in response to the processor asserting BMREQ#.

SPARClite Signals (3/3)

Pin Names	Pin Status		Explanation
	Sleep Mode	Bus Grant	
LOCK# (output)	O(Z)	O(Z)	**Bus Lock Signal**. This is a control signal asserted by the processor to indicate to the system that the current bus transaction requires more than one transfer on the bus. The Atomic Load Store instruction for example requires contiguous bus transactions which cause the LOCK# is active. LOCK# is asserted with the assertion of AS# and remains active until READY# is asserted at the end of the locked transaction.
BMODE16# BMODE32# (input)	--------	--------	**Boot Mode Bus Width**. These signals are sampled at negation of RESET#. And the processor determine the bus width for CS0# area based on the combination of those signals. (BMODE16#,BMODE32#)=(0,0) means that bus width are 8bit, (01),(10), (11) means 16bit, 32bit, 64bit respectively.
ERROR# (input)	O(V)	O(V)	**Error Signal**. Asserted by the CPU to indicate that it has halted in an error state as a result of encountering a synchronous trap while traps are disabled. In this situation the CPU saves the PC and nPC registers, sets the tt value in the TBR, enters into an error state and asserts the ERROR# signal. The system can monitor the ERROR# pin and initiate a reset under the error condition. This pin is high on reset.
IRL<3:0> (input)	--------	--------	**Interrupt Request Level**. The value on these pins defines the external interrupt level. IRL<3:0>=1111 forces a non-maskable interrupt. IRL value of 0000 indicates no pending interrupts. All other values indicate maskable interrupts as enabled in the PIL field of the processor status register (PSR). Interrupts should be latched and prioritized by external logic and should be held pending until acknowledged by the processor.

SDRAM Signals

Pin Names	Pin Status	Explanation
	SleepMode	
SCLK (output)	O(L)	**SDRAM clock**. Should be linked to SDRAM clock input. Clock frequency is the same as internal IMB bus frequency.
CKE (ouput)	O(H)	**SDRAM Clock Enable signal**.
SRAS# (output)	O(H)	**SDRAM RAS signal**.
SCAS# (output)	O(H)	**SDRAM CAS signal.**
SWE# (output)	O(H)	**SDRAM Write Enable signal**.
SCS3# - SCS0# (output)	O(H)	**SDRAM Chip Select signals**.
SBA<1:0> (output)	O(X)	**SDRAM Bank Select signal**.
SADR<12:0>	O(X)	**SDRAM Address signal**. Addresses are multiplexed.

(output)		
SDQ<63:0> (input/output)	O(Z)	**SDRAM Data Bus**.
SDQM<0:7> (output)	O(H)	**SDRAM Input Mask** (Output Enable signal).
SDP<0:7> (input/output)	O(X)	**SDRAM Parity signal**.

DMAC,Debug Support and Sleep Mode Signals

Pin Names	Pin Status		Explanation
	Sleep Mode	Bus Granted	
EOP# (output)	O(V)	O(V)	**End of Process**. The signal indicates the transfer count of DMAC reaches zero. The EOP signal has no precise timing relation to bus cycle. 1) [Transfer from SDRAM bus to SPARClite bus] When EOP is asserted, it is guaranteed that all SDRAM access by DMAC is completed. 2) [Transfer from SPARClite bus to SDRAM bus] When EOP is asserted, the last access to SDRAM are still in progress.
BRKEN# (input)	--------	--------	**Break Enable**. If this signal is active ('0') at negation of RESET#, debug mode is enabled.
DBREAK# (input)	--------	--------	**Debug Break**. Activation of the DBREAK# will cause a Debug Trap at any cycle if DSU(Debug Support Unit) is enabled. If BRKEN# was sampled inactive at RESET# fall, DBREAK# will not have any influence. If both DBREAK# and BRKEN# are sampled active ('0') with RESET# fall, the MB8686X immediately jumps to Debug Trap routine (0x00000ff0), instead of starting from 0.
BRKGO (output)	O(V)	O(V)	**Break Go**. This signal indicates the processor is in debug trap state. BRKGO is asserted with the assertion of AS# for accessing Debug Trap routine and remains active until next AS# is asserted for accessing normal program.
PDOWN#(output)	O(L)	O(V)	**Sleep Mode**. This signal indicates the processor completed to enter sleep mode.
WKUP# (input)	--------	--------	**Wake Up**. Activation of the WKUP# will cause re-start of program execution. This pin is asynchronous input. At least 2 CLKIN cycles is required for WKUP# pulse during Sleep Mode(PDOWN#=="L").
STOP# (input)	--------	--------	**Internal Clock Stop**. Activation of the STOP# signal during Sleep Mode, the CPU goes into STOP Mode and stops PLL, and all internal clocks stop.

JTAG, TEST and Other Signals

Pin Names	Pin Status		Explanation
	Sleep Mode	Bus Granted	
TDI (input)	--------	--------	**Test Data Input**. JTAG Data Input Pin. Pull-up register is required when JTAG is not used .
TMS (input)	--------	--------	**Test Mode Set**. JTAG Mode Set Input Pin. Pull-up register is required when JTAG is not used .
TDO (output)	O(X)	O(X)	**Test Data Output**. JTAG Data Output Pin.
TCLK (input)	--------	--------	**Test Clock Input**. JTAG Clock Input Pin. Pull-up register is required when JTAG is not used .
TRST# (input)	--------	--------	**Test Reset Input**. JTAG Reset Input Pin. Should normally be set to “L”.
BEN# (input)	--------	--------	**PLL Bypass Enable**. This signal can be used for test purpose only. When this signal is “L”, PLL Bypass Mode is enabled. It should normally be fixed to “H”.

BCLK (input)	--------	--------	**PLL Bypass Clock**. This signal can be used for test purpose only. When BEN# has been set to "L" and is in Bypass Mode, clocks are provided to the CPU core from this pin. It should normally be fixed to "H".
PLLCEN# (input)	--------	--------	**PLLCLK Enable**. This signal can be used for test purpose only. If "L" is input to this pin, it outputs a PLL clock to the PLLCLK pin. Should normally be fixed to "H".
NCTEST# (input)	--------	--------	**Test Pin**. Should normally be fixed to "H".
FLOAT# (input)	--------	--------	**Pin Float**. This is a control signal to force all output pin to tri-state. If this pin is tied to "L", CPU sets all output pins and bi-directional pins to High-Z state.
TEST1 (input)	--------	--------	**Test Pin**. Should normally be fixed to "H".
TEST2 (input)	--------	--------	**Test Pin**. Should normally be fixed to "H".

O(V) : Circuit is operating and outputting valid levels.
O(X) : Output is undefined.
O(Z) : Output pin is High-Z.
O(H) : Outputs "H".
O(L) : Outputs "L".
I(Z) : Input status and High-Z.

12. ELECTRICAL CHARACTERISTICS

This electrical characteristics shows Target Spec. These specifications may undergo future changes based on actual device after characterization.

12.1. Absolute Maximum Ratings

V_{SS}=0V

Symbol	Rating	Min.	Max.	Units
V_{DDE}	Supply Voltage (I/O)	-0.5	4.0	V
V_{DDI}	Supply Voltage (Core)	-0.5	3.0	V
V_I	Input Voltage	-0.5	V_{DDE}+0.5	V
T_{STG}	Storage Temperature	-55	125	□
T_{BIAS}	Ambient Temp. Under Bias	0	70	□

Note Stresses above those listed under Absolute Rating may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for external periods may affect device reliability.

Recommended Conditions

Power and ground connections must be made to multiple Vdd and Vss pins. Every MB86860 based circuit board should include power(Vdd) and ground (Vss) planes for power distribution. Every Vdd pin must be connected to the power plane, and every Vss pins must be connected to the ground plane. Pins identified as "N.C" must not be connected in the system.

Liberal decoupling capacitance should be placed near the MB86860. The processor can cause transient power surges when its numerous output buffers transition, particularly when connected to large capacitive loads.

Low inductance capacitors and interconnections are recommended for best high frequency electrical performance. Inductance can be reduced shortening the board traces between the processor and decoupling capacitors as much as possible.

For reliable operation, alternate bus masters must drive any pins that are three-stated by the MB86860 when it has granted the bus, in particular LOCK#, ADR<31:2>, ASI<3:0>, BE0-7#, D<63:0>, AS#, and RDWR#, RD#, DTYP<1:0> must be driven by alternate bus masters. These pins are normally driven by the processor during active and idle bus states and don't require external pull-ups. N.C. pins must always remain unconnected.

12.2. Recommended Operating Conditions

V_{SS}=0V

Symbol	Rating	Min.	Typ.	Max.	Units
V_{DDE}	Supply Voltage (I/O)	3.15	3.3	3.45	V
V_{DDI}	Supply Voltage (Core)	2.4	2.5	2.6	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{IH}	Input High Voltage	2.0	-	V_{DDE}+0.3	V
T_{opr}	Operating Temperature	0	25	70	□

□ **2 Power Supply Systems are required for MB86860. The order of supplying each voltage is recomended as follows.**

On Power-On V_{DDI} V_{DDE} External Signals

On Power-Off External Signals V_{DDE} V_{DDI}

12.3. DC Specifications

V_{SS}=0V, Ta=0~70□

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IL}	Input Low Voltage		0	-	0.8	V
V_{IH}	Input High Voltage		2.0	-	V_{DDE}	V
V_{OL}	Output Low Voltage	I_{OL}= 2mA	0	-	0.4	V
V_{OH}	Output High Voltage	I_{OH}= -2mA	V_{DDE}-0.4	-	V_{DDE}	V
I_{LI}	Input Leakage Current	V_{IN}= 0 or V_{DDE}	-5	-	5	µA
I_{LZ}	3-stateOutput Leakage	V_{OUT}= 0 or V_{DDE}	-5	-	5	µA
I_{DD}	Power Supply Current(V_{DDE})	50MHz (No Load)	-	95	120	mA
	Power Supply Current(V_{DDI})	200MHz	-	1100	1400	mA
I_{SLEEP}	Power Supply Current On Sleep Mode(V_{DDI})	200MHz	-	27	34	mA
P_D	Power Dissipation (V_{DDE} + V_{DDI})	200MHz (No Load)	-	-	4.1	W
C_{PIN}	Input Capacitance	V_{DDE}= V_I= 0 f= 1MHz	-	-	16	pF

12.4. AC Characteristics

SPARClite-IF

AC characteristics of SPARClite interface signals are defined with respect to CLKIN(External Bus Clock) and does not depend on the internal clock.

Ta=0~70□

Item	Parameter Description		Min.	Max.	Units
CLKIN	CLKIN period		20	40	ns
	CLKIN high time		8	-	ns
	CLKIN low time		8	-	ns
	CLKIN rise time		-	2	ns
	CLKIN fall time		-	2	ns
SPARClite-IF Output	D<63:0>, DP0□7	Output valid delay	-	13	ns
		Output hold	2	-	
	ADR<31:2>	Output valid delay	-	13	ns
		Output hold	2	-	
	BE0~7#	Output valid delay	-	13	ns
		Output hold	2	-	
	ASI<3:0>	Output valid delay	-	13	ns
		Output hold	2	-	
	CS0~5#	Output valid delay	-	13	ns
		Output hold	2	-	
	AS#	Output valid delay	-	13	ns
		Output hold	2	-	
	RDWR#	Output valid delay	-	13	ns
		Output hold	2	-	
	RD#	Output valid delay	-	13	ns
		Output hold	2	-	
	DTYP<1:0>	Output valid delay	-	13	ns
		Output hold	2	-	
	LOCK#	Output valid delay	-	13	ns
		Output hold	2	-	
	BGRNT#	Output valid delay	-	13	ns
		Output hold	2	-	
	PBREQ#	Output valid delay	-	13	ns
		Output hold	2	-	
	BMREQ#	Output valid delay	-	13	ns
		Output hold	2	-	
	RDYOUT# (Internal READY Mode)	Output valid delay	-	13	ns
		Output hold	2	-	
	RDYOUT# *6 (External READY	Output valid delay	-	13	ns
		Output hold	2	-	
	ERROR#	Output valid delay	-	13	ns
		Output hold	2	-	

SPARClite-IF (Continued)

AC characteristics of SPARClite interface signals are defined with respect to CLKIN(External bus Clock) and does not depend on the internal clock.

Ta=0~70□

Item	Parameter Description		Min.	Max.	Units
SPARClite-IF Input	READY#	Input setup time	6	-	ns
		Input hold time	2	-	
	MEXC#	Input setup time	6	-	ns
		Input hold time	2	-	
	D<63:0>, DP0□7	Input setup time	6	-	ns
		Input hold time	2	-	
	BREQ#	Input setup time	6	-	ns
		Input hold time	2	-	
	BMACK#	Input setup time	6	-	ns
		Input hold time	2	-	
	IRL<3:0>	Input setup time	async.		ns
		Input hold time	async.		
	BMODE32#, 16#	Input setup time	Must be fixed to 'H'or'L'		--
		Input hold time	Must be fixed to 'H'or'L'		

DMAC, DSU and SLEEP MODE Signals

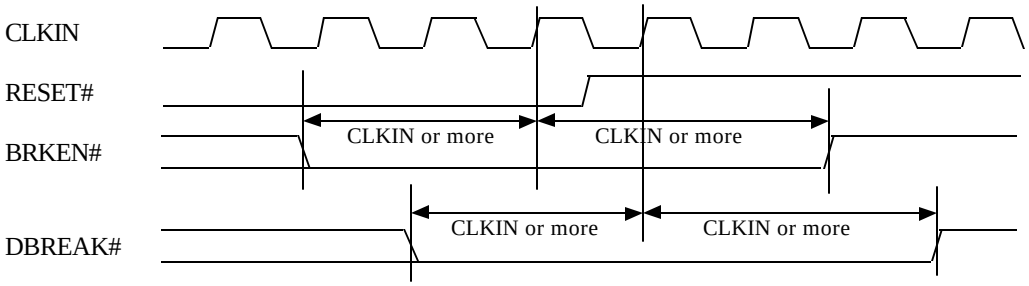
AC characteristics of those signals are defined with respect to CLKIN(External Bus Clock) and does not depend on the internal clock.

Ta=0~70□

Item	Parameter Description		Min.	Max.	Units
Output	EOP#	Output valid delay	-	13	ns
		Output hold	2	-	
	BRKGO#	Output valid delay	-	13	ns
		Output hold	2	-	
	PDOWN#	Output valid delay	-	13	ns
		Output hold	2	-	
Input	WKUP#	Input setup time	async.		ns
		Input hold time	async.		
	STOP#	Input setup time	async.		ns
		Input hold time	async.		
	BRKEN# *1	Input setup time	6	-	ns
		Input hold time	2	-	
	DBREAK# *2	Input setup time	6	-	ns
		Input hold time	2	-	

Note *1) BRKEN# is sampled at negation of RESET#(For detail, see following timing diagram). If BRKEN# is active("0") at negation of RESET#, debug mode is enabled.

Note *2) If both DBREAK# and BRKEN# are sampled active('0') with RESET# fall, MB8686X immediately jumps to Debug Trap Routine (0x00000ff0), instead of starting from 0.



SDRAM-IF

AC characteristics of SDRAM interface signals are defined with respect to SCLK(SDRAM Clock) .

Ta=0~70□

Item	Parameter Description		Min.	Max.	Units
SDCLK Output	SDCLK period		10	20	ns
	SDCLK high time		4	-	ns
	SDCLK low time		4	-	ns
	SDCLK rise time		-	1	ns
	SDCLK fall time		-	1	ns
SDRAM-IF Output	SRAS#	Output valid delay	-	8	ns
		Output hold	2	-	
	SCAS#	Output valid delay	-	8	ns
		Output hold	2	-	
	SWE#	Output valid delay	-	8	ns
		Output hold	2	-	
	CKE#	Output valid delay	-	8	ns
		Output hold	2	-	
	DQM0□7	Output valid delay	-	8	ns
		Output hold	2	-	
	SADR<12:0>	Output valid delay	-	8	ns
		Output hold	2	-	
	SBA<1:0>	Output valid delay	-	8	ns
		Output hold	2	-	
	SCS0□3#	Output valid delay	-	8	ns
		Output hold	2	-	
	SD<63:0>, SDP0□7	Output valid delay	-	8	ns
		Output hold	2	-	
SDRAM-IF Input	SD<63:0>, SDP0□7	Input Setup	3	-	ns
		Input hold	2	-	

Other Signals

Ta=0~70□

Item	Parameter Description	V_{DDE}=3.3V±0.15V		Units
		Min.	Max.	
	RESET#	async.		-
	CLKSEL0,1	Must be fixed to H" or "L"		-
	BCLK Test Pin	Must be fixed to H"		-
	BEN# Test Pin	Must be fixed to H"		-
	PLLCEN# Test Pin	Must be fixed to H"		-
	TEST1,2 Test Pin	Must be fixed to H"		-
	FLOAT# Test Pin	Must be fixed to H"		-

1. Parameters are valid over specified temperature range and supply voltage range unless otherwise noted.
2. All voltage measurements are referenced to ground. All time measurements are referenced at input and output levels of 1.5V. For testing, all inputs swing between 0.4Vand 2.4V. Input rise and fall times are 1.5ns or less.
3. Not more than one output may be shorted at a time for a maximum duration of one second.
4. All output timings are based on a 30pF load.
5. All timings except ones described as Asynchronous are with respect to the rising edge of CLKIN (external clock).
6. If loop back from READY# to RDYOUT# is enabled, RDYOUT# timing is with respect to READY# input on external READY Mode.

* These specifications may undergo future changes for the sake of improvement.

A minimum of 10 CLKIN Cycles are required for RESET# period. Also 600us are required for PLL oscillation stabilization time.