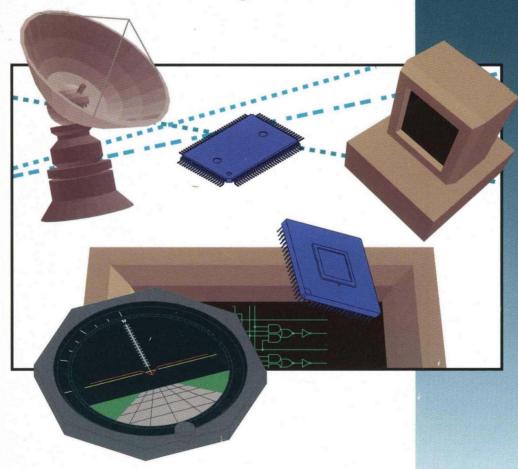
# FUĴITSU

# **CMOS Channeled Gate Arrays**

1991 Data Book and Design Evaluation Guide



1991

FUĴITSU

Design Information

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UHB Series Unit Cell Library

3

CG10 Series Unit Cell Library

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Sales Information

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# **CMOS Channeled Gate Arrays**

1991 Data Book and Design Evaluation Guide

Fujitsu Microelectronics, Inc. Integrated Circuits Division 3545 North First Street, San Jose, CA 95134–1804 Tel: (408) 922–9000 FAX: (408) 432–9044 Copyright© 1990 Fujitsu Microelectronics, Inc., San Jose, California

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#### **Preface**

Fujitsu Microelectronics introduced its first commercially available gate array, a bipolar chip called the B200, in 1974 (Fujitsu had been making them for internal use since 1972). Over the years it has been so popular that it is regarded as the world's most widely implemented gate array. Since that first array, Fujitsu has produced over 9000 successful bipolar and CMOS custom designs.

Fujitsu designs are successful because they are implemented using the most advanced design verification CAD systems available, allowing the production of chips with 90% cell utilization (more functional logic per chip than the industry standard) and one of the highest performance records in the industry.

This data book provides you with information necessary to choose an application specific IC (ASIC) design using one of Fujitsu's advanced CMOS channeled gate array technologies (UHB and CG10). The data book describes Fujitsu's CMOS channeled gate array technologies, explains the benefits and specifications applicable to each, and outlines the process by which logic and circuit designers create a chip. Except where noted, the material presented in this data book is common to all of Fujitsu's CMOS channeled technologies. The device (unit cell) libraries for these channeled gate array technologies are included at the end of this volume. Another volume in this series provides the same information for Fujitsu's channelless or sea-of-gates ASIC technologies.

Fujitsu has pioneered and maintained a technological lead in the production of bipolar as well as CMOS ASIC devices; data books describing Fujitsu's other ASIC product families, as well as any other technical or sales-related information, may be obtained from any Fujitsu Technical Resource Center or Sales Office listed at the end of this book or by calling or writing Fujitsu Microelectronics Inc., 3545 North First Street, San Jose. CA 94135–1804, (408) 922–9000.

## **Fujitsu ASIC Products Listing**

#### **CMOS Channeled Gate Arrays Data Book**

#### UHB Series High Drive CMOS Gate Arrays — 1.5μ, 0.9 ns typical delay

Description	Name	Device Part Number
336 Gates, 58 I/O	СЗЗОИНВ	MB625xxx
530 Gates, 64 I/O	C530UHB	MB624xxx
830 Gates, 74 I/O	C830UHB	MB623xxx
1,233 Gates. 88 I/O	C1200UHB	MB622xxx
1,724 Gates, 102 I/O	C1700UHB	MB621xxx
2,220 Gates, 115 I/O	C2200UHB	MB620xxx
3,066 Gates, 140 I/O	C3000UHB	MB606xxx
4,174 Gates, 155 I/O	C4100UHB	MB605xxx
6,000 Gates, 155 I/O	C6000UHB	MB604xxx
8,768 Gates, 188 I/O	C8700UHB	MB603xxx
12,734 Gates, 220 I/O	C12000UHB	MB602xxx

#### CG10 Series High Drive CMOS Gate Arrays — 0.8µ, 0.5 ns typical delay

3,256 Gates, 108 I/O	CG10272	MBCG10272xxx
4,032 Gates, 123 I/O	CG10342	MBCG10342xxx
5,072 Gates, 148 I/O	CG10492	MBCG10492xxx
6,510 Gates, 163 I/O	CG10572	MBCG10572xxx
7,684 Gates, 163 I/O	CG10692	MBCG10692xxx
11,080 Gates, 188 I/O	CG10103	MBCG10103xxx
14,720 Gates, 220 I/O	CG10133	MBCG10133xxx

#### **CMOS Channelless Gate Arrays Data Book**

## AU Series CMOS Series Gate Arrays — $1.2\mu$ , 0.6 ns typical delay

10,224 Gates, 108 I/O	C10KAU	MB637xxx
15,486 Gates, 138 I/O	C15KAU	MB636xxx
20,876 Gates, 155 I/O	C20KAU	MB635xxx
31,500 Gates, 178 I/O	C30KAU	MB634xxx
41,184 Gates, 220 I/O	C40KAU	MB633xxx
52,164 Gates, 257 I/O	C50KAU	MB632xxx
75,140 Gates, 300 I/O	C75KAU	MB631xxx
102,144 Gates, 332 I/O	C100KAU	MB630xxx

#### CG21 Series CMOS Series Gate Arrays — 0.8µ, 370 ps typical delay

10,224 Gates, 108 I/O	CG21103	MBCG21103xxx
15,486 Gates, 142 I/O	CG21153	MBCG21153xxx
20,876 Gates, 155 I/O	CG21203	MBCG21203xxx
31,500 Gates, 178 I/O	CG21303	MBCG21303xxx
41,184 Gates, 220 I/O	CG21403	MBCG21403xxx
52,164 Gates, 245 I/O	CG21503	MBCG21503xxx
75,140 Gates, 284 I/O	CG21753	MBCG21753xxx
102,144 Gates, 332 I/O	CG21104	MBCG21104xxx

## Fujitsu ASIC Products Listing (Continued)

#### **BiCMOS Gate Arrays Data Book**

#### BC Series BiCMOS Gate Arrays — 1.5μ/1.4μ, 0.65 ns typical delay

Description	Name	Device Part Number
645 Gates, 52 I/O	BC400	MB211xxx
1,218 Gates, 72 I/O	BC800	MB212xxx
1,872 Gates, 96 I/O	BC1200	MB213xxx
3,240 Gates, 112 I/O	BC2000	MB214xxx

#### BC-H Series BiCMOS Gate Arrays — 1.0µ/0.5µ, 0.45 ns typical delay

4,312 Gates, 96 I/O	BC4000H	MB221xxx
8,160 Gates, 128 I/O	BC8000H	MB222xxx
11,968 Gates, 160 I/O	BC12000H	MB223xxx
16,720 Gates, 200 I/O	BC16000H	MB224xxx
7.920 Gates, 200 I/O with 40Kb RAM	BC8040HM	MB228xxx

#### **ECL Gate Arrays Data Book**

## ET Series ECL Gate Arrays — 1.0μ, 220 ps typical delay

1,056 Gates, 64 I/O		ET750	MB121Kxxx
2,112 Gates, 88 I/O	- 1 × × × × × × × × × × × × × × × × × ×	ET1500	MB123Kxxx
4,224 Gates, 120 I/O		ET3000	MB125Kxxx
6,160 Gates, 120 I/O		ET4500	MB128Kxxx
2,640 Gates, 120 I/O with 4.6 Kb RAM		ET2004M	MB181/191xxx
2,640 Gates, 136 I/O, with 9.2 Kb RAM		ET2009M	MB182/192xxx
3,960 Gates, 136 I/O, with 4.6 Kb RAM		ET3004M	MB183/193xxx

#### H Series ECL Gate Arrays — $0.5\mu$ , 100 ps typical delay

9,856 Gates, 200 I/O	ET10000H	MB147/157xxx
9,856 Gates, 300 I/O	E10000H	MB148/158xxx
4 928 Gates 200 I/O with 5 1Kh RAM	F5005HM	MR185/195vvv

#### Ultra High Performance ECL Gate Arrays — $0.5\mu$ , 75 ps typical delay

128 Gates, 23 /I/O	E128H	MB1800
32 Gates, 13 I/O	E32	MB1700
128 Gates 16 I/O	F128	MB1600

#### VH Series ECL Gate Arrays — 0.4μ, 80 ps typical delay

38,948 Gates, 300 I/O	E30000VH	MB162/172xxx
13,440 Gates, 290 I/O, 40Kb RAM	E10040VHM	MB165/175xxx
13,440 Gates, 294 I/O, 160Kb ROM	E10160VHR	MB168/178xxx
2 5// Gates 10/ I/O	ET2600VH	MBBG31363vv

#### **CMOS Standard Cell Data Book**

AU Series Standard Cells —  $1.2\mu$ , 0.6 ns typical delay

AS Series Standard Cells — 0.8μ, 370 ps typical delay



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# **Design Information**

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## 5

## Chapter 1 - Fujitsu CMOS Products

#### **Contents of This Chapter**

- 1.1 Introduction
- 1.2 CMOS Technology for ASICs
- 1.3 CMOS Gate Array Structure
- 1.4 Fujitsu's CMOS Channeled Gate Array Technologies: CG10 and UHB Data Sheets

#### 1.1 Introduction

This section of the data book gives an overview of CMOS technology and introduces the CMOS channeled gate array technology families developed by Fujitsu to implement ASIC designs.

#### 1.2 CMOS Technology for ASICs

ASICs (Application Specific Integrated Circuits) are large scale integrated circuits that provide customers with made-to-order functions. These ICs implement the unique value designed into customer products by producing custom semiconductor designs that allow customers to take advantage of perceived market opportunities in a timely manner. The customized solutions offered by ASICs combine the power of personalized electronics and the advantage of increased system efficiency.

CMOS technology has long been chosen for ASIC applications because of its low power and high density characteristics. Advancing process technology and new production and fabrication techniques have now allowed device speed to increase to the point where it is competitive with bipolar devices. Fujitsu manufactures CMOS gate arrays with advanced silicon gate technology utilizing two-layer and three-layer metal. This fabrication process yields parts that:

- a. require very low power dissipation (typically less than 500 mW per channeled array)
- b. operate at speeds equaling existing bipolar technologies
- c. feature higher gate densities than competing bipolar devices
- d. use a single power supply of 5 volts or less
- e. provide top-grade noise immunity and programmable logic levels compatible with TTL and CMOS logic families

#### 1.3 CMOS Gate Array Structure

Fujitsu CMOS gate arrays are configured in a matrix of basic cells in the center of the chip with input/output (I/O) cells on the device periphery. One basic cell is equivalent to a two-input NAND gate and is the physical building block used to construct the unit cells that perform specific logic functions. The custom logic function is realized by interconnecting basic cells with double- or triple-layer metallization. Fujitsu's CMOS gate array products are fabricated using a twin-tub polysilicon process to produce high-speed, high-density arrays consisting of 300 to 100,000 basic cells.

#### 1.3.1 Process Technology

The process by which the gate array is manufactured varies somewhat among Fujitsu's CMOS technologies; however, the following explanation provides a good model of how a basic cell is fabricated

in any of the CMOS families. The basic cell is constructed from an N-type silicon substrate upon which a P-well is deposited. The surface of the substrate is then covered with a thin layer of silicon dioxide (glass) and two strips of polysilicon are deposited perpendicular to the P-well and geometrically parallel. (Polysilicon is a silicon-based compound chemically altered so that it has good electrical conduction properties.) The polysilicon strips serve as the gate control elements of the basic cell and also as the two electrical interconnections between the sources of the P and N transistor pairs. See Figure 1–1.

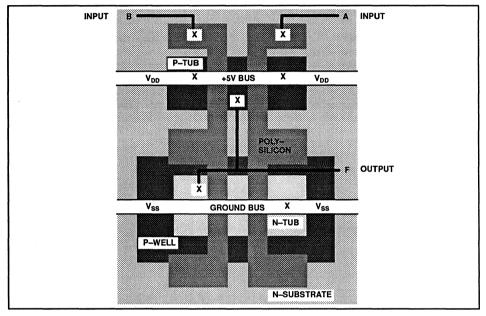


Figure 1-1. Physical Construction of the Unit Cell NAND Gate

The silicon dioxide layer is then stripped away from all areas of the substrate not protected by polysilicon. In two separate steps, the N-type and the P-type material of the twin tubs is diffused onto the substrate.

For the next step, N-type material is diffused or implanted into the P-well that was previously laid down. It straddles the two strips of polysilicon close to their ends. The polysilicon resists the diffusion, which results in the formation of three pads of N-type material separated by the two strips of polysilicon (self-aligned processing). The center pad of N-type material serves as a common drain terminal for both N-channel transistors. The outer pads are the separate source elements.

Then the P-type material is deposited on the N-type substrate straddling the two polysilicon strips. Similarly the center pad of P-type material forms the common source connection for both P-channel transistors. Figure 1–2 diagrams the structure of a basic cell before the custom metallization is applied. The basic cell is then converted to a unit cell by application of a custom metallization pattern that connects (or wires) various points of the basic cell, or a number of basic cells, together. Figure 1–3 diagrams the structure of a basic cell configured as a NAND gate after metallization (represented by the solid bold line connections) has been laid down.

Some unit cells require two or even three layers of metal to be applied. Such layers are separated by an insulating layer of silicon dioxide. Interconnections between the metal layers are made by means of "vias" passing through the glass.

#### 1.3.2 The Basic Cell

The basic cell of Fujitsu's CMOS gate array is a common building block consisting of one pair of P-channel and one pair of N-channel MOS transistors interconnected as shown in Figure 1–2.

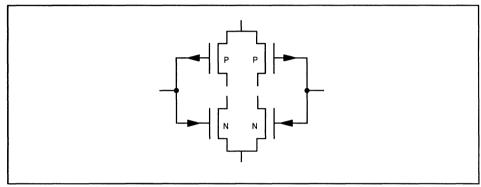


Figure 1-2. The Basic Cell

Since this is a "generic" basic cell, no connections are shown to the power supply (+5 volts), to ground, or to the two common control gate terminals of the circuit. These connections are made as required during the metallization phase of the manufacturing process. All CMOS gate arrays are built up of basic cells.

Figure 1–3 shows a schematic representation of the basic cell with the addition of the custom metallization required to convert the generic basic cell into a 2-input NAND gate.

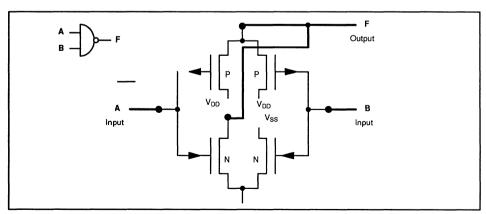


Figure 1-3. The Basic Cell Configured as a 2-Input NAND Gate

#### 1.3.3 Basic Cell Arrangement

Basic cells can be arranged as:

- a. Fundamental logic function units called unit cells (for example, NAND gates, flip-flops, etc.).
- User macros, which are composed of unit cells to form higher level logic block functions (e.g., shift register or decoder). Such blocks are user-defined and may contain any unit cell configuration.
- SuperMacros, which are very high level organizations performing complex functions such as ALUs and programmable timers, as well as CRT, SCSI, and Ethernet controllers.

#### 1.3.4 I/O Cells

I/O cells are a specially configured type of unit cells which serve as input/output buffer cells and are located on the periphery of the basic cell matrix. I/O cells are usually not included in the basic cell count. These buffer cells convert external voltage levels into internal CMOS levels. The output buffers provide a sufficient voltage level to drive TTL components but the input buffers must convert TTL levels to CMOS levels when appropriate. Figure 1–4 shows the structure of a typical input buffer (I2B) and Figure 1–5 shows the structure of a typical output buffer (O2B).

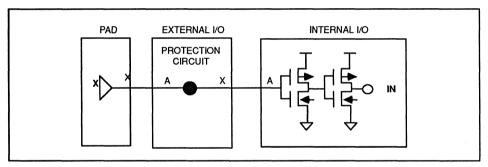


Figure 1-4. Input Buffer (I2B)

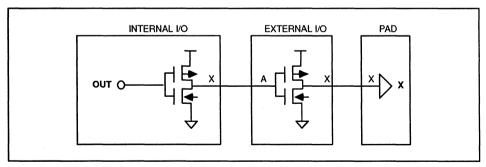


Figure 1-5. Output Buffer (O2B)

#### 1.3.5 User Macros

Different user macros are available for each technology group. For a list of available user macros for each technology, contact any of the Fuiltsu Technical Resource Centers listed in the back of this volume.

#### 1.3.6 Supermacro Implementations for CMOS ASIC

Fujitsu's next step upward in ASIC functionality is embodied in the concept of SuperMacros. SuperMacros are large functional organizations implemented as an integral part of a chip. SuperMacros can be large-scale compiled cells or core cells, as well as generic or proprietary LSI functions. Reduction of board space, reduction of cost, and reduction of design cycle time, as well as extended functionality, reliability, performance, and security of design are all advantages of SuperMacros. Since SuperMacros are not bound to a particular CMOS technology, they may be migrated from one CMOS technology to another.

Fujitsu provides customers with gate and behavioral level models, macro symbols, and data sheets/specifications as well as kit parts in order to provide complete support from development to system integration. The SuperMacros listed in Table 1-1 below are the first to be developed for Fujitsu's CMOS supermacro library.

Table 1-1. Fujitsu Supermacros

Function	Compatible Device	Technology	Gate Complexity
Universal Synchronous/Asynchronous Receiver/Transmitter (USART)	8251A	UHB/AU/CG10/21	2900
Universal Asynchronous Receiver/Transmitter (UART)	8868	UHB/AU/CG10/21	608
Programmable Interval Timer	8253	UHB/AU/CG10/21	5680
Programmable Peripheral Interface	8255A	UHB/AU/CG10/21	785 – 1403 <sup>1</sup>
Programmable Interrupt Controller	8259A	UHB/AU/CG10/21	2205
Programmable DMA Controller	8237	UHB/AU/CG10/21	5100
Clock Generator/Driver	8284	UHB/AU/CG10/21	99
Bus Controller	8288	UHB/AU/CG10/21	250
Programmable Interval Timer	8254	UHB/AU/CG10/21	3500
CRT Controller	6845	UHB/AU/CG10/21	2843
SCSI Protocol Controller <sup>2</sup>	87030	UHB/AU/CG10/21	3630
EtherNet Controller <sup>2</sup>	87012	UHB/AU/CG10/21	4233
First In First Out (FIFO)	N/A <sup>3</sup>	UHB/AU/CG10/21	360
4-bit Arithmetic Logic Unit (ALU) Slice	2901	UHB/AU/CG10/21	917
Carry Lookahead	2902	UHB/AU/CG10/21	33
Status and Shift Control	2904	UHB/AU/CG10/21	449
4-bit Microprogram Sequencer	2909	UHB/AU/CG10/21	428
12-bit Microprogram Controller	2910	UHB/AU/CG10/21	1682

Several options are available (Mode 0 is 785 gates)

<sup>3</sup>Not Applicable

<sup>&</sup>lt;sup>2</sup>Full-featured Fujitsu proprietary supermacro

#### 1.3.7 Structure of the Chip

The arrangement of the basic cells on the chip differs according to the technology. The fundamental chip layout is a matrix of basic cells surrounded by a perimeter of I/O cells. Basic cells are arranged in double columns in the UHB and CG10 technologies (Figure 1–6). The channelless or sea-of-gates technologies are constructed with no wiring channels between the double columns, allowing the wiring to go over the cells, rather than between the cells (Figure 1–7). The channelless technologies are covered in a separate data book.

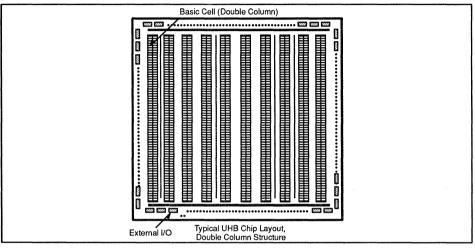


Figure 1-6. Channeled Gate Array Chip Structure

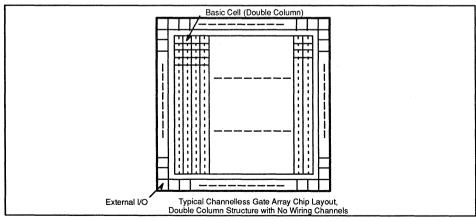


Figure 1-7. Channelless Gate Array Chip Structure

#### 1.4 Fujitsu's CMOS Channeled Gate Array Technologies

Fujitsu offers over 30 different CMOS gate array devices, fabricated with advanced silicon gate technology. Fujitsu's channeled CMOS gate arrays include the technology options described in detail in the data sheets that follow:

- UHB Series CMOS Gate Arrays
- CG10 Series CMOS Gate Arrays

Complete information on Fujitsu's channelless (sea-of-gates) CMOS gate array families is provided in a separate data book.

All offer the same fast turnaround on design, simplified customer interface, full support by Fujitsu ViewCAD system design software if requested, full design support on other major CAE workstations, and a wide variety of packaging options.

The number of gates in relationship to the processing speed of each new CMOS technology is shown in Figure 1–8. Figure 1–9 shows in tabular form the equivalent gate count for each CMOS technology family.

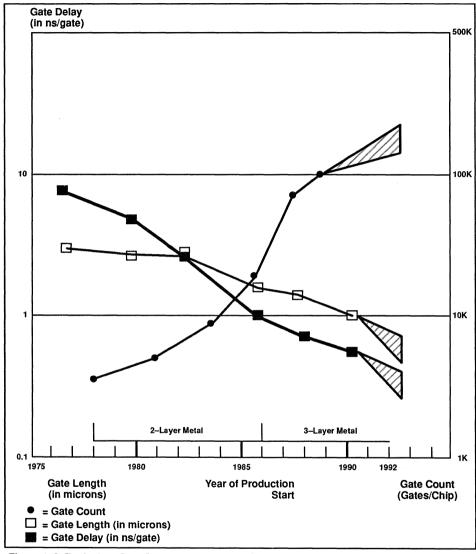


Figure 1–8. Equivalent Gate Count vs. Processing Speed, Fujitsu CMOS Gate Array Technologies



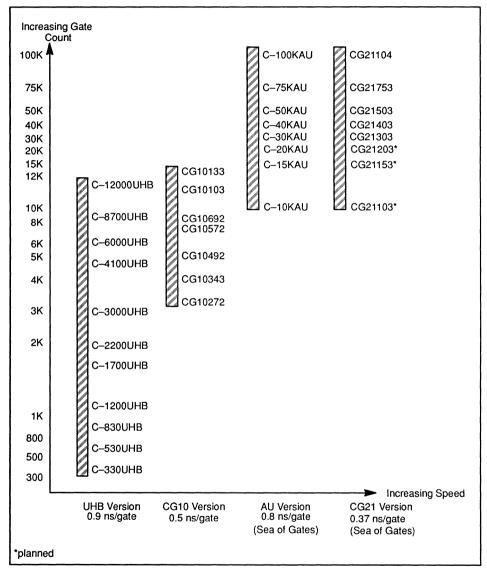


Figure 1-9. Equivalent Gate Count, Fujitsu CMOS ASIC Technology Families

1

UHB Series 1.5-micron CMOS Gate Arrays

# DESCRIPTION

The UHB series of 1.5-micron CMOS gate arrays is a highly integrated low-power, ultra high-speed product family that derives its enhanced performance and increased user flexibility from the use of a system-proven, dual-column gate structure and 2-layer metal interconnect technology. The unique dual-column gate structure increases density and speed performance, as well as gate utilization.

Internal high-drive clock buffers minimize clock skew across the chip while internal bus performance and integrity is assured by incorporating 3-state transmission gate logic underneath the routing channels. The high-drive output buffers provide highly symmetrical output waveforms.

#### **FEATURES**

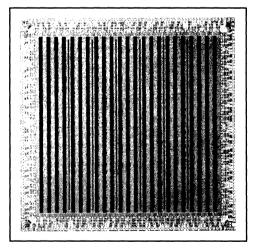
- High-density silicon gate CMOS technology
  - 330 to 12,000 usable gates
  - 90% maximum utilization fully autorouted
- Ultra high speed
  - typical 0.9 ns gate delay
  - narrow delay variation
  - High sink current capability
    - 3.2 mA, 8 mA, 12 mA, and 24 mA options available
    - selectable edge rate control
- Low-skew clock signal distribution
  - High-performance clock drivers
  - Hierarchical clock distributionFrequency-dependent clock routing
- Automatic test pattern generation for 6K gates and up
  - complete family of scan design macros available

•	2-column gate structure that enhances macro
	performance

- High-performance internal 3-state bus
  - buried cells within the routing channels ensure high density and reliable performance
- Proven 1.5-micron 2-layer metal technology
- · Highest pin-to-gate count commercially available
  - 60 logic I/O for 336 gates
  - 222 logic I/O for 1200 gates
- Input buffers with pull-up/pull-down resistance
- · Built-in feedback resistors for oscillators
- User-defined hierarchy-driven placement

Device Name	Utilizable Gates <sup>1</sup>	Maximum Signal Pins <sup>2</sup>
C-330UHB	336 gates	60
C-530UHB	530 gates	66
C-830UHB	830 gates	76
C-1200UHB	1233 gates	92
C-1700UHB	1724 gates	108
C-2200UHB	2220 gates	123
C-3000UHB	3066 gates	148
C-4100UHB	4174 gates	163
C-6000UHB	6000 gates	163
C-8700UHB	8768 gates	188
C-12000UHB	12734 gates	220

Gates available for logic (exclusive of I/O usage). 
'Maximum signal pin numbers depend on the output drive requirements and the package selected.



#### PRODUCT FAMILY DESCRIPTIONS<sup>1</sup>

Device Name Part Number		2-Input Gate Equivalent Complexity Maximum Sig		Total Number of Basic Cells on Chip <sup>3,4</sup>
C-330UHB	MB625xxx	336 gates	60	610 gates
C-530UHB	MB624xxx	530 gates	66	840 gates
C-830UHB	MB623xxx	830 gates	76	1176 gates
C-1200UHB	MB622xxx	1233 gates	92	1680 gates
C-1700UHB	MB621xxx	1724 gates	108	2232 gates
C-2200UHB	MB620xxx	2220 gates	123	2800 gates
C-3000UHB	MB606xxx	3066 gates	148	3744 gates
C-4100UHB	MB605xxx	4174 gates	163	4888 gates
C-6000UHB	MB604xxx	6000 gates	163	6976 gates
C-8700UHB	MB603xxx	8768 gates	188	9720 gates
C-12000UHB	MB602xxx	12734 gates	220	13728 gates

Notes: <sup>1</sup>Typical device gate speed, with F/O = 2, for a 2-input NAND gate, is 0.9 ns.

#### **AC CHARACTERISTICS**

#### **BEST/WORST CASE MULTIPLIERS FOR PROPAGATION DELAYS**

Propagation delays characteristic of a gate array are a function of several factors, including operating temperature, supply voltage, fanout loading, interconnection routing metal, process variation, input transition time, and input signal polarity. Temperature and supply voltage factors affecting propagation delays in the UHB CMOS family of gate arrays are given in the table below.

		Pre-Layout	Simulation		Post-Layout Simulation				
Temperature Range	V <sub>DD</sub> =	5 V ±5%	V <sub>DD</sub> = 5	V <sub>DD</sub> = 5 V ±10%		V <sub>DD</sub> = 5 V ±5%		V <sub>DD</sub> = 5 V ±10%	
	Best Case	Worst Case	Best Case	Worst Case	Best Case	Worst Case	Best Case	Worst Case	
0 - 70°C1	0.35	1.65	0.30	1.75	0.40	1.60	0.35	1.70	
–20 – 70°C	0.35	1.65	0.25	1.75	0.35	1.60	0.30	1.70	
-40 - 70°C	0.25	1.65	0.20	1.75	0.30	1.60	0.25	1.70	
-40 - 85°C2	0.25	1.75	0.20	1.85	0.30	1.70	0.25	1.80	

Notes: <sup>1</sup>Commercial temperature range <sup>2</sup>Industrial temperature range

<sup>&</sup>lt;sup>2</sup>The maximum signal pin numbers depend on the output drive requirements and the package selection.

<sup>&</sup>lt;sup>3</sup>A basic cell is equivalent to a 2-input gate.

<sup>&</sup>lt;sup>4</sup>Basic cells on chip are also used for I/O buffer function.

#### REPRESENTATIVE PROPAGATION DELAYS

Constants for calculating the delays due to process variation, fanout loading, interconnection routing metal, transition time, and signal polarity are given for each unit cell in the UHB Unit Cell Library. Delays using these factors are calculated for a representative selection of unit cells and are shown in the Propagation Delays tables below.

Calculations are representative of unit cells in the C12000UHB (UHB 12000-Gate CMOS gate array).

Typical values are indicated. Worst case multipliers are applied to typical values. Smaller arrays can exhibit significantly greater speed.

	T	<u> </u>			Propa	gation De	elays (in r	ıs)	
Unit Cell Function		Equivalent Gate Count			N <sub>DI</sub> (Fan-				
1 4.104.0				1	2	4	8	16	32
Inverter	V1N	1	t <sub>PLH</sub> t <sub>PHL</sub>	0.86 0.67	1.51 1.04	2.36 1.52	3.53 2.18	5.19 3.11	8.09 4.74
Power 2-Input NAND	N2K	2	t <sub>PLH</sub>	0.66 0.68	.99 .97	1.41 1.34	1.99 1.85	2.83 2.58	4.27 3.85
Power 16-Input NAND	NGB	11	t <sub>PLH</sub>	1.82 3.69	2.15 3.93	2.57 4.25	3.15 4.69	3.99 5.31	5.43 6.40
Power 2-Input NOR	R2K	2	t <sub>PLH</sub>	0.95 0.67	1.53 0.91	2.27 1.23	3.29 1.67	4.75 2.29	7.28 3.38
Power Exclusive OR	X2B	4	t <sub>PLH</sub>	1.72 1.82	2.05 2.03	2.47 2.29	3.05 2.66	3.89 3.18	5.33 4.08
3-wide 2-AND 6-Input AND-OR Inverter (A $\rightarrow$ Y)	D36	3	t <sub>PLH</sub> t <sub>PHL</sub>	1.78 1.22	2.93 1.80	4.41 2.54	6.45 3.56	9.37 5.02	4.43 7.55
2-wide 2-OR 4-input OR-AND-Inverter (A → X)	G24	2	t <sub>PLH</sub> t <sub>PHL</sub>	1.54 1.20	2.73 1.78	4.27 2.52	6.39 3.54	9.40 5.00	14.65 7.53
Power 2-AND 8-Wide Multiplexer (A → X)	T28	11	t <sub>PLH</sub> t <sub>PHL</sub>	2.41 1.66	2.74 1.83	3.16 2.04	3.74 2.33	4.58 2.75	6.02 3.47
Power Clock Buffer	K2B	3	t <sub>PLH</sub>	1.30 1.38	1.57 1.58	1.90 1.83	2.30 2.13	2.81 2.51	3.61 3.11
Scan 8-bit D Flip-flop with Clock Inhibit and 3:1 Data Multiplexer (CK,IH → Q)	SHK	88	t <sub>PLH</sub> t <sub>PHL</sub>	5.22 4.92	5.87 5.29	6.72 5.77	7.89 6.43	9.55 7.36	12.45 8.99
Non–Scan D Flip-flop with Reset (CK → Q)	FDO	7	t <sub>PLH</sub> t <sub>PHL</sub>	2.51 2.14	3.16 2.55	4.01 3.08	5.18 3.81	6.84 4.85	9.74 6.66
Non-Scan Power D Flip-flop with Clear (CK → Q)	FD5	8	t <sub>PLH</sub> t <sub>PHL</sub>	2.17 1.89	2.50 2.10	2.92 2.36	3.50 2.73	4.34 3.25	5.78 4.15
Non-Scan 4-bit Binary Synchronous Up Counter (CI → CO)	C43	48	t <sub>PLH</sub> t <sub>PHL</sub>	2.18 1.10	2.83 1.43	3.68 1.85	4.85 2.43	6.51 3.27	9.41 4.71
Non-Scan 4-bit Binary Synchronous Up Counter (CI → CO)	C45	48	t <sub>PLH</sub> t <sub>PHL</sub>	2.52 1.68	3.22 2.05	4.12 2.53	5.36 3.19	7.13 4.12	10.21 5.75

Note: Delays for inter-block wiring are not included

Continued on next page

## **UHB Series CMOS Gate Arrays**

## REPRESENTATIVE PROPAGATION DELAYS (Continued)

	T	I <u>.</u>			Propag	gation De	lays (in r	18)	
Unit Cell Function	Unit Cell Name	Equivalent Gate Count	uivalent Input te Count Transition			N <sub>DI</sub> (Fan-	out)		
				1	2	4	8	16	32
Non-Scan 4-bit Binary Synchronous Up/Down Counter (DU → CO)	C47	68	t <sub>PLH</sub> t <sub>PHL</sub>	2.87 3.30	3.32 3.63	3.90 4.05	4.70 4.63	5.85 5.47	7.84 6.91
4-bit Binary Full Adder with Fast Carry (CI → S1)	A4H	48	t <sub>PLH</sub> t <sub>PHL</sub>	1.97 2.13	2.87 2.71	4.04 3.45	5.65 4.47	7.93 5.93	11.92 8.46
4:1 Selector (S5 → X)	T5A	5	t <sub>PLH</sub> t <sub>PHL</sub>	1.39 1.12	2.33 1.77	3.55 2.62	5.23 3.79	7.62 5.45	11.79 8.35
4-bit Shift Register with Synchronous Load	FS2	30	t <sub>PLH</sub> t <sub>PHL</sub>	2.90 3.46	3.55 3.83	4.40 4.31	5.57 4.97	7.23 5.90	10.13 7.53
9-bit Odd Parity Generator/Checker	PO9	22	t <sub>PLH</sub> t <sub>PHL</sub>	5.78 6.00	6.43 6.33	7.28 6.75	8.45 7.33	10.11 8.17	13.01 9.61
4-wide 2:1 Data Selector (A $\rightarrow$ X)	P24	12	t <sub>PLH</sub> t <sub>PHL</sub>	1.24 0.97	1.57 1.14	1.99 1.35	2.57 1.64	3.41 2.06	4.85 2.78
4-bit Magnitude Comparator (IS → OG)	MC4	42	t <sub>PLH</sub> t <sub>PHL</sub>	3.17 2.60	4.36 2.93	5.90 3.35	8.02 3.93	11.03 4.77	16.28 6.21
4-bit Bus Driver (A → X)	B41	9	t <sub>PLH</sub> t <sub>PHL</sub>	1.99 1.87	2.48 2.29	3.05 2.78	3.76 3.39	4.64 4.14	6.04 5.34
Input Buffer (Inverter)	I1B	5	t <sub>PLH</sub> t <sub>PHL</sub>	1.84 1.78	2.11 2.05	2.44 2.38	2.84 2.78	3.35 3.29	4.15 4.09
Clock Input Buffer (Inverter)	IKB	4	t <sub>PLH</sub> t <sub>PHL</sub>	2.49 1.94	2.63 2.08	2.79 2.24	2.99 2.44	3.24 2.69	3.64 3.09

I/O Cell	Unit Cell	Equivalent	Input		Output Buffer Load in pF				
Function	Name	Gate Count Transition	12	25	50	100	200	400	
Output Buffer (True)	O2B	2	t <sub>PLH</sub> t <sub>PHL</sub>	2.37 3.24	3.10 4.85	4.50 7.95	7.30 14.15	12.90 26.55	24.10 51.35
Power Output Buffer (True)	O2L	2	t <sub>PLH</sub> t <sub>PHL</sub>	2.53 2.47	3.02 3.01	3.94 4.03	5.79 6.08	9.49 10.18	16.89 18.38
3-State Output Buffer (True)	O4T	4	t <sub>PLH</sub> t <sub>PHL</sub>	3.09 4.08	3.82 5.77	5.22 9.02	8.02 15.52	13.62 28.52	24.82 54.52
Power 3-State Output Buffer (True)	O4W	4	t <sub>PLH</sub> t <sub>PHL</sub>	3.48 4.68	3/97 5.30	4.92 6.47	6.82 8.82	10.62 13.52	18.22 22.92
3-State Output and Input Buffer (True)	H6T	8	t <sub>PLH</sub> t <sub>PHL</sub>	3.09 4.08	3.82 5.77	5.22 9.02	8.02 15.57	13.62 28.52	24.82 54.52
Power 3-State Output and Input Buffer (True)	H6W	8	t <sub>PLH</sub> t <sub>PHL</sub>	3.48 4.68	3.97 5.30	4.92 6.47	6.82 8.82	10.62 13.52	18.22 22.92

Note: Delays for inter-block wiring are not included

## **DC CHARACTERISTICS**

#### **ABSOLUTE MAXIMUM RATINGS**<sup>1</sup>

Rating		Symbol	Minimum	Maximum	Unit
Supply Voltage		V <sub>DD</sub>	V <sub>SS</sub> - 0.5 <sup>2</sup>	6.0	V
Input Voltage		$V_{i}$	V <sub>SS</sub> - 0.5 <sup>2</sup>	V <sub>DD</sub> +0.5	V
Output Voltage		Vo	V <sub>SS</sub> - 0.5 <sup>2</sup>	V <sub>DD</sub> +0.5	V
	$I_{OL} = 3.2 \text{ mA}$		-40		
Output Current <sup>3</sup>	$I_{OL} = 8 \text{ mA}$	l <sub>os</sub>	-40		
Output Gurrent	I <sub>OL</sub> = 12 mA		-60	1	mA
	I <sub>OL</sub> = 24 mA		-90		
Storage Temperature	Ceramic Plastic	T <sub>stg</sub>	65 40	+150 +125	5C
Temperature Under Bias	Ceramic Plastic	T <sub>bias</sub>	-40 -25	+125 +85	5C

Notes: ¹Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
²V<sub>SS</sub> = 0 V.

#### RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage	$V_{DD}$	4.75	5.0	5.25	V
Input High Voltage for TTL Input	V <sub>IH</sub>	2.2	_	-	V
Input Low Voltage for TTL Input	V <sub>IL</sub>	-	_	0.8	V
Input High Voltage for CMOS Input	VIH	V <sub>DD</sub> x 0.7	_	_	V
Input Low Voltage for CMOS Input	ViL	_	-	V <sub>DD</sub> x 0.3	٧
Operating Temperature	T <sub>A</sub>	0	_	70	°C

## **CAPACITANCE** ( $T_A = 25^{\circ}C$ , $V_{DD} = V_I = 0$ V, f = 1 MHz)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input Pin Capacitance	C <sub>IN</sub>			16	pF
Output Pin Capacitance (I <sub>OL</sub> – 3.2 mA, 8 mA, or 12 mA)	C <sub>OUT</sub>		_	16	pF
Output Pin Capacitance (I <sub>OL</sub> – 24 mA)	C <sub>OUT</sub>		_	18	pF
I/O Pin Capacitance (I <sub>OL</sub> – 3.2 mA, 8 mA, or 12 mA)	C <sub>I/O</sub>		_	16	pF
I/O Pin Capacitance (I <sub>OL</sub> – 24 mA)	C <sub>I/O</sub>		_	23	pF

<sup>&</sup>lt;sup>3</sup>Only one output at a time may be shorted for more than one second.

#### **DC CHARACTERISTICS**

(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Power Supply Current	I <sub>DDS</sub>	Steady State <sup>1</sup>	0		100	μΑ
Output High Voltage for Normal Output (I <sub>OL</sub> = 3.2 mA)	V <sub>OH</sub>	I <sub>OH</sub> = -2 mA	4.0	_	V <sub>DD</sub>	٧
Output High Voltage for Driver Output (I <sub>OL</sub> = 8 mA)	V <sub>OH</sub>	I <sub>OH</sub> = -2 mA	4.0	-	V <sub>DD</sub>	٧
Output High Voltagefor Driver Output (I <sub>OL</sub> =12 mA)	V <sub>OH</sub>	l <sub>OH</sub> = -4 mA	4.0	-	V <sub>DD</sub>	٧
Output High Voltage for Driver Output (I <sub>OL</sub> =24 mA)	V <sub>OH</sub>	I <sub>OH</sub> = -8 mA	4.0	_	V <sub>DD</sub>	٧
Output Low Voltage <sup>2</sup> for Normal Output (I <sub>OL</sub> = 3.2 mA)	V <sub>OL</sub>	I <sub>OL</sub> = 3.2 mA	V <sub>SS</sub>		0.4	٧
Output Low Voltage for Driver Output (I <sub>OL</sub> = 8 mA)	V <sub>OL</sub>	I <sub>OL</sub> = 8 mA	V <sub>SS</sub>	_	0.4	٧
Output Low Voltage <sup>2</sup> for Driver Output (I <sub>OL</sub> = 12 mA)	V <sub>OL</sub>	I <sub>OL</sub> = 12 mA	V <sub>SS</sub>	_	0.4	V
Output Low Voltage <sup>2</sup> for Driver Output (I <sub>OL</sub> = 24 mA)	V <sub>OL</sub>	I <sub>OL</sub> = 24 mA	V <sub>SS</sub>	_	0.5	V
Input High Voltage for TTL Input	VIH		2.2	_	_	V
Input Low Voltage for TTL Input	V <sub>IL</sub>		_	_	0.8	V
Input High Voltage for CMOS Input	V <sub>IH</sub>	_	V <sub>DD</sub> x 0.7	_	_	V
Input Low Voltage for CMOS Input	V <sub>IL</sub>		_	_	V <sub>DD</sub> x 0.3	V
Schmitt Trigger CMOS Input <sup>3</sup> Positive-going Threshold Negative-going Threshold Hysteresis	V <sub>T+</sub> V <sub>T-</sub> V <sub>T+</sub> -V <sub>T_</sub>	$V_{\text{IL}}$ to $V_{\text{IH}}$ , $V_{\text{IH}}$ , to $V_{\text{IL}}$	2.5 0.7 1.1	3.3 1.4 1.9	4.0 2.0 2.7	> > >
Schmitt Trigger TTL Input <sup>3</sup> Positive-going Threshold Negative-going Threshold Hysteresis	V <sub>T+</sub> V <sub>T-</sub> V <sub>T+</sub> -V <sub>T_</sub>	  V <sub>IL</sub> to V <sub>IH</sub> , V <sub>IH</sub> , to V <sub>IL</sub>	1.4 0.8 0.4	1.9 1.3 0.6	2.5 1.8 0.7	>>>
Input Pull-up/Pull-down Resistor	R₽	V <sub>IH</sub> to V <sub>DD</sub> V <sub>IL</sub> to V <sub>SS</sub>	25	50	100	kΩ
Input Leakage Current	l <sub>Li</sub>	$V_i = 0 - V_{DD}$	-10		10	μА
Input Leakage Current (3-state)	l <sub>LZ</sub>	$V_i = 0 - V_{DD}$	-10		10	μΑ

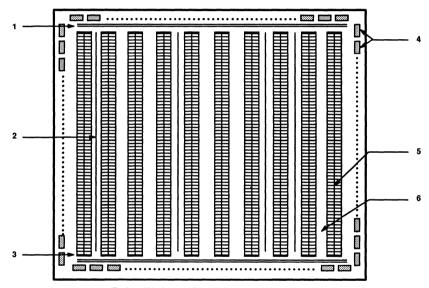
Notes:  $^{1}V_{\text{IN}} = V_{\text{DD}}, V_{\text{IL}} = V_{\text{SS}}$   $^{2}$ With certain restrictions on pin assignment  $^{3}$ These values for reference only

#### **ARRAY ARCHITECTURE**

The typical UHB chip is composed of double columns of CMOS gates (basic cells) separated by dedicated wiring channels. A basic cell consists of a pair of N-channel and a pair of P-channel transistors interconnected by polysilicon gate control terminals. Groups of basic cells are interconnected by custom metallization into unit cells. Fujitsu unit cells provide a wide range of standard logic functions such as exclusive OR gates, flip-flops, buffers, and counters. The UHB Series CMOS gate array family includes over 250 different unit cells. These unit cells are the building blocks from which complex designs are constructed.

The spaces between the double columns of basic cells are occupied by channels for custom metallization. Nearly half of these wiring channels contain transmission gates that implement internal 3-state buses. Bus terminators located at the ends of the double columns of cells maintain the last value to be sent through the bus to ensure proper operation under all conditions.

The I/O cells around the perimeter of the matrix of cells are composed of internal cells with input protection networks and the potential to be configured as input buffers, clock input buffers, output buffers, power output buffers, or bidirectional buffers.



Typical Chip Layout, Double Column Structure

- 1. Dedicated Clock Network for high frequency clocks
- 2. 3-state Bus Logic located in wiring channels
- 3. Bus Terminators prevent floating state on buses
- 4. Driver Transistors and I/O Protection Networks provide high I/O count
- 5. Double Columns for optional macro utilization and speed
- 6. Wiring Channel Area for metallization between unit cells

#### **DESIGN COMPONENTS**

#### **DESIGNING WITH THE UHB PRODUCT FAMILY**

To implement logic functions, you build up the elements of the circuit from unit cells. Simple unit cells are used hierarchically to build higher level functions until the logic is completely defined. Fujitsu offers a complete line of standard logic functions in the unit cell library.

Super macros are used to implement large super-cell functions such as expandable ALUs and multipliers.

#### I/O BUFFERS

Each UHB I/O buffer around the perimeter of the array consists of an input protection network and large N-channel and P-channel transistors capable of supplying the standard 3.2-mA, 8-mA, and 12-mA output currents. Two of these large transistor pairs may be connected in parallel, using high-output-current macros, to obtain 24-mA drive. One of the I/O pads whose output transistors have been used for the 24-mA high-current option may still be used as an input.

Input I/O buffers convert external TTL levels to internal CMOS levels or may receive CMOS level signals directly. Output I/O buffers are totem pole and may drive either CMOS and TTL levels, depending on their AC and DC loads. Any of the pins except the dedicated power and ground pads can be designed to be an input buffer, an input buffer with pull-up/pull-down resistance, a clock input buffer, an output buffer, a high-drive output buffer, an output buffer with noise limiting resistance, a 3-state output buffer, a bi-directional buffer, or a Schmitt trigger input buffer. There are some restrictions on the location of 24-mA buffers.

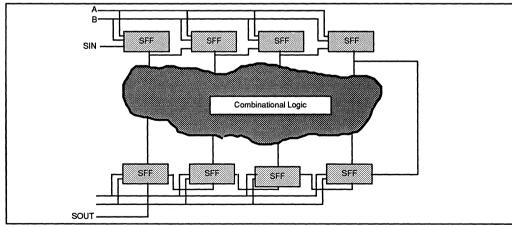
#### INPUT CLOCK DRIVERS

The large output I/O transistor pair is used in a high-drive input clock driver for high fanout applications within the array. This allows you to fully utilize the high speed capabilities of the UHB technology.

#### **TESTING UHB DEVICES**

Two options are available for testing UHB designs: (1) the standard designer-supplied test patterns and test vectors (in Fujitsu's FTDL format) and (2) the use of scan cells combined with Automatic Test Generation (ATG) performed by Fujitsu computers for additional diagnostic test patterns. If you have designed with scan cells and other scan logic elements, Fujitsu will complete the scan test program generation.

Regardless of the selected test option, you need to furnish Fujitsu with enough test patterns to guarantee that the submitted design completely performs its intended logic functions. These patterns include the test function of each I/O pin.



Diagramatic Representation of Design Structure for ScanTesting

## **VDD** and **VSS** REQUIREMENTS

Each UHB Series gate array device has two options for each package type, both supporting a different number of power and ground pins. The number of power and ground pins required depends on the number of simultaneously switching outputs used in the design. Simultaneously switching outputs (SSOs) are output signals that change from H to L or L to H or from Z to H or Z to L within a 20-ns window (including possible skew).

Multiple outputs that switch at the same time can cause noise on Vop and Vss lines and affect the performance of a device. Therefore, to achieve maximum reliability, Fujitsu limits the number of SSOs per Vop pin according to the table below. The maximum number of SSOs per pin is determined by a representative value specified for the driving capability of each type of output. The total representative value of all SSOs used in a design must not exceed 80 per Vss pin. For example, 11 normal 3.2-mA outputs with edge rate control, four 12-mA outputs, or three 24-mA outputs per Vss pin may be SSOs.

Output Drive Type	Representative Value per Output
Normal (3.2 mA)	10
High Drive (12 mA)	20
Normal (3.2 mA) with Edge Rate Control	7
High Drive (12 mA) with Edge Rate Control	14
High Drive (24 mA) with Edge Rate Control	26

## **UHB Series CMOS Gate Arrays**

## **FUNCTIONAL INDEX OF UNIT CELL LIBRARY**

Note: The load unit (lu) is a normalized loading unit of capacitance representing the input load of an inverter without metal interconnection.

nverter and Buffe	r Family			
Unit Cell Name	Description	Basic Cells	Drive (lu)	Polarity
V1N	Inverter	1	18	Neg
V2B	Power Inverter	1	36	Neg
B1N	True Buffer	. 1	18	Pos
BD3	True Delay Buffer (> 5 ns)	5	18	Pos
BD4	Delay Cell (> 4 ns)	4	6	Pos
BD5	Delay Cell (>10 ns)	9	18	Pos
BD6	Delay Cell (>22 ns)	17	18	Pos

Clock Buffer Fami	ly			
Unit Cell Name	Description	Basic Cells	Drive (lu)	Polarity
K1B	True Clock Buffer	2	36	Pos
K2B	Power Clock Buffer	3	55	Pos
КЗВ	Gated Clock (AND) Buffer	2	36	Pos
K4B	Gated Clock (OR) Buffer	2	36	Pos
K5B	Gated Clock (NAND) Buffer	3	36	Neg
KAB	Block Clock (OR) Buffer	3	55	Pos
KBB	Block Clock (OR x 10) Buffer	30	55	Pos
V1L	Double Power Inverter	2	55	Neg

AND Family			
Unit Cell Name	Description	Basic Cells	Drive (lu)
N2N	2-input NAND	1	18
N2B	Power 2-input NAND	3	36
N2K	Fast Power 2-input NAND	2	36
N3N	3-input NAND	2	14
N3B	Power 3-input NAND	3	36
N4N	4-input NAND	2	10
N4B	Power 4-input NAND	4	36
N6B	Power 6-input NAND	5	36
N8B	Power 8-input NAND	6	36
N9B	Power 9-input NAND	8	36
NCB	Power 12-input NAND	10	36
NGB	Power 16-input NAND	11	36
N3K	Fast Power 3-input NAND	3	28
N4K	Fast Power 4-input NAND	4	20

Continued on next page

## FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

R Family			
Unit Cell Name	Description	Basic Cells	Drive (lu)
R2N	2-input NOR	1	14
R2B	Power 2-input NOR	3	36
R2K	Power 2-input NOR	2	36
R3N	3-input NOR	2	10
R3B	Power 3-input NOR	3	36
R3K	Power 3-input NOR	3	20
R4N	4-input NOR	2	6
R4B	Power 4-input NOR	4	36
R4K	Power 4-input NOR	4	12
R6B	Power 6-input NOR	5	36
R8B	Power 8-input NOR	6	36
R9B	Power 9-input NOR	8	36
RCB	Power 12-input NOR	10	36
RGB	Power 16-input NOR	11	36

AND Family				
Unit Cell Name	Description	Basic Cells	Drive (lu)	
N2P	Power 2-input AND	2	36	
N3P	Power 3-input AND	3	36	
N4P	Power 4-input AND	3	36	
N8P	Power 8-input AND	6	36	

OR Family				
Unit Cell Name	Description	Basic Cells	Drive (lu)	
R2P	Power 2-input OR	2	36	
R3P	Power 3-input OR	3	36	
R4P	Power 4-input OR	3	36	
R8P	Power 8input OR	6	36	

xclusive NOR/OI	R Family (EXOR/EXNOR)			
Unit Cell Name	Description	Basic Cells	Drive (lu)	Polarity
X1N	Exclusive NOR	3	18	Neg
X1B	Power Exclusive NOR	4	36	Neg
X2N	Exclusive OR	3	14	Pos
X2B	Power Exclusive OR	4	36	Neg
X3N	3-input Exclusive NOR	5	14	Neg
ХЗВ	Power 3-input Exclusive NOR	6	36	Neg
X4N	3-input Exclusive OR	5	14	Pos
X4B	Power 3-input Exclusive OR6	6	36	Pos

Continued on next page

## **UHB Series CMOS Gate Arrays**

## FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Unit Cell Name	Description	Basic Cells	Drive (lu)	
D23	2-wide 2-AND 3-input AOI	2	14	
D14	2-wide 3-AND 4-input AOI	2	14	
D24	2-wide 2-AND 4-input AOI	2	14	
D34	3-wide 2-AND 4-input AOI	2	10	
D36	3-wide 2-AND 6-input AOI	3	10	
D44	2-wide 2-OR 2-AND 4-input AOI	2	10	

Note: AND-OR-Inverter unit cells are useful in implementing sum-of-products (SOP) expressions

OR-AND-Inverter Family (OAI)							
Unit Cell Name	Description	Basic Cells	Drive (lu)				
G23	2-wide 2-OR 3-input OAI	2	18				
G14	2-wide 3-OR 4-input OAI	2	10				
G24	2-wide 2-OR 4-input OAI	2	10				
G34	3-wide 2-OR 4-input OAI	2	10				
G44	2-wide 2-AND 2-OR 4-input OAI	2	14				

Note: OR-AND-Inverter unit cells are useful in implementing product-of-sums (POS) expressions.

Multiplexer Far	nily				
Unit Cell Name	Type	Description	Basic Cells	Drive (lu)	Function
T24*	4:1	Power 2-AND 4-wide Multiplexer	6	36	SOP
T26*	6:1	Power 2-AND 6-wide Multiplexer	10	36	SOP
T28*	8:1	Power 2-AND 8-wide Multiplexer	11	36	SOP
T32	2:1	Power 3-AND 2-wide Multiplexer	5	36	SOP
T33*	3:1	Power 3-AND 3-wide Multiplexer	8	36	SOP
T34*	4:1	Power 3-AND 4-wide Multiplexer	9	36	SOP
T42	2:1	Power 4-AND 2-wide Multiplexer	6	36	SOP
T43	3:1	Power 3-AND 3-wide Multiplexer	10	36	SOP
T44	4:1	Power 4-AND 4-wide Multiplexer	11	36	SOP
T54	4:1	Power 4-2-3-2 AND 4-wide Multiplexer	10	36	SOP
U24*	4:1	Power 2-OR 4-wide Multiplexer	6	36	POS
U26*	6:1	Power 2-OR 6-wide Multiplexer	9	36	POS
U28*	8:1	Power 2-OR 8-wide Multiplexer	11	36	POS
U32	2:1	Power 3-OR 2-wide Multiplexer	5	36	POS
U33*	3:1	Power 3-OR 3-wide Multiplexer	7	36	POS
U34*	4:1	Power 3-OR 4-wide Multiplexer	9	36	POS
U42	2:1	Power 4-OR 2-wide Multiplexer	6	36	POS
U43	3:1	Power 4-OR 3-wide Multiplexer	9	36	POS
U44	4:1	Power 4-OR 4-wide Multiplexer	11	36	POS

\* Convenient for typical multiplexer applications

Unit Cell Name	Туре	Description	Basic Cells	Drive (lu)	Selects	Output	Bit Width
P24*	2:1	Data Selector	12	36	S, XS	Q	4
T2E	2:1	Selector	5	18	S	XQ	2
T2F	2:1	Selector	8	18	S	XQ	4
T2B*	2:1	Selector	2	18	S, XS	XQ	1
T2C*	2:1	Selector	4	18	S, XS	XQ	2
T2D*	2:1	Selector	2	14	S, XS	XQ	1
T5A*	4:1	Selector	5	9	S, XS	XQ	1
V3A*	1:2	Selector	2	14	S, XS	XQ	1
V3B*	1:2	Selector	4	14	S, XS	XQ	2

<sup>\*</sup> These are transmission gate devices whose outputs can be tied because they can be inhibited with true/inverted selects.

Decoders						
Unit Cell Name	Туре	Description	Basic Cells	Drive (lu)	Active Level Outputs	Output
DE2	2:4	Decoder	5	18	Low	_
DE3	3:8	Decoder	15	14	Low	
DE4	2:4	Decoder	8	14	Low	Low
DE6	3:8	Decoder	30	18	Low	1 High 2 Low

Internal Bus Unit C	ells				
Unit Cell Name	Description	Basic Cells	Drive (lu)	Bus Size	Enable
B41	4-bit Bus Driver	9	36	4 bits	Low

Notes: <sup>1</sup>The number of B41s used is limited by the chosen array series, as shown in the table below.

<sup>&</sup>lt;sup>2</sup>On-chip buses (managing more than one bus source and/or a bi-directional bus) may be implemented with either multiplexer-type unit cells or bus drivers. While bus drivers impose certain design restrictions, the optimum choice is dictated by the specific design.

Device Name	Maximum B41s
C-330UHB	4
C-530UHB	5
C-830UHB	6
C-1200UHB	8
C-1700UHB	12
C-2200UHB	16
C-3000UHB	21
C-4100UHB	26
C-6000UHB	50

## **UHB Series CMOS Gate Arrays**

# FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Unit Cell Name	Description	Basic Cells	Drive (lu)	Enable	Bits	Output	Clear
YL2	Data Latch with TM	5	36	High	1	Q	
YL4	Data Latch with TM	14	36	High	4	Q	_
LTK	Data Latch	4	18	Low	1	Q, XQ	Async
LTL	Data Latch with Clear	5	18	Low	1	Q, XQ	Async
LTM	Data Latch with Clear	16	18	Low	4	Q, XQ	
LT1	S-R Latch with Clear	4	18	Low	1	Q, XQ	Async
LT4	Data Latch	14	18	Low	4	Q, XQ	

Note: Y-type latches incorporate inhibit inputs and transparent mode (TM) to facilitate scan implementation.

Continued on next page

Scan Flip	p-flop Family (Positive-Edge Tri	ggered)						
Unit Cell Name	Description	Basic Cells	Drive (lu)	Bits	Output	Clear	Preset	Clock Inhibit
SDH*	Scan D Flip-flop with 2:1 Multiplex	14	36	1	Q, XQ	Async	_	Yes
SDJ*	Scan D Flip-flop with 4:1 Multiplex	15	36	1	Q, XQ	Async	_	Yes
SDK*	Scan D Flip-flop with 3:1 Multiplex	16	36	1	Q, XQ	Async	-	Yes
SJH	Scan J-K Flip-flop	16	36	1	Q, XQ	Async	_	Yes
SDD*	Scan DFlip-flop with 2:1 Multiplex	16	36	1	Q, XQ	Async	Async	Yes
SDA	Scan 1-input D Flip-flop	12	36	1	Q, XQ			Yes
SDB	Scan 1-input D Flip-flop	42	36	4	Q, XQ	_	_	Yes
SHA	Scan 1-input D Flip-flop	68	18	8	Q, XQ	_		Yes
SHB	Scan 1-input D Flip-flop	62	18	8	Q			Yes
SHC	Scan 1-input D Flip-flop	62	18	8	XQ	_		Yes
SHJ*	Scan D Flip-flop with 2:1 Multiplex	78	18	8	Q, XQ			Yes
SHK*	Scan D Flip-flop with 3:1 Multiplex	88	18	8	Q, XQ		_	Yes

Note: \* Indicates D Flip-flop with multiplexed inputs.

Non-Sca	n Filp-flop Family							
Unit Cell Name	Description	Basic Cells	Drive (lu)	Bits	Output	Clear	Preset	Clock Inhibit
FDM	D Flip-flop	6	18	1	Q, XQ	_	_	Pos
FDN	D Flip-flop with Set	7	18	1	Q, XQ	_	Async	Pos
FDO	D Flip-flop with Reset	7	18	1	Q, XQ	Async		Pos
FDP	D Flip-flop with Set and Reset	8	18	1	Q, XQ	Async	Async	Pos
FDQ	D Flip-flop	21	18	4	Q	_		Neg
FDR	D Flip-flop with Clear	26	18	4	Q	Async	_	Pos
FDS	D Flip-flop	20	18	4	Q		_	Pos
FD2	Power D Flip-flop	7	36	1	Q, XQ		_	Neg
FD3	Power D Flip-flop with Preset	8	36	1	Q, XQ	_	Async	Neg
FD4	Power D Flip-flop with Clear and Preset	9	36	1	Q, XQ	Async	Async	Neg
FD5	Power D Flip-flop with Clear	8	36	1	Q, XQ	Async	_	Neg
FJD	Positive Edge Clocked Power J-K Flip-flop with Clear	12	36	1	Q, XQ	Async		Pos

Note: Synchronous flip-flops my be constructed by adding a simple AND gate (such as N2P) to the input of a flip-flop to create a synchronous clear.

Binary	Counter Family		***************************************	**********		***************************************				
Unit Cell Name	Description	Basic Cells	Drive (lu)	Bits	Outputs <sup>1</sup>	Load	Clear	Enable	Carry In	Up/ Down
SC72	Scan 4-bit Synchronous Binary Up Counter with Parallel Load	62	36	4	Q, XQ, CO (S)	Sync	_	Low	High	Up
SC8 <sup>2</sup>	Scan 4-bit Synchronous Binary Down Counter with Parallel Load	66	36	4	Q, XQ, CO (S)	Sync	_	High	Low	Down
C11 <sup>3</sup>	Non-Scan Flip-Flop for Counter	11	18	_	Q, XQ	_	_	_		
C41	Non-Scan 4-bit Binary Asynchronous Counter	24	18	4	Q, (A)	_	Async	_	_	Up
C42	Non-Scan 4-bit Binary Synchronous Counter	32	18	4	Q	_	Async	_		Up
C43	Non-Scan 4-bit Binary Synchronous Up Counter	48	18	4	Q, CO (S)	Sync	Async	High	High	Up
C45	Non-Scan Binary Synchronous Up Counter	48	18	4	Q, CO	Sync	Sync	High	High	Up
C47	Non-Scan Binary Synchronous Up/Down Counter	68	18	4	Q, CO	Async	_	Low	Low	Up/ Down

Notes: ¹(S), (A) indicate the counter is (S)ynchronous or (A)synchronous.

2Scan counters include clock inhibit and high drive (CDR = 36 lu). For non-Scan counters CDR = 18 lu.

<sup>&</sup>lt;sup>3</sup>C11 may by used for purposes other than counters.

# **UHB Series CMOS Gate Arrays**

# FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Shift F	Shift Register Family										
Unit Cell Name	Description	Basic Cells	Drive (lu)	Bit Width	Load	Outputs	Clock Polarity				
FS1	Serial-in Parallel-out Shift Register	18	16	4	Serial-In only	Q-Parallel	Neg				
FS2	Shift Register with Synchronous Load	30	16	4	Sync-High	Q-Parallel	Neg				
FS3	Shift Register with Asynchronous Load	34	18	4	Async-Low	Q-Parallel	Pos				
SR1	Serial-in Parallel-out Shift Register with Scan	36	36	4	Serial-In only	Q-Parallel	Pos				

Datapat	h Operators (Adder, ALU, Parity)					
Unit Cell Name	Description	Basic Cells	Drive (lu)	Bit Width	Load	Outputs
MC4	Magnitude Comparator	42	18 (=) 10 (<,>)	4	A>B, A=B, A <b< td=""><td>A&gt;B,A=B,ALB</td></b<>	A>B,A=B,ALB
A1A	1-bit Half Adder	5	36	1	s, co	
A1N	1-bit Full Adder	8	18	1	s, co	CI
A2N	2-bit Full Adder	16	14	2	s, co	CI
A4H	4-bit Binary Full Adder w/Fast Carry	48	18 (CO) 14 (S)	4	s, co	CI
PE5	Even Parity Generator/Checker	12	36	5	EVEN, ODD	
PO5	Odd Parity Generator/Checker	12	36	5	ODD, EVEN	
PE8	Even Parity Generator/Checker	18	18	8	EVEN, ODD	
PO8	Odd Parity Generator/Checker	18	18	8	ODD, EVEN	_
PE9	Even Parity Generator/Checker	22	18	9	EVEN, ODD	
PO9	Odd Parity Generator/Checker	22	18	9	ODD, EVEN	_

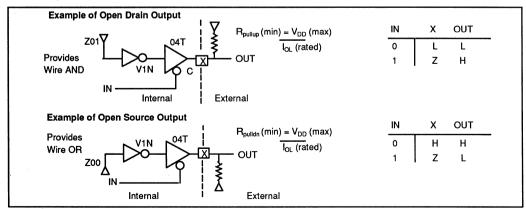
Miscellaneous Cells	Aiscellaneous Cells							
Unit Cell Name	Description	Basic Cells	Function					
Z00	0 Clip	0	Tie to V <sub>SS</sub>					
Z01	1 Clip	0	Tie to V <sub>DD</sub>					

nput Buffer Family								
Description	Basic Cells	Drive (lu)	Logic Level	Туре	Input/Output Polarity			
Input Buffer	5	36	TTL	Signal	Invert			
I1B with Pull-down Resistance	5	36	TTL	Signal	Invert Invert			
Input Buffer	4	36	TTL	Signal	True			
I2B with Pull-up Resistance I2B with Pull-down Resistance	4 4	36 36	TTL	Signal Signal	True True			
Clock Input Buffer	4	72	TTL	Clock	Invert			
IKB With Pull-up Resistance IKB with Pull-down Resistance	4 4	72 72	TTL	Clock Clock	Invert Invert			
Clock Input Buffer	6	72	TTL	Clock	True			
ILB with Pull-up Resistance ILB with Pull-down Resistance	6	72 72	TTL	Clock Clock	True True			
CMOS Interface Input Buffer	5	36	CMOS	Signal	Invert			
I1C with Pull-up Resistance I1C with Pull-down Resistance	5	36 36	CMOS	Signal Signal	Invert Invert			
CMOS Interface Input Buffer	4	36	CMOS	Signal	True			
I2C with Pull-up Resistance I2C with Pull-down Resistance	4	36 36	CMOS	Signal Signal	True True			
Schmitt Trigger Input Buffer	8	18	CMOS	Schmitt	Invert			
I1S with Pull-up Resistance I1S with Pull-down Resistance	8	18 18	CMOS	Schmitt Schmitt	Invert Invert			
Schmitt Trigger Input Buffer	8	18	CMOS	Schmitt	True			
I2S with Pull-up Resistance I2S with Pull-down Resistance	8 8	18 18	CMOS CMOS	Schmitt Schmitt	True True			
Schmitt Trigger Input Buffer	6	18	TTL	Schmitt	Invert			
I1R with Pull-up Resistance I1R with Pull-down Resistance	6	18 18	TTL	Schmitt Schmitt	Invert Invert			
Schmitt Trigger Input Buffer	8	18	TTL	Schmitt	True			
I2R With Pull-up Resistance	8	18 18	TTL	Schmitt	True True			
	Input Buffer I1B with Pull-up Resistance I1B with Pull-down Resistance Input Buffer I2B with Pull-up Resistance I2B with Pull-up Resistance I2B with Pull-up Resistance I2B with Pull-down Resistance I2B with Pull-down Resistance I2B with Pull-up Resistance I2B with Pull-up Resistance I2B with Pull-up Resistance I2B with Pull-down Resistance I2B with Pull-up Resistance I2B with Pull-up Resistance I2C with Pull-down Resistance I3C with Pull-down Resistance I3C with Pull-up Resistance I3C with Pull-up Resistance I3C with Pull-up Resistance I3S with Pull-up Resistance I3S with Pull-down Resistance I3S with Pull-down Resistance I3S with Pull-up Resistance I3S with Pull-up Resistance I3S with Pull-up Resistance I3S with Pull-up Resistance I3S with Pull-down Resistance I4R with Pull-down Resistance I5R with Pull-down Resistance	Input Buffer 5 I1B with Pull-up Resistance 5 I1B with Pull-up Resistance 5 Input Buffer 4 I2B with Pull-down Resistance 4 I2B with Pull-down Resistance 4 I2B with Pull-down Resistance 4 I2B with Pull-up Resistance 4 IKB With Pull-up Resistance 4 IKB with Pull-up Resistance 4 IKB with Pull-up Resistance 6 ILB with Pull-up Resistance 6 ILB with Pull-down Resistance 6 ILB with Pull-down Resistance 5 IC Wos Interface Input Buffer 1 IC with Pull-up Resistance 5 IC with Pull-up Resistance 5 IC with Pull-up Resistance 5 IC with Pull-up Resistance 4 I2C with Pull-up Resistance 4 I2C with Pull-up Resistance 4 I2C with Pull-up Resistance 8 IS with Pull-down Resistance 6 IR with Pull-down Resistance 6 IR with Pull-down Resistance 6 IR with Pull-down Resistance 8 IR with Pull-down Resistance 8 IR with Pull-down Resistance 6 IR with Pull-down Resistance 8 IR with Pull-down R	Description	Description	Description   Basic   Cells   Drive (Iu)   Logic   Level   Type			

Note: A "U" suffixed to the name of an input buffer indicates pull-up resistance of  $50K\Omega$  (typical) and a "D" indicates a pull-down resistance of the equivalent value.

Output Bu	ffer Family						
Unit Cell Name	Description	Basic Cells	Drive (I <sub>OL</sub> )	Logic² Level	Type	Edge Rate Control	Input/Output Polarity
O1B	Output Buffer	3	3.2 mA	TTL/CMOS	Standard	No	Invert
O1L	Power Output Buffer	3	12 mA	TTL/CMOS	Standard	No	Invert
018	Power Output Buffer	5	12 mA	TTL/CMOS	Standard	Yes	Invert
O2B	Output Buffer	2	3.2 mA	TTL/CMOS	Standard	No	True
O2L	Power Output Buffer	2	12 mA	TTL/CMOS	Standard	No	True
O2S	Power Output Buffer	4	12 mA	TTL/CMOS	Standard	Yes	True
O4T <sup>1</sup>	Output Buffer	4	3.2 mA	TTL/CMOS	3-state	No	True
O4W <sup>1</sup>	Power 3-state Output Buffer	4	12 mA	TTL/CMOS	3-state	No	True
O4S!	Power 3-state Output Buffer	5	12 mA	TTL/CMOS	3-state	Yes	True
O1R	Output Buffer	5	3.2 mA	TTL/CMOS	Standard	Yes	Invert
O2R	Output Buffer	4	3.2 mA	TTL/CMOS	Standard	Yes	True
O4R <sup>1</sup>	Output Buffer	5	3.2 mA	TTL/CMOS	3-state	Yes	True
O2S2	High Power Output Buffer	6	24 mA	TTL/CMOS	Standard	Yes	True
O4S21	High Power Output Buffer	7	24 mA	TTL/CMOS	3-state	Yes	True
O1BF	Output Buffer	3	8 mA	TTL/CMOS	Standard	No	Invert
O1RF	Output Buffer	5	8 mA	TTL/CMOS	Standard	Yes	Invert
O2BF	Output Buffer	2	8 mA	TTL/CMOS	Standard	No	True
O2RF	Output Buffer	4	8 mA	TTL/CMOS	Standard	Yes	True
O4RF	3-state Output Buffer	5	8 mA	TTL/CMOS	3-state	Yes	True
O4TF	3-state Output Buffer	4	8 mA	TTL/CMOS	3-state	No	True

Note: 1While all outputs are totem-pole type, Open Drain and Open Source types can easily be defined for all 3-state type outputs.



Note: <sup>2</sup>Totem pole outputs, such as these buffers have, can drive both TTL and CMOS levels. Voltage margins depend on actual source or sink current (see DC specifications).

Unit Cell Name	Description	Basic Cells	Drive (I <sub>OL</sub> )	Logic Level	Edge Rate Control	Input/Output Polarity
H6T H6TU	3-state Output and Input Buffer H6T with Pull-up Resistance	8	3.2 mA 3.2 mA	TTL TTL	No No	True True
H6TD	H6T with Pull-down Resistance	8	3.2 mA	ΠL	No	True
H6W	Power 3-state Output and Input Buffer	8	12 mA	TTL	No	True
H6WU H6WD	H6W with Pull-up Resistance H6W with Pull-down Resistance	8 8	12 mA 12 mA	TTL TTL	No No	True True
H6C	3-state Output and CMOS					
	Interface Input Buffer	8	3.2 mA	CMOS	No	True True
H6CU H6CD	H6C with Pull-up Resistance H6C with Pull-down Resistance	8 8	3.2 mA 3.2 mA	CMOS CMOS	No No	True
			3.2 IIIA	CIVIOS	NO	Tide
H6E	Power 3-state Output and CMOS Interface Input Buffer	8	12 mA	CMOS	No	True
H6EU	H6E with Pull-up Resistance	8	12 mA	CMOS	No No	True
H6ED	H6E with Pull-down Resistance	8	12 mA	CMOS	No	True
H6S	3-state Output and Schmitt					
	Trigger Input Buffer	12	3.2 mA	CMOS	No	True
H6SU	H6S with Pull-up Resistance	12	3.2 mA	CMOS	No	True
H6SD	H6S with Pull-down Resistance	12	3.2 mA	CMOS	No	True
H6R	3-state Output and Schmitt					
	Trigger Input Buffer	12	3.2 mA	TTL	No	True
H6RU	H6R with Pull-up Resistance	12	3.2 mA	TTL	No	True
H6RD	H6R with Pull-down Resistance	12	3.2 mA	TTL	No	True
H8T	3-state Output and Input Buffer	9	3.2 mA	TTL	Yes	True
H8TU	H8T with Pull-up Resistance	9	3.2 mA	TTL	Yes	True
H8TD	H8T with Pull-down Resistance	9	3.2 mA	TTL	Yes	True
H8W	Power 3-state Output and Input Buffer	9	12 mA	TTL	Yes	True
H8WU	H8W with Pull-up Resistance	9	12 mA	TTL	Yes	True
H8WD	H8W with Pull-down Resistance	9	12 mA	TTL	Yes	True
H8W2	High Power 3-state Output and Input Buffer	11	24 mA	TTL	Yes	True
H8W1	H8W2 with Pull-up Resistance	11	24 mA	TTL	Yes	True
H8W0	H8W2 with Pull-down Resistance	11	24 mA	TTL	Yes	True
H8C	3-state Output Buffer and CMOS					
	Interface Input Buffer	9	3.2 mA	CMOS	Yes	True
H8CU	H8C with Pull-up Resistance	9	3.2 mA	CMOS	Yes	True
H8CD	H8C with Pull-down Resistance	9	3.2 mA	CMOS	Yes	True
H8E	Power 3-state Output Buffer and Interface Input Buffer	9	12 mA	CMOS	Yes	True
H8EU	H8E with Pull-up Resistance	9	12 mA	CMOS	Yes	True
H8ED	H8E with Pull-down Resistance	9	12 mA	CMOS	Yes	True

Note: A "U" suffixed to the name of a bidirectional buffer indicates a pull-up resistance of 50Ω (typical) and a "D" indicates a pull-down resistance of the equivalent value.

Bidirectio	nal I/O Buffers (Buses) (Continued)					
Unit Cell Name	Description	Basic Cells	Drive (lu)	Logic Level	Туре	Input/Output Polarity
H8E2	High Power 3-state Output and Input Buffer	11	24 mA	CMOS	Yes	True
H8E1 H8E0	H8E2 with Pull-up Resistance	11 11	24 mA 24 mA	CMOS CMOS	Yes Yes	True True
H8S	3-state Output and Schmitt Trigger Input					
H8SU H8SD	Buffer True H8S with Pull-up Resistance H8S with Pull-down Resistance	13 13 13	3.2 mA 3.2 mA 3.2 mA	CMOS CMOS CMOS	Yes Yes Yes	True True True
H8R	3-state Output and Schmitt Trigger Input BufferTrue	13	3.2 mA	TTL	Yes	True
H8RU H8RD	H8R with Pull-up Resistance H8R with Pull-down Resistance	13 13	3.2 mA 3.2 mA	TTL TTL	Yes Yes	True True
H6TF	3-state Output and SchmittTrigger Input BufferTrue	8	8 mA	TTL	No	True
H6TFU H6TFD	H6TF with Pull-up Resistance H6TF with Pull-down Resistance	8 8	8 mA 8 mA	TTL TTL	No No	True True
H6CF H6CFU H6CFD	3-state Output and Input Buffer H6CF with Pull-up Resistance H6CF with Pull-down Resistance	8 8 8	8 mA 8 mA 8 mA	CMOS CMOS CMOS	No No No	True True True
H8TF H8TFU H8TFD	3-state Output and Input Buffer H8TF with Pull-up Resistance H8TF with Pull-down Resistance	9 9 9	8 mA 8 mA 8 mA	TTL TTL TTL	Yes Yes Yes	True True True
H8CF H8CFU H8CFD	3-state Output and Input Buffer H8CF with Pull-up Resistance H8CF with Pull-down Resistance	9 9 9	8 mA 8 mA 8 mA	CMOS CMOS CMOS	Yes Yes Yes	True True True

Note: While all outputs are totem-pole type, Open Drain and Open Source types can easily be defined for all 3-state type outputs, which includes all bidirectional buffers.

Oscillator	Oscillator Circuits							
Unit Cell Name	Description	Basic Cells	Input Logic Level					
HOC	Output Buffer for Oscillator and Input Buffer	8	CMOS					
HOCS	Output Buffer for Oscillator and Schmitt Trigger Input Buffer	8	TTL					
HOCR	Output Buffer for Oscillator with feedback Resistance	8	CMOS					
IT1O	Input Buffer for Oscillator	0						

## **UHB GATE ARRAY PACKAGE CHARACTERISTICS**

	Package Code					
Pinout Code	Plastic	Ceramic	Number of V <sub>DD</sub>	Number of V <sub>SS</sub>	Available Number or Signal Pins	
DIP-16	DIP-16P-MO2	DIP-16C-C03	1	2	13	
	DIP-16P-MO4					
DIP-18	DIP-18P-MO1	DIP-18C-CO1				
	DIP-18P-MO2					
DIP-20	DIP-20P-MO2	DIP-20C-CO2	1	2	17	
DIP-20U			1	1	18	
DIP-22	DIP-22P-MO2	DIP-22C-C02	2	2	18	
	DIP-22P-MO3					
DIP-22U			1	1	20	
DIP-24	DIP24P-MO1	DIP-24C-C01	2	2	20	
	DIP24P-MO2					
DIP-24U			1	1	22	
DIP-28	DIP-28P-M02	DIP-28C-C02	2	2	24	
	DIP-28P-M03					
DIP-28U			1	1	26	
DIP-40	DIP-40P-M01	DIP-40C-A01	2	4	34	
		DIP-40C-A02				
DIP-40U			1	1	38	
DIP-42	DIP-42P-MO1	DIP-42C-A01	2	4	36	
	DIP-42P-MO2					
DIP-42U			1	1	40	
DIP-48	DIP-48P-MO1	DIP-48C-A01	2	4	42	
	DIP-48P-MO2				The state of the s	
DIP-48U			1	1	46	

# **UHB GATE ARRAY PACKAGE CHARACTERISTICS** (Continued)

Dual In-line Packages (Shrink DIP, 70 mil Pin Pitch)									
	Packaç	je Code							
Pinout Code	Plastic	Ceramic	Number of V <sub>DD</sub>	Number of V <sub>SS</sub>	Available Number of Signal Pins				
DIP-28SH			2	2	24				
DIP-28SHU			1	1	26				
DIP-42SH			2	4	36				
DIP-42SHU			1	1	40				
DIP-48SH			2	4	36				
DIP-48SHU			1	1	46				
DIP-64SH			2	4	58				
DIP-64SHU			2	2	60				

	Package	Code			
Pinout Code	Plastic	Ceramic	Number of V <sub>DD</sub>	Number of V <sub>SS</sub>	Available Number of Signal Pins
DIP-22SK			2	2	18
DIP-22SKU			1	1	20
DIP-24SK			2	2	20
DIP-24SKU			1	1	22
DIP-28SK			2	2	24
DIP-28SKU			1	1	26

Flatpack Packages (Dual-Leaded)								
	Package	Code						
Pinout Code	Plastic	Ceramic	Number of V <sub>DD</sub>	Number of V <sub>SS</sub>	Available Number of Signal Pins			
FPT-16	FPT-16P-MO3		1	2	13			
FPT-16U			1	1	14			
FPT-20	FPT-20P-MO2		1	2	17			
FPT-20U			1	1	18			
FPT-24	FPT-24-MO2		2	2	20			
FPT-24U			1	1	22			
FPT-28	FPT-28P-MO1		2	2	24			
FPT-28U			1	1	26			

# **UHB GATE ARRAY PACKAGE CHARACTERISTICS** (Continued)

Flatpack Pack	ages (Quad-Leaded	t)			
	Package Code				
Pinout Code	Plastic	Ceramic	Number of V <sub>DD</sub>	Number of V <sub>ss</sub>	Available Number of Signal Pins
FPT-44			2	4	36
FPT-44U			2	2	40
FPT-48	FPT-48P-MO2		2	4	42
FPT-48U			2	2	44
FPT-48 *			2	4	42
FPT-48U *			2	2	44
FPT-64*	FPT-64P-MO1		2	4	58
FPT-64U	FPT-70P-MO1		1	1	62
FPT-80	FPT-80P-MO1		2	6	72
FPT-80U			2	4	74
FPT-100	FPT-100P-MO1		4	8	88
FPT-100U			4	4	92
FPT-120			6	12	102
FPT-120U			4	8	108
FPT-160			8	14	138
FPT-160U			6	12	142

<sup>\*</sup> Small body size.

Subject to Change

Pin Grid Arrays	(PGA, Thru-H	ole, 100 mil Pin Pi	tch)		
	Packa	age Code			
Pinout Code	Plastic	Ceramic	Number of V <sub>DD</sub>	Number of V <sub>SS</sub>	Available Number of Signal Pins
PGA-64		PGA-64C-A02	2	4	58
PGA-64U			2	2	60
PGA-88		PGA-88C-A01	4	6	78
PGA-88U			4	4	80
PGA-135			8	12	115
PGA-135U			4	8	127
PGA-179			8	16	155
PGA-179U			8	8	163
PGA-208			12	18	178
PGA-256			16	20	220

# **UHB GATE ARRAY PACKAGE CHARACTERISTICS (Continued)**

Flatpack Packa	ges (Dual-Lea	ded)			
	Packa	age Code			
Pinout Code	Plastic	Ceramic	Number of V <sub>DD</sub>	Number of V <sub>SS</sub>	Available Number of Signal Pins
LCC-28		LCC-28C-A02	2	2	24
LCC-28U			1	1	26
LCC-48		LCC-48C-A01	2	4	42
LCC-48U			1	2	45
LCC-64		LCC-64C-A01	2	4	58
LCC-64U			2	2	60
LCC-68			2	4	62
LCC-68U			2	2	64
LCC-84			4	6	74
LCC-84U			3	4	77

	Package	Code			
Pinout Code	Plastic	Ceramic	Number of V <sub>DD</sub>	Number of V <sub>SS</sub>	Available Number of Signal Pins
PLCC-28	LCC-28P-M01		2	2	24
PLCC-28U			1	1	26
PLCC-44	LCC-44P-MO1		2	4	38
PLCC-44U			1	2	41
PLCC-68	LCC-68P-M01		2	4	62
PLCC-68U			2	2	64
PLCC-84	LCC-84P-M01	THE RESERVE THE PROPERTY OF THE PARTY OF THE	4	6	74
PLCC-84U			2	4	78

Subject to Change

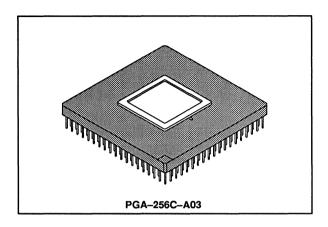
### **UHB GATE ARRAY PACKAGE AVAILABILITY**

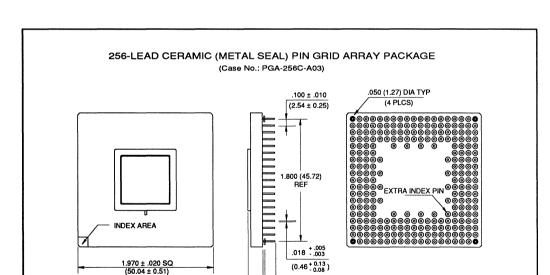
		C-S	330 HB	C-	530 HB	C-	830 HB	C-1	200 HB	C-1 UI	700 IB	C-2 Uł	200 IB	C-3 Uł	000 IB	C-4 Ui	100 IB	C-6	000 HB	C-8 Ul	700 IB	C-12 UI	2000 HB
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C = Ceramic P = Plastic \* = 48-pin FPT, smaller than the other 48 FPT

<sup>•:</sup> available now a under development

### **PACKAGE DIMENSIONS**





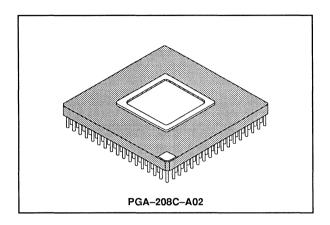
.130 + .020

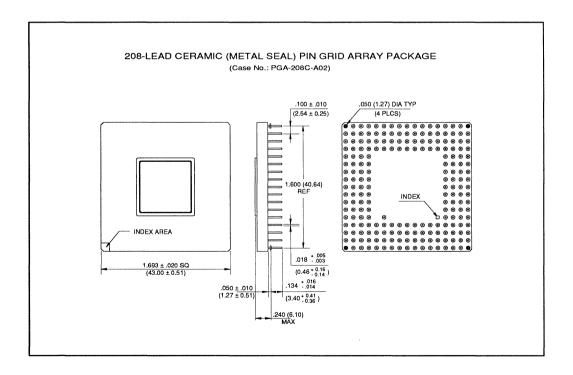
(3.30 + 0.51 )

.250 (6.35) MAX

.050 ± .010 (1.27 ± 0.51)

## PACKAGE DIMENSIONS (Continued)





PRODUCT PROFILE



# CG10 Series 0.8-micron CMOS Gate Arrays

### DESCRIPTION

The CG10 series of 0.8-micron CMOS gate arrays is a highly integrated low-power, ultra high-speed product family that derives its enhanced performance and increased user flexibility from the use of a system-proven, dual-column gate structure and 2-layer metal interconnect technology. The unique dual-column gate structure increases density and speed performance, as well as gate utilization. CG10 architecture is fully compatible with Fujitsu's 1.5-micron UHB arrays.

Internal high-drive clock buffers minimize clock skew across the chip while internal bus performance and integrity is assured by incorporating 3-state transmission gate logic underneath the routing channels. Input buffer options include pull-up and pull-down resistance, Schmitt trigger, CMOS input, and clock driver. Output buffer options include 3-state, bidirectional, edge rate control, and high-drive output. The high-drive output buffers provide highly symmetrical output waveforms.

#### **FEATURES**

- High-density silicon gate CMOS technology
  - 3200 to 14,000 usable gates
  - 90% maximum utilization fully autorouted
- Ultra high speed
  - typical 0.5 ns/0.6 ns gate delay (power type/normal type)
  - narrow delay variation
- High sink current capability
  - 3.2 mA, 8 mA, 12 mA, and 24 mA options available
  - selectable edge rate control

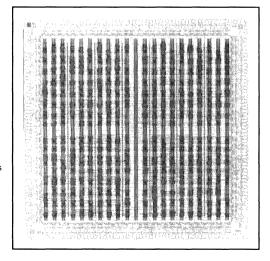
- Low-skew clock signal distribution
  - High-performance clock drivers
- Hierarchical clock distribution
- Frequency-dependent clock routing
- Automatic test pattern generation
  - complete family of scan design macros available

### **PRODUCT FAMILY**

Device Name	Available Gates <sup>1</sup>	Maximum Signal Pins <sup>2</sup>	Power Dissipation at 10 MHz
CG10272	3,256	108	150 mW
CG10342	4,032	123	200 mW
CG10492	5,572	148	200 mW
CG10572	6,510	163	200 mW
CG10692	7,684	163	250 mW
CG10103	11,080	188	250 mW
CG10133	14,720	220	250 mW

Gate count based on 2-input NAND and includes basic cells to form I/O buffer functions

<sup>&</sup>lt;sup>2</sup>Maximum signal pin numbers depend on the output drive requirements and the package selected.



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### **AC CHARACTERISTICS**

### **BEST/WORST CASE MULTIPLIERS FOR PROPAGATION DELAYS**

Propagation delays characteristic of a gate array are a function of several factors, including operating temperature, supply voltage, fanout loading, interconnection routing metal, process variation, input transition time, and input signal polarity. Temperature and supply voltage factors affecting propagation delays in the CG10 CMOS family of gate arrays are given in the table below.

		Pre-Layout	Simulation		Post-Layout Simulation						
Temperature Range	V <sub>DD</sub> =	5 V ±5%	V ±5% V <sub>DD</sub> = 5 V ±10%		V <sub>DD</sub> =	5 V ±5%	V <sub>DD</sub> = 5 V ±10%				
	Best Case	Worst Case	Best Case	Worst Case	Best Case	Worst Case	Best Case	Worst Case			
0 - 70°C1	0.35	1.65	0.30	1.75	0.40	1.60	0.35	1.70			
-20 − 70°C	0.35	1.65	0.25	1.75	0.35	1.60	0.30	1.70			
-40 − 70°C	0.25	1.65	0.20	1.75	0.30	1.60	0.25	1.70			
-40 - 85°C2	0.25	1.75	0.20	1.85	0.30	1.70	0.25	1.80			

Notes: 1Commercial temperature range

<sup>2</sup>Industrial temperature range

### REPRESENTATIVE PROPAGATION DELAYS

Constants for calculating the delays due to process variation, fanout loading, interconnection routing metal, transition time, and signal polarity are given for each unit cell in the CG10 Unit Cell Library. Delays using these factors are calculated for a representative selection of unit cells and are shown in the Propagation Delay tables below.

Calculations are representative of unit cells in the CG10672 (CG10 6700-gate CMOS gate array).

Typical values are indicated. Worst case multipliers are applied to typical values. Smaller arrays can exhibit significantly greater speed.

		I			Propa	gation De	lays (in r	ıs)	
Unit Cell Function	Unit Cell Name	Equivalent Gate Count	Input Transition			N <sub>DI</sub> (Fan	-out)		
				1	2	4	8	16	32
Inverter	V1N	1	t <sub>PLH</sub> t <sub>PHL</sub>	0.38 0.38	0.60 0.57	0.91 0.79	1.34 1.13	2.33 1.88	5.00 0.12
Power 2-Input NAND	N2K	2	t <sub>PLH</sub>	0.33 0.38	0.45 0.56	0.60 0.74	0.82 0.99	1.16 1.38	1.91 2.25
Power 16-Input NAND	NGB	11	t <sub>PLH</sub> t <sub>PHL</sub>	1.06 1.11	1.17 1.28	1.33 1.46	1.55 1.68	1.89 2.02	2.64 2.78
Power 2-Input NOR	R2K	2	t <sub>PLH</sub>	0.46 0.38	0.60 0.50	0.92 0.65	1.31 0.87	1.90 1.21	3.20 1.96
Power Exclusive OR	X2B	4	t <sub>PLH</sub> t <sub>PHL</sub>	1.00 1.01	1.11 1.14	1.26 1.28	1.49 1.46	1.83 1.74	2.58 2.36
3-wide 2-AND 6-Input AND-OR Inverter (A → Y)	D36	3	t <sub>PLH</sub> t <sub>PHL</sub>	0.84 0.72	1.24 0.99	1.82 1.38	2.97 2.15	6.05 4.21	# # # 8.38
2-wide 2-OR 4-input OR-AND-Inverter (A → X)	G24	2	t <sub>PLH</sub> t <sub>PHL</sub>	0.68 0.55	1.09 0.82	1.70 1.21	2.89 1.98	6.07 4.04	# # # 8.21
Power 2-AND 8-Wide Multiplexer (A → X)	T28	11	t <sub>PLH</sub> t <sub>PHL</sub>	1.43 1.39	1.54 1.47	1.70 1.58	1.92 1.73	2.26 1.96	3.01 2.46
Power Clock Buffer	K2B	3	t <sub>PLH</sub> t <sub>PHL</sub>	0.71 0.81	0.77 0.86	0.85 0.94	0.96 1.05	1.13 1.26	1.43 1.52
Scan 8-bit D Flip-flop with Clock Inhibit and 3:1 Data Multiplexer (CK,IH → Q)	SHK	88	t <sub>РLН</sub> t <sub>РНL</sub>	3.10 3.07	3.33 3.25	3.63 3.48	4.07 3.81	5.05 4.56	7.72 2.80
Non–Scan D Flip-flop with Reset (CK → Q)	FDO	7	t <sub>PLH</sub> t <sub>PHL</sub>	1.41 1.37	1.63 1.56	1.94 1.81	2.37 2.18	3.36 3.00	6.03 5.24
Non-Scan Power D Flip-flop with Clear (CK $\rightarrow$ Q)	FD5	8	t <sub>PLH</sub> t <sub>PHL</sub>	1.28 1.34	1.39 1.53	1.55 1.68	1.77 1.86	2.11 2.14	2.86 2.76
Non-Scan 4-bit Binary Synchronous Up Counter (CI → CO)	C43	48	t <sub>PLH</sub> t <sub>PHL</sub>	1.20 1.14	1.43 1.29	1.73 1.49	2.17 1.78	3.15 2.44	5.82 4.24
Non-Scan 4-bit Binary Synchronous Up Counter (CI → CO)	C45	48	t <sub>РLН</sub> t <sub>РНL</sub>	1.41 1.35	1.65 1.52	1.98 1.75	2.45 2.08	3.51 2.83	6.38 4.87

Note: Delays for inter-block wiring are not included

## **REPRESENTATIVE PROPAGATION DELAYS (Continued)**

	T., ., ., .,	I			Propa	gation De	elays (in i	ns)	
Unit Cell Function	Unit Cell Name	Equivalent Gate Count	Input Transition			N <sub>DI</sub> (Fan	-out)		
				1	2	4	8	16	32
Non-Scan 4-bit Binary Synchronous Up/Down Counter (DU → CO)	C47	68	t <sub>РLН</sub> t <sub>РНL</sub>	1.68 1.68	1.84 1.83	2.05 2.03	2.34 2.33	3.02 2.99	4.86 4.78
4-bit Binary Full Adder with Fast Carry (CI → S1)	A4H	48	t <sub>PLH</sub> t <sub>PHL</sub>	1.02 0.98	1.33 1.24	1.75 1.60	2.51 2.25	3.91 3.43	# # # 7.53
4:1 Selector (S5 → X)	T5A	5	t <sub>PLH</sub> t <sub>PHL</sub>	0.64 0.62	0.97 0.93	1.50 1.42	2.45 2.29	# # # 4.91	# # # 9.67
4-bit Shift Register with Synchronous Load	FS2	30	t <sub>PLH</sub> t <sub>PHL</sub>	1.65 1.65	1.88 1.84	2.18 2.07	2.66 2.44	3.67 3.20	6.74 1.75
9-bit Odd Parity Generator/Checker	PO9	22	t <sub>PLH</sub> t <sub>PHL</sub>	3.45 3.39	3.68 3.54	3.98 3.74	4.42 4.03	5.40 4.69	8.07 6.49
4-wide 2:1 Data Selector (A → X)	P24	12	t <sub>PLH</sub> t <sub>PHL</sub>	0.70 0.66	0.81 0.74	0.96 0.84	1.19 0.99	1.53 1.22	2.28 1.73
4-bit Magnitude Comparator (IS → OG)	MC4	42	t <sub>PLH</sub> t <sub>PHL</sub>	1.70 1.52	2.11 1.69	2.72 1.91	3.91 2.35	7.09 0.30	### 2.08
4-bit Bus Driver (A → X)	B41	9	t <sub>PLH</sub> t <sub>PHL</sub>	1.08 1.09	1.18 1.21	1.32 1.36	1.51 1.58	1.81 1.92	2.47 2.67
Input Buffer (Inverter)	I1B	5	t <sub>PLH</sub> t <sub>PHL</sub>	1.05 1.07	1.11 1.15	1.19 1.25	1.30 1.40	1.47 1.63	1.84 2.14
Clock Input Buffer (Inverter)	IKB	4	t <sub>PLH</sub> t <sub>PHL</sub>	1.56 1.56	1.58 1.57	1.61 1.59	1.64 1.63	1.70 1.68	1.81 1.77

I/O Cell	Unit Cell	Equivalent	Input		Ou	tput Buff	er Load i	n pF	
Function	Name	Gate Count	Transition	12	25	50	100	200	400
Output Buffer (True)	O2B	2	t <sub>PLH</sub> t <sub>PHL</sub>	0.93 1.75	1.40 2.78	2.30 4.75	4.10 8.70	7.70 16.60	14.90 32.40
Power Output Buffer (True)	O2L	2	t <sub>PLH</sub> t <sub>PHL</sub>	0.90 1.21	1.21 1.54	1.81 2.19	3.01 3.49	5.41 6.09	10.21 11.29
3-State Output Buffer (True) (OT → X)	O4T	4	t <sub>PLH</sub> t <sub>PHL</sub>	1.07 2.42	1.54 3.46	2.44 5.46	4.24 9.46	7.84 17.46	15.04 33.46
Power 3-State Output Buffer (True) (OT → X)	O4W	4	t <sub>PLH</sub> t <sub>PHL</sub>	1.09 3.03	1.41 3.47	2.00 4.32	3.00 6.02	5.60 9.42	10.40 16.22
3-State Output and Input Buffer (True) (X → IN)	Н6Т	8	t <sub>PLH</sub> t <sub>PHL</sub>	0.87 1.43	1.09 1.73	1.51 2.30	2.36 3.45	4.06 5.75	7.46 10.35
Power 3-State Output and Input Buffer (True) (OT $\rightarrow$ X)	H6W	8	t <sub>PLH</sub> t <sub>PHL</sub>	1.09 3.03	1.40 3.47	2.00 4.32	3.20 6.02	5.60 9.42	10.40 16.22

Note: Delays for inter-block wiring are not included

### **DC CHARACTERISTICS**

### **ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

Rating		Symbol	Minimum	Maximum	Unit
Supply Voltage		$V_{DD}$	V <sub>SS</sub> - 0.5 <sup>2</sup>	6.0	V
Input Voltage		Vı	V <sub>SS</sub> - 0.5 <sup>2</sup>	V <sub>DD</sub> +0.5	v
Output Voltage		Vo	V <sub>SS</sub> - 0.5 <sup>2</sup>	V <sub>DD</sub> +0.5	v
	I <sub>OL</sub> = 3.2 mA		-40		
Output Current <sup>3</sup>	I <sub>OL</sub> = 8 mA	los	-40		mA.
Culput Current	I <sub>OL</sub> = 12 mA	.03	-60		
	I <sub>OL</sub> = 24 mA		-90		
Storage Temperature	Ceramic Plastic	T <sub>stg</sub>	-65 -40	+150 +125	5C
Temperature Under Bias	Ceramic Plastic	T <sub>bias</sub>	-40 -25	+125 +85	5C

Notes: 

1Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage	V <sub>DD</sub>	4.75	5.0	5.25	V
Input High Voltage for TTL Input	V <sub>IH</sub>	2.2	_	_	V
Input Low Voltage for TTL Input	V <sub>IL</sub>	-	-	0.8	V
Input High Voltage for CMOS Input	V <sub>IH</sub>	V <sub>DD</sub> x 0.7	-	-	V
Input Low Voltage for CMOS Input	V <sub>IL</sub>	_	_	V <sub>DD</sub> x 0.3	V
Operating Temperature	T <sub>A</sub>	0	_	70	°C

CAPACITANCE (TA = 25°C, VDD = VI = 0 V, f = 1 MHz)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input Pin Capacitance	C <sub>IN</sub>			16	pF
Output Pin Capacitance (I <sub>OL</sub> – 3.2 mA, 8 mA, or 12 mA)	C <sub>out</sub>		_	16	pF
Output Pin Capacitance (I <sub>OL</sub> – 24 mA)	C <sub>out</sub>		-	18	pF
I/O Pin Capacitance (I <sub>OL</sub> – 3.2 mA, 8 mA, or 12 mA)	C <sub>vo</sub>			16	pF
I/O Pin Capacitance (I <sub>OL</sub> – 24 mA)	C <sub>I/O</sub>		_	23	pF

 $<sup>^{2}</sup>V_{SS} = 0 V.$ 

<sup>&</sup>lt;sup>3</sup>Only one output at a time may be shorted for more than one second.

### **DC CHARACTERISTICS**

(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Power Supply Current	I <sub>DDS</sub>	Steady State <sup>1</sup>	0	_	100	μА
Output High Voltage for Normal Output (I <sub>OL</sub> = 3.2 mA)	V <sub>OH</sub>	l <sub>OH</sub> = -2 mA	4.0	_	V <sub>DD</sub>	V
Output High Voltage for Driver Output (I <sub>OL</sub> = 8 mA)	V <sub>OH</sub>	I <sub>OH</sub> = -2 mA	4.0	_	V <sub>DD</sub>	V
Output High Voltagefor Driver Output (I <sub>OL</sub> =12 mA)	V <sub>OH</sub>	I <sub>OH</sub> = -4 mA	4.0		V <sub>DD</sub>	V
Output High Voltage for Driver Output (I <sub>OL</sub> =24 mA)	V <sub>OH</sub>	I <sub>OH</sub> = -8 mA	4.0		V <sub>DD</sub>	V
Output Low Voltage <sup>2</sup> for Normal Output (I <sub>OL</sub> = 3.2 mA)	V <sub>OL</sub>	I <sub>OL</sub> = 3.2 mA	V <sub>SS</sub>	_	0.4	V
Output Low Voltage for Driver Output (I <sub>OL</sub> = 8 mA)	V <sub>OL</sub>	I <sub>OL</sub> = 8 mA	V <sub>ss</sub>	_	0.4	٧
Output Low Voltage <sup>2</sup> for Driver Output (I <sub>OL</sub> = 12 mA)	V <sub>OL</sub>	I <sub>OL</sub> = 12 mA	V <sub>SS</sub>		0.4	\ \
Output Low Voltage <sup>2</sup> for Driver Output (I <sub>OL</sub> = 24 mA)	V <sub>OL</sub>	l <sub>OL</sub> = 24 mA	V <sub>ss</sub>	_	0.5	٧
Input High Voltage for TTL Input	V <sub>IH</sub>		2.2	_	_	٧
Input Low Voltage for TTL Input	V <sub>IL</sub>	<del>-</del>			0.8	٧
Input High Voltage for CMOS Input	V <sub>IH</sub>	<del>-</del>	V <sub>DD</sub> x 0.7	_	_	٧
Input Low Voltage for CMOS Input	V <sub>IL</sub>	_	_	_	V <sub>DD</sub> x 0.3	V
Schmitt Trigger CMOS Input <sup>3</sup> Positive-going Threshold Negative-going Threshold Hysteresis	V <sub>T+</sub> V <sub>T-</sub> V <sub>T+</sub> -V <sub>T_</sub>	U <sub>IL</sub> to V <sub>IH</sub> , V <sub>IH</sub> , to V <sub>IL</sub>	2.5 0.7 1.1	3.3 1.4 1.9	4.0 2.0 2.7	V V
Schmitt Trigger TTL Input <sup>3</sup> Positive-going Threshold Negative-going Threshold Hysteresis	V <sub>T+</sub> V <sub>T-</sub> V <sub>T+</sub> -V <sub>T_</sub>	  V <sub>IL</sub> to V <sub>IH</sub> , V <sub>IH</sub> , to V <sub>IL</sub>	1.4 0.8 0.4	1.9 1.3 0.6	2.5 1.8 0.7	V V
Input Pull-up/Pull-down Resistor	R <sub>P</sub>	V <sub>IH</sub> to V <sub>DD</sub> V <sub>IL</sub> to V <sub>SS</sub>	25	50	100	kΩ
Input Leakage Current	ILI	$V_{i} = 0 - V_{DD}$	, <b>–</b> 10	_	10	μА
Input Leakage Current (3-state)	l <sub>LZ</sub>	$V_i = 0 - V_{DD}$	-10	_	10	μΑ

Notes:  $^{1}V_{IN} = V_{DD}$ ,  $V_{IL} = V_{SS}$   $^{2}$ With certain restrictions on pin assignment

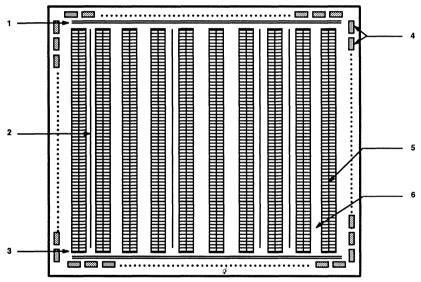
<sup>&</sup>lt;sup>3</sup>These values for reference only

### **ARRAY ARCHITECTURE**

The typical CG10 chip is composed of double columns of CMOS gates (basic cells) separated by dedicated wiring channels. A basic cell consists of a pair of N-channel and a pair of P-channel transistors interconnected by polysilicon gate control terminals. Groups of basic cells are interconnected by custom metallization into unit cells. Fujitsu unit cells provide a wide range of standard logic functions such as exclusive OR gates, flip-flops, buffers, and counters. The CG10 Series CMOS gate array family includes over 250 different unit cells. These unit cells are the building blocks from which complex designs are constructed.

The spaces between the double columns of basic cells are occupied by channels for custom metallization. Nearly half of these wiring channels contain transmission gates that implement internal 3-state buses. Bus terminators located at the ends of the double columns of cells maintain the last value to be sent through the bus to ensure proper operation under all conditions.

The I/O cells around the perimeter of the matrix of cells are composed of internal cells with input protection networks and the potential to be configured as input buffers, clock input buffers, output buffers, power output buffers, or bidirectional buffers.



Typical Chip Layout, Double Column Structure

- 1. Dedicated Clock Network for high frequency clocks
- 2. 3-state Bus Logic located in wiring channels
- 3. Bus Terminators prevent floating state on buses
- 4. Driver Transistors and I/O Protection Networks provide high I/O count
- 5. Double Columns for optional macro utilization and speed
- 6. Wiring Channel Area for metallization between unit cells

### **DESIGN COMPONENTS**

#### **DESIGNING WITH THE CG10 PRODUCT FAMILY**

To implement logic functions, you build up the elements of the circuit from unit cells. Simple unit cells are used hierarchically to build higher level functions until the logic is completely defined. Fujitsu offers a complete line of standard logic functions in the unit cell library.

Super macros are used to implement large super-cell functions such as expandable ALUs and multipliers.

#### I/O BUFFERS

Each CG10 I/O buffer around the perimeter of the array consists of an input protection network and large N-channel and P-channel transistors capable of supplying the standard 3.2-mA, 8-mA, and 12-mA output currents. Two of these large transistor pairs may be connected in parallel, using high-output-current macros, to obtain 24-mA drive. One of the I/O pads whose output transistors have been used for the 24-mA high-current option may still be used as an input.

Input I/O buffers convert external TTL levels to internal CMOS levels or may receive CMOS level signals directly. Output I/O buffers are totem pole and may drive either CMOS and TTL levels, depending on their AC and DC loads. Any of the pins except the dedicated power and ground pads can be designed to be an input buffer, an input buffer with pull-up/pull-down resistance, a clock input buffer, an output buffer, a high-drive output buffer, an output buffer with noise limiting resistance, a 3-state output buffer, a bi-directional buffer, or a Schmitt trigger input buffer. There are some restrictions on the location of 24-mA buffers.

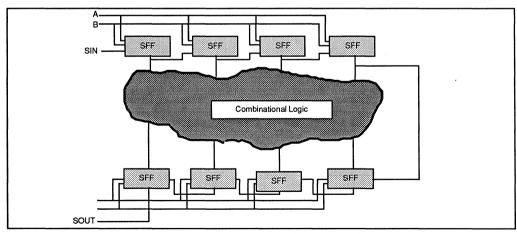
#### INPUT CLOCK DRIVERS

The large output I/O transistor pair is used in a high-drive input clock driver for high fanout applications within the array. This allows you to fully utilize the high speed capabilities of the CG10 technology.

### **TESTING CG10 DEVICES**

Two options are available for testing CG10 designs: (1) the standard designer-supplied test patterns and test vectors (in Fujitsu's FTDL format) and (2) the use of scan cells combined with Automatic Test Generation (ATG) performed by Fujitsu computers for additional diagnostic test patterns. If you have designed with scan cells and other scan logic elements, Fujitsu will complete the scan test program generation.

Regardless of the selected test option, you need to furnish Fujitsu with enough test patterns to guarantee that the submitted design completely performs its intended logic functions. These patterns include your test function of each I/O pin.



Diagramatic Representation of Design Structure for ScanTesting

## **VDD** and **VSS** REQUIREMENTS

Each CG10 Series gate array device has two options for each package type, both supporting a different number of power and ground pins. The number of power and ground pins required depends on the number of simultaneously switching outputs used in the design. Simultaneously switching outputs (SSOs) are output signals that change from H to L or L to H or from Z to H or Z to L within a 20-ns window (including possible skew).

Multiple outputs that switch at the same time can cause noise on Vpp and Vss lines and affect the performance of a device. Therefore, to achieve maximum reliability, Fujitsu limits the number of SSOs per Vpp pin according to the table below. The maximum number of SSOs per pin is determined by a representative value specified for the driving capability of each type of output. The total representative value of all SSOs used in a design must not exceed 80 per Vss pin. For example, 11 normal 3.2-mA outputs with edge rate control, four 12-mA outputs, or three 24-mA outputs per Vss pin may be SSOs.

Output Drive Type	Representative Value per Output
Normal (3.2 mA)	10
High Drive (12 mA)	20
Normal (3.2 mA) with Edge Rate Control	7
High Drive (12 mA) with Edge Rate Control	14
High Drive (24 mA) with Edge Rate Control	26

# **CG10 Series CMOS Gate Arrays**

## **FUNCTIONAL INDEX OF UNIT CELL LIBRARY**

Note: The load unit (lu) is a normalized loading unit of capacitance representing the input load of an inverter without metal interconnection.

nverter and Buffer Family					
Unit Cell Name	Description	Basic Cells	Drive (lu)	Polarity	
V1N	Inverter	1	18	Neg	
V2B	Power Inverter	1	36	Neg	
B1N	True Buffer	1	18	Pos	
BD3	True Delay Buffer (> 5 ns)	5	18	Pos	
BD4	Delay Cell (> 4 ns)	4	6	Pos	
BD5	Delay Cell (>10 ns)	9	18	Pos .	
BD6	Delay Cell (>22 ns)	17	18	Pos	

Clock Buffer Family					
Unit Cell Name	Description	Basic Cells	Drive (lu)	Polarity	
K1B	True Clock Buffer	2	36	Pos	
K2B	Power Clock Buffer	3	55	Pos	
КЗВ	Gated Clock (AND) Buffer	2	36	Pos	
K4B	Gated Clock (OR) Buffer	2	36	Pos	
K5B	Gated Clock (NAND) Buffer	3	36	Neg	
KAB	Block Clock (OR) Buffer	3	55	Pos	
KBB	Block Clock (OR x 10) Buffer	30	55	Pos	
V1L	Double Power Inverter	2	55	Neg	

NAND Family					
Unit Cell Name	Description	Basic Cells	Drive (lu)		
N2N	2-input NAND	1	18		
N2B	Power 2-input NAND	3	36		
N2K	Fast Power 2-input NAND	2	36		
N3N	3-input NAND	2	14		
N3B	Power 3-input NAND	3	36		
N4N	4-input NAND	2	10		
N4B	Power 4-input NAND	4	36		
N6B	Power 6-input NAND	5	36		
N8B	Power 8-input NAND	6	36		
N9B	Power 9-input NAND	8	36		
NCB	Power 12-input NAND	10	36		
NGB	Power 16-input NAND	11	36		
N3K	Fast Power 3-input NAND	3	28		
N4K	Fast Power 4-input NAND	4	20		

NOR Family					
Unit Cell Name	Description	Basic Cells	Drive (lu)		
R2N	2-input NOR	1	14		
R2B	Power 2-input NOR	3	36		
R2K	Power 2-input NOR	2	36		
R3N	3-input NOR	2	10		
R3B	Power 3-input NOR	3	36		
R3K	Power 3-input NOR	3	20		
R4N	4-input NOR	2	6		
R4B	Power 4-input NOR	4	36		
R4K	Power 4-input NOR	4	12		
R6B	Power 6-input NOR	5	36		
R8B	Power 8-input NOR	6	36		
R9B	Power 9-input NOR	8	36		
RCB	Power 12-input NOR	10 ·	36		
RGB	Power 16-input NOR	11	36		

AND Family				
Unit Cell Name	Description	Basic Cells	Drive (lu)	
N2P	Power 2-input AND	2	36	
N3P	Power 3-input AND	3	36	
N4P	Power 4-input AND	3	36	
N8P	Power 8-input AND	6	36	

OR Family				
Unit Cell Name	Description	Basic Cells	Drive (lu)	
R2P	Power 2-input OR	2	36	
R3P	Power 3-input OR	3	36	
R4P	Power 4-input OR	3	36	
R8P	Power 8-input OR	6	36	

Unit Cell Name	Description	Basic Cells	Drive (lu)	Polarity
X1N	Exclusive NOR	3	18	Neg
X1B	Power Exclusive NOR	4	36	Neg
X2N	Exclusive OR	3	14	Pos
X2B	Power Exclusive OR	4	36	Neg
X3N	3-input Exclusive NOR	5	14	Neg
ХЗВ	Power 3-input Exclusive NOR	6	36	Neg
X4N	3-input Exclusive OR	5	14	Pos
X4B	Power 3-input Exclusive OR6	6	36	Pos

## **CG10 Series CMOS Gate Arrays**

## FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

ND-OR-Inverter Family (AOI)					
Unit Cell Name	Description	Basic Cells	Drive (lu)		
D23	2-wide 2-AND 3-input AOI	2	14		
D14	2-wide 3-AND 4-input AOI	2	14		
D24	2-wide 2-AND 4-input AOI	2	14		
D34	3-wide 2-AND 4-input AOI	2	10		
D36	3-wide 2-AND 6-input AOI	3	10		
D44	2-wide 2-OR 2-AND 4-input AOI	2	10		

Note: AND-OR-Inverter unit cells are useful in implementing sum-of-products (SOP) expressions

OR-AND-Inverter Family (OAI)					
Unit Cell Name	Description	Basic Cells	Drive (lu)		
G23	2-wide 2-OR 3-input OAI	2	18		
G14	2-wide 3-OR 4-input OAI	2	10		
G24	2-wide 2-OR 4-input OAI	2	10		
G34	3-wide 2-OR 4-input OAI	2	10		
G44	2-wide 2-AND 2-OR 4-input OAI	2	14		

Note: OR-AND-Inverter unit cells are useful in implementing product-of-sums (POS) expressions.

Multiplexer Far	nily			<del></del>	
Unit Cell Name	Type	Description	Basic Cells	Drive (lu)	Function
T24*	4:1	Power 2-AND 4-wide Multiplexer	6	36	SOP
T26*	6:1	Power 2-AND 6-wide Multiplexer	10	36	SOP
T28*	8:1	Power 2-AND 8-wide Multiplexer	11	36	SOP
T32	2:1	Power 3-AND 2-wide Multiplexer	5	36	SOP
T33*	3:1	Power 3-AND 3-wide Multiplexer	8	36	SOP
T34*	4:1	Power 3-AND 4-wide Multiplexer	9	36	SOP
T42	2:1	Power 4-AND 2-wide Multiplexer	6	36	SOP
T43	3:1	Power 3-AND 3-wide Multiplexer	10	36	SOP
T44	4:1	Power 4-AND 4-wide Multiplexer	11	36	SOP
T54	4:1	Power 4-2-3-2 AND 4-wide Multiplexer	10	36	SOP
U24*	4:1	Power 2-OR 4-wide Multiplexer	6	36	POS
U26*	6:1	Power 2-OR 6-wide Multiplexer	9	36	POS
U28*	8:1	Power 2-OR 8-wide Multiplexer	11	36	POS
U32	2:1	Power 3-OR 2-wide Multiplexer	5	36	POS
U33*	3:1	Power 3-OR 3-wide Multiplexer	7	36	POS
U34*	4:1	Power 3-OR 4-wide Multiplexer	9	36	POS
U42	2:1	Power 4-OR 2-wide Multiplexer	6	36	POS
U43	3:1	Power 4-OR 3-wide Multiplexer	9	36	POS
U44	4:1	Power 4-OR 4-wide Multiplexer	11	36	POS

<sup>\*</sup> Convenient for typical multiplexer applications

Data Select	ors/Multip	lexers	7-11				
Unit Cell Name	Туре	Description	Basic Cells	Drive (lu)	Selects	Outputs	Bit Width
P24*	2:1	Data Selector	12	36	S, XS	Q	4
T2E	2:1	Selector	5	18	S	XQ	2
T2F	2:1	Selector	8	18	S	XQ	4
T2B*	2:1	Selector	2	18	S, XS	XQ	1
T2C*	2:1	Selector	4	18	S, XS	XQ	2
T2D*	2:1	Selector	2	14	S, XS	XQ	1
T5A*	4:1	Selector	5	9	S, XS	XQ	1
V3A*	1:2	Selector	2	14	S, XS	XQ	1
V3B*	1:2	Selector	4	14	S, XS	XQ	2

<sup>\*</sup> These are transmission gate devices whose outputs can be tied because they can be inhibited with true/inverted selects.

Decoders						
Unit Cell Name	Туре	Description	Basic Cells	Drive (lu)	Active Level Outputs	Enable
DE2	2:4	Decoder	5	18	Low	_
DE3	3:8	Decoder	15	14	Low	_
DE4	2:4	Decoder	8	14	Low	Low
DE6	3:8	Decoder	30	18	Low	1. High 2. Low

Internal Bus Unit Cells										
Unit Cell Name	Description	Basic Cells	Drive (lu)	Bus Size	Enable					
B41	4-bit Bus Driver	9	36	4 bits	Low					
B11	1-bit Bus Driver	5	36	1 bit	Low					

Data Latch	T	<del></del>	т	T		Υ	Г
Unit Cell- Name	Description	Basic Cells	Drive (lu)	Enable	Bits	Output	Clear
YL2	Data Latch with TM	5	36	High	1	Q	_
YL4	Data Latch with TM	14	36	High	4	Q	
LTK	Data Latch	4	18	Low	1	Q, XQ	Async
LTL	Data Latch with Clear	5	18	Low	1	Q, XQ	Async
LTM	Data Latch with Clear	16	18	Low	4	Q, XQ	
LT1	S-R Latch with Clear	4	18	Low	1	Q, XQ	Async
LT4	Data Latch	14	18	Low	4	Q, XQ	

Note: Y-type latches incorporate inhibit inputs and transparent mode (TM) to facilitate scan implementation.

Scan Fli	p-flop Family (Positive-Edge Tri	ggered)						
Unit Cell Name	Description	Basic Cells	Drive (lu)	Bits	Output	Clear	Preset	Clock Inhibit
SDH*	Scan D Flip-flop with 2:1 Multiplex	14	36	1	Q, XQ	Async	_	Yes
SDJ*	Scan D Flip-flop with 4:1 Multiplex	15	36	1	Q, XQ	Async	_	Yes
SDK*	Scan D Flip-flop with 3:1 Multiplex	16	36	1	Q, XQ	Async	_	Yes
SJH	Scan J–K Flip-flop	16	36	1	Q, XQ	Async		Yes
SDD*	Scan DFlip-flop with 2:1 Multiplex	16	36	1	Q, XQ	Async	Async	Yes
SDA	Scan 1-input D Flip-flop	12	36	1	Q, XQ	_	_	Yes
SDB	Scan 1-input D Flip-flop	42	36	4	Q, XQ	_	_	Yes
SHA	Scan 1-input D Flip-flop	68	18	8	Q, XQ	_	_	Yes
SHB	Scan 1-input D Flip-flop	62	18	8	Q	_		Yes
SHC	Scan 1-input D Flip-flop	62	18	8	XQ			Yes
SHJ*	Scan D Flip-flop with 2:1 Multiplex	78	18	8	Q, XQ	_	_	Yes
SHK*	Scan D Flip-flop with 3:1 Multiplex	88	18	8	Q, XQ			Yes
SFDM	Scan 1-input D Flip-flop	10	18	1	Q, XQ	_		Yes
SFDO	Scan 1-input D Flip-flop	11	18	1	Q, XQ	Async	_	Yes
SFDP	Scan 1-input D Flip-flop	12	18	1	Q, XQ	Async	Async	Yes
SFDR	Scan 4-input D Flip-flop	36	18	4	QA-QD	Async		Yes
SFDS	Scan 4-input D Flip-flop	31	18	4	QA-QD	_	_	Yes
SFJD	Scan J-K Flip-flop	14	18	1	Q, XQ		_	Yes

Note: \* Indicates D Flip-flop with multiplexed inputs.

Non-Sca	n Flip-flop Family							
Unit Cell Name	Description	Basic Cells	Drive (lu)	Bits	Output	Clear	Preset	Clock Inhibit
FDM	D Flip-flop	6	18	1	Q, XQ		_	Pos
FDN	D Flip-flop with Set	7	18	1	Q, XQ		Async	Pos
FDO	D Flip-flop with Reset	7	18	1	Q, XQ	Async		Pos
FDP	D Flip-flop with Set and Reset	8	18	1	Q, XQ	Async	Async	Pos
FDQ	D Flip-flop	21	18	4	Q			Neg
FDR	D Flip-flop with Clear	26	18	4	Q	Async		Pos
FDS	D Flip-flop	20	18	4	Q			Pos
FD2	Power D Flip-flop	7	36	1	Q, XQ	_	_	Neg
FD3	Power D Flip-flop with Preset	8	36	1	Q, XQ		Async	Neg
FD4	Power D Flip-flop with Clear and Preset	9	36	1	Q, XQ	Async	Async	Neg
FD5	Power D Flip-flop with Clear	8	36	1	Q, XQ	Async	_	Neg
FJD	Positive Edge Clocked Power J-K Flip-flop with Clear	12	36	1	Q, XQ	Async	_	Pos

Note: Synchronous flip-flops my be constructed by adding a simple AND gate (such as N2P) to the input of a flip-flop to create a synchronous clear

Scan C	Scan Counter Family										
Unit Cell Name	Description	Basic Cells	Drive (lu)	Bits	Outputs <sup>1</sup>	Load	Clear	Enable	Carry In	Up/ Down	
SC7 <sup>2</sup>	Scan 4-bit Synchronous Binary Up Counter with Parallel Load	62	36	4	Q, XQ, CO (S)	Sync		Low	High	Up	
SC8 <sup>2</sup>	Scan 4-bit Synchronous Binary Down Counter with Parallel Load	66	36	4	Q, XQ, CO (S)	Sync	_	High	Low	Down	
SC43	Scan 4-bit Synchronous Binary Up Counter with Asynchronous Clear	59	18	4	QA, QD,	Sync	Async	High	Low	Up	
SC47	Scan 4-bit Synchronous Binary Up/Down Counter	78	18	4	QA, QD,	Sync		Low		Up/ Down	

Notes: <sup>1</sup>(S), (A) indicate the counter is (S)ynchronous or (A)synchronous.

<sup>&</sup>lt;sup>2</sup>Scan counters include clock inhibit and high drive (CDR = 36 lu). For non-Scan counters CDR = 18 lu.

Non-So	Non-Scan Counter Family										
Unit Cell Name	Description	Basic Cells	Drive (lu)	Bits	Outputs <sup>1</sup>	Load	Clear	Enable	Carry In	Up/ Down	
C11 <sup>3</sup>	Non-Scan Flip-Flop for Counter	11	18	_	Q, XQ	_		_	_	_	
C41	Non-Scan 4-bit Binary Asynchronous Counter	24	18	4	Q, (A)	_	Async	_	_	Up	
C42	Non-Scan 4-bit Binary Synchronous Counter	32	18	4	Q	_	Async	_	_	Up	
C43	Non-Scan 4-bit Binary Synchronous Up Counter	48	18	4	Q, CO(S)	Sync	Async	High	High	Up	
C45	Non-Scan Binary Synchronous Up Counter	48	18	4	Q, CO	Sync	Sync	High	High	Up	
C47	Non-Scan Binary Synchronous Up/Down Counter	68	18	4	Q, CO	Async	_	Low	Low	Up/ Down	

Notes: 1(S), (A) indicate the counter is (S)ynchronous or (A)synchronous.

<sup>2</sup>Scan counters include clock inhibit and high drive (CDR = 36 lu). For non-Scan counters CDR = 18 lu.

<sup>&</sup>lt;sup>3</sup>C11 may by used for purposes other than counters.

Shift R	legister Family						
Unit Cell Name	Description	Basic Cells	Drive (lu)	Bit Width	Load	Outputs	Clock Polarity
	Serial-in Parallel-out ShiftRegister	18	16	4	Serial-In only	Q-Parallel	Neg
FS2	Shift Register with Synchronous Load	30	16	4	Sync-High	Q-Parallel	Neg
FS3	Shift Register with Asynchronous Load	34	18	4	Async-Low	Q-Parallel	Pos
SR1	Serial-in Parallel-out ShiftRegister with Scan	36	36	4	Serial-In only	Q-Parallel	Pos

# **CG10 Series CMOS Gate Arrays**

Datapat	h Operators (Adder, ALU, Parity)					
Unit Cell- Name	Description	Basic Cells	Drive (lu)	Bit Width	Outputs	Carry In
MC4	Magnitude Comparator	42	18 (=) 10 ( <, >)	4	A>B, A=B, A <b< td=""><td>A&gt;B,A=B,ALB</td></b<>	A>B,A=B,ALB
A1A	1-bit Half Adder	5	36	1	s, co	_
A1N	1-bit Full Adder	8	18	1	s, co	CI
A2N	2-bit Full Adder	16	14	2	s, co	CI
A4H	4-bit Binary Full Adder w/Fast Carry	48	18 (CO) 14 (S)	4	s, co	CI
PE5	Even Parity Generator/Checker	12	36	5	EVEN, ODD	_
PO5	Odd Parity Generator/Checker	12	36	5	ODD, EVEN	_
PE8	Even Parity Generator/Checker	18	18	8	EVEN, ODD	_
PO8	Odd Parity Generator/Checker	18	18	8	ODD, EVEN	_
PE9	Even Parity Generator/Checker	22	18	9	EVEN, ODD	_
PO9	Odd Parity Generator/Checker	22	18	9	ODD, EVEN	_

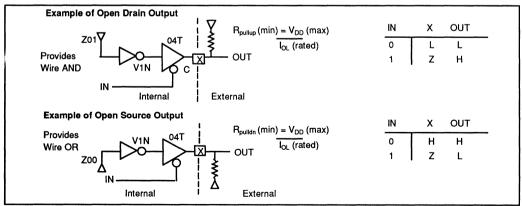
Miscellaneous Cells			
Unit Cell Name	Description	Basic Cells	Function
Z00	0 Clip	0	Tie to V <sub>SS</sub>
Z01	1 Clip	0	Tie to V <sub>DD</sub>

Input Buffe	er Family					
Unit Cell Name	Description	Basic Cells	Drive (lu)	Logic Level	Туре	Input/Output Polarity
I1B	Input Buffer	5	36	TL	Signal	Invert
I1BU	I1B with Pull-up Resistance	5	36	TL	Signal	Invert
I1BD	I1B with Pull-down Resistance	5	36	TL	Signal	Invert
12B	Input Buffer	4	36	보보	Signal	True
12BU	I2B with Pull-up Resistance	4	36		Signal	True
12BD	I2B with Pull-down Resistance	4	36		Signal	True
IKB IKBU IKBD	Clock Input Buffer IKB With Pull-up Resistance IKB with Pull-down Resistance	4 4 4	72 72 72	TTL TTL	Clock Clock Clock	Invert Invert Invert
IKC IKCD	Clock Input Buffer IKC With Pull-up Resistance IKC with Pull-down Resistance	4 4 4	200 200 200	CMOS CMOS CMOS	Clock Clock Clock	Invert Invert Invert
ILB	Clock Input Buffer	6	72	TTL	Clock	True
ILBU	ILB with Pull-up Resistance	6	72	TTL	Clock	True
ILBD	ILB with Pull-down Resistance	6	72	TTL	Clock	True
ILCU ILCD	Clock Input Buffer ILC with Pull-up Resistance ILC with Pull-down Resistance	6 6 6	200 200 200	CMOS CMOS CMOS	Clock Clock Clock	True True True
11C	CMOS Interface Input Buffer	5	36	CMOS	Signal	Invert
11CU	I1C with Pull-up Resistance	5	36	CMOS	Signal	Invert
11CD	I1C with Pull-down Resistance	5	36	CMOS	Signal	Invert
12C	CMOS Interface Input Buffer	4	36	CMOS	Signal	True
12CU	I2C with Pull-up Resistance	4	36	CMOS	Signal	True
12CD	I2C with Pull-down Resistance	4	36	CMOS	Signal	True
11S	Schmitt Trigger Input Buffer	8	18	CMOS	Schmitt	Invert
11SU	I1S with Pull-up Resistance	8	18	CMOS	Schmitt	Invert
11SD	I1S with Pull-down Resistance	8	18	CMOS	Schmitt	Invert
12S	Schmitt Trigger Input Buffer	8	18	CMOS	Schmitt	True
12SU	I2S with Pull-up Resistance	8	18	CMOS	Schmitt	True
12SD	I2S with Pull-down Resistance	8	18	CMOS	Schmitt	True
I1R	Schmitt Trigger Input Buffer	6	18	TTL	Schmitt	Invert
I1RU	I1R with Pull-up Resistance	6	18	TTL	Schmitt	Invert
I1RD	I1R with Pull-down Resistance	6	18	TTL	Schmitt	Invert
12R	Schmitt Trigger Input Buffer	8	18	TTL	Schmitt	True
12RU	I2R With Pull-up Resistance	8	18	TTL	Schmitt	True
12RD	I2R with Pull-down Resistance	8	18	TTL	Schmitt	True

Note: A "U" suffixed to the name of an input buffer indicates pull-up resistance of 50KΩ (typical) and a "D" indicates a pull-down resistance of the equivalent value.

Output Buffer Family							
Unit Cell Name	Description	Basic Cells	Drive (I <sub>OL</sub> )	Logic² Level	Туре	Edge Rate Control	Input/Output Polarity
O1B	Output Buffer	3	3.2 mA	TTL/CMOS	Standard	No	Invert
O1L	Power Output Buffer	3	12 mA	TTL/CMOS	Standard	No	Invert
O1S	Power Output Buffer	5	12 mA	TTL/CMOS	Standard	Yes	Invert
O2B	Output Buffer	2	3.2 mA	TTL/CMOS	Standard	No	True
O2L	Power Output Buffer	2	12 mA	TTL/CMOS	Standard	No	True
O2S	Power Output Buffer	4	12 mA	TTL/CMOS	Standard	Yes	True
O4T <sup>1</sup>	Output Buffer	4	3.2 mA	TTL/CMOS	3-state	No	True
O4W <sup>1</sup>	Power 3-state Output Buffer	4	12 mA	TTL/CMOS	3-state	No	True
O4S!	Power 3-state Output Buffer	5	12 mA	TTL/CMOS	3-state	Yes	True
O1R	Output Buffer	5	3.2 mA	TTL/CMOS	Standard	Yes	Invert
O2R	Output Buffer	4	3.2 mA	TTL/CMOS	Standard	Yes	True
O4R <sup>1</sup>	Output Buffer	5	3.2 mA	TTL/CMOS	3-state	Yes	True
O2S2	High Power Output Buffer	6	24 mA	TTL/CMOS	Standard	Yes	True
O4S21	High Power Output Buffer	7	24 mA	TTL/CMOS	3-state	Yes	True
O1BF	Output Buffer	3	8 mA	TTL/CMOS	Standard	No	Invert
O1RF	Output Buffer	5	8 mA	TTL/CMOS	Standard	Yes	Invert
O2BF	Output Buffer	2	8 mA	TTL/CMOS	Standard	No	True
O2RF	Output Buffer	4	8 mA	TTL/CMOS	Standard	Yes	True
O4RF	3-state Output Buffer	5	8 mA	TTL/CMOS	3-state	Yes	True
O4TF	3-state Output Buffer	4	8 mA	TTL/CMOS	3-state	No	True

Note: 1While all outputs are totem-pole type, Open Drain and Open Source types can easily be defined for all 3-state type outputs.



Note: 
<sup>2</sup>Totem pole outputs, such as these buffers have, can drive both TTL and CMOS levels. Voltage margins depend on actual source or sink current (see DC specifications).

# FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Bidirectio	nal I/O Buffers (Buses)					
Unit Cell Name	Description	Basic Cells	Drive (lu)	Logic Level	Туре	Input/Output Polarity
H6T	3-state Output and Input Buffer	8	3.2 mA	TTL	No	True
H6TU	H6T with Pull-up Resistance	8	3.2 mA	ΠL	No	True
H6TD	H6T with Pull-down Resistance	8	3.2 mA	TTL	No	True
H6W	Power 3-state Output and Input Buffer	8	12 mA	TTL	No	True
H6WU	H6W with Pull-up Resistance	8 8	12 mA	TTL TTL	No	True
H6WD	H6W with Pull-down Resistance	8	12 mA	IIL	No	True
H6C	3-state Output and CMOS		00-4	CMCC	NI-	T
H6CU	Interface Input Buffer H6C with Pull-up Resistance	8	3.2 mA 3.2 mA	CMOS CMOS	No No	True True
H6CD	H6C with Pull-down Resistance	8	3.2 mA	CMOS	No No	True
		•	3.2 IIIA	CIVIOS	INU	1108
H6E	Power 3-state Output and CMOS Interface Input Buffer	8	12 mA	CMOS	No	True
H6EU	H6E with Pull-up Resistance	8	12 mA	CMOS	No	True
H6ED	H6E with Pull-down Resistance	8	12 mA	CMOS	No	True
H6S	3-state Output and Schmitt		1			<del>                                     </del>
1103	Trigger Input Buffer	12	3.2 mA	смоѕ	No	True
H6SU	H6S with Pull-up Resistance	12	3.2 mA	CMOS	No	True
H6SD	H6S with Pull-down Resistance	12	3.2 mA	CMOS	No	True
H6R	3-state Output and Schmitt		<u> </u>			
	Trigger Input Buffer	12	3.2 mA	TTL	No	True
H6RU	H6R with Pull-up Resistance	12	3.2 mA	TTL	No	True
H6RD	H6R with Pull-down Resistance	12	3.2 mA	TTL	No	True
H8T	3-state Output and Input Buffer	9	3.2 mA	TTL	Yes	True
H8TU	H8T with Pull-up Resistance	9	3.2 mA	TTL	Yes	True
H8TD	H8T with Pull-down Resistance	9	3.2 mA	TTL	Yes	True
H8W	Power 3-state Output and Input Buffer	9	12 mA	TTL	Yes	True
H8WU	H8W with Pull-up Resistance	9	12 mA	TTL	Yes	True
H8WD	H8W with Pull-down Resistance	9	12 mA	TTL	Yes	True
H8W2	High Power 3-state Output and Input Buffer	11	24 mA	TTL	Yes	True
H8W1	H8W2 with Pull-up Resistance	11	24 mA	TTL	Yes	True
H8W0	H8W2 with Pull-down Resistance	11	24 mA	TTL	Yes	True
H8C	3-state Output Buffer and CMOS					
	Interface Input Buffer	9	3.2 mA	CMOS	Yes	True
H8CU	H8C with Pull-up Resistance	9	3.2 mA	CMOS	Yes	True
H8CD	H8C with Pull-down Resistance	9	3.2 mA	CMOS	Yes	True
H8E	Power 3-state Output Buffer and Interface Input Buffer	9	12 mA	смоѕ	Yes	True
H8EU	H8E with Pull-up Resistance	9	12 mA	смоѕ	Yes	True
H8ED	H8E with Pull-down Resistance	9	12 mA	CMOS	Yes	True

Note: A "U" suffixed to the name of a bidirectional buffer indicates a pull-up resistance of 50Ω (typical) and a "D" indicates a pull-down resistance of the equivalent value.

# FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Bidirectio	Bidirectional I/O Buffers (Buses) (Continued)						
Unit Cell Name	Description	Basic Cells	Drive (lu)	Logic Level	Туре	Input/Output Polarity	
H8E2	High Power 3-state Output and Input Buffer	11	24 mA	CMOS	Yes	True	
H8E1	H8E2 with Pull-up Resistance	11	24 mA	CMOS	Yes	True	
H8E0	H8E2 with Pull-down Resistance	11	24 mA	CMOS	Yes	True	
H8S	3-state Output and Schmitt Trigger Input Buffer True	13	3.2 mA	CMOS	Yes	True	
H8SU	H8S with Pull-up Resistance	13	3.2 mA	CMOS	Yes	True	
H8SD	H8S with Pull-down Resistance	13	3.2 mA	CMOS	Yes	True	
H8R	3-state Output and Schmitt Trigger Input BufferTrue	13	3.2 mA	ΠL	Yes	True	
H8RU	H8R with Pull-up Resistance	13	3.2 mA	ΠL	Yes	True	
H8RD	H8R with Pull-down Resistance	13	3.2 mA	TTL	Yes	True	
H6TFU	3-state Output and SchmittTrigger Input BufferTrue H6TF with Pull-up Resistance	8 8	8 mA 8 mA	TTL TTL	No No	True True	
H6TFD	H6TF with Pull-down Resistance	8	8 mA	TTL	No	True	
H6CF H6CFU H6CFD	3-state Output and Input Buffer H6CF with Pull-up Resistance H6CF with Pull-down Resistance	8 8 8	8 mA 8 mA 8 mA	CMOS CMOS CMOS	No No No	True True True	
H8TF H8TFU	3-state Output and Input Buffer H8TF with Pull-up Resistance	9 9	8 mA 8 mA	TTL TTL	Yes Yes	True True	
H8TFD	H8TF with Pull-down Resistance	9	8 mA	TTL	Yes	True	
H8CF H8CFU	3-state Output and Input Buffer H8CF with Pull-up Resistance	9	8 mA 8 mA	CMOS CMOS	Yes Yes	True True	
H8CFD	H8CF with Pull-down Resistance	9	8 mA	CMOS	Yes	True	

Note: While all outputs are totem-pole type, Open Drain and Open Source types can easily be defined for all 3-state type outputs, which includes all bidirectional buffers.

# **CG10 GATE ARRAY PACKAGE CHARACTERISTICS**

Dual In-line Pa	ackages (Standar	d DIP)				
	Packag	e Code				
Pinout Code	Plastic	Ceramic	Number of V <sub>DD</sub>	Number of V <sub>ss</sub>	Available Number or Signal Pins	
DIP-16	DIP-16P-MO2	DIP-16C-C03	1	2	13	
	DIP-16P-MO4					
DIP-18	DIP-18P-MO1	DIP-18C-CO1				
	DIP-18P-MO2					
DIP-20	DIP-20P-MO2	DIP-20C-CO2	1	2	17	
DIP-20U			1	1	18	
DIP-22	DIP-22P-MO2	DIP-22C-C02	2	2	18	
	DIP-22P-MO3					
DIP-22U			1	1	20	
DIP-24	DIP24P-MO1	DIP-24C-C01	2	2	20	
	DIP24P-MO2					
DIP-24U			1	1	22	
DIP-28	DIP-28P-M02	DIP-28C-C02	2	2	24	
	DIP-28P-M03					
DIP-28U			1	1	26	
DIP-40	DIP-40P-M01	DIP-40C-A01	2	4	34	
		DIP-40C-A02				
DIP-40U			1	1	38	
DIP-42	DIP-42P-MO1	DIP-42C-A01	2	4	36	
	DIP-42P-MO2					
DIP-42U			1	1	40	
DIP-48	DIP-48P-MO1	DIP-48C-A01	2	4	42	
	DIP-48P-MO2					
DIP-48U			1	1	46	

# CG10 GATE ARRAY PACKAGE CHARACTERISTICS (Continued)

Dual In-line Packages (Shrink DIP, 70 mil Pin Pitch)								
	Packaç	je Code	·					
Pinout Code	Plastic	Ceramic	Number of V <sub>DD</sub>	Number of V <sub>SS</sub>	Available Number of Signal Pins			
DIP-28SH			2	2	24			
DIP-28SHU			1	1	26			
DIP-42SH			2	4	36			
DIP-42SHU			1	1	40			
DIP-48SH			2	4	36			
DIP-48SHU			1	1	46			
DIP-64SH			2	4	58			
DIP-64SHU			2	2	60			

Dual In-line Packages (Skinny DIP, 300 mil Body Pitch)								
	Packaç	je Code	Number of V <sub>DD</sub>					
Pinout Code	Plastic	Ceramic		Number of V <sub>SS</sub>	Available Number of Signal Pins			
DIP-22SK			2	2	18			
DIP-22SKU			1	1	20			
DIP-24SK			2	2	20			
DIP-24SKU			1	1	22			
DIP-28SK			2	2	24			
DIP-28SKU			1	1	26			

Flatpack Packages (Dual-Leaded)								
Pinout Code	Package	Code						
	Plastic	Ceramic	Number of V <sub>DD</sub>	Number of V <sub>SS</sub>	Available Number of Signal Pins			
FPT-16	FPT-16P-MO3		1	2	13			
FPT-16U			1	1	14			
FPT-20	FPT-20P-MO2		1	2	17			
FPT-20U			1	1	18			
FPT-24	FPT-24-MO2		2	2	20			
FPT-24U			1	1	22			
FPT-28	FPT-28P-MO1		2	2	24			
FPT-28U			1	1	26			

# CG10 GATE ARRAY PACKAGE CHARACTERISTICS (Continued)

Flatpack Packages (Dual-Leaded)								
	Package (	Code						
Pinout Code	Plastic	Ceramic	Number of V <sub>DD</sub>	Number of V <sub>SS</sub>	Available Number of Signal Pins			
FPT-44			2	4	36			
FPT-44U			2	2	40			
FPT-48	FPT-48P-MO2		2	4	42			
FPT-48U			2	2	44			
FPT-48 *			2	4	42			
FPT-48U *			2	2	44			
FPT-64*	FPT-64P-MO1		2	4	58			
FPT-64U	FPT-70P-MO1		1	1	62			
FPT-80	FPT-80P-MO1		2	6	72			
FPT-80U			2	4	74			
FPT-100	FPT-100P-MO1		4	8	88			
FPT-100U			4	4	92			
FPT-120			6	12	102			
FPT-120U			4	8	108			
FPT-160			8	14	138			
FPT-160U			6	12	142			

<sup>\*</sup> Small body size.

Subject to Change

	Pack	age Code				
Pinout Code	Plastic	Ceramic	Number of V <sub>DD</sub>	Number of V <sub>SS</sub>	Available Number of Signal Pins	
PGA-64		PGA-64C-A02	2	4	58	
PGA-64U			2	2	60	
PGA-88		PGA-88C-A01	4	6	78	
PGA-88U			4	4	80	
PGA-135			8	12	115	
PGA-135U			4	8	127	
PGA-179			8	16	155	
PGA-179U			8	8	163	
PGA-208			12	18	178	
PGA-256			16	20	220	

# CG10 GATE ARRAY PACKAGE CHARACTERISTICS (Continued)

Flatpack Packages (Dual-Leaded)							
	Pack	age Code					
Pinout Code	Plastic	Ceramic	Number of V <sub>DD</sub>	Number of V <sub>SS</sub>	Available Number of Signal Pins		
LCC-28		LCC-28C-A02	2	2	24		
LCC-28U			1	1	26		
LCC-48		LCC-48C-A01	2	4	42		
LCC-48U			1	2	45		
LCC-64		LCC-64C-A01	2	4	58		
LCC-64U			2	2	60		
LCC-68			2	4	62		
LCC-68U			2	2	64		
LCC-84			4	6	74		
LCC-84U			3	4	77		

	Package	Code		1		
Pinout Code	Plastic	Ceramic	Number of V <sub>DD</sub>	Number of V <sub>ss</sub>	Available Number of Signal Pins	
PLCC-28	LCC-28P-M01		2	2	24	
PLCC-28U			1	1	26	
PLCC-44	LCC-44P-MO1		2	4	38	
PLCC-44U			1	2	41	
PLCC-68	LCC-68P-M01		2	4	62	
PLCC-68U			2	2	64	
PLCC-84	LCC-84P-M01		4	6	74	
PLCC-84U			2	4	78	

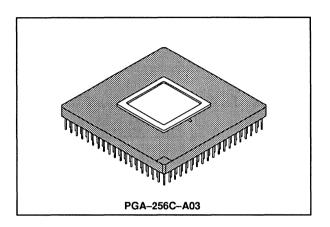
Subject to Change

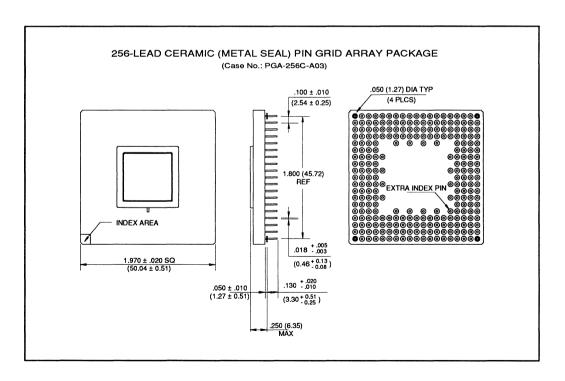
# **CG10 AVAILABLE PACKAGE TYPES**

								Numb	per of
	CG10272	CG10342	CG10492	CG10572	CG10692	CG10103	CG10133	V <sub>DD</sub>	V <sub>ss</sub>
DIP (Dual In-Line Package)									
DIP28	C, P	C, P	Р	Р				2 (1)	2 (1)
DIP40	C, P	C, P	Р	Р	Р			2 (1)	4 (1)
DIP42	C, P	Р	C, P	Р	Р			2 (1)	4 (1)
DIP48	C, P	C, P	C, P	Р	Р	_	_	2 (1)	4 (1)
SH-DIP (S	hrink Dual	In-Line Pac	kage)						
SH-DIP42	C, P	C, P	Р	Р	Р	_	_	2 (1)	4 (1 <sup>-</sup> )
SH-DIP64	Р	Р	Р	Р	Р	_	_	2 (2)	4 (2)
QFP (Qua	d Flat Pack	age)							
QFP48	Р	Р	Р	_	_	_		2	4
QFP64	Р	Р	Р	Р	Р	Р	_	2	4
QFP80	Р	Р	Р	Р	Р	Р		2 (2)	6 (4)
QFP100	Р	Р	Р	Р	Р	Р		4 (4)	8 (4)
QFP120	Р	Р	Р	Р	Р	Р	Р	6 (4)	12 (8)
QFP160	_	_	Р	Р	Р	Р	Р	8 (6)	14 (12)
QFP196		_	_	_	_	_	_	10	18
SQFP (Sh	rink Quad	Flat Packaç	je)						
SQFP64	Р	Р	_	_	_	_	_	2	4
SQFP100	P	Р	P	_	_		_	4 (4)	8 (4)
SQFP176	_	_	_	_	_	P	Р	8	16
SQFP208	_	_	_	_	_	_	Р	12	18
PGA (Pin	Grid Array	Package)							
PGA64	C, P	C, P	C, P	C, P	C, P	C, P	C, P	2	4
PGA88	C, P	C, P	C, P	C, P	C, P	C, P	C, P	4 (4)	6 (4)
PGA135	С	С	C, P	C, P	C, P	C, P	C, P	8 (4)	12 (8)
PGA179		_	C, P	C, P	C, P	C, P	C, P	8 (8)	16(8)
PGA208			_	_	С	С	С	12	18
PGA256	_	_		_	_	С	С	16	20
PGA-50 m	nil (Pin Gric	Array Pac	kage-50 mi	il)					
PGA256	T -		_			I -	С	16	20
PLCC (Pla	astic Leade	d Chip Car	riers)		-		***************************************	•	***************************************
PLCC68	Р	Р	Р	Р	Р	Р	T -	2	4
PLCC84	Р	Р	Р	Р	Р	Р	_	4 (2)	6 (4)

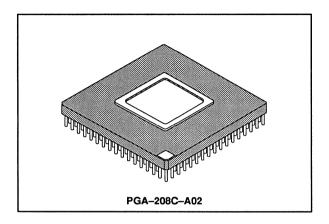
C = Ceramic, P = Plastic

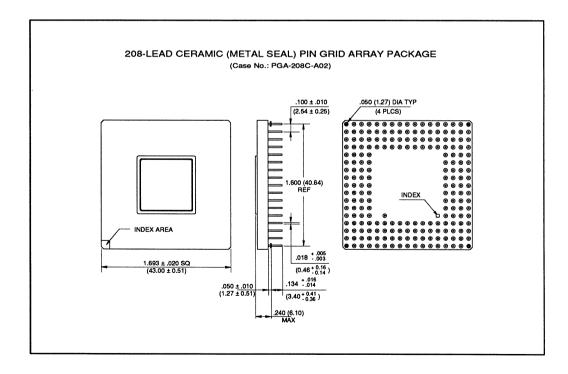
# PACKAGE DIMENSIONS





# PACKAGE DIMENSIONS (Continued)





# Chapter 2 - Steps Toward Design

## **Contents of This Chapter**

- 2.1 Introduction
- 2.2 Choosing Fujitsu as your ASIC Manufacturer
- 2.3 Choosing a Device
- 2.4 Choosing a Package
- 2.5 Technical Review
- 2.6 Design Interface Options

# 2.1 Introduction

This section of the data book takes a look at the issues that must be considered before a design is ready to be entered on a computer-aided engineering (CAE) workstation.

# 2.2 Choosing Fujitsu as Your ASIC Manufacturer

The first step in implementing a given ASIC design is to choose the manufacturer that offers semi-conductor processes capable of actualizing the performance requirements of the IC. The manufacturer should also offer consistent and easily accessible customer support, timely transfer of the design into silicon, and a highly reliable end product.

The data sheet and supplementary information in Chapter 1 enable customers to determine whether their requirements fall within the broad range of Fujitsu's technical capability.

The second step is to discuss the design requirements with one of Fujitsu's Field Applications Engineers at either a Regional Sales Office or a Technical Resource Center. Regional Sales Office and Technical Resource Center addresses and telephone numbers are listed at the back of this volume. Fujitsu's Field Applications Engineers work with each customer to determine which technology would be most suitable for a given design, taking into account the factors outlined in more detail below.

Fujitsu's highly developed software tools, high-capacity manufacturing facilities (the largest in the world) and long history of excellence in the field (Fujitsu has been producing custom gate arrays commercially since 1974) enable customers to turn designs into highly reliable products in a cost-effective time frame.

# 2.3 Choosing A Device

Speed is usually the deciding factor in choosing the technology for a design, but sometimes special requirements such as package availability or on-chip memory (available in the AU and CG21 technologies) influence the final decision.

Usually the device type is a requirement of the design and is chosen before the package size is determined. The size of the package will depend on array size, partitioning, the number of power and ground pins required by the SSOs (simultaneously switching outputs) used in the design, and the high power drive buffers and clock inputs used in the design.

To determine the most suitable device within a given technology, the designer must determine the gate count and pinout requirements from the schematic diagram of the design to be implemented.

The functions in the schematic or logic block diagram may be described using standard logic functions, programmable logic, or Fujitsu's Unit Cell Library.

Gate counts are calculated in terms of how many basic cells make up each component function (unit cell). This number is given for each unit cell in the unit cell library for each technology. By adding up the number of basic cells used in each logic element in a design, a designer can arrive at a good first estimate of the design complexity.

## 2.4 Choosing a Package

Before the final choice of an array can be made, however, the choice of a package must be considered. The intended use of the IC generally determines the type of package used: packaging issues are discussed in detail in the application note "Choosing the Best Package for Your ASIC Design" included in Chapter 7 of Section 1 of this data book. The types of packages available for Fujitsu's CMOS channeled arrays are shown in the data sheets in Section 1 and in Appendix D of the UHB Unit Cell Library (Section 2) and Appendix D of the CG10 Unit Cell Library (Section 3).

The size of the package chosen is regulated by the number of inputs and outputs required, the number of  $V_{SS}$  and  $V_{DD}$  pins required, and the number of simultaneously switching outputs (SSOs) included in the design.

## Package Size vs. SSOs

The number of SSOs can influence the size of the package chosen because additional ground pins are sometimes required in a design that has more simultaneously switching outputs than is acceptable for a given package type. Simultaneously switching outputs are those that switch from a logic low or a high impedance (Z) to a logic high or from a logic high or Z state to a logic low within 20 nanoseconds of each other.

A general rule is to use one ground pin for each group of 10 simultaneously switching low power outputs or for 20 non-simultaneous outputs. Chapter 4 of Section 1 of this book and the Package Pin Assignments section of the Design Manuals cover pin requirement issues in more detail.

Although the Vss and VDD pins are preassigned in each package and cannot be changed, alternate packages are available offering varying numbers of power and ground pins.

#### 2.5 Technical Review

When the CMOS technology, the device, and the package have been decided upon, the customer and Fujitsu's Field Applications Engineer hold a technical review to ensure that all the information necessary to implement the design is available and to allow Fujitsu to derive a schedule and price.

#### 2.6 Design Interface Options

The next step is to determine which computer-aided engineering (CAE) workstation will be used to enter the design. The desired result of entering the design on a CAE workstation is the generation of a successful net list or Fujitsu Logic Description Language (FLDL) file and a list of test vectors or Fujitsu Test Description Language (FTDL) file. These two files (which may be generated on any of several different CAE workstation systems) enable Fujitsu's host mainframe to perform automated layout and rigorous test and simulation of the design.

Four popular dedicated CAE workstation systems (Valid, Mentor, Dazix, and the HP 9000) as well as several hardware-independent CAE packages support Fujitsu's design software. In addition, Fujitsu now offers design support on ViewCAD™, a computer-aided engineering system originated by Fujitsu for ASIC designs.

ViewCAD is written in the C programming language and runs on any UNIX™ platform that supports the X Window System™ (such as the Sun 3 or 4 series of workstations). It includes in one package all of the necessary functions for the design, simulation, and analysis of an ASIC design. ViewCAD makes use of a graphics-oriented interface that allows visual examination of all circuits, circuit test data, and simulation results. Its final product is the logic and test data description files (FLDL and FTDL) that are required by the host mainframe computer to process a design.

Through long experience, Fujitsu has found that by far the most efficient way to achieve a trouble-free end product is for customers to implement the design on a workstation themselves. This can be done:

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- a. on CAD equipment that the customer is already using (Fujitsu provides cell library information files and the expertise to help write a conversion program to produce the FLDL and FTDL files if necessary)
- on one of the design systems that specifically support Fujitsu software (Daisy, Mentor, Valid, HP 9000) either at the customer's workplace or in one of the Technical Resource Centers
- c. on ViewCAD either on the customer's own Sun equipment or at a Technical Resource Center.

# Chapter 3 - Design Procedures

#### **Contents of This Chapter**

- 3.1 Introduction
- 3.2 Workstation Options
- 3.3 Workstation Design Procedures
- 3.4 Post-Design Process
- 3.5 Engineering Sample Testing

#### 3.1 Introduction

This section of the data book explains the steps necessary to implement an ASIC design in one of Fujitsu's channeled CMOS technologies using a computer-aided engineering (CAE) workstation. Designs can be implemented with Fujitsu's ViewCAD design software or with one of the CAE systems or software applications that support Fujitsu designs.

## 3.2 Workstation Options

#### 3.2.1 ViewCAD

Fujitsu developed the ViewCAD design software to generate the logic circuit (net list) and test data files necessary to design Fujitsu ASIC devices and to simulate the logic both before and after layout. ViewCAD complements a wide range of customer third party design tools and includes:

- · A Schematic Capture Module utilizing the X Window System
- A Logic Design Rule Check Module that screens for design violations in the areas of fanout and drive, gate count, I/O requirements, etc.
- A Test Data or Waveform Entry Module for test vector entry
- An Interactive Simulation Module that replicates the Fujitsu software for both functional and timing simulation
- Conversion Modules to define the net list in the Fujitsu Logic Description Language (FLDL) and the
  test vectors in the Fujitsu Test Data Description Language (FTDL) formats required by Fujitsu's
  design implementation software.

#### 3.2.2 Generic (CAE-dedicated) Workstations

Fujitsu provides ASIC Design Software Kits for designers using some of the popular design tools on generic hardware-dedicated CAE workstations. The kits offer support for Dazix, Mentor, Valid, and HP9000 and include:

- Fujitsu Symbol Model Libraries for the CAE system's schematic capture module
- A Logic Design Rule Check module
- Fujitsu Timing Model Libraries for the system's simulator
- A Delay Calculator module
- Conversion Modules to define the net list and test vectors in the FLDL and FTDL formats required by Fujitsu software.

In addition, Fujitsu now offers FAME (Fujitsu's ASIC Management Environment), a menu-driven design management program. FAME enables the user to select the technology, the array size, and the package, to assign the pinout, and to create a design database that is referenced by the other modules to ensure correct-by-construction design. FAME includes a test vector module that allows designers to edit test vectors, assists in defining test groupings, cycle times, and strobe settings, and checks created test files against restrictions.

Fuiltsu designs are also supported by several high-performance third party CAE tools. These include:

- · Verilog-XL® (Cadence Design Systems, Inc.) mixed-mode system simulator
- LASAR™ Version 6 (Teradyne) design simulator and test program generator with fault simulation
- HILO-3® (GenRad) design verification, fault simulation, and test generation tools
- IKOS™ 800 logic validation hardware accelerator
- Synopsys® Design Compiler™ interactive behavioral/logic synthesizer

## 3.3 Workstation Design Procedures

Figure 3–1 shows a flowchart of the design process. Because the function and file names used by each design system may differ, generalized names for each operation are used rather than system-specific names for each step in the process.

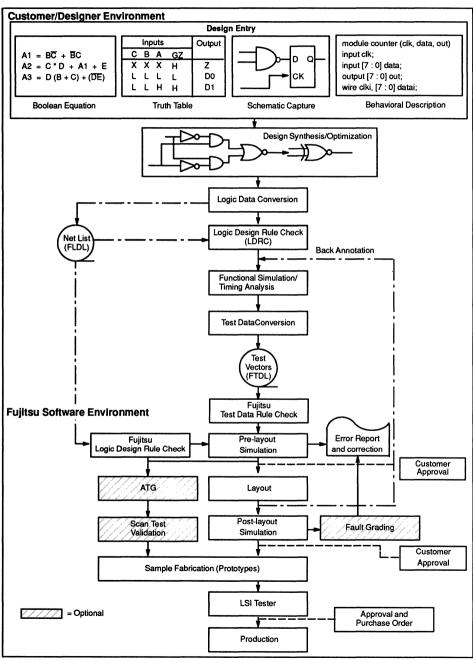


Figure 3-1. Workstation Design Flow

## 3.3.1 Design Entry

Design entry (schematic capture) is the first step in the design automation process. The designer can use the schematic editor program of ViewCAD or the applicable workstation software and Fujitsu's symbol model libraries for schematic capture. In most of the Fujitsu-compatible CAE applications, as in ViewCAD, circuits can be defined as macros, for use as sub-parts of other circuits. Designs can also be entered using Boolean equations, truth tables, or behavioral descriptions.

## 3.3.2 Design Synthesis/Optimization

The information entered in the design entry process can be subsequently subjected to design synthesis/optimization using a behavioral/logic synthesizer such as the one offered by Synopsis.

## 3.3.3 Logic Data Conversion (FLDL Generator)

Fujitsu's FLDL Generator (FLDLGEN) is a program that uses the results of data input (and design synthesis, if used) to create the FLDL file or net list. The purpose of the FLDL file is to provide information to the Fujitsu software environment for automatic layout and logic simulation.

The designer creates an FLDL control file containing the customer's name, the workstation type, the revision, the date, and the designer. The FLDLGEN program receives this information from the FLDL control file and combines it with the schematic data base file created at schematic capture. The FLDLGEN program can then create an FLDL file that describes the design for the Fujitsu design implementation software.

## 3.3.4 Logic Design Rule Check

The Logic Design Rule Check (LDRC) examines the files produced by the schematic capture and Fujitsu formatting processes for conformity to the design rules of the technology in which the design is executed. This program is run before simulation because it catches errors that, undetected under normal workstation design rules, often cannot be tolerated in a Fujitsu gate array. LDRC checks that the design conforms to the logic design rules applicable to all Fujitsu designs, to those unique to a technology, and to those required by the chosen package type. When hierarchy is used, LDRC checks for hierarchy violations.

Even in the general workstation environment, LDRC is Fujitsu software, written specifically for each trechnology.

In order to tailor the LDRC to a particular technology, device, and package, the customer enters required information via an LDRC Control File, which supplies the device and package name and sets the LDRC to output information in the form of a report either on all nets or only on nets that contain errors.

Errors detected during LDRC can then be corrected before the Logic Simulation Program is run.

## 3.3.5 Functional Simulation/Timing Analysis

The steps that make up the functional simulation and analysis process vary between design environments. For some workstations, as for ViewCAD, functional simulation is all one step, while for others it is three separate steps:

- Logic simulator data base file compilation
- b. Delay calculation
- c. Logic simulation and analysis

## Logic Simulator Data Base File

The logic simulator data base file uses a Fujitsu-supplied library to apply behavioral characteristics such as component functions, delay parameters, loading factors, and minimum pulse width, set-up time, and hold time for flip-flops. These values are supplied by the Fujitsu libraries for the appropriate technology. Input stimulus to the circuit is supplied by the designer in the form of the Control File.

#### **Delay Calculator**

Fujitsu provides the program for performing the delay timing calculations. The execution of the program calculates the delay times unique to each net in accordance with the loading condition (fan-out and hierarchy) in the schematic data file. These calculated delays are representative of pre-layout loading conditions.

The calculations for metal loading are based on the same look-up tables and load equations used in the Design Manual. These loads are subject to change after layout, reflecting the actual metal loads experienced.

## **Logic Simulator**

The event-driven logic simulator evaluates the outputs of each gate as a function of its inputs and displays the results as either a waveform drawing or as a data file. Workstation simulations performed under the influence of the Delay Calculator are vitally important to verification of design functionality and to the creation of successful test vectors. Using in-circuit application stimulus from the Logic Simulator Data Base File, simulations are executed in typical, maximum, and minimum modes, with timing checks enabled, to ensure that the design is responding as expected and is stable under all conditions. The results are written to a print-on-change file, which is a list of the signals that changed state, their new state, and the time at which they changed.

#### 3.3.6 Test Data Conversion (FTDL Generator)

Fujitsu's FTDL Generator (FTDLGEN) is a conversion program that translates the Functional Simulator's output file into the FTDL file. In the process of doing this, it applies Fujitsu tester restrictions to the simulator results. If any signal or timing violations are detected, the designer is informed so that the necessary changes can be made to the data file. The final output file of the FTDL Generator becomes the FTDL File, that is, the test vectors for Fujitsu's simulator as well as for the LSI tester.

#### 3.4 Post-Design Process

At this point, the customer has gone as far as possible in designing a CMOS gate array on a CAE workstation. Now the design is transferred to the Fujitsu software environment at one of the Technical Resource Centers for Fujitsu's simulation.

#### 3.4.1 LDRC and TDRC

The designer provides the FLDL and FTDL files to a Technical Resource Center usually in the form of magnetic tape or floppy disk. Fujitsu then checks the FLDL using its own proprietary and more detailed logic design rule check to confirm the validity of the logic data and for formatting errors, unconnected inputs and outputs, loading conditions, etc. The FTDL file is checked by Fujitsu's proprietary test data rule check, which flags any violations of the published test data restrictions.

#### 3.4.2 Pre-layout Simulation

After the LDRC and TDRC have been run successfully on the FLDL and FTDL, the pre-layout simulation can be performed. This is a logic simulation run at typical, maximum, and minimum propagation delay times using estimated metallization capacitance values. If there is no discrepancy between simulation

results and the expected outputs, the design is presumed to be correct. One of two simulators, LBS6 or ViewCAD, runs functional simulations and timing verification including the checking of set-up and hold time, pulse width, and removal times.

## 3.4.3 Automatic Layout

After a successful pre-layout simulation has taken place and customer approval has been obtained, a proprietary Fujitsu application performs automatic placement and metal interconnection routing.

# 3.4.4 Post-Layout Simulation

Post-layout simulation, also known as final validation, is again performed at typical, maximum, and minimum propagation delay times, but using actual calculated capacitance based on the metal interconnection routing resulting from automatic layout. Customers who are using ViewCAD can perform the Fujitsu pre-layout and post-layout simulation themselves using the ViewCAD software to provide a sign-off quality design before the design files are even turned over to Fujitsu.

#### 3.4.5 Fault Grading

After post-layout simulation is completed, customers have the option of requesting that Fujitsu subject the test data to a process called fault grading. This CPU-intensive process analyzes the customer's circuit and test data to calculate the percentage of fault coverage. The input test data is analyzed to determine the adequacy of the stimulus patterns to detect any "stuck" (malfunctioning) nodes. The result, a report of all nodes not tested by the stimulus provided, is given to the customer. The customer then has the option of either changing the test vectors or acknowledging that the untested nodes are acceptable.

# 3.4.6 Sample Fabrication

After a successful post-layout simulation has been performed and customer approval has again been obtained, engineering samples of the array are fabricated for customer evaluation.

## 3.5 Engineering Sample Testing

#### 3.5.1 LSI Tester

Once sample chips have been fabricated, they are tested on the LSI Tester, a test instrument located at the manufacturing facility. Sample chips are tested with input test patterns and expected outputs obtained from the FTDL file.

One of the most important tasks of post-layout simulation is to validate the test vectors for later use on the LSI Tester. For this reason, simulation is executed under conditions adhering as closely as possible to the conditions imposed by the tester. A device that passes all phases of simulation is likely to pass the LSI tester.

The limitations of the LSI Tester place various restrictions upon test data. These restrictions must be respected when preparing the test data pattern and when creating the (stimulus) Control file for running workstation simulations. A summary of test data restrictions for each technology is included in the appropriate Design Manual.

Test data restrictions involve such issues at the numbers of test patterns acceptable for each test type, the minimum test cycle length, input signal timing, output strobe timing, bidirectional buffer simulation, input and output cycle timing, tester skew, and the treatment of data signals.

Tests performed on the LSI Tester include the function test, the delay test, the DC test, and the high impedance ("Z function") test. Specific data found in the UHB or CG10 Design Manual must be included in FTDL to perform each of these tests.

## 3.5.2 Function Test

The function test guarantees the designed function of the gate array by exercising as many of the internal nodes as possible and detecting functional failures. Fujitsu requires the function test because it is the primary means of determining if an ASIC is functioning properly as it comes from manufacturing.

In the course of the function test, input signals are applied in accordance with customer timing specifications, using worst-case input voltage at a clock frequency not to exceed 16 MHz (a period of 63 ns). The dynamic performance of this test also partially verifies the AC characteristics of the device.

The function test may be run in multiple units (blocks), allowing changes to be made in the test vectors to assure thorough testing of the device. The transition from one block to the next requires that the device be powered off, adjustments made to the tester, and pins regrouped as required. After all changes have been made, the test is restarted. For this reason, each test block must re-initialize the circuit.

#### 3.5.3 Z-Function Test

The Z-Function test is administered in the last block(s) of the function test. Its purpose is limited to the verification of the high-impedance function of 3-state and bidirectional output buffers. The Z-function test is necessary only when there are two or more logic combinations that can generate the high-impedance state for a given I/O cell. The test can verify all these logic combinations. If only one logic combination generates the high-impedance condition, then the DC test is adequate.

#### 3.5.4 DC Test

The DC test, as its name implies, verifies the DC characteristics of the array. It is not intended to check circuit functionality, but it can be used as a function test of 3-state circuits having only one signal path that generates the high-impedance condition.

The designer supplies the sequence of input signals and expected outputs in the FTDL. These test patterns must generate every possible state for every type of output and input buffer being used (high, low, and high-impedance).

The DC test applies the designer-specified input signals to measure the following DC parameters:

- a. Steady state power supply current (IDDS)
- b. Output high voltage (VOH)
- c. Output low voltage (VOL)
- d. Input leakage current (III)
- e. High-impedance output leakage current (l<sub>1.7</sub>)

#### 3.5.5 Delay Test

The delay test is optional. It is used to verify critical paths or as a means to characterize the device by testing a small number of paths. The purpose of the delay test is to check that signal paths from various inputs of the chip to their respective outputs meet the customer's standards for minimum and/or maximum delay times. The paths may be sequential and/or combinatorial but only the propagation delay, not the toggle frequency, is measured.

# 3.6 ATG Testing and Scan Design

ATG testing is a special technique that supplements the customer's submitted test patterns (FTDL) to assure both Fujitsu and the customer of a highly reliable gate array by achieving a high degree of fault coverage. ATG testing is implemented by using scan design techniques described at the end of Chapter 4, Design Considerations. Scan test patterns (both applied input stimulus and expected outputs) are automatically generated by Fujitsu's Automatic Test Generator (ATG) software. ATG is offered by Fujitsu for partitioned arrays of the UHB and CG10 technologies and for all arrays in the channelless gate array technologies (AU, CG21, and CG31).

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# Chapter 4 - Design Considerations

## **Contents of This Chapter**

- 4.1 Introduction
- 4.2 Basic Cell Usage
- 4.3 Designing for Reliability and Testability
- 4.4 Designing for Speed
- 4.5 Bus Circuit Design
- 4.6 I/O Design
- 4.7 Designing for Scan Test Technology

#### 4.1 Introduction

This section of the data book gives an overview of the logic and I/O design considerations that are important for a successful design in Fujitsu's CMOS channeled gate array technology. Specific design recommendations for each technology can be found in the Design Manual for that technology.

## 4.2 Basic Cell Usage

In order to benefit from fully automated layout, a designer may use no more than 90% of the actual cell count of a UHB or CG10 gate array. The actual cell count is the number of basic cells used in the device.

In Fujitsu's channeled CMOS technologies, the unit cells are grouped in double columns alternating with wiring channels. Within the columnar architectures, unit cells are always constructed on a double column, i.e., a unit cell cannot bridge the wiring channel between two basic cell columns. This limits the number and complexity of unit cells that can be placed on a column.

The number of inputs and outputs and therefore input and output buffers required also limit the number of basic cells available for logic design since internal basic cells are also used for input/output buffer cell implementation.

#### 4.3 Designing for Reliability and Testability

Following the design guidelines below ensures maximum testability and therefore reliability of a design:

- a. External signal paths must be interfaced to the array by an I/O buffer.
- b. Only one I/O buffer cell can be connected to an external terminal.
- c. Inputs to the same cell may not be tied together.
- d. Inputs to two or more input buffers may not be tied together.
- e. Unused inputs must be tied high or low using clip cells Z00 or Z01, never left floating.
- f. The outputs of a unit cell other than 3-state bus macros may not be wire-ANDed. Generally, if output functions must be tied together, they must be combined through a logic function.
- g. Outputs of unit cells should not be left open. In the case of flip-flops, latches, shift registers, or counters, however, outputs may be left open if at least one output is connected.
- h. Functions such as one-shots and other monostable or astable circuits cannot be incorporated into a Fujitsu CMOS gate array. All logic state changes detected at the output of the array must be predictable for the purpose of test, and as such, be the direct result of changes of input stimulus.

- Series inverters must not be used for the purpose of creating a delay. Fujitsu supplies delay unit cells to assist the designer in solving timing problems such as set-up and hold time requirements. The designer should not, however, use delay cells to construct asynchronous circuits (one-shots or glitch generators).
- j. Circuits incorporating sequential devices (for instance, flip-flops, counters, shift registers, and so on) must have a traceable method of initialization designed into the circuit, independent of feedback loops.
- k. No logic function should be incorporated within the array if it cannot be directly or indirectly set or initialized from a primary input.

Designers have two choices for initialization:

- 1. Supply an external signal (for CLEAR, LOAD, etc.).
- Supply known inputs and allow time for them to propagate through the circuit. If the propagation method is used, UNKNOWN ("X" state) must be an acceptable output state until the initialization is completed.

## 4.4 Designing for Speed

In general, signal delays are caused by the signal having to travel through more gates or over longer distances, especially to enter a different block in gate arrays having block architecture (partitioned arrays). Delay is proportional to length of interconnection metal along which the signal must travel. The following recommendations are therefore made to optimize overall design speed by minimizing the interconnect metal length.

#### 4.4.1 Hierarchical Design

Devices that are not physically partitioned do not allow the designer to control relative path lengths. It is highly recommended, therefore, to design hierarchically, dividing the cell into blocks and the blocks into sub-blocks so that functional groups of unit cells are laid out in close proximity and signals have less far to travel. When it becomes necessary to link blocks, the use of high-power "high-drive" unit cells is recommended to drive signals in the inter-block metal.

It is especially helpful to use hierarchical design for the three largest arrays in the UHB and CG10 series. Not using hierarchy design for these larger arrays imposes a risk of considerable difference between estimated interconnection loading and actual layout loading values.

The suggested hierarchical structure for the larger arrays is a division of the array into four quadrants as shown in Figure 4–1. Each of these quadrants is considered a level 1 listing under the CHIP level. See Figure 4–2.

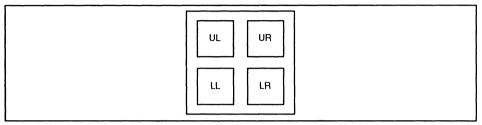


Figure 4-1. Arrangement of Hierarchical Blocks

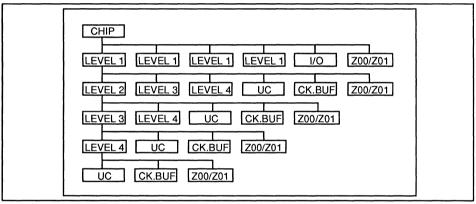


Figure 4-2. Recommended Hierarchial Organization of UHB/CG10 Designs

The CHIP level is the highest level in the hierarchy and represents the entire chip. All I/O cells are defined immediately below the CHIP level, along with any clip cells they may require.

Level 1 blocks must be defined immediately beneath the CHIP level and cannot exceed eight in number (when used for digital logic). Unit cells cannot be described immediately beneath the CHIP level.

Level 2 is defined beneath the Level 1 blocks, Level 3 beneath Level 2, etc. Levels must always be defined in numerical order. There is no limit to the number of Level 2, Level 3, or Level 4 blocks that may be used (when defined below a higher block level). Unit cells may be defined beneath Levels 2, 3, or 4, but the lower in the hierarchy the unit cells are defined, the greater the designer's control of delay will be.

Any level may be the first defined under the CHIP level and any of the levels may be omitted; however, the more the designer deviates from the standard structure, the greater the differences between estimated pre-layout delay and actual post-layout delay will be.

The recommended number of basic cells per each quadrant of an array is shown in Figure 4–1. It is highly recommended that the designer adhere to the guidelines in this table since the tables of estimated metallization load for the cells are based on these block sizes. The basic cell level counts overlap from level to level. The designer may select either of the levels covered by the cell count, but must also use the appropriate table of estimated metallization load for delay calculations.

Minimum BC/Block Maximum BC/Block Array/Series 6000UHB 1000 2500 8700UHB 1500 3000 12000UHB 2000 4000 CG10692 1200 2600 1700 CG10103 3400 CG10133 2300 4300

Table 4-1. Basic Cells per Quadrant

# 4.4.2 Clock Line Design

A clock network is a circuit used for the efficient distribution of an external clock signal to the clock input of internal sequential and combinatorial unit cells. Clock skew is the differential delay of a clock signal as it proceeds through a system; it is determined by the types and relative positions of the gates and blocks within the array. Clock networks must be optimized to minimize skews for both internal and inter-chip clock distribution to ensure accurate high-speed operation.

The designer can optimize clock networks by using dedicated input buffers called *clock input buffers* and dedicated unit cells called *clock distribution buffers*.

Clocks must enter the array through the clock input buffers. They should be further distributed via the clock distribution buffers. Proper use of clock buffers to boost signal strength and balance loads reduces the problems of clock skew and clock pulse variation. The locations of clock input buffers for signals with frequencies greater than 5 MHz are limited to paths on two sides of the die. The number of such buffers is limited depending on the size of the array, as specified in the design manual for each technology.

External clock signals must be wired in parallel with chips; once inside the chip, clock signals must be wired in parallel with logic blocks.

#### 4.5 Bus Circuit Design

The UHB and CG10 families have special provisions for implementing high-performance internal 3-state buses. The internal 3-state bus can be implemented on the chip using bus driver cells and bus terminators that maintain the last logic level on each bus line when all bus drivers switch to their high impedance state. The bus terminator maintains this logic level until any bus driver begins to drive the bus line. The bus terminator is invisible to a logic designer; it is connected to each of the bus lines automatically by Fujitsu's CAD software. It uses only one basic cell per bus line.

The number of internal 3-state buses permitted depends on the technology and on the size of the gate array and the bus width (number of bits per bus) required. Table 4–2 shows the number of bus driver cells permitted per UHB chip; Table 4–3 shows the number of bus driver cells permitted per CG10 chip.

Table 4-2. Maximum Number of Bus Driver Cells per Chip (UHB)

Device Name	Maximum B41 Bus Driver Cells
C330UHB	4
C530UHB	5
C830UHB	6
C1200UHB	8
C1700UHB	12
C2200UHB	16
C3000UHB	21
C4100UHB	26
C6000UHB	50
C8700UHB	70
C12000UHB	90

Table 4-3. Maximum and Recommended Number of Bus Driver Cells per Chip (CG10)

	B41 Bus Driver Cells		B11 Bus Driver Cells	
Device Name	Maximum	Recommended	Maximum	Recommended
CG10272	22	19	88	76
CC10392	26	23	104	92
CG10492	30	27	120	108
CG10592	34	30	136	210
CG10692	72	64	288	256
CG10103	105	94	420	376
CG10133	144	128	576	512

In the largest three arrays of both the UHB and CG10 technologies, there is also a limit on the number of bus driver cells per block (UL, UR, LL, LR, as shown in Figure 4–1) if the array is divided into the four recommended hierarchical blocks.

The maximum number of B41 bus driver cells (or CG10 B11 bus driver cells) permitted in each block is calculated using the following formulas.

## **B41 Bus Driver Unit Cells**

CG10692	(number of basic cells per block / 100) - 1
CG10103	(number of basic cells per block / 100) + 1
CG10303	(number of basic cells per block / 100) $-5$
C6000UHB	(number of basic cells per block / 100) - 2
C8700UHB	(number of basic cells per block / 100) + 1
C12000UHB	(number of basic cells per block / 100) - 4

#### **B11 Bus Driver Unit Cells**

The maximum number of B11 bus driver cells permitted in each block is determined by multiplying the permitted number of B41 bus driver cells by 4.

For example, if there are 3480 basic cells in a block of a CG10131 array:

$$3480/100 - 1 = 33.8$$

Therefore, a maximum of 33 B41s can be used in that block.

$$33 \times 4 = 132$$

A maximum of 132 B11s can be used in that block.

#### 4.6 I/O Design

## 4.6.1 Pin Assignment Guidelines

The following parameters apply to the assignment of I/O pins:

- a. All V<sub>SS</sub> pins must be tied to ground.
- b. All V<sub>DD</sub> pins must be tied to 5 volts.
- c. Voltage and ground pins are predetermined by the package type and cannot be altered.
- d. Pins designated "No Connection" cannot be used.
- Additional V<sub>SS</sub> and V<sub>DD</sub> pins may not be assigned by the designer without first negotiating this
  deviation with Fujitsu.
- f. Fujitsu recommends that the designer assign the pin numbers to the circuit in the \*ASSIGN or \*OPTION section of FLDL or submit the complete pin assignment table with the design. It is also possible to allow the Technical Resource Center to do the assignment automatically using Fujitsu's design software or manually from a customer-supplied form.
- g. The maximum output low current (IOL) must not exceed 70 mA per VSS Pin.

## 4.6.2 Simultaneously Switching Outputs (SSOs)

Outputs are defined as switching simultaneously when they switch from a logic low (or a high impedance state) to a logic high or switch from a logic high (or high impedance state) to a logic low within 20 nanoseconds of each other.

Simultaneously switching outputs increase the momentary charge/discharge current flow at the gate array and cause noise in the form of momentary spikes or ringing in the power and ground lines.

When the ground level is raised by the noise, the input threshold voltage of the gates is also raised, relatively, for the duration of the impulse (as illustrated in Figure 4–3). If  $V_{TH}$  rises, momentarily, above the  $V_{IHmin}$  level, a logic high with a level just above  $V_{IHmin}$  will be recognized as a low level for the duration of the spike. Similar problems are experienced when the ground level is depressed by the noise, affecting logic low levels close to  $V_{ILmax}$ .

The greater the number of SSOs, the greater the noise produced. Therefore, this noise, which may appear as signals to the CMOS logic, must be avoided.

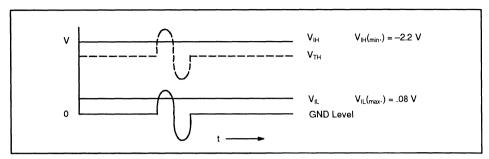


Figure 4-3. SSO-Generated Noise

The severity of the effect of SSOs is determined by:

- · The number of SSOs
- . The density and distribution of SSOs in the package
- · The size of the load capacitance being driven

The number of SSOs allowed in a package is restricted by the number of ground (VSS) pins available, the drive capability of the output buffers, and the location of ground pins on the package (See the Available Package and Pin Assignments section in the appropriate Design Manual). Representative values have been assigned to the effects of output buffers per single ground pin. Output buffers are capable of 3.2 mA, 8 mA, or 12 mA drive capability, and each may be selected with an optional noise-limiting resistance (NLR) value to minimize generated switching noise. The representative values are given in Table 4–4.

Output Buffer	Representative Values (per Output)
Normal Drive with NLR (I <sub>OL</sub> = 3.2 mA)	7
High Drive with NLR (I <sub>OL</sub> = 8 mA)	12
High Drive with NLR (I <sub>OL</sub> = 12 mA)	14
High Drive with NLR (I <sub>OL</sub> = 24 mA)	26
Normal Drive (I <sub>OL</sub> = 3.2 mA)	10
High Drive (I <sub>OL</sub> = 8 mA)	16
High Drive (I <sub>OL</sub> = 12 mA)	20

Table 4-4. Representative Value of Output Buffers

The sum of the representative values for each of the SSOs used in a design must not exceed 80 per V<sub>SS</sub> pin, regardless of the type of package used.

## 4.6.3 Maximum Load per Ground Pin

The maximum total output load per ground pin is limited as a function of the output switching frequency. The product of the output switching frequency in MHz and the total output load in pF per ground pin cannot exceed 12,700 pF x (frequency in MHz), at the maximum junction temperature,  $T_{jmax}$ , of 70°C. As the junction temperature increases, the allowable maximum load per ground pin decreases per the following formula:

 $C \times f \le (12,700 \times K_t) pF \times (f_{[MHz]}/(number of ground pins))$ 

where

C = the output load, in pF

f = the output switching frequency, in MHz

Kt = the junction temperature coefficient of load, a constant determined from Table 4–5.

Tj <sub>Max</sub> °C	Kt
70	1.0
85	0.7
100	0.5
125	0.3
150	0.2

Table 4-5. Junction Temperature Coefficient of Load

## 4.6.4 Maximum Load per Output Pin

The maximum total output load per output pin is limited as a function of the output switching frequency. The product of the output switching frequency in MHz and the total output load in pF of any pin cannot exceed 1200 pF x  $f_{MHz}$ , at a maximum junction temperature ( $T_{jmax}$ ) of 70°C. As the junction temperature increases, the allowable maximum load per output pin decreases per the following formula:

 $C \times f \le (1200 \times K_t)pF \times (f_{IMHz})/(number of ground pins)$ 

where

C = the output load, in pF

f = the output switching frequency, in MHz

Kt = the junction temperature coefficient of load, a constant determined from Table 4–2.

## 4.6.5 Pin Assignment Guidelines

The locations of all V<sub>SS</sub> and V<sub>DD</sub> pins are predetermined and fixed. Since the placement of SSOs on any package is critical, SSOs must be assigned within certain pin groups. Within these pin groups, other restrictions apply regarding the separation of SSOs from each other or their proximity to the V<sub>SS</sub> pins.

As noted above, the total representative value of any SSO group shown in Table 4–4 must not exceed 80. The SSO pin groups differ between packages. The package outlines and designated grouping of SSO pins for specific devices are shown in the Available Packages and Pin Assignment section of the appropriate Design Manual.

As a general rule, however, the pins available for SSOs between two V<sub>SS</sub> pins are assigned as shown in Figure 4–4.

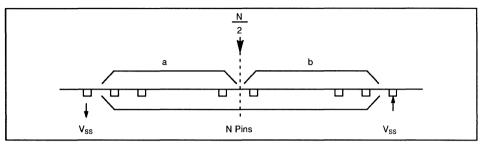


Figure 4-4. SSO Pin Assignments

- Assume that N pins exist between adjacent V<sub>SS</sub> pins
- Find the center point on the package between the two V<sub>SS</sub> pins
- There are N/2 pins in the area between the center point and the first V<sub>SS</sub> pin (part A), and N/2 pins in the area between the center point and the second V<sub>SS</sub> pin (part B)
- The SSOs must be equally distributed between parts A and B, within ±1

## 4.6.6 SSO Pin Placement Summary

The following is a general summary of recommendations for the placement of pins.

- a. SSOs must be placed in close proximity to V<sub>SS</sub> pins.
- b. High-drive SSOs should be placed closer to V<sub>SS</sub> pins than normal-drive SSOs.
- c. Asynchronous inputs such as clocks, presets, and clears should be kept away from SSOs. It is preferable that these inputs be placed close to V<sub>SS</sub> pins, if available, and away from SSOs.
- d. Clock, preset, and clear inputs must not be placed on the corners of a package, especially when the array is packaged in a DIP.
- Output signals to be used as clock, preset, or clear for other devices must be kept away from SSOs and close to a V<sub>SS</sub> pin.
- f. SSOs should not be placed in the outer row of pins of PGA packages.

#### 4.6.7 Test Pins

To facilitate testing, external pins should be provided whenever conditions warrant. The addition of supplementary test pins often allows the reduction of the overall test complexity for a circuit, thus reducing the number of test patterns required and the time necessary to determine functionality of the circuit.

## 4.7 Designing for Scan Test Technology

Scan testing is a supplementary, optional test technique that, when used in conjunction with the function and DC test required of the designer, allows greatly increased fault coverage. This increased fault coverage assures both Fujitsu and the designer of a highly reliable gate array.

# 4.7.1 Scan Test Design

The designer implements scan testing by arbitrarily connecting all the sequential logic elements to form an enormous shift register. This shift register can contain up to 3000 stages and is formed by connecting the Q-output of one stage to the dedicated scan input (SI) of the next. If the Q-output cannot be used for this

purpose, then the XQ-output may be used, but an inverter must be placed between the XQ-output and the SI input of the following stage in order that the data not be inverted.

To implement scan testing, designers use special scan-compatible unit cells for all sequential logic functions. With the use of the serial scan method, the difficult problem of testing a logic circuit containing both combinatorial and sequential logic is simplified to testing combinatorial logic and a shift register, as shown in Figure 4–5 below.

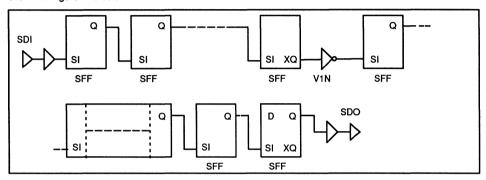


Figure 4-5. Scan Circuit Configuration

Dedicated scan inputs are also used to isolate elements that are not part of the scan test path. Some of these elements can also be tested during the scan test cycle by the use of an alternate scan test mode.

The scan chain design can be considered a data carrier with the ability to carry test input stimulus provided by the LSI tester deep into the design and to apply it to the unit cells under test. Once a unit cell has been tested, its output test result may be stored in the scan data chain and be carried out of the design for comparison to that which was expected. To the designer, scan unit cells perform exactly the same as non-scan unit cells, the only difference being the provision of additional basic cells to facilitate the scan test.

Scan testing usually entails an extra 8 to 20 percent basic cell count, requires the use of seven extra I/O pins, and can cause some degree of propagation delay. Nevertheless, when absolute reliability is the issue, designers find that these considerations are within an acceptable range.

# 4.7.2 Test Pattern Generation

A circuit that is designed for scan testing in this way allows Fujitsu automatic test pattern generation (ATG) software to generate the scan test patterns automatically (both applied input stimulus and expected outputs). The ATG software uses the logic design data from the FLDL file as input from which it generates the test patterns for scan tests. The process requires that all sequential unit cells be of the scan type with the exception of data latches YL2 and YL4. Inclusion of non-scan sequential circuits constructed with combinatorial logic, (i.e., NAND-gate flip-flops, NOR-gate flip-flops, etc.), are discouraged in a scan design because they reduce the overall fault coverage attainable with scan testing. If their use is unavoidable, they must be disabled or isolated by one of the scan test signals discussed below during the ATG process and the scan test.

Scan testing is optional and is applicable only to digital logic unit cells.

#### 4.7.3 Scan Test Signals

Scan test implementation requires the assignment of a dedicated output pin and up to six input pins, six of which are in predefined package locations. The package locations for these pins in each device type are shown in the Available Package and Pin Assignment section of the appropriate Design Manual.

## Pin Name Description

- XACK is the scan input, scan output (SISO) A-clock signal. It is generated by the LSI tester and is applied, inverted, to all scan devices at their A-clock input. It writes data from the unit cell's scan input to the master latch.
- 2. BCK is the SISO B-clock signal. It is generated by the LSI tester and is applied, inverted, to all scan devices at their B-clock input. It transfers data between the unit cell's master and slave latches (the output of the device).
- 3. XSM is the SISO mode signal. It is used for set-up of bidirectional buffers, bus drivers, and RAM. If bidirectional buffers or bus drivers are not used, then XSM is not required and need not be included in the design.
- 4. XTST is the scan test signal. It is used to reconfigure the array to make it suitable for scan test and to establish all conditions required for the use of Fujitsu's ATG software. This includes the isolation or removal of certain circuits unsuitable for scan testing, such as non-scan sequential functions and the asynchronous inputs of all sequential elements. (Since they are inaccessible to scan testing, these circuits and disabled functions must, therefore, be tested with user-prepared test patterns.)
  - If all sequential functions utilize scan type unit cells, if no asynchronous functions are employed (including direct sets and clears), and if circuit isolation is not required, then XTST is not required and is not provided for.
- 5. XTCK is the TC mode clock signal. It is generated by the LSI tester. It is applied, inverted, to the IH-inputs of all sequential unit cells.
- 6. SDI is the serial data input port to the first device of the scan path from outside the chip. It is connected to the SI port of the unit cell. Test data entering the SI input in subsequent devices in the scan path is derived either from the Q-Output of the immediately previous stage or via an inverter from the XQ-output.
  - SDI is the only one of the scan test ports that may be used for another function. The designer may use SDI as a principal input by paralleling the user input with the scan data input.
- 7. SDO is the serial data output port from the last device of the scan-configured shift register to the environment outside the chip. Test data from SDO is taken from the Q-output of the last stage (or from the XQ-output via an inverter) of the giant scan shift register. SDO is the only one of the scan test ports whose location is not fixed; SDO may be placed by the designer at any convenient location.

## 4.7.4 Scan Test Modes

Scan testing consists of two modes of operation: SISO (Scan input/scan output) mode and TC (test clock) mode. Sequential logic is primarily addressed by SISO and combinatorial logic is addressed by TC; the two modes are alternated during the scan test.

#### The SISO Mode

This mode causes all elements of the scan path to be written to and read from. In this mode of operation, the following occurs:

a. The scan SISO path is activated by making XSM = 0

- b. The scan clocks XACK and BCK are supplied
- c. The data to be written is supplied to SDI serial data input
- d. The data is read out of SDO and compared with the expected values

These writing and reading operations are performed in parallel.

#### The TC Mode

This mode tests the array as a normally configured device, but the data is clocked by special clocks provided to the gate array by the LSI tester. In this mode of operation, the following occurs:

- a. The scan SISO path is disabled by making XSM = 1.
- All normal system clocks are disabled, forcing the clock inputs (CK) of all scan unit cells to a logic low.
- c. Input signals are applied to the normal input pins' principal inputs.
- d. The TC system clock, XTCK, is applied to the unit cells' IH-inputs.
- Output signals are read from the normal output pins' principal output and compared with the expected values.

The alternation of these two modes allows the correct functioning of logic elements not directly accessible from a principal input to be verified. The data scanned in is especially useful in providing control inputs to otherwise difficult-to-control internal logic. Prior to the input of the data to the scan path, some detectable faults can be observed externally by application of data to some non-scan external inputs. After data has been clocked into the scan path, other detectable faults can be observed externally. The remaining detectable faults are observable externally after the data has been clocked into the scan path, the TC system clock (XTCK) has been applied, and the resultant data shifted out of the scan path.

# 1

# Chapter 5 - Delay Estimation Principles

#### **Contents of This Chapter**

- 5.1 Introduction
- 5.2 Choosing Critical Paths
- 5.3 Load Units and Loading Guidelines
- 5.4 The Delay Equation
- 5.5 Estimating Gate Delay
- 5.6 Estimating Total Circuit Delay
- 5.7 Delay Calculations when Load Exceeds CDR
- 5.8 Delay Calculations and the Operating Environment
- 5.9 Clock Loading

#### 5.1 Introduction

This section of the data book gives an overview of the engineering considerations important to the design of an ASIC using Fujitsu's CMOS technologies. Included are the loading rules for CMOS gate arrays and a demonstration of how to estimate the delay through a circuit. In addition to the basic delay equation, this chapter also considers the loading limitations for clock signals and the effects of the operating environment on typical delay figures.

#### 5.2 Choosing Critical Paths

A critical path is a logic path whose timing requirements must be satisfied to ensure proper system function. In an ordinary synchronous circuit, data propagates from one register through combinatorial logic into another register. For the circuit to function properly, the sum of the clock-to-Q delay of the source register, the propagation delay through the logic, and the set-up time on the target register must be less than the worst-case system clock period. Correct timing of the signal along the critical path guarantees that this condition is met.

Usually, the critical path is the one with the greatest number of gate levels. However, if such a path is speeded up by redesign, another, less complex path may become the new critical path.

For example, in a design in which a path has eight levels of gating, the designer may determine upon inspection that two groups of NAND-NAND structures can be changed to AND-OR inverters, an efficient CMOS implementation that noticeably increases the speed of the path. In this case, after applying DeMorgan's theorem and reducing the result, the designer finds that another path is now the critical path.

Since each logic state sensitizes different branches, logic paths must be analyzed using the inputs (rising or falling) that will actually be applied to them (since rising and falling delays are not equal) to determine the longest path that will be sensitized and ensure that it meets critical path requirements.

The path delay calculation worked through in this section shows how a designer can analyze each element of a Fujitsu CMOS circuit to make sure the design meets critical path requirements. In this case, the effect of a rising input on the sample circuit is calculated as it would be if this were a critical path and the rising input were forcing the transition of interest.

## 5.3 Load Units and Loading Guidelines

The Fujitsu CMOS load unit (lu) is the input capacitance of an inverter used as the basic unit for measurement and calculation of capacitive loads presented to unit cells within the gate array. Both the output drive factor of a unit cell and its input load factor are defined in terms of load units. Both factors are listed for each unit cell in the unit cell library for the appropriate technology.

#### 5.3.1 Output Drive Factor

The output drive factor ( $C_{DR}$ ) is a parameter expressing the load driving capability of a unit cell. Unit cells can drive loads greater than the output drive factor. The performance of CMOS circuits degrades exponentially with increased loading; if too great a load is driven, an exaggerated increase in delay through the unit cell may be experienced.

It is permissible for the load to exceed  $C_{DR}$  if the associated additional delays are anticipated and tolerable. Additional calculation factors are required to estimate delays of loads greater than  $C_{DR}$ . Figure 5–1 indicates the delays that may be generated when the load exceeds these guidelines.

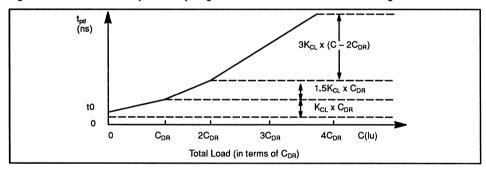


Figure 5-1. Delay Time vs. Loading Factor

## 5.3.2 Input Load Factor

The input load factor of a unit cell is used to estimate the propagation delay of a critical path in a design. The total propagation delay of a path is defined as the sum of the delay factor of each of the unit cells in the path.

# 5.3.3 Delay Factor

The delay factor of each unit cell is made up of two types of capacitive loading:

- a. Load capacitance inherent in the input of each cell (the input loading factor)
- b. Load capacitance due to the metal interconnection of unit cells (C<sub>L</sub>)

The total load (C) presented by a unit cell is estimated by adding the total cell input load or  $N_{F/C}$  (the input loading factors of all other cells connected to the output network of the cell in question) to the total metal load ( $C_1$ ),

or 
$$C = N_{F/O} + C_I$$

# 5.4 The Delay Equation

The basic delay equation combines the AC parameters of a cell and its associated capacitive loads to estimate the delay time through the cell. The rise and fall time of a unit cell may not be symmetrical due to differences in the transconductivity of the N and P transistors as well as to differences in the arrangement of the transistors to form unit cells. The same equation is used with different variables for positive-going and negative-going signals at the unit cell output. These signal polarity variables must be considered separately.

$$t_{up} = t_{0up} + K_{CLup}(N_{F/O} + C_L)$$

$$t_{dn} = t_{Odn} + K_{Cl,dn}(N_{E/O} + C_l)$$

where:

toxx is the circuit delay through the unit cell under no-load conditions (a value given in ns for each cell in the unit cell library).

K<sub>CL</sub>xx is the load derating constant or delay time per loading unit conversion factor (ns/pF) defined for each unit cell (and given in the unit cell library).

N<sub>E/O</sub> is the sum total of the input loads of all unit cells driven on the net (expressed in load units).

C<sub>L</sub> is the amount of loading, in load units, on the unit cell output due to interconnect metal (metal load).

The term "net" refers to the network of metal wiring connecting all the unit cells driven by a specified unit cell. Interconnect metal refers to the metal wiring, also called routing metal, that makes up each net.

# 5.5 Estimating Gate Delay

Figure 5–2 shows a sample circuit for the purposes of demonstrating how the total accumulated delay (tpd) through a short path is estimated.

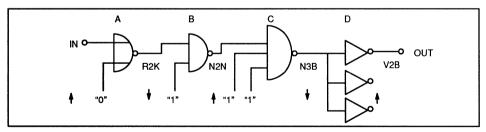


Figure 5-2. Delay Path Sample Circuit

Ordinarily a designer looks up the the specifications of each unit cell in the unit cell library of the applicable technology. For this example, however, all of the necessary specifications have been assembled in Table 5–1, using the values for UHB technology.

		Basic	Input	Output	Propag	ation I	Delay Ti	me
Cell	Celi	Cells	Load	oad Drive			t <sub>dn</sub>	
Function	Name	Used	Factor	Factor	t0	K <sub>CL</sub>	t0	K <sub>CL</sub>
2-Input NOR	R2K*	2	2	36	0.45	0.14	0.45	0.06
2-Input NAND	N2N	1	1	18	0.37	0.16	0.56	0.14
3-Input NAND	N3B*	3	1	36	1.28	0.08	1.70	0.04
Inverter	V2B	1	2	36	0.25	0.08	0.25	0.05

Table 5-1. AC Parameters of Unit Cells

The delays for rising  $(t_{up})$  and falling  $(t_{dn})$  edges of a pulse can differ widely. Digital pulses are either lengthened or shortened while passing through a unit cell. It is therefore important to calculate the pulse width variations along the entire signal path to verify that pulse width is sufficient to pass through each gate.

In the example that follows, based on Figure 5–2, calculations are based on a rising pulse entering the input of unit cell A and changing state several times as it proceeds through the sample circuit. To find the total delay for the circuit, it would be necessary to calculate the values resulting from the opposite case, in which a falling pulse enters the circuit at unit cell A.

### 5.5.1 Delay Parameter for Rising Edge (tup)

The unit cell library shows that the delay time ( $t_0$ ) for an upward transitioning signal at the unit cell output ( $t_{up}$ ) for R2K, a 2-input NOR, is 0.45. It shows that the load/delay conversion factor for an upward transitioning signal ( $K_{CLup}$ ) for R2K is 0.14.

### 5.5.2 Number of Fan-outs (N<sub>F/O</sub>)

The sample schematic in Figure 5–2 shows that the  $N_{F/O}$ , the number of cells that the R2K must drive, is one (an N2N). The unit cell library shows that the N2N has an input load factor of 1 lu.

### 5.5.3 Number of Driven Inputs (N<sub>Di</sub>) and Metal Load (C<sub>I</sub>)

The value for  $C_L$  is based on the number of inputs the cell in question must drive and is derived from the Estimation Tables for Metal Loading at the beginning of the unit cell library. Table 5–2 is a sample metal load table; each technology and device has unique load/delay characteristics. Since the number of driven inputs (or  $N_{DI}$ ) for R2K, N2N, and V2B in Figure 5–2 is one, the amount of loading due to metallization (L) is 1.0 lu. The  $N_{DI}$  for N3B in Figure 5–2 is three; therefore the  $C_L$  is 3.0.

<sup>\*</sup>These are high drive cells that operate faster than their low drive equivalents under these circumstances.

abie 5–2. NDI VS. CL						
N <sub>DI</sub>	C <sub>L</sub> (lu)	l				
1	1.0	l				
2	2.2	l				
3	3.0	l				
4	3.5	l				
5	3.9	l				
6	4.2	l				
7	4.6	l				
8	4.8	ı				
9	4.9	ı				
10	5.0	ı				

Table 5-2. N<sub>DI</sub> vs. C<sub>L</sub>\*

The value given for  $C_L$  in the Estimation Tables for Metal Loading is an estimate of the loading effect of the metallization capacitance on the output based on Fujitsu's careful statistical analysis of typical designs. Actual metal loading is based on the effect of the routing and therefore may vary from these estimates. To compensate for this uncertainty, Fujitsu incorporates  $a\pm 5$  percent variation into the prelayout delay multipliers. After routing, another set of simulations is run to verify the effect of the actual metal routing.

Note: In an array partitioned into blocks, if the interconnected unit cells are located in different blocks, the loading is greatly increased. The designer can avoid this worst-case situation by using the hierarchical approach during the schematic capture process to confine circuits to one block whenever path delay is critical.

### 5.6 Estimating Total Circuit Delay

Based on the values from Table 5-1 and Table 5-2, the propagation delay for R2K in the sample circuit is:

```
t_{dn} A = t_{Odn} + K_{CLdn} (N_{F/O} + C_L)

t_{dn} = 0.45 + 0.06 (1 + 1.0)

t_{dn} = 0.45 + 0.06 (2.0)

t_{dn} = 0.45 + 0.12

t_{dn} = 0.57

t_{dn} A = 0.6 (rounded up to the next 0.1 ns)
```

The propagation delay for N2N, found by following the same procedure, is:

<sup>\*</sup> For a 330UHB gate array.

The propagation delay for N3B, found by following the same procedure, is:

```
\begin{array}{llll} t_{oln} & C & = & t_{oln} & + & K_{CLdn} \left( N_{F/O} + C_L \right) \\ t_{dn} & = & 1.70 & + & 0.04 \left( 3 + 3.0 \right) \\ t_{dn} & = & 1.70 & + & 0.04 \left( 6.0 \right) \\ t_{dn} & = & 1.70 & + & 0.24 \\ t_{dn} & = & 1.94 \\ t_{dn} & C & = & 2.0 & (rounded up to the next 0.1 ns) \end{array}
```

The propagation delay for V2B, found by following the same procedure, is:

```
\begin{array}{lcll} t_{\rm up} \, D & = & t_{\rm Oup} & + & K_{\rm CLup} \, (N_{F/O} + C_{\rm L}) \\ t_{\rm up} & = & 0.25 & + & 0.08 \, (1 + 1.0) \\ t_{\rm up} & = & 0.25 & + & 0.08 \, (2.0) \\ t_{\rm up} & = & 0.25 & + & 0.16 \\ t_{\rm up} & = & 0.41 \\ t_{\rm up} \, D & = & 0.5 & (rounded up to the next 0.1 \, ns) \end{array}
```

Therefore, the delay for a rising pulse through the sample circuit shown in Figure 5-2 is:

$$t_{pd} = t_{dn} A + t_{up} B + t_{dn} C + t_{up} D$$
  
 $t_{pd} = 0.6 + 0.7 + 2.0 + 0.5$   
 $t_{pd} = 3.8 \text{ ns}$ 

### 5.7 Delay Calculations when Loads Exceed CDR

Fujitsu CMOS unit cells are capable of driving loads beyond their published Output Drive Factor ( $C_{DR}$ ). It must be emphasized, however, that the delays that result from this practice are considerably increased. Unit cells may be loaded beyond their  $C_{DR}$ s provided that the increased delay is acceptable.

Anticipation of the effects of loading beyond the published  $C_{DR}$  requires recalculation of delay. Different delay equations must be used depending on the technology being used and the amount that the loading exceeds  $C_{DR}$ .

The different delay equations listed below for Fujitsu's channeled gate array technologies must be used depending on the degree that the loading exceeds  $C_{DR}$ .

When C is CDR or less:

```
t_{pd} = t_0 + (K_{CL} \times C) where C = N_{F/O} + C_L
```

When C is between  $C_{DR}$  and  $2C_{DR}$ :

$$t_{pd} = t_0 + (K_{CL2} \times C_{DR2}) + K_{CL} (C_{DR} - C_{DR2}) + 1.5 K_{CL} (C - C_{DR})$$

When C is between  $2C_{DR}$  and  $3C_{DR}$ :

$$t_{pd} = t_0 + (K_{CL2} \times C_{DR2}) + K_{CL} (C_{DR} - C_{DR2}) + (1.5 K_{CL} \times C_{DR}) + 3K_{CL} (C - 2C_{DR})$$

When C is greater than 3CDR: FORBIDDEN

In these equations:

 $K_{CL2}$  is an initial delay time per load unit defined for cells that have been assigned a  $C_{DR2}$  value.

 $C_{DR2}$  is an initial output driving factor defined for certain cells.  $C_{DR2} = 0$  when the value is not defined in the specification for the cell in the unit cell library.

Some additional calculations are required to estimate the delay of a downward transitioning signal through certain cells for which the parameter  $C_{DR2}$  has been assigned. For these cells, when C is equal to or less than  $C_{DR2}$ , the following formula is used:

$$t_{od} = t0 + (K_{Cl} \circ x C)$$

When C is between  $C_{DR2}$  and  $C_{DR}$ , the following formula is used:

$$t_{pd} = t0 + (K_{CL2} \times C_{DR2}) + (K_{CL} \times (C - C_{DR2}))$$

**NOTE:** Clock networks are never loaded beyond  $C_{DR}$  because clock timing is critical to the proper functioning of the gate array. (See Section 5.9)

### 5.8 Delay Calculations and the Operating Environment

The operating environment of the array can cause variations from the calculated typical delay figures. Influencing factors include ambient temperature, applied voltage, and variations in the manufacturing processes. Figure 5–3 shows how supply voltage and temperature affect the performance of a sample array. It is necessary, therefore, to simulate worst-case conditions during test. Revised estimates of delay under these harsher circumstances may be arrived at by multiplying the typical delay figures by delay multipliers. The actual multipliers used depend on the device technology and/or the device type.

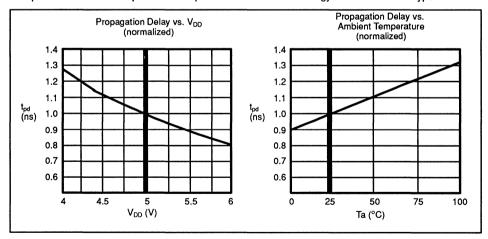


Figure 5-3. Factors Influencing Delay

### 5.8.1 Minimum/Maximum Pre-Layout Delay Multipliers

The minimum delay multiplier and the maximum delay multiplier for Fujitsu's channeled CMOS technologies given in Table 5–3 below incorporate process, power supply, and temperature variation.

Table 5-3. Pre-Layout Delay Multipliers

Technology	Minimum Delay Multiplier (0°C, 2.5 V)	Maximum Delay Multiplier (70°C, 4.75 V)
UHB Technology	0.35	1.65
CG10 Technology	0.35	1.65

These delay multipliers are applied in one of two different ways, depending upon whether they are to be used for the optional delay test calculations or for the other tests performed by Fujitsu using the information in the Fujitsu Test Description Language (FTDL) file, such as DC test, function test, or high impedance test.

### 5.8.2 Delay Calculations for Delay Test (AC Test)

The min/max delays for the delay test are determined by taking the sum of the typical delays and multiplying it by the appropriate minimum or maximum delay factor. The maximum delay figure must be rounded up to the next highest 0.1 ns, while the minimum delay figure must be rounded down to the next lowest 0.1 ns. The result of the sample equation used in section 5.6 to show delay calculation is repeated here and also shown in its modified form. The delay factors used are those for UHB technology.

Typical delay:

$$t_{\text{nd}} = 0.6 + 0.7 + 2.0 + 0.5 = 3.8 \text{ ns}$$

Maximum delay (rounded up to 0.1 ns):

$$t_{pd} = (0.6 + 0.7 + 2.0 + 0.5) \times 1.65 = 6.27 = 6.3 \text{ ns}$$

Minimum delay (rounded down to 0.1 ns):

$$t_{\text{pd}} = (0.6 + 0.7 + 2.0 + 0.5) \times 0.35 = 1.33 = 1.3 \text{ ns}$$

### 5.8.3 Delay Calculations for DC Test, Function Test, and High Impedance Test

The minimum and maximum delays for these tests are determined by multiplying the typical delays for each cell individually by the delay factors. The resulting figures for both maximum and minimum delays are rounded up to the next 0.1 ns for each cell. The final figures for each unit cell of the path are totaled. The delay calculation used earlier is repeated here and is also shown calculated for the DC, function and high impedance tests. The delay factors used are those for UHB technology.

Typical delay (rounded up to 0.1 ns):

$$t_{od} = 0.6 + 0.7 + 2.0 + 0.5 = 3.8 \text{ ns}$$

Maximum delay (delay for each gate rounded up to the next 0.1 ns):

$$t_{pd} = (0.6 \times 1.65) + (0.7 \times 1.65) + (2.0 \times 1.65) + (0.5 \times 1.65)$$
  
= 0.99 + 1.155 + 3.3 + 0.825  
= 1.0 + 1.2 + 3.3 + 0.9  
= 6.4 ns

5

Minimum delay (delay for each gate rounded up to the next 0.1 ns):

$$t_{pd} = (0.6 \times 0.35) + (0.7 \times 0.35) + (2.0 \times 0.35) + (0.5 \times 0.35)$$

$$= 0.21 + 0.245 + 0.7 + 0.175$$

$$= 0.3 + 0.3 + 0.7 + 0.2$$

$$= 1.5 \text{ ns}$$

Minimum/maximum delays are also calculated this way for minimum clock pulse width, minimum data set-up time, minimum data hold time, preset timing, and clear timing. The values of the maximum and minimum delay multipliers shown above apply to pre-layout calculations only; different factors, specific to each technology, are used for post-layout analysis.

### 5.9 Clock Loading

It is acceptable, though not a recommended design practice, to load the output of a unit cell that does not carry a clock signal beyond its Output Drive Factor ( $C_{DR}$ ). To ensure maximum clock accuracy, however, unit cells that output clock signals must never be loaded beyond  $C_{DR}$ . These different loading limitations for clock and non-clock unit cells can lead to "race conditions," in which the clock signal arrives at a flip-flop before the data signal set-up time has elapsed. It is therefore most important, when loading a unit cell beyond  $C_{DR}$ , to modify the fundamental delay equation using the extra delay factors explained in Section 5.7.

## Chapter 6 - Quality and Reliability

### Contents of This Chapter

- 6.1 Introduction
- 6.2 Engineering Testing
- 6.3 In-process Inspection and Quality Control
- 6.4 Reliability Theory6.5 Reliability Testing
- 6.6 Test Methods and Criteria

### 6.1 Introduction

Fujitsu's integrated circuits work. The reason they work is Fujitsu's single-minded approach to built-in quality and reliability, and its dedication to providing components and systems that meet exacting requirements allowing no room for failure.

Fujitsu's philosophy is to build quality and reliability into every step of the manufacturing process. Each design and process is scrutinized by individuals and teams of professionals dedicated to perfection.

The quest for perfection does not end when the product leaves the Fujitsu factory. It extends to the customer's factory as well, where integrated circuits are subsystems of the customer's final product. Fujitsu emphasizes meticulous interaction between the individuals who design, manufacture, evaluate, sell, and use its products.

Quality control for all Fujitsu products is an integrated process that crosses all lines of the manufacturing cycle. The quality control process begins with inspection of all incoming raw materials and ends with shipping and reliability tests following final test of the finished product. Prior to warehousing, Fujitsu products have been subjected to the scrutiny of man, machine, and technology, and are ready to serve the customer in the designated application.

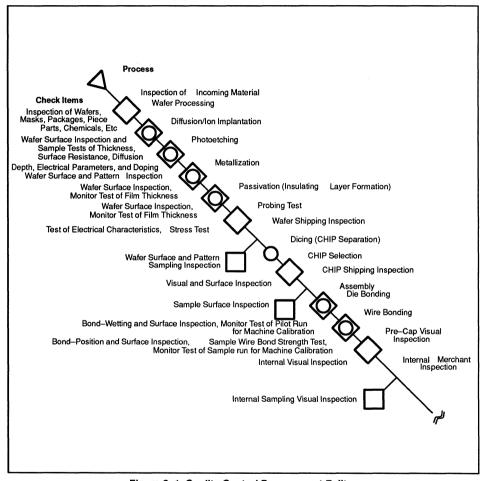


Figure 6-1. Quality Control Processes at Fujitsu

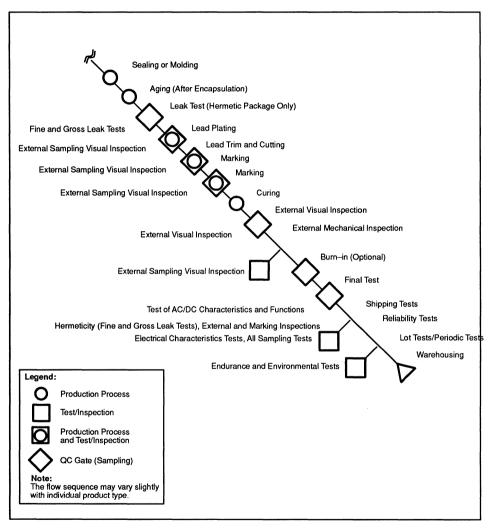


Figure 6-1. Quality Control Processes at Fujitsu (Continued)

### 6.2 Engineering Testing

Engineering testing is the heart of reliability and quality control. The reliability engineering department plans and performs most engineering testing. Whenever a device is developed, it must undergo engineering approval tests. After the device passes these tests, production engineering approval tests are performed on a representative sample of the device. All factors that could influence production of the device are examined. Only if all conditions are favorable and the device passes thorough testing, can the new device go into production.

Tables 6–1a through 6–1d show a sampling plan for engineering testing. These tests are in compliance with MIL-STD-883, Class B. When a change in production (e.g., a material change) is needed, engineering tests are performed on specific items for the change.

Since the representative samples tested must accurately reflect the reliability of the device, the following conditions must also be satisfied: the functions performed by the same basic circuit; the same processing techniques, materials, parts and packages used; and the same processing followed at the same factory.

Table 6-1a. Sampling Plan for Engineering Testing: Endurance Test

Test Items	MIL-STD-883	LTPD* (%)	Acceptance number**	Note
High-temperature storage 150°C	1008 C	7	1	
High-temperature continuous operation	1005 D	7	1	
150°C or 125°C				
High-temperature continuous operation 125°C	1055 D	5	2	
Low-temperature continuous operation -55°C	(1055 C or D)	7	1	As applicable
High-temperature high-humidity storage	1 -	7	1	Plastic package only
85°C, 85% RH				
High-temperature high-humidity continuous	(1005 C or D)	7	1	Plastic package only
operation 85°C, 85% RH	1			

Lot test percent defects

<sup>\*\*</sup> Number of failures permitted per lot

Table 6-1b. Sampling Plan for Engineering Testing: Environmental and Mechanical Test

Test items	MIL-STD-883	LTPD (%)	Acceptance number	Note
External visual inspection	2009	15	1	Same sample
Physical dimensions	2016	15	1	·
Radiophotography	2012	3 devices	0	
Internal visual inspection	2013	15	0	
Lead integrity: Tension Bending stress Lead fatigue	2004 A B B	15 15 15	0 0 0	Devices which failed in electrical characteristics test are acceptable to this test. Each test is performed on one third of the leads of each sample.
Resistance to soldering heat		7	1	Same sample
Temperature cycling	1010 C	7	1	1 '
Thermal shock	1011 A	7	1	
Vibration, variable-frequency	2007 A	<del> </del>	•	
Mechanical shock	2007 A	10	1	1
Constant acceleration	2002 B	1 "	'	
Seal: (Fine and gross leak checks)	1014 A C	7 7	1 1	Hermetic package only
Resistance to solvents	2015	40 devices	1	Devices which failed in electrical characteristics test are acceptable to this test.
Solderability (260°C)	2003	15	1	Devices which failed in electrical characteristics test are acceptable to this test.
Solderability (230°C)	_	15	1	Devices which failed in electrical characteristics test are acceptable to this test.
Internal water-vapor content	1018	3 devices	0	Hermetic package only
Electrostatic discharge sensitivity	3015 A	15	1	
Pressure-Temperature-Humidity Storage (PTHS) 121°C, 2 atm.	_	15	1	Plastic package only

The following tests are performed only when required or when requested by the customer.

Table 6–1c. Sampling Plan for Engineering Testing: Environmental and Mechanical Test (Optional)

Test items	MIL-STD-883	LTPD (%)	Acceptance number	Note
Bond strength	2011 D (or C)	15	2 wires	34 wires/4 devices
Die shear strength	2019	3 devices	0	Hermetic package only
Moisture resistance	1004	15	0	
Salt atmosphere (corrosion)	1009 A	15	0	
Vibration fatigue	2005	15	0	
Immersion	1002 B	15	0	
SEM inspection of metallization	2018	3 devices	0	
Particle impact noise detection (PIND) test	2020 B	15	1	Hermetic package only
Lid torque	2024			Frit sealed package only, as applicable
Adhesion of lead finish	2025			As applicable

Table 6-1d. Sampling Plan for Engineering Testing: Continuity Test

Test item	MIL-STD-883	LTPD (%)	Acceptance number	Note
Continuity check	_	5	2	Plastic package only

### 6.3 In-process Inspection and Quality Control

Every department involved in the manufacturing process is responsible for the quality-control inspection in its sphere of operation. In-process checks, sampling tests, and other inspections are assigned so that each department has certain allotted tasks for which it takes full responsibility. This total control system has rationalized overall operations dramatically.

### 6.3.1 In-process Checks (Including screening)

In-process checks are performed after each step critical to the next process in wafer processing and assembly. Defective or substandard products are weeded out at an early stage. Testing falls into the following three categories:

- (a) Probe testing, chip selection, and final testing. These are defined for each process.
- (b) Voluntary checks. These include inspection of the wafer surface after window opening (before the diffusion process) and inspection of the wafer surface after the metallization.
- (c) 100 percent screening. This includes the aging and visual inspection performed during wafer processing and assembly.

### 6.3.2 In-process Sampling Test

The in-process sampling test is performed as a part of process quality control. The Manufacturing and QC departments check randomly drawn samples at key points in the manufacturing process to check process and facility conditions. This helps in maintaining product quality at the customary high level. The following items are checked in these sampling inspections or monitoring:

 (a) Surface resistance after diffusion, film thickness, evaporated or sputtered electrode thickness, and device characteristics

- (b) Product quality (checked by visual inspection of the chip surface)
- (c) Bonding machine calibration, visual inspection and bond strength after wire bonding, product appearance, marking permanency

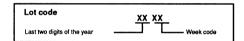
### 6.3.3 In-process Inspection

The Manufacturing and QC departments perform stringent quality checks between major processes to ensure the highest quality. The following four types of inspections are performed:

- (a) Incoming materials, parts, and chemicals Inspection
- (b) Wafer shipping inspection
- (c) Chip shipping inspection
- (d) Shipping test

### 6.3.4 Lot Configuration

A "lot" consists of the same devices produced over a stated period, having the same design and using the same processing techniques, materials, and production line. In addition to the Fujitsu logo, part number, and other markings, each device is marked with a lot code as shown below.



### 6.4 Reliability Theory

### 6.4.1 Estimating the Failure Rate

The graph of a component failure distribution is usually a downward–bowed curve, often called the bathtub curve (Figure 6–2). Life tests show that the instantaneous failure rate decreases with time and graphs as a straight line on a Weibull probability chart (Figure 6–3). Shape parameter m, which shows the instantaneous failure rate, is between 0.3 and 0.7. (In an exponential distribution, the instantaneous failure rate does not change and m=1. As m becomes smaller than 1, the instantaneous failure rate decreases with time.)

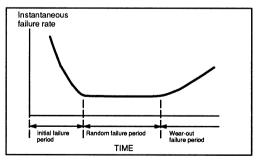


Figure 6-2. Distribution of Component Failure

Usually, the failure rates during the initial and random failure periods are the most important for semiconductors. Figure 6–3 shows an example of life test data graphed on a Weibull probability chart.

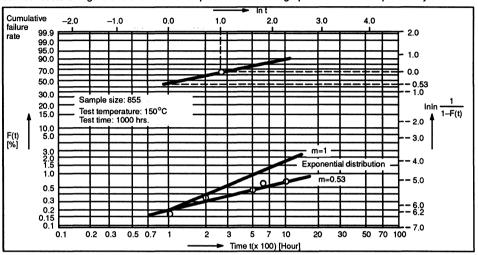


Figure 6-3. Example of Life Test Data on IC

### 6.4.2 Accelerated Life Test

Modern applications require an extremely low failure rate for semiconductors. To guarantee such strict quality requirements, Fujitsu uses an accelerated life test. There is no fixed acceleration rate for semiconductors but, since semiconductor failure is usually caused by physical and chemical changes in materials, an acceleration rate can be calculated from the Arrhenius equation below for the progress speed of physical and chemical phenomena (assuming the R is proportional to the degradation speed):

$$R = A \exp(-Ea/kT)$$

where:

R: Reaction rate

A: Proportionality constant

Ea: Activation energy

k: Boltzmann constant

T: Absolute temperature

The proportionality constant A corresponds to the component reliability. The activation energy,  $E_a$ , depends on the component's materials and their combination, but it ranges from 0.3 to 1.35 eV for semiconductors. This equation does not fit the data perfectly because it assumes that the failure rate is affected only by temperature when, in fact, there are many contributing factors. However, the equation does give a good rough fit. Using the equation on data from the accelerated life test, engineers can estimate and guarantee the field failure rate with reasonable accuracy.

The calculation method for the field failure rate is given below for Fujitsu semiconductor products. Although this method is not generally accepted yet, it has been found to be useful.

- (1) Calculate the junction temperature (Tj(op)) for actual use from the temperature rise (Tj) and the ambient temperature (Ta) under an average load (do not use the worst–case load),Tj(op) = ΔTj + Ta.
- (2) Calculate the junction temperature (Tjt) for a life test. For a high-temperature storage test, Tjt equals Ta (the storage temperature). For a continuous operation test, the temperature rise

under load plus the ambient temperature (25°C except for high-temperature operation) for an operating temperature,  $Tjt = \Delta Tj + Ta$ .

(3) Calculate the acceleration rate ( $\alpha$ ) from the difference of Tj(op) and Tjt using Figure 6–4.

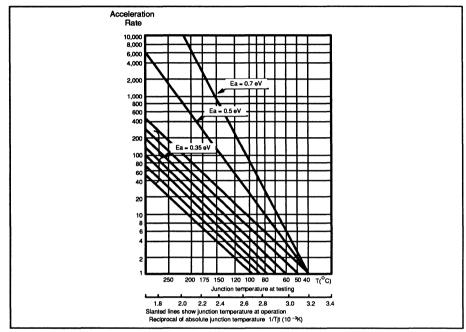


Figure 6-4. Acceleration Rate vs. Junction Temperature

(4) If planning reliability testing or calculating reliability in the field from data obtained in steps (1) to (3), determine the coefficient γ for the 60% confidence level in Table 6–2 from the number of defective units allowed or from the total number of failures found in the test.

Reliability = 
$$\frac{n}{\alpha NT}$$
 x y x 10<sup>9</sup> [FIT]

where:

N: Number of samples

T: Total test time (hrs)

n: Number of failed samples in test

Confidence level No. of failures 60% 90% 0 (0.92)(2.30)2.02 3.89 1 2 1.55 2.66 3 1.39 2.23 4 1.31 2.00 5 1.26 1.85 1.22 1.76 6 7 1 20 1.68 8 1.18 1.62 9 1.16 1.58

Table 6-2. Determination of Coefficient

The above equation applies only when n/N is equal to or less than 10% for the total test time, T. If n/N exceeds 10 percent, use the following method of calculation: divide the total test duration time, T, into subsections,  $\Delta ti$  (i = 1,2,..., m), so that for each  $\Delta ti$  the failure rate,  $(n_{i+1} - n_i)/(N - n_i)$  (where  $n_i$  is the cumulative number of failed samples for  $\Delta ti$ ), does not exceed 10 percent. Calculate  $(N - n_i) \Delta ti$  for each time section  $\Delta ti$ . Calculate the summation  $\Sigma (N - n_i) \Delta ti$  for all the time sections in T. The summation  $\Sigma (N - n_i) \Delta ti$  must then be substituted for NT in the above equation.

1.15

1.54

### 6.4.3 Failure and Causes

Circuit format differences, package types, and operating environments can change the mechanisms of IC failures, so it is difficult to foresee which factor will be the most important in a failure mechanism. Figure 6–5 shows specific electrical failures for ICs, their most common causes, and general corrective actions. Causes of IC failures are largely the same as for planar transistor failures, but the following problems are more common or specific to ICs:

- (a) Surface degradation
- (b) Flaws in an evaporated or sputtered metal film
- (c) Contact failures due to an increased number of wire bondings per package
- (d) Package failures due to an increased number of external leads

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Table 6–3 lists failures with their most common causes, and Table 6–4 shows the relationship between operating environments and failure causes. Test items can be listed only if the failure cause can be pinpointed by the test.

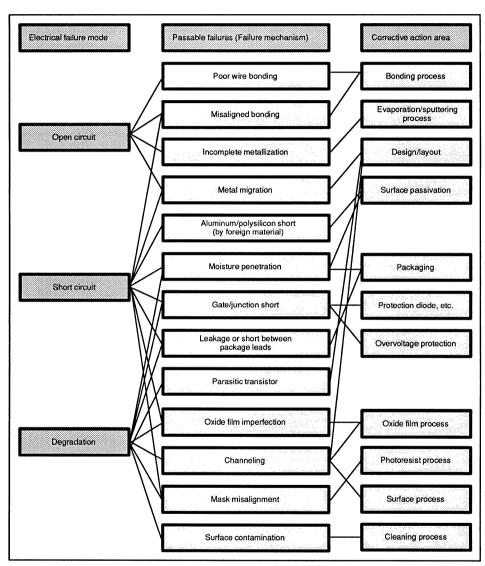


Figure 6-5. Digital IC Failures and Corrective Actions

Table 6-3. Process Defects Analysis

Defect Area	Defect mechanism	Frequency	Source				
71700			Design	Factory Process Control	Manuf. Tech.	Operator Skill	User Application
Junction	Junction failure due to current crowding	High	•				•
(Internal)	Metal migration	Low	•	•	•	•	
Junction	Oxide film imperfection (Pinhole, crack, void, etc.)	Medium		•		•	
(Surface)	Impurity contamination	High	•	•		•	
	Metal peeling	Medium		•	•	•	
	Mask misalignment	Medium				•	
Inter-	Incomplete metallization	Medium		•	•	•	
connection	Improper metallization	Medium					
	Metal over-stress	High					•
	Aluminum corrosion	Medium		•	•	•	
	Aluminum migration	Medium	•			•	
	Bonding peel	High			•	•	
Wire	Purple plague	Medium	•		•	•	
	Wire over-stress	High				•	•
	Particle/wire short	Low				•	
	Leakage	Medium			•	•	
Package	Die bond failure	Low	•		•	•	
	Lead breakage	Medium			•		•
Others	Package corrosion	Medium	•	•	•		•
- 11010	Chip crack	Medium			•	•	•
	Seal contamination	Low		•		•	

Table 6-4. Relationship between Failure Causes and Analytical Test Methods

		Test										
Failure Cause	Solder- ability (2003.2)	Temper- ature Cycling (1010.2)	Thermal shock (1011.2)	Constant Acceleration (2001.2)	Mechanical shock (2002.2)	Vibration, variable frequency (2007.1)	Lead fatigue (2004.2)	Baro- metric pressure reduced (1001)	Moisture resistance (1004.2)	Salt atmos- phere (1009.2)	Vibration fatigue (2005.1)	Vibration noise (2006.1)
Bond integrity (Chip or wire)			•	•	•	•						•
Cracked chip		•	•		•							•
Internal structural defect					•	•						
Contamination-/ contact-induced short				•		•						•
Wire or chip breakage						•						
Glass crack	•	•	•		•		•	•				
Lead fatigue contamination of junction (Surface)	•	•	•				•					•
Thermal fatigue		•										
Seal integrity		•										
Seal contamination				•	•	•						•
Leakage		•	•				•	•	•	•		
Package/material integrity			•		•				•	•		

### 6.5 Reliability Testing

Reliability testing includes three types of tests—lot tests, periodic tests, and "occasional" tests. This section explains the details of each test in turn.

### 6.5.1 Lot Tests

There are two types of lot tests, Group A and Group B. Group A and Group B tests are performed on items that are tested regularly, usually every week. Table 6–5 lists the specific lot tests.

Details of individual tests vary with the product under test, but all samples are selected at random from every weekly lot. Tests are not performed in any particular order unless specified, but are performed for each device type.

Note that the high-temperature storage and continuous-operation tests for Group B usually take 500 hours, although they may take only 168 hours in special cases. Good samples are returned to their lots after non-destructive testing. No-good samples and samples that have undergone destructive testing are destroyed.

### 6.5.2 Periodic Tests

Particulars of the periodic tests are also listed in Table 6–5. There are two types of periodic tests: Group C tests and Group D tests. Group C tests are performed on items that are tested regularly, usually every 13 weeks. Group D tests include special reliability tests and very long life tests. The Group D tests are usually done once every 26 weeks.

Details of individual tests vary with the product under test, but all samples are selected at random. Tests are not performed in any particular order unless specified, but are performed for each device type. Note that the high-temperature storage and continuous-operation tests for Group C take 1000 hours and those for Group D take 3000 hours.

Table 6-5. Sampling Plan for Reliability Testing

		Device cla	ssification	Dev	rice group 1	De	Device group 2		
Group	Subgroup	Test	tems	Sampling plan					
	A1	External visual in	nspection	100% test of sampled devices (All sampled devic			pled devices)		
Α	A2		Function test		LTPD 5%	$A_c = 0$			
^	A3	Electrical	Static characteristics		LTPD 5%	$A_c = 0$			
	A4	Characteristics	Dynamic/Switching characteristics		LTPD 5%	A <sub>c</sub> = 0			
				Sample size	Acceptance number	Sample size	Acceptance number		
	B1	Physical dimens	ions	9	1	6	1		
	B2	Environmental	Resistance to solvant +temp-cycling	9	18	9	18		
		tests	Thermal shock test	9	18	9	18		
	B3		Mechanical environmental test	9	1	9	1		
	B4-I	Solderability (230°C, 5s) <sup>1</sup>		9	1	3	1		
	B4-II	Solderability (26	0°C, 5s)1	9	1	3	1		
	B5	Lead integrity <sup>1</sup>		9	1	3	1		
В		Pressure-temperature-humidity storage <sup>2</sup>		9	13	3	13		
	B6	Pressure-temperature-humidity bias <sup>2</sup>		9	1 <sup>7</sup>	3	17		
	B7		High-temperature storage	14	14	7	14		
	B8		Continuous operation	24	14	11	14		
	B9		High-humidity storage 85° C, 85% RH <sup>2</sup>	24	14	11	14		
	C1		High-temperature storage	14	15	7	15		
С	C2	Endurance	Continuous operation	24	15	11	15		
D	СЗ	test	High-humidity storage 85° C. 85% RH <sup>2</sup>	24	1 <sup>5</sup>	11	15		
	D1		High-temperature storage <sup>6</sup>	14	_	7	<del></del>		
	D2		Continuous operation	24		11	_		
	D3	1	High-humidity storage 85° C, 85% RH <sup>2,6</sup>	24	_	11			

Test cycle: Group A and B for every weekly lot, Group C every 13 weeks, Group D every 26 weeks

<sup>\*\*</sup>These tests take 1000 hours.

<sup>&</sup>lt;sup>6</sup>These tests take 3000 hours.

<sup>&</sup>lt;sup>7</sup>This test takes 48 hours.

<sup>&</sup>lt;sup>8</sup>These tests take 100 cycles.

### 6.5.3 Occasional Tests

Occasional tests are performed on products whenever necessary. The tests are similar to periodic tests, but their details are specified by the QC/Reliability Engineering Division according to the purpose of the test.

### 6.6 Test Methods and Criteria

The reliability of Fujitsu ICs is assured by severe environmental and endurance testing. Test methods are usually based on Japan Industrial Standards (JIS), the standards of the Electronic Industrial Association of Japan (EIAJ), and MIL standards.

Reliability tests are performed for two reasons. Firstly, they check or guarantee the reliability of a type or a lot according to specified standards. Secondly, they are used to determine the failure rate or mode. The most appropriate test method is chosen for each test, and test results are processed in the most suitable manner. Fujitsu usually performs the tests listed in Tables 6–6, 6–7, and 6–8.

Table 6-6. Example of Reliability Testing

Test items	MIL-STD-883	Condition
Resistance to soldering heat		260°C, 10s
Temperature cycling	1010 C	-65°C (30 min.) to 150°C (30 min.), 100 cycles
Thermal shock	1011 A	0°C (5 min.) to 100°C (5 min.), 100 cycles
Vibration, variable-frequency	2007 A	20 to 2,000Hz, 20G
Mechanical shock	2002 B	1,500G, 0.5ms
Constant acceleration	2001 E	30,000G, 1 min, Y1 only
Fine leak <sup>1</sup>	1014 A1	Using compressed helium 99.5 psig, 4 hrs.
Gross leak <sup>1</sup>	1014 C	Using fluorocarbon 75 psig, 1 hr., 125°C
Solderability		230°C, 5s
Solderability	2003	260°C, 5s
Lead fatigue	2004 B2	0.25kgf, 90°, twice
PTHS/PTHB <sup>2</sup>	_	121°C, 2 atm
High-temperature storage	1008 C	150°C, 1,000 hrs.
Continuous operation	1005 A to D	125°C, 1,000 hrs.
High-humidity storage <sup>2</sup>	_	85°C,85%RH, 1,000 hrs.

Notes: 1 Applies to hermetic packages.

2 Applies to plastic packages.

Table 6-7. Example of Electrical Testing

Table 6 1. Example of Electrical Testing							
Circuit classification	Characteristics	Bipolar	MOS				
Gates	DC	V <sub>OH</sub> , V <sub>OL</sub> , II <sub>H</sub> , II <sub>L</sub> , I <sub>CC</sub> (I <sub>EE</sub> )	V <sub>OH</sub> , V <sub>O</sub> L, I <sub>IH</sub> , I <sub>IL</sub> , I <sub>DD</sub> (I <sub>sub</sub> )				
	AC	Function	Function				
Flip-flops	DC	V <sub>OH</sub> , V <sub>OL</sub> , I <sub>IH</sub> , I <sub>IL</sub> , I <sub>OH</sub> , I <sub>CC</sub> (I <sub>EE</sub> )	V <sub>OH</sub> , V <sub>OL</sub> , I <sub>IH</sub> , I <sub>IL</sub> , I <sub>DD</sub> (I <sub>sub</sub> )				
	AC	Function	Function				
Shift registers	DC	V <sub>OH</sub> , V <sub>OL</sub> , l <sub>IH</sub> , I <sub>IL</sub> , l <sub>OH</sub> , l <sub>CC</sub> (l <sub>EE</sub> )	V <sub>OH</sub> , V <sub>OL</sub> , II <sub>H</sub> , I <sub>IL</sub> , I <sub>DD</sub> (I <sub>sub</sub> )				
	AC	Function	Function				
Memories	DC	V <sub>OH</sub> , V <sub>OL</sub> , II <sub>H</sub> , I <sub>IL</sub> , ICC (I <sub>EE</sub> )	V <sub>OH</sub> , V <sub>OL</sub> , I <sub>IH</sub> , II <sub>L</sub> , (I <sub>OH</sub> ),(I <sub>OL</sub> )				
	AC	Function	I <sub>DD</sub> (I <sub>sub</sub> ) Function				
Random-logic devices	DC	V <sub>OH</sub> , V <sub>OL</sub> , I <sub>IH</sub> , I <sub>IL</sub> , I <sub>CC</sub> (I <sub>EE</sub> )	V <sub>OH</sub> , V <sub>OL</sub> , I <sub>IH</sub> , I <sub>IL</sub> , (I <sub>OH</sub> ),(I <sub>OL</sub> )				
	AC	Function	I <sub>DD</sub> (I <sub>sub</sub> ) Function				
Analog devices	DC AC	V <sub>IO</sub> , I <sub>IO</sub> , I <sub>I</sub> , V <sub>OM</sub> , V <sub>OH</sub> ,V <sub>OL</sub> , Av. K <sub>E2</sub> , N <sub>E</sub>	-				

Table 6-8. Example of Electrical Criteria

Parameter	Limit value (in multiples of the absolute value)	
	Upper	Lower
V <sub>OH</sub>	_	L x 0.9
V <sub>OL</sub>	U x 1.1	_
I <sub>IH</sub>	U x 2 (No leak: U x 1.1)	<del>-</del> .
I <sub>IL</sub>	U x 2 (Leak: U x 2	_
юн lcc(lee) lcc (lsuв)	U x 2 (Leak: U x 2	_

<sup>&</sup>quot;U" and "L" stand for the upper and lower limits

# Chapter 7 - Application Notes

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Developing Test Patterns That Work with the Physical Tester Selecting the Best Package for Your ASIC Design

E

## **CMOS ASIC**

# Developing Test Patterns That Work with the Physical Tester

by J. Scott Runner

Fujitsu Microelectronics, Inc.

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### Introduction

This application note briefly describes the process of developing test patterns for the simulation and test of Fujitsu CMOS ASIC designs. This information supplements testing information found in the Design Manual for the appropriate Fujitsu CMOS ASIC technology.

### Tests to be Created

Fujitsu supports the following five types of test

- a. DC test
- b. Dynamic function test
- c. High impedance test (Z-function test)
- d. Delay test (AC test)
- e. Scan test (optional for certain Fujitsu technologies)

The DC test measures DC characteristics such as  $I_{DDS}$ ,  $V_{OH}$ ,  $I_{LI}$ , and  $I_{LZ}$ , while the function test screens for manufacturing faults (metal and transistor faults, principally). The Z-function test augments the DC test and is required for circuits in which one or more enable signals from a 3-state buffer can be generated by logic deeper than one gate of complexity within the ASIC device. The delay test may be used to verify critical timing paths that are necessary for proper system operation.

Scan test methods are used to simplify the [process of testing for manufacturing defects traditionally uncovered by the function test. Automatic test generation is supported in conjunction with scan testing in the UHB/CG10 and AU/CG21 technologies as an option.

E

### Overview of Test Vector Creation

For each set of test patterns defined as a test block, the customer must specify input states and output states (in either vector or wave format), and the timing of inputs and outputs (with bidirectionals being considered both an input and an output). Many designers rely on one of the Fujitsu-supported CAE workstations when generating test vectors, easing the burden of test pattern development. In these cases, the customer creates input stimuli for the workstation simulator, which then generates a print-on-change file containing the resulting output response and the associated input stimulus previously defined by the designer. The print-on-change file is converted by Fujitsu's workstation software into FTDL (Fujitsu Test Description Language), which is the accepted test pattern description format regardless of the method by which patterns are created.

### **Developing the Tester Timing Information**

Whether or not the patterns are generated on the CAE workstation, it is necessary for the customer to generate in the FTDL file a Common Block file, containing administrative information and the test type, and a Test Block file, containing the timing information for all chip inputs and outputs by group (discussed further in the Design Manual). The definition of this overall timing is critical to the success of the test program itself. For example, input timing defines when input signals will transition, while output timing defines when outputs will be compared with their expected values or measured at a transition point.

The designer is responsible for specifying the following timing parameters for the Test Block, depending on the specific type of test:

- a. Test cycle
- b. Grouping of inputs and, if necessary, outputs and bidirectionals
- c. Delay-to-transition (DT) time for each input group of non-return to zero (NRZ) signals
- d. Propagation time (tp) and pulsewidth (Wp) times for the positive-going pulse (PP) and negative-going pulse (NP) for each input group of return to zero (RTZ) signals
- e.\* Delay-to-strobe time (STB) point for each output group
- f.\* DT and STB times for bidirectionals
- g.\*\* T time in the SPATH statement for AC tests

This timing is established for the entire test block and is invariant until another test block is invoked. Therefore, test pattern timing is periodic, that is, a group of inputs may only transition at the time specified in the Test Block, which is relative to the beginning of the test cycle. This delay to transition time for inputs is programmed for each input group with the  $t_p$  parameter in the FTDL INTIM or BUSTIM statement.

Similarly, common output groups are strobed, or sampled, periodically at a time determined by the test cycle and the delay-to-strobe time specified in the OUTTIM or BUSTIM statement, or the  $T_p$  parameter in the FTDL SPATH statement in the case of an AC test.

### **Determining Input and Output Timing Parameters**

During the function test, outputs should stabilize before being strobed. Therefore, the minimum permissible test cycle programmed by the TIMING statement in the Test Block should be set with consideration of the maximum propagation delay from any input to any output, and the respective DT and STB times for those groups should be set far enough apart in time to assure that the outputs are stable under maximum

<sup>\*</sup>Specified in DC, function, and Z-function tests

<sup>\*\*</sup>Applicable only to AC tests.

conditions. Similarly, if the output is strobed before the transition, it must be stable under minimum delay conditions.

Test patterns are required to be invariant over minimum and maximum delay conditions. This is verified in simulation by scaling the typical delays by multipliers representing process, temperature, and power supply variations. Similarly, the strobed or expected output states must be identical under typical, maximum, and minimum conditions. If a propagation delay from input to output is greater than the test cycle defined, output states may not fulfill this requirement (see Figure 1). Furthermore, designers should be careful that glitches or short pulses do not occur anywhere within this minimum/maximum window (see Figure 2).

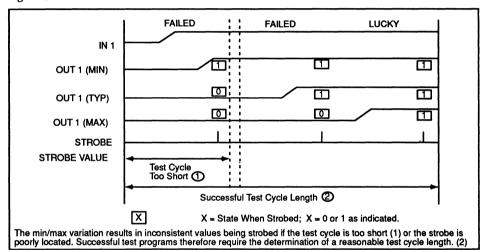


Figure 1. Determining a Successful Test Cycle Length

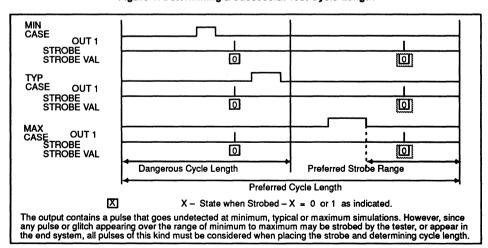


Figure 2. Determining Preferred Cycle Length

### Generating Functional Input Stimulus Given Test Pattern Timing

One issue that must be considered when determining test pattern timing is the relationship between input signals, such as clock/data pairs, which must satisfy set-up and hold times. Other considerations guiding the timing definition are dependent on the particular circuit being tested, and on restrictions imposed by the tester. These restrictions are published in the Summary of Test Data Restriction section of Fujitsu's Design Manuals.

### Tester Skew and its Compensation of Test Timing

The designer must pay particular attention to the issue of tester skew when determining input and output timing for Test Blocks; otherwise, the timing will not correctly represent the behavior of the device under test. Tester skew, specified for each technology in the Summary of Test Data Restrictions, is a result of the variation in the time at which a given signal generator triggers a transition or a comparator measures an output state. Several timings are affected by this skew.

### Input-to-Input Skew

For the purpose of estimating the skew between two signal generators, (one driving data and the other driving its clock, for example), the driver skew, linearity of clocks, clock-to-clock skew, and jitter are collectively called driver accuracy, denoted  $t_{DSKEW}$ .

In the case of data/clock pairs, the clocked data may fail either a set-up or hold time, depending on the direction of the skew. Therefore, when determining DT and  $t_p$  for data/clock pairs, the designer should adjust times to satisfy the following relationships (see Figure 3):

Set-up Time Criteria for Testing:  $(t_p(CLOCK) - DT(DATA)) >= t_S(MIN) + 2 * t_{DSKEW}$ 

Hold Time Criteria for Testing:  $(DT(DATA) - t_p(CLOCK)) >= t_H(MIN) + 2 * t_{DSKEW}$ 

Where  $t_S(MIN)$  and  $t_H(MIN)$  are the worst case set-up and hold times, respectively, sensitized from the internal circuit to the inputs,  $t_{DSKEW}$  is not directly specified in the Summary of Test Data Restriction; however,  $T_{ACC}$ , the overall system timing accuracy, is specified and can be substituted for  $t_{DSKEW}$ .

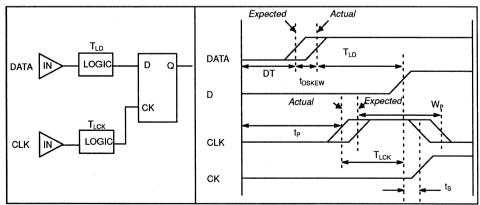


Figure 3. Input-to-Input Skew

### Input-to-Output Skew

In addition to the skew incurred by the signal driver, skew is also introduced by the output comparator of the tester. This skew is dependent on the linearity of the strobe, pin-to-pin skew, skew between dual com-

### Input-to-Output Skew

In addition to the skew incurred by the signal driver, skew is also introduced by the output comparator of the tester. This skew is dependent on the linearity of the strobe, pin-to-pin skew, skew between dual comparators, and the driver-to-comparator timing error. All factors are considered in the overall system timing accuracy, *t<sub>ACC</sub>*, which in turn affects output timing as shown in Figure 4.

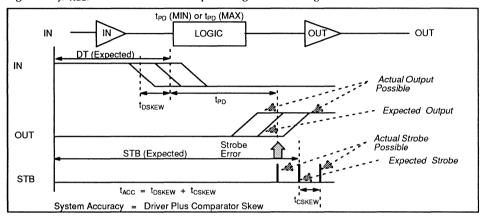


Figure 4. Input-to-Output Skew

### Skew Effect on Input/Output Pairs - Minimum Delay Case

The *STB* (or *T* parameter in the SPATH statement) should expect an output transition at a time relative to the stimulated input transition dictated by

$$(STB - DT) >= t_{PD(MIN}) - t_{ACC}$$

where STB is the strobe point of the output under consideration, DT is the DT time of the stimulating input of interest, and  $t_{PD(MIN)}$  is the minimum propagation delay from this input to the strobed (or measured) output. In the case of the AC test, the quantity (STB - DT) should be replaced by the minimum T parameter in the SPATH statement. Note that if the path delay spans a test cycle boundary, STB should be set to STB plus the test cycle period.

### Skew Effect on Input/Output Pairs - Maximum Delay Case

The complementary case occurs for maximum delay measurements, as described by

$$(STB - DT) \le t_{pd(MAX)}) + t_{ACC}$$

Note that these guidelines regarding the specification of test data timing as affected by tester skew apply to DC and Z-function tests as well. In these cases, the same rules apply as for the function test.

Again, for the specific values of  $t_{ACC}$ , and  $t_{DSKEW}$ , please refer to the Summary of Test Data Restrictions in the Fujitsu Design Manual for the appropriate technology. A designer interested in a methodical approach to the generation and verification of a good set of test vectors must consider the tester hardware on which it is running. Fujitsu has simplified designer responsibility by providing this information as part of the Test Block Information.

However, a lack of implementation and careful analysis of the timing characteristics of the circuit may result in a poor or unfeasible test, resulting in schedule delays or reduced device yield. Therefore, plan a test approach early, design for testability, and consider the effect and operation of the physical tester.

# **ASIC Packaging Information**

# Selecting the Best Package for Your ASIC Design

by J. Scott Runner

Fujitsu Microelectronics, Inc.

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### 1.0 Introduction

The widely varying degrees of complexity (gate count) of Fujitsu's CMOS and BiCMOS devices and the flexibility of their I/O configurations combine to produce devices that take advantage of the broad selection of packages available from Fujitsu. However, the requirements for package selection go far beyond pin count as the sole determinant of the best package. Selection issues include surface mount versus through-hole, plastic versus ceramic, and exotic versus conventional packaging. In fact, Fujitsu offers over 100 packages and 1000 package-die combinations from which to choose. Compounding the selection problem is the effect of increasingly faster outputs coupled with higher drive and wider bus structure, resulting in greater numbers of simultaneously switching outputs (and thereby greater amounts of noise).

The result is that designers are finding ASIC packaging implementation to be an increasingly complex task. This application note provides information about ASIC packaging that is meant to simplify the designer's task. It provides designers with a review of the various Fujitsu packages and their electrical, thermal, and mechanical characteristics, as well as some problem-solving strategies for their use. Sections 2.0 and 3.0 address system requirements and package availability; Sections 4.0 and 5.0 discuss noise and thermal issues.

F

### 2.0 How System Requirements Affect Package Choice

Section 2.0 presents considerations involved in the selection of packages from a system designer's perspective. Table 1 lists issues a designer must consider when determining the optimal packaging for an ASIC design.

Table 1. Considerations for Package Selection

Manufacturing and Cost	Speed Requirements
Board Integration	Package and Interconnect Delays
Double-sided Component Mounting	The Effect of Package on Noise
Number of Packages	Thermal Considerations
Package Outline Area	
Power Density Limitations	
Producibility	Quality
Board Layout	Package Quality and Reliability
Package Construction	Number of Devices
Packaging Complexity	Noise
Manufacturing Flow	Thermal Considerations

### 2.1 Manufacturing and Cost

The manufacturing-related factors discussed below, although not directly related to the design of the device or the number of power and ground pins it requires, are nonetheless important in the choice of an ASIC package.

### 2.1.1 Board Area

One of the most important issues is the board area consumed by a circuit. Some of the factors affecting overall board density are:

Integration (gates per square inch of board)

Double-sided mounting capability (integration)

Number of packages

Package outline area

Additional board space required (for spacing, resistors, capacitors, probe areas, etc.)

Power density area (discussed in Section 5.0)

The critical issue in board area reduction, however, is overall integration. For example, surface mount devices (SMDs) can be densely mounted on both sides of the board, making them ideal for systems demanding high package integration. But a large design integrated into a few very large Sea-of-Gates arrays, even if packaged in large, through-hole packages, may well consume less board space than the same design using surface mount plastic J-leaded chip carriers (PLCCs). The PLCC version would require more space because the PLCCs, although small in outline, cannot house as large a die and therefore require the design to be partitioned into a greater number of devices.

Figure 1 illustrates the board area taken up by the outline of each kind of package Fujitsu offers, excluding any area around the package necessary for spacing, decoupling capacitors, series damping resistors, or solder pads.

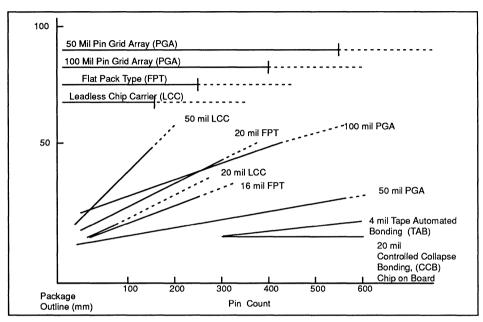


Figure 1. Package Size versus Pin Count

### 2.1.2 Board Layout

Restrictions in board layout or construction must be identified and resolved early in the design process. For example, a design containing large buses (16 bits or 32 bits or more) must be split up to avoid too high a concentration of simultaneously switching outputs per ground pin. Splitting up the buses, however, may result in variations in signal trace length and require extra care in routing. Similarly, flatpacks, a form of SMDs, are a convenient way to support high pin counts in relatively inexpensive plastic packages. However, with pin pitches as narrow as 15 mils, they demand extremely accurate positioning of solder pads. Dense PGAs, on the other hand, provide a spacious 100-mil pin separation, but because of the number of rows of pins, normally require a large number of board layers.

### 2.2 Producibility

Though some unusual packages may appear to promise ultra-high speed or dense integration or minimized component/board cost, the designer must always keep manufacturability in mind. The cost of a system is only partially dependent on materials and labor costs per unit; it is also highly dependent on the manufacturing yield of the end product. Therefore, design and production engineers must jointly consider the choice of package in order to guarantee that the chosen package conforms to existing (or purchasable) manufacturing equipment and that the manufacturing process can meet yield goals.

### 2.3 Speed Requirements

The speed requirements of a system strongly affect package choice. If the interconnect lengths in the system (both inter- and intra-board) can be reduced, system speed may be increased. Reducing interconnect lengths may involve reducing the required number of packages, choosing packages with smaller outlines, changing to double-sided, modular, or piggy-backed mounting, using small form factors, reorganizing boards, and even changing the number of metal routing layers of the board. See Figure 2.

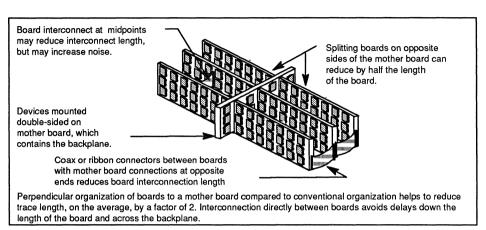


Figure 2. Minimizing Interconnect Length

### 2.3.1 The Effect of Noise on Speed

There are various sources of noise that can affect an integrated circuit (IC), each with its own effect; all forms of noise influence signal speed, quality, and consequently, system reliability. Certain types of noise arise between a chip I/O and ground or power, while other forms of noise are coupled to the power rails and influence system power and ground lines, propagating noise throughout the entire system. Noise appears to an input buffer (receiver) relative to the receiver's ground. Any noise on this referenced signal is superimposed onto the incoming signal itself, as shown in Figure 3. The  $V_{\rm IH}$  or input threshold level of the receiver indicates when the input will switch, if the signal is stable at that level. Therefore, although the input voltage ordinarily would switch 4 ns after the driver switches, when the signal first crosses the threshold, the designer must assume it will not switch until it is stable; in this case at 8 ns, producing a loss of 4 ns due to noise.

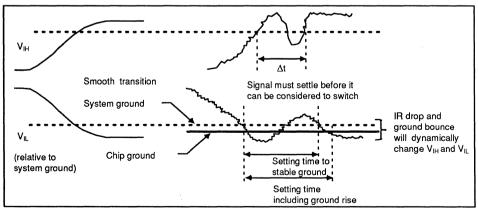


Figure 3. Impact of Noise on Speed

### 2.3.2 Controlling Noise through Package Selection

Each form of noise is dependent not only on current or its first derivative with respect to time, but also on the real and imaginary components of impedance: resistance (R), inductance (L), and capacitance (C). One solution to noise can be to minimize the package L and R and to locate high drive pins where they will minimize L and R.

### 2.3.3 The Effect of Thermal Characteristics on Speed

The speed performance of a CMOS or BiCMOS circuit degrades with temperature rise. Therefore, in very high speed systems, it is sometimes necessary to reduce the junction temperature (Tj) or die temperature as a way to improve speed. Certain packages offer better cooling properties than others, making them more suitable for high speed systems. Thermal issues are discussed in Section 5.0.

### 2.4 Quality

Reliability refers to the defects or failures that appear during the lifetime of a device. Quality, on the other hand, refers to the frequency of occurrence of defects or faults in a device as a result of the manufacturing process. Quality defects are revealed by testing immediately after manufacturing, while reliability defects are revealed by special long-term or intensive test sequences or by time.

### 2.4.1 How Package Type Affects Quality Testing

Conventional (through-hole) packages lend themselves to simplified testing because it is easy to access the leads in order to force a state (1 or 0) at a node and/or to observe the state of the node. These tests are performed with board-level in-circuit or functional testers. Such tests facilitate the manufacture of high-quality systems by ensuring proper connectivity and function.

Surface mount devices, however, generally provide poor probe access, and are known to occasionally possess faulty joints that make temporary connections during probe. Through-hole packages also have occasional bad solder joints, although their node access is fairly good.

### 2.4.2 How Device Integration Affects Reliability

Total system reliability is related to the reliability of the individual devices and to their configurations. Systems may be configured as a series in which all devices are interdependent, in which case any one failure will cause overall system failure, or they may be configured in parallel, in which case all devices must fail for the system to fail. Parallel configuration is used in redundant or fault-tolerant systems.

The reliability of a system also depends on the reliability of the devices that comprise the system. The long-term reliability of a single device is defined as an inverse natural log function in a variable lambda, which is the failure rate of the device in the region of lifetime operation characterized by a constant failure rate. In the first hours of a device's life (the infant mortality period), the failure rate declines. The majority of a device's life is characterized by random failures (expressed as lambda), and the end of a device's life exhibits an increasing failure rate. Today's ICs, however, are designed so that we arout does not even begin to occur for at least several hundred years, and can be considered never to occur.

To understand how the partitioning of a system into circuits can affect the reliability of a system, consider a system in which N components are configured in series. Although the density of ASIC devices has increased by two orders of magnitude in the last decade, the reliability of the devices has remained roughly constant. Therefore, it can be assumed that the failure rate of each of the components is constant. The reliability of systems and subsystems in which components are series-dependent is the product of the individual reliability terms for each component. The reliability function of the system just described is therefore:

R(t)sys = R(t)1 \* R(t)2 \* ...R(t)N

where

 $R(t)N = e - N\lambda t$ , t is the independent variable time, and  $\lambda$  is lambda, the failure rate.

Since all components have the same failure rate, the reliability function of the system is:

$$R(t)sus = e - N\lambda t$$

Because the number of packages affects the reliability more than the integration factor does, a designer's goal in constructing a reliable system should be to maximize integration and thereby reduce part count.

The disadvantage is that increased integration may in turn increase the package pin count, requiring a more complex package, which usually costs more than a simpler, smaller package. Additionally, the larger die sizes cost slightly more per gate than the smaller ones, although the total non-recurring engineering charges (NRE) would typically be lower.

# 2.4.3 How Noise Affects Reliability

Even when Schmitt trigger input buffers are used to receive clock signals, noise may go beyond the hysteresis value of the input buffer and cause a counter to be incorrectly clocked or other circuit malfunction. Noise is in this sense a threat to reliability as well as to speed and must be considered in the package choice as well.

# 2.4.4 How Thermal Issues Affect Reliability

While the junction temperature of a device affects its speed, it also affects reliability expressed as mean time between failures (MTBF) or the mean time a device will operate in a given environment before failure occurs. Figure 6–4 in the previous chapter, Quality and Reliability, illustrates this concept by plotting life test failures as a function of junction temperature. System reliability goals, then, restrict the desired maximum junction temperature in a manner that affects the choice of package according to its thermal characteristics, the chosen type of system thermal management (cooling), and the maximum allowable device power dissipation.

# 2.4.5 How Package Material Affects Reliability

The different materials used in package construction each have distinct thermal and mechanical properties. The most common materials and their characteristics are listed in Table 2 below.

Package Type	Body Material	Thermal Coefficient of Expansion (ppm/5C)	Thermal Conductivity (W/m * 5C)	Dielectric Constant (K)	
Ceramic	Al <sub>2</sub> O <sub>3</sub> (Alumina)	7.0	20	10	
Plastic PGAs	Epoxy Fiberglass	14 – 18	0.16	4.5 – 5.0	
Other plastic packages (DIP, PLCC, Flatpack)	Polyimide Epoxy	15 – 18	0.38	4.5 – 5.0	

**Table 2. Package Material Characteristics** 

To better understand the different characteristics of plastic and ceramic packages, it is helpful to know something about the way they are constructed. Packages provide electrical connection from the IC to the system and isolate the device from destructive elements of the environment. The choice of materials and construction of a package affect its final dimensions, thermal characteristics, and electrical characteristics, as well as device reliability. Fujitsu carefully determines the most appropriate manufacturing methods for a given package and then performs extensive qualification tests to determine its success.

The largest part of the package is the body, which houses the die. The die may be affixed to a lead frame, which physically supports the die and provides the leads that electrically connect the die to the system by means of bonding wires or tab leads. Alternatively, the die may be supported by a cavity on the body of the package or attached to the bottom of the body by a chip carrier.

The die is attached to the surface of the lead frame or to the metallized surface of the cavity or carrier with gold or silver paste, or eutectic. After the die is attached to the lead frame, cavity, or carrier and the bonding pads are bonded to the leads, the assembly is encapsulated. In plastic packages, an epoxy resin is molded around the assembly. In ceramic packages, a cap is sealed onto the lower part of the body or carrier using a frit glass or metal seal (the metal seal has a higher melting temperature than the glass). A solder seal can be used if the cap is metal.

To ensure that the device is completely isolated from its environment, the surface of the die is then coated with glass (SiO<sub>2</sub>) and then polyimide or other coating that prevents gas and moisture from coming in contact with the surface of the die. Figure 4 shows a frontal cross section of the structure of a PLCC package; Figure 5 provides a top view.

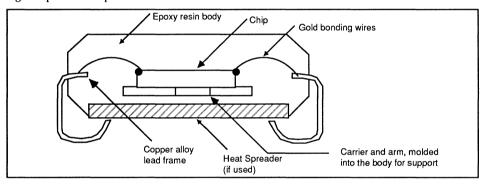


Figure 4. PLCC Package Construction (Front View)

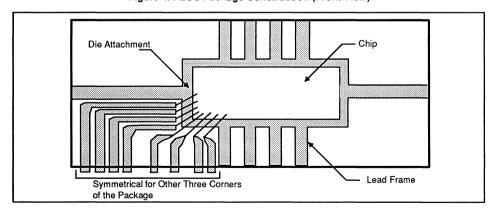


Figure 5. PLCC Lead Frame Construction (Top View)

Each of the various packaging methods has its advantages and disadvantages; for instance each body type and each type of seal has a different maximum case temperature. While plastic packages can tolerate tem-

peratures up to 125°C and high humidity levels with outstanding reliability, ceramic packages are the most reliable for harsh extremes of cold.

Each package type also responds differently to the thermal environment of the board to which the device is attached. Heat can cause thermal stress on the device when different materials expand at different rates, a particularly important factor when surface mount packages are involved.

Different packages also exhibit different electrical characteristics. As the speed and gate densities of CMOS devices rise, the avoidance of electrical parasitics in the form of package delays and noise becomes an increasingly important factor in choosing a package type.

Fujitsu's plastic PGA provides a good example of the tradeoffs involved in package construction. In 1986, Fujitsu introduced the plastic version of its ceramic PGA. The plastic configuration proved to have several advantages over the ceramic version. The body is formed from glass epoxy (VG-10) with an aluminum cap and an epoxy resin sealer. This combination of materials has the same rate of expansion as the PC boards onto which it is mounted; it is also less expensive than ceramic.

Ceramic PGAs have a hermetic seal of solder between the metal lid and the cavity, but plastic PGAs are sealed by filling the cavity with epoxy resin to form an inner seal, then placing a resin sheet over the inner seal to form an outer seal, and then securing an aluminum cap over the outer seal. The aluminum cap provides the necessary rigidity to support the fragile glass epoxy, as well as improving the thermal conductivity of the package.

Connections from the bonding wires to the pins are provided by copper traces designed to minimize mutual and self inductance. Because the plastic PGA is a large package, however, and generally houses a large die, the thermal coefficient of expansion (TCE) difference between the die and the cavity can exert stress on the bonding wires and the die attach. Table 3 lists the package types discussed in this section and the materials used to construct each type.

Package Lead frame/ Body Seal Material Type Metallization Lead/Pad Lead Finish Cap Material Material Plastic DIP le-Ni or Cu Solder Dipped Resin Resin Same Alloy Lead frame Ceramic DIP Kovar or Fe-Au/Sn Plated Metal or Alu-Laminated Tungsten Solder. Metallization Alumina Glass Frit minum CERDIP Fe-Ni Allov Fe-Ni Sn Plated Alumina Alumina Glass Frit Lead frame Plastic Fe-Ni Alloy Same Sn Plated Resin Resin Flatpack Lead frame Ceramic Fe-Ni or Kovar Same Au Plated Metal or Alu-Laminated Solder or Flatoack I ead frame minum Alumina Glass Frit Fe-Ni Allov Sn Plated and Cerpack Same Alumina Alumina Glass Frit Lead frame Solder Dipped Plastic PGA Cu Conductor on Aluminum **Epoxy Glass** Resin Ni Plated and Kovar **Epoxy glass** Solder Dipped Ceramic PGA Tungsten Metal or Laminated Glass Frit Au Plated and Kovar Metallization Solder Dipped Alumina Alumina Plastic LCC Cu Allov Resin Resin Solder Plated Same Lead frame Ceramic LCC Tungsten Metal or Alu-Laminated Solder Tungsten Au Plated Metallization mina Alumina Glass Frit Metal Pad

Table 3. Fujitsu Package Types

Note: All above packages are hermetic. Alumina is a ceramic. Solder is PbSn. Fe-Ni is ferrous (iron) nickel. Kovar is an alloy of cobalt, iron, and nickel. Bonding wires are gold in the case of molded packages (epoxy resin PLCCs, DIPs, Flatpacks) and gold or aluminum for the other cases. Cerpack is the ceramic flatpack equivalent of CERDIP.

# 2.4.6 Package Qualification to Ensure Reliability

Fujitsu performs extensive six-month minimum qualification tests for every package-die combination. After such qualification is performed, the package die-combination is added to a package matrix in the Design Manual for the appropriate technology. The designer can be assured that Fujitsu has considered the issues presented here, as well as others, when releasing an approved package-die combination.

# 3.0 Package Types

Very large scale integration (VLSI) ASIC devices are supported by a wide variety of packages, of both surface mount and through-hole types. Through-hole devices, including DIPs and PGAs, are a proven technology and are supported by widely available production equipment. The pins of these devices are inserted though holes in the PC board to form electrical contact with traces (usually copper) which are embedded in the board or applied to the surface and are routed to drilled pin holes. Solder applied by reflow or wave technique then completes the connection.

# 3.1 Through-hole Packages

# 3.1.1 Dual In-line Packages (DIPs)

DIPs have two rows of pins spaced 300 mils to 900 mils apart, with a pin spacing of 70 to 100 mils. Since the length of the package increases as each pair of pins is added, the size of a DIP tends to be unmanageable over 64 pins. The lead width and length of a DIP varies widely, causing variation in the input and output response of the device and thus, skew. Also, due to their high pin inductance, DIPs tend to be noisy, the degree of noise being a function of the location of outputs and sensitive inputs.

The DIP is relatively simple for manufacturing to support, thanks to a large installed base of well-proven equipment and is one of the least expensive packages available. Furthermore, DIPs, being well established, come in many JEDEC-approved options (see JEDEC Standard 95), and are available in both ceramic and plastic cases.

#### 3.1.2 Pin Grid Arrays (PGAs)

Although PGAs are usually through-hole (Fujitsu also offers SMD versions), they differ from DIPs in that pins are arranged in rows on all four sides. While the pin spacing is usually the same as for DIPs (70 to 100 mils), nesting the pins in rows permits a larger number of pins to be contained within a smaller area allowing PGAs to support high pin counts of more than 300 pins. See Table 4 for a list of Fujitsu PGAs.

Table 4. PGAs Available from Fuiitsu

Package	Туре	Construction	Number of Pins
PGA – 64C, 64P	Through-hole	Ceramic/Plastic	64
PGA - 88C, 88P	Through-hole	Ceramic/Plastic	88
PGA - 135C, 135P	Through-hole	Ceramic/Plastic	135
PGA – 179C, 179P	Through-hole	Ceramic/Plastic	179
PGA – 208C	Through-hole	Ceramic	208
PGA - 256C	Through-hole	Ceramic	256
PGA – 256C	Surface	Ceramic	256
PGA – 299C	Through-hole	Ceramic	299
PGA - 321C	Staggered	Ceramic	321
PGA - 361C	Staggered	Ceramic	361
PGA - 401C	Staggered	Ceramic	401

Through-hole = 100 mil through-hole Surface = 50 mil surface mount PGA Staggered = 71 mil staggered PGA Application Notes

Although PGAs are generally easy to support from a manufacturing standpoint, they may also raise problems. The PC board designer may find it difficult to route signals to and from the inner rows of the PGA, since it has only 100 mils spacing between pins. Additionally, the large cluster of pins confined to a small area tends to create trace congestion and may require boards of up to six layers to be used to support the PGAs. Manufacturing engineers find the solder joints for the pins of inner rows are difficult to inspect, forcing them to rely on the results of "bed-of-nails" in-circuit testers, or sophisticated inspection techniques such as x-ray or infrared.

Although more expensive than DIPs, PGAs have come down in cost with the introduction of plastic PGAs (previous PGAs were usually ceramic). These plastic PGAs are generally constructed of G-10 glass-type epoxy with the traces routed through the epoxy the way they are routed on a typical PC board. (The electrical characteristics are, of course, tightly controlled). Although the reliability of plastic PGAs was initially in question, Fujitsu built them using special construction techniques employing metal lids and heat spreaders to provide rigidity and heat dissipation. Their excellent reliability history up to this point seems to indicate that plastic PGAs will continue to be popular. The widely-used epoxy thick-film substrate, once a quality and reliability concern, has the same TCE as the most common PC boards, and reduces the stress of expansion and contraction that is typically a concern with larger packages. (The distance of expansion per unit change in temperature increases with the size of the package.)

# 3.1.3 Advances in Through-hole Packaging at Fujitsu

The demand for high pin-count plastic packages cannot be satisfied by merely increasing the number of pins a package supports. As size increases, so do the problems inherent in these lower-cost packages. These problems include greater lead inductance and thermal expansion mismatch between die and package. Ceramic flatpacks can support more pins than plastic packages, but they require special manufacturing capabilities, and are difficult to work with since they may have pin pitches down to 10 mils. Surface mount PGAs (discussed in Section 3.2) can support a large number of pins, but require difficult manufacturing processes.

Fujitsu's answer to these problems, for the customer who wants high levels of integration without the need for exotic manufacturing methods, is the staggered PGA, shown in Figure 6.

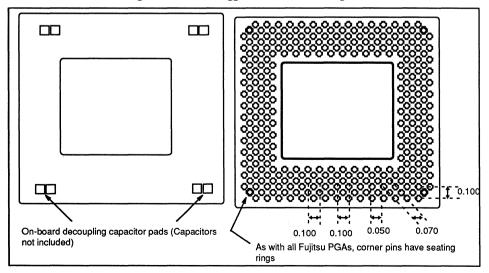


Figure 6. 321-Pin Ceramic Pin Grid Array

Figure 7 illustrates the footprint of the staggered PGA and the method for routing traces through the leads. Note that the routing is oblique, with the traces offset 45 degrees compared to traditional routing. At this angle, the lead spacing is 71 mils, providing the trace density available with standard through-hole devices, while reducing the package outline by approximately 40 percent.

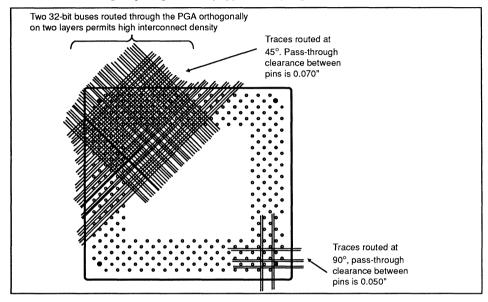


Figure 7. Staggered Pin Grid Array Routing

The lead configuration of a package affects the pin assignment of the ASIC device. For example, Figure 7 shows a situation in which a 32-bit address bus and a 32-bit data bus are routed through the device, with one offset 90 degrees from the other. If you assign consecutive bit significance to the bus, you will notice that the resulting pinout is quite different from an equivalent circuit packaged in a traditional orthogonal PGA. High drive buses can still be distributed around the ground pins, but the associated pads are not concentrated in one specific area of the die, reducing the concentration of SSOs, thereby reducing signal noise.

#### 3.2 Surface Mount Devices (SMDs)

The demands of military applications, space-constrained systems, and boards containing large numbers of memory devices were initially responsible for the development of surface mount technology (SMT). However, the accelerated push for physically reduced systems, the appearance of higher pin count ASICs, and the cost of pin grid arrays have encouraged many more designers to consider surface mount options. Easing the strain of the migration to SMT is the broader availability of pick and place, vapor phase soldering, and other necessary SMT equipment, as well as the availability of SMDs for an increasing percentage of devices on the boards. SMT for VLSI is gaining momentum due to the smaller board area consumption, smaller profile, and proven reliability.

#### 3.2.1 Flatpacks

Plastic flatpacks have been popular for years with manufacturers of peripherals in which the board area is constrained and height is restricted. And recently, the low cost of flatpacks (in plastic) has made them an attractive alternate to PGAs and even to DIPs in cases of higher pin count. As the following figures show,

flatpacks come in several lead type and location configurations. Figure 8a illustrates a small outline integrated circuit (SOIC), with gullwing leads on two sides, Figure 8b illustrates a quad flatpack (QFPT) with gullwing leads on four sides. Flatpacks with axial leads require special assembly, and are generally used only for ECL circuits in which leads may have to be trimmed and formed to tune impedance.

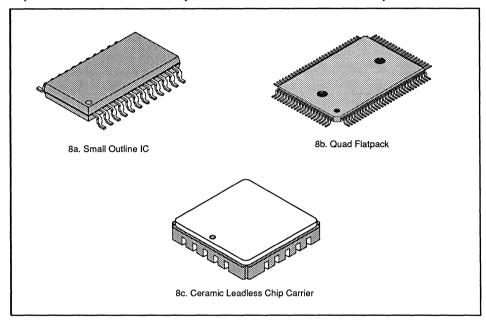


Figure 8. Flatpack Configurations

Because flatpacks feature pin pitches (pin spacing from center to center) down to 10 mils, they can support high pin counts within a small board area. However, the narrow pin spacing means that accuracy in device placement, pad size and placement, and solder paste application tolerance are all more critical. PC board designers also need to determine whether the true package dimensions are in metric or English dimensions, and, when converting between the systems of measure, ensure that enough precision is maintained so that pins on the end of large packages won't roll off due to inaccuracies in pad location.

Probing devices with fine pin pitches can be difficult because the pins do not pierce the bottom of the board, and if probes are attached to the leads, they can easily slip off and short adjacent leads.

# 3.2.2 Leadless Chip Carriers (LCCs)

Ceramic leadless chip carriers (CLCCs), such as the example shown in Figure 8c, have a long history in surface mount packaging. Ceramic packages perform well in high temperature environments, explaining their popularity in military applications. The term "chip carrier" comes from the process of mounting the die directly to a thick-film chip carrier, which also has pads for external connection on the opposite side of the substrate. This configuration differs from that of the PGA, in which the die is housed in the cavity of the package, or the flatpack, in which the die is held by the lead frame and molded with the package. CLCCs are available in pad counts ranging from 28 to 84 and beyond.

Pads, not leads, are located on the bottom of the carrier and are generally spaced at a 40-mil pitch (standard). Solder paste is applied to the pads on the board to which the device will be mounted, usually by screen printing, and the board is then vapor phase or infrared reflow soldered. Because the pads are lo-

cated beneath the package, they are typically very difficult to probe and are subject to manufacturing defects such as solder voiding (gas bubbles in solder formed during reflow).

The most challenging problem inherent to LCC devices relates to TCE mismatch between the chip carrier and the board to which it is mounted. As the temperature of boards and packages rises, the materials expand at different rates. This difference translates to mechanical shear force at the solder joint. This force temporarily deforms the leads of PLCCs and flatpacks, but CLCCs have no leads. Consequently, the force is directed at the solder joint, tending to promote thermal fractures, (shown in Figure 9).

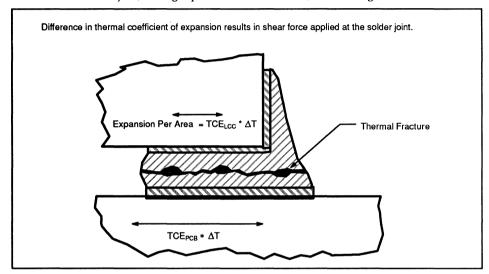


Figure 9. Defect Caused by Difference in Thermal Coefficient of Expansion

Even though CLCC SMDs cost more than equivalent plastic packages, their resistance to high temperatures, availability in hermetically sealed (moisture resistant) packages, and low profile of the CLCC SMDs make them very useful for applications in extreme environments. The TCE mismatch problem affecting LCCs is less severe when they are mounted to ceramic hybrids or PC boards, making their disadvantages acceptable in many circumstances.

# 3.2.3 Plastic J-leaded Chip Carriers (PLCCs)

If cost and TCE mismatch are a significant deterrent to the use of LCCs, leaded chip carriers may be more attractive. Though the chip is still mounted on a carrier (see Figure 10), the electrical connections of PLCCs are through pins that deform to absorb the TCE-induced thermal stress. Furthermore, while solvents used in the post-soldering cleaning process may be retained beneath the low profile of the CLCC and flatpack, the board offset of the PLCC permits it to remain free of these contaminants. In addition, the LCC in a plastic package costs less than the equivalent CLCC.

When more pins are necessary (in the 44-, 68-, 84-pin packages necessary for ASICs), the LCC is called a PLCC. It is also available in a ceramic body version; both are available in pin counts of 28 to 84 and beyond.

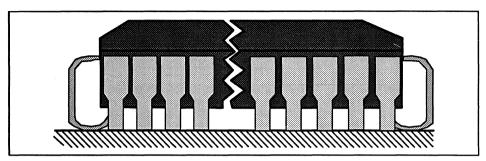


Figure 10. PLCC Package

This package is termed a small outline J-lead (SOJ) when its bent leads are located on only two sides (Figure 11). The leads are bent into the form of a J in order to permit it to be placed on top of the solder pad.

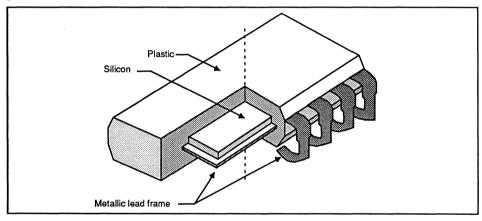


Figure 11. Cross-Section of a Plastic Small-Outline J-lead Package

On the list of drawbacks of the PLCC is its limited ability to withstand high case temperatures, and its unavailability as a hermetic package. It is nevertheless very well suited for industrial and commercial environments. With a 50-mil pin pitch and only slightly greater height and width, the profile of the PLCC is nearly equivalent to the corresponding CLCC.

# 3.2.4 Advances in Surface Mounted Packages

While smaller process geometries themselves have few disadvantages, the associated increase in integration, speed, power, and particularly pin count place heavy burdens on packaging. The greatest challenges CMOS faces is supporting pin counts in excess of 300 in packages with low lead inductance, capacitance, and resistance.

To respond to these demands, Fujitsu has developed a clever solution in packaging to obtain the highest average pin density per board area yet achieved. This is accomplished with surface mount PGAs, which rely on narrow pin pitch (50 and even 25 mils) in a dense grid of multiple rows of pins. Since through-hole packages cannot effectively support pin pitches narrower than 70 mils, these PGAs must be surface mounted, though they still possess pins (see Figure 12).

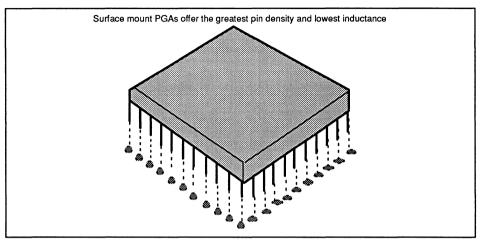


Figure 12. Surface Mount PGA

The surface mount technology also permits traces to run beneath the package leads, increasing available trace density. Figure 13 shows the solder pad design required by these high-pin-density packages.

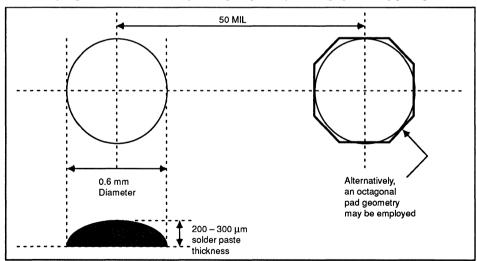


Figure 13. Solder Pad Design for Surface Mount Pin Grid Arrays

Table 5 provides an item-by-item comparison between PGAs, surface mount PGAs, and flatpacks of similar pin counts.

PACKAGE	TYPE	PIN PITCH	OUTLINE (MAX)	PIN DENSITY (Pins Per Sq Inch)
FPT – 160	Surface	25 mil	1.276" x 1.276" (1.63 sq ln)	98
PGA – 256	Through	100 mil	2" x 2" (4 sq ln)	64
PGA – 256	Surface	50 mil	1" x 1" (1 sq ln)	256
PGA - 321	Staggered	71 mil	1.72" x 1.72" (2.96 sq ln)	109
PGA – 401	Staggered	71 mil	1.922" x 1.922" (3.69 sq ln)	109

**Table 5. Comparison of Critical Features** 

The numerous electrical and mechanical advantages of surface-mount PGAs would seem to outweigh their disadvantages. However, the general state of high volume manufacturing has not kept pace with the rapid advances in semiconductor packaging. This is partly due to the requirement for state-of-the-art manufacturing equipment, which is quite expensive, and also to the need to maintain board yields with such complex devices. Therefore, in order to establish these packages as an attractive alternative, Fujitsu personnel are available to assist customers in the mounting and inspecting of these highly complex packages.

#### 3.3 A Comparison of Through-hole and Surface Mount Devices

SMDs provide improved electrical performance and reduced system size and costs. Furthermore, with plastic flatpacks of up to 160 pins and beyond available, SMDs show promise in supporting the rapidly advancing gate size complexities and high pin count of today's ASIC products at a substantially lower cost than the large ceramic PGAs. However, as the manufacturing complexities that have just been reviewed indicate, surface mounting large ASIC devices may be difficult and risky, and the designer should be cautious in their use.

If board space constraints are not critical, if the economic impact of scaling down the end system is not great, if optimal electrical characteristics in packaging are not a critical concern, then through-hole packaging may be the best solution. On the other hand, if speed and integration requirements dictate the use of very dense gate arrays, PGAs or SMT PGAs provide both through-hole and surface mount alternatives.

# 3.3.1 Socketing Surface Mount Devices

Some benefits of SMDs are available to manufacturers employing through-hole packages through the use of sockets for SMDs. Sockets are available for QFPTs, small outline packages (SOPs), CLCCs and PLCCs; however, the use of QFPT and SOP sockets is normally restricted to prototyping and burn-in, while low-cost, reliable production sockets are more commonly available for PLCCs and CLCCs. These production sockets house the SMD (they are tightly tailored to the specific package) in one of two ways. Flatpacks and LCCs use low/zero insertion force with a lid that closes down on the package. PLCCs use pressured socket contacts that drive a pin into the underside of the socket. Socket pins are arranged like those of PGAs: they are through-hole, they have 100-mil spacing (generally), and they are most commonly oriented in a grid of two rows.

One advantage of these sockets is that in applications where through-hole packaging is required and the choice of through-hole packages is limited to PGAs, a plastic SM package plus the production socket will cost less than the through-hole PGA. The scenario typically occurs when the required number of pins is between 40 and 84 for PLCCs and LCCs and up to 160 or more for the flatpacks.

Another significant reason to socket SMDs results from the manufacturing difficulties of SMDs that were presented earlier. ASIC devices are usually among the largest in the system, and the most vital and expensive. For the purpose of field maintenance, many companies feel it is more economical and reliable not to risk running an ASIC device through wave or reflow solder and risking stress fractures or other damage. Furthermore, the test probing difficulties alluded to earlier are alleviated with sockets, which usually provide easy access to the contacts. Often, once reliability of the system is proven, the boards are re-laid out with surface mount devices. Therefore, simply because a manufacturing facility isn't geared up for SMT does not mean that SMT devices cannot be used there.

#### 3.3.2 Noise Problems With Sockets

Sockets for SMDs are convenient for manufacturers not yet ready to go to SMT, or for initial prototyping where the device may frequently be removed. Socketing permits the user to gain many of the benefits of SMDs, such as reduced profile and support of high pin counts in plastic, while avoiding the drawbacks, such as special manufacturing equipment and lead probing difficulties. Unfortunately a major electrical advantage of SMDs, low pin inductance, is compromised when sockets are used. The primary result is greatly increased noise, which adversely affects overall speed and signal quality. In fact, a socketed SMD generally has a higher lead inductance than an equivalent through-hole PGA.

# 3.4 Summary of the Packaging Alternatives

Having reviewed the package selection alternatives presented in Section 2.0 and the various tradeoffs between the packages discussed in this section and summarized in Table 6 below, the designer can weigh the benefits and limitations of the various packages and arrive at an optimal packaging scheme.

Table 6. ASIC CMOS Package Types and their Characteristics

Package Type		f Physical ensions	Electrical Characteristics <sup>1</sup>	Thermal Characteristics (°C/Watt)	Usable Gates³	Relative Cost (per Pin)
Through- Hole DIP	# Pins: Pin Pitch: Body Length: Body Width:	16 to 64 100 mils .75" to 2.3" .300" to .700"	R: Medium L: High C: Low	Ceramic/Plastic θJA <sup>2</sup> : 70 - 40/ 120 - 80	Up to 17K gates	1
Surface Mount SOIC	# Pins: Pin Pitch: Body Length: Body Width:	16 to 28 10 mils 50 to 70 mils .300" to .400"	R: Medium L: Medium C: Low	Ceramic/Plastic θJA <sup>2</sup> : 110 - 80/ 130 - 105	Up to 6500 gates	1
Surface Mount QFPT	# Pins: Pin Pitch: Body Width:	48 to 260 10 mils .65" to 1.7"	R: Medium L: Medium C: Low	<b>Plastic</b> 6JA <sup>2</sup> : 95 - 60	Up to 17K gates	1
				Ceramic		
Surface Mount CLCC	# Pins: Pin Pitch: Body Width:	28 to 84 40 to 50 mils .45" to .97"	R: Medium L: Medium C: Medium	θJA <sup>2</sup> : 70 -45	Up to 25K gates	5
				Plastic		
Surface Mount PLCC	# Pins: Pin Pitch: Body Width:	28 to 84 50 mils .49" to 1.19"	R: Medium L: Medium C: Low	θJA²: 65 - 50	Up to 17K gates	1.05
			Ceramic/Plastic	Ceramic/Plastic		Ceramic/Plastic
Through- Hole PGA	# Pins: Pin Pitch: Body Width:	64 to 299 .100 mils, 70 mils 1.033" to 1.7"	R: Low/Low L: Low/Low C: High/Low	θJA <sup>2</sup> 40 - 19/ 46 - 38	Up to 75K gates	11/ 3.5-5

<sup>1</sup>R = Resistance, L = Inductance, C = Capacitance <sup>2</sup>Assuming Static Airflow Notes:

# 4.0 Electrical Considerations for the Assignment of Signal, Power, and Ground Pins

Driven by the continual demand for high speed systems, CMOS ASICs that exhibit output drive levels, rise and fall times, and propagation delays comparable to yesterday's ECL circuits are now being developed. Consequently, the problems intrinsic to ECL design (even thermal management) are now appearing in CMOS designs. These problems, based on noise and its effect on the device, are introduced in this section and possible solutions are discussed.

# 4.1 Sources and Magnitude of Noise

CMOS circuits operate by charging and discharging node capacitances through pull-up or pull-down transistor networks constructed of P channel and N channel enhancement mode (normally off) MOSFET transistors. As a result, these circuits generate noise when switching. The following review of basic CMOS circuits and how they work explains this phenomenon in greater depth.

<sup>&</sup>lt;sup>3</sup>Assuming 1.5µ CMOS Technology

# 4.1.1 Basic CMOS Circuits

Figure 14 shows a CMOS totem pole output buffer, the typical implementation for CMOS circuits, while Figure 15 illustrates a CMOS-compatible input buffer, and Figure 16 depicts a CMOS input buffer configured to be TTL compatible.

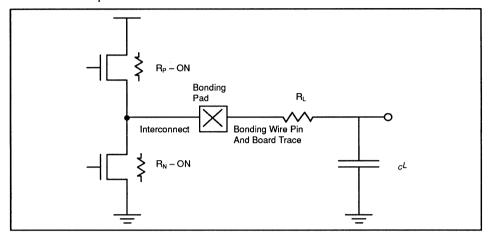


Figure 14. CMOS Output Buffer Model (Totem Pole)

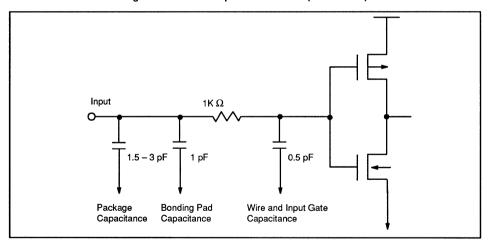


Figure 15. I/O Model, CMOS Input

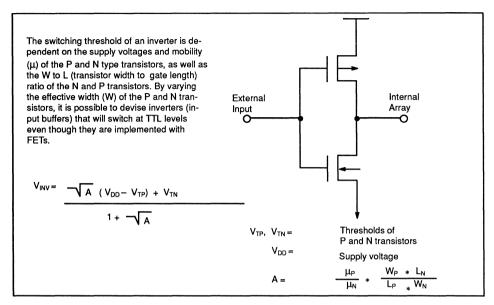


Figure 16. I/O Model, TTL Input

Internal CMOS circuits, such as the NAND gate shown in Figure 17 are typical of CMOS logic designs, which can be represented as a pull-up network and a pull-down network, each with its own logic and analog characteristics.

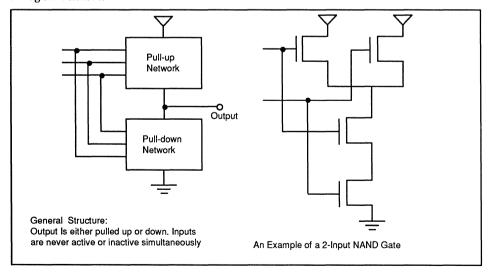


Figure 17. CMOS Basic Gate Structure: The Pull-up/Pull-down Network

The other type of element used in CMOS circuits is the transmission gate, or T-gate, which is useful for the efficient construction of multiplexers and sequential circuits (D-flops, latches, etc.) as shown in Figure 18.

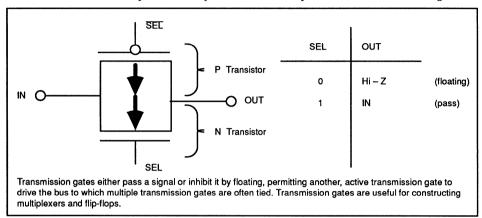


Figure 18. CMOS Basic Gate Structure: The Transmission Gate

# 4.1.2 Output Switching Noise and Simultaneous Switching Outputs (SSOs)

The greatest source of noise in a CMOS circuit is the result of an output switching either high to low or low to high, particularly into or out of a high capacitive load. CMOS outputs drive two types of loads, either CMOS loads, which are high in capacitance but low in leakage current, or TTL loads, which are lower in capacitance but higher in leakage current. Therefore, the AC and DC currents that the buffers see when they switch depend greatly on the type of driven load and its capacitance. When this load discharges through the N-type transistor of the totem pole output, as illustrated in Figure 14, the effect is that of a capacitor discharging through resistance. Consequently, the initial current is high and decreases over time as the output node capacitance becomes charged. Similar currents may be observed when charging the node capacitance, as in the case of a low-to-high transition.

Figure 19 shows the characteristic resistance and capacitance of various parts of the output of an ASIC device.

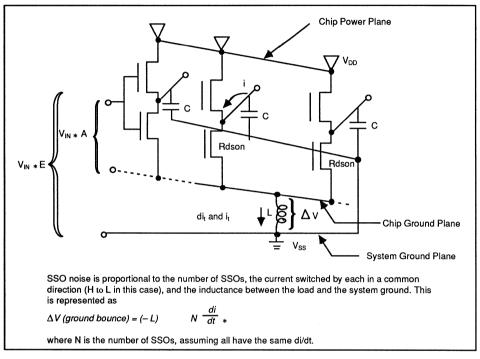


Figure 19. Electrical Model of Simultaneously Switching Outputs

Although small, the total inductance becomes a critical factor when discharging or charging output capacitance, since the instantaneous current (*i*) is high. Recall that the self-induced voltage in an inductance, (*L*) is expressed by

$$\Delta_{VINDUCED} = \frac{L * di}{dt}$$

where t is time and d is rate of change.

In a high-drive CMOS device driving high loads, such as 200 pF, through a voltage swing approaching 5 volts with a rise/fall time of < 2 ns, the instantaneous current may be

$$i = C$$
 \*  $\frac{dv}{dt} \approx C * \frac{\Delta v}{\Delta t}$  (average over rise and fall time)

This induced voltage appears as noise on the receiving end of the signal as referenced to the ground. The current on a high-to-low transition is sunk into ground, causing the current to "bounce" or rise relative to other signals referenced to it. This ground bounce phenomenon may also apply to power on low-to-high transitions, yielding a similar noise problem.

Noise on signals may cause false triggering on the input buffer(s) being driven, or at least create a window of ambiguity in the time at which the driven input should switch (see Figure 20). Therefore, noise may result in degradation in speed resulting from adding settling time to a delay and may even result in

$$nV = N \cdot L \cdot \frac{di}{dt}$$

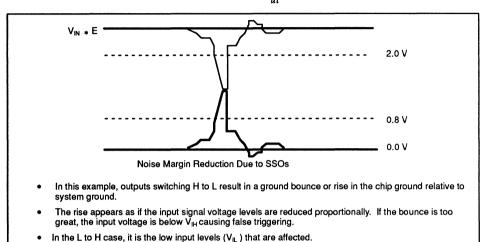


Figure 20. Effect of SSO Noise on Thresholds

Not only inductance but also characteristic resistance can create noise problems. The following paragraphs summarize the types of noise that exist in CMOS systems and explain how packaging impacts this noise.

# 4.1.3 Self-Induced Noise

Self-induced noise results when high-speed, high-drive outputs switch and introduce a spike on the signal relative to ground. The SSO effect, discussed previously, is an example of the level of self-induced noise that can occur. It is predicted by

$$\Delta V_{SI} = L \frac{\Delta i}{\Delta t}$$

where L is the inductance between the pin and ground as well as the trace inductance.  $\Delta i$  is the instantaneous current and  $\Delta t$  is the fall/rise time.

# 4.1.4 Mutually Induced Noise

Mutually induced noise (a form of crosstalk) occurs when a signal trace that has been running parallel to another for some distance switches, inducing a voltage into the adjacent wire. Since both inductive and capacitive coupling occur only during signal transition and propagation, the effect is additive, as the signal propagates down the trace. Resultant noise propagates in both the forward and backward directions down the line. The forward crosstalk has a pulse duration equal to the rise and fall of the signal, with an amplitude equal to the difference between the capacitive and inductive coupling. Backward crosstalk has a pulse duration equal to the transition time down the trace and an amplitude dependent on the sum of the inductive and capacitive coupling as well as the trace length.

# 4.1.5 Capacitive Coupled Noise

Another form of crosstalk resulting from mutual signal coupling, this noise occurs in proportion to the dielectric constant of the board, the distance of trace separation, and the trace length and width. Acting as two thin parallel plates, these traces couple switching current as integrated over time.

# 4.1.6 Ringing on Signals

From basic circuit theory, the designer will recall that if the signal line impedance does not match the output impedance of the buffer, then the signal is not naturally dampened. If the impedance of the load is less than that of the buffer, the signal is over-damped and will have a slow rise/fall time. However, if the buffer possesses lower impedance, then the signal is under-damped and may ring, as illustrated by Figure 3. Typically, signal line impedances are in the range of 50 to 250  $\Omega$ , while in the past buffers possessed "on" resistances of 500  $\Omega$  to 2 K $\Omega$ . However, due to the need for higher current sourcing/sinking and faster switching speeds, "on" resistances of output buffers have come down to the 10- to 50-  $\Omega$  range, requiring the use of special termination techniques, discussed in the Fujitsu Application Note "Interfacing CMOS and BiCMOS VLSIs."

# 4.1.7 iR Drop

Up to this point, the sources of noise discussed have depended on inductance or capacitance. Since the DC current that a ground pin may sink, or that a power supply pin may source can be significant, the familiar voltage drop across a resistor, as current passes through it, is also a source of noise. This iR drop is the phenomenon that limits the sum of source and sink currents through power and ground pins respectively. Ohm's Law describes the effect of this noise source in the following equation defining voltage rise or drop due to iR effects:

$$\Delta V = R \quad * \quad \sum_{n=0}^{N-1} i_n$$

where

R is the output pin-to-ground (sink) resistance, or power pin return-loop (source) resistance (including the "on" resistance of the respective N or P channel device) and

 $i_n$  is the current through the nth output pin connected to this common ground or power pin.

# 4.1.8 Current Spiking or "Crowbar Noise"

As Figure 14 illustrated, a CMOS output buffer is constructed as a totem pole in which the output is taken from the common source (P type) and drain (N type) with the drain of the P type connected to power and the source of the N type connected to ground. When the input to the totem pole (the P and N gates) switches, the Miller capacitance of the gate causes the gates to charge or discharge at some specified time constant. It is possible that both transistors can be on, one in saturation and the other passing through the linear region, creating a current path between power and ground that can damage the device. This is less a concern for internal transistors than it is for the "beefy" transistors at the I/O. This current spiking can not only introduce noise on the power and ground planes, but may damage the device as well. For this reason, Fujitsu has taken precautions in the design of the CMOS output buffers to prevent this problem from occurring.

# 4.2 Recommended Strategy for Pin Assignment

The assignment of Clock, Scan, and other signals, as well as power and ground, to specific pins on the package affects electrical behavior (speed, noise, reliability, etc.), board manufacturing requirements, and device reliability. Therefore, optimal pin assignment strategies should consider the variables over which the user has control (placement of non-scan inputs, outputs and bi-directionals) and the variables over

which the vendor has control (power, ground and scan signal placement). Out of these relationships a method of placement can be developed, using the following approach:

- (a) Prioritize the signals whose placement is most critical.
- (b) Establish guidelines for the location of these signals, both in absolute position and relative to other signals.

# 4.2.1 Prioritization of Signals for Placement

Noise minimization is used to establish signal prioritization. All of the various forms of noise discussed in the last section are dependent on either i or di/dt, and L, M, R, or C. The signals affect i and di/dt, while the package pin location affects L, R and C. Figure 21 provides an illustration of how electrical characteristics vary by pin position.

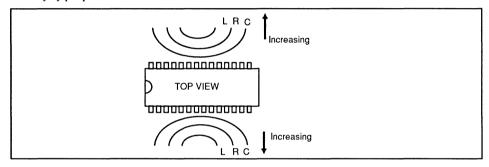


Figure 21. Variation in Inductance, Resistance, and Capacitance as a Function of Pin Position

In general, the further a pin's external contact is from the die connection, the greater its resistance, impedance, and capacitance. Therefore, signal prioritization is established according to current or its time derivative, while location is guided by package pin characteristics. Input signals are classified by their noise sensitivity. If a spike on an input could be disastrous (as with a clock), that signal should be carefully located. Table 7 classifies signal type by electrical characteristics.

Signal Type	Current Characteristics (General)		
Ground	Highest i, DC, and di/dt		
Power	High i, DC, and di/dt		
High drive outputs	High di/dt		
Clocks	Highest noise sensitivity		
Low drive outputs			
Other Signals			

Table 7. Electrical Characteristics of Each Signal Type

# 4.2.2 Characteristics of Package Pins by Location

The inductance, capacitance, and resistance, all of which are critical to minimizing noise, are related not only to board construction, but also to the pin position on given packages, and the circuit to which the pins are bonded. The pin, lead frame, bonding wires, pads, and buffers (input, output or bi-directional) all influence the characteristic L, R, and C of the line. See Figure 22.

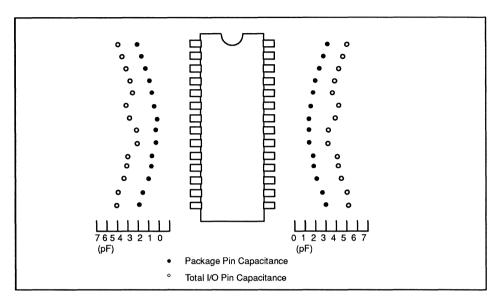


Figure 22. Measured Pin Capacitance by Package Position

# 4.2.3 Relating Signal Type to Pin Location

Since power and ground pins demand a large DC current (i), iR drops are of great concern. Therefore, Fujitsu assigns power and ground to pins with minimum resistance (and inductance). High-drive outputs exhibit a large di/dt, resulting from high capacitive loading, so the best pins for these signals are those of minimum inductance. Furthermore, adjacent pins possess the greatest M, and thus couple the most M di/dt noise. This means that noise-sensitive inputs, such as clock inputs, should be isolated from pins that handle high di/dt, such as high-drive outputs.

#### 4.2.4 Minimizing iR Drops on Power and Ground Pins

Placement of ground pins is critical because noise on ground affects the voltage level of all signals referenced to it. For this reason, Fujitsu has preassigned power ( $V_{DD}$ ) and ground ( $V_{SS}$ ) signals for all packages in a given gate array family according to the electrically optimal locations. Preassigning power pins permits Fujitsu to develop load boards (which interface the packaged device to the tester) advanced enough to carry out high-speed functional testing of devices with high I/O count and to drive devices with relatively low noise. Fujitsu also took into consideration manufacturing issues such as adjacent pin shorting due to probes and package rotation. The predefined power and ground assignments for Fujitsu devices are found in the Package Pin Assignment Guide in the Design Manual for the appropriate gate array family, and are used in conjunction with the Package Matrix to determine pin assignment.

# 4.2.5 Minimizing the Self-Inductance of a Signal

Fujitsu believes that an ASIC designer concerned about designing a mini-computer, PC, mainframe or other complex system should not have to be concerned with determining specific on-chip noise issues, particularly since board-level noise issues are demanding enough. Therefore, Fujitsu developed a straightforward grouping scheme for the placement of various types of signals relative to their distance from the nearest power and ground pins. As Figure 23 shows, the self-inductance associated with a given signal is

a function of the length of wire between it and its nearest ground (for a falling transition) or power (for a rising transition).

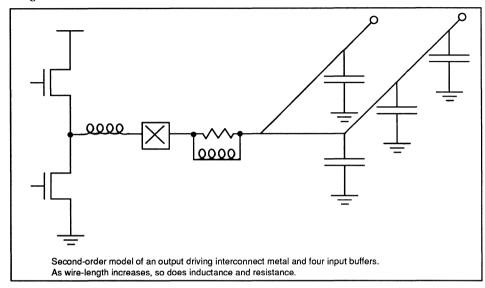


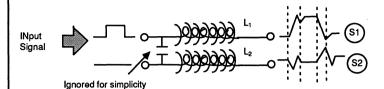
Figure 23. Self-inductance in a Circuit

Since di/dt can vary greatly for outputs within a group, there are some general restrictions relating to SSOs and their total current to the number of grounds on the chip. This is done by summing representative values like those shown in Table 5–4 in Chapter 4, which are weighed depending on the IOL of the given output buffer. Notice that, if the output buffer employs noise limiting circuitry (edge rate grading) then di/dt is less and the representative value is also less, meaning more of these outputs can be supported per ground pin.

In summary, to ensure that the iR drops and the ground bounce effect (L di/dt) are within reasonable limitations, Fujitsu has established guidelines for determining the number of necessary grounds and defining the pinout.

# 4.2.6 Placement of Clock and Asynchronous Clear/Preset Signals

In addition to causing the ground bounce and iR drops that can deteriorate an output signal's quality and alter the ground reference, output switching can also couple noise into adjacent sensitive inputs by mutual inductance, as shown in Figure 24. For that reason, the designer should ensure that clocks and asynchronous clear and preset signals are not placed near outputs, particularly high drive outputs. To further isolate inputs from noise, the designer should minimize the inductance (length) of the return loop from the input buffer to ground by placing this type of input near a ground pin. The mutual inductance of the input buffer itself can be minimized if it, and any outputs nearby, are not assigned to high inductance pins. As discussed in Section 4.2.1, the center pins of a DIP, flatpack, or PLCC possess the lowest L and R, as do the inner rows of PGAs, making them most suitable for  $V_{\rm DD}$ ,  $V_{\rm SS}$  and high drive outputs. But the edges of the package, while suitable for data signals, should be avoided when placing clock and other sensitive signals, as they exhibit a high mutual inductance and large iR drop.



Noise is introduced on the adjacent lead S2 as S1 is driven in a manner described by Faraday as

$$V_S = -M \frac{di}{dt} \frac{S1}{dt}$$

where M is the mutual inductance between the adjacent leads.

If S2 is also being driven, then the mutually induced noise is superimposed on the self induced noise already present, as described by

$$V_{S2} = -M \frac{di}{dt} + L_2 \frac{di}{dt} \frac{S2}{dt}$$

Figure 24. Causes of Crosstalk

# 4.3 Summary: Choosing the Package and Assigning the Pins

This discussion of noise as related to packaging and its effect on pinout should help the designer appreciate the care Fujitsu has taken to ensure that noise margins within the device are restricted to maximize system reliability. It should also provide the designer with a basis for establishing optimum pin assignments. A step-by-step procedure for choosing an optimal package and assigning pins to it follows.

#### 4.4 Package Selection Checklist

When selecting a package for an ASIC device, the designer should consider the following points:

- a. Define a subset of the Fujitsu packages that can be supported by your company's manufacturing capabilities.
- b. Estimate, as closely as possible, the gate and I/O counts of the circuit(s) to be packaged.
- c. Determine the number of power and ground pins required by considering the following:
  - 1. Representative value limitations for SSOs
  - 2. Limitation of the sum of the sink current (I<sub>OL</sub>) per ground pin
  - Limitation of instantaneous current per ground pin to satisfy metal migration restrictions
- d. Using the package and pin assignment section of the Design Manual, determine the packages that satisfy the signal, power, and ground pin requirements of the circuit.
- Make sure that the electrical, mechanical, and thermal properties of the chosen packages are suitable for the application.
- f. Check the mechanical dimensions in Fujitsu's ASIC Package Catalog and the power and ground pin assignment tables and grouping charts in the appropriate package and pin assignment tables for the chosen technology. Please contact Fujitsu regarding pricing trade-offs when evaluating packages or partitioning the system.

# 4.5 Pin Assignment Checklist

- a. Follow Fujitsu's pin assignments in the Package and Pin Assignment section of the Design Manuals. Although multiple pinouts of the same package may be offered in some cases, all power and ground signals indicated on the chosen package must be connected on the board.
- b. Assign input pins (in excess of 5 MHz) and high power output buffers (I<sub>OL</sub> = 24 mA) according to the appropriate pin assignment table.
- c. Place all high-drive (power and high power) outputs near ground pins; the higher the drive, the closer they should be placed. SSOs should be placed particularly close to ground pins.
- d. Place SSOs in groups belonging to given ground pins.
- e. Distance noise-sensitive signals such as clock and asynchronous clear and preset signals away from SSOs and high-drive outputs. Also, assign them to pins with low inductance and resistance, preferably near a ground, if one is available away from SSOs or high-drive outputs.
- Place SSOs on low inductance pins, such as those located on the inner rows and middle position of the PGAs.

These guidelines assist the designer in choosing the best package for the application, resulting in a device with reliable and predictable electrical performance and without harmful DC and AC effects on the system. There are other system interface issues such as device decoupling and termination that should be considered during design. These are discussed in Fujitsu's application note, "Interfacing CMOS and BiCMOS VI.SIs."

# 5.0 Thermal Issues in CMOS ASIC Packaging

CMOS has traditionally been associated with low power, one of the classic advantages it has over ECL. While ECL continually draws high current to supply its internal differential amplifiers and emitter-follower circuits, CMOS draws current primarily when it is switching. The total power dissipation of a CMOS device is dependent on the number of gates, the switching frequency, and the loading on the output of the gates. The revolution in CMOS technology that has resulted in densities of 100K gates has been accompanied by increases in all of the factors influencing power dissipation. Prior to 1985, when Fujitsu introduced the world's first 20,000 gate array, the C20000UH, CMOS gate arrays were not of sufficient integration density to warrant concerns about thermal control, but advancing CMOS technologies have forced this issue to the surface.

Because power is the product of current and voltage, power dissipation is important when defining the necessary power supply currents. Propagation delays and reliability of a device are also dependent on the temperature at which the die operates, as discussed in Sections 2.3.3 and 2.4.4. To ensure that speed and reliability requirements are satisfied, the designer needs to estimate the power dissipation of the device and, from this information, choose appropriate packages and system cooling techniques.

#### 5.1 Estimation of Power Dissipation in CMOS Circuits

There are two constituent factors in the power dissipation of a semiconductor device: the DC power, which is dependent on the steady-state (quiescent) current, and the AC or dynamic power.

# 5.1.1 Estimation of Dynamic (AC) Power Dissipation

CMOS circuits are constructed of FETs, which possess very small leakage currents. Therefore, CMOS possesses a low quiescent or steady-state current. CMOS dissipates power primarily while it is charging or discharging node capacitance, or drawing switching current, which occurs as a gate changes state. This can be modeled as the familiar pull-up/pull-down circuit discussed in Section 4.1, charging and discharging a node capacitance,  $C_L$  (shown in Figure 14). This model holds true whether the node is internal or off-chip.

1

The switching current is a result of charging and discharging the node capacitance which, for periodic signals, occurs twice a cycle: once while charging the capacitance, and once while discharging it. The energy involved in charging or discharging a capacitance is  $1/2(CLV^2)$ . The power is the energy divided by the period of time between successive changes (the clock period, T), multiplied by the two transitions that occur per cycle. Therefore, the dynamic or switching current of a CMOS circuit is defined as

$$Pd-dyn = 2 \qquad * \quad \frac{(C_L * V^2)}{2 * T} = (C_L * V^2) * f$$

where *V* is the supply voltage and *f* is the frequency of the given signal.

This is the power calculation for a single gate. The power dissipation for entire chip, however is much more complicated, since not all gates are simultaneously active. The degree of switching activity varies greatly within a circuit and depends on the nature of the circuits (synchronous sequential gates tend to switch concurrently, while combinatorial gates switch more randomly), the input stimulus (whether the circuit is stimulated at a periodic interval or asynchronously), and other design-dependent issues. Based on Fujitsu's experience, gate activity is on the average about 20 percent. This same figure is applied to the power estimation for output and input buffers.

# 5.1.2 Estimation of Quiescent (DC) Power Dissipation

There are two sources/sinks of DC current in a CMOS ASIC: the leakage current of the gates (gate leakage) and the DC current that flows through output and bidirectional buffers in output mode. The gate leakage in CMOS devices, even dense ones, is in the range of tens of microamperes, and is negligible. The DC current of the output buffers is the current that the buffer sources or sinks in steady state. This current level depends on the leakage currents of the driven loads, but for simplicity will be assumed to be equivalent to the  $I_{OL}$  and  $I_{OH}$  rating of the buffers. The DC power can be estimated for each output buffer by analyzing:

- a. the product of source current times the voltage difference from the power rail  $(V_{DD} V_{OH})$ , and
- b. the sink current times the low-level voltage  $(V_{OL})$ .

This calculation is valid provided the duty cycle, or the portion of the cycle in which the output is low versus the portion of the cycle in which the output is high, weighs the sum of the two components. The total DC power may be determined by extending this method to each output and bidirectional buffer.

#### 5.1.3 Estimation of Total Power Dissipation

The total power dissipation of a circuit is the sum of the DC and AC components. I/O buffers dissipate both DC and AC power when switching, while internal gates may be considered for the sake of simplicity, to dissipate only AC. The theory behind CMOS power dissipation is simple; however, the task of calculating the power dissipation can be tedious and prone to error. Therefore, Fujitsu has devised methods for estimating the power dissipation for each CMOS technology. These methods are presented in the Design Manual for the appropriate technology, available through the Field Applications Engineers at local Fujitsu Sales Offices or Technical Resource Centers.

# 5.2 The Relationship Between Power Dissipation and Temperature

A device draws current through the power supply pins and the I/O buffers. As it does so, it dissipates thermal energy proportional to the power dissipated in the device. Assuming that the power dissipation of a device has been estimated as  $P_d$ , using the method described in Section 5.1.1, how can one relate this power to the temperature of the die and the package, and also determine the warming effect on the surrounding environment?

The answer lies with two principles of heat transfer: conduction and convection. When an object is in a state of thermal equilibrium it is isothermal, seeing a constant temperature across its body. As the tem-

perature of one end of the object is raised by the introduction of energy, it is no longer in equilibrium; heat begins to flow from the warmer region to the cooler region through the process of conduction.

When a lake in winter is filled with water at a constant temperature, just above 32°F, it may still freeze. It will freeze at the surface, however, not the bottom. This is because heat is drawn from the water into the air through convection, the act of cooling by a gas.

These same mechanisms, conduction and convection, act upon a packaged semiconductor device and determine its junction temperature, the package or case temperature, and the warming effect on the surroundings.

#### 5.2.1 Determining the Junction Temperature of a Device

Figure 25 shows the paths through which heat flows in a packaged device. Each interface of materials with different properties of thermal conduction must be considered when determining the flow of heat from the die to the surroundings. The back side of the die is attached to a lead frame or slug, usually by means of a eutectic bond (material heat bonded with some conductive material, such as silver). Heat flows through this path from the die to the package, then from the package to the surrounding air.

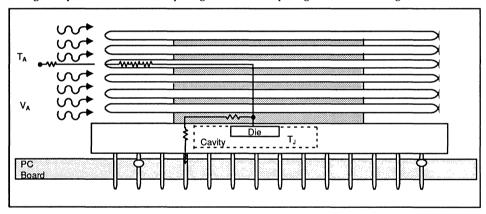


Figure 25. Heat Flow through a Cavity-down Ceramic PGA with an Annular Fin Heat Sink

From the die junction to the package, there is some associated thermal impedance (or resistance to the flow of heat). This impedance can be calculated, but may also be estimated in the following way. Operate a device and determine its power dissipation. Then, using some mechanism such as a thermal diode, whose forward bias voltage tracks linearly with temperature, determine the junction temperature. Then, after measuring the case temperature, determine the thermal impedance along the path from the die junction to the case (package body) using the following equation:

$$\theta jc = \frac{(Tc - Tj)}{P_d}$$

where  $T_c$  and  $T_i$  are the case and junction temperatures, respectively.

A similar procedure is followed when determining the thermal impedance between the junction and the ambient environment, except that the case temperature is replaced by the measurement of the ambient temperature

$$\theta ja = \frac{(Ta - Tj)}{P_d}$$

While  $\theta_{jc}$  relies on conduction as its cooling mechanism,  $\theta_{ja}$  reflects convective cooling. Therefore,  $\theta_{ja}$  varies with airflow and is specified at a given airflow, or as static (= 0).

Since thermal impedance depends on the heat conduction path between the die and some other interface, it can be modeled the same way as current flowing through real impedance or resistance. Therefore, as in circuit theory, when multiple interfaces are oriented in parallel, the thermal impedance is lowered. However, the situation is different from circuit theory in that when a very low impedance interface, such as a heat sink, is placed in the conduction path the flow capacity is increased, with the heat sink pulling heat out at a faster rate, lowering the thermal impedance.

# 5.2.2 Using Thermal Impedance Data

Thermal impedance information and power dissipation information are used to estimate junction temperature and ambient temperature rise. Which impedance figure to use is based on how the device is to be cooled. If the device is air cooled (convective), then  $\theta_{ja}$  should be applied, while  $\theta_{jc}$  should be used if conductive techniques such as heat pipes or cold plates are employed. For example, the junction temperature may be obtained by multiplying the power dissipation of the device by the appropriate  $\Theta_{ja}$  and adding the ambient temperature. It is not surprising that this indicates that a small thermal impedance is desirable to achieve a low junction temperature.

Junction temperature is used to determine worst case delay multipliers and the package options for Fujitsu's CMOS AU (Sea-of-Gates) family. The junction temperature also indicates whether reliability goals are being met. The designer can trade off packages (which exhibit varying thermal impedances) with cooling techniques (such as varying the amount of airflow in a system) to achieve the desired junction temperature and consequently, worst case delay multiplier and reliability targets.

# 5.3 Summary of Thermal Issues

Although thermal factors in CMOS design have not previously been an issue, the increased frequency and density of current generations of CMOS devices require such considerations to be made. This section has surveyed some of the issues involved in applying thermal analysis to CMOS devices and using the information gained from such analysis to determine the appropriate packaging and cooling techniques.

# 6.0 Summary of the Note

As VLSI circuits increase in complexity, pin count and die size increase as well, placing greater demands on packaging, board layout, and manufacturing. Fujitsu has addressed these problems with exotic forms of packaging such as the surface mount PGA and the staggered PGA, while also stressing the importance of other surface mount packages. But simply making these packages available is not enough; Fujitsu must also provide the technical support necessary to ensure that these packages can be used successfully by our customers. Field Applications support in the local sales offices, technical information such as this Application Note, and packaging consultants at Fujitsu's San Jose headquarters all provide this support.

# 5

# References

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# **UHB Series CMOS Gate Array Unit Cell Library**

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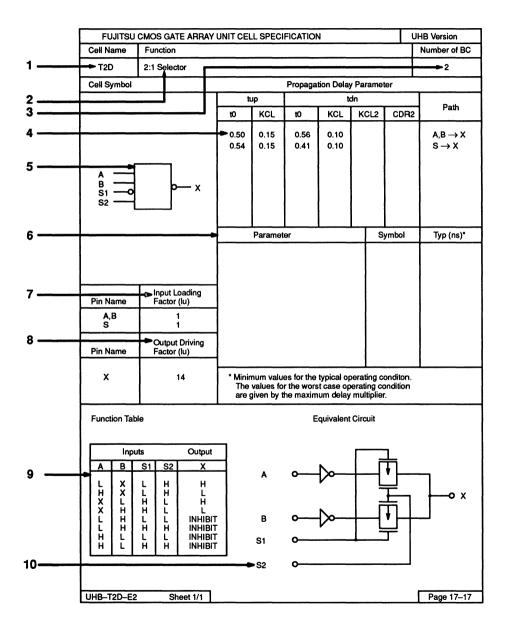
# **Unit Cell Specification Information**

This section contains specifications for all the unit cells available for the UHB Series CMOS Gate Arrays. The unit cell (gate array) is a functional group of one or more basic cells or gates. A basic cell contains one pair of P-channel and one pair of N-channel transistors.

#### How to Read a Unit Cell Specification

The following paragraphs numbered 1–10 explain how the information given in the UHB Unit Cell Library is organized. Each of the numbers corresponds to an area of the Unit Cell Library page illustrated on the right.

- 1. The unit cell name appears in the upper left corner of the page.
- 2. The unit cell function is given on the same line as the unit cell name.
- The number of basic cells (BC) or equivalent that make up the unit cell is shown in the upper right corner of the page.
- 4. Propagation delay parameters for the unit cell are given in a table on the upper right side of the page. The basic delay time of the unit cell (t0) is given in ns. K<sub>CL</sub>, the delay constant for the cell (delay time per load unit) is given in ns/pF. K<sub>CL2</sub> and C<sub>DR2</sub> are a delay constant and an output driving factor used to calculate delay when a unit cell is loaded beyond its published output driving factor (C<sub>DR</sub>).
- 5. The cell (logic) symbol is shown in the top left box under the cell name.
- Clock parameters (in ns) for unit cells such as flip-flops and counters that make use of clock signals are given in a table directly below the propagation delay parameters.
- 7. Input loading factors are shown in a table directly under the cell symbol box on the left side of the page. The input loading factor is the value of the load placed on a net by the connection of the unit cell input. Unit cell loading factors are shown in load units (lu). The Fujitsu CMOS load unit is the input capacitance of an inverter used for the measurement and calculation of capacitive loads presented to unit cells within the gate array.
- The output drive factor is shown directly under the input loading factor. The output drive factor is the maximum number of load units the unit cell can drive while performing at published specifications.
- 9. The function (truth) table, if applicable, is shown in a box at the lower left side of the page.
- 10. The unit cell schematic, or equivalent circuit, illustrates how discrete components would be connected to perform the unit cell function. It is shown in the lower right corner of the page or on the page following.



# **Inverter and Buffer Family**

Page	Unit Cell Name	Function		Basic Cells
2–7	V1N	Inverter		1
2–8	V2B	Power Inverter		1
2–9	V1L	Double Power Inverter		2
2-10	B1N	True Buffer		1
2–11	BD3	True Delay Buffer	(> 5 ns)	5
2-12	BD4	Delay Cell	(> 4 ns)	4
2-13	BD5	Delay Cell	(>10 ns)	9
2-14	BD6	Delay Cell	(>22 ns)	17

FULTITSII (	CMOS GATE ARRAY U	NIT CEL	I. SPECT	FICATIO	N		"UHI	B" Version
Cell Name	Function	MII ODD	n ornor.	LICATIO	N		1	Number of BC
V1N	Inverter							1
Cell Symbol			up Prop	agation	Delay td	Paramet	er	T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.28	0.16	0.35	0.09	0.12	4	Path A → X
	N							
Α	> x							
	V							
		Parame	ter			l s	ymbol	Typ(ns)*
		Turume				-+-	<u>,</u>	135(115)
	Input Loading							
Pin Name	Factor (lu)					1		
A	1							
						}		
	Output Driving							
Pin Name	Factor (lu)							
Х	18							
				_				1141
		Tho	mum val	ues for	the ty	pical o	perati:	ng condition. g condition
		are	values given h	v the m	aximum	delav m	ultipl	ier.
			821011 2	<i>y</i> • • • • • • • • • • • • • • • • • • •				ZZZ.
UHB-V1N-E1	Sheet 1/1							Page 1-1
4 TI4 DT	-11CCC 1/1							

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECT	FICATIO	N		"UHP	" Version
Cell Name	Function		01201	1011110	···		I N	lumber of BC
V2B	Power Inverter							1
Cell Symbol				agation			er	,
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.25	0.08	0.25	0.05	0.08	7	A → X
A	> х							
Α	^							
					,			
		Parame	ter			S	ymbol	Typ(ns)*
							•	*********
						1		
						}		
	Input Loading					l		
Pin Name	Factor (lu)					1		
A	2							
						İ		
 	<u> </u>					l		
D. 11	Output Driving					Ì		
Pin Name	Factor (lu)					1		
Х	36							L
		* M:=:			+ha +**	mical a		a condition
		The	mum vai	for the	worst	bicai o	perating	ng condition. g condition
		270	varues given b	tor the m	WOISE	dolaw m	ultinli	or Condition
	_1	are	PTAGIT D	, cue m	~v+mmm	acray III	CI CIPII	
UHB-V2B-E1	Sheet 1/1							Page 1-2

	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UHE	" Version
Cell Name	Function			1	Number of BC			
V1L	Inverting Clock	Ruffer					- 1	2
Cell Symbol	Inverting Glock	Durier	Prop	agation	Delay	Paramet	er	
			up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.35	0.04	0.67	0.03			A + X
A	> x							
·								
		Parame	ter			S	ymbol	Typ(ns)*
						1		
						1		1
	Input Loading							1
Pin Name	Factor (lu)							
A	4					- 1		
						- 1		1
	0.1					1		ļ i
Pin Name	Output Driving					j		1
X	Factor (lu)					- 1		
		* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
		are	values given h	y the m	aximum	case op delav m	mitini	g condition
	I		<u> </u>	<i>y</i>				
UHB-V1L-F2	Sheet 1/1							Page 1-3

FULTITSU	CMOS GATE ARRAY U	NIT CEL	L SPECT	FICATIO	N		1111	HB" Version
	Function	000	_ 0.001		•			Number of BC
B1N	True Buffer							11
Cell Symbol				agation	Delay	Paramet	er	-
			up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.58	0.16	0.68	0.08			A → X
								1
								1
A	У х							
n n	^							·
		Parame	ter	L		S	ymbol	Typ(ns)*
								1
								}
	Input Loading							
Pin Name	Factor (lu)							(
A	1					į		
						-		
	<u> </u>							
	Output Driving	Ì						
Pin Name	Factor (lu)	l				1		
Х	18	ļ						
		٠ ـ يىر ب		f	*hc *	minal -		ina aandibic=
		" mini	mum vai	ues for	une ty	DICAL C	perat:	ing condition.
		ine	values	for the m	worst	dalaw -	erati ml+:-	ng condition
		are	PTAGH D	y che m	GVTMAM	uciay II	ar orb	1101.
1								
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Į.								
UHB-B1N-E1	Choot 1/1							Page 1-4
OND-BIN-EI	i bheet 1/1 l							1 4 4 5 4 4 4

FUJITSU CMOS GATE ARRAY 1	NIT CEL	L SPECT	FICATIO	N		"ÜH	B" Version
Cell Name Function	000					1 311	Number of BC
BD3 Delay Cell Cell Symbol	T	Pron	agation	Delay	Paramet	<u> </u>	5
Gell Bymbol	t	up	agation	td	n	<u>er</u>	T
	t0	KCL	t0	KCL	KCL2		Path A → X
	5.33	0.16	4.71	0.12	0.13	4	$A \to X$
							1
							İ
						İ	1
						1	
A — > — X						l	
	1						1
İ							
	1						
	Parame	ter			S	ymbol	Typ(ns)*
				-			
Input Loading	4						1
Pin Name Factor (lu)							
A 1	1						
Output Driving	1						
Pin Name Factor (Lu)	_						
X 18							
	* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
	The	values	for the	worst	case or	eratir	ng condition
<u> </u>	are	given b	y the m	aximum	delay n	ultip	ier.
							İ
							<u> </u>
UHB-BD3-E1   Sheet 1/1							Page 1-5

F	UJITSU	CMOS GATE ARRA	Y UNIT CEI	L SPECI	FICATIO	N ·			HB" Version
Cell	Name	Function							Number of BC
								Ì	_
	D4	Delay Cell		n		D-1-6	Damanat		4
Cell	Symbol			Prop	agation	Delay	Paramet	er	
			t0	KCL	t0	KCL	KCL2	CDR2	- Park
			3.56	0.57	4.10	0.31	0.36	4	Path A → X
			1 3.30	0.57	4.10	0.51	0.50	7	" "
			į.						
			ı						1
			ı						
			l						
			1		1			ł	
		<u> </u>	į					1	
	A —	x	1					l	
			I					1	
									1
			İ					l	1
			Parame	eter		·	l s	ymbol	Typ(ns)*
							ł		
			l				į		
			1				I		
		Input Loadir							
Pin	Name	Factor (lu)	•						- 1
	A	4	_						
							- 1		
		Output Drivi							
Pin	Name	Factor (lu)							
	X	6							
					_	_			
			* Min:	imum val	ues for	the ty	pical c	perat	ing condition.
			Ine	values given b	for the	WOIST	dalaw w	erati	ng condition
		. l	are	given i	y the m	aximum	delay a	urcip	iiei.
l									
1									
1									
UHB-	-BD4-E2	Sheet 1/1							Page 1-6

FILTTTCII C	MOS GATE ARRAY U	NIT CEL	CDECT	EICATIO	NT .		l WITH	B" Version
	Function	NII CEL	L SIECI	FICATIO	14		1 011	Number of BC
BD5	Delay Cell							9
Cell Symbol		-	Prop up	agation	Delay td		er	
		to	KCL	t0	KCL	KCL2	CDR2	Path
		10.92	0.16	10.35	0.10	0.15	4	A + X
		1 1						1
1	_	]						
Α —	x							1
		Parame	ter			S	ymbol	Typ(ns)*
		1						
	·	]						
	Input Loading					ŀ		
Pin Name	Factor (lu)	ł				1		
A	1	l				l		1
						-		
l		1				.		
Dia Nama	Output Driving Factor (lu)							
Pin Name X	18	1						
		* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
		The	values	for the	worst	case op	eratin	g condition
	<u> </u>	are	given b	y the m	aximum	delay m	ultipi	ler.
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UHB-BD5-E1	Sheet 1/1							Page 1-7

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		UH!	B" Version
Cell Name	Function							Number of BC
BD6	Delay Cell							17
Cell Symbol				agation	Delay td	Paramet	EI	
		to	up KCL	t0	KCL	n KCL2	CDR2	Path
		22.00	0.17	21.82	0.09	0.14	4	A + X
	_							
Α	<b>X</b>							
,								
								1
		Parame	ter			S	ymbol	Typ(ns)*
		1				-		
		1				İ		
						l		1
	Input Loading	1				l		
Pin Name	Factor (lu)	1						
A	1					- 1		
						- 1		
						- 1		
	Output Driving	1						
Pin Name	Factor (lu)					-		
Х	18							
		* Mini	mum val	ues for	the tv	pical o	perati	ng condition.
		The	values	for the	worst	case op	eratin	g condition
	1	are	given b	y the m	aximum	delay m	ultipl	ier.
UHB-BD6-E1	Sheet 1/1							Page 1-8

## **NAND Family**

Page	Unit Cell Name	Function	Basic Cells
2–17	N2N	2-input NAND	1
2-18	N2B	Power 2-input NAND	3
2-19	N2K	Fast Power 2-input NAND	2
2-20	N3N	3-input NAND	2
2-21	N3B	Power 3-input NAND	3
2-22	N4N	4-input NAND	2
2-23	N4B	Power 4-input NAND	4
2-24	N6B	Power 6-input NAND	5
2-25	N8B	Power 8-input NAND	6
2–26	N9B	Power 9-input NAND	8
2-27	NCB	Power 12-input NAND	10
2-28	NGB	Power 16-input NAND	11
2-29	N3K	Fast Power 3-input NAND	3
2-30	N4K	Fast Power 4-input NAND	4

FULL TOOL C	WOO CAME ADDAY I	VITTE CET	CDECT	PTCATTO			1 117.77	ID! 17
Cell Name	MOS GATE ARRAY U	NII CEL	L SPECI.	FICATIO	N		1 UF	IB" Version Number of BC
Sell Name	1 0110 01011							TARRET OF DO
N2N	2-input NAND							1
Cell Symbol			Prop	agation	Delay :	Paramet	er	
		t	up	<u> </u>	td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.37	0.16	0.56	0.14			A + X
								1
								1
A1 ——	<u></u>							
A2 -	<i>р</i> — х							
		Parame	ter	<u> </u>		1 0	ymbol	Typ(ns)*
		rarame	201			-   -	, 01	1,5(113)
						ŀ		
						1		
						j		
	Input Loading					-		
Pin Name	Factor (lu)							
A	1	i				l		1
						- 1		
								1
						l		
	Output Driving							
Pin Name	Factor (lu)					1		
X	18							
		# Mini	mum 1701	une for	the tw	nical o	norat.	ing condition.
		The	wum vai valnas	for the	worst	rase on	perati	ng condition
		are	varues given h	v the m	aximum	delav m	ultip	lier.
		arc	SIVEN D	y une a	UATHUM .	uciu, i	СТОТР	1101.
								İ
UHB-N2N-E2	Sheet 1/1							Page 2-1
OHD 11211 EZ	DIEEC 1/1							

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UI	HB" Version
Cell Name	Function							Number of BC
N2B	Power 2-input N	AND						3
Cell Symbol				agation	Delay	Paramet	ter	
			up		td		T === :	<b>⊣</b>
		t0	KCL	t0	KCL	KCL2	CDR2	Path A → X
		1.10	0.08	1.42	0.04			$A \rightarrow X$
							1	İ
							1	
							1	
							1	
							1	
A1	·						1	
A2	_ х						1	
	_							
							1	
		'			1		1	
		Damassa	<u> </u>	L	L	<u> </u>	Crmbo <sup>1</sup>	Type (ng)*
l		Parame	LEI				Symbol	Typ(ns)*
								1
								1
<b></b>	Input Loading							
Pin Name	Factor (lu)							
A	1							
1 -	1					1		
1								
1						İ		
	Output Driving	1				1		
Pin Name	Factor (lu)							
Х	36							
		* Mini	mum val	ues for	the ty	pical	operat:	ing condition.
		The	values	for the	worst	case o	perati	ng condition
		are	given b	y the m	aximum	delay	multip	lier.
}								
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1								
IJHR-N2R-F2	Sheet 1/1							Page 2-2
1 112	1 -11000 1/1							1 0

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UHI	B" Version
Cell Name	Function						1	Number of BC
N2K	Power 2-input N	AND						2
Cell Symbol	TOWER 2 INDUC N		Prop	agation	Delay	Paramet	er	
			up		td	n		D.o.
		t0 0.37	KCL 0.08	t0 0.43	KCL 0.07	KCL2 0.09	CDR2	Path A → X
		0.07					-	
_								
A1	) x							1
A2 —								1
		Parame	ter			S	ymbol	Typ(ns)*
								1
İ						l		
						l		
						i		
B/- N	Input Loading					ļ		
Pin Name A	Factor (lu)					ł		
						l		
	Output Driving							
Pin Name X	Factor (lu)							
-								
		* Mini	mum val	ues for	the ty	pical c	perati	ng condition. g condition
		are	given b	y the m	aximum	delay m	ultipl	ier.
1								
l								
								Page 2-3
UHB-N2K-E2	Sheet 1/1							Page 2-3

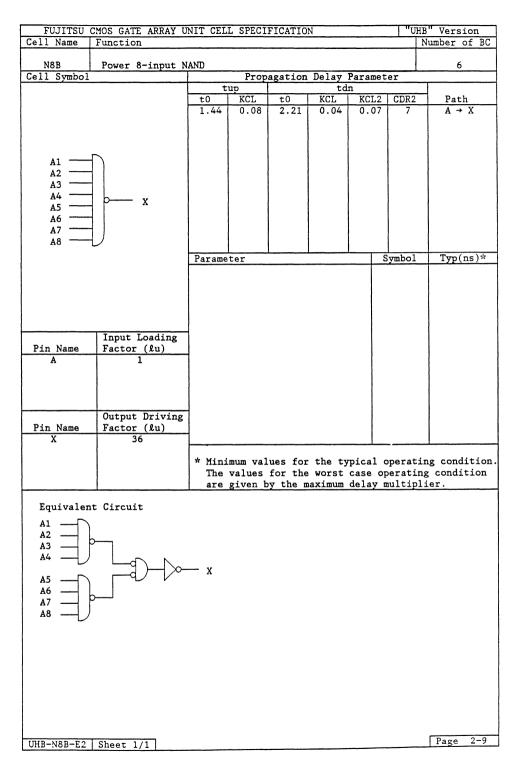
FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"บ	HB" Version
Cell Name	Function							Number of BC
N3N	3-input NAMD							,
Cell Symbol	3-input NAND		Prop	agation	Delav	Paramet	et.	2
2022 0,0001		t	up	-6001011	td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.52	0.16	0.69	0.19			Path A → X
	_							
A1								ļ
A2	р— х							
А3 —								
		Parame	ter			l s	ymbol	Typ(ns)*
						l		
*	Input Loading	1				-		
Pin Name	Factor (lu)							
A	1					- 1		
						- 1		
						- 1		
	Output Driving	1				- 1		}
Pin Name	Factor (lu)					1		
X	14							
				_				
		* Mini	mum vai	ues for	tne ty	picai c	perat	ting condition ing condition
		are	given b	v the m	aximum	delav n	ultit	olier.
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1								
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1								
UHB-N3N-E2	Sheet 1/1							Page 2-4

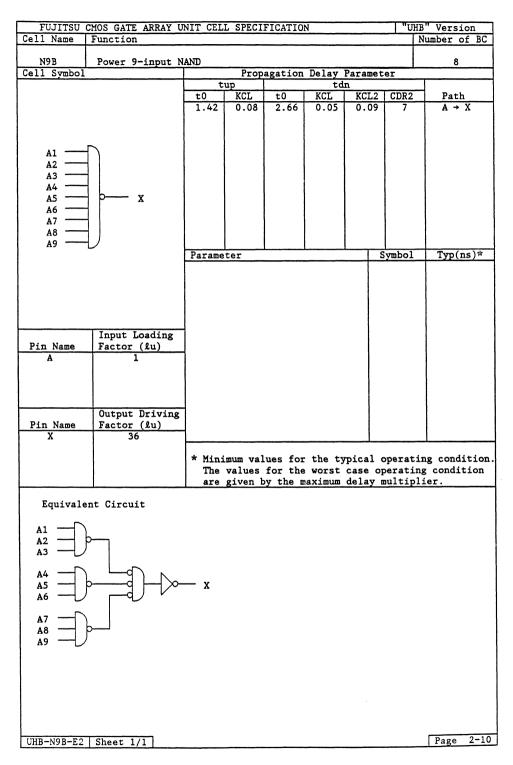
FILTER	CMOS GATE ARRAY U	NITT CEL	CDECT	ETCATTO	NT		i minu	B" Version
Cell Name	Function	HALL CEL	L SPECI	r ICALIO	IN		J UH	Number of BC
							<del></del>	
N3B	Power 3-input N	AND						3
Cell Symbol				agation	Delay	Paramet	er	
			up	+0	td KCL		CDDO	ا ۲۰۰۲
		t0 1.28	KCL 0.08	t0 1.70	0.04	KCL2	CDR2	Path A → X
		1.20	0.00	1.70	0.04			A - A
1								
								]
	$\sim$							
A1 ————————————————————————————————————	р— х						ŀ	1
A3	<b>↑</b>							
					1		[	
				l		L	<u></u>	<u> </u>
1		Parame	ter			<u>s</u>	ymbol	Typ(ns)*
						]		
1						1		
	Input Loading							
Pin Name	Factor (lu)							
A	1					- 1		
						1		
						1		1
						- 1		
	Output Driving					1		
Pin Name	Factor (lu)							
Х	36							1
l		* Mini	mum val	ues for	the tv	mical c	perati	ng condition.
		The	values	for the	worst	case or	eratin	g condition
		are	given b	y the m	aximum	delay n	ultipl	ier.
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UHB-N3B-E2	Sheet 1/1							Page 2-5

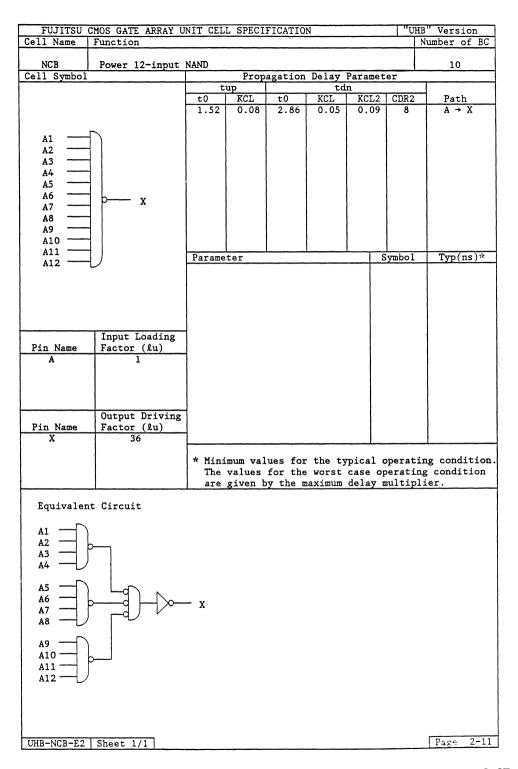
FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		יט"	HB" Versio	n
Cell Name	Function							Number of	BC
N4N	4-input NAND						1	2	
Cell Symbol				agation	Delay		er		
			up		td		0222		
		t0	KCL	t0	KCL	KCL2	CDR2	Path A → X	
		0.62	0.16	0.74	0.24			$A \rightarrow X$	
							1	I	
							İ	į.	
							1	1	
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							1	ı	
A1	$\cup$						1	İ	
A2	- I						1	į	
A3	р—— х						1		
A4	1)							l	
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		Dage			L	ــــــــــــــــــــــــــــــــــــــ	1 2	T (-	. 1 %
		Parame	Ler			<del>-   `</del>	Symbol	Typ(ns	·) "
								1	
								1	
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								1	
	Input Loading								
Pin Name	Factor (0.)					l			
A A	Factor (lu)					[		1	
А	1								
								1	
						1			
	Output Driving								
Pin Name	Factor ((u)								
X	Factor (lu)								
		* Mini	mum val	ues for	the tv	pical o	perat	ing condit	ion.
		The	values	for the	worst	case or	perati	ng conditi	ion
		are	given b	y the m	aximum	delav	nultip	lier.	
	·								
UHB-N4N-E2	Sheet 1/1							Page	2-6

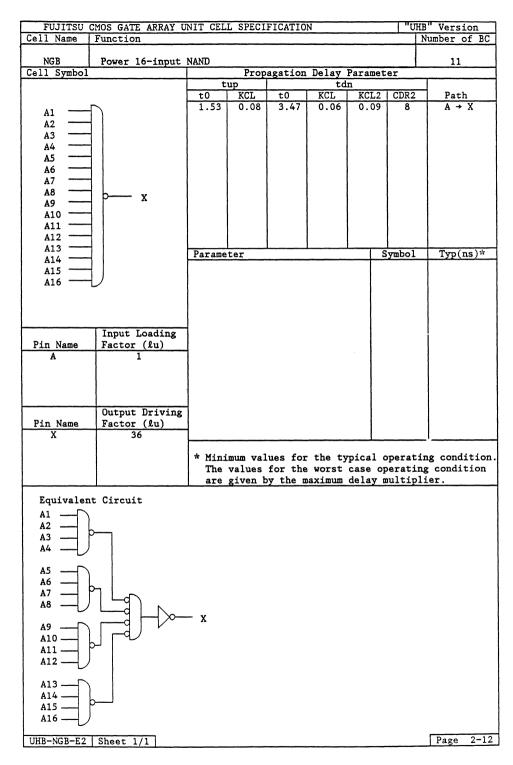
FUJITSU C	MOS GATE ARRAY U	VIT CELI	SPECI	FTCATTO	V		"UHB	" Version
	Function	000	011101	1011110			N	umber of BC
	· · · · · · · · · · · · · · · · · · ·							
N4B	Power 4-input N	AND						4
Cell Symbol				agation			er	,
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.38	0.08	1.90	0.04			A → X
			1					
ı						'		
A1								
A2	р—— x							
A3 ————————————————————————————————————	)							
A4 [								
							L	
		Parame	ter			S	ymbol	Typ(ns)*
	Input Loading							
Pin Name	Factor (lu)					1		
A	1							
						- 1		
	Output Driving							
Pin Name	Factor (lu)							
X	36							
		* Mini	mum val	ues for	the ty	mical c	perati	ng condition.
		The	values	for the	worst	case or	erating	condition
		are	given b	y the m	aximum	delay n	ultipl:	ler.
1								
UHB-N4B-E2	Sheet 1/1							Page 2-7

FULLTELL C	MOC CATTE ADDAY II	NITT CET	CDECT	CICATIO	NT		11777	HB" Version
	MOS GATE ARRAY U	NII CEL	L SPECI	FICALLO	N		1 01	Number of BC
N6B	Power 6-input N	AND						5
Cell Symbol				agation	Delay td		er	
		t0	up KCL	t0	KCL	KCL2	CDR2	Path
		1.37	0.08	2.02	0.04	0.07	7	A + X
1								
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l ,,	\							İ
A1 A2								1
A3	р—— х							
A4	^							
A5 —	)							
AO L							}	
		Parame					ymbol	Typ(ns)*
		rarame	rei				ушьот	1yp(ns)"
	Input Loading							
Pin Name	Factor (lu)							
A	1							
						l		
D. 17	Output Driving	1				i		
Pin Name X	Factor (lu)	1				Ì		
		<b></b>						
		* Mini	mum val	ues for	the ty	pical o	perat	ing condition.
ľ		The	values	for the	worst	case of	erati	ng condition
	<u> </u>	are	given b	y the m	aximum	delay i	nultip	lier.
Equivalent	Circuit							
_								
A1								
A2 — b								
		x						
A4								
A5   b								
A6 —								
UHB-N6B-E2	Sheet 1/1							Page 2-8









FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N .		"UH	IB" Vers	ion
Cell Name	Function	ction							
N3K	Power 3-input 1	NAND		1	3				
Cell Symbol			Prop	agation	Delay	Paramet	er		
		t t	up	+0	td		CDD2	- Part	_
		t0 0.48	KCL 0.07	t0 0.65	0.08	KCL2	CDR2	Pati A →	n X
		0.40	0.07	0.05	0.00			"	*
								1	
A1								1	ĺ
A2	р х							1	
A3								1	
		Parame	ter			S	ymbol	Typ(:	ns)*
						1		1	
		1							
						1		ļ	
		1				l		1	
Din Nama	Input Loading					l			
Pin Name A	Factor (lu)	1							
••	_	1				- 1			
		1							
		1				-			
	Output Driving	-				- 1			
Pin Name	Factor (lu)	İ				- 1			
Х	28	1							
		W Mama	1	6	44. 4	_4_1_			
		" Mini	mum vai values	ues ior for the	worst	picai o case on	perati eratir	ng cond	tion.
		are	given b	y the m	aximum	delay m	ultipl	ier.	
				<del></del>					
									j
HUD_NOV E4 T	Cheet 1/1							Desa	2_12
UHB-N3K-E1	Sheet 1/1							Page	2-13

FILTTCIL	CMOC CATE ADDAY I	NITT CEL	CDECT	ETCATTO	\T		11111	HB" Version
Cell Name	CMOS GATE ARRAY U Function	NII CEL	L SPECI	FICATIO	IN .		1 01	Number of BC
N4K	Power 4-input N	AND					i	4
Cell Symbol		ļ	Prop	agation	Delay td	Paramet	er	
		t0	up KCL	t0	KCL	KCL2	CDR2	Path
		0.56	0.07	0.76	0.10	NODE	ODINE	A + X
						ľ		
							l	
A1	$\Gamma$							
A2						İ		1
A3	р х							
A4	D					ļ		
						1		
		Parame	ter			<u>s</u>	ymbol	Typ(ns)*
	Input Loading	-				İ		
Pin Name	Factor (lu)							
A	2	1						
						1		
		1				1		
	Output Driving	1				ì		1
Pin Name	Factor (lu)	_				- 1		
Х	20			············				
		* Mini	m11m 17a1	ues for	the to	mical o	norat	ing condition
		The	values	for the	worst	case of	perati	ng condition
		are	given b	y the n	naximum	delay n	nultip	lier.
UHB-N4K-E1	Sheet 1/1							Page 2-14

## **NOR Family**

ı	Page	Unit Cell Name	Function	Basic Cells
:	2-33	R2N	2-input NOR	1
2	2–34	R2B	Power 2-input NOR	3
2	2–35	R2K	Power 2-input NOR	2
2	2–36	R3N	3-input NOR	2
2	2–37	R3B	Power 3-input NOR	3
:	2–38	R4N	4-input NOR	2
:	2–39	R4B	Power 4-input NOR	4
:	2-40	R6B	Power 6-input NOR	5
2	2-41	R8B	Power 8-input NOR	6
2	2-42	R9B	Power 9-input NOR	8
:	2-43	RCB	Power 12-input NOR	10
:	2-44	RGB	Power 16-input NOR	11
2	2–45	R3K	Power 3-input NOR	3
:	2-46	R4K	Power 4-input NOR	4

FULLTSU (	CMOS GATE ARRAY U	NIT CELI	. SPECT	FICATIO	N		ווויי ו	B" Version
Cell Name	Function	WII OBD	D DI LOI.	TOATIO			1	Number of BC
	0 1 1700							
R2N Cell Symbol	2-input NOR		Prop	agation	Delay	Parame+	er	1
OCII DYMBOI		tı	up	agacion	td	n	<u></u>	T
		t0	KCL	t0	KCL	KCL2		Path
		0.40	0.29	0.44	0.08	0.11	4	A -> X
	_							
A1	x						1	
A2							]	
							]	
		Parame	ter		L	S	ymbol	Typ(ns)*
	<del></del>							
Pin Name	Input Loading Factor (lu)							
A	1							
	Output Driving							
Pin Name	Factor (lu)							
Х	14							
		* Mini	mum wal	ues for	the to	mical o	perati	ing condition.
		The	values	for the	worst	case op	erati	ng condition
	<u> </u>	are	given b	y the m	naximum	delay m	ultip	lier.
1								
1								
1								
								_
UHB-R2N-E2	Sheet 1/1							Page 3-1

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		ויי" וו	B" Version
Cell Name	Function			Number of BC				
R2B	Power 2-input N	OR						3
Cell Symbol			Prop	agation	Delay	Paramet	er	
		t0	up KCL	t0	td KCL	KCL2	CDR2	Path
		1.36	0.08	1.25	0.04			A -> X
	_							
A1 A2	x							
AZ [								
	:						<u> </u>	
	,	Parame	ter			S	ymbol	Typ(ns)*
	Input Loading					l		
Pin Name A	Factor (lu)							
	1					1		
	Output Driving							
Pin Name	Factor (lu)							
X	36	<u> </u>						
		* Mini	mum val	ues for	the ty	pical c	perati	ng condition.
		The	values	for the	worst	case or	eratin	ng condition
		are	given t	y the m	aximum	delay n	mitibi	.ier.
UHB-R2B-E2	Chart 1/1							Page 3-2
UND-KZB-EZ	Sheet 1/1							1 2 2 2

FUJITSU CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UHF	" Version
Cell Name   Function	JIVII ODD	D DIBOI	11011110				Number of BC
	ion						
R2K Power 2-input N	NOR	Pron	agation	Delay	Paramet		2
Cell Symbol	<del>                                     </del>	up	agation	td		<u>e1</u>	<del>,</del> -
	t0	KCL	t0	KCL	KCL2	CDR2	Path A → X
	0.45	0.14	0.45	0.06			A → X
							1
	I	1					
A1 X							1
A2							
							}
	Parame	ter			1 5	ymbol	Typ(ns)*
	101000					,	1 2) (1.2)
					Ì		
					ĺ		
					1		
					1		
Input Loading	1				1		
Pin Name Factor (lu)	4						
A 2					- 1		
					1		
	4				l		
Output Driving					1		
Pin Name Factor (Lu) X 36	-				1		
	* Mini	mum val	ues for	the ty	pical c	perati	ng condition.
	The	values	for the	worst aximum	delaw m	erating	condition
	are	given b	y the u	aximum	deray ii	urcipi.	.er.
UHB-R2K-E2   Sheet 1/1							Page 3-3

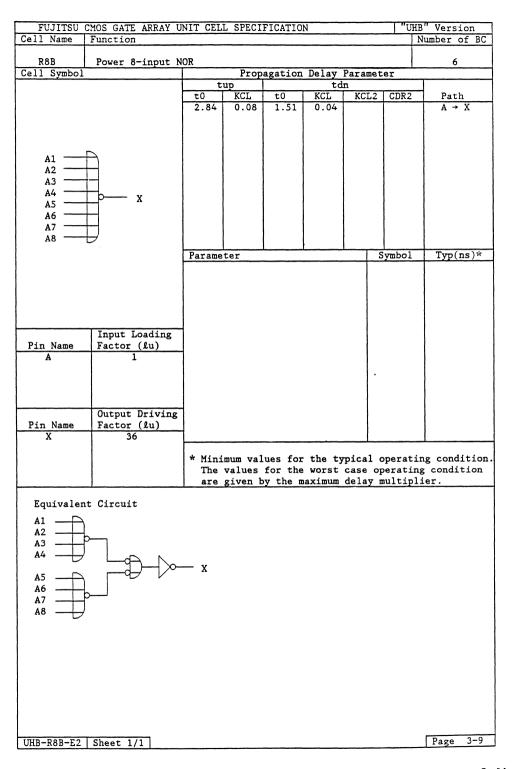
FILITTCII	CMOS GATE ARRAY U	NIT CET	I. SPECT	FICATIO	N		TITTE I	HB" Version
	Function	055	01101	_ 10A110	.,		1 1	Number of BC
Hamo								
R3N	3-input NOR							2
Cell Symbol				agation	Delay	Paramet	er	
			up		td			┥
		t0	KCL 0.41	t0	KCL	KCL2	CDR2	$\begin{array}{c c} & \text{Path} \\ \hline & A \rightarrow X \end{array}$
		0.84	0.41	0.46	0.09	0.12	4	$A \rightarrow X$
							ł	
								1
							1	
	_						l	
A1	A							
A2	<del>р х</del>						1	
A3	$\forall$							1
							1	
		Parame	ter	L	L	٠	ymbol	Typ(ns)*
		rarame	267			-+-	, m.o.i	1,5(113)
						1		1
						1		
								1
	<del></del>							1
Dia Nama	Input Loading					1		
Pin Name A	Factor (lu)					1		
A .	1					1		
						l		
						- 1		
						1		
	Output Driving					1		
Pin Name	Factor (lu)					1		
Х	10							
1								
		" Mini	mum val	ues IOI.	the ty	bicai o	perat	ing condition ng condition
		are	values	y the m	aximum	delay r	multin	lier.
l		416	02.011	., UILC II				
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1								
1								
UHB-R3N-E2	Sheet 1/1							Page 3-4

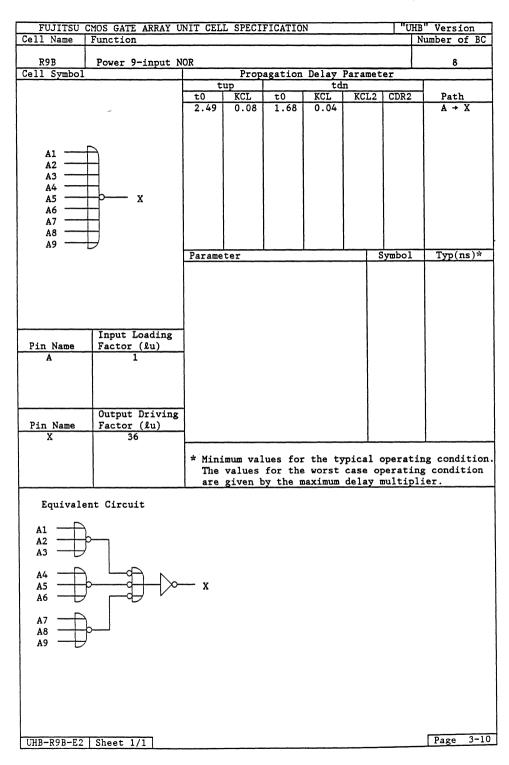
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version  R3B	f BC
Propagation Delay Parameter   tup   tdn	
Propagation Delay Parameter   tup   tdn	
tup tdn t0 KCL t0 KCL KCL2 CDR2 Path 1.99 0.08 1.37 0.04 A →	
t0 KCL t0 KCL KCL2 CDR2 Path 1.99 0.08 1.37 0.04 A →  A1 A2 X	
A1 X	
A2 — + > — X	x j
A2 — + > — X	
A2 — + > — X	
A2 — + > — X	
A2 — + > — X	
A2 — + > — X	1
	1
A3 <del>-    </del>	
Parameter Symbol Typ(n	s)*
1 Julio 1 1) P(1	
	-
Input Loading	
Pin Name Factor (lu)	
A 1	
Output Driving Pin Name Factor (lu)	
X 36	
* Minimum values for the typical operating condi	tion.
are given by the maximum delay multiplier.	1011
dio giron by one manage costs, manage	
	<del></del>
UHB-R3B-E2   Sheet 1/1   Page	3-5

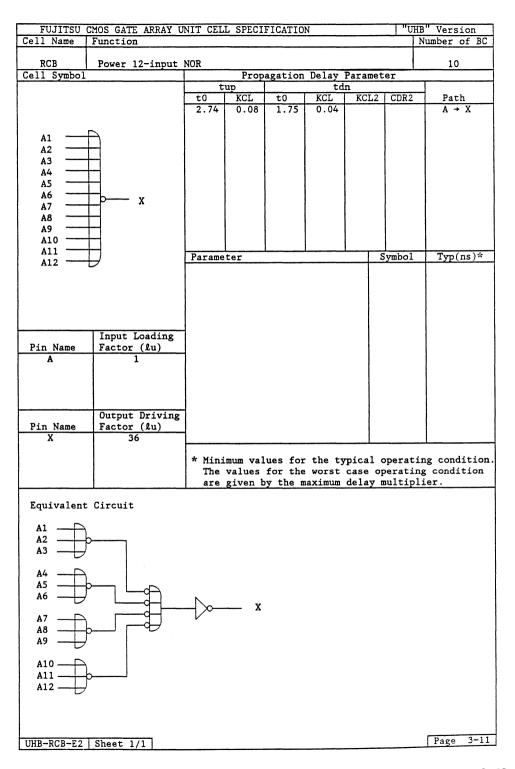
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Versi							B" Version	
Cell Name Function						Number of BC		
R4N	4-input NOR						1	2
Cell Symbol	22,500	Propagation Delay Parameter						
			up		td	n		J
		t0 1.24	KCL 0.54	t0 0.46	0.09	KCL2 0.13	CDR2	Path A → X
		1.24	0.34	0.46	0.09	0.13	4	A 7 X
	_							
A1 -	$\Box$							
A2 ————————————————————————————————————	>— х							
A4	$\vdash$							
		Parame	ter			S	ymbol	Typ(ns)*
D/- M	Input Loading	Ì						
Pin Name A	Factor (lu)							
••	1							
	1	1						
		}						
	Output Driving	}						
Pin Name	Factor (lu)							
X	6							
		J. 14						
		* Minimum values for the typical operating condition  The values for the worst case operating condition						
		are given by the maximum delay multiplier.						
and Server of one mentales done, server								
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IND-DAN ES	Chart 1/1							Page 3-6
UHB-R4N-E2	Sheet 1/1							rage 3-0

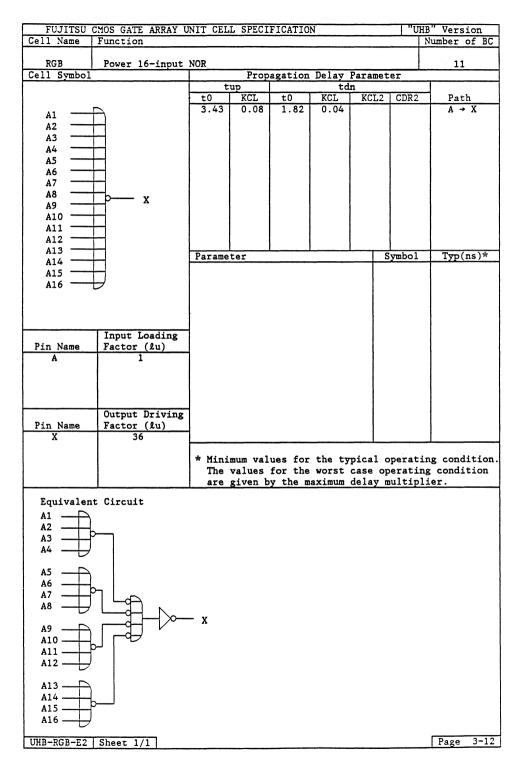
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FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "U Cell Name   Function							1 01	HB" Version Number of H	3C
									-
R4B	Power 4-input N							4	
Cell Symbol Propagation Delay Parameter									_
		t0	up KCL	t0	KCL KCL	KCL2	CDR2	Path	
		2.50	0.08	1.34	0.04			A + X	$\neg$
									- 1
								ĺ	l
									l
								l	l
A1 ——	7								
A2 -	х			'					1
A3	<b>→</b> ^								
A4 —	プ	i i							
		Parame	tor	L	اـــــا	1 8	ymbol	Typ(ns)	*
		1 at aute					,	1,50(113)	$\neg$
						ļ			- 1
		1				İ			
	Input Loading	1				ļ			
Pin Name	Factor (lu)	1				1			1
A	1								1
	-								l
						1		}	
		1							
Pin Name	Output Driving Factor (lu)							-	
X	36	1				İ		1	ł
			_	_	_				
	* Minimum values for the typical operating condition							on.	
	The values for the worst case operating condition are given by the maximum delay multiplier.							"	
are given by the maximum delay multiplier.									
									l
								Page 3-	.7
UHB-R4B-E2	Sheet 1/1							rage 5	

FULTTELL	MOC CATT ADDAY II	NITT CEL	T CDECT	ETCATTO	NT		1111	HB" Version
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "U Cell Name   Function							Number of BC	
R6B Cell Symbol	R6B Power 6-input NOR 5 Cell Symbol Propagation Delay Parameter							
tup tdn								
		t0	KCL	t0	KCL	KCL2	CDR2	
		2.25	0.08	1.48	0.04			A → X
								ļ
A1	7							
A2 -								
A3 ————————————————————————————————————	x							
A5 -	_							
A6 —	eg							
		Parame	ter				ymbo1	Typ(ns)*
ļ	Input Loading	ł						:
Pin Name	Factor (lu)	ļ						
A	1	1						
						l		
						1		
	Output Driving	1				ĺ		
Pin Name	Factor (lu)	1				Ì		
Х	36							
		* Mini	mum val	ues for	the ty	pical o	perat	ing condition.
* Minimum values for the typical operating condition The values for the worst case operating condition								ng condition
are given by the maximum delay multiplier.								lier.
Equivalent Circuit								
A1 —								
A2 ————————————————————————————————————								
A3 —	<u></u>	х						
A4 —								
A5	<b></b>							
A6 —								
UHB-R6B-E2	Sheet 1/1							Page 3-8









FULLTSU	CMOS GATE APPAY II	NIT CEL	I SPECT	FICATIO	N		77177	HB" Version
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " Cell Name   Function								Number of BC
R3K Cell Symbol	Power 3-input N	OR	D	+	Delay	Damamat		3
Cell Symbol		t	up	agation	td		.er	T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.66	0.17	0.32	0.04	0.07	7	A → X
							1	1
								1
	<u> </u>					ł	l	
A1 ————————————————————————————————————	x					l		1 1
A3	· •							1
	_							1
ļ							l	1 1
		Parame	ter	L	<u> </u>	L	ymbol	Typ(ns)*
		Turume					ушьст	1,1,0(115)
						}		
								1
	Input Loading	1				ļ		1 1
Pin Name	Factor (lu)					l		1
A	2					ŀ		
						i		
	Ì					1		
Din Nama	Output Driving Factor (lu)	1						
Pin Name X	20	1				l		
		* Mini	mum val	ues for	the ty	pical o	perat	ing condition.
		The	values	for the	worst maximum	case or	perati:	ng condition
	1	are	given c	y the m	iaximum	delay i	nuitip	lier.
1								
1								
UHB-R3K-E1	Sheet 1/1							Page 3-13

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UH	B" Version
Cell Name	Function							Number of BC
								,
R4K	Power 4-input N	UR	P		Do 1	Dama		4
Cell Symbol		+-	up Prop	agation	Delay td		eI	1
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.08	0.23	0.35	0.03	0.05	7	Path A → X
	:							
								1
	_							
A1	A I							
A2	х							
A3	<b>├</b>							
A4	$\forall$							1
								1
		Parame	ter			S	ymbol	Typ(ns)*
							· ·	
1						1		
						1		
						- 1		
	Input Loading							
Pin Name	Factor (lu)							
Α .	2							
						Ì		
	Output Driving	1				l		
Pin Name	Factor (lu)							
X	12	ĺ				l		
			***************************************					
		* Mini	mum val	ues for	the ty	pical c	perati	ing condition.
		The	values	for the	worst	case or	eratir	ng condition
		are	given b	y the m	aximum	delay n	ultip	lier.
1								
1								
UHB-R4K-E1	Sheet 1/1							Page 3-14

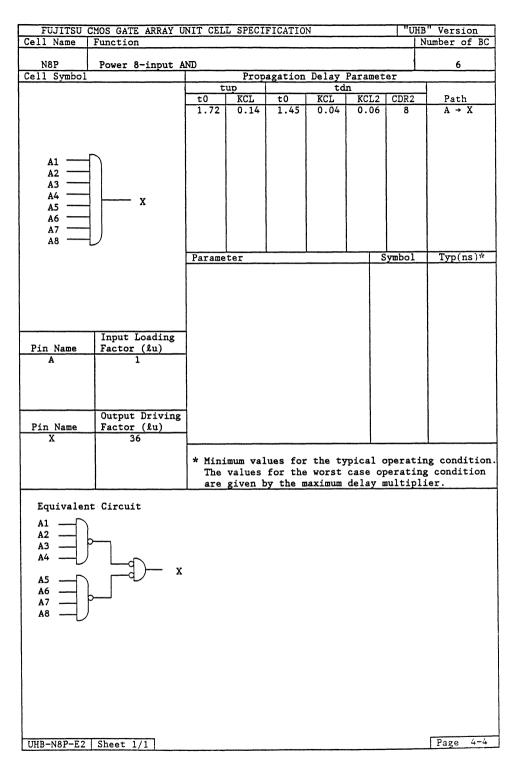
# **AND Family**

	Unit Cell		Basic
Page	Name	Function	Cells
2-49	N2P	Power 2-input AND	2
2-50	N3P	Power 3-input AND	3
2-51	N4P	Power 4-input AND	3
2-52	N8P	Power 8-input AND	6

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UH	B" Version
	Function						1	Number of BC
N2P	Davier 2-innut A	MTN					- 1	,
Cell Symbol	Power 2-input A	ND	Prop	agation	Delay	Paramet	er	2
		t	up	-8	td			T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.01	0.08	0.86	0.04	0.06	7	A + X
								1
						1		1
A1 ——						,		
A2	)— x							j
_								
								1
		Parame	ter			S	ymbol	Typ(ns)*
						-		
						1		
								1
	Input Loading							
Pin Name A	Factor (lu)					1		
A	1							
						1		
	Output Driving							
Pin Name X	Factor (lu)							
Α,	50			····				
		* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
		The	values	for the	worst	case op	eratin	g condition
		are	given b	y the m	aximum	delay m	ultipl	ier.
								1
UHB-N2P-E2	Sheet 1/1							Page 4-1

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		ט" וו	HB" Version
Cell Name	Function							Number of BC
N3P Cell Symbol	Power 3-input A	ND	Dron	agation	Dolor	Daramat		3
Cell Symbol		t	up	agation	td		er	T
		t0	KCL	t0	KCL	KCL2	CDR2	
		1.32	0.08	1.07	0.04	0.06	7	A - X
A1	)							
A2	x							
A3 ——								
		Parame	ter			S	ymbol	Typ(ns)*
						1		
	Input Loading							
Pin Name	Factor (lu)					İ		
A	1							
						- 1		1
	Output Driving							
Pin Name X	Factor (lu)							1
			<del></del>					
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
		The	values	for the by the m	worst	case or	erati 111111	ng condition
	L	are	given L	y the n	IAXIIIUIII	deray u	urcip	TIEL,
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1								
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1								
UHB-N3P-E2	Sheet 1/1							Page 4-2

דווודפוו כ	MOS GATE ARRAY U	NIT CEL	I. SPECT	FICATIO	N		"ITHE	" Version
Cell Name	Function	WII CED.	D BLECT	FICALLO	IN .		I N	umber of BC
N4P	Power 4-input A	ND						3
Cell Symbol			up Prop	agation	Delay td	Paramet	er	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.58	0.08	1.19	0.04	0.06	8	Path A → X
								1
٨,								
A1 ————————————————————————————————————								
A3	х							
A4	)							
		Parame	ter			S	ymbol	Typ(ns)*
1						1		
						ļ		] ]
								1
						1		1
Pin Name	Input Loading Factor (lu)					Į		
A A	1					1		1 1
-	-					1		
						1		1
	Output Driving							
Pin Name	Factor (lu)							1
X	36							1
		* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
		are	values given h	ror the m	aximum	delay m	erating ultipli	er.
			821011	<u>, , , , , , , , , , , , , , , , , , , </u>				
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UHB-N4P-E2	Sheet 1/1							Page 4-3



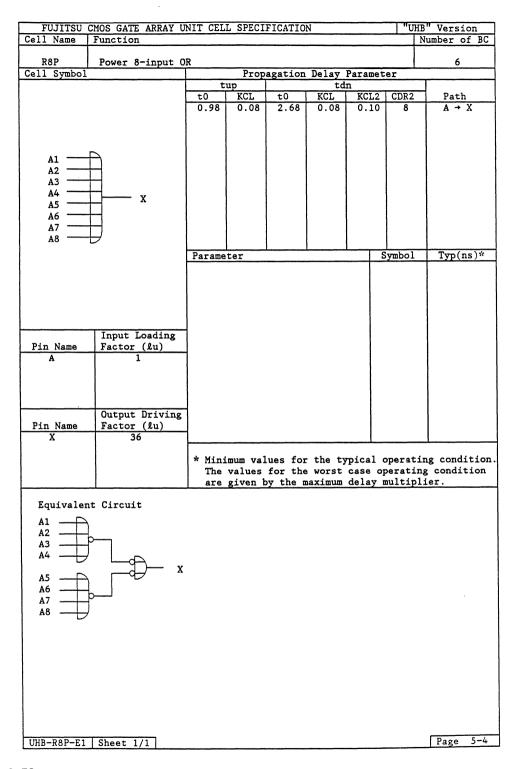
### **OR Family**

Page	Unit Cell Name	Function	Basic Cells
2–55	R2P	Power 2-input OR	2
2–56	R3P	Power 3-input OR	3
2–57	R4P	Power 4-input OR	3
2-58	R8P	Power 8-input OR	6

FUJITSU C	MOS GATE ARRAY U	VIT CEL	L SPECI	FICATIO	N		"UH	B" Versio	on
Cell Name	Function							Number o	f BC
R2P	Power 2-input 0	R						2	
Cell Symbol				agation	Delay	Paramet	er		
			up		td			┙	I
		t0	KCL	t0	KCL	KCL2	CDR2	Path	
		0.78	0.08	1.14	0.05	0.07	8	A → 3	X
		ļ							1
								1	- 1
		ĺ						1	1
								}	
A1 ——	$\rightarrow$								- 1
A2 -	_) <del></del> x							1	
AZ L								1	- 1
								1	
									]
		Parame	ter			S	ymbol	Typ(n	s)*
						T			
						ļ			
	Input Loading								
Pin Name	Factor (lu)								
A	1					1		1	
						1		1	
						1			
	Output Driving					- [		1	
Pin Name	Factor (lu)					- 1		i	
X	36								
		* Mini	mum val	ues for	the ty	pical c	perati	ing condi	tion.
		The	values	for the	worst	case op	erati	ng condit	ion
		are	given b	y the m	aximum	delay m	ultip	lier.	
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UHB-R2P-E2	Sheet 1/1							Page	5-1

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		<b>"</b> UI	HB" Version Number of BC	
Cell Name	Function	rion N							
R3P	Power 3-input 0	R		<del></del>				3	
Cell Symbol		+-	Prop up	agation	Delay td		er		
		t0	KCL	t0	KCL	KCL2	CDR2	Path	
		0.90	0.08	1.84	0.06	0.08	8	A → X	
A1	A								
A2 —— A3 ——	x								
AS									
		Parame	ter	L		l s	ymbol	Typ(ns)*	
	Input Loading								
Pin Name	Factor (lu)					- 1			
A	1								
	Output Driving					İ			
Pin Name	Factor (lu)								
Х	36								
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.	
		The	values	for the	worst	case or	erati	ng condition	
		ı are	given b	y the m	naximum	deray I	urcip	1161.	
1									
UHB-R3P-E2	Sheet 1/1							Page 5-2	

Ellitzell c	WOO CATE ADDAY II	NITT CET	CDECT	PTCATTO	NT.		117777	n" v
Cell Name	MOS GATE ARRAY U	MII CEL	L STEUL	L TCALLO	LN .		I UH	B" Version Number of BC
R4P	Power 4-input 0	R						3
Cell Symbol				agation	Delay		er	
			up VCT	+0 1	KCL KCL	n KCL2	CDR2	I
1		t0 0.90	KCL 0.08	t0 2.52	0.07	0.10	8 8	$\begin{array}{c c} Path \\ A \rightarrow X \end{array}$
		0.50	0.00	2.32	0.07	0.10	0	A T A
Ì								
				ĺ				1
A1 -	$\rightarrow$							
A2 -	x							1
A3								
A4 ——	7							1
		Don	<u></u>				ymbol	Type(no)*
		Parame	rer				ушрот	Typ(ns)*
						- 1		
						}		
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Pin Name	Input Loading Factor (lu)					1		
A A	ractor (xu)							
	•					l		
						i		
						j		
Pin Name	Output Driving Factor (lu)					1		
X	36					1		
		* Mini	mum val	ues for	the ty	pical o	perati	ing condition.
}		The	values	for the	worst	case op	erati	ng condition
	<u></u>	are	given b	y the m	aximum	delay m	ultip.	ier.
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UHB-R4P-E2	Sheet 1/1							Page 5-3
011D K-1 E2	Direct 1/1							



### **EXNOR/EXOR Family**

Page	Unit Celi Name	Function	Basic Cells
2–61	X1N	Exclusive NOR	3
2-62	X1B	Power Exclusive NOR	4
2-63	X2N	Exclusive OR	3
2-64	X2B	Power Exclusive OR	4
2–65	X3N	3-input Exclusive NOR	5
2–66	ХЗВ	Power 3-input Exclusive NOR	6
2–67	X4N	3-input Exclusive OR	5
2-68	X4B	Power 3-input Exclusive OR	6

	CMOS GATE ARRAY U Function	NIT CEL	L SPECI	FICATIO	N		<u>  "U</u>	HB" Version Number of BC
CEII Name	ranceron							TITILDET OF BC
X1N	Exclusive NOR							3
Cell Symbol			Prop	agation			er	
			up		td		anna	→ , ,
İ		t0 1.16	KCL 0.29	t0 0.96	KCL 0.13	KCL2 0.16	CDR2	$\begin{array}{ c c } \hline Path \\ \hline A \rightarrow X \\ \hline \end{array}$
		1.16	0.29	0.36	0.13	0.16	•	A - A
								1
49 (								
A1 —	о— х							
A2								
1		Parame	ter		L	l s	ymbol	Typ(ns)*
						- [		
						-		
1						1		
	Input Loading					1		
Pin Name	Factor (lu)					1		
A	2					l		
	Output Driving							
Pin Name	Factor (lu)							
Х	18							
		* Mini	mum val	nes for	the tv	mical o	nerat	ing condition.
		The	values	for the	worst	case or	erati	ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.
P 1	<b>•</b> Cimenic							
Equivalen	t Circuit							
A1	\.							
A2 -	ρ	_						
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		ノ	Λ.					
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UHB-X1N-E2	Sheet 1/1							Page 6-1
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								- w	
FUJITSU Cell Name	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UHI	B" Versi Number o	on of RC
COLL NAME								···	2 20
X1B	Power Exclusive	NOR					1_	4	
Cell Symbol				agation			er	<del></del>	
			up		td		CDDO	٠	_
		t0	KCL	t0	KCL	KCL2	CDR2	Path A →	1
		1.49	0.08	1.77	0.05	0.09	7	A →	Х
								1	
								1	
	(								
A1	x							1	
A2 -	<del>'</del>			1				1	
								1	
		Parame	ter			T S	ymbol	Typ(I	ns)*
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						ŀ		1	
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								1	
	Input Loading								
Pin Name	Factor (lu)					1			
A	2					1		1	
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						- 1			
	<b>-</b>					- 1		l	
Din Mana	Output Driving							}	
Pin Name X	Factor (lu)	}				l		İ	
^	30							_1	
		* Mini	mum v21	nes for	the tu	mical c	perati	ng cond	ition.
	1	The	values	for the	worst	case or	eratin	g condi	tion
	}	are	given b	v the m	aximum	delav n	ultipl	ier.	<b></b>
1									
Equivaler	nt Circuit								
_									
A1	¬`p								
A2 -	ブ <u> </u>	<u> </u>							
		p(`	>	X					
ĺ									
}									
1									
1									
UHB-X1B-E2	Sheet 1/1							Page	6-2

FILTTSII	CMOS GATE ARRAY U	NIT CEL	L SPECT	FICATIO	Ŋ		11111	IB" Version
	Function	TAL OBL		LUNITU			1 1	Number of BC
X2N	Exclusive OR							3
Cell Symbol				agation			er	
			up		td		anna.	⊣ ,
		t0	KCL	t0	KCL	KCL2	CDR2	Path A → X
		1.11	0.29	1.17	0.13	0.16	4	$A \rightarrow X$
								į į
A1 —	A							
A2	x						l	j
'								
							}	
		Parame	ter		L	1 8	ymbol	Typ(ns)*
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	I Tanna Tandina							1
Pin Name	Input Loading							
A A	Factor (lu)							
••	_	i						
						1		
		}						
	Output Driving							
Pin Name	Factor (lu)	1						
X	14							
		* Mini	mum 1721	ues for	the to	nical c	nerat	ing condition.
		The	values	for the	worst	case or	erati	ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.
	· · · · · · · · · · · · · · · · · · ·	·						
Equivalen	t Circuit							
A1 —	_							
A1 A2	<u>}</u> >────							
1 17-	´ L	<b>A</b> .						
			— x					
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UHB-X2N-E2	Sheet 1/1							Page 6-3
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TUTTENT!	THE PART AND AND AND AND AND AND AND AND AND AND	NITT CEL	T CDECT	TTCATTO	NT		11777	011 17	
Cell Name	CMOS GATE ARRAY U Function	NII CEL	L SPECI	FICATIO.	N		I UH.	B" Versi Number c	on F BC
JOIL Hame	1 011001011							, amber C	- 110
X2B	Power Exclusive	OR						4	
Cell Symbol				agation			er	<del></del>	
		t0	up KCL	t0	KCL KCL	n KCL2	CDR2	Path	,
		1.43	0.08	1.64	0.05	0.07	7	A →	
					'				
								}	
A1									
A1 —	х								
AZ I									
								1	
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		Parame	ter			l s	ymbol	Typ(r	ıs)*
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}									
	Input Loading	İ				-			
Pin Name	Factor (lu)					ł		ĺ	
A	2					ļ			
İ		}				1			
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						ĺ			
	Output Driving	1				1			
Pin Name	Factor (lu)	]				1			
Х	36								
		* Mini	mum val	ues for	the to	mical o	nerati	ng cond:	ition
		The	values	for the	worst	case or	eratin	g condi	tion
		are	given b	y the m	naximum	delay n	ultipl	ier.	
Equivalen	+ Circuit								
Equivalen	C CITCUIT								
A1 -	b								
A2 -									
1   L	<u> </u>	) ) <del></del> -(	>	X					
L									
	J								
UHB-X2B-E2	Sheet 1/1							Page	6-4

FULTEU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		T "TIH	B" Version
	Function	WII ODD		1011110	<u> </u>		1	Number of BC
Vari	3 F 1: :	NOD				-		-
X3N Cell Symbol	3-input Exclusi	ve NUK	Prop	agation	Delay	Paramet	er l	5
GOII DYMEOI		t	up	28001011	td	n	<u> </u>	T
		t0	KCL	t0	KCL	KCL2		Path
		2.72	0.29	2.32	0.13	0.16	4	A - X
A1 ———	7							
A1 A2	-b x					i		
A3	<del>-</del>							
		Parame	ter				ymbol	Typ(ns)*
<u> </u>		1 arame					, m. O 1	1,50(113)
Ì						1		
	Input Loading							
Pin Name	Factor (lu)					]		
A	2							
		1				- 1		
Dia Nama	Output Driving							
Pin Name X	Factor (lu)	{						
	10							_1
		* Mini	mum val	ues for	the ty	pical c	perati	ng condition.
		The	values	for the	worst	case op	eratin	g condition
ļ	l	are	given b	y the m	aximum	delay m	ultipl	ier.
Equivalent	Circuit							
A2 1								
A3	٦							
	х							
A1	IU							
}								
UHB-X3N-E2	Sheet 1/1							Page 6-5

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UHB	" Versi	on
	Function						N	umber c	f BC
хзв	Power 3-input E	vo luodes	ם אוחים					6	
Cell Symbol	rower 3-input L	ACTUSIVO	Prop	agation	Delav	Paramet	er	6	
		tı	up	3	td		- <del></del>		
		t0	KCL	t0	KCL	KCL2	CDR2	Path	
		2.64	0.08	3.39	0.05	0.09	7	A →	X
A1	7							1	
A2	x								
A3 —	7								
							l		
		Parame	ter		L	S	ymbol	Typ(r	ıs)*
								1	
	Input Loading								
Pin Name	Factor (lu)					ļ			
A	2								
						1			
						1			
	Output Driving					1		1	
Pin Name	Factor (lu)								
Х	36								
			_	_					
		* Mini	mum val	ues for	the ty	pical o	perati	ng cond:	ition
		ine	values	for the	e WOIST	delay n	miltinl	ier.	LION
<b> </b>		are	PTACH F	, one ii	· · · · · · · · · · · · · · · · · · ·	coray i			
Equivalent	t Circuit								
A2	<del>_</del>								
A3 ————————————————————————————————————	J LIA NA	х							
A1	+	х							
	, <u> </u>								
1									
1									
UHB-X3B-E2	Sheet 1/1							Page	6-6

DUITE CO	MOG GARTE ADDAM II	NITE OF L	CDECT	DIGATIO	.7		11777	WD 11 W
	MOS GATE ARRAY U	NII CEL	SPECI.	FICATIO	N		1 01	HB" Version Number of BC
X4N	3-input Exclusi	ve OR					1	5
Cell Symbol		+:	up Prop	agation	Delay		er	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.82	0.29	2.53	0.13	0.16	4	A → X
								1
A1	$\rightarrow$							
A2	<del>  x</del>							
A3	7							
							L	
		Parame	ter			s	ymbol	Typ(ns)*
						1		
	Input Loading					1		
Pin Name	Factor (lu)							
A	2	<u> </u>				- 1		
		Ì						
ļ	Output Driving	}						
Pin Name	Factor (lu)							
Х	14							
		* Mini	mum val	ues for	the ty	mical c	perat	ing condition.
		The	values	for the	worst	case or	erati	ng condition
	<u> </u>	are	given b	y the m	aximum	delay m	ultip	lier.
Equivalent	Circuit							
Pderagent	. 0110010							
A2 -								
A3 -	٦							
	Щ							
A1	x							
, n								
1								
}								
UHB-X4N-E2	Sheet 1/1							Page 6-7
3	2	·						

Robert   Symbol   S	FUJITSU C	CMOS GATE ARRAY U	NIT CEL	"Uī	HB" Version Number of BC				
Propagation Delay Parameter  tup tdn  to KCL to KCL CDR2  Path  2.47 0.08 3.13 0.05 0.07 7 A + X  Parameter Symbol Typ(ns)*  Parameter Symbol Typ(ns)*  Parameter Symbol Typ(ns)*  Pin Name Input Loading Factor (£u)  A 2  Pin Name Factor (£u)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2  A3			xclusive	e OR					
To KCL to KCL CDR2 Path  2.47 0.08 3.13 0.05 0.07 7 A + X  Parameter Symbol Typ(ns)*  Parameter Symbol Typ(ns)*  Pin Name Factor (£u)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2  A3				Prop	agation	Delay	Paramet	er	
Pin Name   Input Loading   Factor (£u)    Pin Name   Factor (£u)    A   36    * Minimum values for the typical operating condition   The values for the worst case operating condition   are given by the maximum delay multiplier.								0220	_
Parameter  Parameter  Symbol Typ(ns)*  Parameter  Symbol Typ(ns)*  Pin Name Factor (£u)  A 2  Pin Name Factor (£u)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2  A3									Path
Parameter  Parameter  Symbol Typ(ns)*  Pin Name Factor (£u)  A  Output Driving  Pin Name Factor (£u)  X  Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2  A3  X			2.4/	0.08	3.13	0.05	0.07	<b>'</b>	$A \rightarrow X$
Parameter  Parameter  Symbol Typ(ns)*  Pin Name Factor (£u)  A  Output Driving  Pin Name Factor (£u)  X  Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2  A3  X									1
Parameter  Parameter  Symbol Typ(ns)*  Pin Name Factor (£u)  A  Output Driving  Pin Name Factor (£u)  X  Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2  A3  X									
Parameter  Parameter  Symbol Typ(ns)*  Pin Name Factor (£u)  A  Output Driving  Pin Name Factor (£u)  X  Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2  A3  X									
Parameter  Parameter  Symbol Typ(ns)*  Pin Name Factor (£u)  A  Output Driving  Pin Name Factor (£u)  X  Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2  A3  X									
Parameter  Parameter  Symbol Typ(ns)*  Pin Name Factor (£u)  A  Output Driving  Pin Name Factor (£u)  X  Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2  A3  X		_							
Parameter Symbol Typ(ns)*  Parameter Symbol Typ(ns)*  Pin Name Factor (£u)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2  A3		$\rightarrow$							
Pin Name   Input Loading   Factor (£u)		x						1	
Pin Name Factor (£u)  A 2  Pin Name Factor (£u)  Y 36  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2  A3	A3 —	7							
Pin Name Factor (£u)  A 2  Pin Name Factor (£u)  Y 36  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2  A3									
Pin Name Factor (£u)  A 2  Pin Name Factor (£u)  Y 36  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2  A3									
Pin Name Factor (£u)  A 2  Pin Name Factor (£u)  Y 36  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2  A3			Parame	ter	أحصنبا		l s	vmbol	Typ(ns)*
Pin Name Factor (fu)  A 2  Pin Name Output Driving Factor (fu)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2  A3  X				·					
Pin Name Factor (fu)  A 2  Pin Name Output Driving Factor (fu)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2  A3  X									
Pin Name Factor (fu)  A 2  Pin Name Output Driving Factor (fu)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2  A3  X									1
Pin Name Factor (fu)  A 2  Pin Name Output Driving Factor (fu)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2  A3  X		,							
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Pin Name Factor (fu)  A 2  Pin Name Output Driving Factor (fu)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2  A3  X		Tanua Tandini					l		1
Pin Name Output Driving Factor (Lu)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2  A3  X	Pin Name	Factor (0)							
Pin Name Factor (£u)  X  36  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2  A3  X							1		
Pin Name Factor (£u)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2 A3  X							1		1
Pin Name Factor (£u)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2 A3  X									
Pin Name Factor (£u)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2 A3  X									
Pin Name Factor (£u)  X 36  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2  A3  X		0					l		
* Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2 A3	Pin Name	Factor (811)							
* Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2 A3  X	X		1				1		
The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A2  A3					·····				
Equivalent Circuit  A2 A3  X			* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
Equivalent Circuit  A2 A3  X			The	values	for the	worst	case or	erati	ng condition
A2 A3			are	given b	y the m	aximum	delay n	ultip	lier.
A2 A3 X									
A2 A3	Equivalen	t Circuit							
A3 — X									
1 x		7_							
A1 X	A3 ———————————————————————————————————								
	A1	~\ <del>\</del>	х						
	1								
	1								
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	1								
1									
UHB-X4B-E2   Sheet 1/1   Page 6-8	UHR-YAR-F2	Sheet 1/1							Page 6-8

# AND-OR-Inverter Family (AOI)

	Unit Cell		Basic
Page	Name	Function	Cells
2-71	D23	2 AND into 2 NOR AOI	2
2-72	D14	3 AND into 2 NOR AOI	2
2-73	D24	2, 2 ANDS into 2 NOR AOI	2
2-74	D34	2 AND into 3 NOR AOI	2
2-75	D36	3, 2 ANDS into 3 NOR AOI	3
2-76	D44	2 OR into 2 AND inot 2 NOR AQI2	

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UH	B" Version
Cell Name	Function							Number of BC
D23	2-wide 2-AND 3-	input A	OI					2
Cell Symbol			Prop	agation	Delay		er	
		t0 t	KCL KCL	t0	KCL KCL	n KCL2	CDR2	Path
		0.73	0.29	0.68	0.14	KOHZ	ODICE	A + X
		0.37	0.22	0.37	0.09	0.12	4	B → X
A1 -	7							
A2	х							
В —								
		Parame	ter			S	ymbol	Typ(ns)*
						ļ		
- · · ·	Input Loading							1
Pin Name A	Factor (lu)					j		
В	ī					1		
1						1		
						]		
	Output Driving							
Pin Name X	Factor (lu)							
^	17							
		* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
		are	values given b	ror the m	worst aximum	case op delav m	ultipl	ng condition
	<u> </u>	·	9					
}								
UHB-D23-E1	Sheet 1/1							Page 7-1

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB								
	Function							Number of BC
D14	2-wide 3-AND 4-	input A	OI					2
Cell Symbol				agation	Delay		ter	
			up		td		1 0===	<b>-</b>   <b>.</b>
	'	t0	KCL	t0	KCL	KCL2		$\begin{array}{c c} & \text{Path} \\ \hline & A \rightarrow X \end{array}$
		0.90	0.29	0.70	0.19	0.21		
		0.32	0.20	0.36	0.09	0.12	4	B → X
							I	
_								
A1	,							
A2								
A3 —								
	х							
В ——	^ ^							
	ı							
		Parame	tor				Symbol	Typ(ns)*
		rarame	ret				оушоот	TAP(II2)
						-		
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						İ		
	Input Loading					j		
Pin Name	Factor (lu)							
A	1					1		
В	i					- 1		j
_	_							
						- 1		1
						1		1
	Output Driving							
Pin Name	Factor (lu)					- 1		
X	14					1		Ì
		* Mini	mum val	ues for	the ty	pical	operat	ing condition.
		The	values	for the	worst	case c	perati	ng condition
		are	given b	y the m	aximum	delay	multip	lier.
		············						
								<u></u>
UHB-D14-E1	Sheet 1/1							Page 7-2

FILITZII C	MOS GATE ARRAY U	NTT CELL	CDECT	ETCATTO	NT		n inne	B" Version
	Function	NII CELI	L BrECI.	FICALIO	IN			Number of BC
				***************************************				
D24 Cell Symbol	2-wide 2-AND 4-	input A	OI Prop	castion	Dolarr	Paramet		2
Cell Symbol		tı	up Prop	agation	td		91	<del></del>
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.54	0.22	0.62	0.14			A → X
		0.67	0.22	0.83	0.14			B → X
								1
								1
_								1
A1	_							1
A2 —	х							
В1 —	^ *							]
В2 —								]
		Parame	ter			S	ymbol	Typ(ns)*
	!							
	Input Loading							
Pin Name	Factor (lu)					l		
A B	1 1					-		
В	1							
						ļ		
	Output Driving							
Pin Name	Factor (lu)							
X	14							
		* Wini	m.,m	nos for	the tw	mical a	norati	ng condition.
		The	mum vai values	for the	worst	case op	erating	g condition
		are	given b	y the m	aximum	delay m	ultipl	ier.
						•		
UHB-D24-E2	Sheet 1/1							Page 7-3
OUD-074-F7	Sheer 1/1							11450 / 7

FILITSILC	MOS GATE ARRAY U	NIT CEL	. SPECT	FICATIO	N		111111	HB" Version
	Function	NII CEE	o bildi.	LICATIO			1 01	Number of BC
D34	3-wide 2-AND 4-	input A	OI P		D-1	D		2
Cell Symbol		+,	up Prop	agation	Delay td	Paramet	er	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.15	0.41	0.73	0.15			A + X
		0.62	0.35	0.43	0.09	0.12	4	B → X
A1 -								
A2	٦_							
	4							
B1	- х							
В2 ———								
					i i			
		Parame	ter			S	ymbol	Typ(ns)*
1								
1								
1						-		
1						- 1		
1								
	Input Loading							
Pin Name	Factor (lu)							1
A	1							1
В	1							
		ļ						
	Output Driving	1						
Pin Name	Factor (lu)							
Х	10							
		* Mini	mum val	nes for	the ty	mical o	perat	ing condition.
		The	values	for the	worst	case or	erati	ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.
UHB-D34-E2	Shoot 1/1							Page 7-4
UIID-D34-E2	Sheet 1/1							11450 / 4

FUITTSU C	MOS CATE ADDAY II	NIT CELL	SPECT	ETCATIO	N		amın.	" Version
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "U Cell Name   Function							N	umber of BC
D36   Cell Symbol	D36 3-wide 2-AND 6-input AOI							3
Cell Symbol Propagation Delay Parameter tup tdn								
		t0	KCL	t0	KCL	KCL2	CDR2	Path
ł		0.77	0.28	0.72	0.14			$A \rightarrow X$
		0.98	0.28	0.87				$\begin{array}{c} B \to X \\ C \to X \end{array}$
		1.17	0.28	1.02	0.14			C → X
$A_{A2}$								l l
В1 —	x							
B2 ———————————————————————————————————	<b>A</b>							
		i						
"		لــــــا				L		<b>—</b>
		Parame	ter			S	ymbol	Typ(ns)*
		l						
						1		
		]						
	Input Loading	1						1
Pin Name	Factor (lu)	}				ļ		
A	1	1						
В	1							
С	1					- 1		
1						- 1		
	Output Driving	l						
Pin Name	Factor (lu)					1		
Х	10							l
		+ Mini	mum .r.a.1	nes for	the to	mical c	maratin	g condition.
		The	walues	for the	worst	case or	perating	condition
		are	given b	y the m	naximum	delay n	ultipli	er.
ł								
1								
İ								
UHB-D36-E1	Sheet 1/1							Page 7-5

							1 11	
	MOS GATE ARRAY U	NIT CEL	L SPECI.	FICATIO	N ·		<u>  "U</u>	HB" Version
Cell Name	Function						Number of BC	
D44	2-wide 2-OP 2-AND 4-input ACT							,
	2-wide 2-OR 2-AND 4-input AOI   Propagation Delay Parameter							2
Cell Symbol Propagation Delay Parameter tup tdn								
		to I	KCL	t0	KCL	KCL2	CDR2	Path
Ì		1.04	0.41	0.78	0.14	RODZ	CDRZ	A + X
		1.03	0.41	0.64	0.14			$B \rightarrow X$
1		0.99	0.29	0.48	0.09	0.11	4	$C \rightarrow X$
l		0.33	0.23	0.40	0.03	0.11	_	0 - A
A1 —								
A2	7							
B —	77							
C	<u> </u>							
"	. 0							
								1
							1	1
1		Parame	ter			1 8	ymbol	Typ(ns)*
						<del>-   -</del>	,	-,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,
j						- 1		
		1				1		
		1						
		1				ł		
	Input Loading	1				1		
Pin Name	Factor (lu)	i						
A	1	1						
В	1	l				- 1		
C	1							
						- 1		
		l						
	Output Driving							
Pin Name	Factor (lu)							
X	10							
			_	_	_			
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
		The	values	for the	worst	case op	erati	ng condition
	are given by the maximum delay multiplier.							
1								
								!
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1								
1								
-								
UHB-D44-E1	Sheet 1/1							Page 7-6
UND-D44-E1	DHEEF I/I							1 2

# **OR-AND-Inverter Family (OAI)**

Page	Unit Cell Name	Function	Basic Cells
2–79	G23	2 OR into 2 NAND OAI	2
2-80	G14	3 OR into 2 NAND OAI	2
2-81	G24	2, 2 OR into 2 NAND OAI	2
2-82	G34	2 OR into 3 NAND OAI	2
2-83	G44	2 AND into 2 OR into 2 NAND OAI	2

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		T"UH	IB" Version
	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "U							Number of BC
G23	2-wide 2-OR 3-input OAI							2
Cell Symbol	Propagation Delay Parameter							
			up		td	n		
		t0 0.72	KCL 0.29	t0 0.55	KCL 0.14	KCL2	CDR2	$\begin{array}{ c c } \hline Path \\ \hline A \rightarrow X \\ \hline \end{array}$
		0.72	0.16	0.55	0.14			$B \rightarrow X$
۸,								
A1 A2	٠٠-							
В —	x						1	
					1			
		Parame	ter	L	l	1 9	ymbol	Typ(ns)*
		Idiame					, m.o.c.i	1,50,113,
Pin Name	Input Loading Factor (lu)							
A	1							
В	1	İ				į		
	Output Driving							
Pin Name X	Factor (lu)							
"	10							
		* Mini	mum val	ues for	the ty	pical c	perati	ing condition.
		The	values	for the	worst aximum	delaw m	eratin	ng condition
	<u> </u>	are	given b	y the n	IAXIMUM	deray ii	urcip.	iter.
								ļ
								ļ
UHB-G23-E1	Sheet 1/1							Page 8-1

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION	THE TERMS OF	MOG GAME ADDAY II	NITE CELL	CDECT	CTCATTO			1177777	U 17
Coll Symbol			NIT CELI	SPECI.	FICATIO.	N			
The values for the typical operating condition.  The values for the worst case operating condition are given by the maximum delay multiplier.	JOIL Hame	1 0110 0 1 011						1,	Camper or bo
Tup to KCL to KCL KOL2 CDR2 Path  1.20 0.42 0.65 0.14 RCL2 CDR2 A + X  0.25 0.16 0.65 0.14 B + X  Parameter Symbol Typ(ns)*  Pin Name Factor (Au)  A 1 B 1  Pin Name Factor (Au)  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	G14	2-wide 3-OR 4-i	nput OAl						2
CO   Color   CCL   CCR2   Path	Cell Symbol				agation			er	
A1 A2 A3 B  Parameter  Input Loading Factor (£u)  X  Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									
A1 A2 A3 B Input Loading Factor (£u)  A							KCL2	CDR2	Path A → Y
Parameter  Parameter  Parameter  Parameter  Parameter  Parameter  Parameter  Parameter  Parameter  Parameter  Parameter  Symbol Typ(ns)*  Typ(ns)*  Parameter  Parameter  Parameter  Parameter  Parameter  Parameter  Symbol Typ(ns)*  Whinimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									
Pin Name   Input Loading   Factor (£u)   A			1 1	0.20					
Pin Name   Input Loading   Factor (£u)   A									
Pin Name   Input Loading   Factor (£u)   A	A1 ——			1					
Pin Name   Input Loading   Factor (£u)   A   1   1		7							
Pin Name   Input Loading   Factor (£u)   A	A3 —	1							
Parameter Symbol Typ(ns)*  Pin Name Factor (£u)  A 1 B 1  Pin Name Factor (£u)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.		x —— (		1					
Pin Name   Input Loading   Factor (&u)   A	В								
Pin Name   Input Loading   Factor (&u)   A									
Pin Name   Input Loading   Factor (&u)   A									
Pin Name   Input Loading   Factor (&u)   A			Paramet	ter				vmbo1	Typ(ns)*
Pin Name Factor (£u)  A 1 B 1  Pin Name Output Driving Factor (£u)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.			1 ul ame					,	-5,5(115)
Pin Name Factor (£u)  A 1 B 1  Pin Name Output Driving Factor (£u)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									[
Pin Name Factor (£u)  A 1 B 1  Pin Name Output Driving Factor (£u)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	1								
Pin Name Factor (£u)  A 1 B 1  Pin Name Output Driving Factor (£u)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									
Pin Name Factor (£u)  A 1 B 1  Pin Name Output Driving Factor (£u)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									
Pin Name Factor (£u)  A 1 B 1  Pin Name Output Driving Factor (£u)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.		Input Loading					ĺ		
A 1 1 1 1	Pin Name	Factor (lu)							
Pin Name Factor (£u)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	A	1							
Pin Name Factor (£u)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	В	1							
Pin Name Factor (£u)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									
Pin Name Factor (£u)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									
Pin Name Factor (£u)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.		Output Driving					- 1		
* Minimum values for the typical operating condition.  The values for the worst case operating condition are given by the maximum delay multiplier.	Pin Name	Factor (lu)							
The values for the worst case operating condition are given by the maximum delay multiplier.		10	L						
The values for the worst case operating condition are given by the maximum delay multiplier.									
are given by the maximum delay multiplier.	İ		W Mini	mum val	ues for	tne ty	picai o	peratii	ng condition.
			are	varues given h	v the m	aximum	delay m	ultipl:	ier.
UHB-G14-E1   Sheet 1/1     Page 8-2		1		521011 2	,				
UHB-G14-E1   Sheet 1/1     Page 8-2									
UHB-G14-E1   Sheet 1/1     Page 8-2									
UHB-G14-E1   Sheet 1/1     Page 8-2									
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UHB-G14-E1   Sheet 1/1   Page 8-2									
UHB-G14-E1   Sheet 1/1     Page 8-2									
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UHB-G14-E1   Sheet 1/1     Page 8-2									
UHB-G14-E1   Sheet 1/1   Page 8-2									
UHB-G14-E1   Sheet 1/1   Page 8-2									
UHB-G14-E1   Sheet 1/1     Page 8-2									
UHB-G14-E1   Sheet 1/1     Page 8-2									
UHB-G14-E1   Sheet 1/1   Page 8-2									
	UHB-G14-E1	Sheet 1/1							Page 8-2

FUITSU C	MOS GATE ARRAY U	NIT CELI	. SPECI	FICATIO	N		"UHE	B" Version
	Function	IVII ODD	D DI LOI	TORITO	.,		I N	Number of BC
			_					
G24 Cell Symbol	2-wide 2-OR 4-i	nput OA	Prop	agation	Dolar	Paramet		2
Cell Symbol		tı	up	agacion	td		<u>e1</u>	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.50	0.29	0.70	0.14			A → X
		0.90	0.29	0.60	0.14			B → X
								1
A1 A2	٦؍							
A2	」)>— x							
B1 —								
B2 —								
		Parame	ter		L	s	ymbol	Typ(ns)*
1								
1						1		1
						ļ		
Din Nama	Input Loading							
Pin Name A	Factor (lu)							
В	ī							
		ŀ				-		
ļ	Output Driving	1				ļ		
Pin Name	Factor (lu)					ĺ		
Х	10							
		* Mini	mum val	nes for	the tw	mical c	nerati	ng condition.
		The	values	for the	worst	case or	eratin	g condition
		are	given b	y the m	aximum	delay n	ultipl	ier.
								}
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UHB-G24-E2	Sheet 1/1							Page 8-3

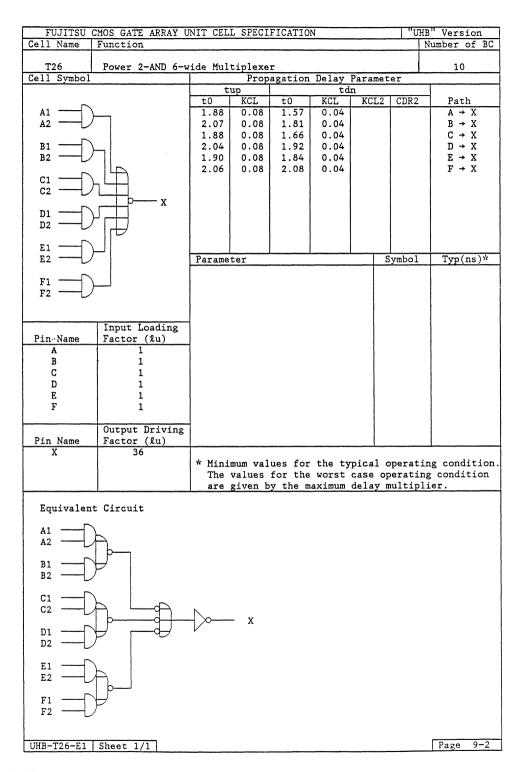
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FUJITSU (	CMOS GATE ARRAY U	NIT CEL.	L SPECI.	FICATIO	N		101	B" Version
Cell Name	Function							Number of BC
G34	3-wide 2-OR 4-i	nnu+ 04	τ				1	2
Cell Symbol	J-wide Z-UK 4-1	nput OA	Pron	agation	Delass	Parama+	<u></u> 1	
Cell Symbol		+-	up	agacion	td	raramet	er	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
	·	0.95	0.29	0.70	0.19	RCLLZ	CDRZ	A + X
		0.70	0.19	0.45	0.16			$B \rightarrow X$
		0.70	0.19	0.45	0.10			D 7 A
A1								
A1 —							l	
1 12	4							
B1	—     b— x							
В2 ——								
7-							l	1
1		Parame	ter				ymbol	Typ(ns)*
		rarame				——	, m 1	1,50,115)
1		l						
	Input Loading	1						
Pin Name	Factor (lu)					-		
A	1	1				- 1		
В	1 1					1		
-	-	l				- 1		
						ļ		
		i				ł		
	Output Driving	t				- 1		
Pin Name	Factor (lu)					- 1		
X	10	1				- 1		
Ì		* Mini	mum val	ues for	the ty	pical o	perat	ing condition.
		The	values	for the	worst	case or	erati	ng condition
		are	given b	y the m	aximum	delay n	ultip	lier.
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UHB-G34-E2	Sheet 1/1							Page 8-4

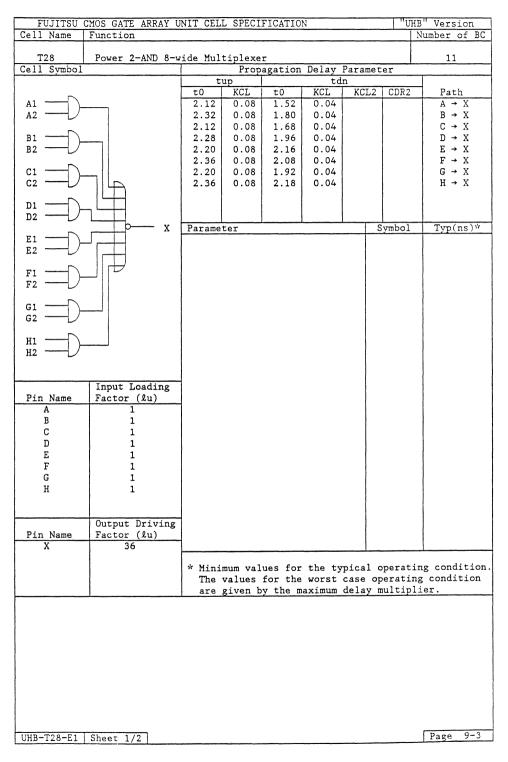
l Prittmen c	THOS CATE ADDAY I	NITT CELL	CDECTI	CTCATTO	N7		TITTE!	011 11
Cell Name	MOS GATE ARRAY U	NII CEL	SPECI	FICATIO	N		) UH.	B" Version Number of BC
CELT HAME	1 4110 0 1 0 11							TOTTOET OF DO
G44	2-wide 2-AND 2-	OR 4-in	out OAI				- 1	2
Cell Symbol			Prop	agation	Delay	Paramet	er	
		ti	αp		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.73	0.29	0.86	0.19			A → X
		0.43	0.29	0.62	0.19			B → X
		0.50	0.16	0.52	0.14			C → X
1 47 —								1
A1 A2	4							
В —								
č	<u>р</u> х							
1		Parame	ter			S	ymbol	Typ(ns)*
						1		
								1
1								
	Input Loading							
Pin Name	Input Loading					- 1		1
A A	Factor (Lu)					i		
B	1					l		
Č	i					l		
"	1.							
		ŀ				1		
	Output Driving							
Pin Name	Factor (lu)					I		
Х	14							
	•							
		* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
		The	values	for the	worst	case op	eratin	g condition
	<u> </u>	are	given b	y the m	aximum	delay m	ultipl	ier.
1								
1								
1								
1								
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UHB-G44-E1	Sheet 1/1							Page 8-5

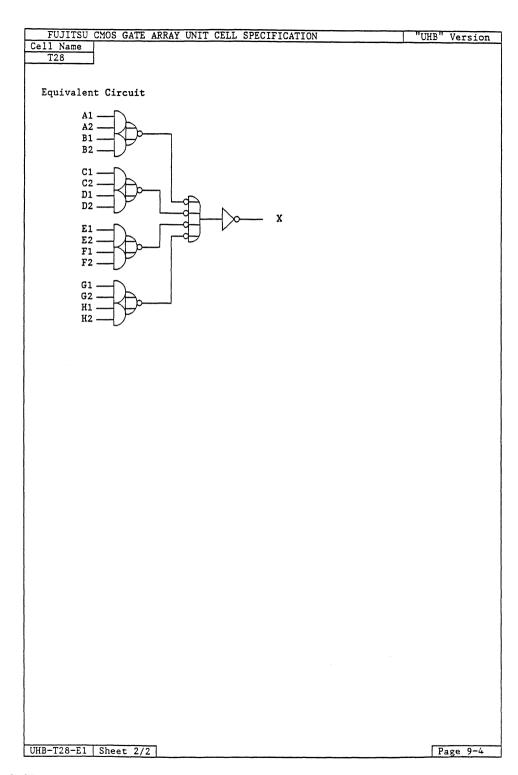
## **Multiplexer Family**

Page	Unit Cell Name	Function	Basic Cells
2–87	T24	4:1 Power 4, 2 ANDs into 4 NOR Multiplexer	6
2–88	T26	6:1 Power 6, 2 ANDs into 6 NOR Multiplexer	10
2–89	T28	8:1 Power 8, 2 ANDs into 8 NOR Multiplexer	11
2–91	T32	2:1 Power 2, 3 ANDs into 2 NOR Multiplexer	5
2–92	T33	3:1 Power 3, 3 ANDs into 3 NOR Multiplexer	7
2-93	T34	4:1 Power 4, 3 AND into 4 NOR Multiplexer	9
2-94	T42	2:1 Power 2, 4 ANDs into 2 NOR Multiplexer	6
2–95	T43	3:1 Power 3, 4 ANDs into 3 NOR Multiplexer	10
2–96	T44	4:1 Power 4, 4 ANDs into 4 NOR Multiplexer	11
2–97	T54	4:1 Power 2, 2-3-4 ANDs into 4 NOR Multiplexer	10
2–98	U24	4:1 Power 4, 2 OR into 4 NAND Multiplexer	6
2–99	U26	6:1 Power 6, 2 OR into 6 NAND Multiplexer	9
2-100	U28	8:1 Power 8, 2 OR into 8 NAND Multiplexer	11
2-101	U32	2:1 Power 2, 3 OR into 2 NAND Multiplexer	5
2-102	U33	3:1 Power 3, 3 OR into 3 NAND Multiplexer	7
2-103	U34	4:1 Power 4, 3 OR into 4 NAND Multiplexer	9
2-104	U42	2:1 Power 2, 4 OR into 4 NAND Multiplexer	6
2–105	U43	3:1 Power 3, 4 OR into 3 NAND Multiplexer	9
2-106	U44	4:1 Power 4, 4 OR into 4 NAND Multiplexer	11

	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			B" Version Number of BC
	ranceron					·····		Mannet Of BC
T24 Cell Symbol	Power 2-AND 4-w	ide Mul			Delay	Dame		6
Cell Symbol		tı	ip Prop	agation	td		ter	T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.62	0.08	1.52 1.76	0.04			$\begin{array}{c} A \rightarrow X \\ B \rightarrow X \end{array}$
		1.58	0.08	1.64	0.04			$C \to X$
A1	<del></del>	1.72	0.08	1.88	0.04			$D \rightarrow X$
A2 -								
B1	44							
B2 —	x							
C1 -	ν <u>π</u>						i	
C2 —								
D1 -								
D2 —	1	Parame	ter				Symbol	Typ(ns)*
Pin Name	Input Loading Factor (lu)							
A B	1 1							
С	1							
D	1							
	Output Driving					-		
Pin Name X	Factor (lu)							
^	36							
		* Mini	mum val	ues for	the ty	pical	operati	ng condition.
		Ine are	values given b	for the v the m	worst	case o delav	peratir multipl	ng condition
			9					
Equivalent	Circuit							
A1 —								
A2	A							
D1 ~	þ—							
B1 ————————————————————————————————————	P   ~ .							
		>	X					1
C1 —	B   W							
	b							
D1	otag							
D2 —	•							
1								
UHB-T24-E1	Chast 1/1							Page 9-1
ORD-124-E1	Sheet 1/1							11050 7 1

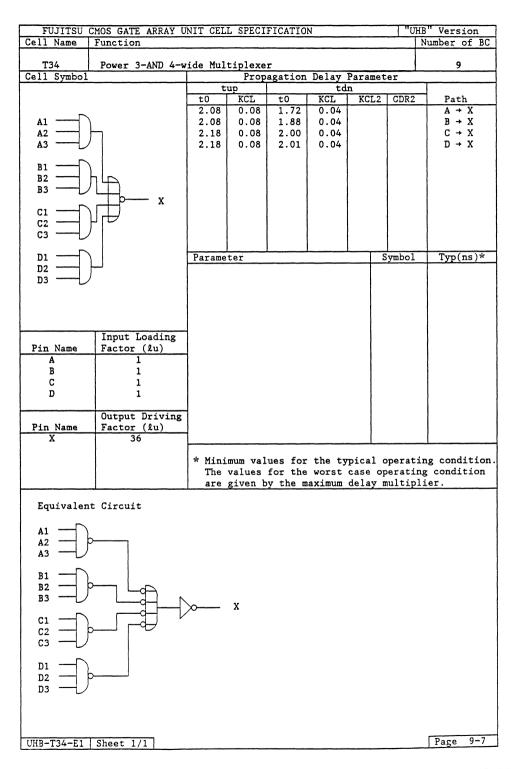




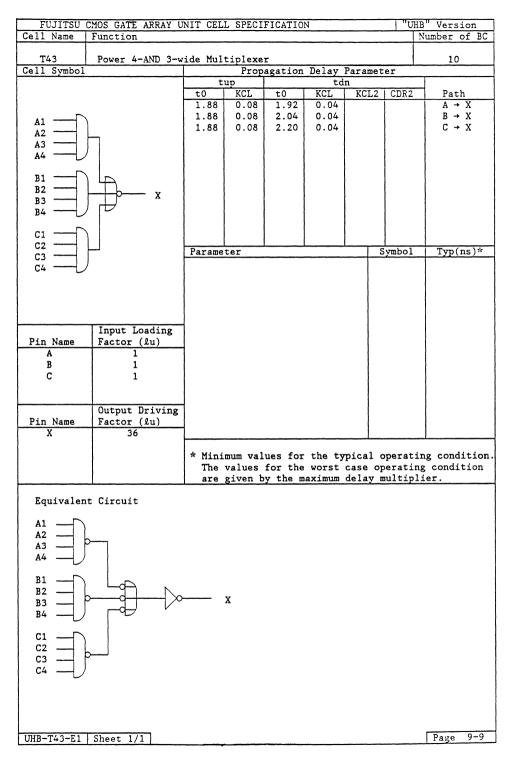


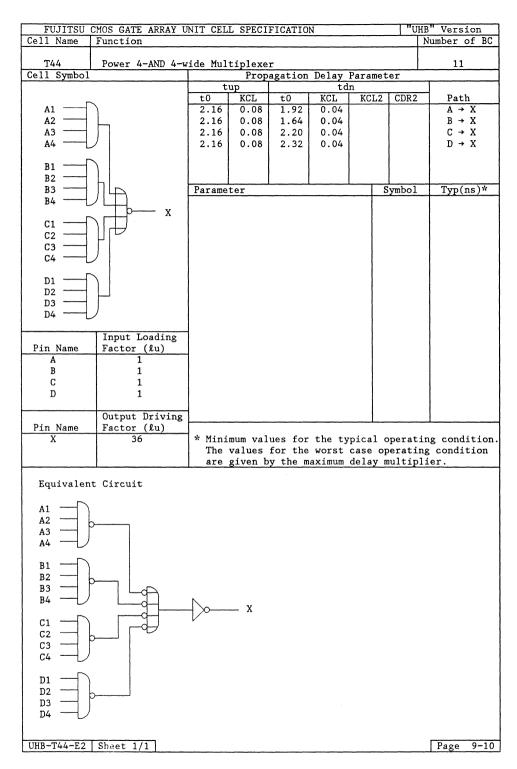
FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		U"UH	B" Version
	Function							Number of BC
T32	Doving 2-AND 2	ido M1	+inl					5
T32 Cell Symbol	Power 3-AND 2-w	rae mul	Prop	r agation	Delav	Paramet	er	3
	<del></del>	t	up	-5	td			T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.52	0.08	1.68	0.04		1	A + X
		1.52	0.08	1.80	0.04			B → X
_							1	
A1	)						1	
A2	$\square_{-}$						1	
A3 —	х							
В1 —	`			į			1	
B2	$\vdash$							
В3 —	)						1	
		Parame	ter			L .	ymbol	Typ(ns)*
		rarame	LET			<del>-   °</del>	,,	Typ(IIS)
						1		
		1				1		
	Input Loading							
Pin Name	Factor (lu)					- 1		
A B	1							
ь	1							
Din Nama	Output Driving							
Pin Name X	Factor (lu)							
-	33							J
		* Mini	mum val	ues for	the ty	pical c	perati	ng condition.
		The	values	for the	worst	case or	eratin	g condition
		are	given b	y the m	aximum	delay n	urcipi	ier.
Equivalent	Circuit							
A1 -								
A2 — Þ								
	<u></u>	>	X					
B1 —		, -						
B2 — 6								
B3 —								
1								
UHB-T32-E1	Sheet 1/1							Page 9-5

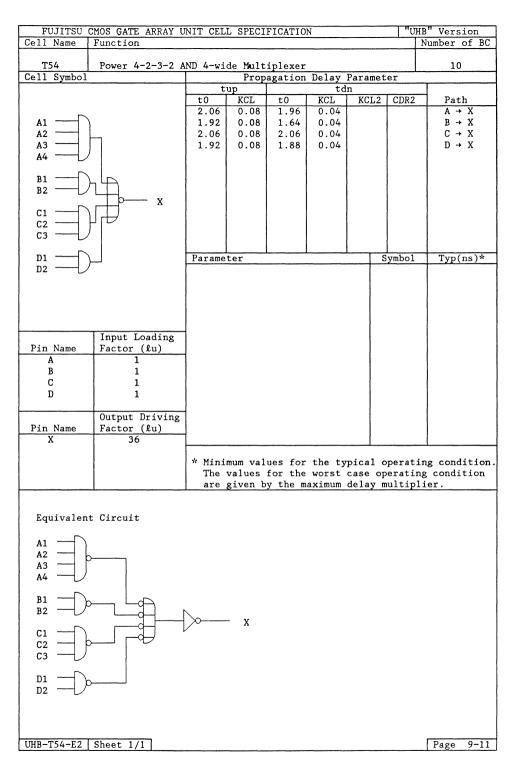
FILTITELL C	MOS GATE ARRAY U	NIT CELL	CDECT	FICATIO	N		"IIIII	B" Version
Cell Name	Function	NII CELI	L SPECI.	FICATIO	IN .		I DAI	Number of BC
							—   ·	
T33	Power 3-AND 3-w	ide Muli	tiplexe	r				7
Cell Symbol				agation		Paramet	er	<del></del>
			up VCT	t0	td	n KCL2	CDDO	- B1
		t0 1.75	KCL 0.08	1.66	KCL 0.04	KCL2	CDR2	Path A → X
		1.75	0.08	1.78	0.04			B + X
		1.75	0.08	1.95	0.04			C → X
A1 -								
A2	7	1						
A3 —		1	1					
B1 -	$\mathcal{T}_{\mathbf{a}}$	1		Ì				
B2	х		1					
B3 —								
C1 —								
C2								
C3 —		Paramet	ter			S	ymbol	Typ(ns)*
1								
						1		
						1		
	Input Loading							
Pin Name	Factor (lu)							
A	1							
В	1					- 1		1
C	1					1		
						-		1
D/- N	Output Driving							
Pin Name X	Factor (lu)							
*	] 50	<b></b>	***************************************					
		* Minir	mum val	ues for	the ty	pical o	perati	ng condition.
		The '	values	for the	worst	case op	erating	condition
	<u> </u>	are	given b	y the m	aximum	delay m	ultipl:	er.
								1
								į
								İ
UHB-T33-E1	Sheet 1/1							Page 9-6



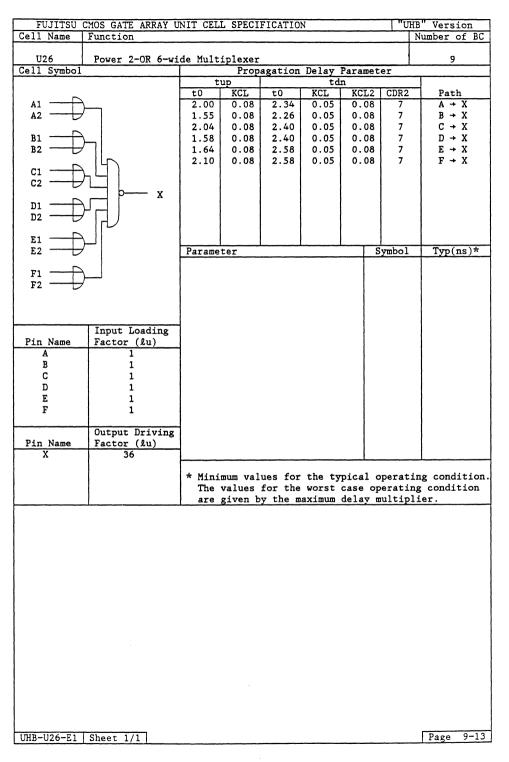
FILTERIA	MOS CATE ADDAY IT	NITT CET	T SPECT	ETCATTO	<u> </u>		111111	B" Version
	MOS GATE ARRAY U Function	MII CEP	L SPECI.	FICALIO	.Y			Number of BC
T42	Power 4-AND 2-w	ide Mul	tiplexe:	<u>r</u>	D-1	Deser		6
Cell Symbol		+	Prop. up	agation	Delay td		er	Т
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.60	0.08	1.88	0.04			A + X
		1.60	0.08	2.00	0.04			$B \rightarrow X$
A1	١							
A2								
A3								
A4 —	' <del></del>							
В1 —	x							
B2								
В3 —								
B4 —	/					L		T- ( ) ('
		Parame	ter			S	ymbol	Typ(ns)*
1								
	Input Loading							
Pin Name	Factor (lu)							
A	1							
В	1							
	Output Driving							
Pin Name	Factor (lu)							
X	36							
		* Mini	mum val	ues for	the tv	pical c	perati	ng condition
		The	values	for the	worst	case op	eratin	g condition
		are	given b	y the m	aximum	delay m	ultipl	ier.
Equipment : : :	Cimanit							
Equivalent	CITCUIT							
A1 —								
A2								
A3 —								
A4 —	1 P		v					
B1 —			X					
B2 -								
В3 —	•							
B4 —								
UHB-T42-E1	Sheet 1/1							Page 9-8
JIID 142 DI	0	<del></del>						1:-9-





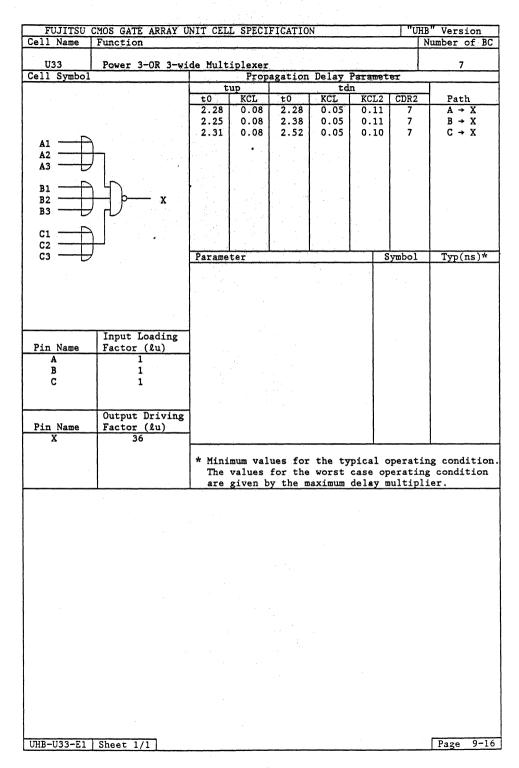


בווודיפוו כי	MOS GATE ARRAY U	NIT CEL	SPECT	FICATIO	N		"IIII"	B" Version
	Function	NII CELL	L BILCI.	FICATIO	<u> </u>		1	Number of BC
1107	D 0 OD /	1. W-1+						
U24 Cell Symbol	Power 2-OR 4-wi	de Mult	Prop	agation	Delay	Paramet	er	6
our cymrer		tı	up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.00	0.08	1.80 1.75	0.05	0.08	7	$\begin{array}{c} A \rightarrow X \\ B \rightarrow X \end{array}$
		1.90	0.08	1.78	0.05	0.08	7	$C \to X$
A1 -		1.38	0.08	1.70	0.05	0.08	7	D → X
A2 —								
В1 —								
B2	1 )							
a:	☐ Þ— x							
C1 C2							ĺ	
D1						L		T ()*
D2 —		Parame	ter			-   S	ymbol	Typ(ns)*
	Input Loading	1						
Pin Name A	Factor (lu)	-						
В	1							
С	1	1						
D	1							
	Output Driving	1						
Pin Name	Factor (lu)	]						
X	36							
		* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
		The	values	for the	worst	case or	eratin	g condition
	<u> </u>	are	given b	y the m	aximum	delay n	ultipl	ier.
1								
UHB-U24-E1	Sheet 1/1							Page 9-12
								<del></del>



FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECT	FICATIO	N		l "U	HB" Version
	Function							Number of BC
U28	Power 2-OR 8-wi	de Mul+	iplexer					11
Cell Symbol	TOUCH 2 OR O WI		Prop	agation	Delay		er	
			up		td		GDDO	
A1 ——		t0 2.11	KCL 0.08	t0 3.18	KCL 0.06	0.10	CDR2	Path A → X
A2		1.55	0.08	3.14	0.06	0.10	7	B → X
==		1.51	0.08	2.81	0.06	0.10	7	C + X
B1 B2	<del></del>	2.07 2.11	0.08	2.86 3.14	0.06 0.06	0.10	7 7	$D \to X$ $E \to X$
		1.55	0.08	3.09	0.06	0.10	7	$\mathbf{F} \rightarrow \mathbf{X}$
C1 C2	¬II_ I	1.46 2.03	0.08	2.54 2.63	0.06	0.10	7 7	$G \rightarrow X$ $H \rightarrow X$
02		2.03	0.08	2.03	0.00	0.10	)	n - k
D1	¬							
D2	<u></u>							
E1 —								
E2 -		Parame	ter			S	ymbol	Typ(ns)*
F1 —								
F2	-1							
G1 ——								
G2						l		
H1 H2								
112						1		-
n	Input Loading							
Pin Name A	Factor (lu)							
В	1							İ
C D	1					}		
E	1							
F	1							
G H	1 1							
п	1							
	Output Driving							
Pin Name X	Factor (lu)							
		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
			values given b					ng condition lier.
	<del> </del>	·						
UHB-U28-E1	Sheet 1/1							Page 9-14

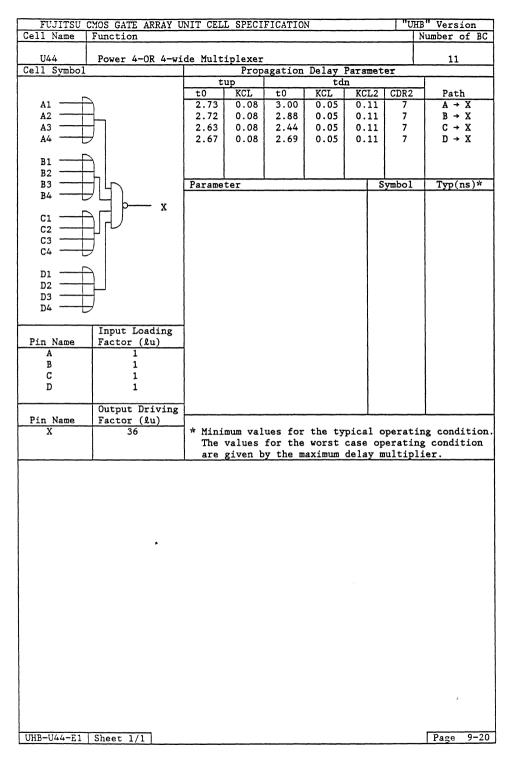
Number of BC   Symbol   S   S	FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UH	B" Version
Propagation Delay Parameter   Symbol   Typ(ns)*									
Propagation Delay Parameter   Symbol   Typ(ns)*	U32	Power 3-OR 2-wi	de Mult	iplexer					5
To   KCL   t0   KCL   KCL2   CDR2   Path	Cell Symbol	10.01 J UN 1 W		Prop	agation	Delay	Paramet	eī	
A1				up	+0			anna	
A1 A2 A3 B1 B2 B3 Parameter Symbol Typ(ns)*  Parameter Symbol Typ(ns)*  Parameter Symbol Typ(ns)*  Pin Name Factor (lu) A B 1 B 1 Comparison of the typical operating condition. The values for the typical operating condition. The values for the worst case operating condition.									Path A + X
A1 A2 A3 B1 B2 B3  Parameter  Symbol Typ(ns)*  Pin Name Factor (lu) A 1 B 1  Pin Name Factor (lu) X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition.									
Parameter  Parameter  Symbol Typ(ns)*  Parameter  Symbol Typ(ns)*  Parameter  Output Driving Pin Name Factor (£u)  X  36  * Minimum values for the typical operating condition. The values for the worst case operating condition.									
Parameter  Parameter  Symbol Typ(ns)*  Parameter  Symbol Typ(ns)*  Parameter  Output Driving Pin Name Factor (£u)  X  36  * Minimum values for the typical operating condition. The values for the worst case operating condition.	<u></u>								
Parameter  Parameter  Symbol Typ(ns)*  Parameter  Parameter  Symbol Typ(ns)*  Parameter  Output Driving Pin Name Factor (£u) X  36  * Minimum values for the typical operating condition. The values for the worst case operating condition.		<del>-</del> -1							1
Parameter  Parameter  Symbol Typ(ns)*  Parameter  Pin Name Factor (lu)  A 1 1  Pin Name Factor (lu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition.		7							
Parameter  Parameter  Symbol Typ(ns)*  Parameter  Parameter  Output Driving Factor (£u)  A 1 B 1  Output Driving Factor (£u)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition.		√ y — x							
Parameter Symbol Typ(ns)*  Parameter Symbol Typ(ns)*  Pin Name Factor (£u)  A 1 1  B 0 1  Pin Name Factor (£u)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition.									
Pin Name   Input Loading   Factor (£u)   A				Ì					
Pin Name   Input Loading   Factor (£u)   A				ĺ					
Pin Name   Input Loading   Factor (£u)   A	}		Parame	ter		L	L	vmbol	Typ(ns)*
Pin Name Factor (2u)  A 1 B 1  Output Driving Factor (2u)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition			. G. ame					, 201	1 275 (115)
Pin Name Factor (2u)  A 1 B 1  Output Driving Factor (2u)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition	1						1		
Pin Name Factor (2u)  A 1 B 1  Output Driving Factor (2u)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition							1		1
Pin Name Factor (2u)  A 1 B 1  Output Driving Factor (2u)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition	1						1		1
Pin Name Factor (2u)  A 1 B 1  Output Driving Factor (2u)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition	ļ						- 1		
A 1 1 B Output Driving Fin Name Factor (£u)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition	Pin Name	Input Loading							1
Pin Name Factor (£u)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition							1		1
Pin Name Factor (2u)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition	В	1							1
Pin Name Factor (2u)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition									1
Pin Name Factor (2u)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition							1		
X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition		Output Driving					-		1
* Minimum values for the typical operating condition. The values for the worst case operating condition							1		1
The values for the worst case operating condition	^	36							
The values for the worst case operating condition are given by the maximum delay multiplier.	]		* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
are given by the maximum delay multiplier.			The	values	for the	worst	case op	eratin	g condition
		L	are	given b	у спе ш	aximum	deray m	ultipi	ier.
	Ì								
	1								
									İ
									]
	•								
UHB-U32-E1   Sheet 1/1   Page 9-15	UHB-U32-E1	Sheet 1/1							Page 9-15



FILITSII (	CMOS GATE ARRAY U	NIT CEL	. SPECT	FICATIO	N		"IIHII	B" Version
	Function	WII ODD	DI BOL	TICATIO			1	Number of BC
	D 0 0 1 1	4. 34 4:	1					
U34 Cell Symbol	Power 3-OR 4-wi	de Mult	Prop	agation	Delay	Paramet	<del></del>	9
Gell Bymbol		t	up	agation	td		<u>e1</u>	1
		t0	KCL	t0	KCL	KCL2	CDR2	Path
	I	2.11	0.08	2.98	0.06	0.10	7	A - X
هـ		2.13	0.08 0.08	3.00 2.44	0.06	0.10	7	$\begin{array}{c} B \to X \\ C \to X \end{array}$
A1 A2		1.92 2.11	0.08	2.44	0.06	0.10	7	$D \to X$
A3 —		2.11	0.00	2.05	0.00	0.10	•	
B1								
B2 B3	747	1						
25	☐ þ— x							
C1 —								
C2 -								
C3 —		Parame	tor		<u> </u>	l	ymbol	Typ(ns)*
D1 —		rarame	reī			- 1 3	ушрот	1 yp(IIS)"
D2	<b> </b>	1						
D3 —								
		}						1
	Input Loading	1						
Pin Name	Factor (lu)					1		
A	1	1						
В	1	[						
C D	1 1							
В	1	1						
	Output Driving							
Pin Name	Factor (lu)	1						1
X	36							l
		* Mini	mum val	ues for	the tv	mical o	perati:	ng condition.
		The	values	for the	worst	case op	eratin	g condition
	<u> </u>	are	given b	y the m	aximum	delay m	ultipl	ier.
UHB-U34-E1	Sheet 1/1							Page 9-17

	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		<b>"</b> UI	HB" Version
Cell Name	Function							Number of BC
U42	Power 4-OR 2-wi	de Mult	iplexer				Ì	6
Cell Symbol			Prop	agation	Delay	Paramet	er	
			ир		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.60	0.08	1.71 1.64	0.05	0.08	7	$\begin{array}{c} A \rightarrow X \\ B \rightarrow X \end{array}$
		2.55	0.00	1.04	0.03	0.08	,	B 7 A
Į.								
A1 -	)							ĺ
A2	<del>-</del> -	<u></u>				<u> </u>		T ()*
A3 A4		Parame	ter			3	ymbol	Typ(ns)*
_	」 > x					ŀ		
B1 —						Ì		
B2	┧	İ				1		
B3	]	1						
B4	,							
		l						
1								
1								
<b>.</b>	Input Loading					l		
Pin Name	Factor (lu)	1						
A B	1							
"	•	1						
		1						
		]				l		
1	Output Driving							
Pin Name X	Factor (lu)		1	f	+hc +	nicci -		ina condition
^	30	The	mum vai values	ues for for the	worst	case or hical c	erati	ing condition.  ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.
			<del></del>	<u> </u>				
1								
1								
UHB-U42-E1	Sheet 1/1							Page 9-18

	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UHI	B" Version
Cell Name	Function						1	Number of BC
U43	Power 4-OR 3-wi	de Mult	iplexer					9
Cell Symbol			Prop.	agation	Delay td		er	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.57	0.08	2.13	0.06	0.08	7	A + X
A1	\	2.62	0.08	2.26 2.39	0.06	0.08	7 7	$\begin{array}{c c} B \to X \\ C \to X \end{array}$
A2								
A3 A4	j							
A4 0			ļ					1
B1	1 4	Parame	ter				Symbol	Typ(ns)*
B2 B3	├─							
В4	, Lo							
cı —								
C2								
C3	<del>]</del>							
C4 —	•							
						j		
	Input Loading					-		
Pin Name	Factor (lu)							
A B	1 1					- 1		
Č	1					- 1		1
								1
	Output Driving							
Pin Name	Factor (lu)							1
Х	36	* Minii	mum val values	ues for for the	the ty	pical o	operatii Deratini	ng condition. g condition
		are	given b	y the m	aximum	delay r	nultipl	ier.
UHB-U43-E1	Sheet 1/1							Page 9-19



## **Clock Buffer Family**

Page	Unit Cell Name	Function	Basic Cells
2–109	K1B	True Clock Buffer	2
2-110	K2B	Power Clock Buffer	3
2-111	КЗВ	Gated Clock (AND) Buffer	36
2-112	K4B	Gated Clock (OR) Buffer	36
2-113	K5B	Gated Clock (NAND) Buffer	3
2-114	KAB	Block Clock (OR) Buffer	55
2-115	KBB	Block Clock (OR x 10) Buffer	30

TILITANI I		NITT OFF	CDCCT	TTO A MT C			117	ID II 17
	CMOS GATE ARRAY U Function	NII CEL	L SPECI	r ICATIO	N		1 "U	IB" Version Number of BC
Cell Name	Function							Mumber of BC
K1B	True Clock Buff	er						2
Cell Symbol				agation			er	
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.72	0.08	0.86	0.04			A → X
	· •							
Α	У х							
								İ
		Parame	ter			l s	ymbol	Typ(ns)*
		Tarane					yu.bor	239(22)
						1		
						į		
	,							ŧ
	Input Loading					[		
Pin Name	Factor (lu)					1		İ
A	1							1
						- 1		Ì
						ļ		
						l		1
						1		
	Output Driving							
Pin Name	Factor (lu)					- 1		
Х	36				<del></del>			1
		* Mini	mum 17a 1	ne for	the to	mical o	nerst	ing condition.
		The	walnes	for the	worst	case on	erati	ng condition
		are	given b	y the m	aximum	delav m	ultip	lier.
	<u> </u>		×					
Equivale	nt Circuit							
A>	x							
	V							
								D 10 1
UHB-K1B-E1	Sheet 1/1							Page 10-1

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		UHI	" Version
Cell Name	Function						1	lumber of BC
K2B	Power Clock Buf	fer						3
Cell Symbol				agation			er	·
			up		td		<del>,</del>	1
		t0	KCL	t0	KCL	KCL2	CDR2	Path A → X
		1.06	0.04	1.20	0.03			A + X
								1
								l
	N							1
Α	x							
								1
								1
		<u> </u>	L		L	<u> </u>	<u> </u>	T ( \sk
		Parame	ter			<u></u>	ymbol	Typ(ns)*
	T T3/							
Din Nama	Input Loading					İ		1
Pin Name	Factor (lu)							
A	1							
						- 1		
	Output Driving					l		
Din Nama	Factor ((1))					ĺ		
Pin Name X	Factor (lu)							
^	-							<u> </u>
	·	sk Mini	mum 1701	une for	the to	mical c	marati	ng condition.
		The	walue	for the	worst	prear c	perating	g condition.
		270	given b	tor the m	avimum	delaw n	miltinl	ier
<b> </b>		are	STAGII D	y cite II	ev Tinnii	deray I	интетрт.	rer .
Equivalan	t Circuit							
Ligarvaren								
_ N	N .							•
A — >	→ ¬ ×							
	V							
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1								
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1								
1								
1								
1								
UHB-K2B-E1	Sheet 1/1							Page 10-2

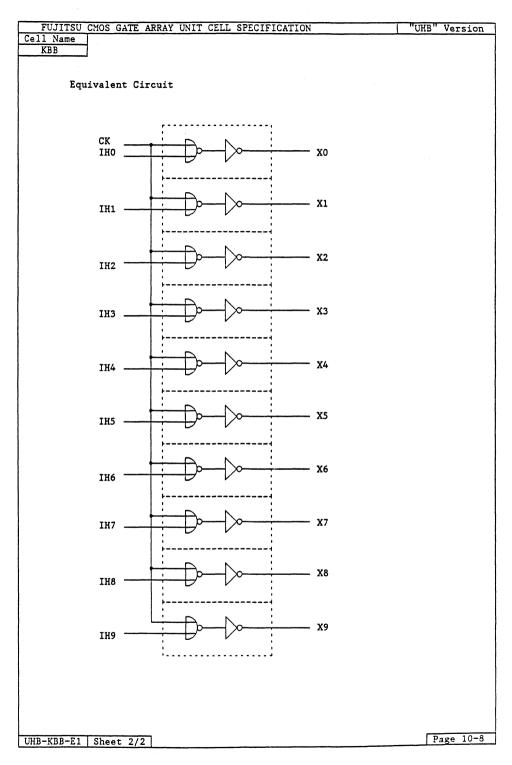
FUJITSU CI	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UH	B" Version
Cell Name	Function							Number of BC
Wan.	C-+ 1 C11- (AN	D) DE.E.						2
K3B Cell Symbol	Gated Clock (AN	D) Buil	Prop	agation	Delay	Paramet	er	2
JOIL DYMESI		tı	up	-8	td			T
		t0	KCL	t0	KCL	KCL2	CDR2	Path A → X
		1.00	0.08	1.00	0.04			A + X
A1	`							
A2 -	)— x							
R2 (								
		Parame	ter			S	ymbol	Typ(ns)*
							·	
						1		
	Input Loading							
Pin Name	Factor (lu)					1		
A	ī							
						1		
	Output Driving							
Pin Name	Factor (lu)							
Х	36							
			_	_				,
		* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
		are	values given h	or the m	aximum	delay m	ultipl	g condition
		<u> </u>	given b	<i>y</i> <b>c</b> nc n	- CALLEDON	doray	- CLULPI	
Equivalent	Circuit							
A1						•		
A2 —	— q x							
_								
								D 10 2
UHB-K3B-E2	Sheet 1/1							Page 10-3

	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		1 "UH	B" Version
Cell Name	Function			<del></del>				Number of BC
K4B	Gated Clock (OR	) Buffer	<u>r</u>					2
Cell Symbol			Prop	agation			er	
			up	+0	td		GDDG	
		t0 0.78	0.08	t0 1.14	0.05	0.07	CDR2	Path   A → X
		0.78	0.08	1.14	0.05	0.07	٥	AAA
								1
A1 ——	<b>→</b> ,,							
A2	x	l						
		Parame	ter			S	ymbol	Typ(ns)*
						l		
						1		
						İ		
	Input Loading							
Pin Name	Factor (lu)							
A	1							1
						`		
	Output Driving							
Pin Name	Factor (lu)							
Х	36							1
		* Mini	mum val	ues for	the tv	nical c	nerati	ng condition.
		The	values	for the	worst	case or	eratin	g condition
		are	given b	y the m	aximum	delay m	ultipl	ier.
							-	
P								
Equivalent	CITCUIT							
A1 —	N							
A1 A2	>							
	ν							
UHB-K4B-E1	Sheet 1/1							Page 10-4

THITTE!! C	MOC CATE ADDAY II	NITT CET	CDECT	EICATIO	NI.		17,777	B" Version
	MOS GATE ARRAY U	HII UEL.	u ofect.	FICHITU	14		I UH	Number of BC
			-		****			
K5B	Gated Clock (NA	ND) Buf	fer					3
Cell Symbol			Prop	agation			er	
			up		td		anna	٠
		t0	KCL	t0	KCL	KCL2	CDR2	Path A → X
		1.14	0.08	1.48	0.04			$A \rightarrow X$
							1	
A1 ——	$\overline{}$							
A2 —	р <u>—</u> х							
AZ [							ļ	1
		Dors	+			L	vmb = 1	Tym(na)*
		Parame	rer				ymbol	Typ(ns)*
								1
	Input Loading							
Pin Name	Factor (lu)							
A	1							
	Output Driving					ľ		
Pin Name	Factor (lu)							
X	36							
		* Mini	mum val	ues for	the ty	pical c	perati	ng condition.
		The	values	for the	worst	case or	eratir	ng condition
		are	given b	y the m	aximum	delay m	ultipl	ier.
Faurinalas	t Circuit							
Equivalent	CITCUIC							
~	, ,							
A1	$\sim$	— х						
A2	V	Λ						
[								
								[D 10 5
UHB-K5B-E2	Sheet 1/1							Page 10-5

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		UHU"	B" Version
Cell Name	Function						1	Number of BC
KAB	Riock Cleak (OP	) R., ff.	-				ĺ	ا
Cell Symbol	Block Clock (OR	, burre	Prop	agation	Delay	Paramet	er	3
		t	up	<u></u>	td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path A → X
		1.08	0.04	1.85	0.03			A → X
A1	A ,							
A2	x						1	
			İ				İ	
							<u></u>	<u> </u>
		Parame	ter			-   -	Symbol	Typ(ns)*
								1
	·							
Din Nama	Input Loading Factor (lu)							
Pin Name A	1							
	_							
	Output Driving							
Pin Name	Factor (lu)							
X	55							
1				_				
1		* Mini	imum val	ues for	the ty	pical o	operati	ng condition.
		are	values given h	ov the m	aximum	delav	peratin multipl	g condition ier.
		are	PTACH F	., one i		20145		
Equivaler	t Circuit							
A1 —	h							
A2	x — ¬							
1								
HILD KAD DO	Chara 1/2							Page 10-6
UHB-KAB-E2	Sheet 1/1							rage 10-0

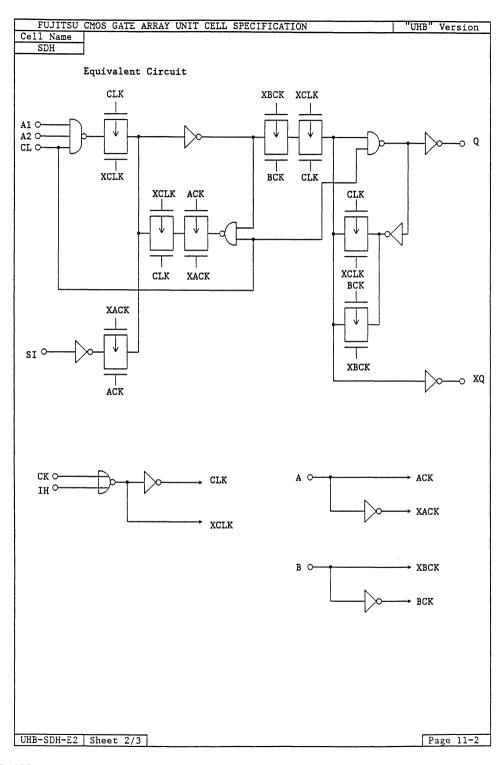
FUJITSU C	MOS GATE ARRAY U	NIT CELI	SPECI	FICATIO	N		"UH	B" Version
	Function			1011110				Number of BC
КВВ	Block Clock Buf	fer (OR	x 10)					30
Cell Symbol	BIOCK CIOCK BUI	Tel (OK	Prop	agation	Delay	Paramet	er	30
			up		td	n		
		t0 1.34	KCL 0.04	t0 2.08	KCL 0.03	KCL2	CDR2	Path CK → X
		1.08	0.04	1.85	0.03			IH → X
GT/								
CK								
ІНО —	xo						ļ	
IH1 IH2	X1 X2						]	
ІНЗ	хз						ĺ	
IH4 IH5	X4 X5							
IH6	X6							
IH7	X7				i 	L	<u> </u>	
IH8 IH9	X8 X9	Parame	ter				ymbol	Typ(ns)*
	T T 3'-							
Pin Name	Input Loading Factor (lu)							
CK	10							
IH	1					1		
	Output Driving					l		
Pin Name	Factor (lu)					- 1		
Х	55							
		* Mini	mum val	ues for	the ty	pical c	perati	ng condition
		The	values	for the	worst	case op delay m	eratin	g condition
	1	are	given b	y the m	axIIIUIII .	deray n	urcipi	iei.
•								
ו ים מקע_קעון	Shoot 1/2							Page 10-7
UHB-KBB-E1	Sheet 1/2				<del>,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,</del>			Tage 10 /

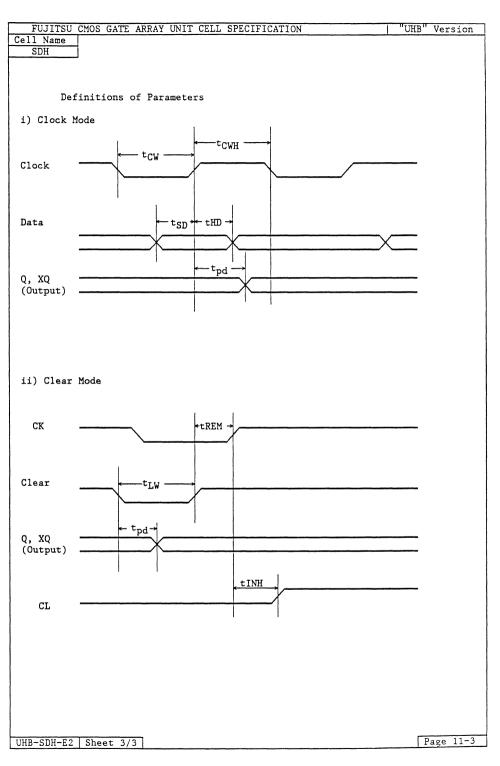


## Scan Flip-flop (Positive Edge Type) Family

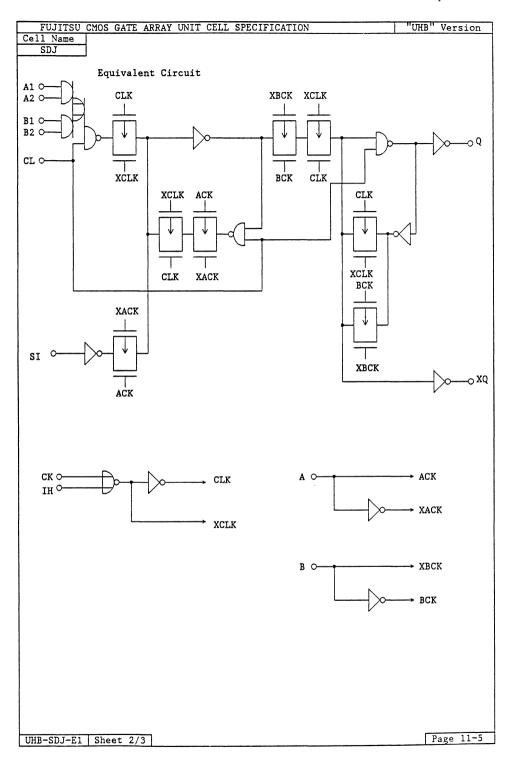
Page	Unit Cell Name	Function	Basic Cells
2–119	SDH	Scan D Flip-flop with 2:1 Multiplex with Clear and Clock Inhibit	14
2–122	SDJ	Scan D Flip-flop with 4:1 Multiplex with Clear and Clock Inhibit	15
2–125	SDK	Scan D Flip-flop with 3:1 Multiplex with Clear and Clock Inhibit	16
2-128	SJH	Scan J-K F with Clear and Clock Inhibit	36
2–131	SDD	Scan D Flip-flop with 2:1 Multiplex, Preset Clear, and Clock Inhibit	16
2-135	SDA	Scan 1-input D Flip-flop with Clock Inhibit	12
2-138	SDB	Scan 1-input D Flip-flop with Clock Inhibit	42
2-142	SHA	Scan 1-input D Flip-flop with Clock Inhibit	68
2–145	SHB	Scan 1-input D Flip-flop with Clock Inhibit and Q Output	62
2–148	SHC	Scan 1-input D Flip-flop with Clock Inhibit and XQ Output	62
2–151	SHJ	Scan D Flip-flop with 2:1 Multiplex and Clock Inhibit	78
2–154	SHK	Scan D Flip-flop with 3:1 Multiplex and Clock Inhibit	88

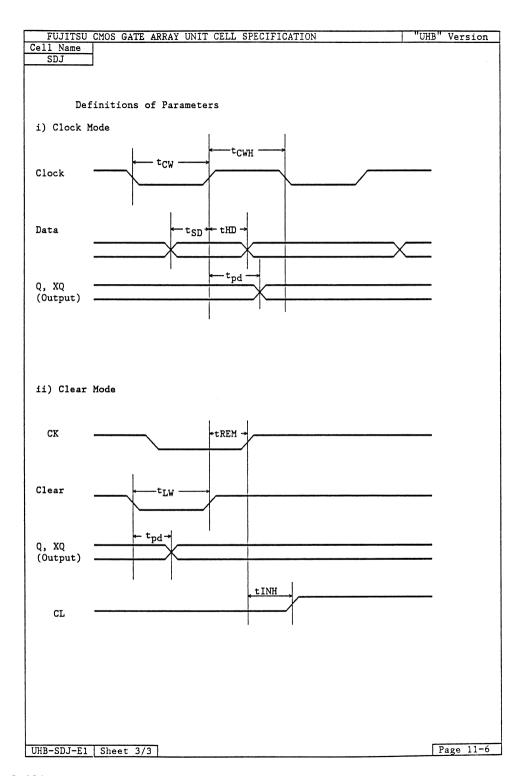
FUJITSU			RRAY U	NIT CEI	L SPECI	FICATIO	N			"UH	IB" Version
Cell Name	Func	tion								4	Number of BC
SDH	SCA	N 2-in	put DF	T with	Clear 8	Clock-	Inhibit	t			14
Cell Symbo	1					agation			eter		
					up	<del> </del>		dn Tror	0   00	77.0	J
				t0 3.72	0.08	t0 2.98	KCL 0.04	KCI 0.0		7 7	Path CK,IH → Q
				2.35	0.08	2.15	0.04	1		7	CK,IH → XQ
				3.79	0.08	1.07	0.04	1		7	CL + Q,
і г		7		1							XQ
A1 ————————————————————————————————————								1			
CK			Q	İ	ļ						
IH —		1				Ì			İ		
					<u> </u>						
sı —											
A		p	XQ						L_		
в — с				Parame		1: d+b			Symb tCW		Typ(ns)*
	Ŷ				Pulse V				tCh		5.4
	- 1			GIOCK	rause .	TIME				111	7.3
	CL				Setup Ti				tSI		3.7
				Data I	Hold Tim	ne			tΗ	)	1.0
				<u> </u>	D. 1	11.1+1-			+T1	.,	/ -
					Pulse V				tLV		3.0
	Inp	ut Loa	ding		Hold T				tIN		1.5
Pin Name		tor (l									
A1,A2		1		1							
CK		1						l			
CL		1 3		1				1			
SI	1	1									
A,B		2						1			
1								1			
								}			
	011	put Dr	izzina	1							
Pin Name		tor (l									
Q	1	36		* Min	imum vai	lues for	the t	ypica:	l oper	at:	ing condition.
XQ		36		The	values	for the	worst	case	opera	atiı	ng condition
				are	given l	by the n	naximum	dela	y mult	tip.	lier.
Function	Table										
runction	Table										
					•				7		
MODE			INI	PUT			OUT	PUT	4		
	CLK	CL	D	A	В	sı	Q	XQ	1		
	CLIK	<u> </u>				31	<u> </u>	<u> </u>	┪		
CLEAR	X	L	Х	X	X	х	L	н			
				_	_				7		
CLOCK	L→H	H	Di	L	L	X	Di	Di	-		
	Н	Н	Х	L	L	x	Q <sub>o</sub>	XQ <sub>o</sub>			
						-	٠.٠	40	4		
SCAN	Н	H	X	$L{\to}H{\to}L$	Н	Si	$Q_{o}$	$XQ_0$			
	17			<b>-</b>		v .	C :	<del></del>	1		
	H	H	X	L	H→L→H	X	Si	Si	١		
						Note	: CLK	= CK	+ IH		
								= A1			
UHB-SDH-E2	Shee	t 1/3	L								Page 11-1



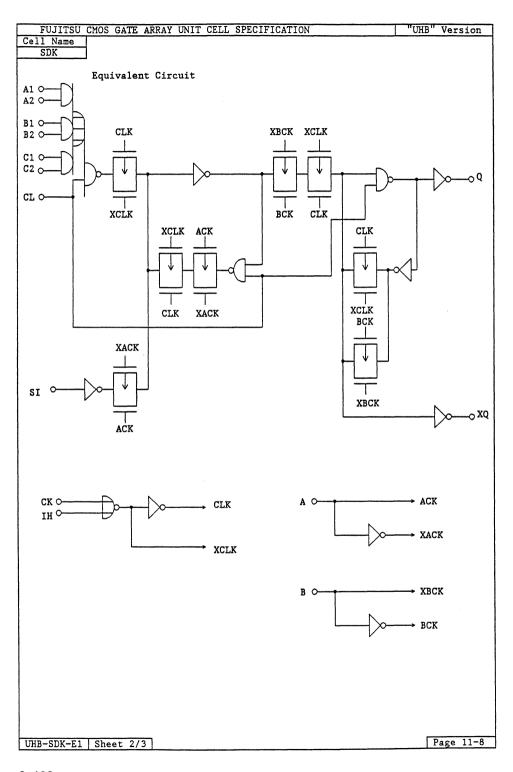


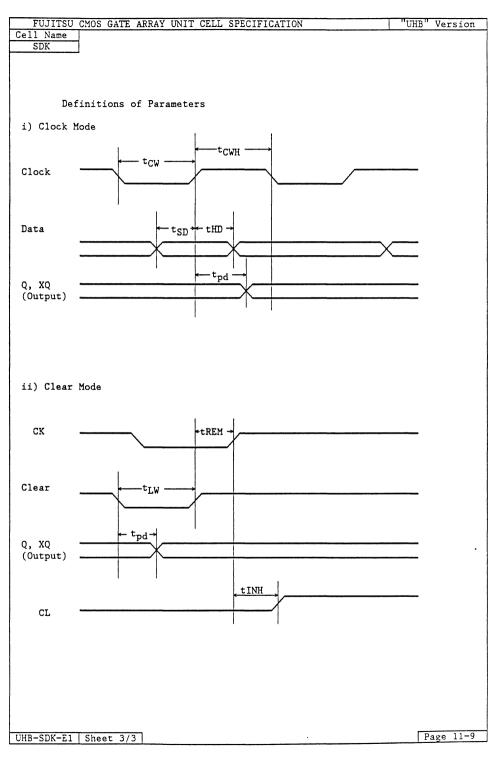
FUJITSU	CMOS	GATE A	RRAY	UNIT CE	LL SPECI	FICATIO	N			T "U	HB" Version
Cell Name	Func										Number of BC
SDJ	SCA	N 4-in	nut Di	FF with	Clear 8	2 Clock-	·Inhihi	+			15
Cell Symbo		17 111	pac D	T WICH		pagation			nete	r	13
					tup			dn			
				t0	KCL	t0	KCL		_	CDR2	
				2.75	1	3.02	0.04			7 7	CK,IH → Q CK,IH → XQ
_	·	_		3.74		1.06	0.04			7	$CL \rightarrow Q$
A1				3.,,	1 0.00	1.00	0.04	1		•	XQ
A2							1				
B1			Q			İ					
CK —							l				
IH —		į.			1						
***				ŀ				1	ŀ		
sı —		р— xq									
Α				Param						mbol	Typ(ns)*
в — 9					Pulse V					CW	5.4
_	9			Clock	Pause ?	ıme			t	CWH	4.5
				Data	Setup T:	ime			t.	SD	4.4
	CĽ				Hold Tir					HD	0.8
					Pulse V					LW	4.5
	T <del>T</del>	T	33		Release					REM INH	3.0
Pin Name		ut Loa tor (l		Clear	Hold T	гше				INI	1.3
A1,A2	1	1	<u>-,                                     </u>								
B1,B2	1	1		1							
CK	l	1						1			
IH CL		1 3						İ			
SI		1		1							
A,B		2						i			
	1			1				1			
			<del>, ,</del>	4				İ			
Pin Name		put Dr tor (l						1			
Q	Tac	36	<u>u)</u>	* Min	imum vai	lues for	the t	vpica	1 op	erat	ing condition.
XQ	Ì	36		The	values	for the	worst	case	ope	rati	ng condition
				are	given	by the m	naximun	dela	y mu	ltip	lier.
Function	Table										
runction	labie										
									7		
MODE			IN	PUT			ou	TPUT	4		
	CLK	CL	D	A	В	sı	Q	XQ			
	ODK	- OH							1		
CLEAR	X	L	Х	X	X	Х	L	H			
0.5.5.5					_			=-			
CLOCK	L→H	H	Di	L	L	X	Di	Di	4		
	н	Н	х	L	L	x	Q.	ΧQο	1		
		**					٧0		4		
SCAN	Н	H	Х	$L\rightarrow H\rightarrow L$	Н	Si	$Q_{o}$	$XQ_0$			
	Н	Н	Х	L	H→L→H	Х	Si	Si	7		
									_		
					Note	: CLK =			<b>,-</b> -		
UHB-SDJ-E	1   Cha-	+ 1/2	1			D =	(A1 x	A2) +	(B)	L X B	Page 11-4
CHD-SDJ-E.	r   piree	t 1/3									



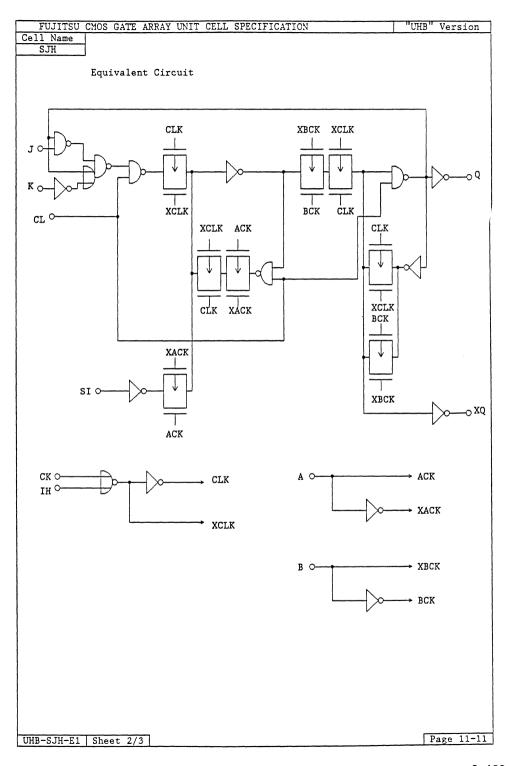


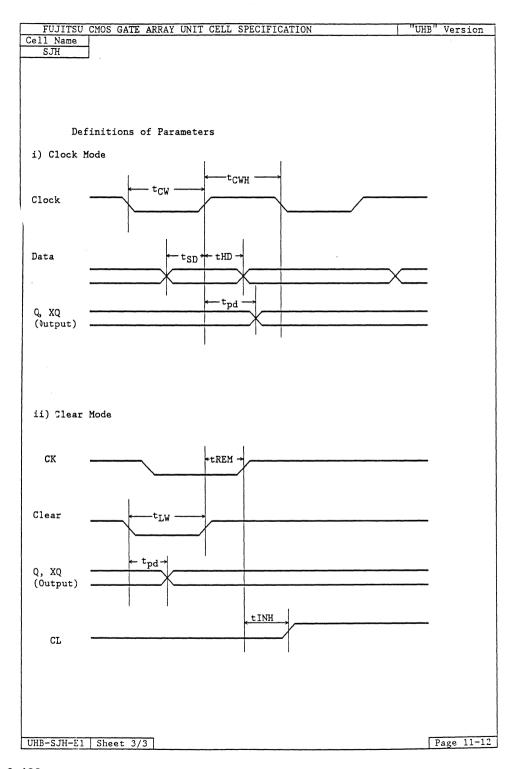
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version											
Cell Name	Func										Number of BC
SDK	SCA	N 6-in	out DE	T with	Clear &	Clock-	Inhibi	t		İ	16
Cell Symbo			7		Prop	agation	Delay	Para	neter	:	
					up			dn	F 0 1 6	7000	Dh
				10 3.70	KCL 0.08	t0 3.00	KCL 0.04	KC:		DR2 7	Path CK,IH → Q
1 -		7		2.32	0.08		0.06			7	CK, IH → XQ
A1 -				3.74	0.08	1.02	0.04	0.	08	7	CL → Q,
A2 B1				1							XQ
B2		<b> </b>	Q	1							
C1 -				l							
C2 CK		1		j			i				
IH —											
		þ—	ΧQ		<u> </u>			<u> </u>			
SI				Parame	ter Pulse W	idth				nbol CW	Typ(ns)* 5.4
B — d					Pause T					WH CWH	4.5
	Ŷ										
					Setup Ti					SD m	0.5
1	Data Hold Time tHD								ш	1 0.3	
					Pulse W					_W_	4.5
	Tan	ut Loa	diaa		Release Hold Ti					REM INH	3.0
Pin Name		tor (l		Clear	noid ii	ше			L.	LINII	+
A1,A2		1		1							
B1,B2											
C1,C2 CK											
IH	1										
CL		3									
SI A,B		1 2		İ							
,-				]							
Pin Name		put Dr tor (l									
Q	Fac	36	<u>u)</u>	* Mini	.mum val	ues for	the t	vpica	1 000	erati	ing condition.
XQ		36		The	values	for the	worst	case	oper	atir	ng condition
				are	given b	y the m	aximum	dela	y mul	ltip	lier.
Function	Table										
									7		
MODE			INF	TU			OUT	PUT	-		!
	CLK	CL	D	A	В	sı	Q	хq			
CLEAR	х	L	х	Х	X	x	L	Н			
CLOCK	L→H	н	Di	L	L	x	Di	Di			
	Н	н	х	L	L	х	Q <sub>0</sub>	XQ <sub>o</sub>			
SCAN	Н	Н	x	L→H→L	Н	Si	Q <sub>0</sub>	XQ <sub>o</sub>	1		
	Н	Н	Х	L F	I→L→H	х	Si	Si	1		
			Note		= CK + $= (A1 x)$		(B1 x	B2) +	(C1	x C2	2)
UHB-SDK-E1	Shee	t 1/3	<u></u>								Page 11-7





FUJITS	CMOS	GATE A	RRAY U	NIT CE	ELL SPE	CIFICA	TIO	N	<del></del>		"U	HB" Version
Cell Name												Number of BC
SJH	SCA	N T-K	FF wit	h Clas	ar & Clo	ock-Tr	hih	i+				16
Cell Symbo		uv J·K	IF WIC	li Ciea				Delay	Para	nete		10
					tup			td				
				t0	KCL	tO		KCL	KCI		CDR2	Path
				4.24	1	1	37	0.04	0.0		7	CK,IH → Q
				2.36	t	1	16	0.06	0.:		7	CK,IH → XQ
				3.76	5 0.0	3   1.	39	0.04	0.0	08	7	CL → Q,
J —									Ì			XQ
<u>к</u> — ф			Q			İ				l		•
ck —		1	•	Parar	neter				$\vdash$	Sv	mbol	Typ(ns)*
IH —					Pulse		1				CW	5.4
				Clock	c Pause	Time				t	CWH	4.5
SI —												
A		ρ—	XQ	Data	Setup ?	Time (	J)				SD	4.4
в — 9					Setup :			,			SD	4.8
	Y			Data Hold Time (J,K) tHD							ш	0.5
				Clear	Pulse	Width	ı			t	LW	4.5
	CL				Releas						REM	3.0
				Clean	Hold '	Γime					INH	1.5
***************************************												
D: 17		ut Loa		1								
Pin Name J,K	Fac	tor (l	.u)	l								
CK	1	1										
IH		ī		1								
CL		3					İ					
SI	1	1		Ì					1			
A,B		2										
		D		1					1			
Pin Name		put Dr							l			
Q	120	* Minimum values for the typical operat										ing condition.
χQ	l	36					ng condition					
~~~					e given							
T	_ Tr.1											
Function	n Table											
	····			INPUT					OU.	TPUT		
MODE												
	CLK	CL	J	K	A	В	S	<u> </u>	Q	Х	Q	
CLEAR	Х	L	Х	х	Х	X	Х		L	Н		
	L→H	н	L	L	L	L	Х		L	Н		
	L→H	н	н	н	L	L	Х		Н	L		
CLOCK	L→H	н	L	н	L	L	х			χQ		
CLOCK				<del></del>					Q <sub>0</sub>			
	L→H	Н	Н	L	L	L	X		XQ <sub>0</sub>	Q	!o	
	Н	Н	X	X	L	L	Х		Q <sub>0</sub>	XQ	0	
SCAN	Н	Н	X	Х	L→H→L	Н	S	i	Q <sub>0</sub>	XQ	0	
	Н	Н	Х	Х	L :	H→L→H	Х		Si	S	i	
HID CHI P	1   61	+ 1/0	٦		Not	e : CI	LK =	CK + 1	Н			Page 11-10
UHB-SJH-E	I   Shee	t 1/3	L									Page 11-10





FUJITSU	CMOS G	ATE AP	RAY II	NIT CEL	I. SPECT	FICATIO	N			1 717	HB" Version
Cell Name	Funct		IAI O	MII OLL	D DILLOI	TIONITO				1 -	Number of BC
SDD			ut DF	F with	Clear.	Preset	& Cloc	k-Inh	ibit		16
Cell Symbol						agation					
				t	up			dn			
	PR			t0	KCL	t0	KCL	KC	L2   (	CDR2	Path
	1			3.70	0.08	3.22	0.04	0.	08	7	CK, IH → Q
				2.65	0.08	2.14	0.06	0.	12	7	CK, IH → XQ
	_	_		4.50	0.08	1.02	0.04	0.	08	7	CL → Q,
A1 ————————————————————————————————————			Q	3.84	0.08	2.35	0.06	0.	12	7	PR → Q,
IH —								<u></u>			
sı —				Parame		2.241-				mbol	Typ(ns)*
A		р x	Q		Pulse W Pause T					CW CWH	5.4
В —				CIOCK	rause 1	Tue			E	CMU	4.3
	Q	J		Data C	etup Ti	mo			+ (	SD	5.4
1					old Tim					HD HD	1.0
-	1			Data II	Old III						+
	CL			Clear	Pulse W	idth			t1	LW	5.0
					Release					REM	3.0
	Inpu	t Load	ing	Clear	Hold Ti	me			t:	INH	1.5
Pin Name	Fact	or (lu	)								
A1,A2		1			Pulse					PW	6.8
CK		1			Releas					REM	3.7
IH	1	1		Preset	Hold T	ime			t.	INH	1.0
CL	1	3									
PR SI	-	3 1									
A,B		2									
н, в		2									
Din Nama		ut Dri									
Pin Name Q	Fact	or (lu 36	,	* Mini	m11m 17a1	ues for	the t	unica	1 000	erst.	ing condition.
xQ	į.	36									ng condition
		-									
Function	Table										
MODE				INPUT OUT					UTPU	т	
	CLK	CL	PR	D	A	В	sı	Q		χQ	
CLEAR	х	L	Н	X	Х	х	x	L	1	н	
PRESET	Х	н	L	Х	Х	Х	х	Н	1	L_	
CLOCK	L→H	Н	Н	Di	L	L	х	Di	j	Di	

X X X Prohibited

Note : CLK = CK + IH

D = A1 x A2

X

Si

Х

 $Q_{\boldsymbol{o}}$ 

 $Q_{\boldsymbol{0}}$ 

Si

 $XQ_{\,\boldsymbol{0}}$ 

 $\text{XQ}_{\,\textbf{0}}$ 

 $\overline{Si}$ 

UHB-SDD-E3 Sheet 1/4

SCAN

CL/PR

Н

Н

Н

H

H

H

H

Н

Н

X

X

Х

Х

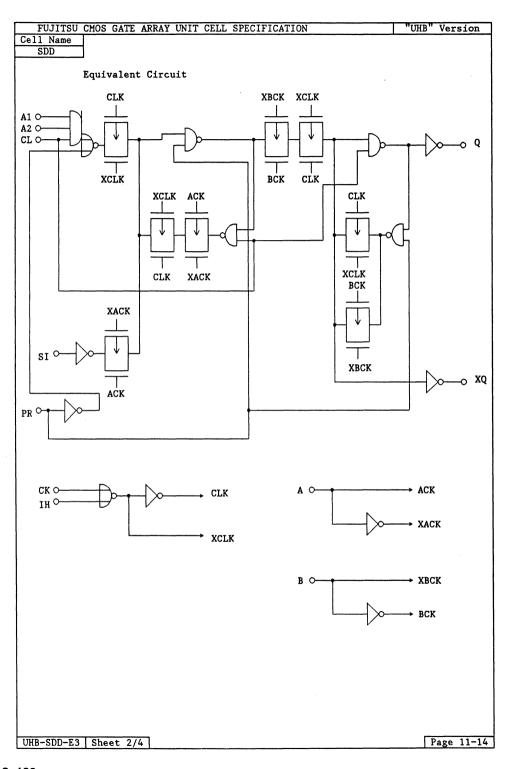
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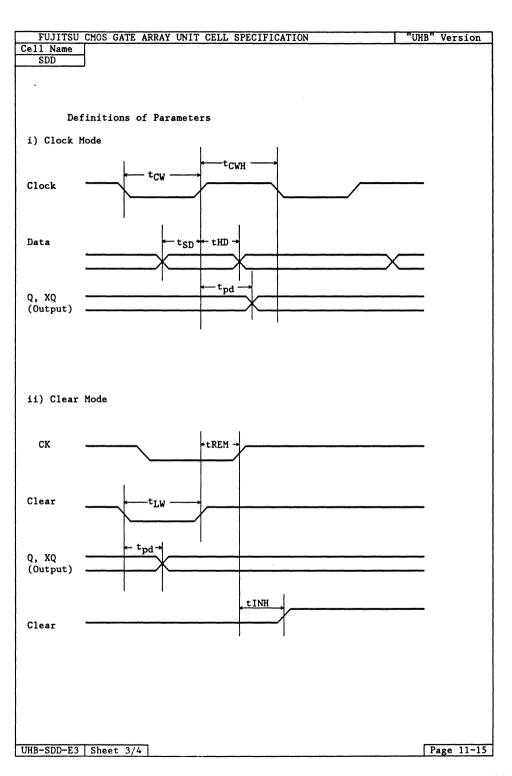
L→H→L H

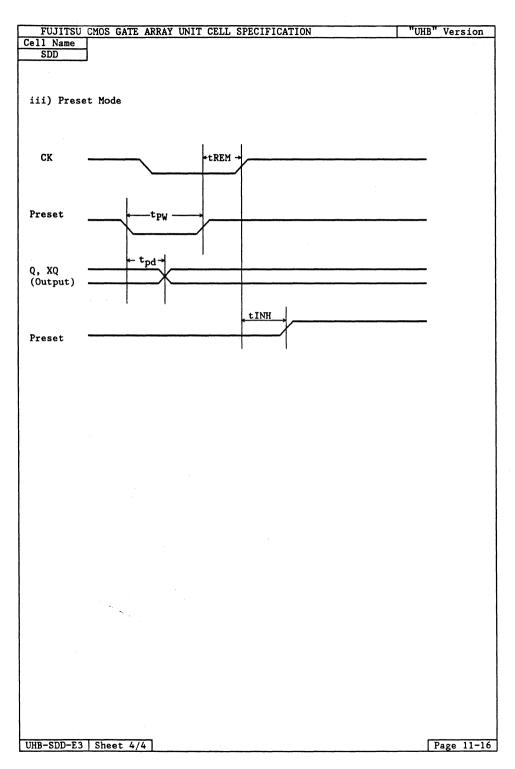
L H→L→H

L

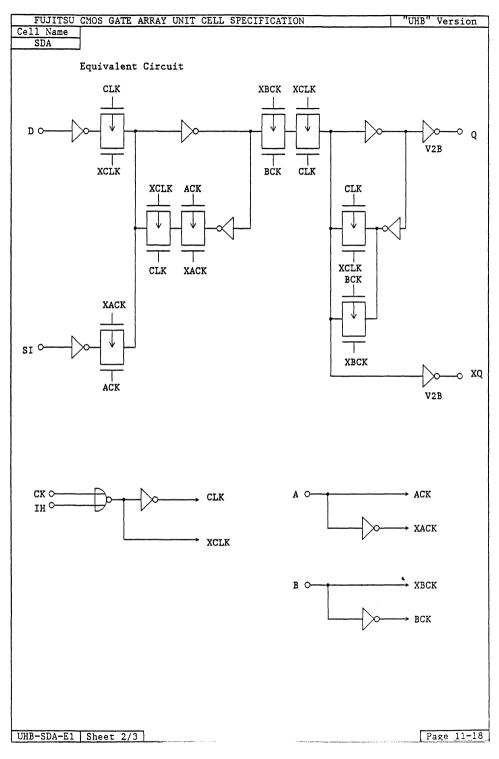
Page 11-13

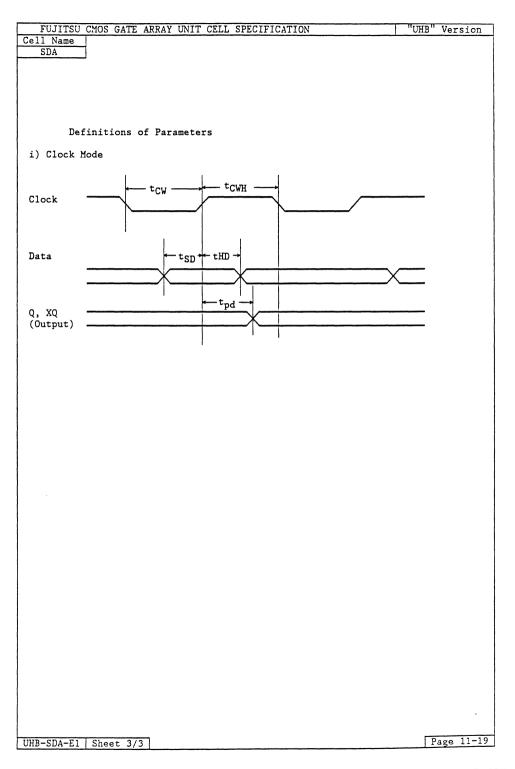




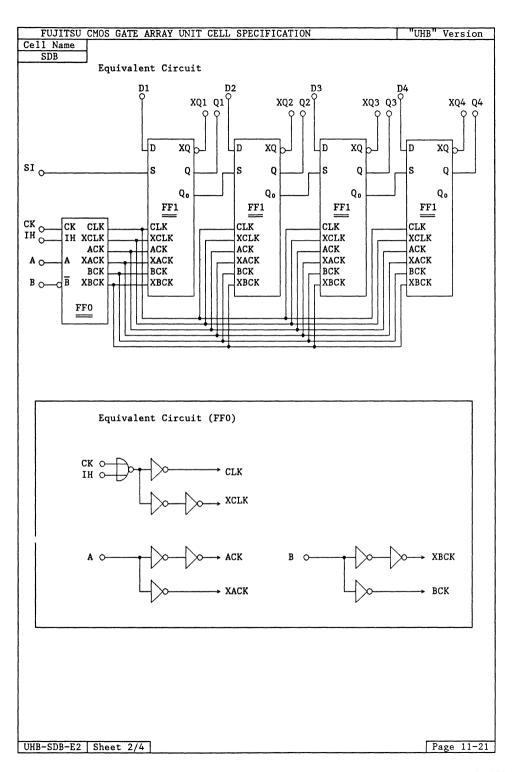


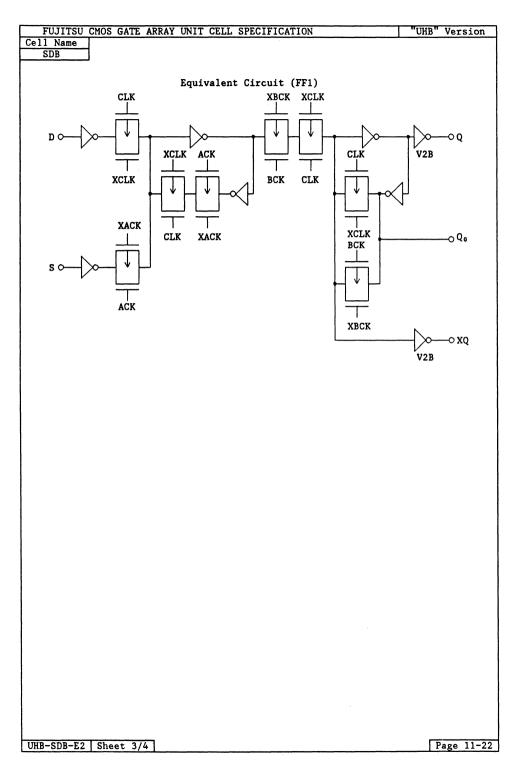
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version Cell Name   Function   Number of BC											
JII Name	1 dilection								+	dimber of bo	
SDA	SCAN 1-	input DF	F with			- <u></u> -				12	
ell Symbol			ļ <u>.</u>		agation			eter		T	
			to	KCL	t0	td KCL	KCL	2   CD	R2	Path	
			3.18	0.08	3.00	0.04	0.0		7	CK, IH → Q	
			2.33	0.08	2.17	0.06	0.1	1	7	CK, IH → XQ	
Г										j	
D		· Q				i i		l			
ск —	γ—	. XQ									
IH —								ł		ł	
SI —				j				- 1			
A B			Parame		<u> </u>	l	ــــــــــــــــــــــــــــــــــــــ	Symb	-1	Tron (mg) if	
• 1				Pulse W	lidth			tCW		Typ(ns)* 5.4	
				Pause T				tCW		4.5	
				etup Ti				tSD		3.5	
			Data F	old Tim	ie			tHD		1.4	
							ĺ				
	Input L										
Pin Name D	Factor 1		1								
CK	1										
IH	1		ļ				1				
SI	1										
A,B	2						1				
							1			1	
	Output									<u> </u>	
Pin Name	Factor			1			1				
Q XQ	3	6 6								ng condition condition	
		•	are	given b	y the m	aximum	delay	mult	ipli	er.	
Function 7	Table										
					1						
MODE		INPUT			OUT	PUT					
	יי עזי		ъ	C.T		vo					
<del>                                     </del>	CLK D	A	В	SI	Q	xQ					
CLOCK	L→H Di	L	L	X	Di	Di					
	H X	L	L	X	Q <sub>0</sub>	XQ <sub>o</sub>					
SCAN	н х	L→H→L	Н	Si	Q.	XQ.					
	**				- 40						
	H X	L	H→L→H	X	Si	Si					
					N-+-	: CLK =	- CV -	L TII			
					моте	. CLK =	- UK 1	TH			
										<u> </u>	
HB-SDA-E1	Sheet 1/	3								Page 11-17	

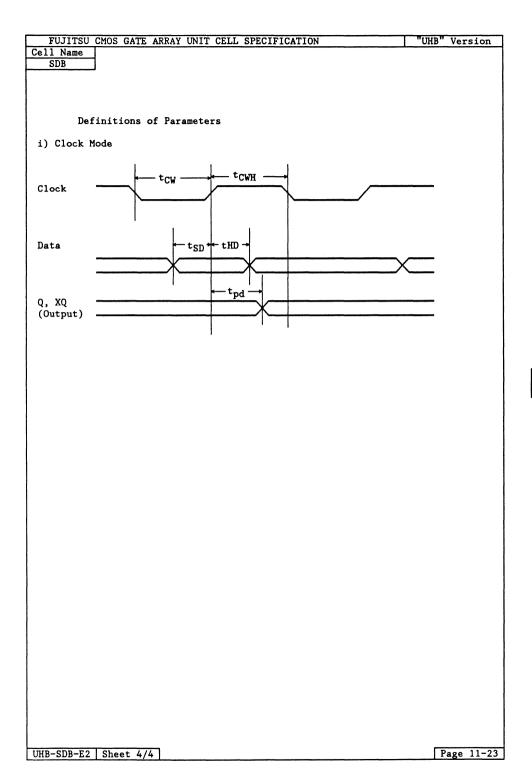




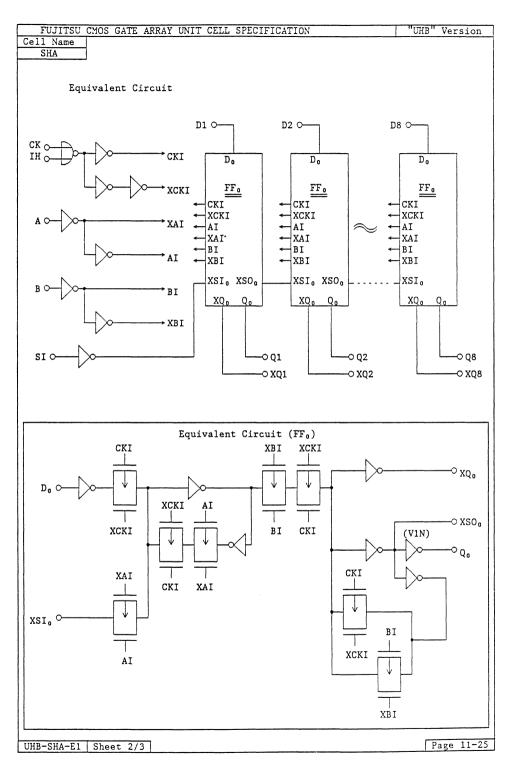
FUJITSU	CMOS	GATE A	ARRAY U	NIT CE	LL SPECI	FICATIO	N		"U	MB" Version
Cell Name	Func									Number of BC
SDB	SCA	N 1-i	nput 4-	bit DF	F with C	lock-In	hibit			42
Cell Symbo	01				Prop	agation	Delay		eter	
				t0	tup   KCL	t0	KCL KCL	n KCL:	2   CDR2	Path
				4.24		3.94	0.04	0.0		CK,IH → Q
			1	3.25	0.08	3.32	0.06	0.1	2 7	CK, IH → XQ
	<u> </u>	1							-	
D1 ———	1	_	Q1 XQ1							
D3	4	<u> </u>	Q2						1	
D4	1	þ—	XQ2						1	
ск —	1	b—	Q3 XQ3						ļ	
IH —	]		Q4	Param					Symbol	Typ(ns)*
A	-	p	XQ4		Pulse W				tCW tCWH	6.8
В ——	9	]		CIOCK	rause 1	TINE			COWII	3.0
					Setup Ti				tSD	2.2
				Data	Hold Tim	e		_	tHD	3.3
	Inn	ut Lo	ading							
Pin Name		tor (								,
D		1						}		
CK IH	į	1 1								
SI		1								
A,B	1	2								
	ı									
	į.							- 1		
	Out	put D	riving	1						
Pin Name		tor (	lu)			_			***************************************	
Q XQ		36 36								ing condition. ing condition
					given b					
Function	Table									
runction	labie									
MODE			TAIDIFF			OTET	'PUT			
NODE			INPUT			001	FUI	$\dashv$		
	CLK	Dn	A	В	SI,Qn-1	Qn	XQn	4		
CLOCK	L→H	Di	L	L	x	Di	$\overline{ exttt{Di}}$			
-25511	**************************************							7		
	H	X	L	L	X	Qn∘	XQn∘	_		
SCAN	Н	Х	L→H→L	Н	Si	Qno	XQn0			
	Н	Х	L	H→L→H	х	Si	Si			
						Note	: CLK =		· IH	
							11 - 1			
IIMB_CDB_E	2   Ch	t 1/4								Page 11-20
UHB-SDB-E	2   Snee	:L 1/4	· L							rage 11-20







FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		יט"	IB" Version Number of BC		
Cell Name	Cell Name Function									
SHA	SCAN 1-input 8-	bit DFF						68		
Cell Symbol				agation	Delay		er			
		t0	up KCL	t0	td KCL	KCL2	CDR2	Path		
		4.72	0.16	4.72	0.09	0.10	4	CK, IH → Q		
D1	Q1	4.12	0.16	4.00	0.13	0.18	4	CK, IH → XQ		
D2	р—— хq1						1			
D3	Q2									
D4	D— XQ2 — Q3									
D6	р xqз									
Д7 ——	Q4						l			
D8	р—— xq4									
	Q5						1			
	D XQ5 Q6									
ск —	р—— XQ6	Parame	ter			1 8	ymbol	Typ(ns)*		
IH —	Q7		Pulse W				tCW	7.2		
SI	р— хо <sub>7</sub>	Clock	Pause T	ime			tCWH	5.5		
А ——	—— Q8 >—— XQ8	Data S	etup Ti	me			tSD	1.8		
<u>_</u>		Data H	old Tim	е			tHD	3.3		
	γ									
Pin Name	Input Loading Factor (lu)	ĺ				- 1				
D D	1									
CK	1									
IH	1	l								
SI A	1	}				l				
В	1									
D: 17	Output Driving									
Pin Name Q	Factor (lu)									
ΧQ	18	* Mini	mum val	ues for	the ty	pical c	perati	ing condition.		
-		The	values	for the	worst	case or	eratir	ng condition		
	L	are	given b	y the m	aximum	delay m	ultipl	ier.		
UHB-SHA-E1	Sheet 1/3							Page 11-24		



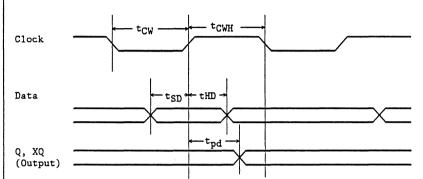
Page 11-26

Cell Name

Definitions of Parameters

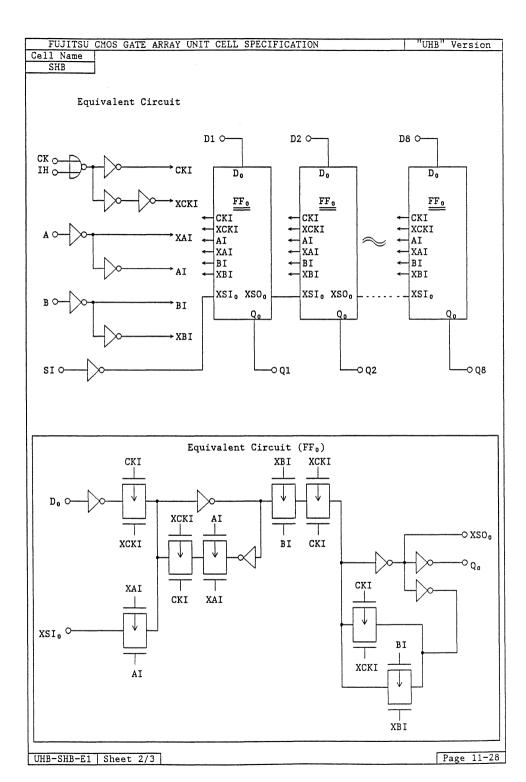
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION

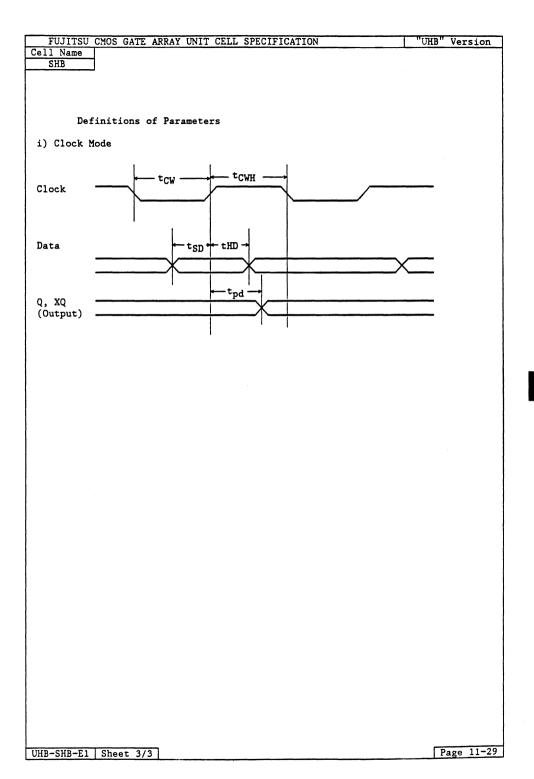
i) Clock Mode



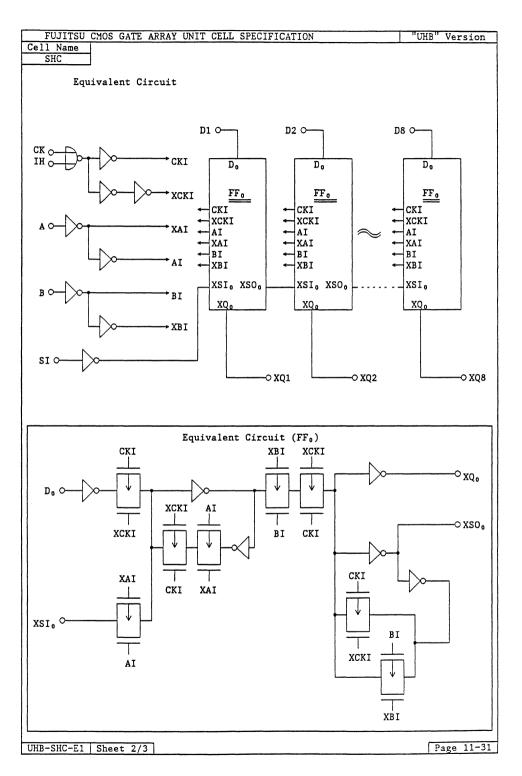
UHB-SHA-E1 | Sheet 3/3

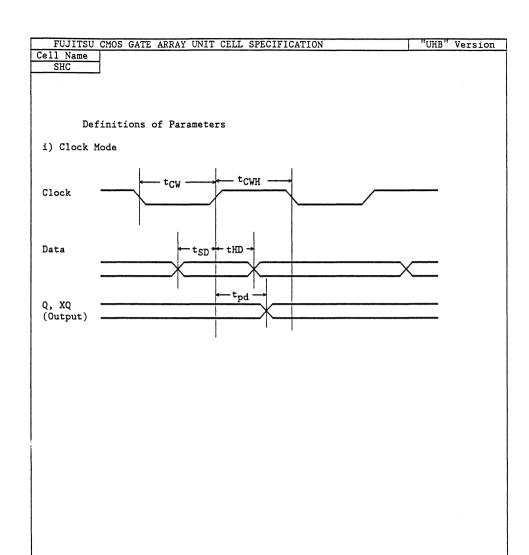
EUTTEU C	MOC CATE ADDAY II	NIT CET	T CDECT	ETCATTO	NT.		1 11777	B" Version
	MOS GATE ARRAY U	NII CEL	L SPECI.	FICATIO	iN .		1 01	Number of BC
		······						
SHB	SCAN 1-input 8-	bit DFF	with C	lock-In	hibit &	Q Out	out	62
Cell Symbol				agation	Delay		er	_,
			up		td			1
		t0 4.32	KCL 0.16	t0 4.42	KCL 0.09	KCL2 0.10	CDR2	Path CK,IH → Q
_		4.32	0.16	4.42	0.09	0.10	4	CK, IR + Q
D1	Q1						1	
D2	- Q2						1	1
D3	—						1	1
D4	Q4							
D5 -	Q5						ł	
D6	Q6						l	
D7 ————————————————————————————————————	Q7							
į.	Q8						]	
ck —								
IH		Parame	ter			1 5	ymbol	Typ(ns)*
SI —		Clock	Pulse W				tCW	7.2
А —— с		Clock	Pause T	ime			tCWH	5.5
" "_								1
		Data S	etup Ti	me			tSD tHD	1.9
		рата Н	old Tim	е			ממז	3.3
	Input Loading							1
Pin Name	Factor (lu)					1		
D	1							
CK	1					- 1		
IH	1					i		
SI	1							
A	1							
В	1					1		
	Output Driving							
Pin Name	Factor (lu)					1		
Q	18							
		* Mini	mum val	ues for	the ty	pical o	perati	ing condition.
		The	values	for the	worst	case of	peratir	g condition
<u> </u>	l	are	given b	y the m	aximum	delay r	nultipl	ier.
UHB-SHB-E1	Sheet 1/3							Page 11-27
DI JI								





FILITCII C	MOS GATE ARRAY U	NIT CET	T CDECT	FICATIO	N7		1 1777	B" Version
	Function	NII CEL	L SPECI	FICATIO	14		1 01	Number of BC
SHC	SCAN 1-input 8-	bit DFF	with C	lock-In	hibit &	XQ Out	put	62
Cell Symbol				agation			er	
			up		td		Larra	٠, .
		t0	KCL	t0	KCL	KCL2		Path
		4.18	0.16	4.10	0.13	0.18	4	CK,IH → XQ
D1	b vo1						]	
D2	P XQ1 P XQ2						ł	
D3	р—— xQ3						1	
D4	р xQ4							
D5	р xQ5						1	
D6	р xQ6							
D7	р—— xq7							
D8	р <del></del> хов							
ск —							1	1
IH —		- B	<u></u>			يبنا		T ( \ ) **
si —		Parame	ter Pulse W	idth			tCW	Typ(ns)* 7.2
A -		Clock	Puise w Pause T	ime			tCWH	5.5
в — о							20.711	1
		Data S	etup Ti old Tim	me			tSD	1.9
		Data H	old Tim	е			tHD	3.3
<b>.</b>	Input Loading					ł		
Pin Name D	Factor (lu)					İ		
CK	1 1							
IH	i					ļ		
SI	i					ł		1
A	Ī					1		
В	1							
						- 1		
Dia Nama	Output Driving	ĺ				- 1		
Pin Name XQ	Factor (lu)					L		
AY	10	* Mini	mum val	ues for	the tv	mical o	perati	ng condition.
	}	The	values	for the	worst	case of	peratir	ng condition
		are	given b	y the m	aximum	delay n	nultipl	ier.
į								
IND OUR DE	2) 1/2							D 11. 20
UHB-SHC-E1	Sheet 1/3							Page 11-30

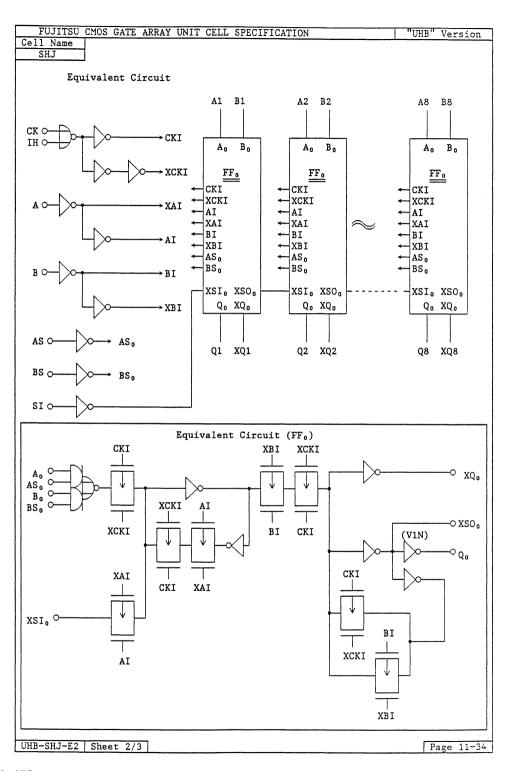


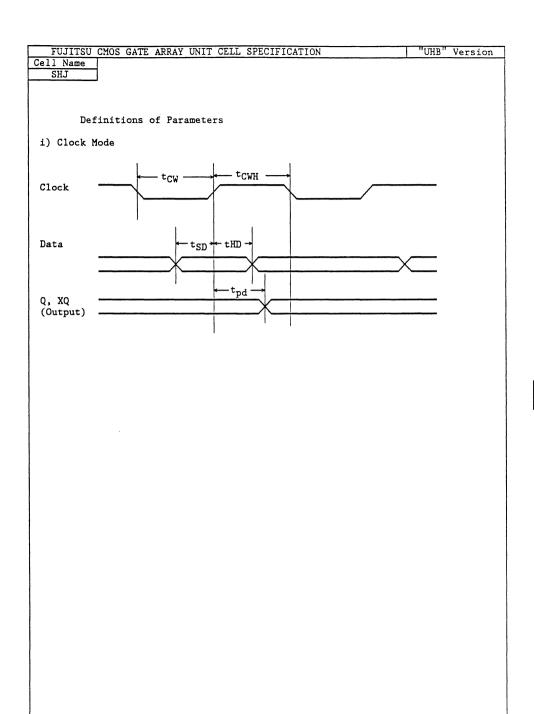


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UHB-SHC-E1 | Sheet 3/3

	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			B" Version
Cell Name	Function SCAN 8-bit DFF	with Cl	ock-Inh	ibit				Number of BC
SHJ	& 2-to-1 Data M			TDIC				78
Cell Symbol				agation	Delay	Paramet	er	
			ир		td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		4.82 4.12	0.16	4.84	0.08	0.12	4	CK, IH → Q CK, IH → XQ
A1	Q1	4.12	0.16	4.00	0.11	0.20	*	CK, IN - AQ
B1 —	⊳ xQ1							
A2	Q2						1	
B2	$\sim \tilde{\chi}_{Q2}$							
A3	—— Q3							
В3 —	р—— xQз							
A4	Q4							
B4 —	0 XQ4						1	
A5 ————————————————————————————————————	Q5 —— XQ5						1	
A6 —	Q6							
В6 ——	> xQ6							
A7	Q7			]				
В7 ——	р—— xq7							
A8	—— Q8							
В8 —	р хов				1			
AS —					1			
BS —								1
CK -								
IH —								1
si —		Parame	ter	<u> </u>	l	1 5	Symbol	Typ(ns)*
A		Clock	Pulse W				tCW	7.2
В — 9_		Clock	Pause T	ime			tCWH	5.5
		Data Setup Time tS						
		Data S	etup Ti	.me			tSD	3.0
		Data H	old Tim	ie			tHD	3.1
·	Input Loading							1
Pin Name	Factor (lu)							
An,Bn	1							
(n=1~8)	_							
AS,BS	1					-		
CK	1					1		
IH	1	1						
SI	1							
A,B	1	}						
<b></b>	Output Driving	1						
Pin Name	Factor (lu)							
Q	18							
XQ	18	* Mini	mum val	lues for	the ty	pical (	operati	ing condition.
		The	values	for the	worst	case of	peratir	ng condition
	L	are	given h	by the m	naximum	delay	nultipl	lier.
1								
UHB-SHJ-E2	Sheet 1/3							Page 11-33
OHD-SHJ-EZ	pueer 1/3							1 - 450 11 00

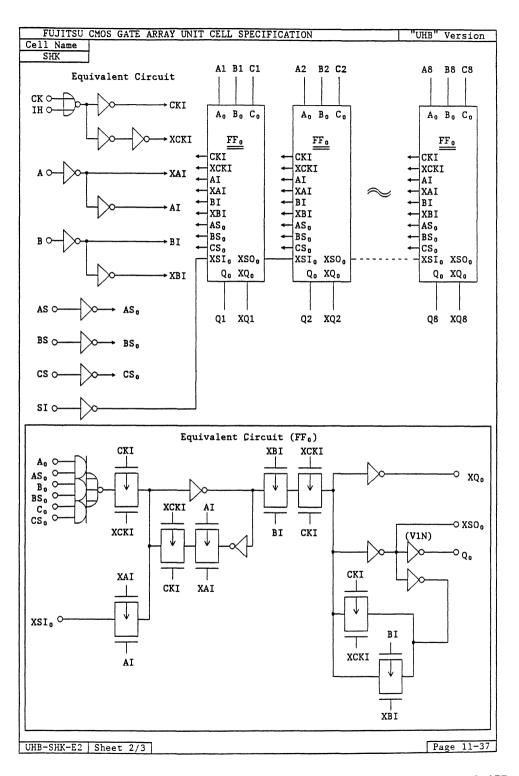


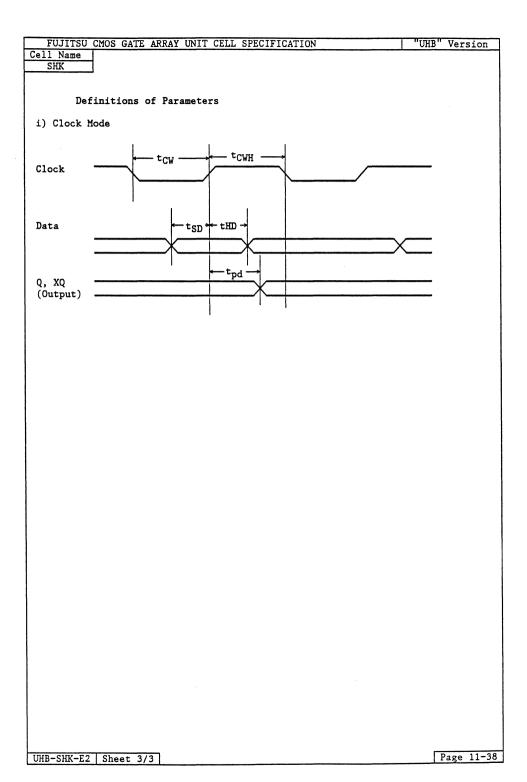


UHB-SHJ-E2 | Sheet 3/3

Page 11-35

Cell Name   F	•			FICATION	. 1		1 01	HB" Version
1	Function Number of BC							
	SCAN 8-bit DFF			ibit				
SHK	& 3-to-1 Data M	ultiple						88
Cell Symbol			Prop	agation	Delay 1	Paramet	er	
			up		tdi			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
A1		4.64	0.16	4.60	0.09	0.10	4	CK, IH → Q
B1	Q1	4.08	0.16	4.00	0.13	0.18	4	CK, IH → XQ
C1	1			1 1				1 '
A2	P xq1			1 1				
B2	Q2			1				
C2	1						l	
A3	P XQ2			1			l	
B3	Q3						İ	
C3	ا د			1				
A4	р—— xqз			į į			1	Į.
	0,						1	
B4	Q4							
C4	Þ xQ4						ļ	
A5	1 1						1	
B5	Q5						1	
C5	⊳ xq5							
A6	1							
B6	Q6						1	1
C6	р xq6						1	
A7							1	
В7	Q7							
C7	□ xq7							
A8	ΛQ/						1	ļ
B8	Q8							
C8	voo						1	į
	Р хов							
AS			[				1	
BS			1					
csq							1	
CK —			1					
IH —		Parame	ter				Symbol	Typ(ns)*
si —		Clock	Pulse W	lidth			tCW	7.2
A		Clock	Pause T	ime			tCWH	5.5
В — ф								
		Data S	etup Ti	me			tSD	3.8
		Data H	old Tim	ne .			tHD	2.9
		· · · · · · · · · · · · · · · · · · ·						1
	Input Loading							
Pin Name	Factor (lu)							
An, Bn, Cn	1							1
(n=1~8)	-					1		1
AS,BS,CS	1					-		1
CK CK	1					l		1
IH	1	1						
SI	1							1
A,B	1					-		1
4,5	•					-		1
	Output Driving	ł						
Pin Name	Factor (lu)							
Q	18	<del> </del>						
xQ	18	1 Min -	mum ***	lues for	the +=	mical	000==+	ing condition.
	10	The	walnee	for the	woret	Lace .	operat	ng condition
1		1110	varues	oy the m	avimum	delaw	mul+in	lier
1	L	are	Riven I	Jy che n	Idatilli	deray	шитетр	1161.
UHB-SHK-E2	Sheet 1/3							Page 11-36





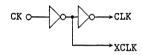
# Non Scan Flip-flop Family

Page	Unit Cell Name	Function	Basic Cells
2-159	FDM	Non-Scan D Flip-flop	6
2-161	FDN	Non-Scan D Flip-flop with Set	7
2-163	FDO	Non-Scan D Flip-flop with Reset	7
2-165	FDP	Non-Scan D Flip-flop with Set and Reset	8
2-168	FDQ	Non-Scan D Flip-flop	21
2-170	FDR	Non-Scan D Flip-flop with Clear	26
2-173	FDS	Non-Scan D Flip-flop	20
2-175	FD2	Non-Scan Power D Flip-flop	7
2-177	FD3	Non-Scan Power D Flip-flop with Preset	8
2-179	FD4	Non-Scan Power D Flip-flop with Clear and Preset	9
2-181	FD5	Non-Scan Power D Flip-flop with Clear	8
2–183	FJD	Non-Scan Positive Edge Clocked Power J-K Flip-flop with Clear	12

	MOS GATE ARRAY ( Function	NIT CELL SPECIFICATION	"U	HB" Version Number of B
FDM	Non-SCAN DFF	Y		6
Cell Symbol		Propagation Delay Par	ameter	
			CL2   CDR2	Path
		1.75 0.16 1.80 0.09	tobb obii	CK → Q
		2.16 0.16 2.36 0.09		CK → XQ
				1
			İ	
				1
				1
D -	Q			
ck			į	
L	p—_ xq		İ	
		Parameter	Symbol	Typ(ns)
		Clock Pulse Width	tCW	4.0
		Clock Pause Time	tCWH	4.0
		Data Setup Time	tSD	2.1
		Data Hold Time	tHD	1.5
	Input Loading	4		
Pin Name	Factor (lu)		į	
D	2	1	l	
CK	1		1	
			i	
			-	
n	Output Driving			
Pin Name	Factor (lu)	4		
Q	18 18			
XQ	10	* Minimum values for the typic	ing condition	
	l	The values for the worst cas	se operati	ng condition
	Ì	are given by the maximum de	lay multip	lier.
Function 7	Table			
Inputs	Outputs			
Imputs	Outputs			
D CK	Q XQ			
Н ↑	H L			
L ↑	LH			
L				
L				

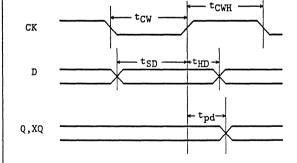
UHB-FDM-E2 | Sheet 1/2

Cell Name FDM



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION

Definition of Parameters



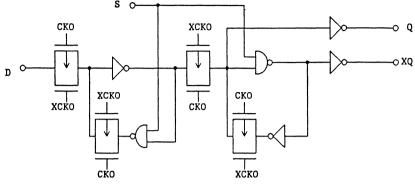
UHB-FDM-E2 | Sheet 2/2

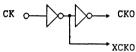
FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		<b>"</b> U	HB" Version	
Cell Name	Function								
FDN	Non-SCAN DFF wi	th SET						7	
Cell Symbol				agation			er		
			up		td				
		t0	KCL	t0	KCL	KCL2	CDR2		
		1.80	0.16	1.75	0.09	0.12	4	CK → Q	
		2.46	0.16	2.42	0.08			CK → XQ	
	S	2.24	0.16	1.07	0.08			$S \rightarrow Q, XQ$	
		1					1		
	$\downarrow$						1		
_ [									
D —	Q					Ì	i		
ск						1	ŀ		
	h	ł				ŀ			
	р— хо						l		
							1		
		Parame	•			ــــــــــــــــــــــــــــــــــــــ	ymbol	Typ(ns)*	
			Pulse W	1.d+h			tCW	4.0	
			Pause T			tCWH	4.0		
		Glock ladse lime						<del></del>	
		Data Setup Time					tSD	2.1	
		Data Hold Time					tHD	1.5	
		- Dava n	010 110				UILD	1	
	Input Loading	Set Pu	lse Wid	th			tSW	4.0	
Pin Name	Factor (lu)		lease T				tREM	0.3	
D	2	Set Ho	ld Time				tINH	3.8	
S	2					]			
CK	1	1				1			
		l				ŀ			
	<u> </u>	l							
	Output Driving	l				ı			
Pin Name	Factor (lu)					1			
Q	18								
ΧQ	18	١	_	_					
								ing condition	
								ng condition	
·	1	are	given b	y the m	aximum	delay n	ultip	lier.	
Function 1	[ablo								

UHB-FDN-E3 | Sheet 1/2

	put				puts
S	D	CK	9	}	XQ
L H H	X H L	X †	H	ł	L L H

Equivalent Circuit

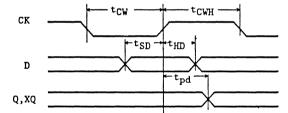




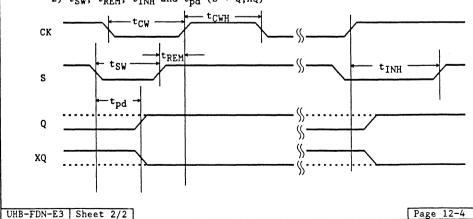
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION

Definition of Parameters

1)  $t_{CW}$ ,  $t_{CWH}$ ,  $t_{SD}$ ,  $t_{HD}$  and  $t_{pd}$  (CK  $\rightarrow$  Q,XQ)



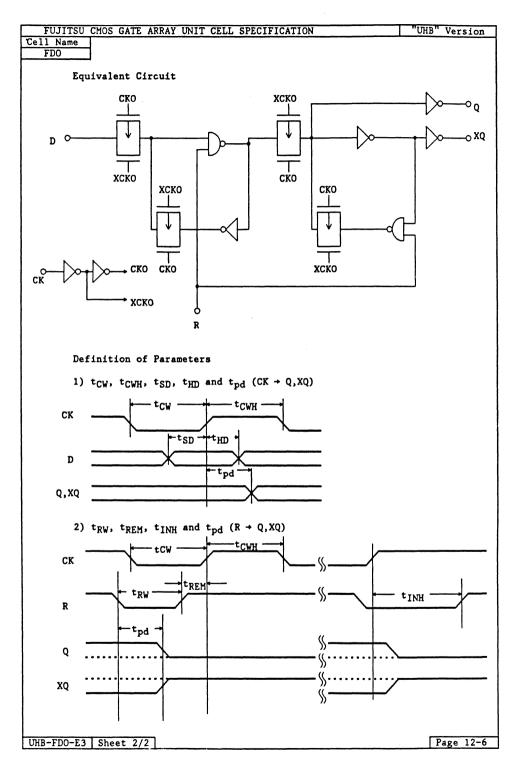
2)  $t_{SW}$ ,  $t_{REM}$ ,  $t_{INH}$  and  $t_{pd}$  (S  $\rightarrow$  Q,XQ)



FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		<b>"</b> U	HB" Version	
Cell Name	Function Number of BC								
FDO	Non-SCAN DFF wi	Non-SCAN DFF with RESET							
Cell Symbol			Prop	agation	Delay	Paramete	er		
		t	up		td	n			
		t0	KCL	t0	KCL	KCL2	CDR2		
		1.93	0.16	1.78	0.10	T T		CK → Q	
		2.16	0.16	2.58	0.09			CK → XQ	
		2.00	0.16	1.64	0.10			$R \rightarrow Q, XQ$	
		'							
D CK	Q								
	р—— <b>х</b> Q								
_									
	R	Parame	+	L	L	<u> </u>	ymbol	Typ(ns)*	
	Л	Clock Pulse Width tCW						4.0	
		Clock Pause Time					tCWH	4.0	
		CIOCK	rause 1	Tille		COMI	4.0		
		Data S	etup Ti	me			tSD	2.1	
							tHD	1.5	
		Data Hold Time						<del> </del>	
	Input Loading	Reset	Pulse W	idth			tRW	4.0	
Pin Name	Factor (lu)		Release		R)		tREM	0.9	
D	2		Hold Ti				tINH	3.3	
R	2								
CK	1	1							
	Output Driving	1							
Pin Name	Factor (lu)								
Q	18	1				]			
χQ	18								
		* Mini	mum val	ues for	the tv	pical of	perat	ing condition.	
								ng condition	
						delay m			

Ir	put	s	Out	puts
R	D	CK	Q	XQ
L H H	X H L	X †	L H L	H L H

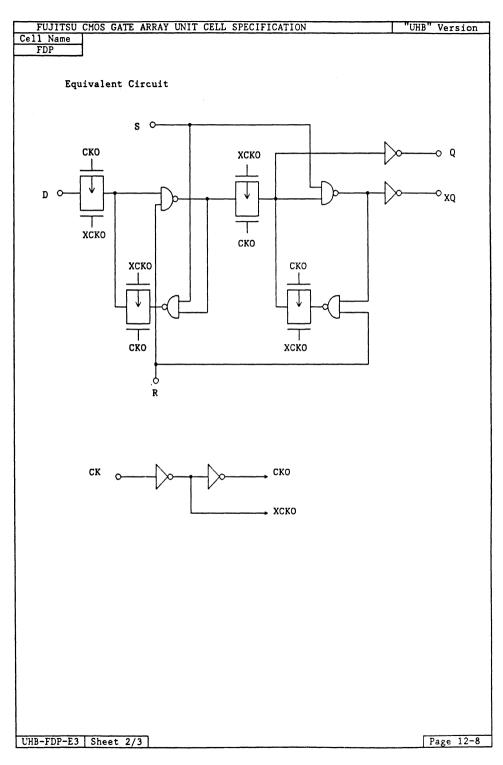
UHB-FD0-E3 | Sheet 1/2

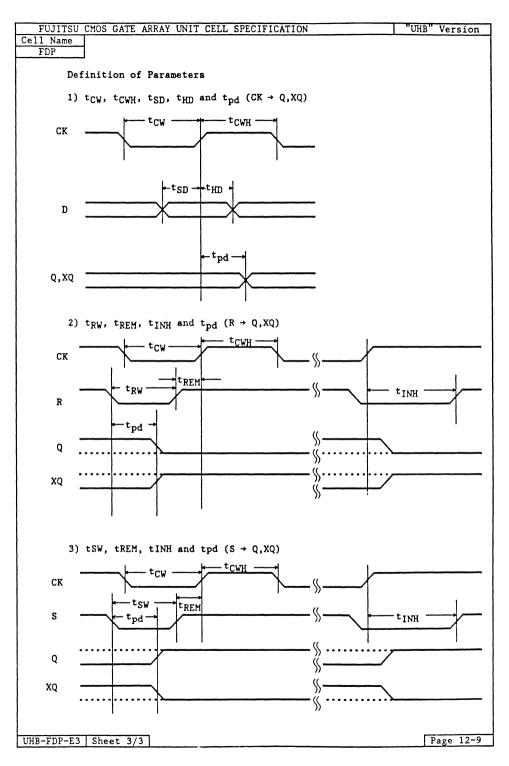


FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		T "U	HB" Version		
	Function Number of BC									
FDP	Non-SCAN DFF wi	th Set	and Res	et				8		
Cell Symbol					Delay	Paramet	er	·		
		t	up		td	n				
		t0	KCL	t0	KCL	KCL2	CDR2			
		1.96	0.16	1.76	0.10			CK → Q		
		2.45	0.16					CK → XQ		
	S	2.24			0.10			$R \rightarrow Q, XQ$		
		2.54	0.16	1.01	0.09			$S \rightarrow Q, XQ$		
	<u> </u>									
. г										
D	Q									
CK		1								
	h									
	р—— <b>х</b> Q									
-	Y									
	R	Parame	ter	L	نــــــا	l s	ymbol	Typ(ns)*		
		Clock Pulse Width tCW						4.0		
		Clock Pause Time tCWH						4.0		
		Data S	etup Ti	me			tSD	2.1		
		Data H	old Tim	e			tHD	1.5		
	Input Loading		lse Wid				tSW	4.0		
Pin Name	Factor (lu)		lease T				tREM	0.3		
D	2	Set Ho	ld Time				tINH	3.8		
S	2									
R	2		Pulse W				tRW	4.0		
CK	1		Release		R)		tREM	0.9		
		Reset	Hold Ti	me			tINH	3.3		
	Output Driving					1				
Pin Name	Factor (lu)	ł								
Q	18							L		
XQ	18	l	_	_						
								ing condition.		
		The values for the worst case operating condition are given by the maximum delay multiplier.								
	1	are	given b	y the m	aximum	delay m	ultip	olier.		

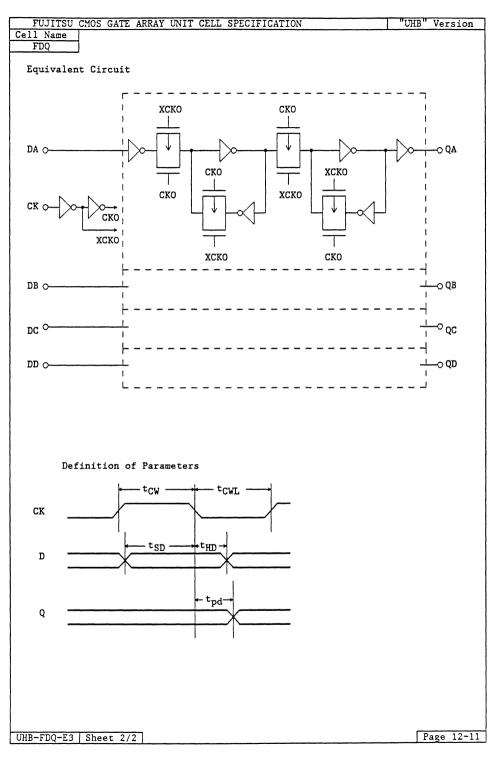
	Inpi	ıts	Outputs	
s	R	D	CK	Q XQ
н	L	X	х	L H
L	H	X	Х	H L
L	L	X	X	Inhibited
н	H	H	<b>†</b>	H L
н	H	L	•	L H
L				<u> </u>

UHB-FDP-E3 | Sheet 1/3





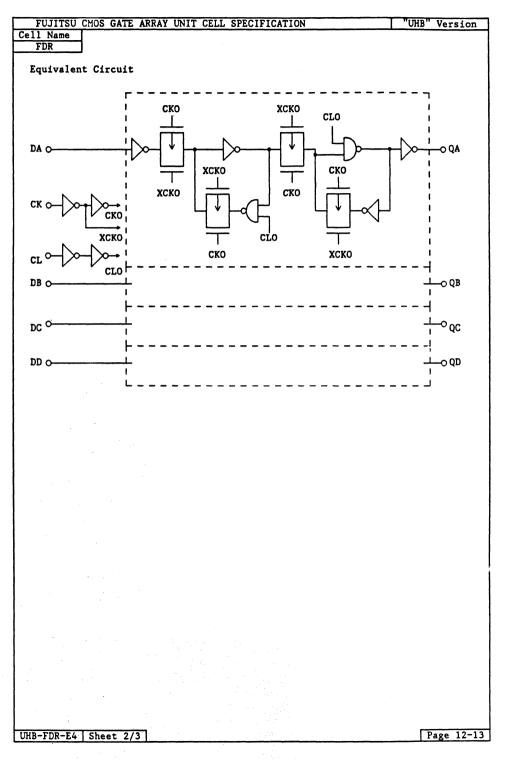
FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			IB" Version
Cell Name	Function		Number of BC					
FDQ	Non-SCAN 4-bit	DEE					İ	21
Cell Symbol		DFF	Prop	agation	Delay	Paramet	er l	21
	<del></del>	t	T					
1		t0	KCL	t0	KCL	KCL2	CDR2	Path
		3.37	0.16	2.74	0.08			CK → Q
DA.	DC						1	
1	B DD							
1								
	QA							
ск —	QB	1						
	QC QC		l				ļ	
<u> </u>	QD QD							
		Parame	ter	L	L	1 5	Symbol	Typ(ns)*
			Pulse W	idth			tCW	4.0
l		Clock	Pause T	ime			tCWL	4.0
		D + 6	<u> </u>				+CD	<del>                                     </del>
		Data B	etup Ti Old Tim	me			tSD tHD	1.1
		Data I	OIG III					
	Input Loading	1						
Pin Name	Factor (lu)					į		
D CK	1	ļ						
O.K								1
		1						
Die Vier	Output Driving							
Pin Name Q	Factor (lu)	ł						1
"	10							
		* Mini	mum val	ues for	the ty	pical o	perat:	ing condition.
		The values for the worst case operating condition are given by the maximum delay multiplier.						
		are	given c	y the m	aximum	delay i	multip.	lier.
Function	Table							
Tanut	10::t=::t							
Input CK D	Output							
<del>  311   2</del>	+							
↓ H	н							
	L							
UHB-FDO-E3	Sheet 1/2							Page 12-10

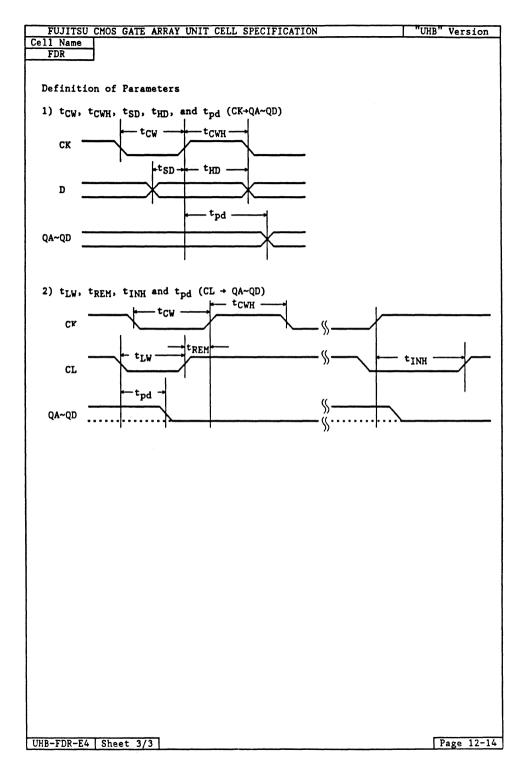


FILITCII	CMOS CA	TE ADDAV II	NIT CEL	T SDECT	FICATIO	N	<u> </u>	1 777	HB" Version	
Cell Name	Function									
		- 11								
FDR	Non-S	CAN 4-bit	DFF wit	OFF with CLEAR						
Cell Symbol				Propagation Delay Parameter						
				up <sup>†</sup>		td				
			t0	KCL	t0	KCL	KCL2	CDR2		
			2.64	0.16	3.62	0.08		1	CK → Q	
DA	D.C.		-	-	2.18	0.08		1	CT → Ø	
	B DD						i	1	1	
ا	ו זיו ז							ł		
							1	1		
		04						1		
İ		— QA — QB						1		
CK —		— Qc							1	
		— QD				i '	1			
L		QD				1				
	Ĭ						l			
			Parame	<u></u>	L	l	<u> </u>	Symbol	T ()*	
	CL			Pulse W	idth			tCW	Typ(ns)* 4.0	
				Pause T			-+	tCWH	4.0	
			020011				-+			
			Data S	etup Ti	me			tSD	1.1	
			Data Hold Time					tHD	2.8	
			Clear Pulse Width tLV							
D/ 11		Loading						tLW	4.0	
Pin Name D	Facto	r (lu)	Clear Release Time tREM Clear Hold Time tINH						1.5	
CK		1	Clear	noid ii	ше		<del></del>	LINA	4.3	
CL		1								
02		•								
							- 1		1	
		t Driving								
Pin Name		r (lu)	l							
Q		18	ļ							
	İ									
	1								ing condition	
				given b						
				0-1011	,					
Function	Table									
Inpu		Output	_							
CK D	CL	Q	4							
	.   ,									
XXX		L L	1							
			1							

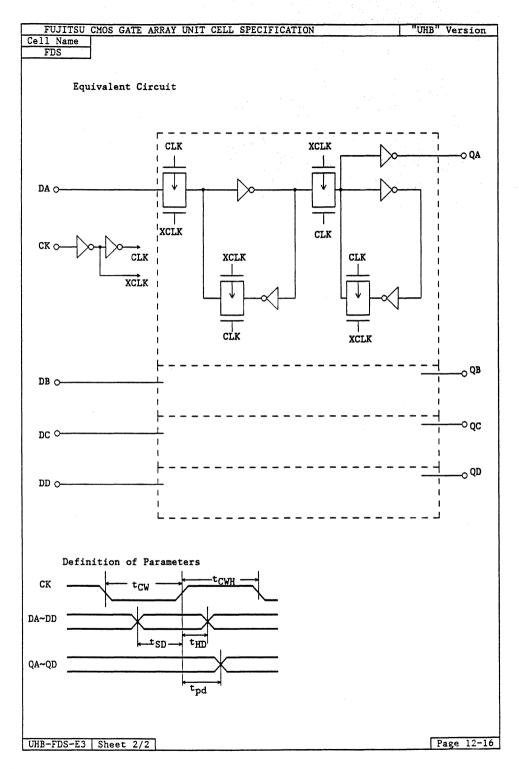
	Output	
D	CL	Q
X L H	L H H	L L H
	X L	X L L H

UHB-FDR-E4 | Sheet 1/3



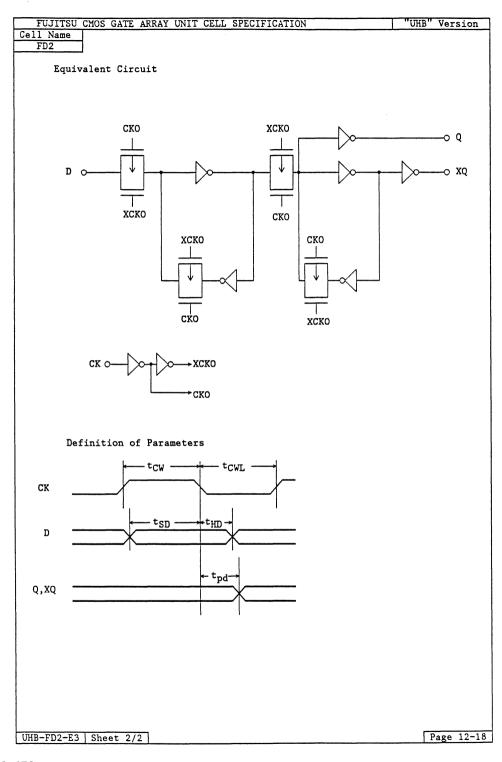


Number of BC	FILITEII C	MOC CATE ADDAY IT	NIT CEL	T CDECT	FICATIO	NI .		וויוי (	B" Version
Propagation Delay Parameter   Tell			NII CEL	L SPECI.	FICATIO	IN .			
Propagation Delay Parameter  tun  tun  to KCL to KCL CDR2  Path  3.03 0.16 2.45 0.09  CK QB  QC  QC  QC  QC  Parameter  Clock Pulse Width  Clock Pause Time  Data Setup Time  Data Hold Time  ThD  ThD  ThD  ThD  ThD  ThD  ThD  Th									
Tup tdn KCL tO KCL KCL2 CDR2 Path 3.03 0.16 2.45 0.09 CK + Q  OR OR OR OR OR OR OR OR OR OR OR OR OR O		Non-SCAN 4-bit	DFF					l	20
DA DB DC DD  QA QB QC QC QD  Parameter Clock Fulse Width Clock Pause Time Clock Pause Time Town Ame Tactor (Lu) Q CK QC CK QC CK QC CK QC CK QC CT CT CT CT CT CT CT CT CT CT CT CT CT	Cell Symbol				agation			ter	
DA DB DC DD  CK QB QB QC QC QC QD  Parameter Clock Pulse Width tCW 4.0 Clock Pause Time tCWH 4.0 Data Setup Time Data Hold Time  THD  CK  1  CK 1  Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Inputs Outputs CK D Q  Outputs CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK + Q  CK					±0			CDR2	- Path
Parameter Symbol Typ(ns)*  Clock Pulse Width tCW 4.0  Clock Pause Time tCWH 4.0  Data Setup Time tSD 1.1  Data Setup Time tHD 2.5  Pin Name Factor (Lu)  Data Hold Time tHD 2.5  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Inputs Outputs  CK D Q								1	
Parameter Symbol Typ(ns)*  Clock Pulse Width tCW 4.0  Clock Pause Time tCWH 4.0  Data Setup Time tSD 1.1  Data Setup Time tHD 2.5  Pin Name Factor (Lu)  Data Hold Time tHD 2.5  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Inputs Outputs  CK D Q	ı								
Parameter Symbol Typ(ns)*  Clock Pulse Width tCW 4.0  Clock Pause Time tSD 1.1  Data Setup Time tSD 1.1  Data Hold Time tHD 2.5  Pin Name Factor (£u)  Q 18  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Inputs Outputs  CK D Q	DA D	B DC DD					i	l	
Parameter Symbol Typ(ns)*  Clock Pulse Width tCW 4.0  Clock Pause Time tSD 1.1  Data Setup Time tSD 1.1  Data Hold Time tHD 2.5  Pin Name Factor (£u)  Q 18  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Inputs Outputs  CK D Q	1	111							
Parameter Symbol Typ(ns)*  Clock Pulse Width tCW 4.0  Clock Pause Time tSD 1.1  Data Setup Time tSD 1.1  Data Hold Time tHD 2.5  Pin Name Factor (£u)  Q 18  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Inputs Outputs  CK D Q									
Parameter Symbol Typ(ns)*  Clock Pulse Width tCW 4.0  Clock Pause Time tSD 1.1  Data Setup Time tSD 1.1  Data Hold Time tHD 2.5  Pin Name Factor (2u)  Q 18  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Inputs Outputs  CK D Q									
Parameter Symbol Typ(ns)*  Clock Pulse Width tCW 4.0  Clock Pause Time tCWH 4.0  Data Setup Time tSD 1.1  Data Hold Time tHD 2.5  Pin Name Factor (Lu)  Q 18  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Inputs Outputs  CK D Q	Cw								
Parameter Symbol Typ(ns)*  Clock Pulse Width tCW 4.0  Clock Pause Time tCWH 4.0  Data Setup Time tSD 1.1  Data Hold Time tHD 2.5  Pin Name Factor (fu)  Data Hold Time thD 2.5  Pin Name Factor (fu)  A minimum values for the typical operating condition the values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Inputs Outputs  CK D Q	CK						1		
Clock Pulse Width tCW 4.0  Clock Pause Time tCWH 4.0  Data Setup Time tSD 1.1  Data Hold Time tHD 2.5  Pin Name Factor (fu)  D 2  CK 1  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Inputs Outputs  CK D Q									
Clock Pulse Width tCW 4.0  Clock Pause Time tCWH 4.0  Data Setup Time tSD 1.1  Data Hold Time tHD 2.5  Pin Name Factor (fu)  D 2  CK 1  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Inputs Outputs  CK D Q							ļ		
Clock Pulse Width tCW 4.0  Clock Pause Time tCWH 4.0  Data Setup Time tSD 1.1  Data Hold Time tHD 2.5  Pin Name Factor (fu)  D 2  CK 1  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Inputs Outputs  CK D Q			Danie				L .	Sumb al	Tum(na)#
Clock Pause Time tCWH 4.0  Data Setup Time tSD 1.1  Data Hold Time tHD 2.5  Pin Name Factor (£u)  CK 1  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Inputs Outputs  CK D Q					idth		<del></del> -		
Data Setup Time tSD 1.1 Data Hold Time tHD 2.5    Data Hold Time tHD 2.5    Data Hold Time tHD 2.5    Data Hold Time tHD 2.5    Data Hold Time tHD 2.5    Data Hold Time tHD 2.5    Data Hold Time tHD 2.5    Data Hold Time tHD 2.5    Data Hold Time tHD 2.5    Data Hold Time tHD 2.5    Data Hold Time tHD 2.5    Data Hold Time tHD 2.5    Data Hold Time tHD 2.5    Data Hold Time tHD 2.5    Data Hold Time tHD 2.5    Data Hold Time tHD 2.5    Data Hold Time tHD 2.5    Data Hold Time tHD 2.5    Data Hold Time tHD 2.5   Data Hold Time tHD 2.5   Data Hold Time tHD 2.5   Data Hold Time tHD 2.5   Data Hold Time tHD 2.5   Data Hold Time tHD 2.5   Data Hold Time tHD 2.5   Data Hold Time tHD 2.5   Data Hold Time tHD 2.5   Data Hold Time tHD 2.5   Data Hold Time tHD 2.5   Data Hold Time tHD 2.5   Data Hold Time tHD 2.5   Data Hold Time tHD 2.5   Data Hold Time tHD 2.5   Data Hold Time tHD 2.5   Data Hold Time tHD 2.5   Data Hold Time tHD 2.5   Data Hold Time tHD 2.5   Data Hold Time tHD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data Hold Time thD 2.5   Data									
Data Hold Time									
Pin Name   Input Loading   Factor (£u)   D									
Pin Name   Factor (lu)   D   2   CK			Data H	old lim	е		-	THU	2.3
Pin Name   Factor (lu)   D   2   CK		Input Loading					- 1		
CK 1  Pin Name Output Driving Factor (Au)  Q 18  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Inputs Outputs  CK D Q		Factor (lu)							
Pin Name Factor (£u)  Q 18  * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Inputs Outputs  CK D Q	_								
Pin Name   Factor (Lu)	CK	1	ĺ						
Pin Name   Factor (Lu)		ļ	1						
Pin Name   Factor (Lu)									
Pin Name   Factor (Lu)		0.1.1.2							
# Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Inputs Outputs CK D Q	Pin Name	Factor ((1))	1						
The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Inputs Outputs  CK D Q		18							į ,
The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table  Inputs Outputs  CK D Q	•								
Function Table  Inputs Outputs  CK D Q			* Mini	mum val	ues for	the ty	pical o	operati	ing condition.
Function Table  Inputs Outputs  CK D Q			ine	values	or the m	WOIST	delaw	peratii multini	ig condition
Inputs Outputs CK D Q		1	are	PTAGIT D	, c.i.e m		-cray		
CK D Q	Function T	Cable							
CK D Q	l	<del></del>							
CK D Q	Inpute	Outputs							
	- inputs								
	CK D	Q							
	† L	L							
	[								
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FUJITSU	CMOS GATE	ARRAY	UNIT CEL	L SPECI	FICATIO	N		ี "บ.	HB" Version
Cell Name	Function								Number of BC
FD2		N Power	DFF						7
Cell Symbol				Prop	agation	Delay		er	
				up		td		,	
			t0	KCL	t0	KCL	KCL2		
			1.65	0.08	1.72	0.05 0.04	0.10	7	CK → Q CK → XQ
D ——C	<b>)</b>	Q XQ							
			Parame	ter Pulse W	idth		S	ymbol tCW	Typ(ns)*
				Pause T				tCW	4.0
				etup Ti				tSD	1.1
			Data H	old Tim	e			tHD	2.4
Pin Name	Input I Factor	(lu)							
CK	1								
Pin Name	Output Factor	Driving (lu)							
Q XQ	36 36	,	Ī						
			The	values	for the	the ty worst aximum	case or	erati	ing conditioning condition lier.
Function	Table								
Inputs		puts							
CK	D Q	XQ							
<b> </b>	H H L L	L H							

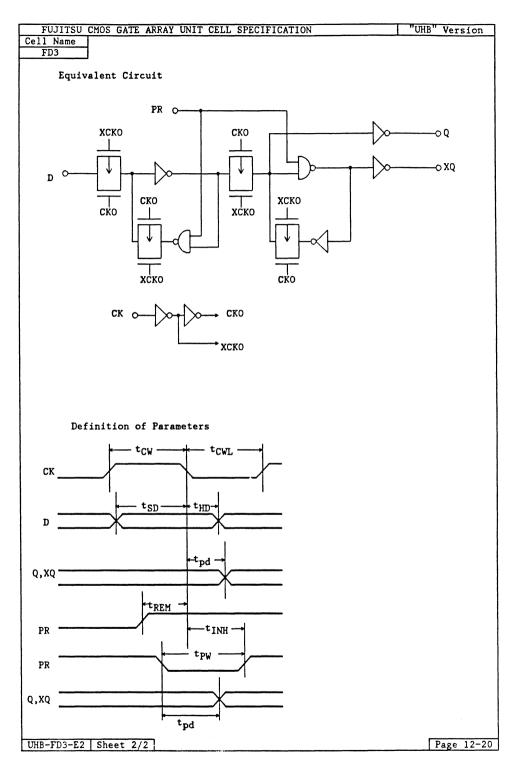
UHB-FD2-E3 | Sheet 1/2



FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N N		<b></b> "u	JHB" Version	
Cell Name	Function							Number of BC	
					-				
FD3	Non-SCAN Power	DFF wit			D. 1	D		8	
Cell Symbol			up Prop	agation	Delay		ter	7	
		to	KCL	t0	KCL	KCL2	T CDR2	Path	
		1.71	0.06	1.73	0.04	0.10			
ł :	PR	2.80	0.06	2.50	0.04	0.07		CK → XQ	
	1	2.39	0.06	0.91	0.04	0.07		PR → Q,XQ	
İ							Ì		
р ——	Q								
		Parame					Symbol	Typ(ns)*	
			Pulse W				tCW	4.0	
		Clock	Pause T	ime			tCWL	4.0	
		Data S	etup Ti	me			tSD	2.1	
			old Tim				tHD	1.5	
								<del></del>	
	Input Loading		Pulse				tPW	4.0	
Pin Name	Factor (lu)		Releas				tREM	0.3	
D	2	Preset	Hold T	ime			tINH	3.8	
CK PR	1 2	İ				1		j	
I I'N	2								
						1			
	Output Driving	1							
Pin Name	Factor (lu)	]				- 1			
Q	36								
XQ	36	l	_	_					
	1	* Minimum values for the typical operating condition.							
		The values for the worst case operating condition are given by the maximum delay multiplier.							
<b></b>	L	1 are	given b	y the m	aximum	deray	multl	JIIEI.	

	Inputs	Outputs				
PR	CK	D	Q	XQ		
L H H	X +	X H L	H H L	L L H		

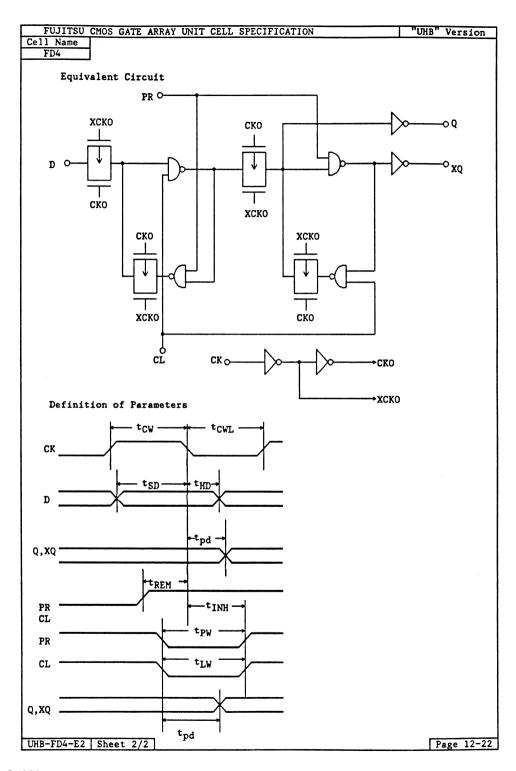
UHB-FD3-E2 | Sheet 1/2



	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"ບ	HB" Version
Cell Name	Function							Number of BC
FD4	Non-SCAN Power	DFF wit						9
Cell Symbol				agation	Delay		eter	
			up		td			
		t0	KCL	t0	KCL	KCL		
		1.90	0.07	1.72	0.05	0.1		CK → Q
	PR	2.81			0.04	0.0		CK → XQ
	1	2.47			0.05	0.1		CL → Q,XQ
	Į.	2.49	0.07	0.92	0.04	0.0	7 7	PR + Q,XQ
	_						1	1
D —	- Q						i	
ск							1	
	L						ı	
	р—— <b>х</b> Q						1	İ
-	Ŷ						1	
							1	1
	CĹ						,	İ
		Parame	<u> </u>				Symbol	Typ(ns)*
			Pulse W	ideb			tCW	4.0
			Pause T				tCWL	4.0
		DIOCK	1 ause 1	THE			COND	<del></del>
		Data S	etup Ti	me			tSD	2.1
			old Tim				tHD	1.5
	Input Loading	Preset	Pulse	Width			tPW	4.0
Pin Name	Factor (lu)	Preset	Releas	e Time			tREM	0.3
D	2	Preset	Hold T	ime			tINH	3.8
CK	1							
CL	2	Clear	Palse W	idth			tLW	4.0
PR	2	Clear	Release	Time			tREM	0.9
		Clear	Hold Ti	me			tINH	3.3
	Output Driving							
Pin Name	Factor (lu)	1				- 1		1
Q	36	1				- 1		
χQ	36							
•	1	* Mini	mum val	ues for	the ty	pical	operat	ing condition
								ng condition
	1				aximum			

		Inp	Out	puts		
I	PR	CL	CK	D	Q	XQ
	L H H H	H L H H	X X +	X H L	H L H L	L H L H

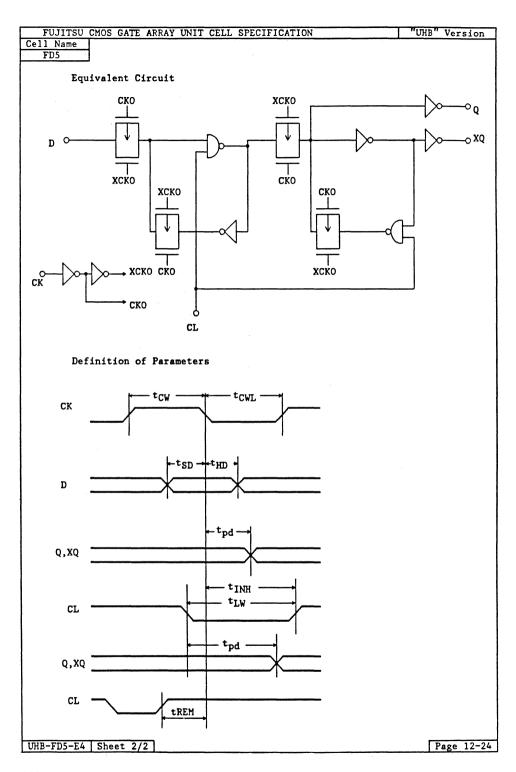
UHB-FD4-E2 | Sheet 1/2



FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			"U	HB" Version
Cell Name	Function								Number of BC
FD5	Non-SCAN Power	DFF wit							8
Cell Symbol				agation			nete:	r	
Į.			up		td				
		t0	KCL	t0	KCL	KCI		CDR2	
		1.88	0.08	1.71	0.05	0.1		7	CK → Q
		2.57	0.08	2.57	0.04	0.0		7	CK → XQ
1		2.36	0.08	1.52	0.05	0.1	10	7	CL → Q,XQ
			İ				- 1		
		1				l			İ
D	├ <b></b> Q					l			j
<b>c</b> k							1		
1	р—— хо					i			Į.
	^^^					l	ı		
	Y					l	- 1		1
1			1			l			- 1
1 .	CL		1			ŀ	- 1		ļ
,	01	Parame	ter			└──	Sv	mbol	Typ(ns)*
1			Pulse W	idth				CW	4.0
l		Clock	Pause T	ime			t	CWL	4.0
ĺ		Data S	etup Ti	me			t	SD	1.1
		Data H	old Tim	е			t	HD	2.4
	Input Loading		Pulse W					LW	4.0
Pin Name	Factor (lu)		Release					REM	1.5
D	2	Clear	Hold Ti	me			t	INH	4.5
CK	1								
CL	2								1
		1				- 1			1
	<u> </u>	i							
l	Output Driving								
Pin Name	Factor (lu)	1				- 1			
Q	36	<u> </u>				1			
XQ	36		1		41. 4				
1	1								ing condition.
	1		values given b						ng condition
	<u> </u>	are	given b	y the m	aximum	de 18	у ши	ıtıp	IIef.

	Input	s	Out	puts
CL	CK	D	0	XQ
L H H	X ↓ ↓	X H L	L H L	H L H

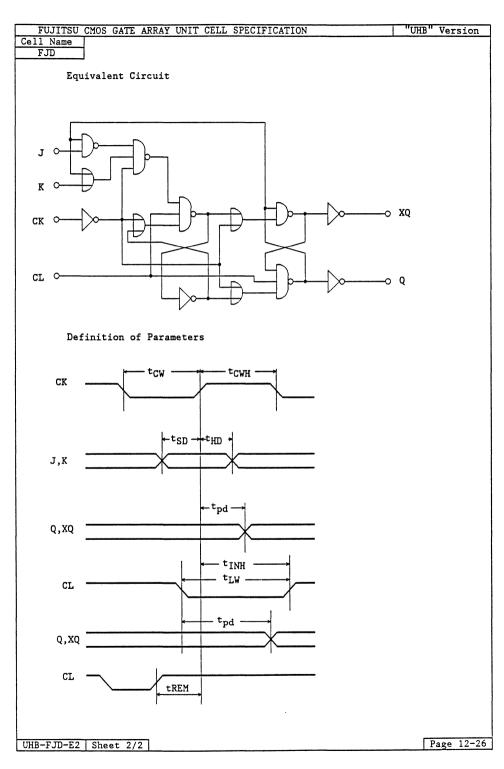
UHB-FD5-E4 | Sheet 1/2



FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		ט" ו	HB" Version
Cell Name	Function							Number of BC
FJD	Non-SCAN Positi	ve edge	clocke	d Power	JKFF w	ith Clo	ear	12
Cell Symbol			Prop	agation	Delay	Parame	ter	
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	
		4.40	0.08	2.96	0.05	0.08	7	CK → Q
		4.43	0.08			0.08		CK → XQ
		2.40	0.08	1.29	0.05	0.08	7	CL → Q,XQ
		1					1	
							1	
							i	
J —	Q						1	
CK —								
к —	x <sub>Q</sub>	ļ					1	
^ L			1					
	Y						1	
							l	
	CL	Parame	ter	L	L	-	Symbol	Typ(ns)*
		Clock	Pulse W	idth			tCW	5.6
		Clock	Pause T	ime			tCWH	5.6
		J,K Se	tup Tim	e			tSD	2.5
		J,K Ho	ld Time				tHD	1.2
	T	ļ						
<b>.</b>	Input Loading		Pulse W				tLW	4.0
Pin Name	Factor (lu)		Release				tREM	2.5
CL	2	Clear	Hold Ti	me			tINH	4.5
J K	1 1					- 1		1
CK	1 1					- 1		
CX	1					- 1		
	Output Driving	1						
Pin Name	Factor (lu)					- 1		
Q	36	i						
χQ	36							
		* Mini	mum val	ues for	the tv	pical	operat	ing condition.
								ing condition
			given b					
	···		<u> </u>					<del></del>

	Inpi	ıts		Outputs
CL	СК	J	ĸ	q xq
L H H H	X † †	X L H H	X L H L	L H Q <sub>0</sub> XQ <sub>0</sub> L H H L XQ <sub>0</sub> Q <sub>0</sub>

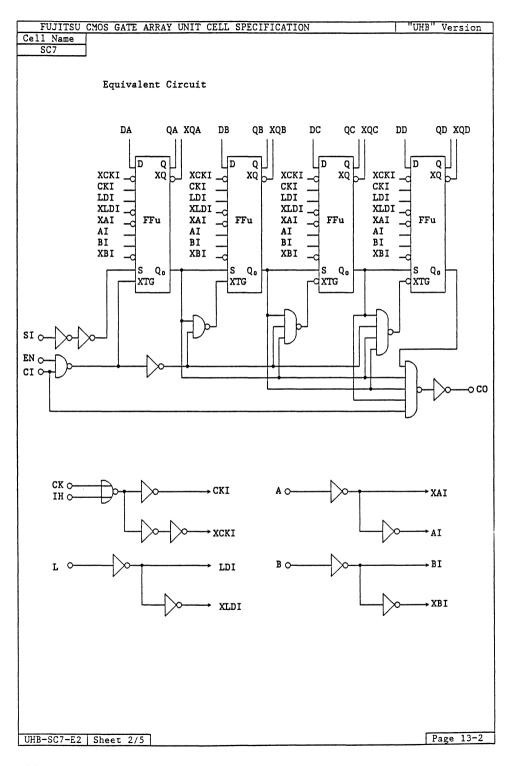
UHB-FJD-E3 | Sheet 1/2

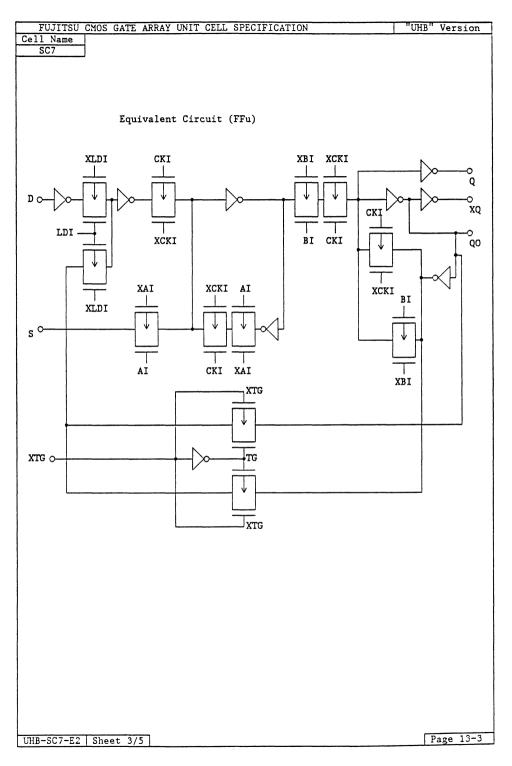


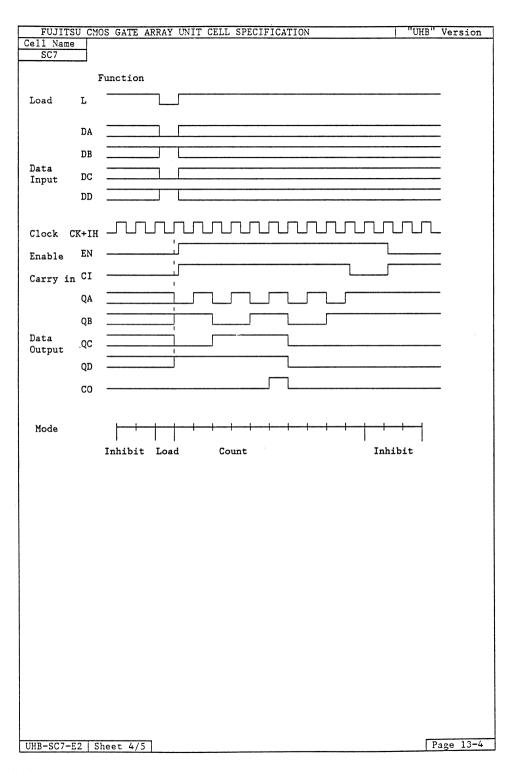
## **Binary Counter Family**

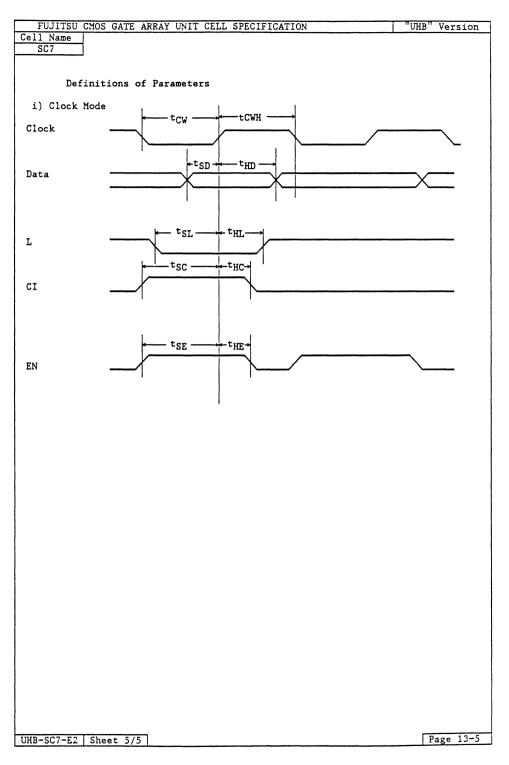
Page	Unit Cell Name	Function	Basic Cells
2–187	SC7	Scan 4-bit Synchronous Binary Up Counter with Parallel Load	62
2–192	SC8	Scan 4-bit Synchronous Binary Down Counter with Parallel Load	66
2–197	C11	Non-Scan Flip-flop for Counter	11
2-199	C41	Non-Scan 4-bit Binary Asynchronous Counter	24
2-202	C42	Non-Scan 4-bit Binary Synchronous Counter	32
2-205	C43	Non-Scan 4-bit Binary Synchronous Up Counter	48
2-209	C45	Non-Scan Binary Synchronous Up Counter	48
2–213	C47	Non-Scan Binary Synchronous Up/Down Counter	68

FUNTION	FULLTSU	MOS GATE ARRAY II	NIT CEL	L SPECT	FICATIO	N			ппн	IB" Version
SCA   SCA   Spite   Symbol   Spine   Start   Symbol   Start   Symbol   Start   Symbol   Start   Symbol   Start   Symbol   Start   Symbol   Start   Symbol   Start   Symbol   Start   Symbol   Start   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   Symbol   S			1111 000	<u> </u>	1 1011110	*1				
SC7		SCAN 4-bit Sync	hronous	Binary						
Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup   Tup		Up Counter with	Parall:	el Load						62
DA	Cell Symbol				agation			neter		
DA										⊣
S,78										
DA										
DA							:	1		CK TH - CO
DB	DA						_		_	
DC	1		2.00	0.00	1.00	0.04				01 , 00
DD	1									
CK	DD —							- 1		
Name	CY									
Parameter   Symbol   Typ(ns)**   Clock Pulse Width   tCW   7.2	1 1									
CI	1 -1						Ĺ,			
Clock Pause Time	1									
Data Setup Time   tSD   2.0	EN —	1								
Data Setup Time	si —	CO	Clock	Pause 1	ıme			t	-WH	1.2
Data Hold Time			Data S	etup Ti	me			+ 9	SD	2.0
Load Setup Time	в — 9									
Load Hold Time										<del></del>
Input Loading			Load S	etup Ti	me					
Pin Name			Load H	old Tim	е			tŀ	IL.	3.6
Pin Name		<del></del>								
D	D4= N									
CK 1 EN Setup Time tSE 7.2  IH 1 1  CI 2  EN 1 1  SI 1  A,B 1 1  Output Driving Factor (flu)  Q 36  XQ 36  CO 36 * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.			CI HOL	u lime				t)	16	2.1
IH 1 1 EN Hold Time tHE 2.7  L 1 1 2 EN 1 1 SI 1 A,B 1 1			EN Set	un Time				+9	SE	7 2
L 1 CI 2 EN 1 SI 1 A,B 1  Output Driving Pin Name Factor (Au)  Q 36 XQ 36 CO 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.			EN Hol	d Time						
EN 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	i i								
SI A,B 1  Output Driving Factor (2u)  Q 36  XQ 36  CO 36 * Minimum values for the typical operating condition The values for the worst case operating condition are given by the maximum delay multiplier.	CI	2								
A,B 1  Output Driving Factor (fu)  Q 36  XQ 36  CO 36 * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	h .	1								
Pin Name Factor (lu)  Q 36  XQ 36  CO 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	t .									
Pin Name Factor (lu)  Q 36 XQ 36 CO 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	A,B	1								
Pin Name Factor (lu)  Q 36 XQ 36 CO 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.		Outros Desirates								
Q 36 XQ 36 CO 36 * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	Pin Name	Factor (011)								
XQ 36 CO 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.										
CO 36 * Minimum values for the typical operating condition.  The values for the worst case operating condition are given by the maximum delay multiplier.							l			
The values for the worst case operating condition are given by the maximum delay multiplier.			* Mini	mum val	ues for	the ty	pica	l ope	erati	ng condition.
			The	values	for the	worst	case	oper	ratin	ng condition
UHB-SC7-E2   Sheet 1/5     Page 13-1		<u> </u>	are	given b	y the m	aximum	dela	y mul	ltipl	ier.
UHB-SC7-E2   Sheet 1/5   Page 13-1										
UHB-SC7-E2   Sheet 1/5     Page 13-1										
UHB-SC7-E2   Sheet 1/5     Page 13-1										
UHB-SC7-E2   Sheet 1/5     Page 13-1										
UHB-SC7-E2   Sheet 1/5     Page 13-1										
UHB-SC7-E2   Sheet 1/5     Page 13-1										
UHB-SC7-E2   Sheet 1/5										
UHB-SC7-E2   Sheet 1/5   Page 13-1										
UHB-SC7-E2   Sheet 1/5   Page 13-1										
UHB-SC7-E2   Sheet 1/5   Page 13-1										
UHB-SC7-E2   Sheet 1/5   Page 13-1										
UHB-SC7-E2   Sheet 1/5   Page 13-1										
UHB-SC7-E2   Sheet 1/5   Page 13-1										
UHB-SC7-E2   Sheet 1/5   Page 13-1										
UHB-SC7-E2   Sheet 1/5   Page 13-1										
UHB-SC7-E2   Sheet 1/5   Page 13-1										
	UHB-SC7-E2	Sheet 1/5								Page 13-1

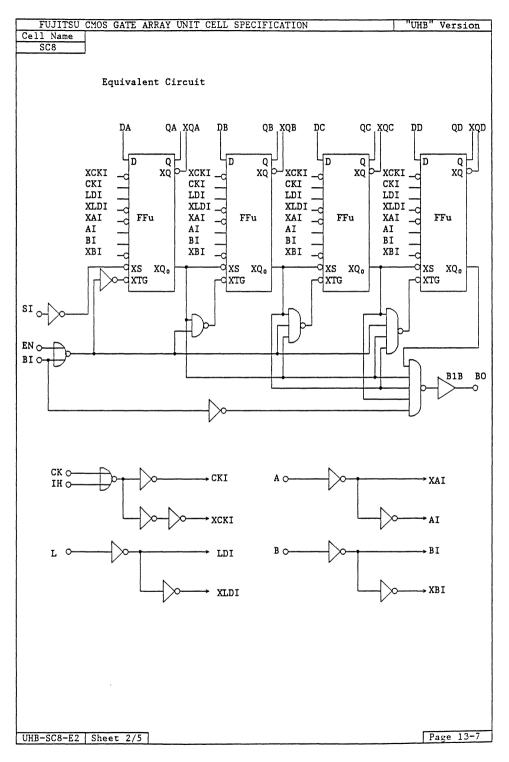


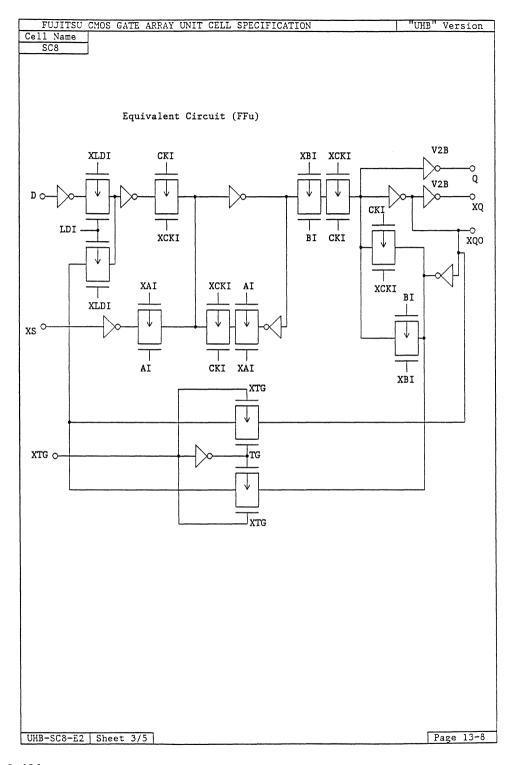


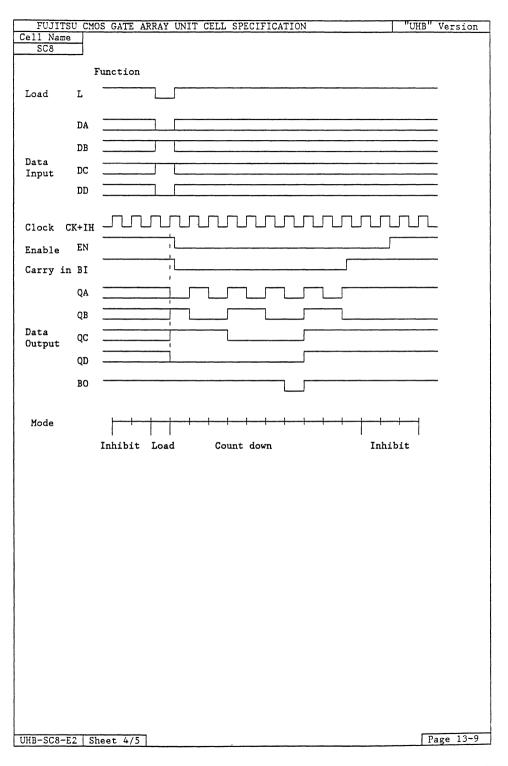


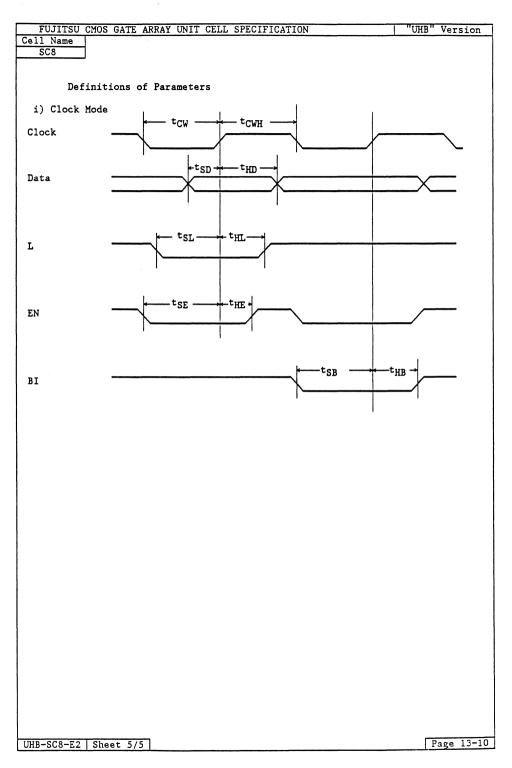


	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		ט"ן	JHB" Version
Cell Name	Function							Number of BC
000	SCAN 4-bit Sync							
SC8	Down Counter wi	th Para	liel Lo	ad				66
Cell Symbol				agation			ter	
			up	+0	td		GDDO	— B
		t0 3.37	KCL 0.07	t0	KCL	KCL2 0.13		$\begin{array}{c c} Path \\ \hline CK, IH \rightarrow Q \end{array}$
				3.18	0.06	0.13	'	
		4.40 6.41	0.06	4.32 8.37	0.04		1	CK, IH → XQ
DA -		1.49	0.08	2.27	0.04		ł	CK, IH → BO BI → BO
DB —	QA	1.49	0.00	2.27	0.04		1	B1 7 B0
DC -	P XQA						1	1
DD	QB						1	
1	р—— xqв							
CK -	QC			1		· ·	1	•
IH —	p xqc						ì	
r — 9	QD	Parame	ter				Symbol	Typ(ns)*
BI — q	р хор		Pulse W	idth		-+	tCW	6.8
EN ——	L		Pause T				tCWH	6.8
SI	р во							
A —		Data S	etup Ti	me			tSD	2.0
В — С			old Tim				tHD	3.3
	*****							
			etup Ti				tSL	6.3
		Load H	old Tim	е			tHL	3.6
	Input Loading	EN Set	up Time				tSE	8.1
Pin Name	Factor (lu)	EN Hol	d Time				tHE	1.8
D	1							
CK	1	BI Set	up Time				tSB	8.1
IH	1	BI Hol	d Time				tHB	1.8
L	1							
BI	2							
EN	1					- 1		
SI	1							
A,B	1							
	Out to Division							
D/- 11	Output Driving							
Pin Name	Factor (lu)							
Q XQ	36 36	ļ						
BO	36	* Mini	m11m 77.01	nes for	the to	nice1	onero+	ing condition.
	]							ing condition.
				y the m				
	1		<u> </u>					
1								
1								
1								
1								
1								
1								
1								
1								
	<u> </u>							D 12 (
UHB-SC8-E2	Sheet 1/5							Page 13-6





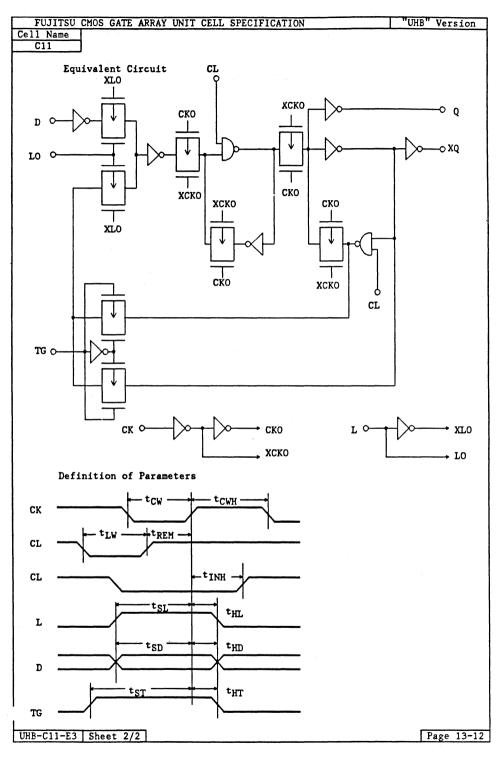




FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		ט" ו	HB" Version			
Cell Name	Function							Number of BC			
C11	Non-SCAN Flip-F	lop for	Counte	r				11			
Cell Symbol					Delay	Paramet	er				
		t	up		td	n					
		t0	KCL	t0	KCL	KCL2	CDR2				
		1.90	0.16	1.75	0.10			CK → Q			
		2.53	0.16				ĺ	CK → XQ			
		2.62	0.16	1.73	0.10	İ	1	CL + Q,XQ			
١ ٢		1		Ì	1						
D —											
L —	├─ <b>-</b> Q	!					l				
		l			1						
							l				
CK —				l	i			]			
		ļ		1							
TG -	р—— <b>х</b> о	j		1							
_	<del>-</del>	Parameter Sym						Typ(ns)#			
		Clock Pulse Width to						4.0			
	CL	Clock Pause Time tCV						4.2			
	02										
		Clear	Pulse W	idth			tLW	4.0			
			Release				tREM	1.0			
	<del></del>	Clear	Hold Ti	me			tINH	0.5			
	Input Loading	<u> </u>									
Pin Name	Factor (lu)		etup Ti		CK)		tSL	2.3			
L	2	Load H	old Tim	<u>ie (</u>	CK)		tHL	0.5			
TG	2	<u> </u>			61//						
CL	2		etup Ti		CK)		tSD	2.5			
D,CK	1	Data H	old Tim	ie (	CK)		tHD	0.5			
	Output Driving	77C C-4	77/	<del>,</del>	CK)		tST	2.9			
Pin Name			up Time d Time	tHT	0.0						
	Factor (lu)	10 101	+ 0.0								
Q XQ	18										
ΛŲ	10	+ M:	m.,m ,,_1	fa-	+ha +	mical -		ing condition			
		* Minimum values for the typical operating condition.  The values for the worst case operating condition									
	.1	are	Fineu p	y the m	aximum	GETAN E	ultip	ilel.			

L	а	TG	CL	СК	Q(Q <sub>0</sub> )
х	Х	Х	L	х	L
н	Н	х	н	+	н
н	L	x	н	+	L
L	x	L	н	+	Q(Q <sub>0</sub> )
L	x	н	н	+	$\overline{\mathbb{Q}}(\overline{\mathbb{Q}_{\theta}})$

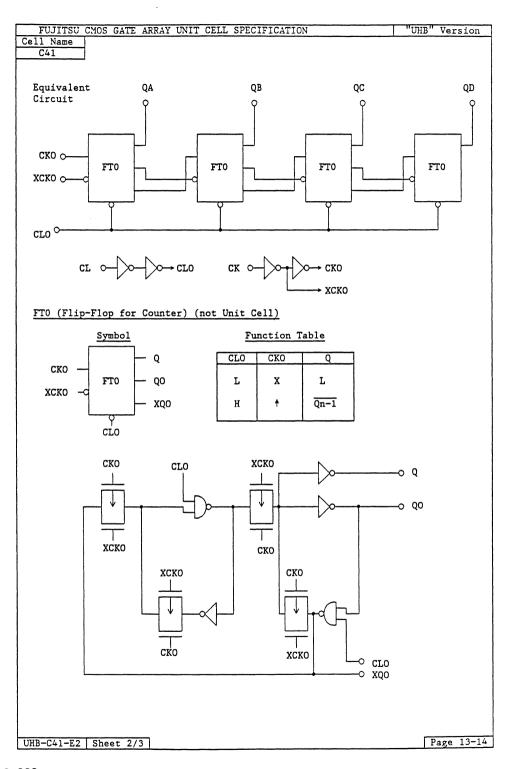
UHB-C11-E3 | Sheet 1/2

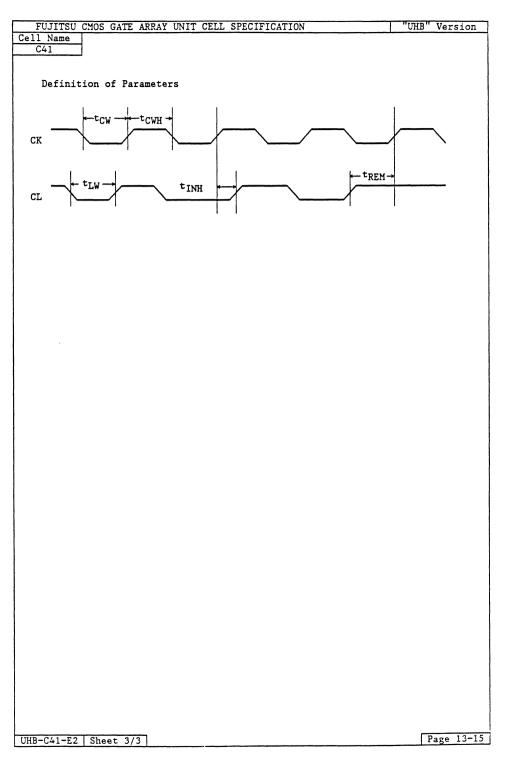


FULLTSU	CMOS GATE ARRAY U	NIT CEL	T. SPECT	FICATIO	NI .		1 11	HB" Version		
Cell Name	Function	TIT OLL	D 01 101	TICATIO	.,			Number of BC		
C41	Non-SCAN 4-bit	Binary						24		
Cell Symbol				agation			er			
			up		td					
ļ		t0 2.00	KCL 0.14	t0	KCL	KCL2	CDR2			
				1.86	0.10	-	-	CK → QA		
		3.67	0.14		0.10	-	-	CK → QB		
1		5.13	0.14		0.10	-	-	CK → QC		
1		6.60	0.14	6.20	0.10	-	-	CK → QD		
l r		-	-	4.19	0.10	-	-	CL → Q		
	QA									
1	├── QB									
	— QC									
1	— QD						ļ			
ck —	1									
011							i			
1	ļ	j					ì			
		Parame	ter			l s	vmbol	Typ(ns)*		
1	Ĭ	Clock Pulse Width					tCW	4.3		
	1	Clock Pause Time					tCWH	4.6		
	CL									
			Pulse W				tLW	3.9		
			Release				tREM	2.1		
	Input Loading	Clear	Hold Ti	me			tINH	6.7		
Pin Name	Factor (lu)	1				1				
CK	1	1				- 1				
CL	1					1				
1	1	l						1		
1	ļ	1				1				
								1		
	Output Driving	1						1		
Pin Name	Factor (lu)	1								
Q	18	1				-		1		
,										
* Minimum values for the typical operating condition										
	The values for the worst case operating condition									
	are given by the maximum delay multiplier.									
<b></b>	are given by the maximum delay multiplier.									

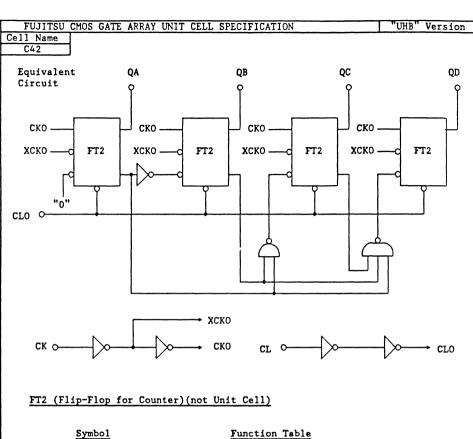
Inp	uts	Outputs				
CL	CK	Q				
H L	† X	Count up L				

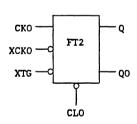
UHB-C41-E2 | Sheet 1/3





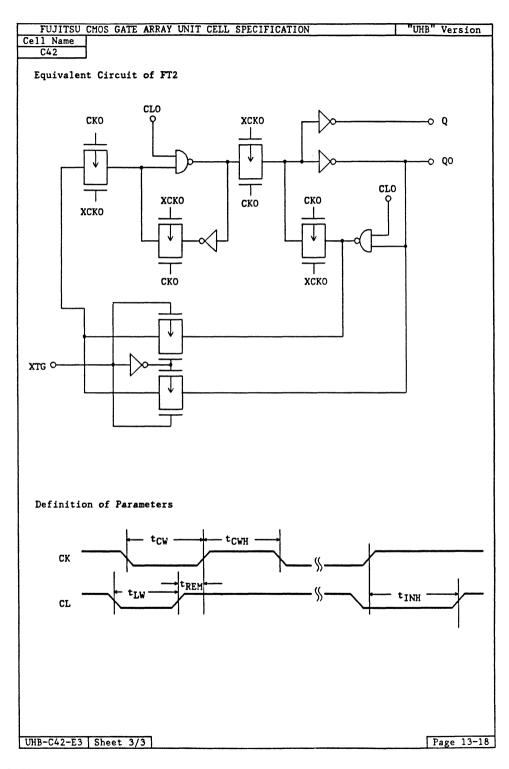
FILITSILO	MOS GATE ARRAY U	NIT CEL	I SDECT	FICATIO	NI.		T "ITH	B" Version		
Cell Name	Function	DIVIT CLL	L BILCI	FICATIO			1 011	Number of BC		
C42	Non-SCAN 4-bit	Binary	Synchro	nous Co	unter	D		32		
Cell Symbol		├	up	agation	Delay td		er			
		to	KCL	t0	KCL	KCL2	CDR2	Path		
		3.18	0.14	2.34	0.09	0.12	4	CK → Q		
		-	-	3.36	0.09	0.12	4	CL → Q		
_							}			
	QA						l			
	QB						1			
	QC									
CV	QD	1					1			
ск —										
		L								
_	<del></del>	Parame					ymbol	Typ(ns)*		
		Clock	Pulse W Pause T	inc			tCW tCWH	4.3		
	CL	CTOCK	iause I	1111E		-+	LUWN	+ *.0		
		Clear	Pulse W	idth			tLW	4.0		
			Release				tREM	2.1		
Din Nama	Input Loading	Clear	Hold Ti	me			tINH	6.7		
Pin Name CL	Factor (lu)	1								
CK	ī	1				ı		1		
						ļ				
	Output Driving	4								
Pin Name	Factor (lu)							1		
Q	18	1								
				_	-					
		* Mini	imum val	ues for	the ty	pical c	perati	ng condition.		
		are	The values for the worst case operating condition are given by the maximum delay multiplier.							
		1 216	02.011	,c m						
Function T	Table									
Tacuta	Outmut									
Inputs CL CK	Outputs Q									
<del>  </del>										
Н 🛉	Count up									
LX	L									
IND CO FO	Chast 1/2							Page 12-16		
UHB-C42-E3	Sheet 1/3							Page 13-16		





	Inputs CLO   XTG   CKO								
CLO	XTG	Q(Q0)							
L	x	х	L						
н	н	<b>†</b>	Qn-1						
н	L	†	Qn−1						

UHB-C42-E3 | Sheet 2/3 Page 13-17

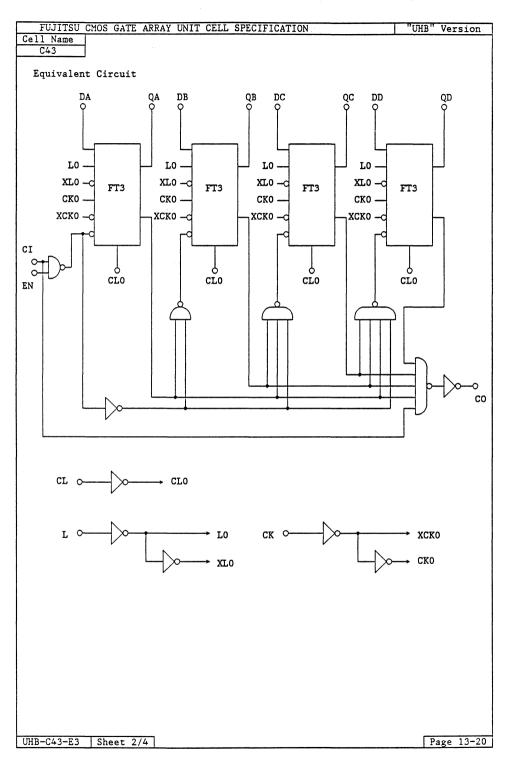


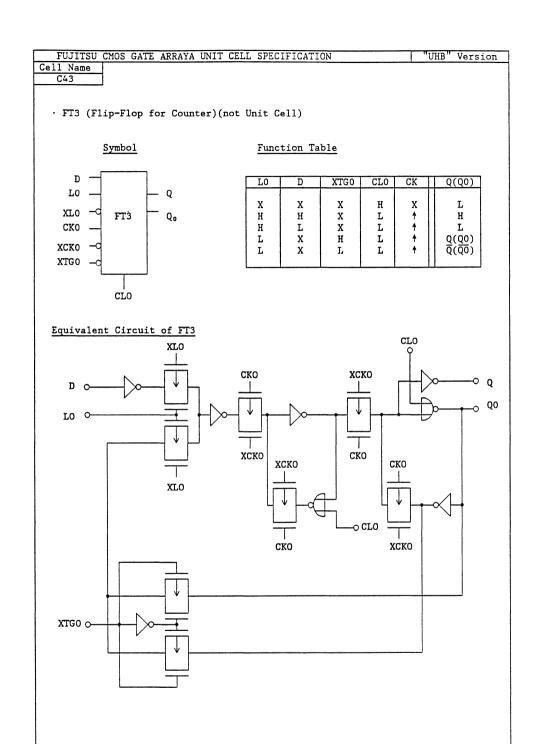
FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		<b>"</b> U	HB" Version	
Cell Name	Function							Number of BC	
C43	Non-SCAN 4-bit	Binary						48	
Cell Symbol				agation	Delay		eī		
i			up		td				
		t0	KCL	t0	KCL	KCL2	CDR2		
ĺ		2.96	0.16	2.40	0.09			CK → Q	
	5.60	0.16	3.56	0.08			CK → CO		
		1.60	0.16	0.81	0.08			CI → CO	
			-	3.88	0.09			CL → Q	
l г	<del></del>	-	-	2.64	0.08			Cr → co	
DA — QA — QB — QC — QC — QD — QD — CK — EN — CO — CO		Clock Data S	Pulse W Pause T etup Ti	idth ime me			ymbol tCW tCWH	Typ(ns)* 4.7 6.7 2.6	
			old Tim				tHD	2.9	
			etup Ti				tSL	4.4	
l	Input Loading		old Tim				tHL	1.3	
Pin Name	Factor (lu)		up Time				tSC	4.3	
D	1	CI Hol					tHC	0.9	
L,EN	1		up Time				tSE	4.3	
CK,CL	1	EN Hol					tHE	0.9	
CI	2		Pulse W				tLW	5.6	
	I	Clear Release Time tREM						1.9	
	Output Driving	Clear Hold Time tINH						8.3	
Pin Name	Factor (lu)	1							
Q	18								
CO	18	* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							

		Outputs				
CL	L	D	Q			
L H H H H	X L H H	X H L X X	X X X X L H	X X X L X H	X † * X X	L H L No Counting No Counting Count up

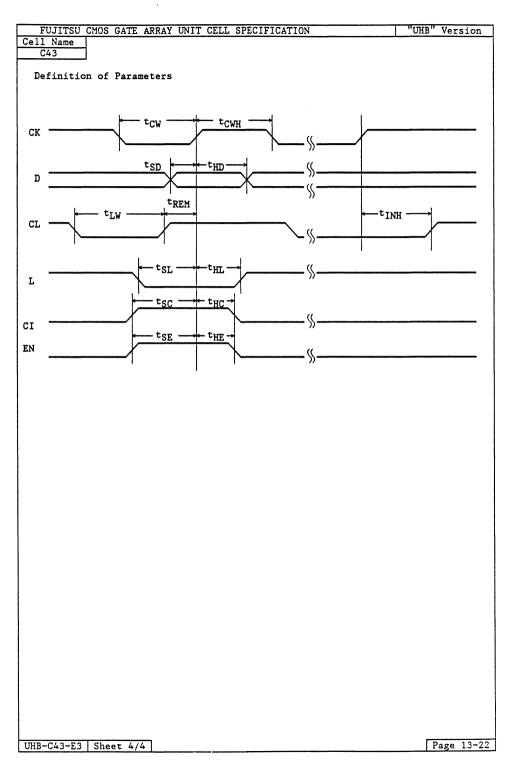
Note: The CO output produces a high level output data when the counter overflows.

UHB-C43-E3 Sheet 1/4





UHB-C43-E3 | Sheet 3/4

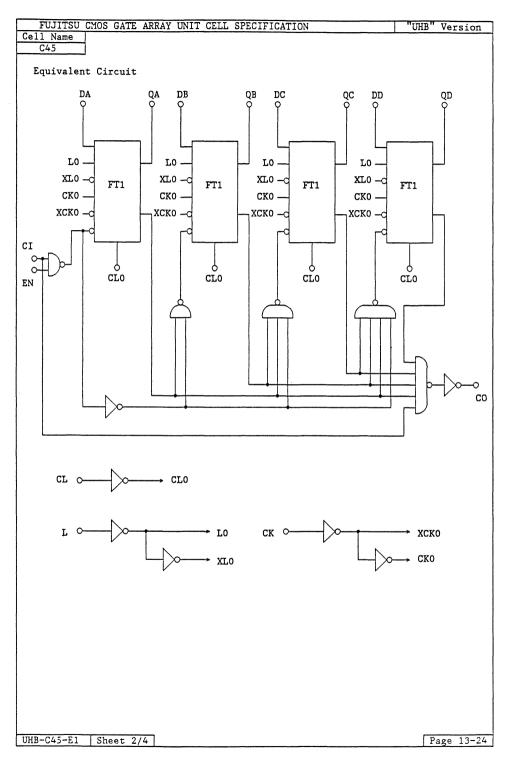


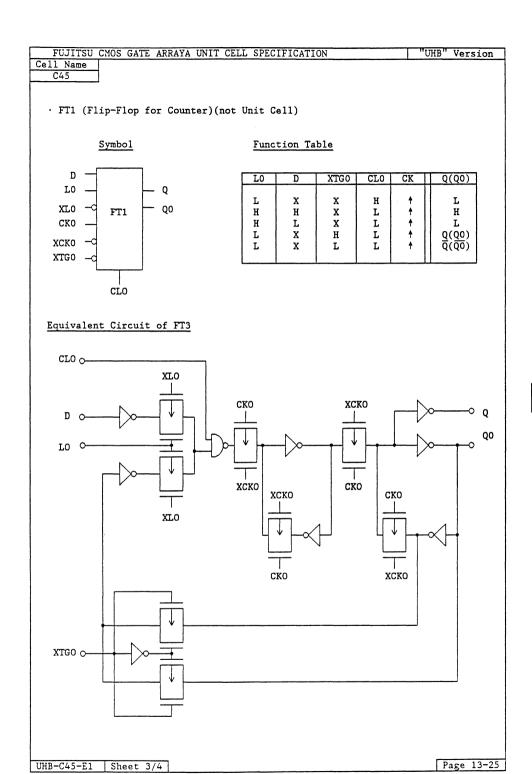
FUJITSU (	CMOS GATE ARRAY U	NIT CEL	I. SPECI	FICATIO	N		1111	HB" Version	
Cell Name	Function	.,,,,	D DIDGI	11011110				Number of BC	
								THE DOLL OF DO	
C45	Non-SCAN 4-bit	Binary	Synchro	nous Up	Counte	r		48	
Cell Symbol			Prop	agation	Delay	Paramet	er		
		t	up						
		t0	KCL	t0	KCL	KCL2	CDR2	Path	
		2.67	0.14	1.87	0.09	0.13	4	CK → Q	
				2.82	0.09		1	CK → CO	
		1.91	0.17	1.36	0.09		1	CI → CO	
							ł		
1 -							1		
DA -	QA		1				1		
DB -	QB								
DC -	—— QC		ł				1	1	
	QD		1				-		
r —d							1		
CK -							1	1	
EN -			1				1		
CI —	со		!				1		
-	<del></del>	Parame	ter			1 5	ymbol	Typ(ns)*	
		Clock Pulse Width					tCW	4.0	
	CL	Clock	Pause T	ime			tCWH	4.6	
	CL		etup Ti				tSD	3.8	
			old Tim				tHD	2.1	
			etup Ti				tSL	5.0	
	Input Loading		old Tim				tHL	2.1	
Pin Name	Factor (lu)		up Time				tSC	6.6	
D	1		d Time				tHC	1.9	
L,EN	1		up Time				tSE	6.6	
CK,CL	1		d Time				tHE	1.9	
CI	2		Setup T				tSR	3.8	
	<del> </del>	Clear	Hold Ti	me			tHR	2.0	
1	Output Driving					1			
Pin Name	Factor (lu)					1			
Q	18								
co	18	* Minimum values for the typical operating condition.							
		The values for the worst case operating condition are given by the maximum delay multiplier.							
	1	are	given b	y the m	axımum	delay r	ultip	lier.	

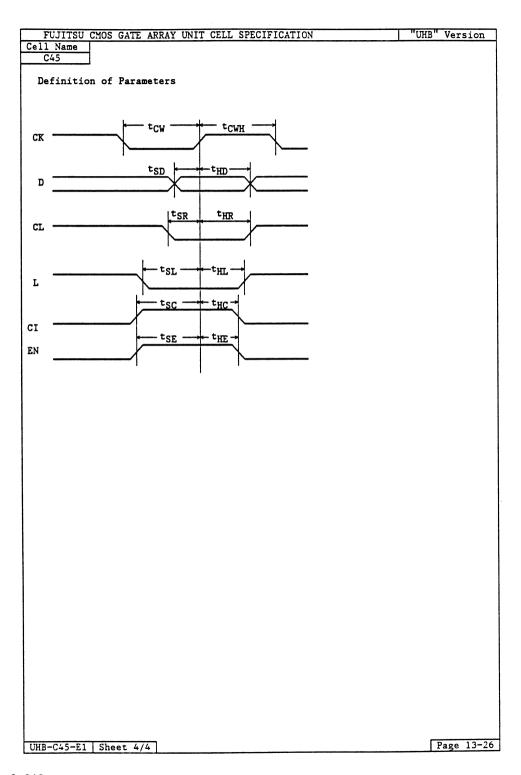
		Outputs				
C	L	D	Q			
L H H H	X L H H	X H L X X	X X X X L	X X X L X	† † X X	L H L No Counting No Counting Count up

Note: The CO output produces a high level output data when the counter overflows.

UHB-C45-E1 | Sheet 1/4





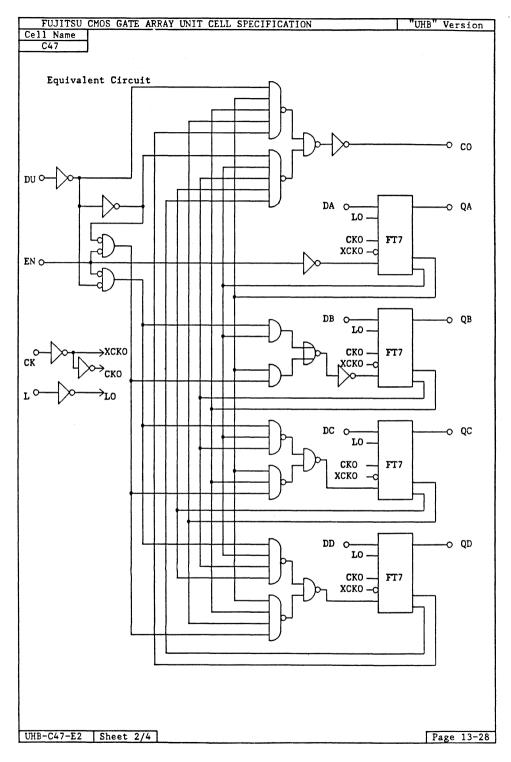


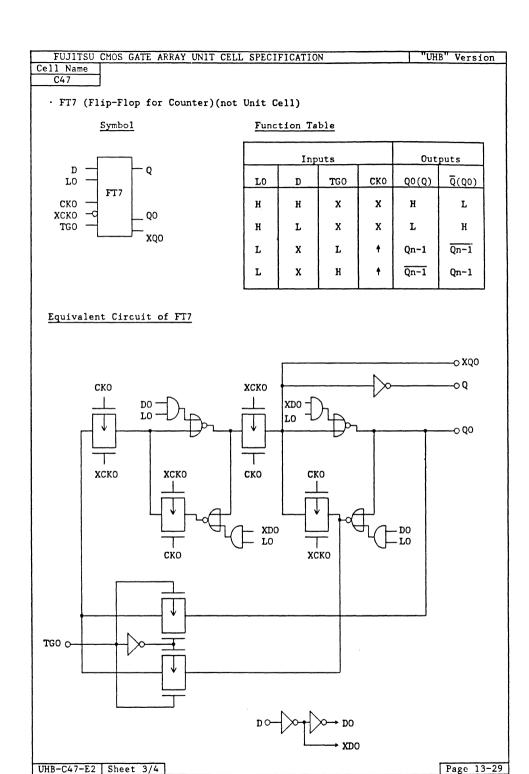
FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		l "U	HB" Version	
Cell Name	Function							Number of BC	
C47	Non-SCAN 4-bit	Binary						68	
Cell Symbol				agation			er		
			up		td				
		t0	KCL	t0	KCL	KCL2	CDR2		
		3.99	0.16	3.59	0.16	0.25	4	CK → Q	
	i	5.41	0.11		0.08		١.	CK → CO	
		5.01	0.16	5.54	0.16	0.25	4	L + Q	
		2.47	0.11	3.01	0.08			DU → CO	
DA	— QA — QB — QD	D						5-4-14	
		Parameter Clock Pulse Width					ymbol tCW		
		Clock Pulse Width					tCWH	5.6	
		Clock Pause lime					tcwn	0.9	
		Data S	etup Ti	<b>m</b> o			tSD	0.7	
			old Tim				tHD	1.8	
	Input Loading	Data n	OIG IIII				CILD	1.0	
Pin Name	Factor (lu)	DU Set	up Time				tSU	5.3	
D	1	DU Hol					tHU	0.8	
Ĺ	2								
DŪ	ī	EN Set	up Time				tSE	5.0	
CK	1	EN Hol					tHE	1.2	
EN	3								
	1	Clear	Release	Time			tREM	2.3	
	Output Driving	Clear Hold Time tIN						11.1	
Pin Name	Factor (lu)								
Q	18	Load P	ulse Wi	tLW	4.6				
co	18	The	values		worst	case or	erati	ing condition. ng condition olier.	

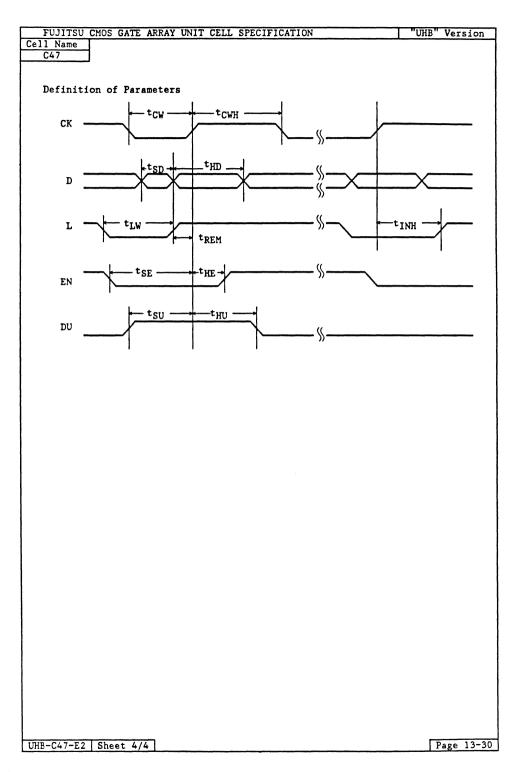
		Outputs			
Q	L	EN	DU -	CK	Q
H L X X	L L H H	X H L	X X X L H	X X † †	H L No Counting Count Up Count Down

Note: The CO output produces a low level output pulse when the counter overflows or underflows.

UHB-C47-E2 | Sheet 1/4



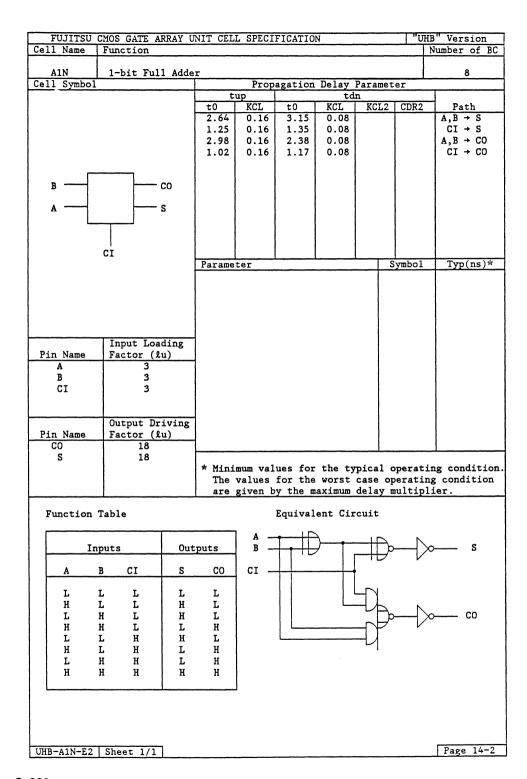




# **Adder Family**

Page	Unit Cell Name	Function	Basic Cells
2–219	A1A	1-bit Half Adder	5
2-220	A1N	1-bit Full Adder	8
2-221	A2N	2-bit Full Adder	16
2-223	A4H	4-bit Binary Full Adder with Fast Carry	48

Di Timari a				<del></del>		1 11	211		
Cell Name	MOS GATE ARRAY Function	INIT CELL SPECIF	TCATIO	N .		"UH	B" Version Number of BC		
A1A	1-bit Half Add	Propagation Delay Parameter							
Cell Symbol		tup	gation	Delay P		<u> </u>			
		tO KCL	t0	KCL		CDR2	Path		
		1.22 0.08	1.44	0.04			A → S		
		1.09 0.08	1.46	0.04	İ		B → S A → CO		
		1.27 0.08	1.15	0.04			B + CO		
		1 1 1		1					
В	со	1 1 1	i	l					
"-			j						
A	s								
<u> </u>					1				
				1	1				
1							<del> </del>		
		Parameter			Sy	mbo1	Typ(ns)*		
Pin Name	Input Loading Factor (lu)	1			į				
A A	2	1			ĺ				
В	2								
					Ì				
	Output Driving				ĺ				
Pin Name CO	Factor (lu)	-							
s	36								
		* Minimum valu	es for	the typ	oical op	erati	ng condition.		
		The values if	tor the	worst o	case ope	ratin Iltipl	g condition		
	1					P±			
Function '	<b>Table</b>	F	Equival	ent Circ	uit				
		7 A			-				
A :	B CO S	В —		-	1h	N	a		
	, , ,						> s		
i i	LLL								
1 1	LLH			14	$\perp$	N	~ 22		
н	H L					$\neg \lor$	> co		
L		J							
LITID ALL DO	Sh 1 /1 ]						Page 14-1		
UHB-A1A-E2	Sheet 1/1						rage 14-1		

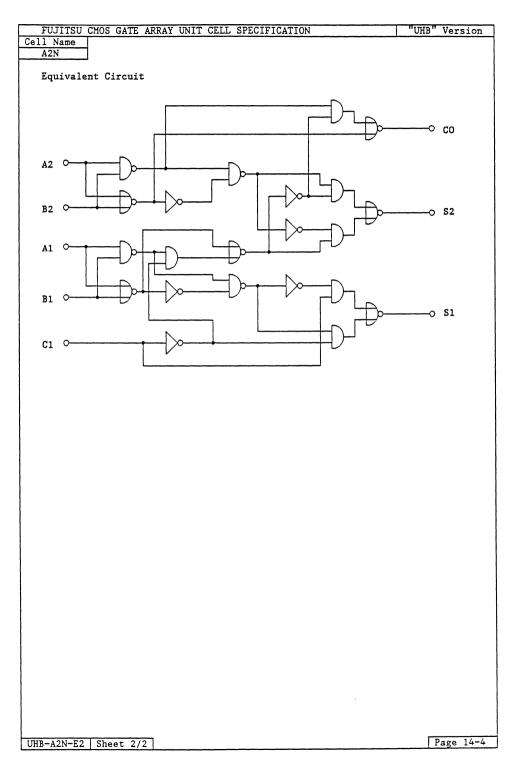


FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version										
Cell Name	Function							Number of BC		
A2N	2-bit Full Adde	r						16		
Cell Symbol				agation	Delay		er			
1			tup tdn							
1		t0	KCL	t0	KCL	KCL2	CDR2			
1		2.85	0.29	2.81	0.14		ł	A1 → CO		
		2.74	0.29	2.87	0.14			B1 → CO		
1		1.58	0.29	1.36	0.09	0.12	4	A2 → CO		
		1.47	0.29	1.36	0.09	0.12	4	B2 → CO		
		2.79	0.29	2.58	0.14			CI → CO		
B2-	со	2.97	0.22	2.75	0.14		i	A1 → S1		
A2		2.97	0.22	2.75	0.14			B1 → S1		
B1	S2	1.18	0.22	1.19	0.14		l	CI → S1		
A1	S1	2.82	0.22	2.75	0.14		l	A1 → S2		
		3.11	0.22	2.95	0.14		1	A2 → S2		
ļ		2.71	0.22	2.81	0.14		l	B1 → S2		
		3.11	0.22	2.95	0.14		1	B2 → S2		
	CI	2.76	0.22	2.52	0.14			CI → S2		
		Parameter					vmbol	Typ(ns)*		
		rarame	ter				ушоот	Typ(IIS)		
	Input Loading	1						}		
Pin Name	Factor (lu)	l								
A,B	2	1								
CI	2									
	1									
1						1		1		
		]								
	Output Driving	1								
Pin Name	Factor (lu)	l				1				
S	14									
co	14									
								ing condition.		
								ng condition		
	1	are	given b	y the m	aximum	delay m	ultip	lier.		

	Inpu	its		Outputs						
				(	CI = L			CI = H		
A1	B1	A2	B2	S1	S2	CO	S1	S2	CO	
							1			
L	L	L	L	L	L	L	H	L	L	
H	L	L	L	Н	L	L	L	H	L	
L	H	L	L	H	L	L	L	H	L	
H	H	L	L	L	H	L	Н	H	L	
L	L	H	L	L	Н	L	н	H	L	
H	L	H	L	н	Н	L	L	L	H	
L	H	H	L	н	H	L	L	L	H	
Н	H	H	L	L	L	H	н	L	H	
L	L	L	Н	L	Н	L	н	H	L	
Н	L	L	H	н	Н	L	L	L	H	
L	H	L	H	н	Н	L	L	L	Н	
H	Н	L	H	L	L	H	н	L	Н	
L	L	Н	Н	L	L	Н	н	L	H	
Н	L	Н	Н	н	L	Н	L	н	Н	
L	H	Н	H	н	L	H	L	Н	Н	
H	Н	Н	H	L	H	H	н	Н	Н	
	••	••	••	-	••	••				

UHB-A2N-E2 | Sheet 1/2

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FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version											
Cell Name	Function							Number of BC			
А4Н	4-bit Binary Fu	11 Adde	r with	Fast Ca	rrv			48			
Cell Symbol	- DIO DIMILY TO	i nauc				Paramet	er				
		t	Propagation Delay Parameter tup tdn								
		t0	KCL	t0	KCL	KCL2	CDR2	Path			
}		1.18	0.22	1.63	0.14			CI → S1			
Ì		2.65	0.29	3.07	0.14			CI → S2			
		3.03	0.29	2.98	0.14			CI → S3			
B4	co	3.14	0.29	3.54	0.14			CI → S4			
A4	S4	2.87	0.16	3.21	0.08			CI → CO			
В3 —											
A3	s3	3.81	0.22	3.39	0.14			A1,B1 → S1			
B2		3.17	0.29	3.08	0.14			A1,B1 → S2			
A2	S2	3.42	0.29	3.85	0.14			A1,B1 → S3			
B1		3.75	0.29	3.92	0.14			A1,B1 → S4			
A1	S1	3.30	0.16	3.78	0.08			A1,B1 → CO			
	<del></del>										
1		3.09	0.29	3.37	0.14			A2,B2 → S2			
	07	3.66	0.29	3.60	0.14			A2,B2 → S3			
1	CI	3.74	0.29	4.05	0.14			$A2,B2 \rightarrow S4$			
		3.87	0.16	3.83	0.08			$A2,B2 \rightarrow CO$			
								}			
1	Input Loading	2.81	0.29	2.85	0.14		1	A3,B3 → S3			
Pin Name	Factor (lu)	3.84	0.29	4.04	0.14		l	A3,B3 → S4			
A	2	3.80	0.16	3.82	0.08			A3,B3 → CO			
В	2						١.	1			
CI	2	2.90	0.22	3.01	0.09	0.12	4	$A4,B4 \rightarrow S4$			
	<u> </u>	3.66	0.16	3.51	0.08			A4,B4 → CO			
l	Output Driving	1			l						
Pin Name	Factor (lu)						l				
CO	18						L				
S1,S3,S4	14										
S2	18	1									
<b> </b>	1	L						<del> </del>			

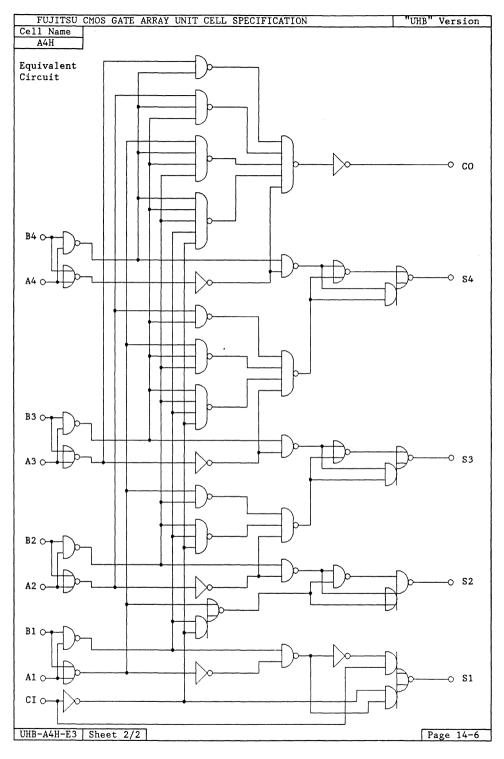
UHB-A4H-E3 Sheet 1/2

				OUTPUT							
	INP	UT		<u>CI</u> C2	$=\frac{L}{L}$		CI C2				
- <u>A</u> 1	$\frac{B1}{B3}$	<u>A</u> 2 <u>A</u> 4	$\frac{B2}{B4}$	$\frac{S1}{S3}$	<u>S2</u> <u>S4</u>	C2_ C0	_ <u>S</u> 1_ S3	<u>\$2</u> \$4	C2_ C0_		
L H L H L H L	L L H L H H L H H L H H L H H L H H L H H L H H H L H H H H H H H H H H H H H H H H H H H H	L L L H H H L L L H H	L L L L L L H H H H H	L H H L H H L H H H H H	L L L H H H H L H H L L L L	L L L L L L L L H L L H H H H H H H H H	H L L H H L L L L L L L L L L L L L L L	L H H H L L L H L L H H	L L L L H H H H H H H H H H H H H H H H		

#### Note:

Input conditions at A1, A2, B1, B2 and CI are used to determine outputs S1 and S2 and the value of the internal carry C2. The values at C2, A3, B3, A4 and B4 are then used to determine outputs S3, S4 and CO.

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# **Data Latch Family**

Unit Cell				Basic		
	Page	Name	Function	Cells		
	2-227	YL2	Data Latch with TM	5		
	2-229	YL4	Data Latch with TM	14		
	2-231	LTK	Data Latch	4		
	2-233	LTL	Data Latch with Clear	5		
	2-235	LTM	Data Latch with Clear	16		
	2-238	LT1	S-R Latch with Clear	4		
	2-240	LT4	Data Latch	14		

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		<b>"</b> UI	dB" Version
Cell Name	Function							Number of BC
YL2	1-bit Data Latc	h with						5
Cell Symbol				agation	Delay		ter	- <b>-</b>
			up		td		T ====	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.73	0.08	2.81	0.04		ł	CK, IH → Q
		1.16	0.08	1.28	0.04		1	$D \rightarrow Q$
							1	1
_						ł	1	1
D —	├- Q					l		
1 1	Ų					<b>[</b>	İ	
ск — ⊲						ł	1	
IH —						İ	į	
TM						İ	1	
-						{	1	
							İ	
ļ		İ					1	l l
1		Parame	ter	<del></del>			Symbol	Typ(ns)*
		Clock	Pulse W	idth			tCW	6.8
1								
			etup Ti				tSD	3.2
l		Data H	old Tim	<u>e</u>			tHD	2.5
<u></u>	T +	l						
Die Noon	Input Loading							
Pin Name D	Factor (lu)							1
CK	1	1						
IH	1							
TM	1 1							
1 ""	1					- 1		
		1						
<u> </u>	Output Driving	1						1
Pin Name	Factor (lu)							
Q	36	1				- 1		1
1								
		* Mini	mum val	ues for	the ty	pical (	operat:	ing condition.
1								ng condition
					aximum			

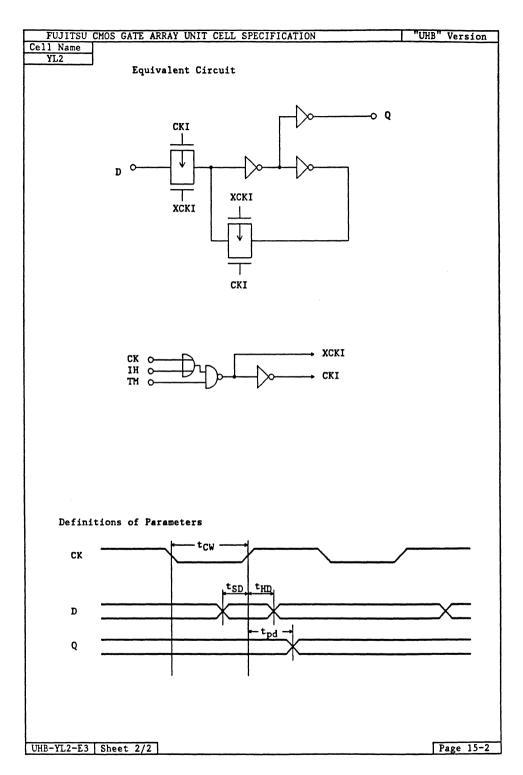
### Note:

The TM terminal must be kept LOW during the SCAN Mode.

### Function Table

	Inp	ut		Output	Mode	
TM	TM IH CK		D Q		noue	
L	LXX		D	D	SCAN	
Н	Н	X	X	Q <sub>0</sub>		
Н	Х	Н	X	l Q <sub>o</sub> l	LATCH	
Н	L	L	D	D		

UHB-YL2-E3 | Sheet 1/2



FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		<b>"</b> UF	B" Version
Cell Name	Function							Number of BC
YL4	4-bit Data Late	h with						14
Cell Symbol		<u> </u>		agation	Delay		ter	<del></del>
			up KCL	40	td KCL	n KCL2	CDDA	
1		t0 3.33	0.08	t0 3.43	0.04	KUL	CDR2	Path CK,IH + Q
		1.10	0.08	1.29	0.04		ļ	$D \rightarrow Q$
1		1.10	0.00	1.23	0.04		1	Dad
-	<del></del>						ļ	
D1 -	├─ Q1							
D2 -	- Q2						ł	
D3 -	<b></b>	1					ı	
D4 -	├─ Q4						i	1
ck -d							ı	
IH —	j						1	İ
TM -d							j	į.
							j	}
İ		Parame	<u> </u>				Symbol	Typ(ns)*
		rarame	tel			-+	Symbol .	Typ(iis)"
		Clock	Pulse W	idth	(CK	7	tCW	7.2
j .								
ł		Data S	etup Ti	me	(D)		tSD	1.8
ļ		Data H	old Tim	e	(D)		tHD	4.0
<u> </u>								
	Input Loading					- 1		
Pin Name	Factor (lu)	l				- 1		1
D	2	1				- 1		1
CK IH	1	ł				- 1		1
TM	1	l				- 1		}
I In	1 1	ì				- 1		Į.
		l				- 1		1
1						- 1		l
	Output Driving	1				- 1		1
Pin Name	Factor (lu)	1				1		l
Q	36							_1
}				_	_			
}		* Mini	mum val	ues for	the ty	pical	operati	ing condition.
1	1							ng condition
	<u> </u>	are given by the maximum delay multiplier.						

## Note :

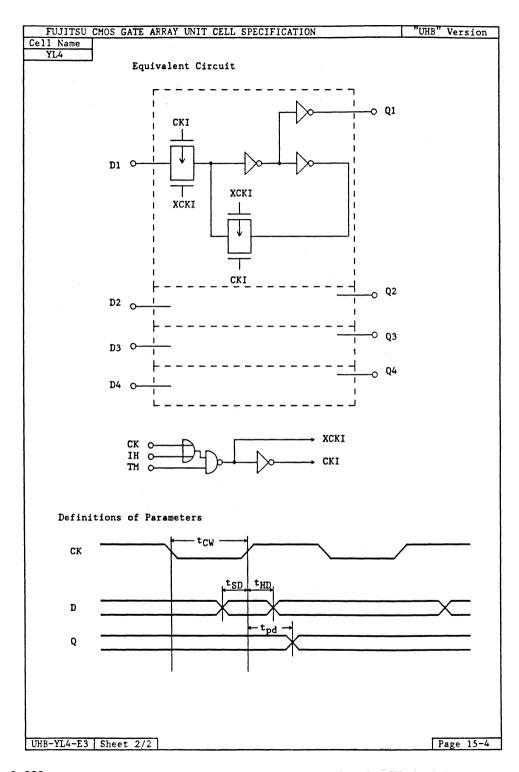
The TM terminal must be kept LOW during the SCAN Mode.

#### Function Table

	Inp	ut		Output	Mode
TM	IH	CK	Dn	Qn	node
L	X	X	D	D	SCAN
Н	Н	X	X	Qno	
H	X	Н	X	Qno	LATCH
Н	L	L	D	D	
n =	1 ~	4		-,	

 $n = 1 \sim 4$ 

UHB-YL4-E3 Sheet 1/2

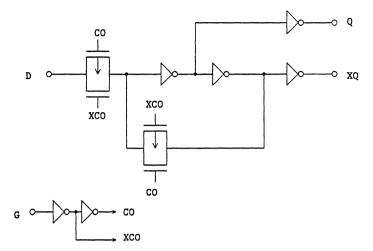


FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N	,	"UHE	B" Version
Cell Name	Function							Number of BC
LTK	Data Latch							4
Cell Symbol			Prop	agation	Delay 1	Paramet	er	
		t0 t	up KCL	+0	KCL KCL	KCL2	CDR2	Path
		1.03 1.45 1.75 2.12	0.16 0.16 0.16 0.16	1.15 1.63 1.82 2.34	0.08 0.08 0.08 0.08	KCLZ	CDR2	D + Q D + XQ G + Q G + XQ
D ————————————————————————————————————	— q >— хq							
		G Inpu	ter t Pulse	Width			tGW	Typ(ns)* 4.0
			etup Ti old Tim			-+-	tSD tHD	1.6
		Data II	OIG III				CILD	2.3
Pin Name	Input Loading Factor (lu)					ļ		
D	2	1						
G	1							
Pin Name	Output Driving Factor (lu)							
Q XQ	18 18							
		The	values	for the	the ty worst	case of	perating	ng condition g condition ier.
Function T	able							
Inputs	Outputs							
D G	Q XQ							
X H H L L L	Q <sub>0</sub> XQ <sub>0</sub> H L L H							
UHB-LTK-E2	Sheet 1/2							Page 15-5

Cell Name LTK

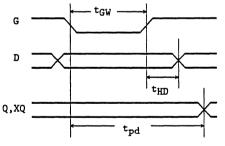
Equivalent Circuit

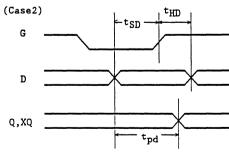
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION



Definition of Parameters

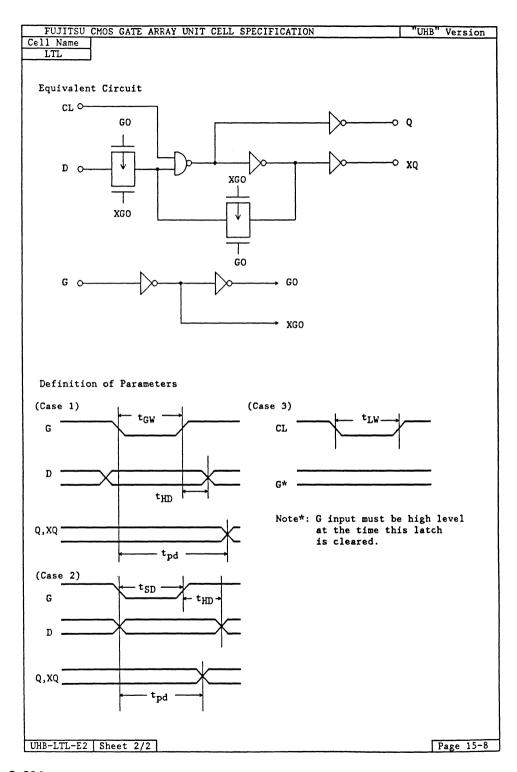
(Case1)



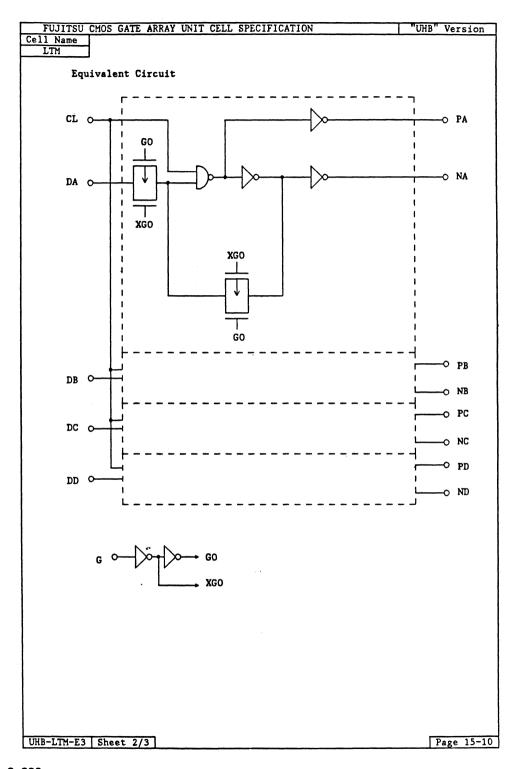


UHB-LTK-E2 | Sheet 2/2

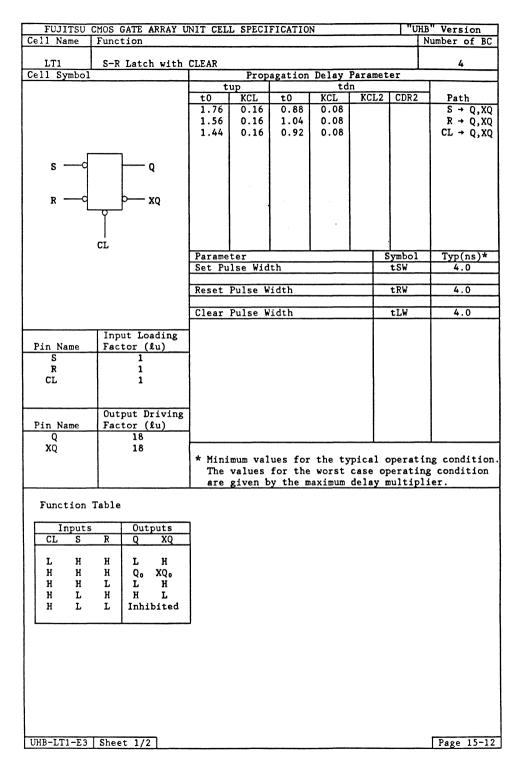
		UNIT CELL SPECIFICATION	"UHB" Version
cell Name	Function		Number of B
LTL	1-bit Data Lat	ch with Clear	5
Cell Symbol		Propagation Delay Para	
		tup tdn	
			CL2 LD2 Path
		1.39 0.16 0.85 0.09 1.18 0.16 1.22 0.09	$\begin{array}{c} CL \rightarrow Q, X \\ D \rightarrow Q \end{array}$
		1.52 0.16 1.71 0.09	$D \rightarrow Q$
		1.96 0.16 1.92 0.09	$G \rightarrow Q$
		2.22 0.16 2.51 0.09	$G \rightarrow XQ$
D	Q		
	"		
G — 9			
	þ xq		
<u> </u>	<del>-                                    </del>		
	CL		
	OD.	Parameter	Symbol Typ(ns)*
		G Input Pulse Width	tGW 4.0
		Data Setup Time	tSD 1.3
		Data Hold Time	tHD 0.5
		Data Nota Time	0.5
		Clear Pulse Width	tLW 4.0
	Input Loading		
Pin Name	Factor (lu)	4	
D G	2 1		1
CL	i		1
0.2	1		
	Output Driving		1
Pin Name	Factor (lu)	4	1
Q XQ	18 18		<u> </u>
AQ	10	* Minimum values for the typica	al operating condition
		The values for the worst case	operating condition
		are given by the maximum dela	
_			
Funcion Ta	able		
Input	s Outputs	٦	
CL D	G Q XQ	1	
	1 3 3	7	
LX	i i		
HX			
H H L	L H L L L H		
" "	r r r		
L		_	
וווום_דידד _בים	Choo+ 1/2		Page 15-7
UHB-LTL-E2	Sheet 1/2		rage 15-7

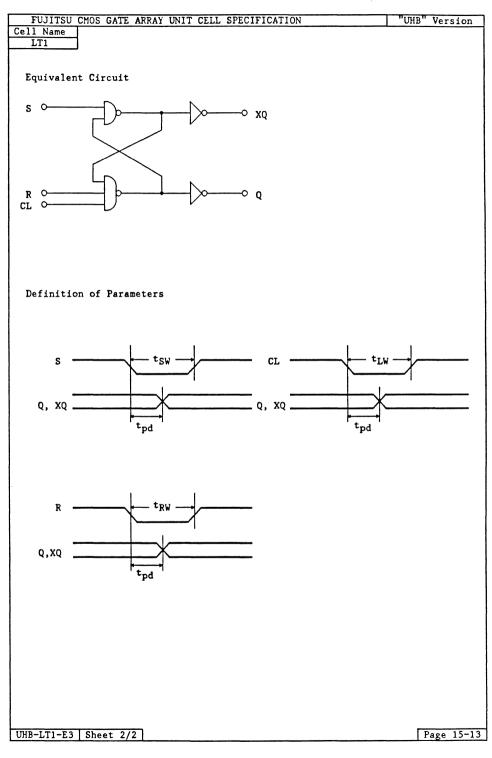


FILITCILC	MOS GATE ARRAY L	NIT CELL	CDECI	FICATIO	NI.		TITE TO	B" Version
	Function	NII CEL	L SPECI.	FICATIO	14			Number of BC
			01					
LTM Cell Symbol	4-bit Data Late	h with (		agation	Delay	Paramete		16
cell Cymbel		tı	up	agacion	td			T
DA	PA	1.54 1.22 1.60 2.61 2.73	0.16 0.16 0.16 0.16 0.16 0.16	0.97 1.29 1.79 2.45 3.15	0.08 0.08 0.08 0.08 0.08	KCL2	CDR2	Path  CL + P,N  D + P  D + N  G + P  G + N
DB — DC — DD — G — C	O— NA — PB O— NB — PC O— NC — PD O— ND							
		Parame		Widel			ymbol tGW	Typ(ns)* 4.0
	CL	G Inpu	t Pulse	Width			EGW	4.0
		Clear	Pulse W	idth			tLW	4.0
		Data S	etup Ti	me			tSD	1.6
		Data H	old Tim	<u>e</u>			tHD	2.3
Pin Name	Input Loading Factor (lu)	1						
D	2	1						1
CL CL	1 4							
	•							
	Output Driving							
Pin Name P	Factor (lu)	{						
N	18							
		The	values	for the	worst		eratin	ing condition. ng condition lier.
Function T	able							
Inputs	Outputs							
CL D G	PN							
LXH	1 1							
HHI								
HLI								
UHB-LTM-E3	Sheet 1/3							Page 15-9
בייה היוו היי	J 2/3							1.765 15 7

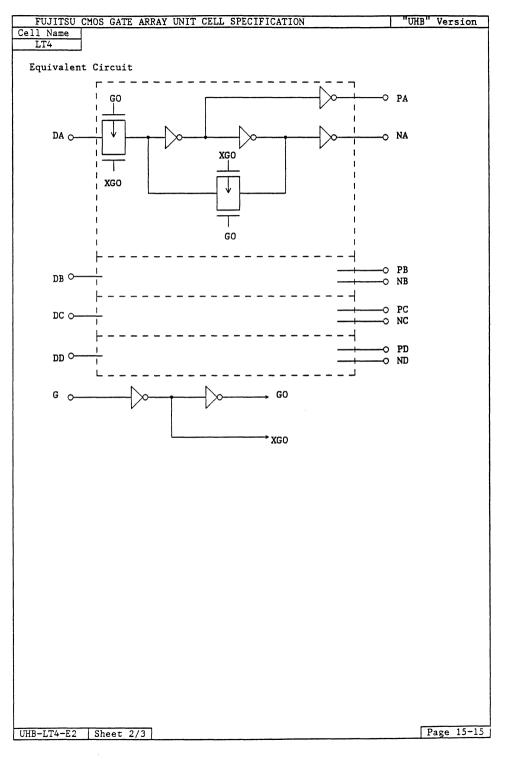


FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version Cell Name LTM Definition of Parameters (Case1) -tGW -P,N (Case2) G tHD tSD (Case3) CL \*G P,N Note \*: G input must be high level at the time this latch is cleared. Page 15-11 UHB-LTM-E3 | Sheet 3/3

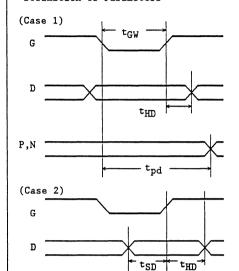




FII	וופדוו מ	MOS GATE	APPAV	INIT CEL	T. SPECT	FICATIO	NI		I III	HB" Version
Cell I		Function		OIVII OLL	n biloi	TICATIO	.,		1 1	Number of BC
	,	, , ,		- 1						
Coll	Symbol	4-bit I	Data Lat	ch	Pron	agation	Dolor	Daramat		14
Cell .	зушьот			+ t	up	agation	td		ET	
				t0	KCL	t0	KCL	KCL2	CDR2	Path
l				2.50	0.16	2.28	0.08			G → P
ļ				2.50	0.16	3.05	0.08			G → N
1				1.05	0 16 0.16	1.18	0.08			$D \rightarrow P$ $D \rightarrow N$
DA	_	<u> </u>	- PA	1.40	0.10	1.00	0.08			D T N
DB	-	þ-	- NA							
DC	$\neg$		- PB							
DD		p-	- NB							
G	<b>-</b> −d	5-	- PC - NC	1						
	1	F	- PD							
1		þ-	- ND							
	L			<u> </u>						
				Parame		عاجاته إزارا		<u>s</u>	ymbol tGW	Typ(ns)* 4.0
				G Inpu	t Pulse	Width			TGW	4.0
				Data S	etup Ti	me			tSD	1.6
				Data H	old Tim	е			tHD	2.3
1										
		Input 1	Loading	-						
Pin l	Name	Factor	(lu)					į		
D			2							
G			l	1						
		1		İ						
İ		1								
		Output	Driving	7						
Pin		Factor		4						
N		1 12								
1		-	-	* Mini	mum val	ues for	the ty	pical o	perat	ing condition.
				The	values	for the	worst	case or	erati	ng condition
<u> </u>		ــــــــــــــــــــــــــــــــــــــ		are	given b	y the m	aximum	delay n	ultip	lier.
Fun	ction ?	Table								
	Input		puts							
	D C	G P	N							
	н 1	H Po	No.							
		H Po								
		L H	L							
	L 1	LL	н							
	L									
UHB-T.	T4-E2	Sheet 1	/3							Page 15-14
			1							



Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION

P,N

UHB-LT4-E2 | Sheet 3/3

# **Shift Register Family**

Page	Unit Cell Name	Function	Basic Cells
2–245	FS1	Serial-in Parallel-out Shift Register	18
2-247	FS2	Shift Register with Synchronous Load	30
2-249	FS3	Shift Register with Asynchronous Load	34
2-252	SR1	Serial-in Parallel-out Shift Register with Scan	36

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"บ	HB" Version
Cell Name	Function							Number of BC
FS1	4-bit Serial-in	Parall	el-out	Shift R	egister			18
Cell Symbol			Prop	agation	Delay	Paramet	er	
		tup tdn						
1		t0	KCL	t0	KCL	KCL2	CDR2	
SD —C	— QA — QB — QC — QD	2.42	0.16	3.14	0.09	0.12	4	CK → Q
		Parame		l	L		Symbol	
		Clock	Pulse W	idth		_	tCW	4.0
		SD Set	up Time			tSSD	0.6	
1			d Time			tHSD	0.2	
		Clock		C ≦ 1	6 lu		tCWL*	* 5.8
	Input Loading	Pause	16	< C ≦ 3	2 lu		tCWL*	* 8.4
Pin Name	Factor (lu)	Time	32	< C ≦ 3 < C ≦ 4	8 lu		tCWL*	* 10.9
SD CK	1	dit con	imum va ion. dition	lues fo The val are giv	r the tues for	the w	orst c	ting con- ase operating elay
Pin Name Q	multiplier.  Output Driving Pin Name Factor (lu) ** The value of tCWL depends on the load							

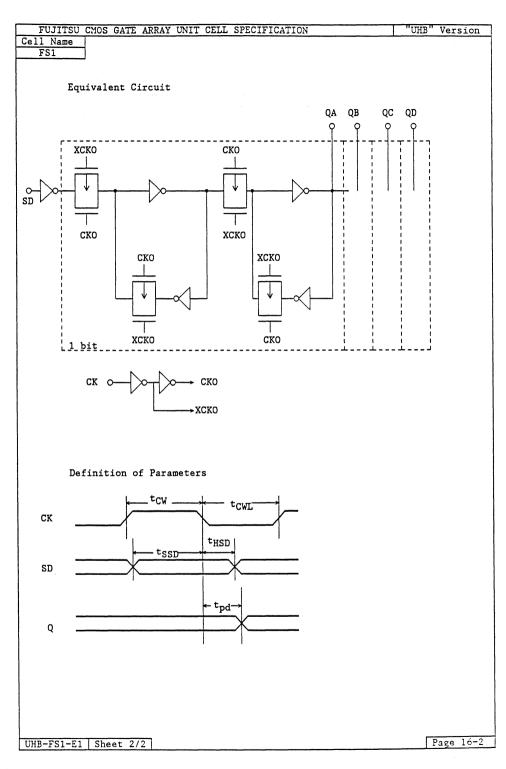
#### Function Table

-	Inp	uts	Outputs							
ļ	SD	CK	QA	QB	QC	QD				
	SD	<b>+</b>	SD	QAn	QBn	QCn				

Note:  $\cdot$ SD = H or L

·QAn, QBn and QCn are levels of QA, QB and QC respectively, before the falling edge of CK, i.e. 1 bit shift by the falling edge of CK.

UHB-FS1-E1 | Sheet 1/2



	CMOS GATE ARRAY U	NIT CELI	SPECI	FICATIO	N			B" Version
Cell Name	Function							Number of BO
FS2	4-bit Shift Regi	ster wit						30
Cell Symbol		<u> </u>		agation	Delay		ter	T
		tı			td		I GDD0	
		t0 2.32	KCL 0.16	3.14	KCL 0.09	KCL2 0.12		Path CK → O
PA PB PC PD CK CK L	QA QB QC QD	Paramet Clock	cer		0.09		Symbol tCW	Typ(ns)*
		SD Seti					tSSD	2.8
		SD Hold	1 Time				tHSD	1.2
		Load Se	tup Ti	me			tSL	4.3
		Load Ho					tHL	0.5
		P Setu	Time				tSP	3.6
		P Hold	Time				tHP	1.5
	Input Loading							
Pin Name	Factor (lu)	Clock		C ≦ 1			tCWL**	
CK	1	Pause		< C ≦ 3			tCWL**	
SD	1	Time	32	< C ≦ 4	8 lu		tCWL**	11.0
L P	1 1 Output Driving	dit	ion.	The val	ues for	the w	orst ca	ing con- se operatin
Pin Name	Factor (lu)	condition are given by the maximum delay multiplier.						ıay
Q	16				depend output			(C) , QB, QC an

#### Function Table

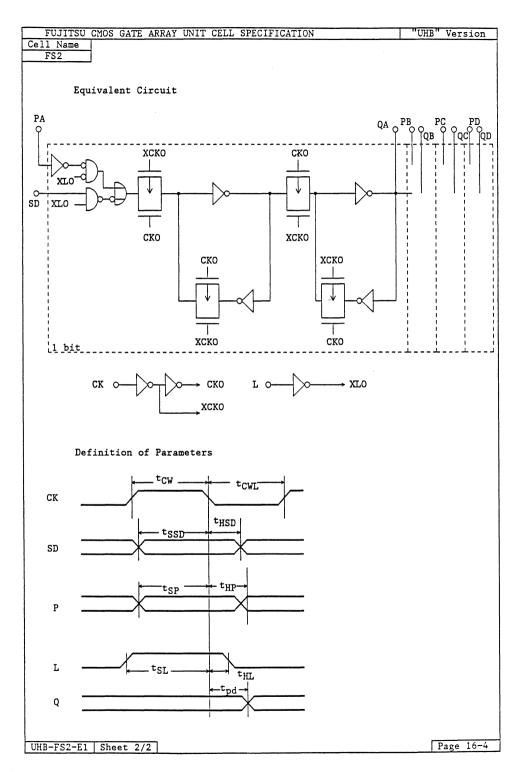
	Inp	uts		Outputs					
SD	L	P	CK	QA	QB	QC	QD		
SD	L	Х	<b>+</b>	SD	QAn	QBn	QCn		
х	н	P	<b>+</b>	PA	PB	PC	PD		

Note:  $\cdot$ SD = H or L

·QAn, QBn and QCn are levels of QA, QB and QC respectively, before the falling edge of CK, i.e. 1 bit shift by the falling edge of CK.

 $\cdot P$  represents PA, PB, PC and PD.

UHB-FS2-E1 | Sheet 1/2

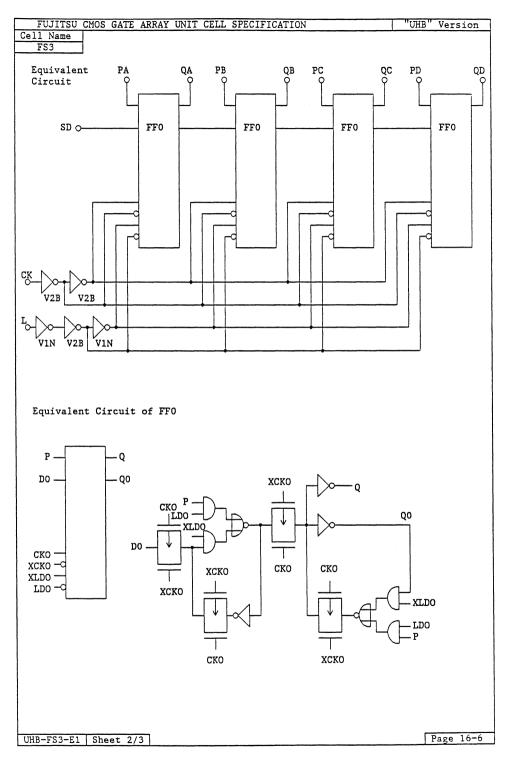


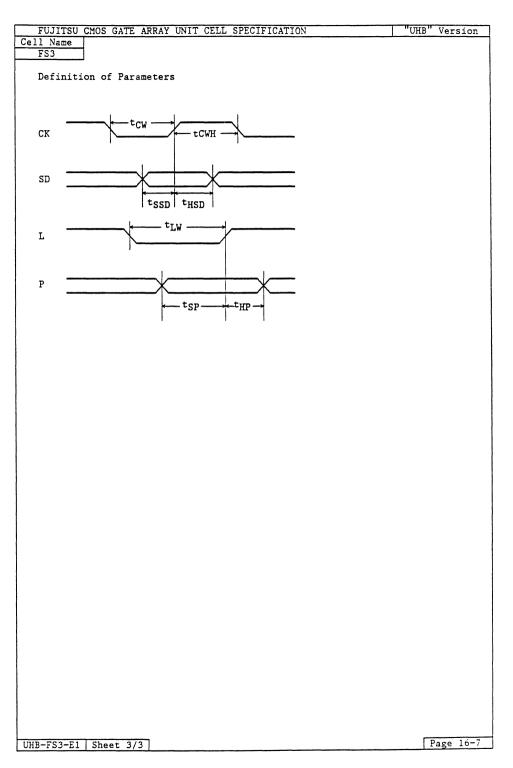
	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		ש"ט	HB" Version
Cell Name	Function						Number of BC	
FS3 Cell Symbol	4-bit Shift Register with Asynchronous Load Propagation Delay Parameter						34	
Cell Symbol		+	up Prop	agation	Delay td		cer	<del></del>
		to l	KCL	t0	KCL	KCL2	CDR2	Path
		2.28	0.17	2.12	0.11	KCL2	CDRZ	CK → Q
		4.64			0.11		1	$L \rightarrow Q$
		2.03	0.17	3.02	0.11		1	$P \rightarrow Q$
		2.03	0.17	3.02	0.11			P → Q
PA ————————————————————————————————————	—— QA —— QB —— QC —— QD							
r —d		Parame					Symbol	Typ(ns)*
<del></del>			Pulse W				tCW	4.0
		Clock	Pause T	ime			tCWH	4.0
		Load P	ulse Wi	dth			tLW	6.2
		CD Cat	Ti				tSSD.	1.0
		SD Setup Time tSSD SD Hold Time tHSD						1.7
		2D UOI	d lime				споп	1./
	Input Loading	P Setu	n Time			-+	tSP	0.3
Pin Name	Factor (lu)	P Hold				-+	tHP	2.3
CK SD	2 2	1 nord	TIME				- CIII	
L	ī					- 1		-
P	2							1
-	1							
	Output Driving	1						1
Pin Name	Factor (lu)					1		
Q	18							
		The	values	for the		case o	perati	ing condition ng condition lier.

### Function Table

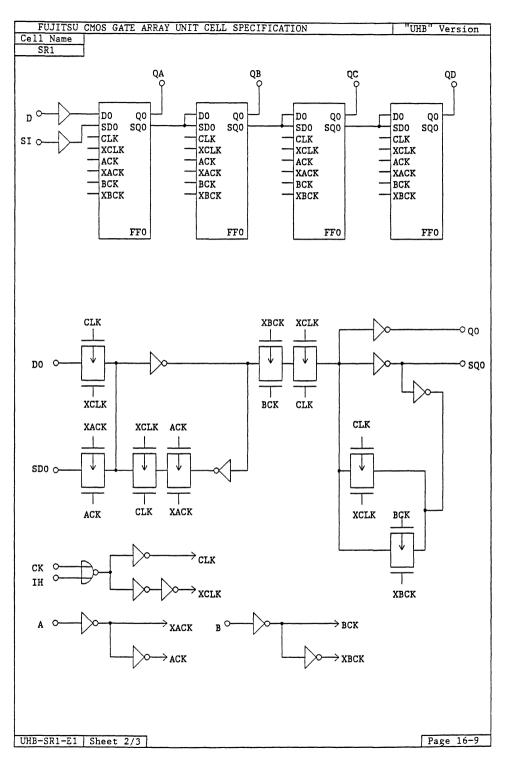
	Inp	Output		
L	P	SD	CK	Q
L L H H	L H X X	X L H	X X †	L H L H

UHB-FS3-E1 | Sheet 1/3





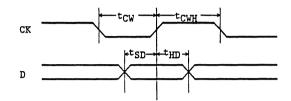
FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		l "UH	B" Version
	Function	IVII OLL	D DI DOI	IIONIIO	.,			Number of BC
	4-bit Serial-in	Parallel-out Shift Register with SCAN 36 Propagation Delay Parameter						36
Cell Symbol				agation	Delay td		er	
		t0	up KCL	t0	KCL	KCL2	CDR2	Path
		3.27	0.09	3.37	0.07	0.11	7	CK → Q
		2.58	0.09	2.90	0.07	0.11	7	$B \rightarrow Q$
							İ	
D	— QA							
	├— QB							
CK _	— QC							
IH —	— QD							
A -		l	l				ļ	
В							1	
L								
1		Parame	ter			S	ymbol	Typ(ns)*
1		Clock	Pulse W	idth			tCW	5.5
1		Clock	Pause T	Ime			tCWH	5.6
		Data S	etup Ti	me			tSD tHD	3.3
		Data H	old Tim	e			עתט	1.3
		1				}		
	Input Loading	i						
Pin Name	Factor (lu)							
D	1	1				1		
CK	1							1
IH	1							
SI	1					ĺ		
A,B	1	1						
D/- N	Output Driving					İ		
Pin Name Q	Factor (lu)	-				- 1		
"	. 30							<u></u>
		* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
		The	values	for the	worst	case of	peratin	g condition
		are	given b	y the m	aximum	delay n	multipl	ier.
1.								
1								
IND_CD1_E1	Shoot 1/2							Page 16-8
UHB-SR1-E1	Sheet 1/3							Tage 10-0



"UHB" Version

SR1

Definitions of Parameters

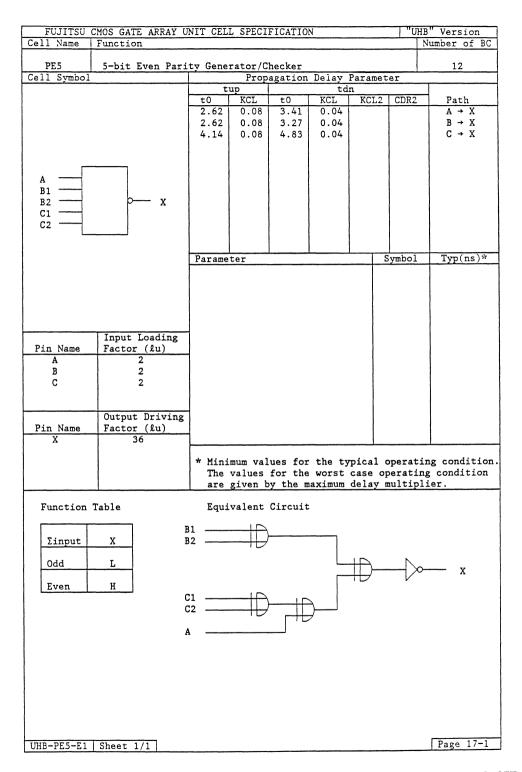


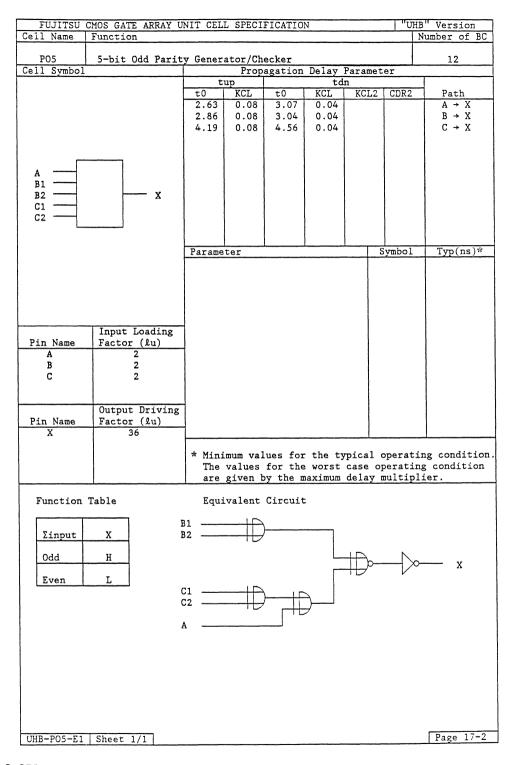
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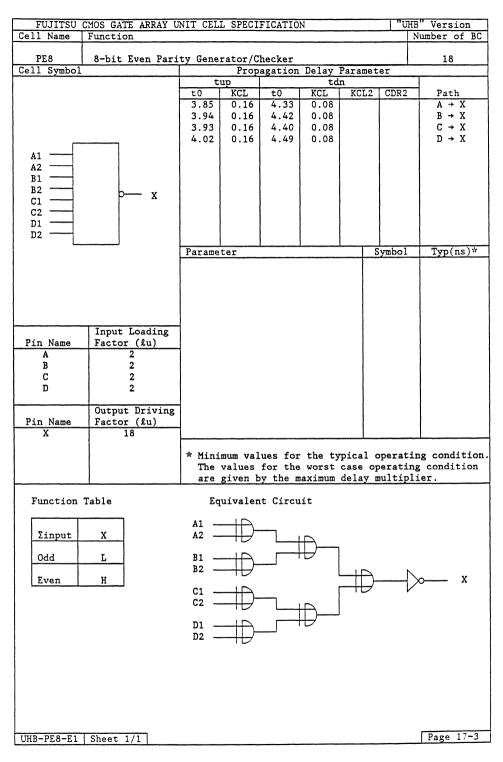
UHB-SR1-E1 | Sheet 3/3

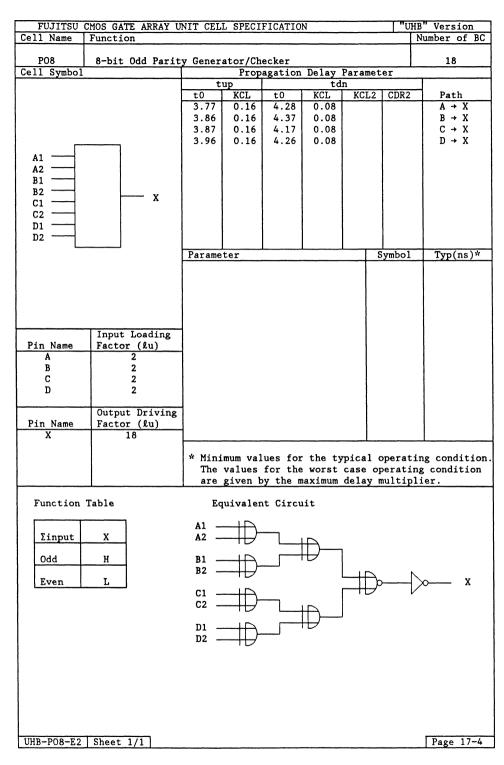
# Parity Generator/Selector/Decoder Family

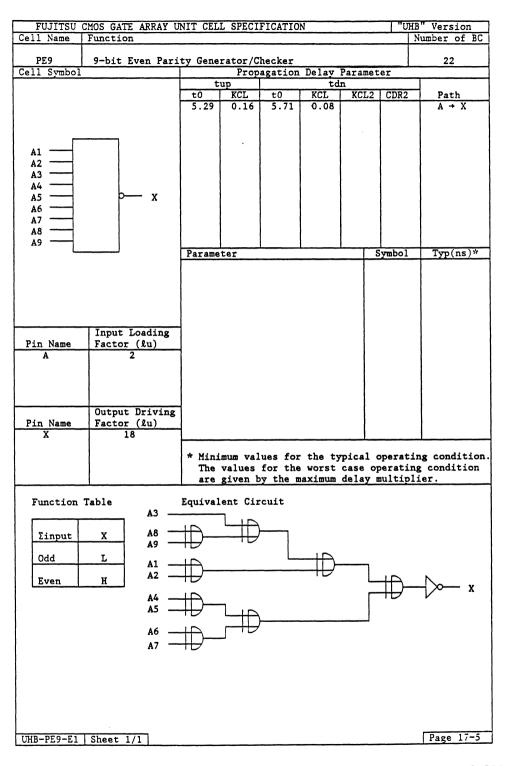
Page	Unit Cell Name	Function	Basic Cells					
Parity Generators/Checkers								
2-257	PE5	Even Parity Generator/Checker	12					
2-258	PO5	Odd Parity Generator/Checker	12					
2-259	PE8	Even Parity Generator/Checker	18					
2-260	PO8	Odd Parity Generator/Checker	18					
2-261	PE9	Even Parity Generator/Checker	22					
2–262	PO9	Odd Parity Generator/Checker	22					
Data Sele	ector							
2–263	P24	2:1 Data Selector	12					
Decoders	<b>S</b>							
2-264	DE2	2:4 Decoder	5					
2-265	DE3	3:8 Decoder	15					
2-267	DE4	2:4 Decoder	8					
2–268	DE6	3:8 Decoder	30					
Selectors	•							
2-270	T2B	2:1 Selector	2					
2-272	T2C	2:1 Selector	4					
2–273	T2D	2:1 Selector	2					
2-274	T2E	2:1 Selector	5					
2–275	T2F	2:1 Selector	8					
2–277	T5A	4:1 Selector	5					
2–279	V3A	1:2 Selector	2					
2–280	V3B	1:2 Selector	4					
Magnitud	le Compara	tor						
2-281	MC4	Magnitude Comparator	42					

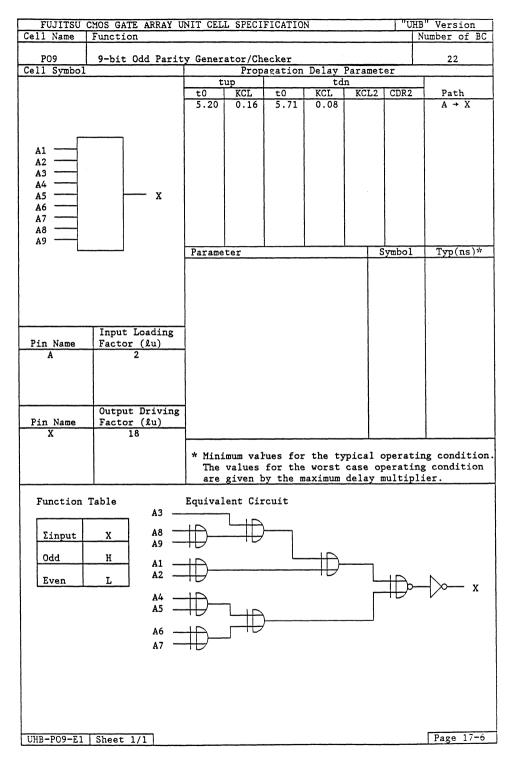


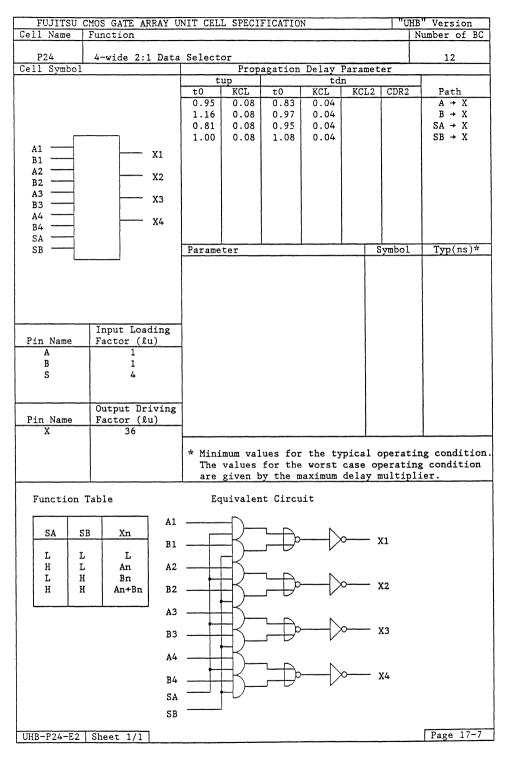


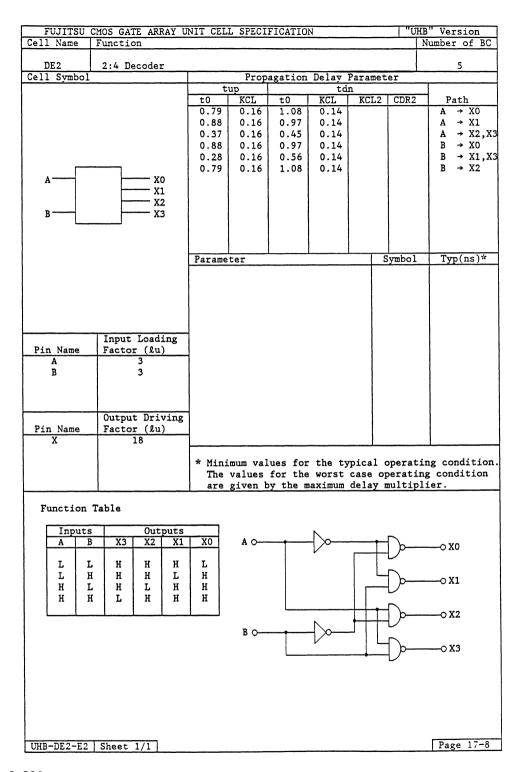










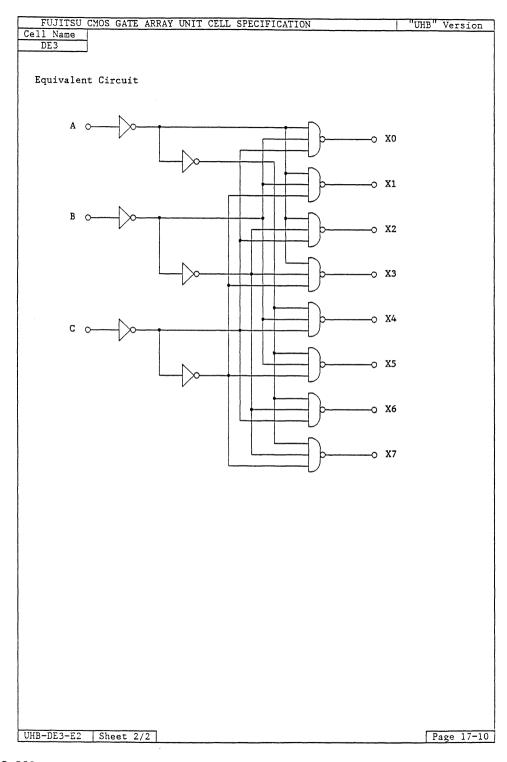


Cell Name	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"U	HB" Version
Cell Name	Function							Number of BC
DE3	3:8 Decoder							15
Cell Symbol			Prop	agation	Delay		er	
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	
1		1.44	0.16	1.67	0.19		ļ	A → X0~X3
		2.44	0.16	2.44	0.19		!	A → X4~X7
		1.33	0.16	1.72	0.19		Ì	B → X0~X3
		2.33	0.16	2.49				B → X4~X7
1	xo	1.23	0.16	1.78	0.19			C → X0~X3
Α —	X1	2.23	0.16	2.55	0.19		j	C → X4~X7
	X2							
В —	хз	i						
	X4						ļ	
	X5						l	1
С	X6							
	λ/							
		Parame	ter		İ	L .	vmbo1	Typ(ns)*
		1 di dinc	001				· ymbol	
		1				- 1		
						- 1		}
						į		Ì
1		İ				- 1		}
						l		1
	Input Loading	1				1		
Pin Name	Factor (lu)	İ				ļ		ļ
A	1	1				1		
В	1	1				Ì		
C	1	Ì				ł		
1	1	l				1		Ì
		!						
	Output Driving	1				ĺ		
Pin Name	Factor (lu)	1				- 1		1
Х	14							
	1							
								ing condition.
								ng condition
	are given by the maximum delay multiplier.							

### Function Table

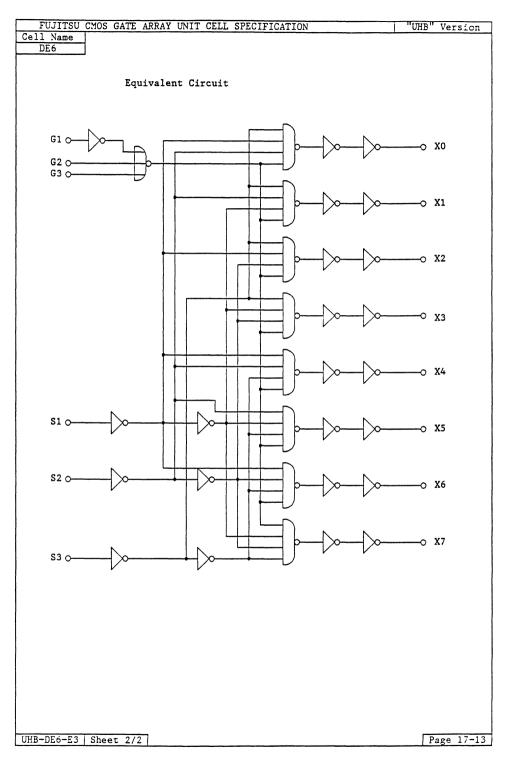
Ir	put	S				Outp	ıts			
A	В	С	X0	X1	X2	Х3	X4	X5	X6	X7
L	L	L	L	Н	н	н	н	н	н	н
L	L	H	Н	L	H	H	H	H	H	H
L	H	L	Н	H	L	H	Н	H	H	H
L	H	H	H	H	H	L	H	H	H	H
Н	L	L	н	H	H	Н	L	H	H	H
н	L	H	н	H	H	H	H	L	H	H
н	H	L	н	Н	H	H	H	H	L	Н
Н	H	H	Н	H	H	H	H	H	H	L
	••		"	••	••	••	••	••		_

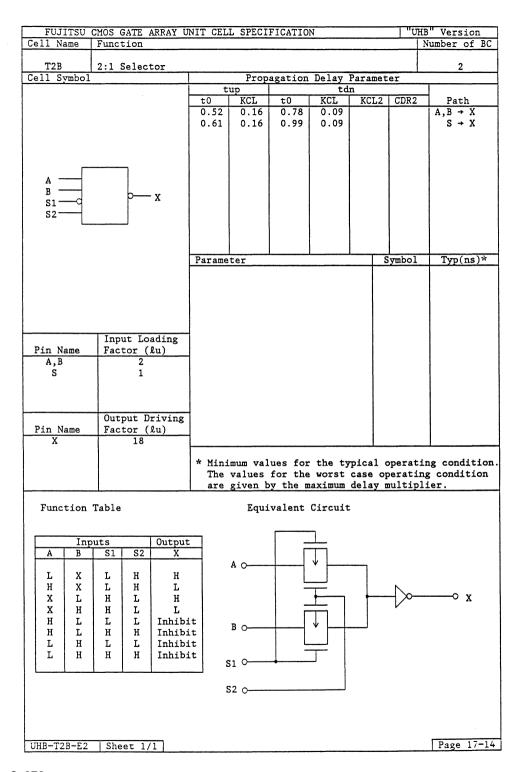
UHB-DE3-E2 | Sheet 1/2



FU.	JIT	SU C	MOS G	ATE AF	RAY I	NIT (	ELL S	PECI	FICATIO	)N		תזיי	HB" Version
Cell			Funct									Ť	Number of BC
DE	4		2.4 1	Decode	r wit	h Fra	hle					ļ	8
Cell		bol			- WIL			Prop	agation	Delay	Paramet	er	
						t0 1.1 0.8 1.0	.9 0 36 0	.16 .16 .16	t0 1.46 1.11 1.14	KCL 0.19 0.19 0.19	n KCL2	CDR2	Path G → X A → X B → X
A B G		- - - - -	0000	<u> </u>	(0 (1 (2 (3								
						Para	meter				S	ymbol	Typ(ns)*
Pin A B G	1	e		t Load or (li 3 3 1									
Din	Ma-	_		ut Dr:									
Pin X		<del>-</del>	ract	or (li 14	<u>. ,</u>								
						T	ne val	ues	for the	the ty worst	case or	erati	ing condition. ng condition lier.
Fun	cti	on I	able						I	Equivale	ent Circ	uit	
G	;	A	В	хз	X2	X1	X0		G	<u> </u>		7	
н	1	x	х	н	Н	Н	Н		Α	<del></del>			р хо
		L L H	L H L H	H H H L	H H L H	H L H H	L H H H						) X1
								1	В —				) X2
													у хз
UHB-D	)E4-	E2	Sheet	1/1									Page 17-11

Ce	FUJI:		MOS (		ARRAY	UNI	T CEL	L SP	CIF	ICATI	ON				ן"[		Version
		-			<b></b>		P 1-1									<u> </u>	
Ce	DE6	nbol	3:8	Deco	der wi	th	Enabl	e Pr	opa	gatio	n D	elav	Para	met	er	<u> </u>	30
						t	t	up		8		to	ln				<del></del>
							t0	KCI		t0		KCL	KC	L2	CDR2	-	Path
							3.05	0.:		5.95 3.28		0.08 0.08	l			- 1	$G \rightarrow X$ $S \rightarrow X$
							2.09	٠.,	10	3.20	' l	0.00		- 1			3 7 A
				٦									1			١	
	31 —	_		<b>—</b>	- X0								1			- 1	
	32 —				- X1 - X2						1		1			l	
	33 <del></del>	1			- X3						1			1		1	
	S1 —				- X4											İ	
	s2 — s3 —	_		-	- X5						ı		l			- [	
					- X6											- 1	
		L		_	- X7											ļ	
						F	arame	ter						S	ymbol		Typ(ns)*
						Г											
						-											
_			Inp	ut Lo	ading	7								1			
P:	in Na	me	Fac	tor (	lu)	4								l		l	
	S			1									1				
	-			_										1			
														1			
			011+	+ D	rivin	$\exists$											
P	in Na	me		tor (		٠								l			
	X			18													
						Γ.					_						
						"	Mini	mum	valu	es for	or t	he ty	ypica	al o	perat	ina	g condition condition
										the							
								<u> </u>									
	Funct	ion T	able														
1															٦.		
	G1	G2+	G3	S3	S2 :	31	X7	X6	X5	X4	хз	X2	X1	χo			
							i								7		
	X	Н		X		`	Н	H	H	Н	H	H	H	H			
	L	Х		Х	X :	ζ.	H	Н	H	Н	Н	H	H	Н			
	н	L	,	L	L :		н	н	Н	н	Н	Н	Н	L			
	H	L		L	L	ł	H	Н	H	H	H	н	L	H			
	H	L		L		٠	Н	Н	H	H	H	L	H	H			
	H	L		L		Ŧ	H	H	H	H	L H	H H	H H	H H			
	H H	L		H		L H	H	H H	H L	L H	л Н	n H	н	H			
	н	Ī		H		Ĺ	н	L	H	Н	Н	H	H	H			
	н	L		н		H	L	H	H	H	H	H	H	H			
	L	L		L													
UH	B-DE6	-E3	Shee	t 1/2	2												Page 17-1:

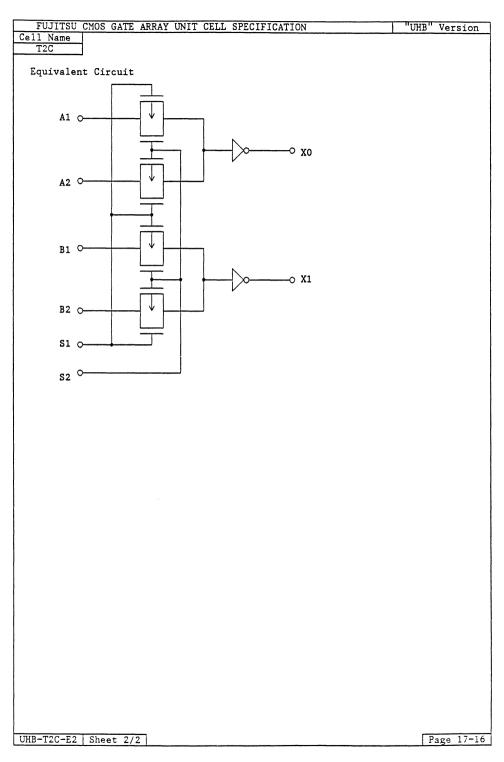


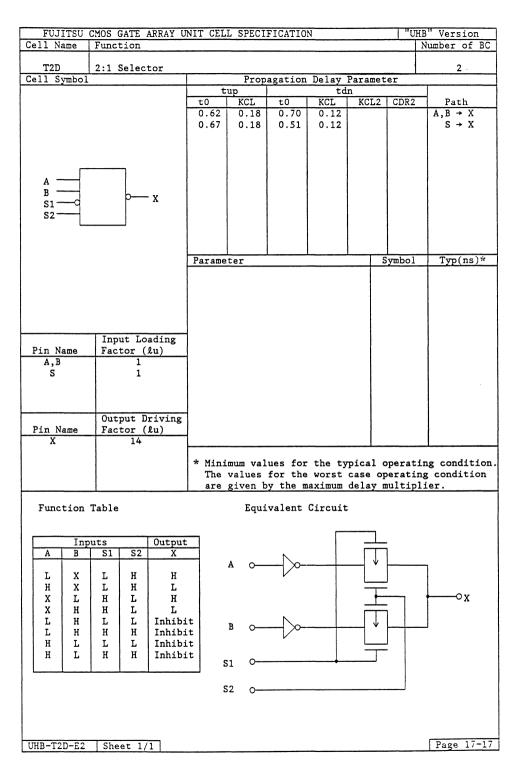


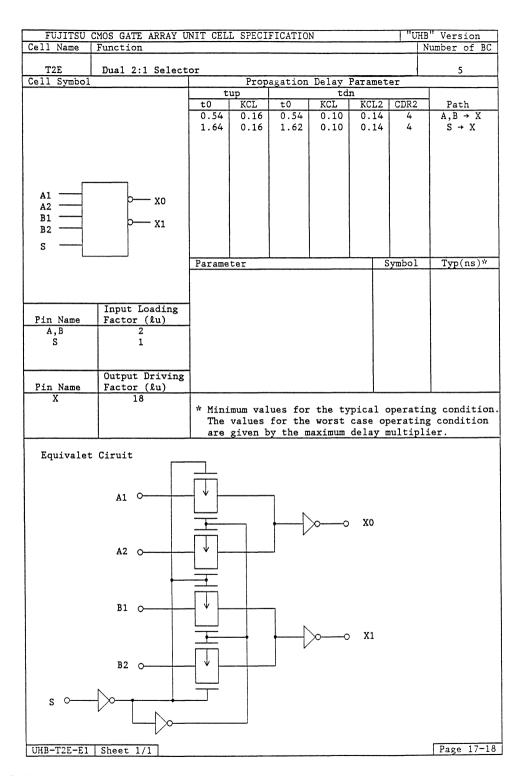
FUJITSU			AY UN	NIT CEL	L SPEC	IFICATIO	N		"បា	HB" Version
Cell Name	Functio	n								Number of BO
T2C	Dual 2:	1 0-1	+	-					- 1	4
Cell Symbol	Dual 2:	1 Sel	ec 101	•	Pro	pagation	Delay	Paramet	er	
Jell Dymbol			+	t.	gp	Jagation	td			T T
			F	t0	KCL	t0	KCL	KCL2	CDR2	Path
			r	0.51	0.16		0.09			$A,B \rightarrow X$
			1	0.67	0.16		0.09			$s \rightarrow x$
S1	S2		- 1							
1	1		-							
L <sub>C</sub>			- 1							
A1	p-	xo	1							
A2			l							
B1			l				1			
B2	0	X1	į			į				
										1
				Parame	± 0 =	_l	.l	L	ymbol	Typ(ns)*
			ŀ	rarame	rei				ушрот	Typ(IIS)"
								ŀ		}
								l		
								}		
								- 1		
	Input		ng							
Pin Name	Factor									
A,B		2								
S		2								
	Output	. D								
Din Namo	Factor									
Pin Name X		.8						l		
1	1 1	. •	ŀ							
				* Mini	mum va	lues for	r the tv	rpical o	perat	ing condition
										ng condition
						by the				
								-		
Function	Table									
		,								
Inpu A1,B1	ts A2,B2	S1	S2	Output		X1				

Inp	uts			Outputs	
A1,B1	A2,B2	S1	S2	X0	X1
L	x	L	н	н	н
H	X	L	H	L	L
X	L	H	L	H	Н
X	н	Н	L	L	L
L	н	L	L	Inhibit	Inhibit
Н	L	L	L	Inhibit	Inhibit
L	н	н	н	Inhibit	Inhibit
н	L	н	н	Inhibit	Inhibit

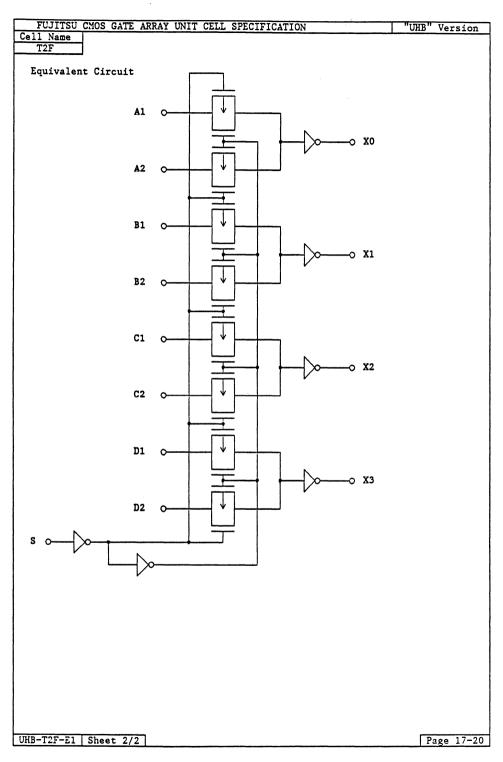
UHB-T2C-E2 | Sheet 1/2







FILITTSH C	MOS GATE ARRAY U	NIT CEL	CDECT	FICATIO	N		1171	HB" Version
	Function	NII CLL	L SILCI.	FICATIO	14	*****************	1 01	Number of BC
T2F Cell Symbol	2:1 Selector	r	Pron	acation	Delay	Donomo	+0=	8
Cell Symbol		t	up	agacion	td		tel	T
		t0	KCL	t0	KCL	KCL2		Path
		0.54	0.16	0.54	0.10	0.14	+ 4	A,B,
		1.64	0.16	1.62	0.10	0.14	4	$C,D \rightarrow X$ $S \rightarrow X$
		1.04	0.10	1.02	0.10	0.1-		
							1	
A1	⊳— xο						İ	
A2 B1								
B2	P X1							
C1	→ X2							
C2								
D2	р <del></del> хз							
s								
L		Parame	ter				Symbol	Typ(ns)*
						-		
						1		
						ł		
<u> </u>	Input Loading	1						
Pin Name	Factor (lu)							
A,B,C,D	2							
S	1							
		j						
	Output Driving							
Pin Name X	Factor (lu)	1						
	1							
		* Mini	mum val	ues for	the ty	pical	operat	ing condition.
		The	values	for the	worst aximum	delaw	operati: multin	ng condition
	<u> </u>	are	given b	y che ii	IAXIIIUIII	delay	шатетр	1161.
UHB-T2F-E1								Page 17-19



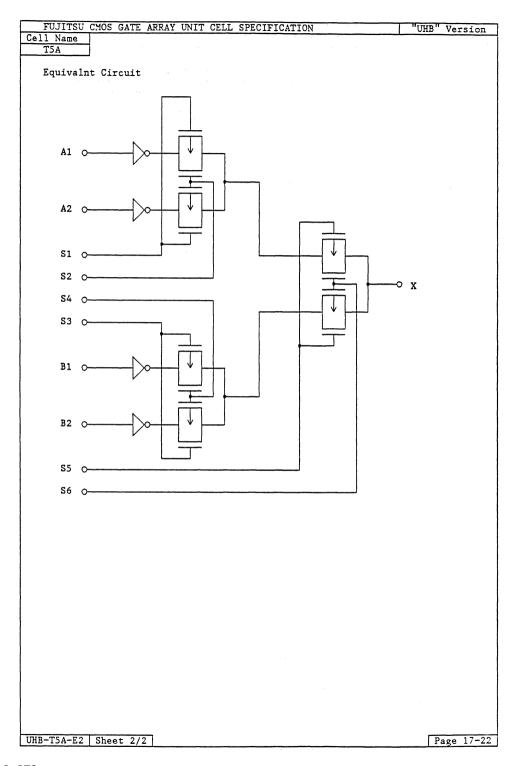
FULLESIL	ITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version									
	Function	1111 000	<u> </u>	LIONITO	.,			Number of BC		
	4:1 Selector							5		
Cell Symbol				agation	Delay td		er			
		to	up KCL	t0	KCL	KCL2	CDR2	Path		
		1.00	0.23	1.00	0.16	ROHZ	CDRZ	A,B + X		
		1.00	0.23	0.84	0.16			S1~4 + X		
S1 S	S1 S2 S3 S4			0.54	0.16		l	S5~6 → X		
							[			
لم ا							1			
A1							1	•		
A2	<u>_</u>						1			
B1	р—— х						l			
B2	İ						l			
4 ا	T							1		
							l	1		
85	S6									
		Parame	ter			S	ymbol	Typ(ns)*		
						1				
		}								
						1				
	Input Loading	1								
Pin Name	Factor (lu)							1		
A,B	1	1				1				
Ś	1					İ		İ		
	}	]								
		l								
		]						]		
D:	Output Driving	1								
Pin Name X	Factor (lu)	1								
^	,	<del></del>								
		* Mini	mum val	ues for	the tv	mical c	perat	ing condition		
		The	values	for the	worst	case or	erati	ng condition		
			given b							
T	N - 1 - 1 -									

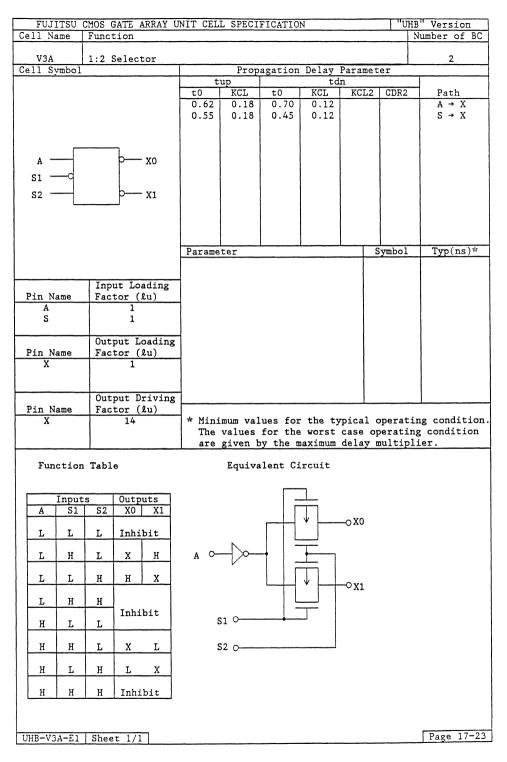
### Function Table

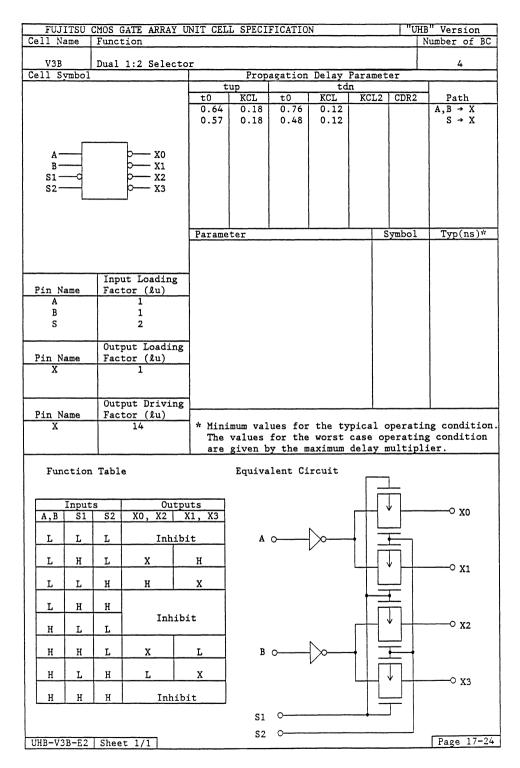
				Inp	uts					Output
A1	A2	B1	B2	S1	S2	S3	S4	S5	S6	X
L H	L H	L H	L H	L L H H	H H L	L L H H	H H L	L L H H H	H H H L L	H L H L H L

A1=A2  $\rightarrow$  S1=S2 or S5=S6 Inhibit B1=B2  $\rightarrow$  S3=S4 or S5=S6 Inhibit A1,A2=B1,B2 or S5=S6 Inhibit

UHB-T5A-E2 | Sheet 1/2





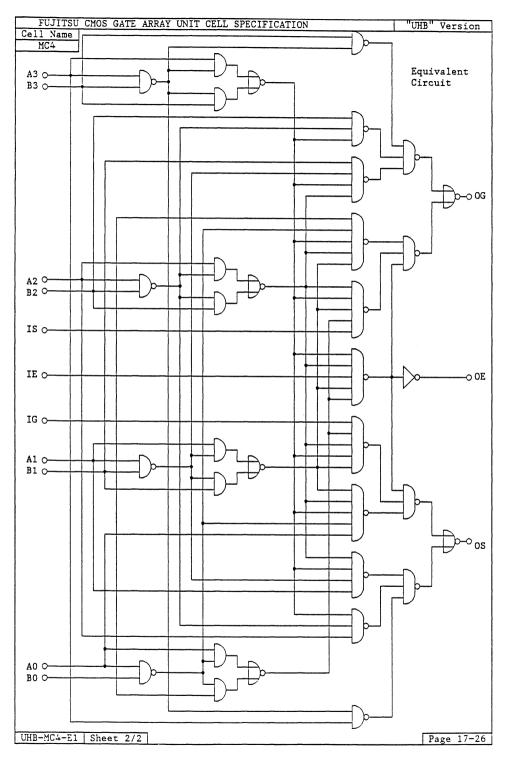


FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version									
Cell Name	Function							Number of BC	
MC4	4-bit Magnitude	Compar	ator			_		42	
Cell Symbol				agation	Delay		er	<del></del>	
		t0	up KCL	t0	KCL KCL	n KCL2	CDR2	— ", ", ", "	
		5.29	0.29	6.32	0.08	0.11	CDR2	Path A → OS	
		5.38	0.29	6.21	0.08	0.11	4	$B \rightarrow OS$	
		2.36	0.29	2.78	0.08	0.11	4	IE → OS	
A3 B3		1.93	0.29	2.41	0.08	0.11	4	IG → OS	
		5.18	0.29	6.53	0.08	0.11	4	A → OG	
A2 B2 ==================================		5.27	0.29	6.42	0.08	0.11	4	B → OG	
AO BO		2.25	0.29	2.99	0.08	0.11	4	IE → OG	
AU DU		2.13	0.29	2.31	0.08	0.11	4	IS → OG	
		5.69	0.16	4.36	0.09	0.12	4	A → OE	
IG-	OG	5.58	0.16	4.45	0.09	0.12	4	B → OE	
IE-	OE	2.14	0.16	1.43	0.09	0.12	4	IE → OE	
IS	os		0.10	1.75	0.05	0.122	· .		
		Parame	ter			S	ymbol	Typ(ns)*	
						1		}	
						1			
	T * *								
Pin Name	Input Loading Factor (lu)					}			
A A	3								
В	3								
IE	1								
IG	1							1	
IS	ī								
	_					l			
	Output Driving	1						1	
Pin Name	Factor (lu)								
OE	18							1	
OG	10								
os	10	* Mini	mum val	ues for	the ty	pical c	perat	ing condition	
		The	values	for the	worst	case or	erati	ng condition	
		are	given b	y the m	aximum	delay m	ultip	lier.	

### Function Table

	Comparin	g Inputs		Casca	ding In	puts	Outputs			
				IG	IS	IE	OG	OS	OE	
A3,B3	A2,B2	A1,B1	AO,BO	(A>B)	(A <b)< td=""><td>(A=B)</td><td>(A&gt;B)</td><td>(A<b)< td=""><td>(A=B)</td></b)<></td></b)<>	(A=B)	(A>B)	(A <b)< td=""><td>(A=B)</td></b)<>	(A=B)	
A3>B3	X	X	X	X	X	X	H	L	L	
A3 <b3< td=""><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>L</td><td>H</td><td>L</td></b3<>	X	X	X	X	X	X	L	H	L	
A3=B3	A2>B2	X	X	X	X	X	H	L	L	
A3=B3	A2 <b2< td=""><td>Х</td><td>X</td><td>X</td><td>Х</td><td>X</td><td>L</td><td>Н</td><td>L</td></b2<>	Х	X	X	Х	X	L	Н	L	
A3=B3	A2=B2	A1>B1	Х	Х	Х	X	н	L	L	
A3=B3	A2=B2	A1 <b1< td=""><td>X</td><td>Х</td><td>X</td><td>X</td><td>L</td><td>H</td><td>L</td></b1<>	X	Х	X	X	L	H	L	
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	Н	L	L	
A3=B3	A2=B2	A1=B1	A0 <b0< td=""><td>x</td><td>X</td><td>X</td><td>L</td><td>н</td><td>L</td></b0<>	x	X	X	L	н	L	
A3=B3	A2=B2	A1=B1	AO=BO	X	X	н	L	L	Н	
A3=B3	A2=B2	A1=B1	AO=BO	н	L	L	H	L	L	
A3=B3	A2=B2	A1=B1	AO=BO	L	н	L	L	Н	L	
A3=B3	A2=B2	A1=B1	AO=BO	н	н	L	L	L	L	
A3=B3	A2=B2	A1=B1	AO=BO	L	L	L	н	Н	L	
							ŀ			

UHB-MC4-E1 | Sheet 1/2



## **Bus Driver**

Page	Unit Cell Name	Function	Basic Cells
2-285	B41	4-bit Bus Driver	9

MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		TUI"UI	HB" Version
Function							Number of BC
/ 1 /- D - D /							
							9
	t		agacion				7
	t0	KCL	t0	KCL	KCL2	CDR2	Path
							$A \rightarrow X$
	2.50	0.07	1.90	0.06	l		C → X
<del></del>							
├── xo					1		
X1				1			
					İ		
Λ3					1		
	1				1		
	1				l		
					- 1		[
	Parame	ter		LI	1 8	vmho1	Typ(ns)*
	Tarame	261				ymbol	1 1 1 JP(IIIS)
	ł						1
					- 1		
	j				1		
Input Loading					- 1		
	l				į		
					ł		
1	1				ĺ		
Output Loading	1				- 1		
Factor (lu)	1				- 1		1
Factor (lu)							
Output Driving Factor (lu)							
1 Output Driving							
Output Driving Factor (lu)	* Mini	mum v.21	ues for	the tw	nical o	nerat	ing condition
Output Driving Factor (lu)	* Mini The	mum val	ues for	the type	pical opcase op	perat erati:	ing condition.
Output Driving Factor (lu)	The	values	for the	the type worst of aximum of	case op-	erati:	ng condition
Output Driving Factor (lu)	The	values	for the	worst o	case op-	erati:	ng condition
Output Driving Factor (Lu)	The are	values given b	for the	worst o	case op-	erati:	
Output Driving Factor (lu)	The are	values given b	for the	worst o	case op-	erati:	ng condition
Output Driving Factor (lu)  36	The are	values given b h UHB d	for the m	worst (	case opdelay m	erati: ultip	ng condition
Output Driving Factor (lu)  36	The are	values given b h UHB d	for the	worst (	case opdelay m	erati:	ng condition
Output Driving Factor (lu)  36  umber of B41 used	The are	values given b	for the medice	worst (	case opdelay m	erati: ultip	ng condition
Output Driving Factor (lu)  36	The are	values given b	for the m	worst (	case opdelay m	erati: ultip	ng condition
	Function  4-bit Bus Drive  X0  X1  X2  X3  Input Loading Factor (lu)  1  Output Loading	Function  4-bit Bus Driver  to 1.58 2.50  X0 X1 X2 X2 X3  Parame  Input Loading Factor (lu)  1 1 Output Loading	Function  4-bit Bus Driver	Function  4-bit Bus Driver	Propagation Delay I   tup   tdr   t0   KCL   t0   KCL   1.58   0.07   1.52   0.06   2.50   0.07   1.90   0.06	Propagation Delay Parameter   Tup   tdn   t0   KCL   t0   KCL   t0   KCL   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   t0   tdn   tdn   t0   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn   tdn	Propagation Delay Parameter   Tup   Tdn   To   KCL   t0   KCL   KCL2   CDR2

C-830UHB

C-1200UHB

C-1700UHB

C-2200UHB

UHB-B41-E3 | Sheet 1/2

6

8

12

16

C-6000UHB

C-8700UHB

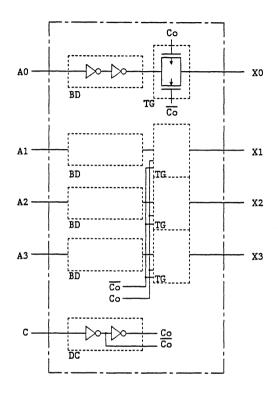
C-12000UHB

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50

70 90 FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version
Cell Name
B41

Equivalent Circuit



#### Note:

- $\cdot$  TG is configured using the special transmission gates buried in the channel area of the UHB devices.
- $\cdot$  BD and DC use the regular internal baisc cells in the UHB devices.
- $\cdot$  A Bus Terminator is invisible to logic designers and is automatically connected to each Bus line, when B41 is used.

UHB-B41-E3 | Sheet 2/2

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## 2

# Clip Cells

Page	Unit Cell Name	Function	Basic Cells
2-289	Z00	0 Clip	0
2-290	Z01	1 Clip	0
2-291	KD2	Load Gate (Fan-in = 2)	1

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB							HB" Version	
Cell Name	Function							Number of BC
700	0.01:5						l	_
Z00 Cell Symbol	0 Clip		Prop	agation	Delay	Paramet	er 1	0
JOIL BYMBOI		t	up	agaston	td	n	<u> </u>	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
								1
	x							1 1
	1							
	$\wedge$							
					İ			
							}	
		Parame	ter			S	ymbol	Typ(ns)*
			***************************************					
						-		
	Input Loading					1		
Pin Name	Factor (lu)							
						1		
						l		
	Output Driving							
Pin Name	Factor (lu)							· ·
Х	200							
		* Mini	mum 1101	une for	+ha +v	nical c	nerat	ing condition.
		The	values	for the	worst	case or	erati	ng condition
		are	given b	y the m	aximum	delay m	ultip	lier.
		·						
1								
1								
	·							- 10 1
UHB-Z00-E1	Sheet 1/1							Page 19-1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UH	B" Version
Cell Name	Function							Number of BC
701	1 61							
Z01 Cell Symbol	1 Clip		Pron	agatio-	Dolar	Daramat	<u> </u>	0
CEIT SAMPOI		t	up rrop	agation	Delay td	n aramet	<u>e</u> т	T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
	<del></del>							
	\/							
	Y							
	x							
	Δ							
		Parame	ter	L	I	l s	ymbol	Typ(ns)*
							-	
						l		
	Input Loading							
Pin Name	Factor (lu)							
	Output Driving	1				ĺ		
Pin Name	Factor (lu)							
X	200	<u> </u>						
				_	.1			
		" Mini	mum val	ues for	the ty	pical c	perati	ng condition. g condition
		are	values	ror the m	aximum	delay n	multipl	ier.
		, 416	0	,				
1								
UHB-Z01-E1	Sheet 1/1							Page 19-2

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UH	B" Version
Cell Name	Function				B" Version Number of BC			
KD2	Load Gate Fan-i	n = 2						1
Cell Symbol				agation	Delay	Paramet	er	
			up		td			_
		t0	KCL	t0	KCL	KCL2	CDR2	Path
							1	
							1	1
			1				1	İ
							1	
	N						ł	
Α								
			[					
							1	
							l	
			Ļ		L	L	<u></u>	<del></del>
		Parame	ter			S	ymbol	Typ(ns)*
								1
						ļ		
								1
	Input Loading							
Din Nama	Factor ((u)							
Pin Name A	Factor (lu)							
h								
						1		
	Output Driving	1						
Pin Name	Factor (lu)							
1211 1141110	140001 (24)	1				- 1		
								<del> </del>
		* Mini	mum val	ues for	the tv	pical c	perati	ng condition.
		The	values	for the	worst	case or	eratin	ng condition
		are	given b	y the m	aximum	delay	ultipl	ier.
			· · · · · · · · · · · · · · · · · · ·					
	1 21							<u> </u>
UHB-KD2-E1	Sheet 1/1							Page 19-3

## I/O Buffer Family

Page	Unit Cell Name	Function	Basic Cells
Input But	ifers		
2-295 2-296 2-297 2-298 2-299 2-300 2-301 2-302 2-303 2-304 2-305 2-306 2-307 2-308 2-310 2-311 2-312 2-313 2-314 2-315 2-316 2-317 2-318 2-319 2-319 2-320 2-321 2-322 2-323	11B 11BU 12BU 12BU 12BB 12BB 12BB 11CD 11CD 11CD 12CUD 11SU 11SU 11SD 11RD 12SU 12SU 11RD 12RD 12RD 12RD	Input Buffer  11B with Pull-up Resistance  11B with Pull-down Resistance  Input Buffer  12B with Pull-up Resistance  12B with Pull-up Resistance  12B with Pull-down Resistance  12B with Pull-up Resistance  12B with Pull-up Resistance  12B with Pull-up Resistance  12B with Pull-up Resistance  12B with Pull-up Resistance  12B with Pull-up Resistance  11C with Pull-up Resistance  11C with Pull-up Resistance  11C with Pull-up Resistance  12C with Pull-up Resistance  12C with Pull-up Resistance  12C with Pull-up Resistance  12S with Pull-up Resistance  11S with Pull-down Resistance  11S with Pull-down Resistance  12S with Pull-down Resistance  12S with Pull-down Resistance  12S with Pull-down Resistance  12S with Pull-down Resistance  12S with Pull-down Resistance  12S with Pull-up Resistance  11R with Pull-up Resistance  12R with Pull-up Resistance  12R with Pull-up Resistance	555444444666555544448888886668888
Output B	uffers		
2-325 2-326 2-327 2-328 2-329 2-330 2-331 2-332 2-333 2-334 2-335 2-336 2-337 2-338 2-340 2-341 2-342 2-343 2-344	01B 01L 01R 01S 02B 02L 02R 02S 02S2 04R 04S 04S 04T 04W 01BF 01BF 02BF 02RF 04RF 04TF	Output Buffer Power Output Buffer Output Buffer Power Output Buffer Output Buffer Output Buffer Power Output Buffer Output Buffer Power Output Buffer High Power Output Buffer Output Buffer Power 3-state Output Buffer Output Buffer Power 3-state Output Buffer Output Buffer Output Buffer Output Buffer Output Buffer Output Buffer Output Buffer Output Buffer Output Buffer Output Buffer 3-state Output Buffer	33552244655744352454
		iers (Buses)	
2-345 2-346 2-347	H6TU H6TU H6TD	3-state Output and Input Buffer H6T with Pull-up Resistance H6T with Pull-down Resistance	8 8 8

## I/O Buffer Family (Continued)

2-348 2-349 2-350 2-351 2-352 2-353	H6WU H6WD H6C H7CU H6CD	Power 3-state Output and Input Buffer H6W with Pull-up Resistance H6W with Pull-down Resistance 3-state Output and CMOS Interface Input Buffer H6C with Pull-up Resistance H6C with Pull-down Resistance	8 8 8 8 8
Output Bu	ıffers		
2-354 2-355 2-356 2-357 2-358 2-359 2-360 2-361 2-362 2-363 2-365 2-366 2-367 2-370 2-377 2-377 2-377 2-377 2-377 2-377 2-377 2-377 2-378 2-377 2-380 2-381 2-384 2-388 2-389 2-390 2-391 2-391 2-392 2-393 2-394 2-395 2-397	H6EEUD H6ESSUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD H6ESRUD	Power 3-state Output and CMOS Interface Input Buffer H6E with Pull-up Resistance H6E with Pull-down Resistance 3-state Output and Schmitt trigger Input Buffer H6S with Pull-up Resistance 3-state Output and Schmitt trigger Input Buffer H6R with Pull-up Resistance 3-state Output and Input Buffer H6R with Pull-up Resistance H6R with Pull-up Resistance H6R with Pull-up Resistance H8T with Pull-up Resistance H8T with Pull-up Resistance H8T with Pull-up Resistance H8W with Pull-up Resistance H8W with Pull-up Resistance H8W with Pull-up Resistance H8W2 with Pull-up Resistance H8W2 with Pull-up Resistance H8W2 with Pull-up Resistance H8C with Pull-up Resistance H8C with Pull-up Resistance H8C with Pull-up Resistance H8E with Pull-up Resistance H8E with Pull-up Resistance H8E with Pull-up Resistance H8E2 with Pull-up Resistance H8E2 with Pull-up Resistance H8E2 with Pull-up Resistance H8E3 with Pull-up Resistance H8E4 with Pull-up Resistance H8E5 with Pull-up Resistance H8E6 With Pull-up Resistance H8E7 with Pull-up Resistance H8E8 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance H8E9 with Pull-up Resistance	888112121129999991111 9999999111111333338888889999999
2–398 Oscillator	H8CFD Circuits	H8CF with Pull-down Resistance	9
2–399	IT10	Input Buffer for Oscillator	0
2-400 2-401	HOC HOS	Output Buffer for Oscillator and Input Buffer	8
2-401	HOCR	Output Buffer for Oscillator and Schmitt trigger Input Buffer Output Buffer for Oscillator	8 8

FILITTSII C	MOS GATE ARRAY U	NIT CEL	CDECT	FICATIO	N		עוויי	B" Version
Cell Name	Function	VII OLL	D BILCI.	r ICATIO.	14		1 011	Number of BC
IlB	Input Buffer (I	nverter	)					5
Cell Symbol				agation	Delay		er	
			up	+0	td		CDDO	ا ہے۔
		t0	KCL 0.04	t0	KCL	KCL2	CDR2	Path X → IN
		1.60	0.04	1.54	0.04			X → IN
							1	1
							į	1
							İ	
								1 1
1,	_						i	1
x —	>>- IN							
							İ	1
							<u></u>	+
		Parame	ter .			-   8	ymbol	Typ(ns)*
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						- 1		
						ļ		
	Input Loading					l		
Pin Name	Factor (lu)					Ì		
						ĺ		
								1
						,		
		ŀ				1		1
Dia Mana	Output Driving					- 1		
Pin Name IN	Factor (lu)					1		
IN	36							
1		* Mini	mum val	ues for	the tv	mical o	perati	ing condition.
		The	values	for the	worst	case of	eratin	ng condition
		are	given b	y the m	naximum	delay r	multipl	lier.
1								
UHB-I1B-E1	Sheet 1/1							Page 20-1
	····							

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UH	B" Version
Cell Name	Function						1	Number of BC
	Input Buffer (I:	nverter	)					
I1BU	with Pull-up Res	istance						5
Cell Symbol				agation	Delay		er	
			up	+0	td		CDR2	- Path
		t0 1.60	KCL 0.04	t0 1.54	KCL 0.04	KCL2	CDK2	Path X → IN
		1.60	0.04	1.54	0.04			A → IN
۲	_							
х —	>>- IN							
L								
								1
		Parame	† A T	L		1 6	ymbol	Typ(ns)*
		гагаше	CCT				2 mpOT	Typ(IIS)"
						1		
						1		
	Input Loading							
Pin Name	Factor (lu)							
								1
						l		
	Output Driving							
Pin Name	Factor (lu)							
IN	36							
		* Mini	mum val	ues for	the ty	pical c	perati	ng condition.
		The	values	for the	worst	case or	eratin	g condition
	<u> </u>	are	given b	y the m	aximum	delay m	ultipl	ier.
		•						
UHB-I1BU-E1	Sheet 1/1							Page 20-2

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UHI	B" Version
Cell Name	Function						1	Number of BC
	Input Buffer (I	nverter	)					
I1BD	with Pull-down R	esistan	D=0=	agatio-	Dolar	Daramat	<u>_</u>	5
Cell Symbol		+-	up	agation	td		<u>e1</u>	1
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.60	0.04	1.54	0.04			X + IN
		İ						
	_							1 1
х	>>- IN							
					T(nc)*			
		Parame	rei			-   S	ymbol	Typ(ns)*
						}		1
						l		
Dim Nama	Input Loading Factor (lu)					1		
Pin Name	ractor (ku)							
	Ì							
								1
	Output Driving							
Pin Name IN	Factor (lu)							
IN	30							_L
		* Mini	mum val	ues for	the ty	pical c	perati	ng condition.
		The	values	for the	worst	case or	eratin	g condition
		are	given b	y the m	aximum	delay m	ultipl	ier.
1								
UHB-I1BD-E1	Sheet 1/1							Page 20-3

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			IB" Version
Cell Name	Function							Number of BC
I2B	Input Buffor (T	rue)						4
Cell Symbol	Input Buffer (T	106)	Prop	agation	Delay	Paramet	er	<u>-</u>
			up		td	n .		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.06	0.04	1.84	0.04			X → IN
х	IN							
		Parame	ter		I	<u> </u>	Symbol	Typ(ns)*
						1		
						1		
						1		
	Input Loading							
Pin Name	Factor (lu)	ł						
		]						
	10 · · · · · · · · · · · · · · · · · · ·	1						
Pin Name	Output Driving Factor (lu)							
IN	36	1						
		* Mini	mum val	ues for	the ty	pical	operat	ing condition.
		The	values given b	for the n	worst	delay	perati multip	ng condition
		l are	0	,				
TTL Equiva	lent Circuit							
[	7							
1								
7/00/								
74S04 74LS04	74S04 74LS04							
772504	, ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,							
UHB-I2B-E1	Sheet 1/1							Page 20-4

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UH	B" Version
Cell Name	Function							Number of BC
	Input Buffer (T	rue)					Γ	, 7
I2BU	with Pull-up Res	istance	D		D - 1			4
Cell Symbol		+-	up Prop	agation	Delay td		er	- <del></del>
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.06	0.04	1.84	0.04	ROBL	ODICE	X + IN
		1.00		110				
								1
1								
х —	IN				'			
•								
							l	
							1	
		Parame	ter			S	ymbol	Typ(ns)*
								1
	1							
Pin Name	Input Loading Factor (lu)							
FIII Name	ractor (Eu)							
						ľ		
						ł		
						ļ		
	Output Driving					-		
Pin Name	Factor (lu)							
IN	36							
		Jan 10						
		* Mini	mum vai	ues ror	the ty	picai c	perati	ng condition.
		ine	varues	ror the m	aximum	delaw n	miltini	ng condition
·		are	given r	y the n	aximum	delay ii	101 01 01	.161.
								1
UHB-I2BU-E1	Sheet 1/1							Page 20-5
	1 -11-00 1/1							

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"បា	HB" Version
Cell Name	Function							Number of BC
	Input Buffer (T	rue)						
I2BD	with Pull-down R	esistan	ce					4
Cell Symbol		<del></del>	Prop	agation	Delay	raramet	er	7
		t0	up KCL	t0	td KCL	n KCL2	CDR2	- Park
		1.06	0.04	1.84	0.04	KCL2	CDR2	Path X → IN
		1.00	0.04	1.04	0.04			ATIN
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		Parame		L		<del>ل                                    </del>	ymbol	Tarm (ma)*
		rarame	rer			<del>-   -</del>	yabot	Typ(ns)*
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	Input Loading							
Pin Name	Factor (lu)					Ì		
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	Output Driving	1						
Pin Name	Factor (lu)	1				1		
IN	36							
		* Mini	mum val	ues for	the ty	pical o	perat	ing condition
		The	values	for the	worst	case of	erati	ng condition
		are	given b	y the m	aximum	delay n	ultip	lier.
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UHB-I2BD-E	1   Sheet 1/1							Page 20-6

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	Ŋ		т"ОН	B" Version
	Function							Number of BC
IKB	Clock Input Buff	er (In	verter)					4
Cell Symbol	CIOCK INPUE BUIL	<u>er (111</u>	Prop	agation	Delay	Paramet	er	
			up		td	n		
		t0 2.37	KCL 0.02	t0 1.82	KCL 0.02	KCL2	CDR2	Path X → CI
		2.37	0.02	1.02	0.02			A 7 01
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		Parame	ter			l s	ymbol	Typ(ns)*
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Pin Name	Input Loading Factor (lu)					į		
TIM Name	Tactor (24)							1
						- 1		
	Output Driving							
Pin Name CI	Factor (lu)					- 1		
61	130							
		* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
		The	values	for the	worst	case op	eratin	g condition
	<u> </u>	are	given b	y the m	aximum	deray m	ultipi	ler.
TTL Equival	ent Circuit							
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UHB-IKB-E2	Sheet 1/1							Page 20-7

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		ש"ט	HB" Version
	Function							Number of BC
	Clock Input Buff	er (In	verter)					
IKBU	with Pull-up Res	istance						4
Cell Symbol				agation	Delay	Paramet	er	
			up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.37	0.02	1.82	0.02			X → CI
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		Parame	tor	L	L	٠ ٦ -	ymbol	Typ(ns)*
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	Input Loading					1		
Pin Name	Factor (lu)							
1111 Mame	ractor (xu)							
						- 1		
	Output Driving					- 1		
Pin Name	Factor (lu)							
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01	150							
		* Mini	mum val	ues for	the tv	pical c	perat	ing condition.
		The	values	for the	worst	case or	erati	ng condition
		are	given b	y the m	aximum	delav m	ultip	lier.
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TTL Equiva:	lent Circuit							
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UHB-IKBU-E2	Sheet 1/1							Page 20-8

TUTTOU O				TTO 1 MTO			1 11/17/19	.,
	MOS GATE ARRAY U	NIT CEL	L SPECI.	FICATIO	N			Version
Cell Name	Function Clock Input Buff	er (In	verter					Number of BC
IKBD	with Pull-down R	esistan	CE					4
Cell Symbol		001000	Prop	agation	Delay	Paramet	er	
		t	up		td	n		
1		t0	KCL	t0	KCL	KCL2	CDR2	Path
ĺ		2.37	0.02	1.82	0.02			X → CI
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Pin Name	Input Loading Factor (lu)							
FIII Name	ractor (xu)							
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	Output Driving	1						
Pin Name	Factor (lu)	]				ł		
CI	150							
		* Mini	mum val	ues for	the ty	pical c	perati	ng condition.
		The	values	for the	worst	case or	erating	condition
	<u> </u>	are	given b	y the m	aximum	delay n	ultipl:	ier.
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UHB-IKBD-E2	Sheet 1/1							Page 20-9
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FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		T"UI	HB" Version
Cell Name	Function							Number of BC
		/m	>					
ILB Cell Symbol	Clock Input Buff	er (Tr	ue) Prop	agation	Delav	Paramet	er l	6
		tı	up	-3	td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path X → CI
		2.03	0.02	2.56	0.02			X → CI
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		ter			l s	ymbol	Typ(ns)*	
		101000					,	
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	Input Loading							
Pin Name	Factor (lu)							
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	Output Driving							
Pin Name	Factor (lu)							ļ
CI	150							
		* Mini	mum val	ues for	the ty	pical c	perat:	ing condition.
		The	values	for the	worst	case op	erati	ng condition
	J	are	given b	y the m	axımum	сетау п	uitip.	lier.
UHB-ILB-E2	Sheet 1/1							Page 20-10

FULL POLICE	WOO CAME ADDAY I	NITT OF	T CDECT	CTCATTO			1 11777	711 11
	MOS GATE ARRAY U	NII CEL	L SPECI.	L TCALLO	in		I UH	B" Version Number of BC
JCII .iame	Clock Input Buff	er (Tr	ue)					amber of bo
ILBU	with Pull-up Res	istance	-,				1	6
Cell Symbol			Prop	agation	Delay	Paramet	er	
			up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path X → CI
		2.03	0.02	2.56	0.02			X → CI
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		Parame	ter			l .	vmbol	Typ(ns)*
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	Output Driving							1
Pin Name	Factor (lu)							
CI	150							
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		" Mini	mum val	ues for	the ty	pical c	perati	ng condition. g condition
		are	values given b	A the w	aximum	delav m	ultin	ier.
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TTL Equival	ent Circuit							
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UHB-ILBU-E2	Sheet 1/1							Page 20-11

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"บห	B" Version
Cell Name	Function							Number of BC
	Clock Input Buff	er (Tr	ue)					
ILBD	with Pull-down R	esistan	се					6
Cell Symbol				agation			er	
			up		td			
	,	t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.03	0.02	2.56	0.02			X → CI
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Parameter Symbol								Typ(ns)*
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	Input Loading					- 1		
Pin Name	Factor (lu)							
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	Output Driving					1		
Pin Name	Factor (lu)					1		
CI	150							<u> </u>
		J. 14						
		" Mini	mum vai	ues for	the ty	pical c	perati	ing condition. ng condition
		270	values	y the m	avimum	delaw n	nultin	ier
	<u> </u>	are	given b	y the n	IAXIMUM	delay i	шитетр	iter.
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UHB-ILBD-E2	Sheet 1/1							Page 20-12

FILITTEIL (	CMOS GATE ARRAY U	NIT CEL	T SDECT	FICATIO	NI.		THIT	" Version
	Function	NII CLL	D SILCI.	FICATIO	14		I N	Number of BC
I1C	CMOS Interface I	nput Bu	ffer (	Inverte	r)			5
Cell Symbol				agation	Delay		er	
			up		td		GDDG	1 1
		t0	KCL	t0	KCL	KCL2	CDR2	Path X → IN
		1.32	0.04	1.44	0.04			$X \to IN$
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x	>> IN							
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		Parame	ter			l s	ymbol	Typ(ns)*
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	Input Loading							
Pin Name	Factor (lu)							
TIII Name	Tactor (xa)							
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	Output Driving					1		
Pin Name IN	Factor (lu)					1		1
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		* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
		The	values	for the	worst	case of	perating	g condition
		are	given b	y the m	aximum	delay n	ultipl:	ier.
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UHB-I1C-E1	Sheet 1/1							Page 20-13
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FULLTSU (	CMOS GATE ARRAY U	NIT CEL	L SPECT	FICATIO	N		n <sub>t1</sub>	HB" Version
	Function	000	- 0.101	- 1011110	·			Number of BC
	CMOS Interface I	nput Bu	ffer (	Inverte	<del>r</del> )			
I1CU	with Pull-up Res	istance	(		- /		l	5
Cell Symbol	"LUI LUII UP NES	-2	Prop	agation	Delay	Ратата	PT	
	<u>-</u>	+	up	-5001011	td		<u></u>	
		t0	KCL	t0	KCL	KCL2	CDR2	Path
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		1.54	0.04	1.44	0.04			V - 11
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		Parame	ter			S	ymbol	Typ(ns)*
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	Input Loading					1		
Pin Name	Factor (lu)					]		1
TITI MAME	Lactor (Lu)	1						1
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<b></b>	Output Driving	1						
Pin Name	Factor (lu)	1				1		
IN	36							1
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		* Mini	mum val	ues for	the ty	pical c	perat	ing condition.
		The	values	for the	worst	case of	erati	ng condition
		are	given b	y the m	aximum	delay n	ultip	olier.
UHB-I1CU-E1	Sheet 1/1							Page 20-14

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UHE	B" Version
Cell Name	Function						N	Number of BC
	CMOS Interface I	nput Bu	ffer (	Inverte	r)			
I1CD	with Pull-down R	esistan	ce					5
Cell Symbol			Prop	agation	Delay:	Paramet	er	
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.35	0.04	1.44	0.04			X → IN
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		Daras	tor			٦ ,	ymbol	Typ(ns)*
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	Input Loading							1
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	Output Driving					i		
Pin Name	Factor (lu)					1		
IN	36							
		* Mini	mum val	ues for	the ty	pical c	perati	ng condition.
		The	values	for the	worst	case or	eratin	g condition
		are	given b	y the m	aximum	delay m	ultipl	ier.
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UHB-I1CD-E1	Sheet 1/1							Page 20-15
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FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECT	FICATIO	N		<b>"</b> UI	HB" Version
Cell Name	Function						1	Number of BC
i								
I2C	CMOS Interface I	nput Bu	ffer (T	rue)				4
Cell Symbol				agation			er	
			up	+0	td		0000	-  <sub>5</sub> ,
		t0 0.92	KCL 0.04	t0 1.33	KCL 0.04	KCL2	CDR2	Path X → IN
		0.92	0.04	1.33	0.04			$X \rightarrow IN$
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		Parame	ter			S	ymbol	Typ(ns)*
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	Input Loading							
Pin Name	Factor (lu)							
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D/- N	Output Driving							
Pin Name IN	Factor (lu)					ı		
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		* Mini	mum val	ues for	the tv	pical c	perat	ing condition.
		The	values	for the	worst	case or	erati	ng condition
		are	given b	y the m	aximum	delay n	ultip	lier.
UHB-I2C-E2	Sheet 1/1		_					Page 20-16

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECT	FICATIO	N		"UHB	" Version
Cell Name	Function	IVII ODD	D DI DOI.	TOMITO	.,		IN	umber of BC
	CMOS Interface I	nput Bu	ffer				<del> ``</del>	
12CU	with Pull-up Res	istance	(True)					4
Cell Symbol			Prop	agation	Delay	Paramet	er	
		t	up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.92	0.04	1.33	0.04			Path X → IN
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Pin Name	Factor (lu)					}		
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Pin Name	Factor (lu)	ļ						1
IN	36							l
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		" mini	mum vai	ues for	the ty	picar	peratin	ng condition.
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UHB-I2CU-E	2   Sheet 1/1							Page 20-17
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FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		ט" [	JHB" Version
Cell Name	Function							Number of BC
	CMOS Interface I:	nput Bu	ffer					
I2CD	with Pull-down R	esistan	ce (Tru	e)				4
Cell Symbol				agation	Delay		er	
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	
		0.92	0.04	1.33	0.04			X → IN
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	Input Loading					1		
Pin Name	Factor (lu)							
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n	Output Driving					1		
Pin Name	Factor (lu)	1						
IN	36							
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		are	given h	v the m	naximum	delay r	nulti	plier.
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FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UH	B" Version
Cell Name	Function							Number of BC
	Schmitt Trigger	Input B	uffer					
I1S	(CMOS Type, Inve							8
Cell Symbol				agation	Delay		er	
			up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		3.90	0.16	2.68	0.08		ĺ	X → IN
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	Output Driving					ł		
Pin Name	Factor (lu)					- 1		
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		* Mini	mim val	ues for	the tv	nical c	perati	ng condition.
		The	values	for the	worst	case or	eratin	g condition
		are	given b	v the m	aximum	delav n	ultipl	ier.
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UHB-I1S-E1	Sheet 1/1							Page 20-19

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		ייָּטיִוי	B" Version
Cell Name	Function Schmitt Trigger	Innut P	uffe=					Number of BC
IISU	(CMOS Type, Inve	rter) w	ith Pul	l-up Re	sistanc	e	-	8
Ceil Symbol			Prop	agation	Delay	Paramet	er	
			up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		3.90	0.16	2.68	0.08			X → IN
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		Parame	ter			S	ymbol	Typ(ns)*
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	Input Loading							
Pin Name	Factor (lu)							
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	Output Driving	1						1
Pin Name	Factor (lu)	1				ł		
IN	18							
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		* Mini	mum val	ues for	the ty	pical o	perat	ing condition.
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UHB-I1SU-E	1   Sheet 1/1							Page 20-20

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UH	B" Version
	Function							Number of BC
	Schmitt Trigger	Input B	uffer					
I1SD	(CMOS Type, Inve	rter) w	ith Pul	l-down	Resista	nce		8
Cell Symbol			Prop	agation	Delay	Paramet	er	
		t	up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		3.90	0.16	2.68	0.08			Path X → IN
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	Output Driving							
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IN	18							
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	1	* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
		The	values	for the	worst	case or	eratin	g condition
		are	given b	y the m	aximum	delay n	ultipl	ier.
UHB-I1SD-E1	Sheet 1/1							Page 20-21

FULTITOU C	MOS GATE ARRAY U	NIT CEL	L SPECT	FICATIO	N		utin	B" Version
	Function	.111 (11)	L OFFOI.	TOULTO	.,		1 01	Number of BC
	Schmitt Trigger	Input R	uffer					
I2S	(CMOS Type, True	)					1	8
Cell Symbol	,, -100		Prop	agation	Delay	Paramet	er	-
		t	up	3	td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.48	0.16	3.08	0.10			X + IN
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	Input Loading							
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	Output Driving							
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		are	given h	v the m	aximum	delay n	ultip	lier.
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UHB-I2S-E1	Sheet 1/1							Page 20-22

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"[]	HB" Version
	Function							Number of BC
	Schmitt Trigger	Input B	uffer					
I2SU	(CMOS Type, True	) with !	Pull-up	Resist	ance			8
Cell Symbol				agation			er	
			up		td		anna	
		t0	KCL	t0	KCL	KCL2	CDR2	
		2.48	0.16	3.08	0.10			X → IN
							1	
	_						l	
х —	√ IN						l	
••								
								1
		Parame	ter			S	ymbol	Typ(ns)*
						- 1		
	Input Loading							
Pin Name	Factor (lu)							
IIII Name	ractor (ku)							
						ļ		
	Output Driving							
Pin Name	Factor (lu)					1		
IN	18							
		* M:-:	1	f	+	-:1 -	+	ing condition.
		The	mom var	for the	worst	bicai c	perat	ng condition.
		are	given h	y the m	aximum	delav m	ultip	lier.
			82.011	,				
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UHB-I2SU-E1	Sheet 1/1							Page 20-23

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UHE	" Version
Cell Name	Function						l N	Number of BC
	Schmitt Trigger	Input B	uffer					
I2SD	(CMOS Type, True	) with	Pull-do	wn Resi	stance		-	8
Cell Symbol		·	Prop	agation	Delay	Paramet	er	
		t	up		td			T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.48	0.16	3.08	0.10			X → IN
								1
х —	√ IN							
A I	<u> </u>							
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		Parame	ter	L	L	٠ ٦ ٥	ymbol	Typ(ns)*
		таташе	267			<del></del>	, moo1	1,5(115)
						İ		
						1		
	Input Loading							
Pin Name	Factor (lu)							
I III Name	Tactor (xu)							
								ĺ
		İ				i		
	Output Driving					1		
Pin Name	Factor (lu)							
IN	18							
	1							1
	İ	* Mini	mum val	ues for	the ty	mical o	perati	ng condition.
		The	values	for the	worst	case or	perating	g condition
		are	given h	v the n	aximum	delav	nultipl	ier.
			0-10	, , , , , ,				
UHB-12SD-F1	Sheet 1/1							Page 20-24

FUJITSU C	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UH	B" Version
	Function							Number of BC
	Schmitt Trigger	Input B	uffer					
I1R	(TTL Type, Inver	ter)						8
Cell Symbol				agation	Delay	Paramet	er	
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		4.48	0.16	2.36	0.08			X → IN
								1
								1
								1
,	<del></del>							
x —	Д>>>— IN							
		Parama	tor	لـــــا	L	1 6	ymbol_	Typ(ns)*
		Parame	rei			<del>-                                     </del>	Ampot	Typ(IIS)"
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	Input Loading							
Pin Name	Factor (lu)					- 1		
1 211 1101110	1					1		
						1		1
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								1
								l
	Output Driving							
Pin Name	Factor (lu)							
IN	18					- 1		
		* Mini	mum val	ues for	the tv	pical o	perati	ng condition.
		The	values	for the	worst	case op	eratin	g condition
		are	given b	y the m	aximum	delay m	ultipl	ier.
	<u> </u>							
1010 TAN NO 1	63							D 00 05
UHB-I1R-E2	Sneet 1/1							Page 20-25

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UH	B" Version
Cell Name	Function							Number of BC
	Schmitt Trigger	Input B	uffer					
I1RU	(TTL Type, Inver	ter) wi	th Pull	-up Res	istance			8
Cell Symbol			Prop	agation	Delay	Paramet	er	
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		4.48	0.16	2.36	0.08		ł	X → IN
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х —	<u>1</u> 5>>─ IN						1	
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		Parame	ter	L ,	L	ء ا	ymbol	Typ(ns)*
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						- 1		1
	Input Loading					- 1		
Pin Name	Factor (lu)							
						- 1		
						1		
	Output Driving					1		
Pin Name	Factor (lu)	l				1		
IN	18	ļ						
	1	* Mimi	m11m *** 1	ne for	the +=	mical -	mara+4	ing condition.
		The	walues	for the	worst	Case Of	peratit	ng condition
		are	given b	v the m	aximum	delay n	nultipl	ier.
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UHB-I1RU-E2	Sheet 1/1							Page 20-26

FUJITSU C	MOS GATE ARRAY U	"UH	B" Version					
Cell Name	Function							Number of BC
	Schmitt Trigger	Input B	uffer					
I1RD	(TTL Type, Inver	ter) wi	th Pull	-down R	<u>esista</u> n	ce		. 8
Cell Symbol			Prop	agation	Delay	Paramet	er	
		t t	up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		4.48	0.16	2.36	0.08			X → IN
								i
								1
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1	_						İ	
х —	<b>√&gt;</b> → IN						ł	
L							1	
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		Parame	ter			S	ymbol	Typ(ns)*
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						- 1		1
	Input Loading							1
Pin Name	Factor (lu)							1
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								ł
						į		ł
	Output Driving							
Pin Name	Factor (lu)					ı		<b>!</b>
IN	18							
		* Mini	mum val	ues for	the ty	pical o	perati	ng condition.
		The	values	for the	worst	case op	eratin	g condition
		are	given b	y the m	aximum	delay m	ultipl	ier.
1000 1100 0	1.01							<u> </u>
UHB-I1RD-E2	Sheet 1/1							Page 20-27

	JJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB								
Cell Name	Function							Number of BC	
	Schmitt Trigger	Input B	uffer					_	
I2R	(TTL Type, True)				D 1			8	
Cell Symbol				agation	Delay td	raramet -	er	<del></del>	
		t0	up KCL	t0	KCL	KCL2	CDR2	Path	
		2.24	0.16	3.72	0.13	RODZ	ODRZ	Path X → IN	
			0.10	01.72	0.110		l		
ļ									
х —	IN IN							1	
							İ		
		Parame	ter			8	ymbol	Typ(ns)*	
						l			
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						1			
	Input Loading					İ			
Pin Name	Factor (lu)					- 1			
1111 Name	Tactor (xu)								
	Output Driving								
Pin Name	Factor (lu)		*	i					
IN	18								
		* Mini	mum val	nes for	the ty	mical o	perat	ing condition.	
		The	values	for the	worst	case of	perati	ng condition	
		are	given b	y the m	aximum	delay	nultip	lier.	
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UHB-I2R-E1	Sheet 1/1							Page 20-28	

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UHI	B" Version
Cell Name	Function						1	Number of BC
	Schmitt Trigger	Input B	uffer					
I2RU	(TTL Type, True)	with P	ull-up	Resista	nce		-	8
Cell Symbol			Prop	agation	Delay	Paramet	er	
		t	up		td			
		t0	KCL	t0	KCL		CDR2	Path X → IN
		2.24	0.16	3.72	0.13			X → IN
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							}	
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х —	√ IN							1
*	<u> </u>						1	
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								1
		Parame	ter		L	7 5	Symbol	Typ(ns)*
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								1
	Input Loading					1		
Pin Name	Factor (lu)					- 1		
I III Hame	Tactor (24)					ŀ		
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						1		
								1
						İ		1
	Output Driving					1		
Din Nama	Factor ((v)							
Pin Name IN	Factor (lu)							
114	10							<u> </u>
		de Mini	mum 17.01	was for	the tw	nical d	norati	ng condition.
		The	walues	for the	worst	Case Of	neratin	g condition
		270	given b	w the m	avimum	delav r	multipl	ier
		are	given b	y the m	aximum	deray i	uur crpr	161.
THE TORK TO	101							Page 20-29
UHB-I2RU-E1	Sheet 1/1							Fage 20-29

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UH	B" Version
Cell Name	Function					,		Number of BC
	Schmitt Trigger	Input B	uffer					
I2RD	(TTL Type, True)	with P	ull-dow	n Resis	tance			8
Cell Symbol				agation	Delay		er	<del></del>
		t0 2.24	WCL 0.16	t0 3.72	td KCL 0.13	KCL2	CDR2	Path X → IN
х —	IN	Parame	tar			l s	ymbol	Typ(ns)*
		rarame	CEI				ушыот	Typ(ns)
Pin Name	Input Loading Factor (lu)							
	Output Driving							
Pin Name	Factor (lu)					1		1
IN	18	The	values	for the	the ty worst	case or	eratin	ng condition. g condition ier.
UHB-I2RD-E1	Sheet 1/1							Page 20-30

FUJITSU (	U CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version									
Cell Name	Function							Number of BC		
			_					_		
01B	Output Buffer(IO	L=3.2mA				D	1	3		
Cell Symbol				agation	Delay td		er			
		t0	up KCL	t0	KCL	n KCL2	CDR2	Path		
		1.93	0.056	2.24	0.124	KCD2	CDR2	OT → X		
		(5.29)	0.030	(9.68)			1	01 4 1		
		(3.2)		(3.00)			1			
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от —	>>- x						1			
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		Parame	ter		·	2	ymbol	Typ(ns)*		
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	Input Loading									
Pin Name	Factor (lu)					- 1				
OT	2	1				1				
	}					1				
						- 1				
	1	1				- 1				
Pin Name	Output Driving					1				
rin Name	Factor (lu)					İ				
	-	<b></b>								
	1	* Mini	mum val	ues for	the tv	mical o	perat	ing condition.		
	The values for the worst case operating condition are given by the maximum delay multiplier.									

Note: 1. The unit of  $K_{\mbox{CL}}$  is ns/pF.

- Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			JHB" Versio	n	
Cell Name	Function							Number of		
O1L	Output Buffer(IO	L=12mA,	Invert	er)				3		
Cell Symbol			Prop	agation	Delay	Paramet	er			
			up		td					
		t0	KCL	t0	KCL	KCL2	CDR 2			
		2.29	0.037	2.47	0.041			OT → X		
		(4.51)		(4.93)						
				l						
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	N			i				İ		
								1		
OT -	√ x					1				
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		Parame	ter	L	L	<del>'                                    </del>	ymbo]	l Typ(ns	*(:	
		Tarame				—— <del>—</del>	J	1,7,5(	,,	
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	Input Loading	1				1		1		
Pin Name	Factor (lu)	1				- 1				
OT	2	1				- 1				
		Ì				1		1		
	1	l				- 1				
		j				1				
		j				1		į		
	Output Driving					Ì		į		
Pin Name	Factor (lu)					1		- 1		
		١								
1		- Mini	mum val	ues for	tne ty	pical c	pera	ting condit	tion.	
1	1	The	values	IOT The	worst	dalam -	1+ /-	ing conditi	LOU	
		1 are	given t	by the m	Jaximum	deray b	uıt1	hiiei.		
Note: 1	The unit of K <sub>CL</sub> is	ns/nF								
1	the district of MCL 10	. 110, pr .								
2. (	Output load capaci	tance c	f 60 pI	is use	d for I	uiitsu'	8			
	logic simulation.									
3. 7	3. The parameters in parentheses are the values applied to the simulation.									
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Page 20-32

UHB-01L-E3 | Sheet 1/1

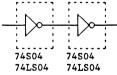
771. 22	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version								
		NIT CEL	L SPECI	FICATION			"UHB" Version		
Cell Name	Function							Number of BC	
	Output Buffer(IO			ter)			Γ		
O1R	with Noise Limit	Resist						5	
Cell Symbol			Prop	agation	Delay P	aramete	r		
		t	up		tdn				
		t0	KCL	t0	KCL	KCL2	CDR2	Path	
		3.30	0.056	5.18	0.13			OT + X	
		(6.66)		(12.98)			l	1	
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		Parameter S							
		rarame	ter	3	mbol	Typ(ns)*			
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D/- N	Input Loading								
Pin Name	Factor (lu)							1	
OT	1								
	1							1	
	1							l .	
	<u> </u>					1			
	Output Driving							1	
Pin Name	Factor (lu)					- 1			
								<u> </u>	
								ng condition.	
								g condition	
		are	given b	y the ma	ximum d	elay mu	ltipl	ier.	
1 1.7 . 4 TT	1	/- T							

Note: 1. The unit of K<sub>CL</sub> is ns/pF.

- Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

FUJITSU	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version									
Cell Name	Function							Number	of BC	
	Output Buffer(IO			er)						
01S	with Noise Limit	Resist						<u> </u>	5	
Cell Symbol				agation			er			
		t0	up KCL	t0	tdn KCL	KCL2	CDF	Pat		
		4.02	0.038	6.39	0.054	KCLZ	+ CDF	OT -		
		(6.30)		(9.63)				"	Λ	
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		Parame	ter		L		ymbo]	Typ	(ns)*	
rarameter Symbol									(113)	
						- 1				
	Input Loading					- 1				
Pin Name	Factor (lu)									
OT	1									
								-		
						- 1		- 1		
								l		
	Output Driving									
Pin Name	Factor (lu)									
			_	_						
		* Mini	mum val	ues for	the typ	ical c	perat	ing cond	dition.	
				for the ma					ition	
			given b	y cire ma	XIII G	cray m	ui ti	71161.		
Note: 1. The unit of K <sub>CL</sub> is ns/pF.										
	utput load capaci	tance o	f 60 pF	'is used	for Fu	jitsu'	s			
1	ogic simulation.									
3. Т	he parameters in	parenth	eses ar	e the va	lues an	nlied	to ti	ne simula	ation.	
	,	<b>,</b>			<b>-</b> F	F				

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version										
Cell Name	Function						Number of BC			
O2B Cell Symbol	Output Buffer (I	OL=3.2mA, True	) tis=	Dolar-	Darama +		2			
Cell Symbol		tup	agation	Delay td		er				
		tO KCL	t0	KCL	KCL2	CDR2	Path			
		1.70 0.056	1.75	0.124			OT → X			
		(5.09)	(9.19)			•				
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	ymbol	Typ(ns)*								
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	Input Loading									
Pin Name	Factor (lu)	]								
OT	4	1								
	Output Driving	1								
Pin Name	Factor (lu)				1					
İ		* Minimum val	ues for	the ty	pical c	perat	ting condition.			
		The values	for the	worst	case or	erati	ing condition			
ļ	1	are given b	y the m	aximum	delay m	ultip	olier.			
TTL Equivalent Circuit										
	0110410									
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74504	74504									



Note: 1. The unit of  $K_{\mbox{\scriptsize CL}}$  is ns/pF.

- 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-02B-E4 | Sheet 1/1

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"บ	HB" Version		
Cell Name	Function							Number of BC		
								_		
02L	Output Buffer(IO	L=12mA,			<b>D</b> 1	D		2		
Cell Symbol				agation	Delay td		er			
		t0	up KCL	t0	KCL	n KCL2	.CDR2	Path		
		2.09	0.037	1.98	0.041	KCL2	.CDR2	OT → X		
		(4.31)		(4.44)			l	01 7 %		
		(4.31)		(4.44)			l			
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	Input Loading									
Pin Name	Factor (lu)									
OT	4					i				
		[				- 1				
		l								
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<b></b>	Output Driving	i								
Pin Name	Factor (lu)	l								
		1								
								ing condition.		
1								ing condition		
		are	given b	y the m	aximum	delay r	nultip	olier.		

Note: 1. The unit of  $K_{\mbox{CL}}$  is ns/pF.

- Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

FULLITSH	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version								
Cell Name	Function	MII ODD	D DI LOI	TIONTION				IN	umber of BC
	Output Buffer(IO	L=3.2mA	. True)					+ -	amber or bo
O2R	with Noise Limit								4
Cell Symbol				agation	Delay P	arame	ter		
		t	up		tdn				
		t0	KCL	t0	KCL	KCL	2 CD	R2	Path
		2.99	0.056	4.69	0.13		- 1		OT → X
		(6.35)		(12.49)			- 1		
							- 1		
							- 1		
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$ $ or $\longrightarrow$ $ $ $ $									
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							- 1		
Parameter Syn						Symbo	1	Typ(ns)*	
						- 1			
						- 1			
	Input Loading								
Pin Name	Factor (lu)					- 1			
OT	2								
						ı			
						- 1			
	Output Driving					- 1			
Pin Name	Factor (lu)								
									l
		<b></b>							4141
									g condition.
				for the ma					condition
	.1	are	PTACH D	y che ma	ALMUM U	cray	<u> </u>	<u>, , , , , , , , , , , , , , , , , , , </u>	
Note: 1. T	he unit of K <sub>CL</sub> is	ns/pF.							
	OL -	•							
2. Output load capacitance of 60 pF is used for Fujitsu's									

- 3. The parameters in parentheses are the values applied to the simulation.

FUJITSU (	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			"ИНВ	" Version
Cell Name	Function								umber of BC
	Output Buffer(IO	L=12mA,	True)						
02S	with Noise Limit	Resist	ance						4
Cell Symbol				agation	Delay	Paran	neter		
		t	up		td				
		t0	KCL	t0	KCL	KCI	.2 C	DR2	Path
		3.71	0.038	5.87	0.054	)	- 1		OT → X
		(5.99)		(9.11)		l			
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OT —	x					l	- 1		
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						1	- 1		
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						<u> </u>			
		Parame	ter				Syn	bol	Typ(ns)*
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		l							
<u></u>	I Imput I andina	ĺ				I			
Din Nama	Input Loading					i			
Pin Name OT	Factor (lu)	l				- 1			
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1									
		l				1			
Į.						ı			
	Output Driving	ł				- 1			
Pin Name	Factor (lu)	Į.				- 1			
1211 1141110	120001 (20)	l				1			
]									
1		* Mini	mum val	ues for	the ty	mical	one	ratin	g condition.
									condition
				y the m					
	<del></del>								i
Note: 1. Th	ne unit of K <sub>CL</sub> is	ns/pF.							
2. Ot	itput load capaci	tance c	of 60 pH	is use	d for F	ujit	su's		
	ogic simulation.		-						
3. Th	ne parameters in	parenth	eses ar	e the v	alues a	pplie	ed to	the	simulation.
1									
1									
1									
1									
1									

Page 20-38

UHB-02S-E3 | Sheet 1/1

FILITON	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version										
Cell Name		MII CEPP	SPECIF	ICALIUN							
Cell Name	Function	T = 2 / = A	T \				<u>N</u>	umber of BC			
0252	Output Buffer(IO							,			
O2S2 Cell Symbol	with Noise Limit	resista		antian Da	1 av D	t	i_	6			
Cell Symbol		4		gation De	tdn	ameter					
		tu t0	KCL	t0	KCL	KCL2	CDR2	Path			
		5.27	0.032	9.51	0.06	KULZ	CDRZ	OT → X			
		(7.19)		(13.11)	0.00			01 <del>-</del> X			
		(7.13)		(13.11)							
ОТ —	>— x										
		Paramet	er			Sym	bol	Typ(ns)*			
						i					
						ļ					
						1					
						1					
						1					
	T +					1					
D. 11.	Input Loading					1					
Pin Name	Factor (lu)										
OT	2					1					
						1					
						1					
						1					
	Output Driving					1					
Pin Name	Factor (lu)					1					
IIII Name	Factor (Eu)					1					
								L			
		* Minim	11m va111	es for th	e tonic	al one	retin	e condition			
		* Minimum values for the typical operating condition.  The values for the worst case operating condition									
				the maxi							
	I			- III WIGHT		-, -, -, -, -, -, -, -, -, -, -, -, -, -		<u> </u>			

Note: 1. The unit of  $K_{\mbox{CL}}$  is ns/pF.

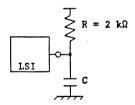
- Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

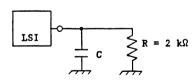
UHB-02S2-E3 | Sheet 1/1

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version Cell Name Number of BC Function Tri-state Output Buffer(IOL=3.2mA, True) 04R with Noise Limit Resistance 5 Cell Symbol Propagation Delay Parameter tup tdn KCL t0 KCL KCL2 | CDR2 t0 Path 3.12 5.66 OT + X 0.056 0.13 (6.76)(14.11)X  $L \rightarrow Z$  $Z \rightarrow L$ KCL t0 KCL t0  $C \rightarrow X$ 6.47 0.13 2.22 (13.44)(14.92)Input Loading Pin Name Factor (lu) OT C 2 H → Z Z → H t0 KCL t0 KCL 3.07 3.20 0.056 Output Driving (13.44)(14.92)Pin Name Factor (lu)

\* These values are subject to external loading condition.

Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:





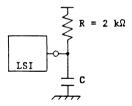
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

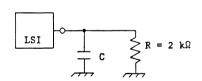
Note: 1. The unit of KCL is ns/pF.

- Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-04R-E3 | Sheet 1/1

FULLITSU	CMOS GATE ARRAY U	NIT CEL	T. SPECT	FICATION	V		l "UH	B" Version
Cell Name	Function	ODD	D DI DO	1110/1110	`			Number of BC
	Tri-state Output	Buffer	(IOL=12	mA. True	е)			
048	with Noise Limit			,	-,			5
Cell Symbol				pagation	Delay Pa	aramete	r	
		t	up	I	tdn			1
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		3.96	0.038	7.25	0.054			OT → X
		(6.43)		(10.76)	ol l			1
					1			
				1				
	^			1				1
								1
ОТ	x			1				
	V				1 1		1	
					ļ		1	1
	,			1			l	
	С			1	1		1	Ì
			L + 2	,		$Z \rightarrow L$	<u> </u>	
		t0	<del></del>	KCL	t0		CL	d c → x
i		3.6	5	VCF	7.40		054	-
		(17.8		*	(10.91		034	
		(17.0	,		(10.31	′		
			- 1					
	Input Loading		İ					
Pin Name	Factor (lu)		1			- 1		
OT	2					1		1
С	2		H → 2	Z		$Z \rightarrow H$		7
		t0		KCL	t0	K	CL	7
		3.7	5		3.69	0.	038	
	Output Driving	(17.8	3)	*	(10.91	)		
Pin Name	Factor (lu)					1		
			1			j		
						1		
			[			- 1		





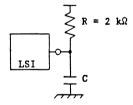
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

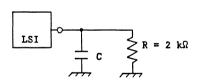
Note: 1. The unit of KCL is ns/pF.

- Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-04S-E3 | Sheet 1/1

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	1		<b>"</b> UH	" Version
Cell Name	Function							Number of B
	Tri-state Output	Buffer	(IOL=24	mA, True	e)			
0482	with Noise Limit	Resist						7
Cell Symbol			Prop	agation	Delay P	aramete	r	
		tup tdn						
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		5.61	0.032	11.62	0.06			OT + X
		(7.69)		(15.52)			1	1
							1	1
	^			1			İ	
от —	x			Į.			1	İ
	M			1			1	1
							1	1
	,			1			ì	1
	С			l				1
				<u> </u>			<u> </u>	
			L + 2			$Z \rightarrow L$		<b>.</b>
		t0		KCL	t0		KCL	C → X
		5.3			11.18		.06	
		(19.2	3)	*	(15.08	)		
			- 1			1		
	1	1	- 1	1				
D: 11	Input Loading		- 1	1				
Pin Name	Factor (lu)					- 1		
OT	2							4
С	2		H → 2			Z → H	701	4
	1	t0 6.3	<del>,  </del>	KCL	t0		KCL	-
	Out-ut Defeates			*	5.25		.032	
Pin Name	Output Driving Factor (lu)	(19.2	ا (د	_	(15.08	7		
rin Name	ractor (tu)	1	1	1		l		
						- 1		
	1	1	1	1		- 1		ı
	l .	)	l l	1		ı		1





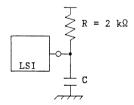
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

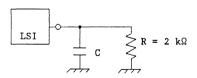
Note: 1. The unit of KCL is ns/pF.

- Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-04S2-E3 | Sheet 1/1

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version											
Cell Name	Function								umber of BO	,	
04T	Tri-state Output	Buffer							4		
Cell Symbol				agation		aramete	r				
		t0	up KCL	t0	tdn   KCL	KCL2	CDR	2	Path		
		2.42 (6.06)	0.056	2.52 (10.97)	0.13				OT → X		
от ——	x c										
			$L \rightarrow Z$			Z + L	L	7			
		t0		KCL	t0		CL		$C \rightarrow X$		
		2.0 (12.3		*	2.55 (11.00	1	13	İ			
	Input Loading										
Pin Name	Factor (lu)			1				- 1			
OT C	4 2		H → Z	,		$Z \rightarrow H$		_			
\		t0	-11 / 2	KCL	t0		CL	-			
		3.4	1		2.31		056	_			
Pin Name	Output Driving Factor (lu)	(12.3	5)	*	(11.00)						
	<u> </u>							1			





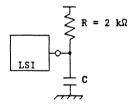
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

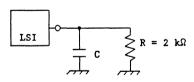
Note: 1. The unit of  $K_{\mbox{\scriptsize CL}}$  is ns/pF.

- 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the  $\operatorname{simulation}$ .

UHB-04T-E5 | Sheet 1/1

FUJITSU (	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N			HB" Version
Cell Name	Function							Number of BC
04W	Tri-state Output	Buffer	(IOL=12	mA, Tru	e)			4
Cell Symbol			Prop	agation			er	
			up		td			
		t0	KCL	t0	KCL	KCL2	CDR2	
		3.02 (5.49)	0.038	4.12 (7.17)	0.047			OT → X
от —	c x							
			L + 2			Z + I		
		t0		KCL	t0		KCL	c → x
		2.9 (16.3		*	3.6 (6.7		0.047	
Pin Name OT	Input Loading Factor (lu)							
С	2		H → 2	Z		$Z \rightarrow I$	ĭ	
		t0		KCL	t0		KCL	
Pin Name	Output Driving Factor (lu)	4.0 (16.3	1	*	2.72 (6.75		0.038	





- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of KCL is ns/pF.

- Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- The parameters in parentheses are the values applied to the simulation.

UHB-04W-E3 | Sheet 1/1

FIIITSII (	CMOS GATE ARRAY U	NIT CEL	T SDECT	FICATIO	N1		771	HB" Version
Cell Name	Function	NII CLL	D SEECI.	FIUMITO	14			Number of BC
0011	T direction.		***************************************	<del></del>				Number of 25
O1BF	Output Buffer (I	OL=8mA,						3
Cell Symbol				agation	Delay		er	
			up	1	td		Tanna	
		1.96	KCL 0.056	t0 2.01	KCL 0.063	KCL2	CDR2	Path OT → X
		(5.32)		(5.79)		ĺ	1	01 7
		(3.32)		(3)		ĺ	1	
			!			İ		
			!			ĺ		
			!		1		1	
ļ	$\sim$	'	1 !					
от —	>─ x		!					
		1	1 1	1			ļ	
		1 1				į	İ	
		1 1	'					
		Parame	ter	<u> </u>	L	L 5	Symbol	Typ(ns)*
		1010			<del></del>		//	-35(5)
		l						
		l						
		1						
		l						
	Input Loading	l				- 1		
Pin Name	Factor (lu)	l				-		
OT	2	l				l		
		l						
		1				l		
		l						
	Output Driving	1				į		
Pin Name	Factor (lu)	l						
		L						
								_
								ing condition.
			values given b					ing condition
<b></b>	J	are	given b	y the a	RYTHUM	deray .	DUILIP	niei.
Note: 1. T	he unit of K <sub>CL</sub> is	ns/pF.						
· ·								
	utput load capaci	tance o	f 60 pF	'is use	d for F	'ujitsu'	8	
logic simulation.								
3. T	he parameters in	parenth	eses ar	e the v	alues a	pplied	to th	ne simulation.

UHB-01BF-E1 | Sheet 1/1

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Vers  Cell Name Function Number  Output Buffer (IOL=8mA, Inverter) with Noise Limit Resistance 5	ion of BC
Output Buffer (IOL=8mA, Inverter) O1RF with Noise Limit Resistance 5	of BC
O1RF   with Noise Limit Resistance 5	
UIKF   with Noise Limit Resistance 5	
Cell Symbol Propagation Delay Parameter	
tup         tdn           t0         KCL         t0         KCL         KCL2         CDR2         Pat	
$ \begin{array}{c ccccc} t0 & KCL & t0 & KCL & KCL2 & CDR2 & Pat \\ \hline 3.39 & 0.056 & 5.60 & 0.063 & & OT \rightarrow \end{array} $	
(6.75) $(9.38)$	^
(6.73)	
Parameter Symbol Typ(	ns)*
i i i i	
Input Loading	
Pin Name Factor (lu) OT 1	
OT 1 1	
Output Driving	
Pin Name Factor (lu)	
TIN Name   Factor (Au)	
* Minimum values for the typical operating cond	ition
The values for the worst case operating condi	
are given by the maximum delay multiplier.	

Note: 1. The unit of K<sub>CL</sub> is ns/pF.

- Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

FUJITSU C	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version										
Cell Name	Function							Number of BC			
O2BF	Output Buffer (I	OL=8mA.	True)					2			
Cell Symbol	output puller (1		Prop	agation	Delay	Paramet	er				
			up		td	n					
		t0	KCL	t0	KCL	KCL2	CDR2	Path			
		1.76	0.056	1.52	0.063		l	OT → X			
		(5.12)		(5.30)			l	1 1			
							l				
							l				
١.							Į				
							İ				
OT —	x						1				
1							1	1			
Ì											
1							1				
		Parame	ter			S	ymbol	Typ(ns)*			
1											
1											
	Input Loading										
Pin Name	Factor (lu)					į					
TO	4	ĺ				1					
		l				- 1		1			
	Output Driving										
Pin Name	Factor (lu)										
		* Mini	mum wa1	nes for	the to	mical c	nerat	ing condition.			
İ		The	values	for the	worst	case or	erati	ng condition			
		are	given b	y the m	aximum	delay n	ultip	lier.			
TTL Equival	ent Circuit							1			
i											
								ļ			
1 -1/2-											
1	: :										
74504	74S04 74LS04										
74LS04	741504										
Note: 1. Th	ne unit of K <sub>CL</sub> is	ns/pF.									
	tput load capaci	tance o	of 60 pF	is use	d for F	ujitsu'	S				
10	ogic simulation.										
3. Th	ne parameters in	parenth	eses ar	e the v	alues a	pplied	to th	e simulation.			
	*	•				.,	<b></b>				
IND-OOR PS	Choo+ 1/1							Page 20-89			
UHB-02BF-E1	Sheet 1/1							Fage 20-09			

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION					B" Version
Cell Name	Function								Number of BC
·	Output Buffer (I							1	
O2RF	with Noise Limit	Resist							4
Cell Symbol			Prop	agation	Delay P	arar	nete	r	
			up		tdn				_
	*	t0	KCL	t0	KCL	K(	CL2	CDR2	
		3.08	0.056	5.11	0.063				OT → X
		(6.44)		(8.89)					
						1			
						l			
						l			
						ł			ļ
					į.	1			
OT	x				]				ļ
						1		į	
			<u> </u>		L	Ц,		ــِـــ	
		Parame	ter				ьу	mbol	Typ(ns)*
		1				- 1			
		ĺ				- 1			1
						- 1			
		i				- 1			i
						ı			
	Tanua Tandi					- 1			
Pin Name	Input Loading Factor (lu)								
OT OT	Pactor (ku)					l			
01	1 2	1							į
		<b> </b>				ı			
									l
						l			
	Output Driving	1							1
Pin Name									
FIII Name	Factor (lu)	1							1
		<del> </del>							
		* Mini	mum 37.01	ues for	the twr	dea	1 00	areti	ng condition
	İ								g condition
				y the ma					
		I are	PTACH D	J the ma	VINOR C	CIA	,		101.

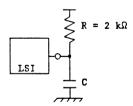
Note: 1. The unit of  $K_{\rm CL}$  is ns/pF.

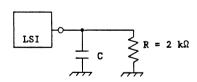
- 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

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UHB-02RF-E1 | Sheet 1/1

	CMOS GATE ARRAY U	NIT CELL S	PECI	FICATION	4			B" Version
Cell Name	Function						1	Number of BC
	Tri-state Output			mA, True	e)			
O4RF	with Noise Limit	Resistan	:e					5
Cell Symbol			Prop	agation	Delay P	aramete	r	
		tup			tdn			
		t0 1	CL	t0	KCL	KCL2	CDR2	Path
			056	5.96	0.070			OT + X
		(6.85)		(10.51)			İ	
					1			
					1			
								1
от —	x	1			1			
	M	l 1						
		1		ļ			1	1
	•	1			1		1	
	С							i
				<u>L</u>	1		<u> </u>	
			. → Z			$Z \rightarrow L$		4
		t0		KCL	t0		CL	] c → x
		2.62	1		6.82		070	1
		(15.89)	- }	*	(11.37	)		
			-			- 1		
			-			- 1		1
	Input Loading		1			-		1
Pin Name	Factor (lu)		1			- 1		
OT	2							
С	2		1 → Z			Z → H		
		t0		KCL	t0		CL	4
	1	3.30		*	3.21		056	
<b>D</b>	Output Driving	(15.89)		*	(11.37)			
Pin Name	Factor (lu)							
	_l		l					





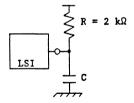
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

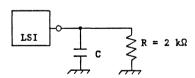
Note: 1. The unit of  $K_{\rm CL}$  is ns/pF.

- Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-04RF-E1 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CELI	SPECI	FICATIO	N N		"UH	IB" Version
Cell Name	Function	0000	J DI DOI	1 10///10				Number of BC
04TF	Tri-state Output	Buffer	(IOL=8	mA, Tru	e)			4
Cell Symbol					Delay Pa	aramete	r	7. <del>- 7</del>
		tı	qı		tdn			
İ		t0	KCL	t0	KCL	KCL2	CDR2	
ļ		2.51	0.056	3.27				OT → X
		(6.15)		(7.37	기			
				1				
				l				1
	$\setminus$			1	1			1
от —	>— x			1	1 1		1	
				1			1	
		1						
	_	]						
	С	1		l	1 1			
			L + 2	<u> </u>		Z + L	L	
		t0		KCL	t0		CL	$ c \rightarrow x$
		2.29			3.35		063	٦
		(14.80	0)	*	(7.45)	)		
			1					
1	Input Loading							
Pin Name OT	Factor (lu)					1		
1 °C	2		H → 2	,		$Z \rightarrow H$		-
1	1	t0		KCL	t0		CL	-
	1	3.12			2.37		056	
	Output Driving	(14.80		*	(7.45			1
Pin Name	Factor (lu)					- 1		
			- 1					
	1							
			1			1		
1	1	l						

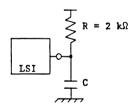


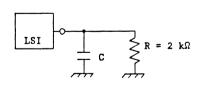


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  is ns/pF.
  - Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-04TF-E1 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	1		וט" ד	B" Version	
Cell Name	Function							Number of BC	
Н6Т	Tri-state Output	(IOL=3.						8	
Cell Symbol			Prop	agation			r		
1			up		tdn				
		t0	KCL	t0	KCL	KCL2	CDR		
		1.06	0.04	1.84	0.04		l	X → IN	
		(7.18)		(13.57)			l	OT → X	
	1	(7.10)		(13.37)	Ί Ι				
IN —	<b>─</b> < h								
1	N 1								
от —	<b>X</b>							1	
	LP .								
]								1	
	1			1					
	С			1					
			L	<u></u>	<u> </u>		<u> </u>		
		<u> </u>	L → Z			$Z \rightarrow L$	OT		
		t0 2.0	<del>,  </del>	KCL	±0 2.55		CL 13	C → X	
		(15.3		*	(13.60		13		
İ		(15.5	3)	.	(13.00	'			
				l		ı			
<b></b>	Input Loading	1				1		1	
Pin Name	Factor (lu)							1	
OT	4								
С	2		H → 2			Z → H			
		t0		KCL	t0		CL	_	
	<del> </del>	3.4	_		2.31		056	1	
Die Name	Output Driving	(15.3	3)	*	(13.60	)		1	
Pin Name IN	Factor (lu)	ł	1	İ		1			
114	30	1							
ļ	1	1	-					1	
		1				- 1			
	_								

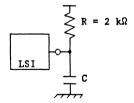


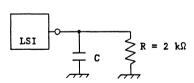


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H6T-E4 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPEC	IFICATION	N .		T"UHI	B" Version
	Function				·			Number of BC
	Tri-state Output	(IOL=3.	2mA) δ	Input B	uffer (T	rue)		
H6TU	with Pull-up Res					,		8
Cell Symbol				pagation	Delay P	aramet	er L	
		t	up	1	tdn			T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.06	0.04	1.84				X → IN
		2.42	0.056	2.52	0.13		i	OT + X
		(7.18)		(13.57)			1	1
		, ,		1	1		1	1
IN ——			İ	1				1
Í							1	1
от —	> <del></del>							
	P		1	1	1		1	1
•			1	ł			1	1
	l							
	C					1	1	
				1			İ	1
			L →			$Z \rightarrow L$		
		t0		KCL	t0		KCL	] c → x
		2.0			2.55	_	.13	
		(15.3	5)	*	(13.60	)		i
			- 1					1
			- 1			ļ		1
	Input Loading		- 1					
Pin Name	Factor (lu)	1	- 1					
OT	4							_
С	2		Н →			$Z \rightarrow H$		_
		t0		KCL	t0		KCL	1
	ļ	3.4	-	_	2.31		.056	1
	Output Driving	(15.3	5)	*	(13.60	)		
Pin Name	Factor (lu)	1	1			ł		1
IN	36	l	1					
	1		1			- 1		
		1	- 1			- [		1
	1	1						1

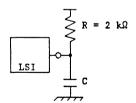


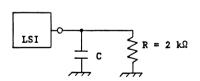


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H6TU-E4 | Sheet 1/1

	CMOS GATE ARRAY U	"Ul	B" Version							
Cell Name	Function							Number of BC		
	Tri-state Output			Input Bu	ıffer (T	rue)				
H6TD	with Pull-down R	esistan						8		
Cell Symbol				agation	Delay P		r			
			up		tdn					
		t0	KCL	t0	KCL	KCL2	CDR2			
		1.06	0.04	1.84	0.04		ĺ	X → IN		
		2.42	0.056	2.52	1 1		1	OT → X		
	1	(7.18)		(13.57)	)		1	Ì		
IN —	<b>-</b> < h				1		l	į		
	7	[ ]					İ			
от —	x	1 1					İ	1		
01	^									
								1		
		1					l	1		
	С									
	•							1		
		<u> </u>	L + 2	:		$Z \rightarrow L$	L	<del>- </del>		
		t0		KCL	t0	K	CL	¬ c → x		
		2.0	7		2.55	0.	13	7		
		(15.3	5)	*	(13.60	)		1		
			1			j		1		
				ļ		- 1				
	Input Loading	1	1	1		- 1				
Pin Name	Factor (lu)	1				ı		1		
OT	4							4		
С	2		H → Z			Z + H		4		
		t0		KCL	t0		CL			
	1 Date of Date of	3.4		*	2.31		056	1		
Din Nama	Output Driving	(15.3	ا (د	*	(13.60	, l				
Pin Name IN	Factor (lu)	1		-						
114	30	]				1		1		
		l	- 1	1		- 1				





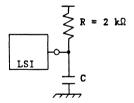
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

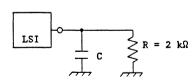
Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-H6TD-E4 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	HB" Version						
	Function							Number of BC
H6W	Tri-state Output	(IOL=12r						8
Cell Symbol				agation			er	
			KCL	t0	KCL KCL	n KCL2	CDR2	<b>-</b>   -,
		t0 1.06	0.04	1.84	0.04	KULZ	CDRZ	Path X → IN
		3.02	0.038	4.12	0.047		l	OT + X
		(6.25)	0.030	(8.12)			1	0
IN	$\prec \uparrow$	(0.23)		(0.11)			ł	
**	$\backslash$						ł	
от —	<b>x</b>						}	
01	^ ^							ĺ
	1			1			ł	-
	С	İ						
		I	L + 2			$Z \rightarrow I$	<u> </u>	
		t0		KCL	t0		KCL	⊢ c → x
		2.90	6		3.6		0.047	
		(20.2	5)	*	(7.6	9)		
			l			l		
<b></b>	Input Loading		- 1		1			
Pin Name	Factor (lu)		-					1
OT	4		l		l	ı		
С	2		H → 2			Z + 1		
		t0		KCL	t0		KCL	
		4.0	. ,		2.7		0.038	
Pin Name	Output Driving	(20.2	5)	*	(7.6	9)		
Pin Name IN	Factor (lu)		1					1
111	50	[			1			1
						l		
1		1	1			- 1		





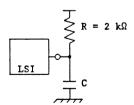
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

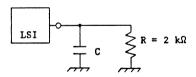
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- The parameters in parentheses are the values applied to the simulation.

UHB-H6W-E3 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		<b>"</b> U	HB" Version	
Cell Name	Function							Number of BC	
	Tri-state Output			nput Bu	ffer (T	rue)			
H6WU	with Pull-up Res	istance						8	
Cell Symbol			Prop	agation			er		
			up		td				
		t0	KCL	t0	KCL	KCL2	CDR2		
		1.06	0.04 0.038	1.84	0.04		1	$X \rightarrow IN$ OT $\rightarrow X$	
		3.02 (6.25)		4.12				01 7 X	
	1	(0.23)		(8.12)					
IN —	<b>─</b> < h			1					
	N 3						Ì	1	
от —	→ x						l	1	
1									
<u> </u>	l								
	С	}							
			$L \rightarrow Z$			$Z \rightarrow I$			
i		t0		KCL	t0		KCL	c → x	
		2.9		*	3.6		.047		
		(20.2	5)	*	(7.6	19)			
	Input Loading	1	j						
Pin Name	Factor (lu)		l						
OT	4	1	1		ĺ				
C	2		H → Z		<b> </b>	$Z \rightarrow 1$	ı .		
_	_	t0		KCL	t0		KCL		
1		4.0			2.7	2 0	0.038		
	Output Driving	(20.2	5)	*	(7.6	9)		1	
Pin Name	Factor (lu)	]			l	l		1	
IN	36				1	I			
		1							
					1	ŀ			
		L			L				

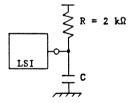


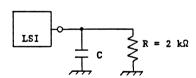


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the  ${\tt simulation.}$

UHB-H6WU-E3 | Sheet 1/1

FULLTSU (	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UH											
	Function	IVII ODD	D DI DO.	11 1011110	••			HB" Version Number of BC				
	Tri-state Output	(IOL=12	mA) & :	Input Bu	ffer (T	rue)						
H6WD	with Pull-down R	esistan			-	<u> </u>		8				
Cell Symbol			Pro	pagation	Delay	Paramet	er					
			up		td							
		t0	KCL	t0	KCL	KCL2	CDR2					
		1.06	0.04	1.84	0.04	ł	ł	X → IN				
		3.02	0.038	4.12	0.047			OT → X				
	/	(6.25)		(8.12)			ł	1				
IN -	<b>─</b> < h						1					
1	\											
ОТ —	> x						Í					
	<b>√</b>						l	1				
							į					
	1							1				
1	C						1					
							<u> </u>					
			L + S			$Z \rightarrow I$						
		t0		KCL	10 3.6		KCL	C → X				
		2.9 (20.2		*	(7.6		0.047					
ļ		(20.2	"	•	(/.6	اروا						
Ì			1			1						
	Input Loading		l			- 1						
Pin Name	Factor (lu)											
OT	4		l			- 1		1				
С	2		H → :	Z		$Z \rightarrow 1$	ł					
		t0		KCL	t0		KCL					
<u> </u>		4.0	-		2.7	- 1 -	0.038					
	Output Driving	(20.2	5)	*	(7.6	9)		1				
Pin Name	Factor (lu)											
IN	36				1	1						
					l							
						1						
1	i ·	1	1		1			1				





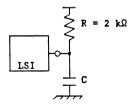
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

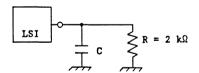
Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- The parameters in parentheses are the values applied to the simulation.

UHB-H6WD-E3 | Sheet 1/1

FUJITSU (	MOS GATE ARRAY U	NIT CELL	SPECI	FICATIO	N .		T "UI	HB" Version			
	Function							Number of BC			
	Tri-state Output	(IOL=3.2	mA)								
H6C	& CMOS Interface			(True)				8			
Cell Symbol		***********	Prop	agation	Delay P	aramete	r				
		tu			tdn						
Ì		t0	KCL	t0	KCL	KCL2	CDR				
		0.92	0.04	1.33				X → IN			
		2.42	0.056	2.52	0.13		l	OT → X			
	1	(7.18)		(13.57	)		1				
IN —	-<- h										
	<u>,                                    </u>						l				
	\ \ \					l					
OT -	x	}					1	1			
1	1	l i									
							ł				
	C										
	U	l l		l			l				
			L + Z	l		$Z \rightarrow L$	L				
<u>{</u>		t0		KCL	t0		CL	⊢ c → x			
1		2.07			2.55		.13	- "			
		(15.35		*	(13.60						
		(	<b>´</b>			1					
1											
	Input Loading										
Pin Name	Factor (lu)										
TO	4										
C	2		H → Z			Z → H					
							CL				
		3.41			2.31		056				
1	Output Driving	(15.35	5)	*	(13.60	)					
Pin Name	Factor (lu)										
IN	36		1			1					
			1								
			1								
l	1		- 1			ı					

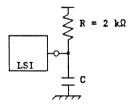


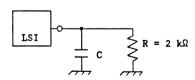


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H6C-E4 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPEC	FICATIO	N		T "UH	B" Version
Cell Name	Function				·			Number of BC
	Tri-state Output	(IOL=3.	2mA) &	CMOS In	terface			
H6CU	Input Buffer (Tr	ue) wit	h Pull-	up Resi	stance		1	8
Cell Symbol	\		Pro	pagation	Delay P	aramete	r	
		t	up	T	tdn			
		t0	KCL	t0	KCL	KCL2   CDR2		Path
		0.92	0.04	1.33	0.04		·	X + IN
		2.42	0.056	2.52	0.13		l	OT → X
	_	(7.18)		(13.57	)		1	
IN —	_/_	` ′		`	1		1	
IN				l			l	
							l	
от —	→ x			1				
	M						l	ŧ
							l	ļ
	1							
	С	1		ł	1			
					$Z \rightarrow L$			
		t0		KCL	t0		CL	C → X
		2.0		-	2.55		.13	į.
		(15.3	5)	*	(13.60	)		1
		1						ì
	<b>,</b>	l	1					
<b>.</b>	Input Loading		ł			1		1
Pin Name	Factor (lu)							
OT	4							4
С	2		H → Z			Z → H		4
	1	t0		KCL	t0		CL	4
	1	3.4		*	2.31		056	į
D/- N	Output Driving	(15.3	ارد	#	(13.60	)		
Pin Name IN	Factor (lu)		ı			ı		
IN	36		l	į		1		
	1		1			l		
	<u> </u>	<u> </u>						1





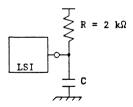
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

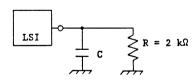
Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-H6CU-E4 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CELI	SPECI	FICATIO	N N		<b>"</b> UH	B" Version
Cell Name	Function				··		T	Number of BC
	Tri-state Output	(IOL=3.2	2mA) &	CMOS In	terface			
H6CD	Input Buffer (Tr						- 1	8
Cell Symbol					Delay P		r	
		tı	up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	
		0.92	0.04	1.33				X → IN
		2.42	0.056	2.52				OT → X
	_	(7.18)		(13.57	)			
IN —	<b>─</b>						İ	ļ
2.11	_ 기	İ		l				
				1				j
ОТ	x +			İ			l	
	V							1
				İ				1
	_			l			Ì	
	С			i			İ	
				<u> </u>		<u> </u>	l	
			L + 2			$Z \rightarrow L$	OT.	
		10 2.0		KCL	10 2.55		CL .13	_ c → x
				*	(13.60		.13	
		(15.3	۱ (۹	*	(13.60	'		
			- 1					1
	Input Loading		- 1					
Pin Name	Factor (lu)		- 1					
OT OT	ractor (ku)		- 1					1
C	2		H → 2			$Z \rightarrow H$		-
	1	t0		KCL	t0		CL	⊣
		3.4		VOT	2.31		056	
	Output Driving	(15.3	-	*	(13.60		050	
Pin Name	Factor (lu)	(15.5.	,		(13.00	<b>'</b>		1
IN	36	1	- 1					
<b>-</b> .,			- 1					1
ĺ			- 1					1
								1

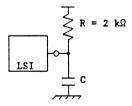


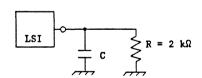


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H6CD-E4 | Sheet 1/1

	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "U										
Cell Name	Function							Number of BC			
	Tri-state Output	(IOL=12	mA) & (	CMOS Int	erface						
H6E	Input Buffer (Tr	ue)						8			
Cell Symbol			Pro	pagation	Delay	Paramet	er				
		t	up		td						
,**		t0	KCL	t0	KCL	KCL2	CDR2	Path			
		0.92	0.04	1.33	0.04		l	X → IN			
		3.02	0.038		0.047		ĺ	OT → X			
	_			(8.12)			1	Į			
IN	<b></b>	·					l				
211	$\sqrt{N}$	1					l				
	x						1				
OT	·					1	İ				
	•					ł	į				
	l					1	Į				
	1			1			1	1			
	С	}	l				1	1			
			L <u>.</u>			L					
		<u> </u>	L +			$Z \rightarrow I$		٠. ي			
		t0	_	KCL	t0 3.6		KCL 0.047	_ c → x			
		2.9		*			0.047				
		(20.2	ا (د	*	(7.6	9)					
		l	1			- 1		ŀ			
	Input Loading	l	- 1		1	1		1			
Pin Name	Factor (lu)	1	ı					1			
OT OT	Factor (£u)	ł	1			l					
C	2		H →	7	<u> </u>	Z + 1		-1			
C	1	t0	_ n =	KCL	to		KCL	-			
		4.0	3	YOU	2.7		0.038	-			
	Output Driving	(20.2		*	(7.6						
Pin Name	Factor (lu)	`	- /		l (,,,	7		1			
IN	36	i			1			1			
			1		1			1			
		1			l	1					





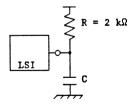
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

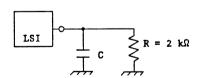
Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-H6E-E3 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"U	HB" Version
Cell Name	Function				·			Number of BC
	Tri-state Output	(IOL=12	mA) & C	MOS Int	erface			
H6EU	Input Buffer (Tr	ue) wit						8
Cell Symbol			Prop	pagation			er	
ŀ			up		td			
1		t0	KCL	t0	KCL	KCL2	CDR2	
		0.92 3.02	0.04	1.33	0.04		İ	X → IN OT → X
		(6.25)		4.12 (8.12)			1	01 + X
	1	(6.23)		(0.12)				
IN —	<b>─</b> < h						1	
	\			1				
от —	> x						l	
	· ·							ı
						1	l	
	1				1			
	C			1	'	1	l	1
				<u> </u>			<u> </u>	
j			L → 2			$Z \rightarrow I$		
		t0		KCL	t0		KCL	c → x
l		2.9			3.6		.047	
		(20.2	5)	*	(7.6	9)		
		l	- 1		1	1		
	Tana Tandini		- 1		l	l		
Pin Name	Input Loading Factor (lu)	1				l		
OT OT	ractor (£u)	1	ł		İ			
C	2	<del> </del>	H → 2	7.		$Z \rightarrow 1$	<del>1</del>	-
	1	t0	<del>-                                    </del>	KCL	to		KCL	_
1		4.0	3	<b></b>	2.7		0.038	
	Output Driving	(20.2		*	(7.6			
Pin Name	Factor (lu)		1		1	l		
IN	36	1						Į
						1		
Ì								
		L						

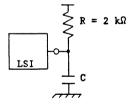


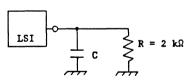


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H6EU-E3 | Sheet 1/1

Cell Name	Function							Number of BC
	Tri-state Output	(IOL=12m	A) & C	MOS Int	erface			
H6ED	Input Buffer (Tr	ue) with	Pull-	down Re	sistanc	е		8
Cell Symbol			Prop	agation	Delay	Paramet	er	
		tu			td			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
			0.04	1.33	0.04			X + IN
			0.038	4.12	0.047		1	OT → X
	4	(6.25)		(8.12)				
IN —	-	1					]	
111	$\sqrt{}$			l			1	1
				1			l	1
от —	x -						1	1
	M	1					1	
		1		ł			1	
	_							
	С	1		1	'		Ì	1
			L + Z			$Z \rightarrow I$		
	i	t0 2.96		KCL	10 3.6		KCL 0.047	- $c + x$
		1		*	_		7.047	i i
		(20.25	'	•	(7.6	9)		1
			l			1		1
<del></del>	Input Loading		- 1			- 1		1
Pin Name	Factor (lu)		l		1	- 1		
OT	ractor (£u)							1
C	2		H → Z	,	<b></b>	$Z \rightarrow I$	1	
U	-	t0		KCL	tO		KCL	-
		4.03			2.7		0.038	-
	Output Driving	(20.25		*	(7.6			
Pin Name	Factor (lu)	\-	1		l ```	'		
IN	36	1	1		1	l		1
		1	l		ĺ			
		1	1			l		1
		1						1

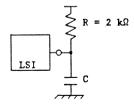


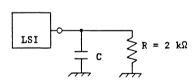


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H6ED-E3 | Sheet 1/1

FUJITSU (	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"ин	B" Version
Cell Name	Function							Number of BC
	Tri-state Output	(IOL=3.	2mA) &					
H6S	Schmitt Trigger	Input B	uffer(C	MOS Typ	e, True)		- 1	12
Cell Symbol	<del></del>	T			Delay P	aramete	r	
		t	up	1	tdn			T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2,48	0.16	3.08				X → IN
		2.42	0.056	2.52	0.13		l	OT → X
		(7.18)		(13.57				
	$\mathcal{F}$	( , , , , ,		(	1 1		1	
IN —				1	i i		1	
	7							
от —	> x						1	
• •	√ ".			1	1		l	
•								
	С			l				
	C			1	1			ļ
			L + 2	,		$Z \rightarrow L$	Ь	
		t0	<del></del>	KCL	t0		CL	$d c \rightarrow x$
		2.0	<del>,</del>	KCD	2.55		0.13	-
				*	(13.60	1	7.13	
		(15.3	ا (د	*	(13.60	'		
		1	- 1			1		
	1		- 1			- 1		
Dia Nama	Input Loading	l	į			- 1		
Pin Name	Factor (lu)		1			İ		j
OT	4							_
С	2		H → 2			Z → H		
		t0	_	KCL	t0		CL	
	ļ	3.4	- 1		2.31		056	
	Output Driving	(15.3	5)	*	(13.60	)		
Pin Name	Factor (lu)	Į				ļ		
IN	18	1						
		l	l					
		l	- 1					1





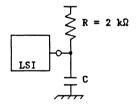
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

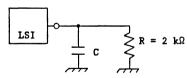
UHB-H6S-E2 | Sheet 1/1

"UHB" Version FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION Cell Name Function Number of BC Tri-state Output(IOL=3.2mA) & Schmitt Trigger H6SU Input Buffer (CMOS Type, True) with Resistance 12 Cell Symbol Propagation Delay Parameter tup tdn KCL t0 KCL KCL2 | CDR2 Path 2.48 0.16 3.08 0.10 X + IN OT → X 2.42 0.056 2.52 0.13 (7.18)(13.57)IN X  $L \rightarrow Z$ t0 KCL t0 KCL  $C \rightarrow X$ 2.07 2.55 0.13 (15.35)(13.60)Input Loading Factor (lu) Pin Name OT С 2 H → Z  $Z \rightarrow H$ t0 KCL t0 KCL 3.41 2.31 0.056 Output Driving (15.35)(13.60)Pin Name Factor (lu) IN 18

\* These values are subject to external loading condition.

Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:

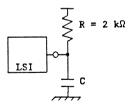


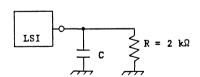


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H6SU-E2 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	SPECI	FICATION	ı .		T"U	HB" Version		
Cell Name	Function						Ť	Number of BC		
	Tri-state Output	(IOL=3.	2mA) &	Schmitt	Trigger					
H6SD	Input Buffer(CMO	S Type,						12		
Cell Symbol			Prop	agation			r			
			up		tdn					
į		t0	KCL	t0	KCL	KCL2	CDR			
		2.48	0.16	3.08	0.10			$X \rightarrow IN$ OT $\rightarrow X$		
		2.42 (7.18)	0.056	2.52			1	01 <del>7</del> X		
	<u></u>	(7.10)		(13.37)	1		İ	1		
IN —	<b>─</b> <~\/ h						1			
	N 1			i						
от —	→ x						1			
1	LP									
İ										
}	i									
i	С									
1			$\begin{array}{c ccccccccccccccccccccccccccccccccccc$							
		t0	$L \rightarrow 2$	KCL	t0		CL	$ c \rightarrow x$		
		2.0	<del>,  -</del>	VCT	2.55		1.13	⊢ ' ' ^		
i		(15.3		*	(13.60		,.13			
		(13.3	"		(13.00	<b>'</b>				
			- 1							
	Input Loading	1	- 1							
Pin Name	Factor (lu)	}						1		
OT	4	<u> </u>								
С	2		Η → 2			$Z \rightarrow H$				
1		t0		KCL	t0		CL	_		
ļ	1	3.4		*	2.31		056	1		
Din Name	Output Driving	(15.3	ارد	*	(13.60	ソ		1		
Pin Name IN	Factor (lu)	1	I					1		
114	10	l						1		
			- 1			1				
			1			1				





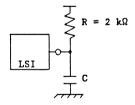
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

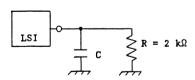
Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-H6SD-E2 | Sheet 1/1

Tri-state Output(IOL=3.2mA) & Schmitt Trigger	e of BC
Tri-state Output(IOL=3.2mA) & Schmitt Trigger   1	ath → IN
H6R	ath → IN
Propagation Delay Parameter   tup   tdn   t0   KCL   t0   KCL   KCL2   CDR2   Parameter	ath → IN
Tup tdn tdn t0 KCL t0 KCL CDR2 Pa 2.24 0.16 3.72 0.13 X 2.42 0.056 2.52 0.13 OT (7.18)	→ IN
TO KCL tO KCL KCL2 CDR2 Pa  2.24 0.16 3.72 0.13 X  2.42 0.056 2.52 0.13 OT  (7.18) (13.57)	→ IN
1N	→ IN
IN	
IN (7.18) (13.57)	, Y
IN T	
от — х	
от х	
$L \rightarrow Z \qquad Z \rightarrow L$	
	→ X
2.07 2.55 0.13	
(15.35) * (13.60)	
(13.55)	
Input Loading	
Pin Name Factor (lu)	
OT 4	
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	
to KCL to KCL	
3.41 2.31 0.056	
Output Driving (15.35) * (13.60)	
Pin Name Factor (lu)	
IN 18	





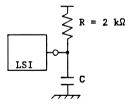
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

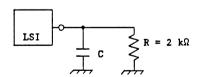
Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-H6R-E2 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CELL	SPECI	FICATIO	N		ט" ו	HB" Version	
Cell Name	Function							Number of BC	
	Tri-state Output	(IOL=3.2m	A) &	Schmitt	Trigger				
H6RU	Input Buffer (TI	L Type, T	rue)	with Pu	11-up Re	sistano	ce	12	
Cell Symbol			Prop	agation	Delay P	aramete	er		
		tup			tdn				
			KCL	t0	KCL	KCL2	CDR		
			.16	3.72			1	X → IN	
		1 1	.056	2.52			1	OT → X	
	1	(7.18)		(13.57	)		l		
IN	<i>&lt;</i> ⊅h			1					
	7						ŀ		
от —	x						1		
01	^								
					1		1		
	С	i i					į	İ	
	Ū				1		Į.		
			$L \rightarrow 2$		,	$Z \rightarrow L$			
		t0		KCL	t0	7 1	KCL	c → x	
		2.07			2.55		0.13		
		(15.35)		*	(13.60	)			
						1			
						-			
	Input Loading					- 1			
Pin Name	Factor (lu)		ı			ŀ			
OT	4								
С	2		H → Z			Z → H			
		t0 3.41		KCL	t0		KCL	$\dashv$	
· · · · · · · · · · · · · · · · · · ·	Output Driving	(15.35)	- 1	*	2.31 (13.60	_	.056		
Pin Name	Factor (Lu)	(13.33)	- 1	~	(13.60	, I			
IN IN	18		- 1			1			
117	1		- 1			- 1			
			- 1		1	- 1			
			- 1						

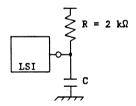


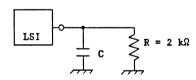


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H6RU-E2 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPEC	IFICATIO	N		T "UHE	" Version
Cell Name	Function							lumber of BC
	Tri-state Output	(IOL=3.	2mA) δ	Schmitt	Trigger			
H6RD	Input Buffer (TT						nce	12
Cell Symbol				pagation				
	<del></del>	t	up	1	tdn			T T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.24	0.16	3.72	0.13			X + IN
		2.42	0.056	2.52	0.13		1	OT + X
		(7.18)		(13.57	)			l
TN								
170	. 🔰							
				1				
ОТ	>→ x							
								l
	1			1			1	
	C			i				
			L →			$Z \rightarrow L$		
		t0		KCL	t0		CL	] c → x
		2.0			2.55		1.13	
		(15.3	5)	*	(13.60	)		
			- 1					1
	<del></del>					1		1
5	Input Loading		- 1					
Pin Name	Factor (lu)		- 1			1		
OT	4			-	ļ			1
С	2	$H \to Z \qquad Z \to$					CT	4
		t0	-+	KCL	t0 2.31		CL 056	4
	Output Driving	(15.3	- 1	*	(13.60		סכט	
Pin Name	Factor (lu)	(13.3	ا (د	-	(13.60	'		
IN IN	18							
114	10		- [					
			1			- 1		
		1						1





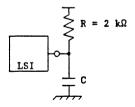
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

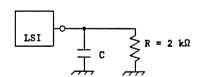
Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-H6RD-E2 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		T"UI	HB" Version
	Function							Number of BC
	Tri-state Output	(IOL=3.	2mA) wi	th Nois	e Limit	Resista		
H8T	& Input Buffer (	True)						9
Cell Symbol			Prop	pagation	Delay Pa	aramete	r	
			up		tdn			
İ		t0	KCL	t0	KCL	KCL2	CDR	
		1.06	0.04	1.84			İ	X → IN
		3.12	0.056	5.66			l	OT → X
		(7.88)		(16.71	'l I		1	
IN —	<b>─</b> < h			I	1		l	
]	7			1			l	
от —	>→ x							
	9						l	
				į			ł	
}	1						l	
	С						Ì	
				<u> </u>	لـــــــلم		L	
l		+0	$L \rightarrow 2$	KCL		$Z \rightarrow L$	CL	$ +$ $+$ $\times$
		t0 2.2	<del>,  </del>	KCL	6.47		13	⊣ <sup>ს 7</sup> ^
l		(16.4	- 1	*	(17.52	1 -	13	
		(10.4	"		(17.32	′		ŀ
1			- 1					
	Input Loading							
Pin Name	Factor (Lu)							
OT	2							
С	2		H → 2			Z → H		_
1		t0	_	KCL	t0		CL	4
	Outrus Dadari	3.0		*	3.20		056	1
Pin Name	Output Driving Factor (£u)	(16.4	47	•	(17.52	'		
IN	36		1			- 1		
						- 1		
1						- 1		
1						1		

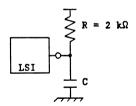


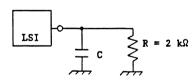


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the  ${\tt simulation}.$

UHB-H8T-E3 | Sheet 1/1

FULLTSU	CMOS GATE ARRAY U	NIT CELL	SPECI	FICATIO	N .		"UHP	" Version
Cell Name	Function	MII OBBB	OI DOI	IIONIIO	<u>'</u>			lumber of BC
	Tri-state Output	(IOL=3.2	mA) wi	th Nois	e Limit	Resista		
H8TU	& Input Buffer (							9
Cell Symbol					Delay P		r	
		tu			tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
ļ			0.04	1.84				X → IN
			0.056	5.66			İ	OT → X
	1	(7.88)		(16.71	기			ļ
IN —	<b>-</b> < h ∣							1
	7							
от —	x -							
01	<b>^</b>						1	
1	i	'						
	C						1	
l							ļ	
			$L \rightarrow Z$			$Z \rightarrow L$	•	
		t0		KCL	t0		CL	] c → x
		2.22			6.47		13	
		(16.44	•)	*	(17.52	)		
						- 1		
	I Tamus Tandina		l			- 1		
Pin Name	Input Loading Factor (lu)					1		
OT OT	Pactor (Lu)		ļ			1		
C C	2		H → Z			Z + H		1
	_	t0		KCL	t0		CL	
		3.07			3.20		056	
	Output Driving	(16.44	)	*	(17.52			
Pin Name	Factor (lu)		1			- 1		
IN	36		i					
	1							
	1							<u> </u>

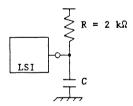


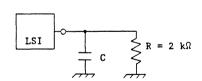


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8TU-E3 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	N		T"UI	HB" Version
Cell Name	Function							Number of BC
	Tri-state Output	(IOL=3.	2mA) wi	th Noise	e Limit	Resista	nce	
H8TD	& Input Buffer (	True) w						9
Cell Symbol			Prop	agation	Delay P		r	
ļ			up		tdn			_
		t0	KCL	t0	KCL	KCL2	CDR:	
		1.06	0.04	1.84				X → IN
		3.12	0.056	5.66				OT → X
	1	(7.88)		(16.71)	기			
IN	<b>-</b> < h							
1	7			l				
от —	x			1				
01	^	'						}
1								
İ	С			1				
	· ·			1			ł	
			$L \rightarrow 2$	!		$Z \rightarrow L$	·	
		t0	=-	KCL	t0		CL	$ c \rightarrow x$
		2.2	2		6.47		13	_
		(16.4	4)	*	(17.52	)		-
1								
				İ				
	Input Loading	1				}		
Pin Name	Factor (lu)		- 1			- 1		
OT	2							
C	2		H → Z			Z → H		_
		t0		KCL	t0		CL	_
	ļ	3.0			3.20	1	056	
h	Output Driving	(16.4	4)	*	(17.52	)		
Pin Name	Factor (lu)	{	ł					
IN	36	İ	Ì			1		
			i					
	1							
	.1	L						

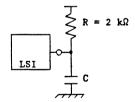


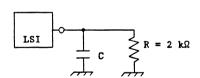


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the  ${\tt simulation}.$

UHB-H8TD-E3 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CELI	SPECI	FICATION	1		"טא	B" Version
Cell Name	Function							Number of BC
	Tri-state Output	(IOL=12r	nA) wit	h Noise	Limit R	esistan	ce	
H8W	& Input Buffer (	True)						9
Cell Symbol			Prop	agation	Delay P	aramete	r	
			ıρ		tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	
		1.06	0.04	1.84				X → IN
		3.96	0.038	7.25				OT → X
	1	(7.19)		(11.84)	)			
IN —	<b>-</b> <- h	1		l			İ	
1		i i		İ	1 1			
								1
от —	x						l	
į	ľ						ļ	
		1					1	1
	_			-	1			1
	С							
			L → 2	<u> </u>	<u> </u>	$Z \rightarrow L$	<u></u>	
		t0	<u> </u>	KCL	t0		CL	$d c \rightarrow x$
		3.6	5	KCD	7.40		054	<b>⊣</b>
		(21.7		*	(11.99		054	1
			,		(11177	′		1
		[		1				1
	Input Loading		- 1					
Pin Name	Factor (lu)	1						
OT	2	1	1			ļ		
C	2		H + 2			$Z \rightarrow H$		
		to	1	KCL	t0	K	CL	7
	ļ	3.7			3.69	0.	038	
	Output Driving	(21.7	3)	*	(11.99	)		
Pin Name	Factor (lu)	ļ `			•			
IN	36	1	1			1		
		1						
	İ	l						
	1	(	ı			1		İ

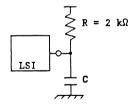


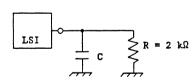


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the  ${\tt simulation.}$

UHB-H8W-E2 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CELL	SPECT	FICATION	V .		<b>"</b> UH	B" Version
	Function		01201					Number of BC
	Tri-state Output	(IOL=12mA	) wit	h Noise	Limit R	esistan		
нswu	& Input Buffer (							9
Cell Symbol	C Input Duller (	1140/ 410			Delay P		r	
OCII DJIIIDOI		tup		Legacion	tdn	ar ame ee	-	T
			KCL	t0	KCL	KCL2	CDR2	Path
			.04	1.84		1.022	- ODINA	X → IN
			.038	7.25			]	OT + X
		(7.19)	.050	(11.84)			1	0
	$\nearrow$	(7.13)		(11.04)	ΊΙΙ		l	1
IN —	<b>─</b> < h				1 1		l	į
	7			1			1	
от	<b>X</b>			1			1	
01	<b>√</b> •						l	1
							1	}
				l			1	ļ
	С				1		ł	1
					1		į .	ì
			L + Z	!		$Z \rightarrow L$	l	
		t0		KCL	t0		CL	⊢ c → x
		3.65	-+-	KCD	7.40		054	-
		(21.73)		*	(11.99		. 054	
		(21.73)			(11.))	'		
			- 1					1
<del> </del>	Input Loading	1						1
Pin Name	Factor (lu)							1
OT	2		- 1					
C	2		H → Z	,		Z → H		-
١	1 4	t0		KCL	t0		CL	-
		3.75		VOD	3.69		038	┥
	Output Driving	(21.73)		*	(11.99	•	. 0.50	1
Din Nama	Factor (lu)	(21.73)	'		(11.33	<b>'</b>		1
Pin Name IN	36	1	- 1	Ì				1
114	30	Į.	- {	İ		- 1		1
			- 1					1
1		1	1					Ì
L	1	l						

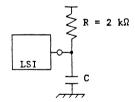


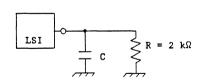


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8WU-E2 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPEC	IFICATION	N .		T"UH	B" Version
Cell Name	Function							Number of BC
	Tri-state Output	(IOL=12	mA) wi	th Noise	Limit R	esistan		
H8WD	& Input Buffer (							9
Cell Symbol				pagation			r	
		t	up	T	tdn			T
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.06	0.04	1.84	0.04			X → IN
		3.96	0.038	7.25	0.054			OT → X
		(7.19)		(11.84)	)		l	
IN							l	
IN	. 🔰							
				1			l	1
ОТ —	→ x							
	LΥ							
							1	1
	I							
	С			ĺ	1			
				1			ĺ	
			L +	Z		$Z \rightarrow L$		
		t0		KCL	t0	K	CL	c → x
		3.6	5		7.40	0.	054	7
		(21.7	3)	*	(11.99	)		
						·		1
		1	- 1					
	Input Loading	1						
Pin Name	Factor (lu)		- 1					1
OT	2	1	- 1					1
С	2		Η →	Z		$Z \rightarrow H$		
		t0		KCL	t0	k	CL	
		3.7	5		3.69	0.	038	
	Output Driving	(21.7	3)	*	(11.99	)		
Pin Name	Factor (lu)	]	-					
IN	36	1	1					
	1		1					
	1	l	- 1					1

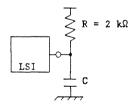


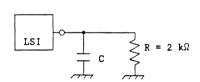


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\rm CL}$  for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8WD-E2 | Sheet 1/1

	CMOS GATE ARRAY U	NIT CELI	SPECI	FICATION	N		"บ	HB" Version
Cell Name	Function							Number of BC
	Tri-state Output	(IOL=24r	nA) wit	h Noise	Limit R	esistan	ce	
H8W2	& Input Buffer (	TTL, Tri						11
Cell Symbol			Prop	agation	Delay P	aramete	r	
		tı	qu		tdn			
		t0	KCL	t0	KCL	KCL2	CDR:	2 Path
		1.06	0.04	1.84	0.04			X → IN
		5.61	0.032	11.62	0.06		İ	OT → X
	_	(8.33)		(16.72)			1	
IN —		}		İ	1		İ	
III	. \	[		Į.			1	
		}			]		l	
от ——	- x			1				
	V9	1					1	
		1					ĺ	
	l .	1		}				
	С						!	
		i						
			L → Z			Z → L		
		t0		KCL	t0		CL	c → x
		5.30	5		11.18	0.	06	
		(23.2	3)	*	(16.28	)		
			- 1	1				
		}	1	j				
	Input Loading		- 1	ŀ		1		
Pin Name	Factor (lu)		1			1		
OT	2							
С	2		H → Z			Z → H		
		t0		KCL	t0		CL	
		6.3	7		5.25	0.	032	
	Output Driving	(23.2	3)	*	(16.28	)		1
Pin Name	Factor (lu)		l	i				
IN	36		İ			1		
		ĺ	ł	1		1		
			- 1	İ		1		
		l	1			- 1		l





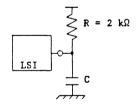
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

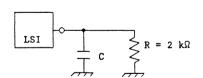
Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8W2-E2 | Sheet 1/1

FUJITSU (	MOS GATE ARRAY U	NIT CELL	SPECI	FICATION	N		<b>"</b> U}	B" Version	
Cell Name	Function	-						Number of BC	
	Tri-state Output	(IOL=24mA	) wit	h Noise	Limit R	esistar	nce		
H8W1	& Input Buffer (	TTL, True	) wit	h Pull-	up Resis	tance	1	11	
Cell Symbol			Prop	agation	Delay P	aramete	er		
		tup		T :	tdn				
		t0	KCL	t0	KCL	KCL2	CDR2	Path	
		1.06 0	.04	1.84	0.04			X → IN	
		5.61 0	.032	11.62	0.06		1	OT → X	
		(8.33)		(16.72	)				
IN -								1	
IN	$\sim$								
				1					
ОТ —	> → x			1			1		
					1		1		
	I			1					
	C						1	Į.	
							l		
l		L → Z				$Z \rightarrow L$			
		t0		KCL	t0		KCL	c → x	
		5.36			11.18	0.	.06		
		(23.23)		*	(16.28	)			
			1						
			1			l		1	
	Input Loading								
Pin Name	Factor (lu)		- 1						
OT	2								
C	2		H → 2			Z → H			
1		t0		KCL	t0		KCL		
		6.37			5.25		.032		
	Output Driving	(23.23)		*	(16.28	)			
Pin Name	Factor (lu)					- 1			
IN	36								
						1			
	1								

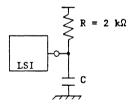


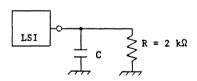


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8W1-E2 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	٧		"UH	B" Version
Cell Name	Function							Number of BC
	Tri-state Output	(IOL=24	mA) wit	h Noise	Limit R	esistar		
наwo	& Input Buffer (							11
Cell Symbol			Prop	agation	Delay P	aramete	er	
		t	up	1	tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
1		1.06	0.04	1.84	0.04			X + IN
		5.61	0.032	11.62	0.06		1	OT + X
		(8.33)		(16.72)				"
		```	ļ	,	1		i	į.
IN —							1	
1	$\setminus$ 1						1	
ОТ	√ x				1		1	-
				ļ			1	
				1			1	
	1						1	-
Ì	С			1		Ì	Í	1
	·						1	1
			L → 2			$Z \rightarrow L$	1	<del></del>
		t0		KCL	t0		KCL	d c → x
		5.3	6	1102	11.18		.06	┥゛¨
		(23.2	-	*	(16.28			
		(33.5	·	1	(20.20	1		
1				į		- 1		
	Input Loading	1	]	1		- 1		1
Pin Name	Factor (lu)	l		1		- 1		<b>J</b>
OT	2	1				i		1
C	2		H → Z	:		$Z \rightarrow H$		_
	_	t0		KCL	t0		KCL	_
1		6.3	7		5.25		.032	7
	Output Driving	(23.2	,	*	(16.28			1
Pin Name	Factor (lu)	\	-/	ĺ	(20.20	´		
IN	36	1	1	j		1		1
		[	- 1	1		l		
1		l		i		- 1		

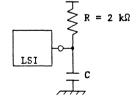


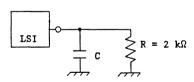


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H8W0-E2 | Sheet 1/1

FULLTSU	CMOS GATE ARRAY U	NIT CEL	T CDF	CIEICATIO	N		, ultri	B" Version
Cell Name	Function	NII CEL	D BIL	CIFICATIO				Number of BC
Cell Name	Tri-state Output	(IDI=3	2mA)	with Nois	o Timit	Pacieta		Number of Bo
нвс	& CMOS Interface				e Dimit	Nesista	ince	9
Cell Symbol		. Input		opagation	Dolar D	aramata		<del></del>
Dell Bymbol		-	up	opaga cion	tdn		1	Т
		t0	KCL	to	KCL	KCL2	CDR2	Path
		0.92	0.04			KCDZ	CDRZ	X → IN
		3.12	0.05				l	$OT \rightarrow X$
		(7.88)		(16.71			l	01 7 7
	1	(7.00)		(10.71	4		l	
IN -	<b>─</b> < h			ļ			l	
1	/ 1			1				1
от	x			- 1			1	
01	^			ı			1	
					1		1	
ŀ				1	1		į.	
	С			1			1	1
1	C			1	į		1	
1			L →			$Z \rightarrow L$	i	<del> </del>
ľ		t0		KCL	t0		CL	d c → x
		2.2	2		6.47		0.13	1 "
		(16.4	4)	*	(17.52			1
1		,	1		(	´		İ
1		1						
	Input Loading	1						
Pin Name	Factor (lu)		1			1		
OT	2	1	1					1
С	2	l	H →	Z		$Z \rightarrow H$		1
1		t0		KCL	t0	K	CL	7
1		3.0	7		3.20	0.	.056	7
	Output Driving	(16.4	4)	*	(17.52	)		
Pin Name	Factor (lu)	'						
IN	36		ı					1
1								
1		l	l					
		1				- 1		1





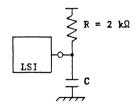
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

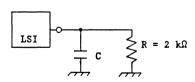
Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-HSC-E3 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		T"UH	B" Version
	Function							Number of BC
	Tri-state Output(	IOL=3.2	mA) w/	Noise L	imit Res	istance		
нвси	CMOS Interface In							9
Cell Symbo		<u> </u>			Delay P			
		t	up	T	tdn			7
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.92	0.04	1.33	0.04			X → IN
		3.12	0.056	5.66	0.13			OT → X
		(7.88)		(16.71				
IN				l				
114	$\mathcal{N}$			<b>!</b>			1	1
OT -	-			l				
	M			1				
				ļ				
	•	1		1			1	
	C	i 1					ĺ	1
				<u> </u>				
		L → Z				$Z \rightarrow L$		
		t0		KCL	t0		CL	_ c → x
		2.2	4		6.47		13	1
		(16.4	4)	*	(17.52	)		1
						- 1		
		l	1					1
	Input Loading	1	1					1
Pin Name	Factor (lu)	l				ł		
OT	2				ļ			4
С	2		H → Z			Z → H		4
		t0		KCL	t0		CL	-
	<del> </del>	3.0		*	3.20		056	1
Dia Nasa	Output Driving	(16.4	4)	*	(17.52	,		
Pin Name IN	Factor (lu)	1						
IN	30	1				ļ		1
		1						1
		1						1
	1	ı	1		i	1		1

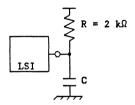


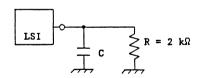


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\mbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8CU-E3 | Sheet 1/1

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UHI	B" Version
Cell Name	Function							Number of BC
	Tri-state Output(	IOL=3.2	mA) w/	Noise L	imit Res	istance	&	
H8CD	CMOS Interface In							9
Cell Symbol		ĺ	Prop	agation	Delay P.	aramete	r	
		t	up	1	tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.92	0.04	1.33				X + IN
		3.12	0.056	5.66	, ,			OT + X
		(7.88)		(16.71				
		(,,,,,,		(	1 1		1	]
IN -	<b>─</b> < ħ				1		l	ì
	N 1							
от —	-						1	
01	1 × "				1		l	
		1 1		l	1 1		l	Ì
	1				1 1			
	С	1 1		1	1 1			į
	C	1 1			1 1		ļ	
			L + Z	<u> </u>	لـــــــــــــــــــــــــــــــــــــ	$Z \rightarrow L$	<u> </u>	ļ
		to		KCL	t0		CL	d c → x
		2.2		KCL	6.47		0.13	-
				*			1.13	İ
		(16.4	4)	•	(17.52	,		
						1		1
		1	1			- 1		l
	Input Loading	l				ł		l
Pin Name	Factor (lu)	1				į		
TO	2							4
С	2		H → Z			Z → H		1
		t0		KCL	t0		CL	1
		3.0			3.20		056	
	Output Driving	(16.4	4)	*	(17.52	)		
Pin Name	Factor (lu)					1		
IN	36	)				- 1		1
						- [		1
		l	- 1			- 1		1
	1	1				1		1

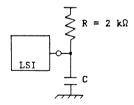


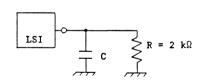


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H8CD-E3 | Sheet 1/1

Tri-state Output(IOL=12mA) with Noise Limit Resistance & CMOS Interface Input Buffer (True)	FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPE	CIFICATIO	N			" Version
H8E	Cell Name	Function							lumber of BC
Cell Symbol		Tri-state Output	(IOL=12	mA) w	ith Noise	Limit Re	sistance		
To   KCL   t0   KCL   CDR2   Path		& CMOS Interface	Input	Buffe:	r (True)				9
TN OT  C    C   C   C   C   C   C   C   C   C	Cell Symbol			Pro	opagation	Delay Pa	rameter		
O.92 0.04 1.33 0.04 VX + OT +  C  L + Z Z + L  t0 KCL t0 KCL  3.65 (21.73) * (11.99)  C + Din Name Factor (lu)  OT 2  C 2 H + Z Z + H  t0 KCL t0 KCL  3.65 (21.73) * (11.99)			t	up		tdn			
IN OT  C  L + Z  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D			t0	KCL	t0	KCL	KCL2	CDR2	Path
IN OT  C  L + Z  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D  T + D			0.92	0.04	1.33	0.04			X → IN
IN  OT  C  L + Z  D + L  TO  KCL  3.65  (21.73)  TO  C  TO  C  TO  C  TO  C  TO  C  TO  C  TO  C  TO  C  TO  C  TO  C  TO  C  TO  TO			3.96	0.03	8 7.25	0.054			OT → X
IN  OT  C  L + Z  D + L  t0			(7.19)		(11.84	)			
OT C  L + Z Z + L  t0 KCL t0 KCL  3.65 (21.73) * (11.99)  Pin Name Factor (lu)  OT 2 C 2 H + Z Z + H  t0 KCL t0 KCL  3.65 (21.73) * (11.99)	T.N					1	1		
C  L + Z Z + L  t0 KCL t0 KCL  3.65 (21.73) * (11.99)  Pin Name Factor (lu)  OT 2 C 2 H + Z Z + H  t0 KCL t0 KCL  3.65 (21.73) * (11.99)  OT 0	111	$\sim$			ŀ	1			
C  L + Z Z + L  t0 KCL t0 KCL  3.65 (21.73) * (11.99)  Pin Name Factor (lu)  OT 2 C 2 H + Z Z + H  t0 KCL t0 KCL  3.65 (21.73) * (11.99)  OT 0					Į.	1			
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	ОТ —	+ <b>→</b> x		1		1			
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		M		l		1			
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			1			1			
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		1				1	l i		
t0 KCL t0 KCL C →  3.65 (21.73) * (11.99)  Pin Name Factor (lu)  OT C 2 H → Z Z → H  t0 KCL t0 KCL C →  H → Z Z → H  t0 KCL t0 KCL 3.75 3.69 0.038  Output Driving (21.73) * (11.99)		С							
t0 KCL t0 KCL C →  3.65 (21.73) * (11.99)  Pin Name Factor (lu)  OT C 2 H → Z Z → H  t0 KCL t0 KCL C →  H → Z Z → H  t0 KCL t0 KCL 3.75 3.69 0.038  Output Driving (21.73) * (11.99)									
3.65 (21.73) * (11.99) 0.054    Pin Name   Input Loading Factor (lu)   OT   2				L →					
C   C   C   C   C   C   C   C   C   C					KCL		KCL		C → X
Pin Name   Input Loading   Factor (lu)			3.6	5		7.40	0.05	4	1
Pin Name         Factor (lu)         Image: Control of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property			(21.7	3)	*	(11.99)	J		
Pin Name         Factor (lu)         Image: Control of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property of the property				- 1			l l		
Pin Name Factor (lu)  OT 2  C 2 H → Z Z → H  t0 KCL t0 KCL  3.75 3.69 0.038  Output Driving (21.73) * (11.99)									
OT 2 2	, , , , , , , , , , , , , , , , , , , ,	Input Loading	1	1					1
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Pin Name	Factor (lu)	İ	- 1					l
t0 KCL t0 KCL 3.75 3.69 0.038 Output Driving (21.73) * (11.99)	OT	2	1	- 1					
t0 KCL t0 KCL 3.75 3.69 0.038 Output Driving (21.73) * (11.99)	С	2		H →	Z		Z → H		1
3.75 3.69 0.038 Output Driving (21.73) * (11.99)			t0					,	1
Output Driving (21.73) * (11.99)				5		3.69	0.03	8	1
		Output Driving	(21.7	3)	*	(11.99)			
	Pin Name	Factor (lu)	l	·		` ′			1
IN 36			1				I		1
			1						1
		1		1		}	İ		
				1		į			1

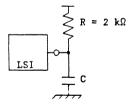


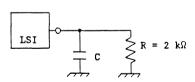


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8E-E2 | Sheet 1/1

FULLTELL	CMOS GATE ARRAY U	NIT CEL	CDEC	ITICATIO	.,	— т	TILLD	" Version
Cell Name	Function	NII CEL	L SPEC	IFICALIU.	IN			umber of BC
DELL Name	Tri-state Output(	TOT=12m	A) wi+	h Noise	Timit Rosi	stance &		duper of pc
нвец	CMOS Interface In							9
Cell Symbo		put bul			Delay Par			
GCII Bymbo.		+	up	I	tdn	<u>umerer</u>		
		t0	KCL	t0	KCL	KCL2 C	DR2	Path
İ	!	0.92	0.04	1.33				X → IN
		3.96	0.038			l		OT → X
}		(7.19)		(11.84	)	1		
711		` ′		1		1		
IN -	$\sim$					]		
					i			
OT -	→ x							
	V							
				1				
	ľ			1				
	С							
				<u> </u>				
			L +			Z → L		
		t0		KCL	t0	KCL		C → X
		3.6		*	7.40	0.054		
		(21.7	ا (د		(11.99)			
	Input Loading	1	- 1					
Pin Name	Factor (lu)					1		
OT	2	1						
c	2	<b></b>	H →	Z		$Z \rightarrow H$		
	_	t0	T	KCL	t0	KCL		1
		3.7	5		3.69	0.038		1
	Output Driving	(21.7	3)	*	(11.99)			
Pin Name	Factor (lu)		1			1		
IN	36	1	ł					
			- 1			1		
			ı					
1	1	1	- 1		I	1		I

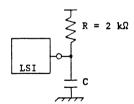


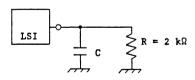


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8EU-E2 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"ИНВ	" Versi	on
Cell Name	Function								
	Tri-state Output(	IOL=12m	A) with	Noise	Limit Res	istance			
H8ED	CMOS Interface In							9	
Cell Symbo	1		Prop	agation	Delay Pa	rameter			
			up		tdn		,		
1		t0	KCL	t0	KCL	KCL2	CDR2		
1		0.92	0.04	1.33			l	X →	
1		3.96	0.038	7.25	1			OT → :	X
l	/	(7.19)		(11.84	'		ł		
IN -	—< h			ŀ					
]				ŀ			į		
от —	$\rightarrow$ $\times$								
				ł					
				į	]				
	1			1					
	С			1	1				
							<u> </u>		
			L + 2			Z → L		_	
		t0		KCL	t0	KC		C→	X
		3.6		*	7.40	0.0	154		
		(21.7	ا (د	•	(11.99)	- 1			
1			ł						
	Input Loading		i			l		l	
Pin Name	Factor (lu)								
OT	2		- 1						
C	2		H → 2	Z		$Z \rightarrow H$		1	
		t0		KCL	t0	KC	CL	1	
1		3.7	5		3.69	0.0	38	1	
	Output Driving	(21.7	3)	*	(11.99)			1	
Pin Name	Factor (lu)		ļ						
IN	36				l	İ		1	
					Ì			İ	
		l			<u> </u>			<u> </u>	

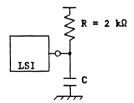


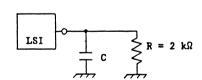


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8ED-E2 | Sheet 1/1

FULLTSUIC	MOS GATE ARRAY U	NIT CEI	T SDECT	FICATIO	N		מעוויי ו	" Version
	unction	MII CEL	L SPECI	FICATIO	N		I ONB	Number of BC
	Tri-state Output	(IOL=24	mA) w/	Noise L	imit Resis	stance	<del></del>	Number of Bu
	& Input Buffer (						- 1	11
Cell Symbol				agation	Delay Par	rameter		
		t	up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.92	0.04	1.33				X → IN
		5.61	0.032	11.62	1			OT → X
		(8.33)		(16.72	)			
IN —	<b>-</b> < h ∣				1 1			
1	\ 7							
то Т	<b>x</b>							
01	^ ^			1	1			
					1			
				Ì	1 1			
ł	С			İ				
	_			İ				
1			L + 2	ż		$Z \rightarrow L$		
		t0		KCL	t0	KC	L	$C \rightarrow X$
		5.3			11.18	0.0	)6	
		(23.2	3)	*	(16.28)			
ł			1			1		
<b>]</b>	T =					1		
B45 None	Input Loading					1		•
Pin Name OT	Factor (lu)		1			1		
C	2 2	<b></b>	H → 2	7.		$Z \rightarrow H$		
"	-	t0	<del>- "' '</del>	KCL	t0	I KC	:T.	
		6.3	7		5.25	0.0		
	Output Driving	(23.2		*	(16.28)		_	
Pin Name	Factor (lu)	,			, , , , ,	1		
IN	36	1	1			1		
1		l	- 1			- [		
1		1			l	- 1		
	1	l	- 1		l	1		l

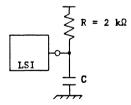


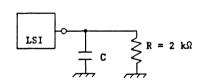


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H8E2-E2 | Sheet 1/1

FULLTSU	CMOS GATE ARRAY U	NIT CEL	I. SPEC	IFICATIO	N	T	UHB	" Version
Cell Name	Function	000	<u> </u>		• • • • • • • • • • • • • • • • • • • •			umber of BC
	Tri-state Output(	IOL=24m	A) w/ 1	Noise Li	mit Resis	tance	1	
H8E1	& Input Buffer(CM	OS, Tru	e) w/ 1	Pull-up	Resistance	е		11
Cell Symbo	1		Pro	pagation	Delay Pa:	rameter		
		t	up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	
		0.92	0.04	1.33	1	i		X → IN
		5.61	0.032			1		OT → X
	_	(8.33)		(16.72	)	į		
IN —	<b></b> < h				1 1	ł		
	7				1 1	j		
0.7	- x			1	1 1			
OT -	X X				1 1			
						l		
1				1	1			
l	С							
	•				1 1			
			L +	Z		$Z \to L$		
		t0		KCL	t0	KCL		C → X
		5.3	6		11.18	0.06		
		(23.2	3)	*	(16.28)	1	i	
1								
<u></u>								
	Input Loading		1			1		
Pin Name	Factor (lu)		- 1			1		
OT	2				ļ			
C	2		H → :			Z → H		
l		t0 6.3	<del>,  </del>	KCL	t0 5.25	0.03		
<u> </u>	Output Driving	(23.2		*	(16.28)	1 0.03	4	
Pin Name	Factor (lu)	(23.2	ا (`	•	(10.20)	- 1		
IN	36		1		Ì	1		
1 *"	1 -0		- 1			1		
	1		- 1		l			
1	1				1	1		





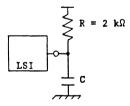
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

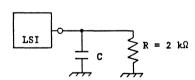
Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8E1-E2 | Sheet 1/1

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		"UHB	" Version
Cell Name								umber of BC
	Tri-state Output(	IOL=24m	A) w/ N	Noise Li	mit Resis	tance		
H8E0	& Input Buffer(CM	OS, True	e) w/ I	Pull-dow	n Resista:	nce		11
Cell Symbo	1		Prop	pagation	Delay Pa	rameter		
			up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	
		0.92	0.04	1.33		i	]	$X \rightarrow IN$
		5.61	0.032	1		l		$OT \rightarrow X$
	1	(8.33)		(16.72	)	- 1		
IN	<b>─</b> < h				1	1		
	7					l		
	\			1				
от —	→ x	1 1		l	l l		- 1	
	V	1 1		İ	i i		- 1	
		1		1		i		
	Ċ							
	C	1 1		ĺ				
			L + 2	7		$Z \to L$		
		to		KCL	t0	KC	L L	c → x
		5.3	6		11.18	0.0		-
		(23.2	3)	*	(16.28)			
		,			` '	- 1		
		]						
	Input Loading	]	- 1					
Pin Name	Factor (lu)		1					
TO	2							
С	2		H + 2			Z → H		
	ŀ	t0		KCL	t0	KC		
		6.3			5.25	0.0	32	
<b>5.</b>	Output Driving	(23.2	3)	*	(16.28)			
Pin Name	Factor (lu)	ļ	- 1			1		
IN	36		- 1			1		
					l	1		
	1	l .	- 1			1		





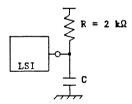
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

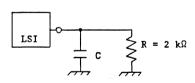
Note: 1. The unit of K<sub>CL</sub> for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8E0-E2 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		Т"ИНВ	" Version
Cell Name	Function							umber of BC
	Tri-state Output	(IOL=3.	2mA) &	Schmitt	Trigger			
H8S	Input Buffer (CM					Resist	ance	13
Cell Symbol					Delay Pa			
		t	up	T	tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		2.48	0.16	3.08	0.10			X → IN
		3.12	0.056	5.66	0.13		l	OT → X
		(7.88)		(16.71)	)		1	
IN	$-\pi$			1	1 1			
114					1		1	
OT	<b>x</b>			1				
	Y						l	
				İ	1 1		1	
	,			1	1 1			
	C			1	1 1			
				l				
			$L \rightarrow 2$			$Z \rightarrow L$		
		t0		KCL	t0		CL	C → X
		2.2			6.47		13	
		(16.4	4)	*	(17.52	)		
		1						
	Input Loading		- 1			1		
Pin Name	Factor (lu)	1	1					
OT	2	ļ						
С	2		H → 2			Z + H		
		t0		KCL	t0		CL	1
	Donate De de d	3.0		*	3.20		056	
Die Nees	Output Driving	(16.4	4)	*	(17.52	<b>,</b>		
Pin Name IN	Factor (lu)		1					
IN	10	l				- 1		
	1		- 1	1		- 1		
			ļ			1		ŀ





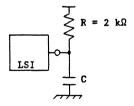
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

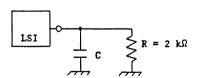
Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- The parameters in parentheses are the values applied to the simulation.

UHB-H8S-E2 | Sheet 1/1

בויוודכון כ	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version										
	Function	OLD	D DI LUI	1 10/110	17		1 7	Number of BC			
17	ri-state Output(	IOL=3.2	mA) & S	chmitt	Trigger		$\neg \uparrow$				
	nput Buffer(CMOS					sistano	e				
	/ Pull-up Resist	ance						13			
Cell Symbol			Prop	agation	Delay P		r				
			up		tdn						
		t0	KCL	t0	KCL	KCL2	CDR2				
		2.48	0.16	3.08			l	X + IN			
		3.12 (7.88)	0.056	5.66				OT → X			
	<i>√</i>	(7.00)		(10.71	1		l				
IN —	~~\rangle \frac{1}{2} \rangle \frac{1}{2}						1				
	\ 1						1				
от —	> x			1			l				
l l											
				į			1				
	Ċ						l				
	С					ľ	1				
			$L \rightarrow 2$		1	$Z \rightarrow L$	L				
		t0		KCL	t0		CL	d c → x			
		2.2			6.47		13	7 "			
		(16.4	4)	*	(17.52	)					
			- 1								
Dia Nama	Input Loading										
Pin Name OT	Factor (lu)		- 1					1			
C	2		H → 2	·		Z + H		┥ ゚			
	_	t0	<del></del>	KCL	t0		CL	┪ .			
		3.0	7		3.20		056	7			
	Output Driving	(16.4	4)	*	(17.52	) [					
Pin Name	Factor (lu)		- 1			1					
IN	18					1					
ļ			j								
			- 1								
	<u> </u>				<u> </u>						





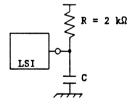
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

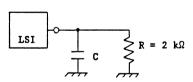
Note: 1. The unit of  $K_{\mbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- The parameters in parentheses are the values applied to the simulation.

UHB-H8SU-E2 Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	1		"Uł	B" Version
Cell Name	Function							Number of BC
	Tri-state Output(							
ı	Input Buffer(CMOS		True) w	/ Noise	Limit Ro	esistan	ce	
H8SD	w/ Pull-down Resi	stance						13
Cell Symbo	1			agation	Delay P	aramete	r	
			up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	
		2.48	0.16	3.08			l	X → IN
		3.12 (7.88)	0.056	5.66 (16.71)			İ	OT → X
	<b>∕</b> €1	(7.00)		(10.71	ή Ι			
IN —	—<√\h			1	1 1		ļ	1
	N 71			i				}
от —	-  >- - x			1	1 1		l	
				ì	1 1		İ	
				1	1 1		İ	1
	ı						į	1
	C				1			ì
				<u> </u>				
			$L \rightarrow Z$			$Z \rightarrow L$		┩╻
		t0 2.2		KCL	6.47		CL	C → X
		(16.4			(17.52		13	
		(10.4	"'	•	(17.52	'		1
		ŀ						
·	Input Loading							1
Pin Name	Factor (lu)							
OT	2					1		
С	2		H → Z	;		Z + H		7
		tO KCL tO						7
		3.0			3.20	0.	056	
	Output Driving	(16.4	4)	*	(17.52	)		
Pin Name	Factor (lu)							
IN	18					1		
		L		1				l





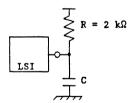
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

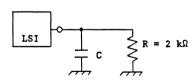
Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- The parameters in parentheses are the values applied to the simulation.

UHB-H8SD-E2 Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CELL S	PECT	FICATIO	N		"U	HB" Version
Cell Name	Function	0000		1 1011110	``			Number of BO
-	Tri-state Output	(IOL=3.2mA	۸ (	Schmitt	Trigger			
H8R	Input Buffer (TT						stance	13
Cell Symbol			Prop	agation	Delay P	arame	eter	
		tup			tdn			
1		t0 K	CL	t0	KCL	KCL	L2 CDR	2 Path
		2.24 0.	16	3.72	0.13			X + IN
			056	5.66		l	1	OT → X
İ	_	(7.88)		(16.71)	)[	[	l	1
IN —	<b>-</b> < <b>⊅</b> h			1	1	ł		
1	, 7				1	l		1
	<b> </b> \				1	1	ı	
ОТ —	x				1	l		
	ľ				1			
					1	l		
	<u>'</u>			1	1			
	С			1	İ	l		
		ļ <u>-</u>	→ Z	L		$\frac{1}{Z}$	<del>-</del> ـــــ	
		t0		KCL	t0	<del>- 2 - 7</del>	KCL	$ c \rightarrow x$
		2.22	+	VCT	6.47		0.13	° → ^
1		(16.44)	l	*	(17.52		0.13	
l		(10.44)		•	(17.52	"		
}			1					
	Input Loading		1	ļ		ĺ		
Pin Name	Factor (lu)		1					
OT	2		1					
C	2	н	→ Z			$\frac{1}{Z}$	н	
	_	t0		KCL	t0		KCL	_
		3.07	T		3.20	,	0.056	
	Output Driving	(16.44)	1	*	(17.52			
Pin Name	Factor (Lu)	` ′			,			
IN	18					- 1		
	1		1			- 1		
	1	l	1			- 1		

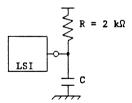


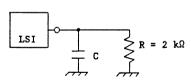


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8R-E2 | Sheet 1/1

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATIO	N		וט"	HB" Version
Cell Name	Function							Number of BC
	Tri-state Output(							
HBRU	<pre>Input Buffer(TTL w/ Pull-up Resist</pre>		rue) w/	Noise .	Limit ke	Sistand	·e	13
Cell Symbo		ance	Prop	agation	Delay P	aramata		13
Cell Bymbo	1	+	up	agation	tdn		-1	1
		t0	KCL	t0	KCL	KCL2	CDR	2 Path
		2.24	0.16	3.72			1	X + IN
		3.12	0.056	5.66			1	OT → X
	_	(7.88)		(16.71			1	
IN -	$-\sqrt{\pi}$						1	1
114								1
				İ				ı
OT	→ x			1				
	VY							
				j				
	Ċ	j					1	
	С			1				
			$L \rightarrow Z$		لــــــا	$Z \rightarrow L$	<u></u>	
		t0		KCL	t0		CL	$\neg \mid c \rightarrow x$
		2.2			6.47	0.	13	7
		(16.4	4)	*	(17.52	)		
		]						
		]						
	Input Loading							
Pin Name	Factor (lu)	1	1					
OT	2							_
С	2	<u> </u>	H → Z			Z → H	, C.T.	_
		t0 3.0		KCL	t0 3.20		CL	_
	Output Driving			*			056	
Pin Name	Factor (lu)	(16.4	47	•	(17.52	'		
IN IN	18	1						
211								
	1		- 1					1





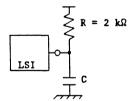
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

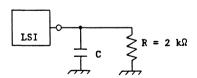
Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8RU-E2 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION				HB" Version
Cell Name	Function							Number of BC
	Tri-state Output(							
	Input Buffer(TTL	Type, T	rue) w/	Noise I	imit Re	sistanc	e	
H8RD	w/ Pull-down Resi							13
Cell Symbo			Prop	agation	Delay P	aramete	r	
		t	up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR	2 Path
		2.24	0.16	3.72	0.13			X → IN
		3.12	0.056	5.66	0.13		1	OT → X
		(7.88)		(16.71)	i i		1	
	$\mathcal{A}$	` ′		' '	1 1			
IN				1			ł	
	N 1						1	
ОТ	-				1 1		1	
							l	
				]	1		l	
				1			l	
	С			1			ĺ	
	· ·							
		<b></b>	$L \rightarrow 2$	!		$Z \rightarrow L$	<u> </u>	<del></del>
		t0		KCL	t0		CL	$\dashv c \rightarrow x$
		2.2	2		6.47		13	┥ ゛ ¨
		(16.4		*	(17.52			
		(20.4	7	1	(17.52	′		
		l		1		l		
	Input Loading	1	- 1	l				
Pin Name	Factor (lu)	ĺ	- 1	į				
OT	2	1	-	I				
C	2		H → 2	,		$Z \rightarrow H$		
C		t0	11 - 2	KCL	t0		KCL	
		3.0	7	VOT	3.20		056	_
	Output Driving	(16.4		*	(17.52		0.00	
Pin Name	Factor (lu)	(10.4	·*/	" [	(17.32	'		
IN IN	18	-	-	1		1		
IN	10					1		
		(				1		
		ł						



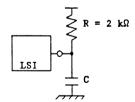


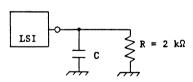
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

simulation.

UHB-H8RD-E2 | Sheet 1/1 |

	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	<u> </u>			B" Version
Cell Name	Function							Number of BC
H6TF	Tri-state Output	(IOL=8m						8
Cell Symbol				agation			r	
			up		tdn			J
		t0	KCL	t0	KCL	KCL2	CDR2	
		1.06	0.04 0.056	1.84	0.04			X + IN
		2.51 (7.27)	0.056	3.27 (8.63)	0.063		ŀ	OT → X
	/	(1.2/)		(0.03)			ł	
IN —	<b>─</b> < h							
	N 7						l	
от	→ x						l	
	[ ]							
					1			
	1						ł	
	С	,					1	
							L	_
		<u> </u>	L + Z			Z + L		
		t0		KCL	t0		CL	C → X
		2.2		*	3.35		063	
		(18.6	<sup>2)</sup>		(8.71	'		
		1	- 1	- 1				1
	Input Loading	1	Į.			l		
Pin Name	Factor (lu)		- 1			1		
OT	4	1	- 1			1		
С	2		H → Z			Z + H		7
		t0	T	KCL	t0	K	CL	
		3.1	2		2.37		056	
	Output Driving	(18.6	2)	*	(8.71	)		
Pin Name	Factor (lu)	1	ŀ			- 1		
IN	36	1	1	1		1		
		l	ı			l		1





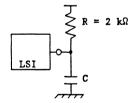
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

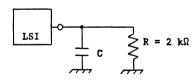
Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

UHB-H6TF-E1 | Sheet 1/1 | Page 20-93

FUJITSU (	CMOS GATE ARRAY U	NIT CELL SE	ECIFICATIO	N		'UHB	" Version
Cell Name	Function			<u> </u>			umber of BC
	Tri-state Output	(IOL=8mA) &	Input Buf	fer (True)		1	
H6TFU	with Pull-up Res			,			8
Cell Symbol			ropagation	Delay Par	ameter		
		tup		tdn			
		to KO	L to	KCL	KCL2 CI	DR2	Path
		1.06 0.0	1.84	0.04			X + IN
		2.51 0.0	56 3.27	0.063			OT → X
	_	(7.27)	(8.63		1		
IN —			1				
IN			1	1 1	ĺ		
			1		- 1		
OT -	> <b>x</b>		1		j		ì
			1		-		
			Į				l
	1		1	1 1	1		
	C						
			→ Z		→ L		
		t0	KCL	t0	KCL		C → X
		2.29		3.35	0.06	3	
		(18.62)	*	(8.71)	1		!
					1		Ì
					1		
	Input Loading		1				
Pin Name	Factor (lu)		1		l		1
OT	4						_
С	2		→ Z		→ H		]
	•	t0	KCL	t0	KCL		1
	ļ	3.12	1 .	2.37	0.05	6	
	Output Driving	(18.62)	*	(8.71)			1
Pin Name	Factor (lu)						ļ
IN	36		1		1		I
	Į.		1		1		l
	1				1		
	1	l	1	l	1		1

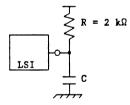


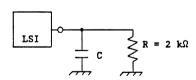


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H6TFU-E1 | Sheet 1/1

TUITTCU (	DMOC CATE ADDAY D	NITE OF	r coro	TTCATTO			1 111111	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,
Cell Name	CMOS GATE ARRAY U Function	NII CEL	L SPECI	FICATIO	N			" Version Tumber of BC
Cell Name	Tri-state Output	(TOT -0-	A) C 7-	D	fam (Tm)	-7		dumber of BC
H6TFD	with Pull-down R	(10D-0m	A) & 11	iput Bur	rer (1ru	e)		
Cell Symbol	with Pull-down R	esistan			D-1 D			8
Cell Symbol				pagation	tdn		<u> </u>	Υ
		t0	up KCL	to	KCL	KCL2	CDR2	Path
ı						KULZ	CDR2	
1		1.06	0.04	1.84				X → IN
İ		2.51	0.056	3.27				OT → X
	1	(7.27)		(8.63	4			
IN —	<b>-</b> < h		Ì		1			
	\ \				1			
	\			1				1
OT -	x			İ	1			
	ľ			1	1			
				1	1			
	_		1	1				1
	С		Ì					
			L	<u></u>	<u> </u>		L	
			L + 2			$Z \rightarrow L$		
		t0		KCL	t0		CL	C → X
ı		2.2			3.35		063	ļ
		(18.6	2)	*	(8.71	)		
			1			- 1		
			1					
	Input Loading		1			į		
Pin Name	Factor (lu)					1		
OT	4							_
С	2		H → 2			Z → H		]
	1	t0		KCL	t0		CL	]
		3.1			2.37		056	
	Output Driving	(18.6	2)	*	(8.71	)		
Pin Name	Factor (lu)							
IN	36		ł					
ı			i			- 1		
ı			l			- 1		
	1		- 1			1		1





- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

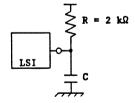
Note: 1. The unit of  $K_{\mbox{CL}}$  for paths OT, C to X is ns/pF.

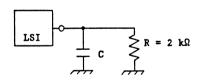
- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- The parameters in parentheses are the values applied to the simulation.

UHB-H6TFD-E1 | Sheet 1/1

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION UHB" Version Cell Name Function Number of BC Tri-state Output(IOL=8mA) **H6CF** & CMOS Interface Input Buffer (True) Cell Symbol Propagation Delay Parameter tup tdn ±0 KCL t0 KCL KCL2 | CDR2 Path 0.92 0.04 1.33 0.04 X + IN OT → X 2.51 0.056 3.27 0.063 (7.27)(8.63)IN OT  $L \rightarrow Z$  $Z \rightarrow L$ t0 KCL t0 KCL C → X 2.29 3.35 0.063 (18.62)(8.71)Input Loading Pin Name Factor (lu) OT 2 H → Z Z → H C t0 KCL t0 KCL 2.37 3.12 0.056 Output Driving (8.71)(18.62)Factor (lu) Pin Name IN

\* These values are subject to external loading condition. Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:





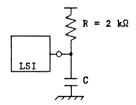
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

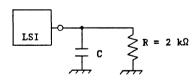
Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.

- Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- The parameters in parentheses are the values applied to the simulation.

UHB-H6CF-E1 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	1		<b>"</b> U	нв'	Version
Cell Name	Function			<del></del>					umber of BC
	Tri-state Output	(IOL=8m	A) & Ch	10S Inter	face In	put Buf	fer		
H6CFU	(True) with Pull	-up Res							8
Cell Symbol				pagation			r		
			up	<u> </u>	tdn		CDD	ᅴ	<b>.</b>
		t0	KCL	t0	KCL	KCL2	CDR	2	Path
		0.92 2.51	0.04	1.33	0.04			- 1	$X \rightarrow IN$ OT $\rightarrow X$
[		(7.27)		(8.63)				-	01 7 X
	/	(1.2/)		(8.65)	1				
IN —	<b>─</b> < h			1				- 1	
	N 1			j			l		
от	- → x						1	- 1	
ļ	L9			1			1	- 1	
				1			1		
	ı			1	1			- 1	
	С			ì			l	ı	
				<u> </u>	<u> </u>		<u> </u>	_	
		<u> </u>	L → i			$Z \rightarrow L$	CL	$\dashv$	6 . v
l		t0 2.2	<del>.  </del>	KCL	±0 3.35		0.063	$\dashv$	C → X
		(18.6		*	(8.71		.003	'	
1		(10.0	2)	.	(6.71	'		ı	
1			1			1		١	
	Input Loading	1		ŀ				ļ	
Pin Name	Factor (lu)	1		İ					
OT	4	1		i					
С	2		H → :	Z		$Z \rightarrow H$			
	1	t0		KCL	t0	, k	CL		
		3.1	2		2.37	0.	056		
	Output Driving	(18.6	2)	*	(8.71	)			
Pin Name	Factor (lu)	Į.		ł		1		1	
IN	36	1	i	j		1		İ	
1			- 1						
			1						
		L							<u> </u>

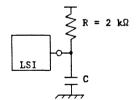


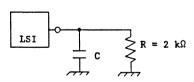


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H6CFU-E1 | Sheet 1/1

FUJITSU (	MOS GATE ARRAY U	NIT CEL	L SPE	CIFICATIO	N		่ "บา	dB" Version
Cell Name	Function						1	Number of BC
	Tri-state Output	(IOL=8m	A) &	CMOS Inte	rface In	put Buf	fer	
H6CFD	(True) with Pull	-down R					1	8
Cell Symbol			Pr	opagation	Delay P	aramete	r	
			up		tdn			
		t0	KCL		KCL	KCL2	CDR:	
		0.92	0.04				1	X + IN
		2.51	0.05				l	OT → X
1	/	(7.27)		(8.63	기 :		1	İ
IN —	<b>-</b> < h ∣			1			l	
	7							
от —	<b>X</b>						l	
01	^						l	1
				1			l	
							1	
	С			l			l	
	ŭ			l	1			
			L →	Z		$Z \rightarrow L$		
		t0	T	KCL	t0	ŀ	CL	c → x
İ		2.2	9		3.35	C	0.063	7
		(18.6	2)	*	(8.71	)		1
			- 1					
	Input Loading		1					
Pin Name	Factor (lu)							
OT	4							_
C	2		Н →		4.0	Z → H	7.CT	-
l		t0 3.1	<del>,  </del>	KCL	±0 2.37		CL .056	_
<b></b>	Output Driving	(18.6		*	(8.71		סכט	
Pin Name	Factor (lu)	(10.0	ا ر-	- 1	(0.71	'		1
IN	36		į			- 1		
1								
	ļ					- 1		

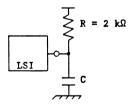


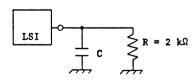


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H6CFD-E1 Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	٧		<b>"</b> ຫ	HB" Version
Cell Name	Function				·		Ť	Number of BC
	Tri-state Output	(IOL=8m	A) with	Noise I	Limit Re	sistance	3	
H8TF	& Input Buffer (	True)						9
Cell Symbol				agation				
		t	up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR:	
		1.06	0.04	1.84		i		X + IN
1		3.21	0.056	5.96	•	ļ		OT → X
ł	1	(7.97)		(11.91)	ן	}		
IN —	<b>-</b> < h ∣					1		
	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \			1				
от —	<b>X</b>			1				
01	^ *			ł				
1		l l		l				
	С	1		ł				
	J							
i			L + 2	2		$Z \rightarrow L$		
		t0		KCL	t0	K	CL	c → x
l		2.6	2		6.82	0.0	070	
		(19.7	1)	*	(12.77	)		ļ
				ļ		ı		
		l	- 1					
	Input Loading					1		İ
Pin Name	Factor (lu)							
OT	2							_
С	2	$H \rightarrow Z$ $Z \rightarrow H$						
i		t0		KCL	t0		CL	_
	10	3.3		*	3.21		056	1
Dia Name	Output Driving	(19.7	1)	~	(12.77	,		
Pin Name IN	Factor (lu)	1	ŀ					
111	30	l	ı	1				1
		1						
	_l	<u> </u>						

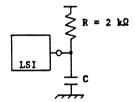


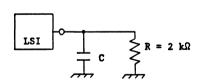


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H8TF-E1 | Sheet 1/1

FUJITSU (	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	1		"UH	B" Version
Cell Name	Function							Number of BC
	Tri-state Output	(IOL=8m	A) with	Noise 1	imit Re	sistanc	e	
H8TFU	& Input Buffer (						- 1	9
Cell Symbol			Prop	agation	Delay Pa	aramete	r	
		t	up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		1.06	0.04	1.84	0.04			X → IN
		3.21	0.056	5.96	0.070			OT → X
	4	(7.97)		(11.91)	)		1	1
IN	<b>-</b> ∕				1 1		1	
IN	$\sim$				1 1		l	
				1	1 1		1	1
ОТ	<b>→</b> x			l			l	
	ΓY			l				1
					1 1			ŀ
	ı			İ	1 1		l	1
	C			ł				l
			$L \rightarrow Z$			$Z \rightarrow L$		
		t0		KCL	t0		CL	_ c → x
		2.6			6.82		070	
		(19.7	1)	*	(12.77	)		1
		1				1		1
			1	į		- 1		1
	Input Loading			1				
Pin Name	Factor (Lu)					1		1
OT	2							_
С	2		H → Z			$Z \rightarrow H$		_
		t0		KCL	t0		CL	4
	<u> </u>	3.3		. 1	3.21		056	1
	Output Driving	(19.7	1)	*	(12.77	)		
Pin Name	Factor (Lu)	1	- 1			ı		1
IN	36	1				- 1		
		1				- 1		
	1	l	ı	1		1		
	I	I	- 1	- 1		1		1

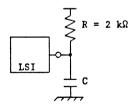


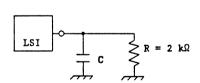


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8TFU-E1 | Sheet 1/1

FULLITSU (	CMOS GATE ARRAY U	NIT CEL	I. SPE	CIFICATIO	<u>,                                      </u>		"UH	B" Version
Cell Name	Function	NII ODD	011	CITIONITO	`		<del>- 1 011</del>	Number of BC
	Tri-state Output	(IOL=8m	A) wi	th Noise	Limit Re	sistanc		
H8TFD	& Input Buffer (						- 1	9
Cell Symbol				opagation			r	
		t	up		tdn			
İ		t0	KCL		KCL	KCL2	CDR2	
		1.06	0.04				l	X → IN
		3.21	0.05				1	OT → X
1		(7.97)		(11.91)	)			1
IN	<b>-</b> < h ∣						1	-
	7						l	
от —	x				j		l	
01	^ ^						l	
							i	1
1							ł	
	c				1	1	ŀ	
1	_				1		İ	
			L -	Z		$Z \rightarrow L$		
		t0		KCL	t0	K	CL	_ c → x
		2.6			6.82	1	070	7
		(19.7	1)	*	(12.77	)		1
l								1
1	Input Loading		1					
Pin Name	Factor (lu)							
OT	2 2		H -			$Z \rightarrow H$		4
С	2	t0	_ <del>_                                  </del>	KCL	t0		CL	-
		3.3	<del>,  </del>	VCT	3.21		056	-
	Output Driving	(19.7	-	*	(12.77		. 0.50	
Pin Name	Factor (lu)	(1).,	-,		(12.//	<b>'</b>		
IN	36		- 1			1		
	1					ļ		
			- 1			- 1		
			- {			- 1		

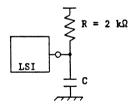


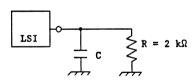


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H8TFD-E1 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPECI	FICATION	1		"UH	B" Version
Cell Name	Function	***************************************						Number of BC
	Tri-state Output	(IOL=8m	A) with	Noise 1	imit Re	sistanc	e	
H8CF	& CMOS Interface	Input						9
Cell Symbol			Prop	agation	Delay P	aramete	r	
		t	up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	
		0.92	0.04	1.33	0.04		l	X → IN
		3.21	0.056	5.96	0.070		1	OT → X
	1	(7.97)		(11.91)			l	
IN —	<b>-</b> < h		İ		1		l	
	<u> </u>		ĺ				l	
			ļ		1			
OT	x ×		İ				l	
	νĭ		İ				Į	Ì
			İ				İ	1
	C		İ	1				
	C		ĺ					Ì
			L + 2	!		$Z \rightarrow L$	1	+
		t0		KCL	t0		CL	$\exists c + x$
		2.6	2		6.82	0	.070	7
		(19.7	1)	*	(12.77	)		
		`	·	1				
		j	1					1
	Input Loading							
Pin Name	Factor (lu)	1		1				
OT		ł						_
	2	<b></b>						
C	2 2		H → Z			$Z \rightarrow H$		4
		t0		KCL	t0	K	CL	
	2	3.3	10	KCL	3.21	0.	CL 056	1
С	2 Output Driving		10			0.		
C Pin Name	Output Driving Factor (£u)	3.3	10	KCL	3.21	0.		
С	2 Output Driving	3.3	10	KCL	3.21	0.		
C Pin Name	Output Driving Factor (£u)	3.3	10	KCL	3.21	0.		

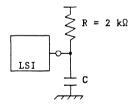


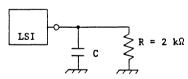


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{\hbox{\scriptsize CL}}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - The parameters in parentheses are the values applied to the simulation.

UHB-H8CF-E1 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CELI	L SPECI	FICATIO	N		"UH	B" Version
Cell Name	Function							Number of BC
	Tri-state Output(	IOL=8mA	) w/ No	ise Lim	it Resis	tance &		
H8CFU	CMOS Interface In	put Buf	fer (Tr	ue) w/ 1	Pull-up	Resista	nce	9
Cell Symbo	l				Delay P			
		tı	up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.92	0.04	1.33				X → IN
		3.21	0.056	5.96			1	OT → X
	4	(7.97)		(11.91	)			
IN —	<b>─</b>	1			1			
214	, \			1				
				}				
ОТ —	- x			1				
	M						l	
					1		l	
	1			l			1	
	С			l	1		l	
				<u> </u>	<u> </u>		<u> </u>	
			$L \rightarrow Z$			$Z \rightarrow L$		
		t0		KCL	t0		CL	c → x
		2.6			6.82		.070	ł
		(19.7	1)	*	(12.77	)		
		1						
		į		j				
<b>.</b>	Input Loading	ĺ						
Pin Name	Factor (lu)	ł	1					
OT	2		<u> </u>	,		$Z \rightarrow H$		-
С	2			KCL	10		CL	-
		10 3.3		VCT	t0 3.21		056	4
	Output Driving	(19.7		*	(12.77		020	
Pin Name	Factor (lu)	(19.7	1		(12.//	<b>,</b>		
IN IN	36	1						
117	] 30	ł				- 1		
		1						1
İ		1						1
		<u> </u>			L			<u></u>

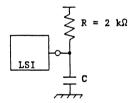


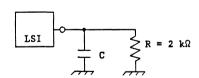


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of  $K_{CL}$  for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the  ${\tt simulation.}$

UHB-H8CFU-E1 | Sheet 1/1

FUJITSU	CMOS GATE ARRAY U	NIT CEL	L SPEC	IFICATION	ĭ		"UHI	B" Version
Cell Name	Function							Number of BC
	Tri-state Output(	IOL=8mA	) w/ No	oise Limi	it Resist	ance &		
H8CFD	CMOS Interface In	put Buf	fer (Tru	ue) w/Pu	111-down	Resist	ance	9
Cell Symbo	1		Pro	pagation	Delay Pa	ramete	r	
		t	up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.92	0.04	1.33	0.04			X → IN
		3.21	0.056	5.96	0.070			OT → X
		(7.97)		(11.91)	ol l			
IN -					1 1			1
IN	$\sim$							
								1
от —	-  > x			1	1 1			1
	L P			į.	1 1			1
					1			1
	1			1	1 1			1
	C			ł	1 1			1
				1	l			
			L + :	Z		$Z \rightarrow L$		
		t0		KCL	t0	K	CL	] c → x
		2.6	2		6.82	0	.070	
		(19.7	1)	**	(12.77)	1		1
				1		ļ		
		]	1					
	Input Loading		1			1		1
Pin Name	Factor (lu)							
OT	2	l						
С	2		Η →	Z		$Z \rightarrow H$		
		t0		KCL	t0		CL	
		3.3			3.21		056	
	Output Driving	(19.7	1)	*	(12.77)			
Pin Name	Factor (lu)	]	1			1		
IN	36	}	1			- 1		
		1	- 1			1		
		1	-					
	1	1				- 1		l





- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

UHB-H8CFD-E1 | Sheet 1/1

FILITSII C	MOS GATE ARRAY U	NIT CEL	I. SPECT	FICATIO	N		w <sub>III</sub>	HB" Version
	Function	···· ODD	D DILUI	10/1110			<del>- ' ''</del>	Number of BC
							+	
IT10	Input Buffer for	Oscill	ator Ci	rcuit			!	0
Cell Symbol			Prop	agation	Delay	Paramet	er	
			up		td	n		
		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0	0	0	0			X + IN
								1
							l	1
							İ	
							<b>{</b>	
							1	]
r	_						Ì	
х —	IN						1	
ı							ļ	
							1	
							1	
						L	٠.,	<del></del>
		Parame	ter			-   - '	Symbol	Typ(ns)*
						ı		
						İ		
						į		
						- 1		
	Input Loading							
Pin Name	Factor (lu)					- 1		
	1							1
						- 1		
	Output Driving					- 1		
Pin Name	Factor (lu)					1		
	1							
								ing condition.
								ng condition
· ·	<u></u>	are	given b	y the n	naximum	delay	multip	lier.

This cell if for the oscillator circuit only. Please refer to the document Fujitsu CMOS Gate Array 'UHB' Version User's Manual for I/O Cell for Oscillator Circuit GATI0281 $\Delta$  for the details.

UHB-IT10-E1 | Sheet 1/1

	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATION			"UHB	" Version
	Function						N	umber of BC
	Output Buffer fo	r Oscil	lator					
	with CMOS Interf			er				8
Cell Symbol			Prop	agation	Delay P	aramete		
Jerr Bymbor		+	up	Legacion	tdn			I
1							CDDO	D-Ab
1		t0	KCL	t0	KCL	KCL2	CDR2	Path
		0.92	0.04	1.33	0.04		İ	X → IN
1				l			l	l
ł				l				
							1	
				1	ĺ		İ	İ
ł	$\overline{}$			i				
IN	<b>-</b> < h		}		]			
١ ،	\ 7			1		ŀ		
			ļ			1		
OT	>> <b>→</b> x		l			1		
			]				1	
						1		1
1		l		1		1	1	1
1		Parame	ter			Sv	mbol	Typ(ns)*
1								<b>1</b>
						1		1
						- 1		
1		}						1
1						1		
		<b>!</b>				ļ		
	Input Loading					1		ļ
Pin Name	Factor (lu)							
		1						
	l					İ		
	i	İ				ı		
						- 1		
	Output Driving							İ
Pin Name	Factor (lu)	İ						
IN	36	1				1		
	1							
		* Mini	miim 1701	lues for	the tyr	sical or	oratir	ng condition.
		The		for the	une typ	rear of	octabli	is condition.
		Ine	values	for the	worst C	ase ope	rating	condition
	<u> </u>	are	given l	by the ma	ximum c	ielay mu	utipli	Ler.
This cell:	is for the oscill	ator ci	ircuit o	only. Pl	lease re	efer to	the do	ocument
"Fujitsu Cl	MOS Gate Array 'U ATI0281Δ)" for th	JHB' Ver	sion Us	ser's Mar	nual for	: I/O Ce	ell for	c Oscillator
Circuit (G	ATI0281A)" for th	e detai	ils.			•		
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UHB-HOC-E1 | Sheet 1/1

	MOS GATE ARRAY U	NIT CEL	L SPECI	FICATION			"UI	HB" Version
Cell Name	Function							Number of BC
	Output Buffer fo	r Oscil	lator					
HOS	with Schmitt Tri	gger In					l	8
Cell Symbol				agation	Delay P	aramete	r	
		t	up		tdn			
		t0	KCL	t0	KCL	KCL2	CDR	2 Path
		2.48	0.16	3.08	0.10			X → IN
							}	
IN	<i></i> ⟨ <i>I</i>   <sub>1</sub>							
	$\backslash \mathcal{A}$							
			]				ŀ	
OT TO	>>→ x							
l								
		Parame	ter			Sy	mbol	Typ(ns)*
								1
	Input Loading							
Pin Name	Factor (lu)							
						1		1
								ł
	Output Driving							1
Pin Name	Factor (lu)	ļ						
IN	18							
								ing condition.
		The values for the worst case operating condition						
	are given by the maximum delay multiplier.							

This cell is for the oscillator circuit only. Please refer to the document "Fujitsu CMOS Gate Array 'UHB' Version User's Manual for I/O Cell for Oscillator Circuit (GATI0281 $\Delta$ )" for the details.

UHB-HOS-E1 | Sheet 1/1

FUJITSU	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "UHB" Version								
Cell Name	Function	Number of BC							
	Output Buffer fo	r Oscil	lator						
HOCR	w/ CMOS Interfac	e Input	Buffer	w/ Feed	back Re	sistan	ce	8	
Cell Symbol			Prop	agation	Delay P	aramet	er		
	······································	t	up		tdn			T	
		t0	KCL	t0	KCL	KCL2	CDR	2 Path	
		0.92	0.04	1.33	0.04			X → IN	
							İ		
							1	1	
IN									
IN	$\sim$								
от	→ ×			•	l				
				i				l i	
						1			
			L		<u> </u>	L			
		Parame	ter			S	ymbol	Typ(ns)*	
								1	
						i			
	T + . +								
<b>.</b>	Input Loading					1			
Pin Name	Factor (lu)					1			
						- 1			
	}							)	
	1					- 1			
	Output Driving					- 1			
Pin Name	Factor (lu)								
IN	36								
•	1		_	_	_				
		" Mini	mum val	ues for	the typ	oical c	perat	ing condition.	
								ng condition	
ļ		are	given b	y the ma	ximum c	ielay n	nultip	lier.	
The second second	4 - F			1 7.1				4	
Inis cell	is for the oscill	ator ci	rcuit	oniy. Pi	lease re	erer to	tne	document	
rujitsu (	CMOS Gate Array 'U GATI0281A)" for th	ns ver	sion Us	ser s mar	lual for	: 1/0 (	ell i	or Uscillator	
Circuit (	$5AT10281\Delta$ )" for the	e detai	ıls.						
1									
1									

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UHB-HOCR-E1 | Sheet 1/1

## 2

## **Appendix A: General AC Specifications**

Simulation Delay Specifications (Recommended Operating Conditions, Ta = 0 to 70°C,  $V_{DD}$  = 5  $V_{\pm}5\%$ 

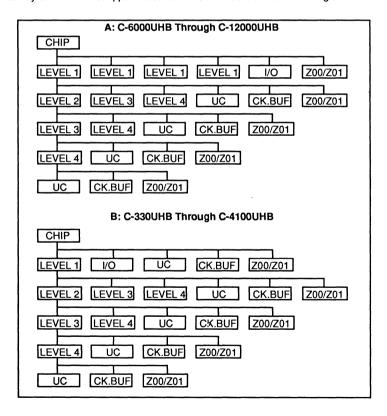
Delay Multipliers	Min.	Max.
Pre-layout Simulation	0.35	1.65
Post-layout Simulation	0.40	1.60

# **Appendix B: Hierarchical Structure**

Hierarchical blocks (or Functional Logic Blocks) within other hierarchical blocks are user-defined groups of cells laid out in close proximity to each other in both X and Y dimensions of the array.

The hierarchical method of design allows circuit sections to be placed within the array at positions relative to each other. This is made possible by the designer's defining and placing functional logic blocks within the hierarchy and thus controlling path lengths.

There are five levels of hierarchy, also referred to as Functional Logic Blocks (FLBs). Certain design rules regarding what may and what must appear at certain levels are condensed in the diagram below.



Use of the hierarchical design method is mandatory for partitioned arrays and optional for non-partitioned arrays. Section A of the figure above addresses partitioned arrays C-6000UHB through C-12000UHB. Section B of the figure above addresses non-partitioned arrays C330UHB through C4100UHB. Immediately below the chip level, four Level 1 (FLB1) blocks must be defined, giving identity to each of the four partitioned quadrants of the array.

# Appendix B: Hierarchical Structure (Continued)

All I/O buffers and their associated circuitry must be defined immediately beneath the chip level with the FLB1 blocks. Nothing but I/O buffers may be so defined. If pull-up or pull-down cells (A01s or X00s) are required for unused inputs of the I/O buffers, they must also be defined at this level. Unit cells (UC) may be defined at each level.

For optimum delay characteristics, Level 2 blocks should be defined under each of the Level 1 blocks, Level 3 Blocks under Level 2 blocks, and so on. Unit cells should be defined under Level 4.

# **Appendix C: Estimation Tables for Metal Loading**

## C-330UHB

NDI	CL(lu)	NDI	CL(lu)
1 2 3 4	1.0 2.2 3.0 3.5	10 11 12 13	5.0 5.0 5.1 5.2
5 6 7 8 9	3.9 4.2 4.6 4.8 4.9	14 15 16–30 31–50	5.3 5.7 6.6
9	4.9	51–75 76–100	6.7 7.4

## C-530UHB

NDI	CL(lu)	NDI	CL(lu)
1	1.1	10	5.6
2	2.5	11	5.6
2	3.4	12	5.7
4 5 6	3.9	13	5.8
5	4.4	14	5.9
	4.7	15	5.9
7	5.1	16–30	6.4
8	5.4	31-50	7.4
9	5.5	51-75	7.5
	l	76-100	8.3

## C-830UHB

NDI	CL(lu)	NDI	CL(lu)
1 2	1.3 3.0 4.0	10 11 12	6.7 6.7 6.8
2 3 4 5	4.7 5.2	13 14	6.9 7.1
6 7	5.6 6.1	15 16–30	7.1 7.7
8 9	6.4 6.6	31–50 51–75 76–100	8.8 9.0 9.9

## C-1200UHB

NDI	CL(lu)	NDI	CL(lu)
1	1.7	10	8.2
2	3.6	11	8.2
3	4.9	12	8.3
4	5.7	13	8.4
5	6.3	14	8.6
6	6.8	15	8.6
7	7.4	16–30	9.3
8	7.8	31–50	10.6
9	8.0	51-75	10.9
		76-100	12.0

# C-1700UHB

NDI	CL(lu)	NDI	CL(lu)
1	1.8	10	8.8
2	3.9	11	8.8
3	5.3	12	9.0
4	6.2	13	9.1
5	6.8	14	9.3
6	7.4	15	9.3
7	8.1	16–30	10.1
8	8.4	31–50	11.5
9	8.6	51-75	11.8
		76–100	13.0

# Appendix C: Estimation Tables for Metal Loading 4 (Continued)

## C-2200UHB

NDI	CL (lu)	NDI	CL (lu)
1	2.2	10	10.7
2	4.7	11	10.7
3	6.4	12	10.8
4 5	7.4	13	10.9
	8.2	14	11.2
6	8.9	15	11.2
7	9.7	16–30	12.1
8	10.1	31–50	13.9
9	10.4	51-75	14.3
		76–100	15.7

## C-3000UHB

NDI	CL (lu)	NDI	CL (lu)
1	2.6	10	12.9
2	5.7	11	12.9
2	7.7	12	13.1
4	9.0	13	13.2
4 5	10.0	14	13.6
6	10.8	15	13.6
7	11.8	16–30	14.7
8	12.3	31-50	16.8
9	12.6	51-75	17.3
		76–100	19.0

## C-4100UHB

NDI	CL (lu)	NDI	CL (lu)
1	3.0	10	14.8
2	6.6	11	14.8
2	8.8	12	15.0
4	10.3	13	15.2
5	11.4	14	15.5
6	12.4	15	15.5
7	13.5	16–30	16.8
8	14.0	31–50	19.3
9	14.4	51-75	19.8
		76–100	21.8

# C-6000UHB (Within Block)

NDI	CL (lu)	NDI	CL (lu)
1 2 3 4 5 6 7 8	1.6 3.5 4.7 5.5 6.1 6.6 7.2 7.5 7.7	10 11 12 13 14 15 16–30 31–50 51–75	7.9 7.9 8.0 8.2 8.4 8.4 9.1 10.4 10.6
		76–100	11.7

## C-6000UHB (Inter-Block)

NDI	CL (lu)	NDI	CL (lu)
1	3.5	10	17.2
2	7.6	11	17.2
3	10.2	12	17.4
4	12.0	13	17.6
5	13.3	14	18.1
6	14.4	15	18.1
7	15.7	16–30	19.6
8	16.3	31–50	22.4
9	16.8	51–75	23.0
		76–100	25.3

Inter-Block tables must be applied to a net which has an inter-block connection. If a net, for example, has 3 NDI in a block and 1 NDI in a different block, NDI = 4 of the Inter-Block table must be applied.

# **Appendix C: Estimation Tables for Metal Loading (Continued)**

# C-8700UHB (Within Block)

NDI	CL(lu)	NDI	CL(lu)
1 2 3 4 5 6	2.2 4.7 6.4 7.4 8.2 8.9 9.7	10 11 12 13 14 15 16–30	10.7 10.7 10.8 10.9 11.2 11.2
8 9	10.1 10.4	31–50 51–75 76–100	13.9 14.3 15.7

#### C-8700UHB (Inter-Block)

			,
NDI	CL(lu)	NDI	CL(lu)
1	4.2	10	20.8
2	9.2	11	20.8
3	12.4	12	21.0
4	14.5	13	21.3
5	16.0	14	21.8
6	17.3	15	21.8
7	18.9	16–30	23.6
8	19.7	31–50	27.1
9	20.2	51-75	27.8
		76–100	30.5

## C-12000UHB (Within Block)

NDI	CL(lu)	NDI	CL(lu)
1	2.6	10	12.9
2	5.7	11	12.9
3	7.7	12	13.1
4	9.0	13	13.2
5	10.0	14	13.6
6	10.8	15	13.6
7	11.8	16–30	14.7
8	12.3	31–50	16.8
9	12.6	51–75	17.3
		76–100	19.0

# C-12000UHB (Inter-Block)

NDI	CL(lu)	NDI	CL(lu)
1	4.9	10	24.3
2	10.8	11	24.3
3	14.5	12	24.6
4	17.0	13	25.0
5	18.8	14	25.6
6	20.3	15	25.6
7	22.2	16–30	27.7
8	23.1	31–50	31.7
9	23.7	51–75	32.6
		76–100	35.8

Inter-Block tables must be applied to a net which has an inter-block connection. If a net, for example, has 3 NDI in a block and 1 NDI in a different block, NDI = 4 of the Inter-Block table must be applied.

# 2

# **Appendix C: Estimation Tables for Metal Loading for Clock Nets**

## C-330UHB (for CK20, CK40)

NDI	CL (lu)	NDI	CL (lu)
1-2	5.1	11 – 12	12.7
3 – 4	9.5	13 – 15	13.0
5-6	11.9	16 – 30	13.3
7-8	12.2	31 – 50	15.4
9 – 10	12.4	51 - 80	18.1

# C-330UHB (for CK60, CK80)

NDI	CL (lu)		NDI	CL (lu)
1-2	7.0		11 – 12	17.6
3 – 4	13.4		13 – 15	17.9
5-6	16.7		16 – 30	18.1
7-8	17.0		31 – 50	20.2
9 – 10	17.3	П	51 – 80	23.0

## C-530UHB (for CK20, CK40)

NDI	CL (lu)	NDI	CL (lu)
1-2	5.1	11 - 1	
5-6	9.6 14.1	13 – 1 16 – 3	
7 – 8 9 – 10	14.4 14.6	31 – 5 51 – 8	

## C-530UHB (for CK60, CK80)

NDI	CL (lu)	NDI	CL (lu)
1 – 2 3 – 4	7.3 14.0	11 – 12 13 – 15	21.4 21.7
5 – 6	20.7	16 – 30	21.9
7 – 8 9 – 10	20.9 21.2	31 – 50 51 – 80	23.8 26.4

# C-830UHB (for CK20, CK40)

NDI	CL (lu)		NDI	CL (lu)
1-2	5.6		11 – 12	18.5
3-4	10.5		13 – 15	18.8
5-6	15.4		16 – 30	19.1
7-8	18.0		31 – 50	21.2
9 – 10	18.2	l	51 – 80	24.1

# C-830UHB (for CK60, CK80)

NDI CL((Iu)) NDI CL (IL	1)
1 - 2 8.1 11 - 12 27.3 3 - 4 15.5 13 - 15 27.6 5 - 6 22.9 16 - 30 27.8 7 - 8 26.7 31 - 50 30.0 9 - 10 27.0 51 - 80 32.8	

# C-1200UHB (for CK20, CK40)

NDI	CL (lu)	NDI	CL (lu)
1-2	6.2	11 - 12	2 23.3
3-4	11.7	13 – 1	5 23.7
5-6	17.2	16 - 3	0 24.0
7-8	22.7	31 - 5	0 26.3
9 – 10	23.0	51 - 8	0 29.3

# C-1200UHB (for CK60, CK80)

NDI	CL (lu)	NDI	CL (lu)
1-2 3-4 5-6 7-8 9-10	9.3 18.0 26.7 35.4 35.7	11 - 12 13 - 15 16 - 30 31 - 50 51 - 80	36.0 36.3 36.6 38.9 41.9
9 – 10	35.7	51 - 80	41.9

# **Estimation Tables for Metal Loading for Clock Nets** (Continued)

# C-1700UHB (for CK20, CK40)

NDI	CL(lu)	NDI	CL(lu)
1-2	6.6	11 – 12	28.0
3-4	12.6	13 – 15	28.3
5-6	18.6	16 – 30	28.6
7-8	24.5	31 – 50	31.0
9 – 10	27.7	51 - 80	34.2

# C-1700UHB (for CK60, CK80)

NDI	CL(lu)	NDI	CL(lu)
1-2 3-4 5-6	10.3 19.9 29.5	11 - 12 13 - 15 16 - 30	44.4 44.7 45.0
7-8	39.1 44.1	31 – 50	47.4 50.6

# C-2200UHB (for CK20, CK40)

NDI	CL(lu)		NDI	CL(lu)
1-2	7.1		11 – 12	33.1
3-4	13.5		13 – 15	33.4
5-6	19.9	li	16 – 30	33.8
7-8	26.3		31 – 50	36.3
9 – 10	32.8	H	51 – 80	39.6

# C-2200UHB (for CK60, CK80)

NDI	CL(lu)		NDI	CL(lu)
1-2 3-4 5-6	11.2 21.8 32.3		11 - 12 13 - 15 16 - 30	53.7 54.1 54.4
7-8	42.8	ı	31 – 50	56.9
9 – 10	53.4	ı	l 51 – 80 l	60.2

## C-3000UHB (for CK20, CK40)

NDI	CL(lu)	NDI	CL(lu)
1-2	7.7 14.8	11 – 12 13 – 15	43.0 43.3
5-6 7-8	21.8 28.9	16 – 30 31 – 50	43.7 46.3
9 – 10	35.9	51 – 80	49.8

## C-3000UHB (for CK60, CK80)

NDI	CL(lu)	NDI	CL(lu)
1-2	12.6	11 - 12	72.1
3-4	24.5	13 – 15	72.4
5-6	36.4	16 – 30	72.8
7 – 8	48.3	31 – 50	75.4
9 – 10	60.2	51 – 80	78.9

# C-4100UHB (for CK20, CK40)

NDI	CL(lu)	NDI	CL(lu)
1-2	8.4	11 - 12	47.3
3-4	16.2	13 - 15	51.4
5-6	24.0	16 - 30	51.7
7-8	31.7	31 - 50	54.6
9-10	39.5	51 - 80	58.4

# C-4100UHB (for CK60, CK80)

NDI	CL(lu)	NDI	CL(lu)
1-2 3-4 5-6 7-8	14.0 27.4 40.7 54.1	 11 - 12 13 - 15 16 - 30 31 - 50	80.8 87.6 88.0 90.9
9 – 10	67.4	51 - 80	94.6

# 2

# Estimation Tables for Metal Loading for Clock Nets (Continued)

# C-6000UHB (for CK20, CK40)

NDI	CL(lu)
1	9.9
2	14.9
3	24.1
4	29.2

# C-6000UHB (for CK60, CK80)

NDI	CL(lu)
1	13.2
2	24.8
3	37.3
4	48.9

# C-8700UHB (for CK20, CK40)

NDI	CL(lu)
1	11.8
2	17.8
3	28.9
4	34.9

# C-8700UHB (for CK60, CK80)

NDI	CL(lu)
1	15.7
2	29.7
3	44.8
4	58.7

# C-12000UHB (for CK20, CK40)

NDI	CL(lu)
1	13.7
2	20.7
3	33.7
4	40.8

# C-12000UHB (for CK60, CK80)

NDI	CL(lu)
1 2 3 4	18.3 34.7 52.3 68.7

# **Appendix D: Available Package Types**

# UHB CMOS Available Package Types Plastic

	C-330 UHB	C-530 UHB	C-830 UHB	C-1200 UHB	C-1700 UHB	C-2200 UHB	C-3000 UHB	C-4100 UHB	C-6000 UHB	C-8700 UHB	C-12000 UHB
DIP											
Standard	(100 mil p	in pitch)							***************************************		
16 DIP	•					_	-	_	_	_	_
18 DIP	СН		_				_				
20 DIP	•	•	•	_			***************************************			_	_
22 DIP 24 DIP	•	:		•	:	-	•				-
28 DIP		•						•	_	_	
40 DIP	•					•			•	СН	_
40 DIP 42 DIP						•		•		CH	_
48 DIP				•	•	•	•	•	•	CH	
l	(70 11 1	•	•		•	•	•	•	•	On	
Shrink	(70 mil pi	n pitch)	_	_	_						
28 SHDIP	•	•	•	•	•	_	_	•	-		
42 SHDIP 48 SHDIP	•	•	•	•	•			•		_	
64 SHDIP	•	•					•	•		CH	
ŀ			. •	•	•	•	•	•	•	CH	
Skinny	(300 mil w	-	)								
22 SKDIP 24 SKDIP	сн	СH	_	_	_	_	_		_		_
28 SKDIP	ŇŴ	ŇŴ	_			_	-	_	_		
FPT											
	(leads on	two sides)									
16 FPT	•	CH	CH	CH							
20 FPT	•	CH	CH	CH		_	_				
24 FPT	•	•	•	•				-			
28 FPT	•	•	•	•		_					_
	(leads on a	all four sid	es)								
44 FPT	•	•	•	•	•		_				
48 FPT	•	•	•	•	•	•	•			_	_
48 FPT-S*	•	•	•	•	•				-	-	
64 FPT	•	•	•	•	•	•	•	•	•	CH	_
80 FPT		•	•	•	•	•	•	•	•		
100 FPT		_	•	•	•	•	•	•	•		
120 FPT			_	•	•	•	•	•	•	•	_
160 FPT							•	•	•	•	-
	*smaller th	nan the oth	ner 48p	in FPT							
PLCC											
28 PLCC	•	•	•	•	•	•	•				_
44 PLCC	•	•	•	•	•	•	•	СН	CH		_
68 PLCC	•	•	•	•	•	•	•	•	•	CH	CH
84 PLCC					•	•	•	•	•	СН	СН
PPGA											
	100 mil pi	in pitch)							***************************************		
64 PGA	•	•	•	•	•	•	•	•	•	•	_
88 PGA		•	•	•	•	•	•	•	•	•	
135 PGA	_		-			_	•	•	•	•	_

# NOTES:

: Available
 : Not Available
 UD : Under Development
 NW : Newly Available

Newly Available
 The availability of the package has changed, i.e., become unavailable

# Appendix D: Available Package Types (Continued)

# UHB CMOS Available Package Types Ceramic

	C-330 UHB	C-530 UHB	C-830 UHB	C-1200 UHB	C-1700 UHB	C-2200 UHB	C-3000 UHB	C-4100 UHB	C-6000 UHB	C-8700 UHB	C-1200 UHB
DIP											
Standard	(100 mil p	in pitch)									
20 DIP	•					_					_
22 DIP	•	•	•		_	_	_			-	_
24 DIP	•	•	•	•		•					_
28 DIP	•	•	•	•	•	•		_			_
40 DIP	•	•	•	•	•	•				_	_
42 DIP	_	-	_	•	•		•	_		_	_
48 DIP			•	•	•	•	•				
Shrink	(70 mil pir	pitch)									
28 SHDIP	•	•	•			-					
42 SHDIP		_	-	•	•	•	_	_			_
FPT											
	(leads on a	all four sid	es)								
48 FPT	_		•	•	•	•	_				_
80 FPT	_	_						_	-	UD	_
100 FPT		_		_	•	•		_	_	UD	_
120 FPT	_	_	_		_		_	•	•	•	UD
160 FPT	_			_					_	_	CH
LCC											
28 LCC	•	•	•	•	_	_				_	
48 LCC	•	•	•	•	•	•	•	•			
64 LCC	•	•	•	•	•	•	•	•	•	•	CH
68 LCC		•	•	•	•	•	•	•	•	•	CH
84 LCC											CH
PGA											
	100 mil pi										
64 PGA	•	•	•	•	•	•	•	•	•	•	•
88 PGA		СН	•	•	•	•	•	•	•	•	UD
135 PGA			_	•	•	•	•	•	•	•	•
179 PGA		_	_				NW	NW	NW	•	•
208 PGA					-	_	•	NW	NW	NW	NW
256 PGA		_			-					•	•
NOTES:											
	/ailable										
	ot Available										
	nder Developi										
	wly Available			been char							

# **Appendix E: TTL 7400 Function Conversion Table**

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
7400	Quad 2-input NAND	4 x N2N	4
7401	Quad 2-input NAND, Open Collector Outputs	T24 multiplexer	6
7402	Quad 2-input NOR	4 x R2N	4
7403	Quad 2-input NAND, Open Collector Outputs	T24 multiplexer	6
7404	Hex Inverter	6 x VIN	6
7405	Hex Inverter, Open Collector Outputs	R6B	5
7406	Hex Inverter/Buffer, Open Collector Outputs	R6B	5
7407	Hex Buffer, Open Collector Outputs	2 x N3N into R2N	5
7408	Quad 2-input AND	4 x N2P	8
7409	Quad 2-input AND, Open Collector Outputs	N8P	6
7410	Triple 3-input NAND	3 x N3N	6
7411	Triple 3-input AND	3 x N3P	9
7412	Triple 3-NAND, Open Collector Outputs	T33	7
7413	Dual 4-input NAND, Schmitt Trigger	2 x (4 x I2R to N4N)	68
7414	Hex Schmitt Trigger Inverter	6 x I1R	48
7415	Triple 3-input AND, Open Collector Outputs	N8P to N2P	8
7418	Dual 4-input NAND, Schmitt Trigger	2 x (4 x I2R to N4N)	68
<b>'</b> 419	Hex Schmitt Trigger Inverter	6 x l1R	48
7420	Dual 4-input NAND	2 x N4N	4
421	Dual 4-input AND	2 x N4P	6
7422	Dual 4-input NAND, Open Collector Outputs	2 x N4N + N2P	6
7423	Expanded Dual 4-input NOR with Strobe	R4P to D23 + R4P to R2N	9
424	Quad Schmitt Trigger 2-input NAND	8 x I2R + 4 x N2N	68
425	Dual 4-input NOR with Strobe	2 x (R4P + R2N)	8
426	Quad 2-input NAND, High Voltage Output	4 x N2N	4
427	Triple 3-input NOR	3 x R3N	6
7428	Quad 2-input NOR Buffer	4 x R2N	4
7430	8-input NAND	N8B	6
7432	Quad 2-input OR	4 x R2P	8
7433	Quad 2-input NOR Buffer, Open Collector		•
100	Outputs	4 x R2N + N4P	7
434	Hex Noninverter	6 x B1N	6
7435	Hex Noninverter with Open Collector Outputs	2 x N3N into R2N	5
7437	Quad 2-input NAND Buffer	4 x N2B	12
438/9	Quad 2-input NAND Buffer, Open Collector	4 X 142D	12
430/3	Outputs	4 x N2N + N4P	7
7440	Dual 4-input NAND Buffer	2 x N4B (N4N if not power)	8(4
440	BCD to Decimal Decoder		
442	EX3 to Decimal Decoder	4 x V2B + 10 x N4N	24
443 444		4 x V2B + 10 x N4N	24
444	4 to 10 Line Decoder	4 x V2B + 10 x N4N	24
	BCD to Decimal Decoder/driver (30V)	4 x V2B + 10 x N4N	24
446	BCD to 7-segment Decoder/Driver (30V)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
447	BCD to 7-segment Decoder/Driver (15V)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
448	BCD to 7-segment Decoder/Driver	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
449	BCD to 7-segment, Open Collector Outputs	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
450	Dual 2-input, 2-wide AOI (One Expandable)	D36 + D24	5
451	AOI	2 x D24	4
452	Expandable 4-wide AND-OR	N3N + D36 + V1N into N3N	8
453	Expandable 4-wide AOI	D36 + D23 into N2P	7
7454	4-wide AOI	2 x N3N + 2 x N2N + N4N + V1N	9
455	2-wide 4-input AOI	T42	6
460	Dual 4-input Expander	2 x N4P	6
7461	Triple 3-input Expander	3 x N3P	6
462	4-wide AND-OR Expander	2 x N3N + 2 x N2N + N4N	8
7464	4-2-3-2 AOI	T54	10
101			

# TTL 7400 Function Conversion Table (Continued)

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
7470	AND-gated positive-edge JK FF with Preset		
. 4. 0	and Clear	3 x V1N + 2 x N3N + N2N + R2N + FJD	21
	or:	FD4 + 2 x N2N + R2N + V1N + R2P + D24	17
7471	AND-gated RS M/S FF with Preset	TOTAL ATTENDED	
	and Clear	FD4 + 2 x N3N + 2 x D23 + 2 x V1N	19
	or:	LT1+ 2 x N4N + N2P	10
7472	AND-gated JK M/S FF with Preset		
	and Clear	V1N + 2 x N3N + N2N + R2N + FJD	19
	or:	FD4 + N3P + N3N + V1N + D24	17
7473	Dual JK FF with Clear	2 x FJD	24
7474	Dual positive-edge D-FF with Preset and		
	Clear	2 x FDP	16
7475	4-bit Bistable Latch	LTM	16
7476	Dual JK FF with Preset and Clear	2 x (FJD + N2N + R2N + V1N)	30
7477	4-bit Bistable Latch	LTM	16
7478	Dual JK FF with Preset and Common	2 x (FJD + N2N + R2N + V1N)	30
	Clear and Clock	,	
7480	Gated Full Adder	A1N	8
7482	2-bit Binary Full Adder	A2N	16
7483	4-bit Binary Full Adder with Fast Carry	A4H	48
7484	4-bit Magnitude Comparator	MC4	42
7486	Quad 2-input XOR	4 x X2N	12
7487	4-bit True/Complement Zero/One Element	4 x N2N + V1N + 4 x N2N	17
7489	64-bit (16 x 4) Memory	2 x DE6 + V1N + 16 x LT4	298
		+ 5 x (V2B + T5A) + 10 x V2B	
7490	Decade Counter	2 x (FDP + FDO + N2P + N2N + R2N) + V1N	39
	(Different Implementation)	4 x N2P + 2 x R2P + N2N + C41 + LT1	41
7491	8-bit Shift Register	2 x FDS + V1N	41
7492	Divide-by-12 Counter	4 x FDO + 2 x V1N + 2 x R2N + N2N	33
7493	4-bit Binary Counter	C41 + N2N (for the resets)	25
7494	4-bit Shift Register, 2 asynchronous Presets	FS3	34
	4-bit Shift Register, 2 asynchronous		
	Presets, Full Implementation	4 x FDP + 4 x D24 + 2 x V1N	42
7495	4-bit Parallel-access Shift Register	FS2 + D24 + 2 x V1N	34
7496	5-bit Shift Register	5 x FDP + 5 x N2N + V1N(clock)	46
7497	Synch 6-bit Binary Rate Multiplier	FDR + 2 x FDO + 3 x V1N + 2 x N2N	122
		+ 2 x N3N + 2 x N4N + 5 x N6B + 3 x N8B	
		+ R2B + X2N + 5 x X1B.	
7498	4-bit Data Selector/Storage Register	FDQ + T2F + 4 x V1N	33
7499	4-bit Universal Shift Register	FS2 + LTK + 2 x D24 + 4 x V1N	42
74100	8-bit Bistable Latch	2 x YL4 + 2 x V1N	30
74101	AO-gated JK Negative-Edge FF,		
	with Preset	FD3 + V1N + 3 x D24	15
74102	AND-gated JK Negative-Edge FF with		
	Preset and Clear	FD4 + D24 + N3P + N3N	16
74103	Dual JK FF with Clear	2 x FJD + 2 x V1N (for clock)	26
	or:	2 x (FD5 + D24 + V1N)	22
74106	Dual JK Negative-Edge FF with Preset		
	and Clear	2 x (FD4 + D24 + V1N)	24
74107	Dual JK FF with Clear	2 x (FJD + 2 x V1N)	22
74108	Dual JK Negative-Edge FF with Preset		_
	and Common Clear and Clock	2 x (FD4 + D24 + V1N)	24
74109	Dual JK Positive-Edge FF with Preset and		
	Clear	2 x (FDP + V1N + D24)	22
74110	AND-gated JK M/S FF with Data		
	Lockout	FDP + D24 + N3P + N3N	15
74111	Dual JK M/S FF with Data Lockout	2 x (FDP + D24 + V1N)	22
74112	Dual JK Negative-Edge FF with Preset		
ı	and Clear	2 x (FD4 + D24 + V1N)	24

# TTL 7400 Function Conversion Table (Continued)

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
74113 74114	Dual JK Negative-Edge FF with Preset Dual JK Negative-Edge FF with Preset and	2 x (FD3 + D24 + V1N)	22
, -111-	Common Clear and Clock	2 x (FD4 + D24 + V1N)	24
74116	Dual 4-bit Latch with Clear	2 x LTM	32
74120	Dual Pulse Synchronizer/Driver	2 x (N2P + LT1 + 4 x N3N + 2 x N2N + 2 x V1N)	36
74125	Quad Bus Buffer with 3-state Output	B41	9
74126	Quad Bus Buffer with 3-state Output	B41 + 4 x V1N	13
74132	Quad 2-input NAND Schmitt Trigger	4 x (2 x I2R + N2N)	68
74133	13-input NAND	2 x N4N + N3N + N2N into R4P	10
74134	12-input NAND with 3-state Outputs	NCB + O4R	15
74135	Quad 3-input EXOR/EXNOR	4 x X4N	20
74136	Quad 2-input EXOR with Open-Collector	4 X A4IN	20
4100	Outputs	4 x X2N + R4N	14
74137	3-line to 8-line Decoder with Address	7.75.7	
	Latch	3 x LTK into DE6	42
74138	3-line to 8-line Decoder with Enable	DE6	30
74139	Dual 2-line to 4-line Decoder	2 x DE4	16
74141	BCD-to-Decimal Decoder	4 x V2B + 10 x N4N	24
74145	BCD-to-decimal Decoder	4 x V1N + 10 x N4N	24
74147	10-line to 4-line BCD Priority Encoder	3 x N4N + 3 x N3N + 2 x N2N + 2 x N2P	36
, 4, 4,	10 mile to 4 mile Bob i Horry Erroder	+ 3 x R2N + R4N + 13 x V1N	00
74148	8-line to 3-line Octal Priority Encoder	N9B + 2 x N2N + R2P + R4N + 4 x N3N	40
74140	6-line to 5-line Octai Phonty Encoder	+ 2 x N4N + G44 + 12 x V1N	40
74450	4 As 4C Mahislanan		
74150	1-to-16 Multiplexer	DE3 + 2 x U28 + D24 + 2 x V1N	41
74151	1-to-8 Multiplexer with Strobe	DE3 + U28 + N2N + V1N	28
74152	1-to-8 Multiplexers	DE3 + U28	26
74153	Dual 4-line to 1-line Selector/Multiplexer	DE2 + 2 x U24 + 2 x R2N	19
74154	4-line to 16-line Decoder/Demultiplexer	2 x DE6 + V1N	61
	or:	2 x DE4 + N2P + 16 x R2P	50
74155	Dual 2-line to 4-line Decoder/Demultiplexer (Totem Pole)	8 x N3N + 2 x R2N + 5 x V1N	23
74156	Dual 2-line to 4-line Decoder/Demultiplexer		
	(Open Collector)	8 x N3N + 2 x R2N + 5 x V1N	23
74157	Quad 2-line to 1-line multiplexer	T2F + 4 x R2N + B1N	13
74158	Quad 2-line to 1-line multiplexer		
	(Inverter Data Outputs)	4 x D24 + V1N + 2 x R2N	11
74159	4-line to 16-line Demultiplexer	2 x DE6 + V1N (without open collector)	50
74160	Synchronous 4-bit Counter	4 x C11 + K1B + 2 x V2B + V1N + B1N+	62
	(Decimal with Direct Clear)	N2K + 2 x R3N + R4N + 3 x R2N + N2N	
74161	Synchronous 4-bit Counter (Binary		
	with Direct Clear)	C43	48
74162	Synchronous 4-bit Counter		
	(Decimal with Synchronous Clear)	C45 + D36 + N3P + 2 x R2N + B1N	57
74163	Synchronous 4-bit Counter (Binary	and the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of the state of t	3,
	with Synchronous Clear)	C45	48
74164	8-bit Parallel Output Serial Shift		+0
110-1	Register, Asynchronous Clear	2 x FDR + N2P	54
74165	8-bit Shift Register	2 x FDS + 8 x D24 + 11 x V1N + K4B + R2P	71
74165 74166	8-bit Shift Register	2 x FDS + 8 x D24 + 11 x V IN + K4B + H2P 2 x FDR + 8 x D24 + 10 x V1N + K4B	/ 1 80
		6 X FUR + 0 X U24 + 1U X V IN + N4B	80
74168	4-bit Up/Down Synchronous Counter	A Odd A Too T NION O NION DON	
	(Decade)	4 x C11 + 4 x T32 + 7 x N2N + 2 x N3N + R2N	85
74400	4 his Ha/Danna Ornacha C	+ 7 x V2B + K1B	
74169	4-bit Up/Down Synchronous Counter	A.=	
	(Binary)	C47	68
74170	4-by-4 Register File	4 x (YL4 + B1N + V1N + U24) + 2 x DE4	10
74171	Quad D-FF with Clear	FDR + 4 x V1N	30
74172	16-bit (8 x 2) Register File	3 x DE6 + 4 x FDS + 16 x (N2N + G34 +	34
		+ V1N + 2 x R2P + 4 x U28) + 2 x V1N + 2 x R2P	

# TTL 7400 Function Conversion Table (Continued)

4-bit D-type Register	TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
(3-state Output)  (3-state Output)  (4)  Hex D-FF (Single Output)  74175  Quad D-FF (With Clear)  74176  Presettable Binary Counter  74177  74178  4-bit Universal Shift Register  74179  74181  ALU/Function Generator  74182  Look-ahead Carry Generator  74183  Dual Carry-save Full Adder  74184  BCD-to-binary Counter (Binary)  74190  Synch Up/Down Counter (Binary)  74191  Vp/Down Dual Clock Counter (Binary)  74192  Up/Down Dual Clock Counter (Binary)  74193  Up/Down Dual Clock Counter (Binary)  74194  4-bit Bidirectional Universal Shift Register  74195  74196  74197  74197  74198  BCD-to-Sperment Decoder/Driver  (30V, Active Low Open Collector)  74248  BCD-to-Segment Decoder/Driver  (15V, Active Low Open Collector)  74240  PCD-to-Jope FF with Clear  Quad J-FF With Clear  Quad J-FF With Clear  Quad J-FF With Clear  A x FDP + 2 x R2N + B41 + 6 x V1N + K1B + 4 x D24  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FDR + 2 x FDO  FD	74173	4-hit D-type Register		
Hax D=FF (Single Output)	74170		FDR + 2 x R2N + B41 + 6 x V1N + K1B + 4 x D24	53
74176	74174			40
74176 Presettable Discade/Binary Counter 74177 Presettable Binary Counter 74178 4-bit Universal Shift Register 74179 4-bit Universal Shift Register (Direct Clear) 74180 9-bit Cdd/Even Parity Checker 74181 ALU/Function Generator 74181 ALU/Function Generator 74182 Look-ahead Carry Generator 74183 Dual Carry-save Full Adder 74184 BCD-to-binary Code Converter 74185 Binary-to-BCD Code Converter 74185 Binary-to-BCD Code Converter 74190 Synch Up/Down Counter (BCD) 74191 Synch Up/Down Counter (BCD) 74192 Up/Down Dual Clock Counter (Binary) 74193 Up/Down Dual Clock Counter (Binary) 74194 4-bit Bidirectional Universal Shift Register 74195 A-bit Bidirectional Universal Shift Register 74196 Preset Binary Counter/Latch 74197 Preset Binary Counter/Latch 74198 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74276 Quad J-K FF 74276 Quad J-K FF 74276 Quad J-K FF 74276 Quad J-K FF 74276 Quad J-K FF 74276 Quad J-K FF 74276 Quad J-K FF 74276 Quad J-K FF 74276 Quad J-K FF 74276 Quad J-K FF 74276 Quad J-K FF 74276 Quad J-K FF 74276 Quad J-K FF 74276 Quad J-K FF 74276 Quad J-K FF 74276 Quad J-K FF 74276 Quad J-K FF 74276 Quad J-K FF 74276 Quad J-K FF 74197 Preset Binary Counter/Diver 74276 Quad J-K FF				30
74177				49
74179				47
4-bit Universal Shift Register (Direct Clear)				30
(Direct Clear)  74180  9-bit Odd/Even Parity Checker  74181  ALU/Function Generator  74182  Look-ahead Carry Generator  74184  BCD-to-binary Code Converter  74185  Binary-to-BCD Code Converter  74195  Synch Up/Down Counter (BCD)  74191  Synch Up/Down Counter (BCD)  74192  Up/Down Dual Clock Counter (Binary)  74193  Up/Down Dual Clock Counter (Binary)  74194  4-bit Bidirectional Universal Shift Register  74195  74196  Preset Decade/Binary Counter/Latch  74197  74198  8-bit Bidirectonal Universal Shift Register  74199  8-bit Bidirectonal Universal Shift Register  74190  74191  74192  74194  74194  74195  Preset Decade/Binary Counter/Latch  74196  74197  74198  8-bit Bidirectonal Universal Shift Register  74199  8-bit Bidirectonal Universal Shift Register  74199  74190  74191  74194  8-bit Bidirectonal Universal Shift Register  74195  74196  74197  74198  8-bit Bidirectonal Universal Shift Register  74199  8-bit Bidirectonal Universal Shift Register  74199  74190  74190  74191  74191  74191  74194  74194  74195  74195  74196  74196  74197  74198  74198  74198  74199  74199  74199  74199  74199  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190  74190				
74180			FS2 + 9 x N2N + B1N	40
ALU/Function Generator	74180	9-hit Odd/Even Parity Checker		23
N6B + N4B + 2 x N2N + 2 x N4P				20
Table   Look-ahead Carry Generator   Dual Carry-save Full Adder   2 x A1N	, 4, 6,	ALON GIOLON GONOIGLO		113
74183         Dual Carry-save Full Adder         2 x A1N           74184         BCD-to-binary Code Converter         These devices are ROM based           74185         Binary-to-BCD Code Converter         These devices are ROM based           74190         Synch Up/Down Counter (BCD)         4 x FDP + 4 x X2N + K1B + 3 x V1N + 3 x N3N + 9 x N2N + 2 x T32 + T43           74191         Synch Up/Down Counter (Binary)         C47           74192         Up/Down Dual Clock Counter (BCD)         4 x C11 + 4 x V2B + N6B + 2 x N3N + R2N + T32 + T42 + T43           74193         Up/Down Dual Clock Counter (Binary)         4 x C11 + 2 x N6B + 4 x V2B + R2N + D24 + T32 + T42 + T43           74194         4-bit Bidirectional Universal Shift Register         FDR + 6 x V1N + R2N + 4 x D36 + D23 + B1N           74195         4-bit Parallel Access Shift Register         FDR + 6 x V1N + R2N + 4 x N3N + K1B           74196         Preset Decade/Binary Counter/Latch         4 x FDP + 2 x R2N + 5 x N2N + 4 x N3N + K1B           74197         Preset Binary Counter/Latch         4 x FDP + 2 x R2N + 5 x N2N + 4 x N3N + K1B           74198         8-bit Bidirectional Universal Shift Register         2 x FDR + D24 + 10 x V1N + B1N + R2N + 8 x N2P           74199         8-bit Bidirectional Universal Shift Register         4 x FDP + 5 x N2N + 4 x N3N + K1B           74246         BCD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector	74182	Look-ahead Carry Generator		36
These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   These devices are ROM based   Thes				16
These devices are ROM based		•		10
74190 Synch Up/Down Counter (BCD)	74184		These devices are ROM based	
74191 Synch Up/Down Counter (Binary) 74192 Up/Down Dual Clock Counter (BCD) 74193 Up/Down Dual Clock Counter (Binary) 74194 4-bit Bidirectional Universal Shift Register 74195 4-bit Parallel Access Shift Register 74196 Preset Binary Counter/Latch 74197 Preset Binary Counter/Latch 74198 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74190 8-bit Bidirectional Universal Shift Register 74191 8-bit Bidirectional Universal Shift Register 74192 8-bit Bidirectional Universal Shift Register 74193 8-bit Bidirectional Universal Shift Register 74196 8-bit Bidirectional Universal Shift Register 74197 8-bit Bidirectional Universal Shift Register 74198 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74246 BCD-to-7-Segment Decoder/Driver (30V, Active Low Open Collector) 74247 BCD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector) 74249 BCD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector) 74249 BCD-to-7-Segment Decoder/Driver (Open Collector) 74249 BCD-to-7-Segment Decoder/Driver (Open Collector) 74260 Dual 5-input NOR 74260 Quad 2-EXNOR, Open Collector 74273 Octal D-type FF with Clear 74276 Quad J-FF 74276 Quad J-FF			These devices are ROM based	
74191 Synch Up/Down Counter (Binary) 74192 Up/Down Dual Clock Counter (BCD) 74193 Up/Down Dual Clock Counter (Binary) 74194 4-bit Bidirectional Universal Shift Register 74195 4-bit Parallel Access Shift Register 74196 Preset Decade/Binary Counter/Latch 74197 Preset Binary Counter/Latch 74198 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74190 8-bit Bidirectional Universal Shift Register 74191 4 x FDP + 5 x N2N + 4 x N3N + K1B 74276 20 Cpan Collector) 74244 8CD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector) 74249 8CD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector) 74249 8CD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector) 74249 8CD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector) 74249 8CD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector) 74249 8CD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector) 74249 8CD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector) 74249 8CD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector) 74249 8CD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector) 74249 8CD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector) 74249 8CD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector) 74249 8CD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector) 74249 8CD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector) 74240	74190	Synch Up/Down Counter (BCD)	4 x FDP + 4 x X2N + K1B + 3 x V1N + 3 x N3N	
Table			+ 9 x N2N + 2 x T32 + T43	
74193 Up/Down Dual Clock Counter (Binary)  74194 4—bit Bidirectional Universal Shift Register 74195 4—bit Parallel Access Shift Register 74196 Preset Decade/Binary Counter/Latch 74197 Preset Binary Counter/Latch 74198 8—bit Bidirectional Universal Shift Register 74199 8—bit Bidirectional Universal Shift Register 74199 8—bit Bidirectional Universal Shift Register 74199 8—bit Bidirectional Universal Shift Register 74199 8—bit Bidirectional Universal Shift Register 74199 8—bit Bidirectional Universal Shift Register 74199 8—bit Bidirectional Universal Shift Register 74199 8—bit Bidirectional Universal Shift Register 74246 BCD—to—7-Segment Decoder/Driver (30V, Active Low Open Collector) 74247 BCD—to—7-Segment Decoder/Driver (15V, Active Low Open Collector) 74248 BCD—to—7-Segment Decoder/Driver (15V, Active Low Open Collector) 74249 BCD—to—7-Segment Decoder/Driver (Open Collector) 74249 BCD—to—7-Segment Decoder/Driver (Open Collector) 74260 Dual 5—input NOR 74260 Quad 2—EXNOR, Open Collector 74273 Octal D—type FF with Clear 74276 Quad J—FF 74276 Quad J—FF 74276 Quad J—FF	74191	Synch Up/Down Counter (Binary)	C47	68
+ T42  T4194	74192	Up/Down Dual Clock Counter (BCD)		79
74195 4-bit Parallel Access Shift Register 74196 Preset Decade/Binary Counter/Latch 74197 Preset Binary Counter/Latch 74198 8-bit Bidirectional Universal Shift Register 8-bit Bidirectional Universal Shift Register 8-bit Bidirectional Universal Shift Register (JK Serial Input) or: 74246 BCD-to-7-Segment Decoder/Driver (30V, Active Low Open Collector) 74247 BCD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector) 74248 BCD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector) 74249 BCD-to-7-Segment Decoder/Driver (Internal Pull-up) 74249 BCD-to-7-Segment Decoder/Driver (Open Collector) 74249 BCD-to-7-Segment Decoder/Driver (Open Collector) 74240 Dual 5-input NOR 74260 Quad 2-EXNOR, Open Collector 74260 Quad 2-EXNOR, Open Collector 74273 Octal D-type FF with Clear 74276 Quad J-K FF 74276 Quad J-K FF	74193	Up/Down Dual Clock Counter (Binary)		72
74195 4-bit Parallel Access Shift Register 74196 Preset Binary Counter/Latch 74197 Preset Binary Counter/Latch 74198 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register 74240 BCD-to-7-Segment Decoder/Driver 74241 8-bit Bidirectional Universal Shift Register 74242 BCD-to-7-Segment Decoder/Driver 74243 BCD-to-7-Segment Decoder/Driver 74244 BCD-to-7-Segment Decoder/Driver 74245 BCD-to-7-Segment Decoder/Driver 74249 BCD-to-7-Segment Decoder/Driver 74249 BCD-to-7-Segment Decoder/Driver 74249 BCD-to-7-Segment Decoder/Driver 74240 Dual 5-input NOR 74260 Quad 2-EXNOR, Open Collector 74260 Quad 2-EXNOR, Open Collector 74273 Octal D-type FF with Clear 74276 Quad J-FF	74194	4-bit Bidirectional Universal Shift Register	FDR + 6 x V1N + R2N + 4 x D36 + D23 + B1N	48
74196 Preset Decade/Binary Counter/Latch 74197 Preset Binary Counter/Latch 74198 8-bit Bidirectional Universal Shift Register 74199 8-bit Bidirectional Universal Shift Register (JK Serial Input) 74246 BCD-to-7-Segment Decoder/Driver (30V, Active Low Open Collector) 74247 BCD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector) 74248 BCD-to-7-Segment Decoder/Driver (16V, Active Low Open Collector) 74249 BCD-to-7-Segment Decoder/Driver (Internal Pull-up) 74249 BCD-to-7-Segment Decoder/Driver (Open Collector) 74250 Quad 2-EXNOR, Open Collector 74260 Quad 2-EXNOR, Open Collector 74273 Octal D-type FF with Clear 74276 Quad J-FF	74195	4-bit Parallel Access Shift Register	FS2 + D24 + 2 x V1N	34
74197 Preset Binary Counter/Latch	74196	Preset Decade/Binary Counter/Latch	4 x FDP + 2 x R2N + 5 x N2N + 4 x N3N + K1B	49
74199 8-bit Bidirectional Universal Shift Register (JK Serial Input) 2 x FS2 + D24 + 3 x V1N + B1N + R2N + 8 x N2P or: 2 x FDR + 7 x D24 + T33 + 11 x V1N + R2N  74246 BCD-to-7-Segment Decoder/Driver (30V, Active Low Open Collector) 4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74247 BCD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector) 4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74248 BCD-to-7-Segment Decoder/Driver (Internal Pull-up) 4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74249 BCD-to-7-Segment Decoder/Driver (Open Collector) 4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74260 Quad 2-EXNOR, Open Collector 4 x V1N 74266 Quad Complementary Output Element 74276 Quad J-type FF with Clear 2 x FDR 74276 Quad J-KFF 4 x (FDP + V1N + D24) + 2 x B1N	74197	Preset Binary Counter/Latch	4 x FDP + 5 x N2N + 4 x N3N + K1B	47
or: 2 x FDR + 7 x D24 + T33 + 11 x V1N + R2N  74246 BCD-to-7-Segment Decoder/Driver (30V, Active Low Open Collector) 4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74247 BCD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector) 4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74248 BCD-to-7-Segment Decoder/Driver (Internal Pull-up) 4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74249 BCD-to-7-Segment Decoder/Driver (Open Collector) 4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74260 Dual 5-input NOR 2 x R6B  74265 Quad Complementary Output Element 74266 Quad 2-EXNOR, Open Collector 4 x X1N  74273 Octal D-type FF with Clear 2 x FDR  74276 Quad J-K FF 4 x (FDP + V1N + D24) + 2 x B1N			2 x FDR + D24 + 10 x V1N + R2N + 8 x D36	89
74246 BCD-to-7-Segment Decoder/Driver (30V, Active Low Open Collector) 4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74247 BCD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector) 4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74248 BCD-to-7-Segment Decoder/Driver (Internal Pull-up) 4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74249 BCD-to-7-Segment Decoder/Driver (Open Collector) 4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74260 Copen Collector) 4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74260 Quad 2-EXNOR, Open Collector 4 x X1N  74266 Quad 2-EXNOR, Open Collector 4 x X1N  74276 Quad J-Hype FF with Clear 2 x FDR  74276 Quad J-K FF 4 x (FDP + V1N + D24) + 2 x B1N		Register (JK Serial Input)	2 x FS2 + D24 + 3 x V1N + B1N + R2N + 8 x N2P	83
74246 BCD-to-7-Segment Decoder/Driver (30V, Active Low Open Collector)			2 x FDR + 7 x D24 + T33 + 11 x V1N + R2N	85
(30V, Active Low Open Collector)  74247 BCD-to-7-Segment Decoder/Driver (15V, Active Low Open Collector)  74248 BCD-to-7-Segment Decoder/Driver (Internal Pull-up)  74249 BCD-to-7-Segment Decoder/Driver (Open Collector)  74260 Quad Complementary Output Element  74265 Quad Complementary Output Element  74266 Quad 2-EXNOR, Open Collector  74273 Octal D-type FF with Clear  74276 Quad J-FF  74276 Quad J-FF  74277 Quad J-FF  74278 Quad J-FF  74278 Quad J-FF  74278 Quad J-FF  74279 Quad J-FF  74279 Quad J-KFF  74279 Quad J-KFF  74270 Quad J-KFF  74271 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74278 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74278 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74278 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74279 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74270 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74270 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74270 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74270 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74270 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74270 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74270 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74270 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74270 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74270 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74270 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74270 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74270 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74270 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74270 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74270 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74270 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74270 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74270 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74270 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74270 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74270 Ax V1N + 11 x N2N + 10 x N3N + 4 x N3P	74246			
(15V, Active Low Open Collector)  74248 BCD-to-7-Segment Decoder/Driver (Internal Pull-up)  74249 BCD-to-7-Segment Decoder/Driver (Open Collector)  74260 Dual 5-input NOR  74265 Quad Complementary Output Element  74266 Quad 2-EXNOR, Open Collector  74273 Octal D-type FF with Clear  74276 Quad J-KFF  74276 Quad J-KFF  74276 Quad J-KFF  74276 Quad J-KFF  74278 Quad J-KFF  74278 Quad J-KFF  74278 Quad J-KFF  74278 Active Low Open Collector)  4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  2 x R6B  81N + V1N  2 x K1N  2 x FDR  4 x (FDP + V1N + D24) + 2 x B1N	74247	(30V, Active Low Open Collector)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
(Internal Pull–up) 4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74249 BCD-to-7-Segment Decoder/Driver (Open Collector) 4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P  74260 Dual 5-input NOR 2 x R6B  74265 Quad Complementary Output Element B1N + V1N  74266 Quad 2-EXNOR, Open Collector 4 x X1N  74273 Octal D-type FF with Clear 2 x FDR  74276 Quad J-K FF 4 x (FDP + V1N + D24) + 2 x B1N	74248	(15V, Active Low Open Collector)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
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# **Unit Cell Specification Information**

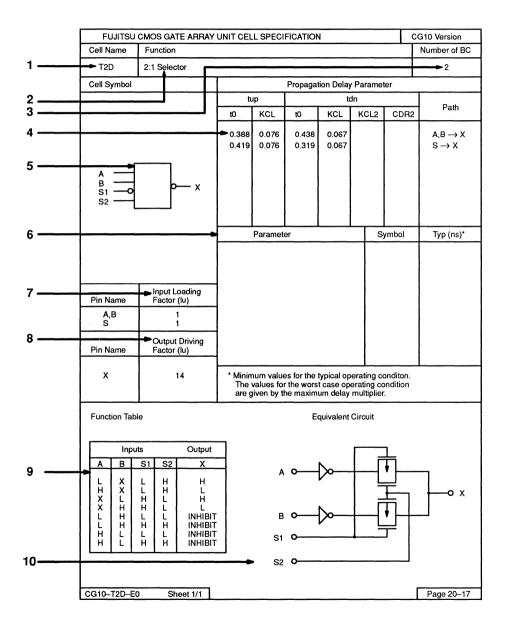
This section contains specifications for all the unit cells available for the CG10 Series CMOS Gate Arrays. The unit cell (gate array) is a functional group of one or more basic cells or gates.

#### How to Read a Unit Cell Specification

The following paragraphs numbered 1–10 explain how the information given in the CG10 Unit Cell Library is organized. Each of the numbers corresponds to an area of the Unit Cell Library page illustrated on the right.

- 1. The unit *cell name* appears in the upper left corner of the page.
- 2. The unit cell function is given on the same line as the unit cell name.
- 3. The *number of basic cells (BC)* or equivalent that make up the unit cell is shown in the upper right corner of the page.
- 4. Propagation delay parameters for each signal path offered by the unit cell are given in a table on the upper right side of the page. The basic delay time of the unit cell (t0) is given in ns. K<sub>CL</sub>, the delay constant for the cell (delay time per load unit) is given in ns/pF. K<sub>CL2</sub> and C<sub>DR2</sub> are a delay constant and an output drive factor used to calculate delay when a unit cell is loaded beyond its published output drive factor (C<sub>DR</sub>).
- 5. The cell symbol (logic symbol) is shown in the top left box under the cell name.
- Clock parameters (in ns) for unit cells such as flip-flops and counters that make use of clock signals are given in a table directly below the propagation delay parameters.
- 7. Input loading factors are shown in a table directly under the cell symbol box on the left side of the page. The input loading factor is the value of the load placed on a net by the connection of the unit cell input. Unit cell loading factors are shown in load units (lu). The Fujitsu CMOS load unit is the input capacitance of an inverter used for the measurement and calculation of capacitive loads presented to unit cells within the gate array.
- The output drive factor is shown directly under the input loading factor. The output drive factor is the maximum number of load units the unit cell can drive while performing at published specifications.
- 9. The function table, (truth table) if applicable, is shown in a box at the lower left side of the page.
- The unit cell schematic, or equivalent circuit, illustrates how discrete components would be connected to perform the unit cell function. It is shown in the lower right corner of the page or on the page following.

3



3

# **Inverter and Buffer Family**

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FUJIT	SU CMOS GATE AF	RRAY UNIT	CELL S	PECIFICA	ATION		" CG10	* Version
Cell Name	Function							Number of B
V1N	Inverter							1
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Pin Name	Output Driving					ı		
×	Factor (lu)	-						
^	"	* Minimu	m values for	the typical	operating o	ondition.		·
		The val	ues for the v				given by th	e maximum delay
		multiplie	er.					
	I							
C10-V1N-E0	Sheet 1/1							

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG10	" Version
Cell Name	Function			·····				Number of BC
V2B	Power Inverter							1
Cel	Symbol			Proj	pagation D		eter	
		t O	KCL	t O	KCL	in KCL2	CDR2	Path
		0.156	0.034	0.156	0.028	0.045	7	A to X
		000	0.00	000	0.020	0.0.0	'	
	<b>N</b>							
Α	> ×							
	•							
						L		
		Paramete	r				Symbol	Typ (ns) *
							İ	
						1		
Pin Name	Input Loading Factor (lu)							
Α	2							
••	_					į		
						1		
						İ		
Pin Name	Output Driving Factor (lu)							
×	36					ı		
		* Minimu	m values fo	r the typical	operating of	condition.		
				worst case	operating o	ondition are	given by the	maximum delay
		multiplie	ər.					
C10 V2P E0	Sheet 1/1							
C10-V2B-E0	Sheet 1/1							Page 1-2

Cell Symbol True Buffer 1  Cell Symbol Propagation Delay Parameter to the Color of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of the World of	EILUT	SILOMOS GATE AD	DAV LINIT	CELLS	DECIEIC	ATION		" CG10	" Version
Cell Symbol  Up UD	Cell Name	Function Function	DAT UNI	OELL S	r EUIFIU/	MITON		<u> </u>	Number of BC
Pin Name Input Loading Factor (lu)  X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	B1N	True Buffer							1
Pin Name Input Loading Factor (tu)  X  18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									
Pin Name Input Loading Factor (Iu)  A 1  Pin Name Output Driving Factor (Iu)  X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.					••			0000	Path
Plin Name Input Loading Factor (tu)  X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							KCL2	CDR2	A to X
Pin Name Input Loading Factor (lu)  A 1  Pin Name Output Driving Factor (lu)  X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	۸	· v							
Pln Name Input Loading A 1  Pln Name Output Driving Factor (Iu)  X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	^	`							
Pln Name Input Loading A 1  Pln Name Output Driving Factor (Iu)  X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									<del></del>
Pin Name Output Driving Factor (tu)  X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.			Paramete	er				symbol	ıyp (ns) "
Pin Name Output Driving Factor (tu)  X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									
Pin Name Output Driving X 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.		Factor (lu)							
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	A	1							
Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Minimum values for the typical operating condition are given by the maximum delay multiplier.		Factor (lu)							
C10_R1N_F0 Sheet 1/1	X	18	The val	ues for the	r the typical worst case	operating o	ondition. ondition are	given by the	e maximum delay
	C10_R1N_F0	Sheet 1/1							
Page 1–3	C10-B1N-E0	Sheet 1/1							Page 1_2

	011 01100 01TE 1DE		0511.0	DEOIEIO	171011		" CC10	7 \/ 0 == 2 ==
Cell Name	SU CMOS GATE ARP	RAY UNII	CELLS	PECIFICA	ATION		" CG10	Number of BC
BD3	Delay Cell							5
Cel	l Symbol			Pro		elay Param	eter	
		t O	IP KCL	t O	KCL to	in KCI 0	6000	Path
Α	×	3.331	0.067	2.944	0.067	0.073	4 4	A to X
		Paramete				٠,	Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)							
A	1							
Pin Name	Output Driving Factor (lu)							
X	18	* Minimur The value multiplie		r the typical worst case	operating o	condition.	given by the	maximum delay
C10-BD3-E0	Sheet 1/1							
								Page 1-4

							I # 0010			
FUJIT	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG10" Version  Cell Name Function Number of B									
BD4	Delay Cell							4		
	l Symbol	1		Pro	pagation D	elay Paran	neter	<del></del>		
<del></del>		t	φ			dn		Path		
		t O	KCL	t O	KCL	KCL2	CDR2			
		2.225	0.240	2.563	0.174	0.202	4	A to X		
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						l				
		1				1				
		l			ŀ	1	1			
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	_	l	1		İ	ł				
Α	×		1			l				
•						l				
						1				
						1	Į			
		Paramete			L	<del></del>	J Symbol	Typ (ns) *		
		- c.amete	·				_,01	. , , , (113)		
		l				- 1				
						1				
· · ·	Input Loading	1				- 1				
Pin Name	Factor (lu)									
A	4					- 1				
						ľ	,			
							,			
Pin Name	Output Driving	1								
	Factor (lu)	ļ								
×	6	<del> </del>						<u> </u>		
		* Minimu	m values for	the typical	operating o	condition.	aiven by th	e maximum delay		
		multiplie		MOISI Case	operating o	oridition are	given by a	o maximum oday		
C10-BD4-E0	Sheet 1/1									
310 004-00	<u> </u>							Page 1-5		

FUJIT Cell Name	SU CMOS GATE ARE	RAY UNIT	CELLS	PECIFICA	ATION		" CG10	" Version Number of BC
BD5	Delay Cell							9
Cell	Symbol			Pro	pagation D	elay Param	neter	
		t 0	JP KOL	t'0		in	0000	Path
		6.825	KCL 0.067	6.469	ксL 0.056	0.084	CDR2	A to X
		0.023	0.007	0.403	0.050	0.004	"	AIUA
					1			
Α	x							
~								
		Paramete			L	٠ .	Symbol	Typ (ns) *
		1						
		ļ				- 1		
Pin Name	Input Loading Factor (Iu)							
Α	1	1						
		l						
		j						
Pin Name	Output Driving	1						
х	Factor (lu) 18	ł						
^		* Minimu	m values fo	the typical	operating o	ondition.		
		The val	ues for the				given by the	maximum delay
		multiplie	er.					
	L	<del></del>						
C10-BD5-E0	Sheet 1/1							
								Page 1-6

FILIIT	SU CMOS GATE AR	RAY LINIT	CELLS	PECIFIC	ATION		" CG10	" Version
Cell Name	Function	OIVII	O		,,,,,,,,,			Number of BC
BD6	Delay Cell							17
Cel	l Symbol			Pro		elay Paran	neter	
		10	KCL	to	KCL	tn KCL2	CDR2	Path
		13.750	0.072	13.638	0.051	0.079	4	A to X
		10.700	0.072	10.000	0.00	1 0.070	'	
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						l	1 1	
		1		1				
					i		1	
				1		1		
Α	×							
							1 1	
		1						
		ļ				}		
		Paramete	эг				Symbol	Typ (ns) *
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		Ì					l	
		l					ĺ	
	[	-				ŀ		
Pin Name	input Loading Factor (lu)	į				1		
Α	1	1						
		ł				- 1		
		ł						
		j						
Pin Name	Output Driving Factor (lu)					- 1		
x	18	1						
^		* Minimu	m values fo	r the typical	operating o	condition.		
		The val	ues for the				given by th	e maximum delay
		multiplie	er.					
		J						
C10-BD6-E0	Sheet 1/1							
C10-000-E0	Sheet 1/1							Page 1-7
								1 age 1-7

## **NAND Family**

Page	Unit Cell Name	Function	Basic Cells
3–17	N2N	2-input NAND	1
3–18	N2B	Power 2-input NAND	3
3–19	N2K	Fast Power 2-input NAND	2
3-20	N3N	3-input NAND	2
3–21	N3B	Power 3-input NAND	3
3–22	N3K	Fast Power 3-input NAND	3
3–23	N4N	4-input NAND	2
3-24	N4B	Power 4-input NAND	4
3–25	N4K	Fast Power 4-input NAND	4
3-26	N6B	Power 6-input NAND	5
3–27	N8B	Power 8-input NAND	6
3-28	N9B	Power 9-input NAND	8
3–29	NCB	Power 12-input NAND	10
3–30	NGB	Power 16-input NAND	11

3

Cell Name	SU CMOS GATE ARF	IAT UNIT	CELL 3	r EGIFICA	TION		0070	" Version Number of
N2N	2-input NAND							1
Cel	l Symbol			Pro	pagation D	elay Paran	neter	i
			ıp		to	in		Path
		0.231	KCL 0.067	0.350	KCL 0.079	KCL2	CDR2	A to X
A1 A2	<b>∩</b> o— ×							
A2	D^							
		Paramete				1	Symbol	Typ (ns) *
				_				135 ()
Pin Name	Input Loading Factor (lu)							
A	1							
Pin Name	Output Driving Factor (lu)							
x	18	* Minimu The val multiplie		the typical worst case	operating o	condition. condition are	given by th	e maximum delay

ELLIT	SU CMOS GATE ARE	TIMIT VAC	CELL C	DECITIO	ATION		" CG10 "	Version
Cell Name	Function	AT UNII	CELLS	PECIFICA	ATION		CG10	Number of BC
N2B	Power 2-input N	IAND			-			3
Cel	Symbol			Pro	pagation D	elay Paran	neter	
		tu				in		Path
A1 ————————————————————————————————————	D•—×	0.688	0.034	0.888	0.023	KCL2	CDR2	A to X
		Paramete					Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)							
A	1							
Pin Name	Output Driving							
×	Factor (Iu)							
^	36	* Minimur The value multiplie	ues for the	r the typical worst case	operating o	condition.	given by the	maximum delay
C10-N2B-E0	Sheet 1/1							
								Page 2-2

FUJI	TSU CMOS GATE AR	RAY UNIT	CELL S	PECIFICA	ATION		" CG10	" Version
Cell Name	Function							Number of B
N2K	Power 2-input	NAND						2
	II Company	<del></del>		D	pagation D	alau Danas		
Ce	li Symbol	+	ıb	Proj		in Paran	reter	
		10	KCL	t O	KCL	KCL2	CDR2	Path
		0.231	0.034	0.269	0.039	0.051	7	A to X
		1						
		}						
A1	<b>√</b> "							
A2	×							
	-							
			Ì					
		Paramete	er				Symbol	Typ (ns) *
						- 1		
						- 1		
						ı		
Pin Name	Input Loading							
	Factor (lu)	-				i		
A	2							
	ļ	4						
Pin Name	Output Driving Factor (lu)	1				ļ		
×	36	1						
		* Minimu	m values for	the typical	operating o	ondition.		
							given by th	e maximum delay
	ļ	multiplie	er.					
		<u> </u>						
C10-N2K-E0	Sheet 1/1							

FUJIT Cell Name	SU CMOS GATE ARF	RAY UNIT	CELLS	PECIFIC	ATION		" CG10	" Version Number of BC
N3N	3-input NAND							2
Cell	l Symbol			Pro	pagation D	elay Para	meter	
		10	JP KCL		KCL	tn KCL2	CDR2	Path
		0.325	0.067	0.431	0.107	NOL2	CURZ	A to X
		0.525	0.007	0.451	0.107	ļ	1 1	7107
							1 1	
						1		
					1	1	1 1	
					1	l	1 1	
A1	_					l		
A2	b ×				l		1 1	
АЗ	V							
					l			
		Paramete	r				Symbol	Typ (ns) *
							į	
						1		
						1		
						- 1		
	Input Loading					İ		
Pin Name	Factor (lu)							
A	1						]	
						ı		
						- 1		
	Output Driving							
Pin Name	Factor (lu)							
х	14							
		* Minimu	m values for	the typical	operating o	condition.		maximum delay
		multiplie		worst case	operating o	ondition at	re given by the	maximum delay
C10 NON EC	Choot 4/4							
C10-N3N-E0	Sheet 1/1							Page 2-4

FUJIT	SU CMOS GATE AR	RAY UNIT	CELL S	PECIFICA	ATION		" CG10	" Version
Cell Name	Function							Number of B
N3B	Power 3-input I	DNAN						] 3
	l I Symbol	1		Pro	pagation D	elav Paran	neter	
	-,	tı	qı			n		Path
		10	KCL	t O	KCL	KCL2	CDR2	
		0.800	0.034	1.063	0.023			A to X
			<b>.</b>					
		1						
		l					i i	
		l					}	
	~	1					] ]	
A1 ——— A2 ———	Ъ×							
A3 ——	)	1						
							1	
		1						
		Paramete	!			<u> </u>	Symbol	Typ (ns) *
		1						
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		l				1		
	Input Loading	-					į	
Pin Name	Factor (lu)	ļ						
A	1	1						
		ľ						
		ł				- 1		
		1						
Pin Name	Output Driving Factor (lu)	}						
x	36	1						
			m values for					
		The val		worst case	operating o	ondition are	given by th	e maximum delay
		mulupik	ar.					
C10-N3B-E0	Sheet 1/1							
								Page 2-5

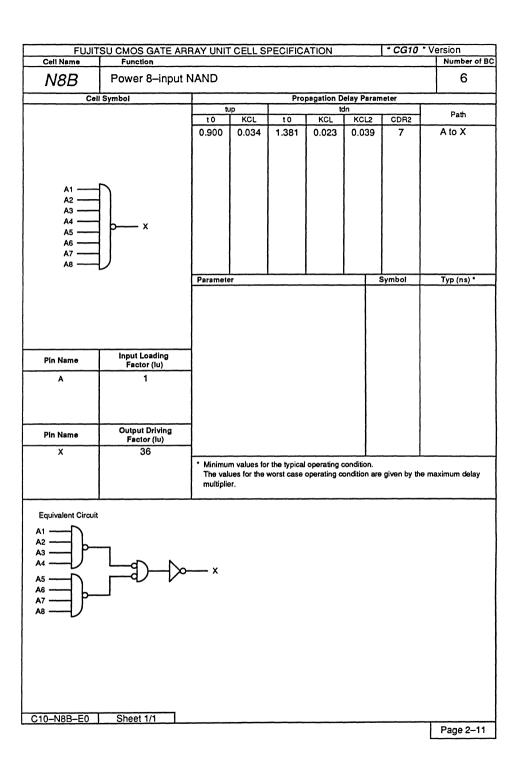
F11115	OU 01400 04TF 4DF	3 4 3 / 1 15 117		DEOLEIO	A T1011		L # 0040 P	Maraian
Cell Name	SU CMOS GATE ARF	AAY UNII	CELLS	PECIFICA	ATION		" CG10 "	Number of BC
N3K	Power 3-input N	IAND						3
Cel	l Symbol			Pro	pagation D	elay Param	neter	
			dr.			nt		Path
A1 ————————————————————————————————————	<b>∑</b> —×	to 0.300	0.030	t0 0.406		dn KCL2	CDR2	Path A to X  Typ (ns) *
Pin Name	input Loading Factor (lu)							
	2					ĺ		
Pin Name	Output Driving Factor (lu) 28							
		* Minimui The val multiplie		r the typical worst case	operating o	condition. ondition are	given by the	maximum delay
C10-N3K-E0	Sheet 1/1							Page 2-6
								. Faue 2-0

Cell Name   Function   A-input NAND   2    Cell Symbol   Propagation Delay Parameter   Input Loading   Factor (Iu)    A	FILIT	SUCMOS GATE ARE	RAY LINIT	CELLS	PECIFIC	ATION		" CG10	" Version	
Cell Symbol  Tup  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To K	Cell Name	Function		<u> </u>						er of BC
Cell Symbol  Tup  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To KCL  To K	N4N	4-input NAND							2	2
Pin Name Input Leading Factor (lu)  A 1  Pin Name Pactor (lu)  A 1  Pin Name Output Driving Factor (lu)  X 10  * Minimum values for the typical operating condition are given by the maximum dela multiplier.			r		Pro	nagation D	elay Parar	neter		
Pin Name Input Loading Factor (lu)  X  10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.		i Oyiiiboi	tı	JD QL	7.10			iletoi	D. 11	
Pin Name Input Leading Factor (Iu)  A 1  Pin Name Soutput Driving Factor (Iu)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.							KCL2	CDR2		
Pin Name Input Leading Factor (lu)  A 1  Pin Name Sector (lu)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.			0.388	0.067	0.463	0.135	1	1	A to X	
Pin Name Input Leading Factor (lu)  A 1  Pin Name Sector (lu)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.						ł	l	Ì		
Pin Name Input Leading Factor (lu)  A 1  Pin Name Sector (lu)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.			1					!	ı	
Pin Name Input Leading Factor (lu)  A 1  Pin Name Sector (lu)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.				ľ			ł	İ		
Pin Name Input Leading Factor (lu)  A 1  Pin Name Sector (lu)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.				ł						
Pin Name Input Loading Factor (lu)  A 1  Pin Name Soutput Driving Factor (lu)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.		U		l						
Pin Name Input Loading Factor (lu)  A 1  Pin Name Pactor (lu)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.		b x								
Pin Name Input Loading Factor (Iu)  A 1  Pin Name Output Driving Factor (Iu)  X 10  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.		1)		ļ						
Pin Name   Input Loading   Factor (lu)    A			1	}			1	j l		
Pin Name   Input Loading   Factor (lu)    A								}		
Pin Name Output DrIving Factor (Iu)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.			Paramete	er				Symbol	Typ (n	s) *
Pin Name Output DrIving Factor (Iu)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.										
Pin Name Output DrIving Factor (Iu)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.										
Pin Name Output DrIving Factor (Iu)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.							}			
Pin Name Output DrIving Factor (Iu)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.			l				1			
Pin Name Output DrIving Factor (Iu)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.	Pin Name	Input Loading Factor (Iu)					ł			
Pin Name Sector (Iu)  X 10  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.	A		İ				j			
* Minimum values for the typical operating condition.  The values for the worst case operating condition are given by the maximum dela multiplier.			1				j			
* Minimum values for the typical operating condition.  The values for the worst case operating condition are given by the maximum dela multiplier.							1			
* Minimum values for the typical operating condition.  The values for the worst case operating condition are given by the maximum dela multiplier.							l			
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.	Pin Name	Output Driving Factor (lu)								
The values for the worst case operating condition are given by the maximum dela multiplier.	x									
multiplier.			* Minimu	m values for	the typical	operating o	condition.	airea by th	a mavimum d	lolov
					WOISE CASE	operating G	originori are	a given by a	o maximum o	ыау
									<del></del>	
C10 NAN EO I Shoot 1/1 I	C10 NAN EC	Choot 4/4								
C10-N4N-E0   Sheet 1/1   Page 2-	C10-N4N-E0	Sheet 1/1							Page	2-7

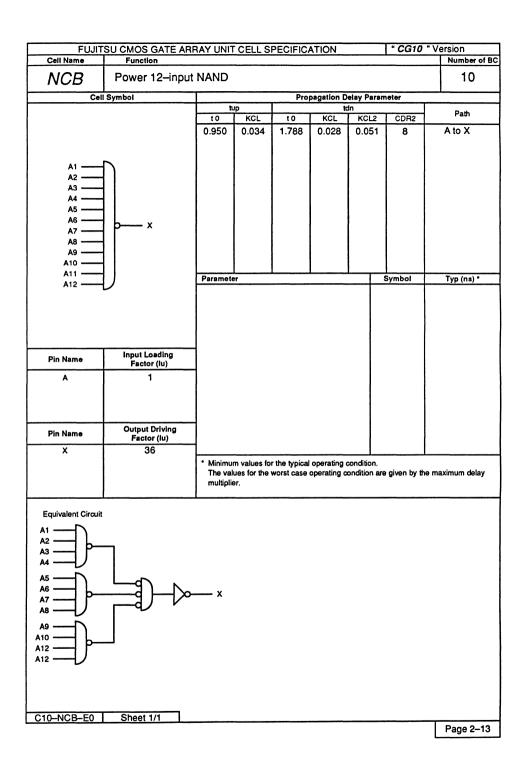
FU.IIT	SU CMOS GATE ARE	RAY LINIT	CELLS	PECIFICA	ATION		" CG10	" Version	_
Cell Name	Function	0.411	J VI					Number of	ВС
N4B	Power 4-input N	IAND	والتاليز وسيطار وسيادا الأوس					4	
Cell	Symbol			Proj	pagation D		meter		
		tu		10		in KCIO	CDDC	Path	
		t 0 0.863	KCL 0.034	1.188	KCL 0.023	KCL2	CDR2	A to X	
		0.003	0.034	1.100	0.023	1		7.0 X	
						1			
A1	<b>D</b>				l				
A2	р—— х								
A3	] ]								
		Paramete	r				Symbol	Typ (ns) *	
						1			
2	i								
Pin Name	Input Loading								
	Factor (lu)								i
A	1								
Pin Name	Output Driving								
	Factor (lu)								
X	36	* Minimu	m values fo	r the typical	operating				
		The val	ues for the	worst case	operating c	ondition a	re given by th	e maximum delay	
		multiplie	er.						
	L	L							
C10-N4B-E0	Sheet 1/1							Page 2-	
								1 Page 2-3	×

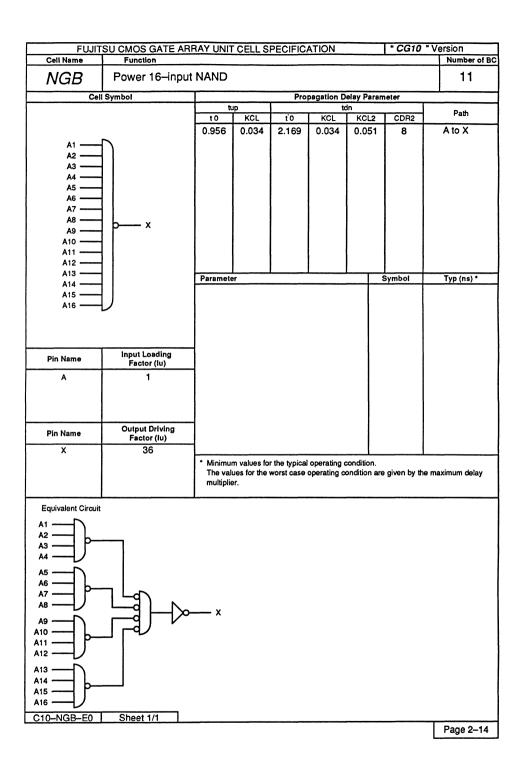
FUJIT	SU CMOS GATE ARE	RAY UNIT	CELLS	PECIFICA	ATION		" CG10	"Version
Cell Name	Function		<u> </u>					Number of BC
N4K	Power 4-input N	DNAN						4
Cel	Symbol			Pro	pagation D		neter	
		t O	KCL	t O	KCL	in KCL2	CDR2	Path
A1 A2 A3	<b>∫</b> ₀— ×	0.350	0.030	0.475	0.056	ROLE	ODAZ	A to X
A4	D	Paramete	er				Symbol	Typ (ns) *
	input Loading							
Pin Name	Factor (lu)							
A	2							
Pin Name	Output Driving Factor (lu)							
X	20						given by th	e maximum delay
C10-N4K-E0	Sheet 1/1							
								Page 2-9

FUJIT Cell Name	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG10	" Version Number of BC
N6B	Power 6-input N	IAND						5
L							·	
Cel	l Symbol	t t	JD D	Pro	pagation D to	elay Para In	meter	
		t O	KCL	t O	KCL	KCL2	CDR2	Path
		0.856	0.034	1.263	0.023	0.039	7	A to X
							1	
							1	
	_							
A1 ————————————————————————————————————	1)							
A3 ——	р—— х							
A5							1 1	
A6	V						1 1	
		Paramete	er			١	Symbol	Typ (ns) *
İ							1	
	r						1	
Pin Name	Input Loading Factor (lu)					İ		
A	1					İ		
Pin Name	Output Driving Factor (lu)							
×	36							
			m values for					maximum delay
		multiplie		worst case	operating o	ondition a	re given by the	maximum delay
	<u> </u>	L						
Equivalent Circuit								
A1 —								
A2 D								
A4 —		— x						
A5								
C10-N6B-E0	Sheet 1/1							Dog 0 40
								Page 2-10



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG10" V										
Cell Name	Function							Number of BC		
N9B	Power 9-input N	IAND						8		
Cel	Symbol			Pro	pagation D		neter			
		t O	KCL	10	KCL	in KCL2	CDR2	Path		
		0.888	0.034	1.663	0.028	0.051	7	A to X		
A1 ————————————————————————————————————	> ×									
A7										
A9		Paramete				L	Symbol	Typ (ns) *		
Pin Name	Input Loading Factor (lu)					ļ	l			
A	1									
Pin Name	Output Driving Factor (lu)									
X	36	* Minimur The value multiplie	ues for the v	the typical worst case	operating o	condition. condition are	given by the	maximum delay		
Equivalent Circuit A1 A2 A3 A4 A5 A6 A7 A8 A9		— х								
C10-N9B-E0	Sheet 1/1							Page 2–12		





## **NOR Family**

Page	Unit Celi Name	Function	Basic Cells
3–33	R2N	2-input NOR	1
3–34	R2B	Power 2-input NOR	3
3–35	R2K	Power 2-input NOR	2
3–36	R3N	3-input NOR	2
3–37	R3B	Power 3-input NOR	3
3–38	R3K	Power 3-input NOR	3
3–39	R4N	4-input NOR	2
3-40	R4B	Power 4-input NOR	4
3–41	R4K	Power 4-input NOR	4
3-42	R6B	Power 6-input NOR	5
3-43	R8B	Power 8-input NOR	6
3–44	R9B	Power 9-input NOR	8
3–45	RCB	Power 12-input NOR	10
3–46	RGB	Power 16-input NOR	11

3

EUNT	CILCMOS CATE ADI	DAY HAIT	CELL C	DECIFIC	ATION		" CG10	" Version
Cell Name	SU CMOS GATE ARE	TAT UNII	CELLS	PECIFICA	ATION		CG10	Number of BC
R2N	2-input NOR							1
Cel	Symbol			Proj	pagation D		neter	
			IP KCL	40		in VOLO	0000	Path
		0.250	0.122	t 0 0.275	KCL 0.045	KCL2 0.062	CDR2	A to X
A1 A2	<b>₽</b> ⊶×	Paramete		0.273	0.043		Symbol	Typ (ns) *
Pin Name	Input Loading							
	Factor (lu)	1						
A Pin Name	1 Output Driving							
	Factor (lu)							
X	14						given by th	ie maximum delay
C10-R2N-E0	Sheet 1/1							
								Page 3-1

								1/
Cell Name	SU CMOS GATE ARE	RAY UNII	CELL S	PECIFICA	ATION		" CG10 "	Number of BC
R2B	Power 2-input N	NOR	·					3
Cel	l Symbol	Γ		Proj	pagation D	elay Paran	neter	
			ıp		to			Path
		0.850	ксL 0.034	0.781	KCL 0.023	KCL2	CDR2	A to X
A1 A2	<b>&gt;</b> ×							
		Paramete	er				Symbol	Typ (ns) °
Pin Name	Input Loading Factor (lu)							
A	1							
Pin Name	Output Driving Factor (lu)							
x	36	* Minimur The value multiplie		r the typical worst case	operating coperating co	condition.	given by the	maximum delay
C10-R2B-E0	Sheet 1/1							
J.J.,.ED-EJ	<u> </u>							Page 3-2

FUJIT Cell Name	SU CMOS GATE ARE	RAY UNIT	CELLS	PECIFIC	ATION		" CG10	" Version Number of BC
R2K	Power 2-input N	NOR						2
	l   Symbol			Pro	pagation D		neter	
		t O	KCL	t O	KCL to	in KCL2	CDR2	Path
A1 A2	<b>▷</b> —×	0.281	0.059	0.281	0.034			A to X
		Paramete	r				Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)							
A	2							
Pin Name	Output Driving Factor (lu)							
×	36	* Minimu The val multiplie		r the typical worst case	operating o	condition.	given by th	e maximum delay
C10-R2K-E0	Sheet 1/1		····					Page 3–3

Cell Name	SU CMOS GATE ARI	RAY UNIT	CELLS	PECIFICA	ATION		" CG10 "	Version Number of BC
R3N	3-input NOR							2
Cel	l Symbol			Pro	pagation D		neter	
		10	KCL	10	KCL	in KCL2	CDR2	Path
		0.525	0.172	0.288	0.051	0.067	4	A to X
							·	
A1	A							
A2	<del>   - </del> ×							
A3	<del>D</del>							
		Paramete				L	Symbol	Tun (ne) t
		Paramete	<del>.</del>				Symbol	Typ (ns) *
		ļ				ı		
Pin Name	Input Loading Factor (lu)	İ						
A	1	1						
						l		
Pin Name	Output Driving					į		
x	Factor (lu)	ł				l		
		* Minimu	m values for	r the typical	operating of	ondition.		
		The val		worst case	operating o	ondition are	given by the	maximum delay
		moluplie	۶۱. 					
1								
0.00 0011 00	01							
C10-R3N-E0	Sheet 1/1							Page 3-4
								aye 5-4

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELL S	PECIFIC	ATION		* CG10	" Ve	ersion	
Cell Name	Function								Number of BC	
R3B	Power 3-input N	IOR							3	
	Symbol .			Dear	nagation D	elav Paren	neter			
Con	i Oyiiiooi	ħ	Propagation Delay Parameter tup tdn							
		10	KCL	t O	KCL	KCL2	CDR2		Path	
		1.244	0.034	0.856	0.023				A to X	
		Į					1 1			
		1								
j							1			
	_	1					1		:	
A1	x									
A3 —	^									
İ '										
		Paramete				٠	Symbol		Typ (ns) *	
]										
	1									
Pin Name	Input Loading Factor (lu)					ı				
Α	1									
						- 1				
						- 1				
Pin Name	Output Driving Factor (lu)									
×	36					1				
		* Minimu	m values for	the typical	operating o	ondition.				
				worst case	operating o	ondition are	given by th	e ma	ximum delay	
		multiplie	er.							
	<u> </u>									
									į	
C10-R3B-E0	Sheet 1/1									
								L	Page 3-5	

FUJIT Cell Name	SU CMOS GATE ARE	RAY UNIT	CELLS	PECIFICA	ATION		" CG10 "	
	Function							Number of BC
R3K	Power 3-input N	NOR						3
Cel	Symbol			Pro	pagation D	elay Paran	neter	
		t O	JP VOI	t O		in KOLO	0000	Path
		0.413	KCL 0.072	0.200	KCL 0.023	KCL2 0.039	CDR2	A to X
		0.413	0.072	0.200	0.023	0.039	'	Alox
							1	
							1 1	
A4	_	į ·	}					
A1 ——— A2 ———	₽ <b>&gt;</b> —×							
A3	Ð							
		Paramete	er				Symbol	Typ (ns) *
						1		
						l		
	Input Loading	ĺ				ı		
Pin Name	Factor (lu)	]						
A	2							
		İ						
		1						
Pin Name	Output Driving Factor (lu)							
X	20							********************
			m values fo					
		The val		worst case	operating o	ondition are	given by the	maximum delay
								:
C10-R3K-E0	Sheet 1/1							Page 3-6

Cell Symbol  Cell Symbol  Cell Symbol  Tup Tropsgation Delay Parameter  Tup To KCL 10 KCL CDR2 Path  10 KCL 10 KCL CDR2 Path  0.775 0.227 0.288 0.051 0.073 4 A to X  Parameter  Parameter  Parameter  Symbol Typ (ns)*  Pin Name Input Leading Factor (lu)  A 1  Pin Name Output Driving Factor (lu)  X 6  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG10	" Version		
Cell Symbol    No   No   No   No   No   No   No   N	Cell Name	Function							Number of BC		
Pin Name Input Loading Factor (tu)  A 1  Pin Name Practor (tu)  A 1  Pin Name Substitute of the worst case operating condition are given by the maximum delay multiplier.	R4N	4-input NOR							2		
Pin Name Input Leading Factor (tu)  A 1  Pin Name Output Driving Factor (tu)  X 6  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	Cel	Symbol			Pro			neter			
Pin Name Input Leading Factor (tu)  A 1  Pin Name Factor (tu)  X 6  Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.					• • •			LCDDa	Path		
Pin Name Input Loading Factor (tu)  A 1  Pin Name Output Driving Factor (tu)  X 6  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									A to X		
Pin Name Output Driving Factor (lu)  X 6  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	A2 A3	<b>-</b> ×						Symbol	Typ (ns) *		
Plin Name Output Driving Factor (lu)  X 6  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10-R4N-E0 Sheet 1/1	Pin Name	Input Loading									
Pln Name Output Driving Factor (lu)  X  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10-R4N-E0 Sheet 1/1											
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10-R4N-E0   Sheet 1/1	A										
* Minimum values for the typical operating condition.  The values for the worst case operating condition are given by the maximum delay multiplier.  **C10-R4N-E0** Sheet 1/1**	Pin Name	Output Driving Factor (lu)									
210-R4N-E0   Sheet 1/1	^	•	The val	ues for the	r the typical worst case	operating o	condition.	given by th	e maximum delay		
C10-H4N-E0   Sheet 1/1											
	C10-R4N-E0	Sheet 1/1		-					Page 3-7		

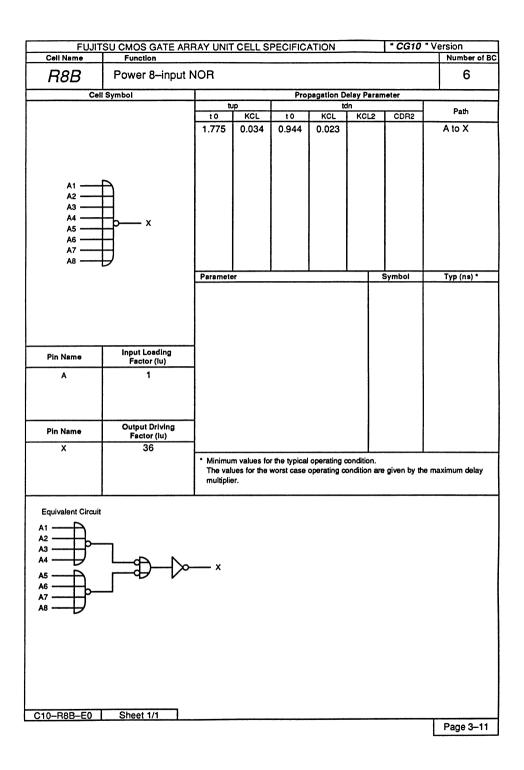
Cell Name Function Number of BC R4B Power 4-input NOR 4 Cell Symbol Propagation Delay Parameter tdn tup Path KCL2 | CDR2 t O KCL t O KCL 1.563 0.034 0.838 0.023 A to X Parameter Symbol Typ (ns) \* Input Loading Factor (lu) Pin Name Α **Output Driving** Pin Name Factor (lu) x 36 Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier. C10-R4B-E0 Sheet 1/1 Page 3-8

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION

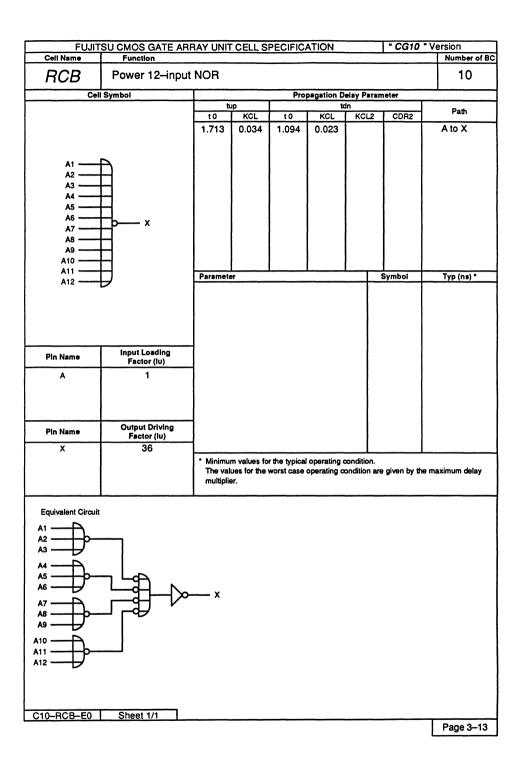
" CG10 " Version

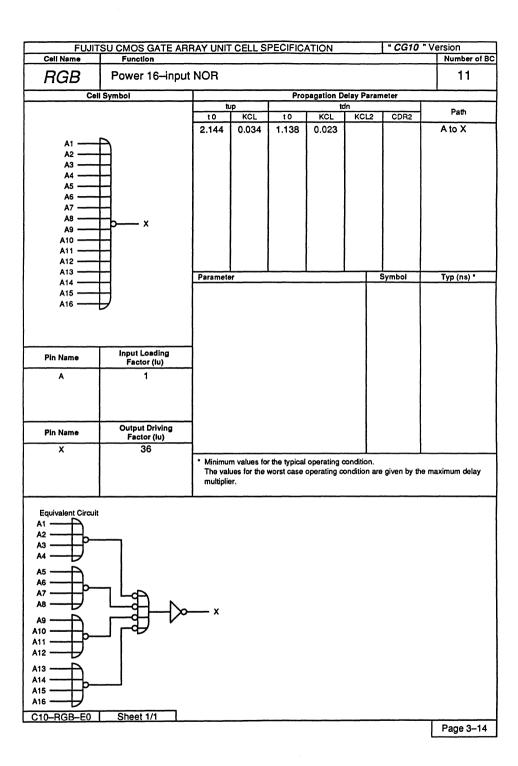
	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG10	" Version		
Cell Name	Function					····		Number of BC		
R4K	Power 4-input N	NOR						4		
Cell	Symbol			Pro	pagation D	elay Paran	neter			
		t O	IP KCL	t O	KCL	fn KCL2	CDR2	Path		
A1	A	0.675	0.097	0.219	0.017	0.028	7	A to X		
A2 A3 A4	A3 A4									
		Paramete					Symbol	Typ (ns) *		
Pin Name	Input Loading Factor (lu)									
Α	2									
Pin Name	Output Driving Factor (lu)									
x	12	* Minimus The val multiplie		the typical worst case	operating o	condition. ondition are	given by th	ne maximum delay		
C10-R4K-E0 ]	Sheet 1/1									
<u> </u>	Oncot I/1							Page 3-9		

FULL	CU 01400 04TF 4DF	2 437 1 15 117	0511.0	DEOLEIO	171011		1 " 0010 "	Varsian
Cell Name	SU CMOS GATE ARF	RAY UNII	CELLS	PECIFICA	ATION		" CG10 "	Number of BC
R6B	Power 6-input N	IOR				····		5
	l Symbol	Ι	neter					
			ıp		to	'n		Path
		1.406	0.034	t'0 0.925	KCL 0.023	KCL2	CDR2	A to X
Ì		1.400	0.004	0.525	0.020			
							1 1	
							1	
A1	A							
A2 ———	H							
A4	×							
A5	H						]	
A6	<del>D</del>							
		Paramete	r			<u> </u>	Symbol	Typ (ns) *
							· i	
		l						
						İ		
	Input Loading	1					1	
Pin Name	Factor (lu)	l						
A	1							
						-		
	Output Driving					1		
Pin Name	Factor (lu)							
×	36	Minimus		- at - a - ! !				
					operating o		given by the	maximum delay
		multiplie	er.					
	L .	I						
Equivalent Circuit								
A1 —								
A2	7 ~ ,							
A4 ——		x						
A5								
A6 ————————————————————————————————————								
C10-R6B-E0	Sheet 1/1							
			_					Page 3-10



FI	OLLOWOO OATE ADD	2427112117	0511.0	DEOLEIO	ATION		# CC10 "	Varaian	
Cell Name	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG10 " Version  Cell Name Function Number of BC								
R9B	Power 9-input N	IOR						8	
Cel	l Symbol			Pro	pagation D	elay Paran	neter		
		tı	Path						
		10	KCL	t0	KCL	KCL2	CDR2	A to X	
		1.556	0.034	1.050	0.023			AIOX	
							1		
A1	A						1 1		
A2									
A3	<b>H</b> .								
A4 ————————————————————————————————————	Б— х								
A6	Π ^								
A7	H								
A8									
A9	<del>-</del>	Paramete	er			<del>'                                    </del>	Symbol	Typ (ns) *	
								,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	
						- 1			
						Į.			
Pin Name	Input Loading Factor (Iu)								
A	1								
^	•								
	i '								
							l		
	Output Driving								
Pin Name	Factor (lu)					ļ			
×	36								
		* Minimu	n values for	the typical	operating o	xondition.	aiven by the	maximum delay	
}		multiplie		MO131 0430	operating o	oridition are	given by aid	maximom ociay	
		L							
Equivalent Circuit									
1 _									
A1									
A3 —									
A4 ————————————————————————————————————	L-&								
A5	<del>─</del> —ᠯ—ऻ≫	— x							
A6 ————————————————————————————————————									
A7 —	1								
A8									
A9 ————									
1									
1									
C10-R9B-E0	Sheet 1/1								
								Page 3-12	





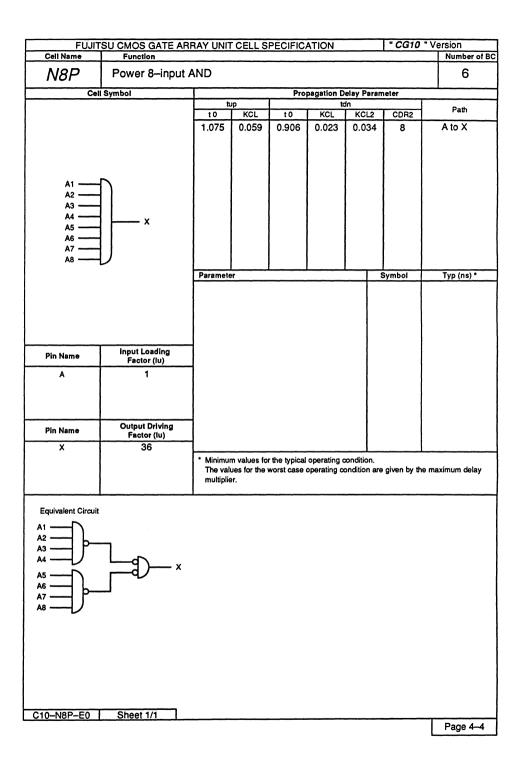
## **AND Family**

Page	Unit Cell Name	Function	Basic Cells
3-49	N2P	Power 2-input AND	2
3-50	N3P	Power 3-input AND	3
3–51	N4P	Power 4-input AND	3
3-52	N8P	Power 8-input AND	6

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION								" CG10 " Version		
Cell Name Function  N2P Power 2-input AND									Number of BC	
Cell Symbol Propagation Delay Parameter										
Con Cymbol		tup tdn					Path			
		t O	KCL	ťÒ	KCL	KCL2	CDR2	<u> </u>		
A1 X		0.631	0.034	0.538	0.023	0.034	7	ŀ	A to X	
							İ			
		Paramete	r				Symbol		Typ (ns) *	
Pin Name	Input Loading Factor (lu)									
Α	1					İ				
,,	'					l				
						ľ				
						l				
Pin Name	Output Driving Factor (lu)									
x	36	1								
	* Minimum values for the typical operating condition.									
	The values for the worst case operating condition are given by the maximu								ximum delay	
	multiplier.									
C10-N2P-E0	Sheet 1/1									
									Page 4-1	

	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG10 '	
Cell Name	Function							Number of BC
N3P	Power 3-input A	ND						3
Cel	Symbol			Proj	pagation D	elay Paran	eter	
			ıp			in	0000	Path
		t 0	KCL	10 0.000	KCL	KCL2	CDR2	A to X
		0.825	0.034	0.669	0.023	0.034	7	A IO A
A1	$\cap$							
A2	x							
А3 ——								
		Paramete	r				Symbol	Typ (ns) *
						- 1	İ	
						- 1		
							1	
		ĺ				1	Ì	
		}				i	1	
Pin Name	Input Loading Factor (lu)					- 1	l	
Α	1					- 1	ł	
	·						l	
						1	Ì	
							ı	
Pin Name	Output Driving					1	1	
	Factor (lu)					l	l	
x	36						L	
		* Minimu	m values for	the typical	operating o	xondition.	aiven hy the	maximum delay
		multiplie		1013t Case 1	operating of	ondition are	givein by and	maximum delay
		L						
C10-N3P-E0	Sheet 1/1							Dans 4 C
								Page 4-2

Cell Symbol  Cell Symbol  Propagation Delay Parameter    10   KCL   10   KCL   CDR2   Path				CELLS		111011			" Version
Cell Symbol  tup toth KCL 10 KCL COR2 Path  0.988 0.034 0.744 0.023 0.034 8 A to X  Parameter Symbol Typ (na)*  Pin Name Input Loading Factor (tu)  A 1  Pin Name Output Driving Factor (tu)  **Name Parameter Factor (tu)  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Typ (na)**  **Name Parameter Symbol Ty	NIAD			·					Number of
Parameter  Parameter  Parameter  Parameter  Parameter  Parameter  Parameter  Parameter  Symbol Typ (na)*  Typ (na)*  Pin Name Parameter  A 1  Pin Name Output Driving Factor (tu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.	114	Power 4-input	AND						3
Pin Name Input Loading Pactor (Iu)  A 1  Pin Name Output Driving Factor (Iu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delar multiplier.	Cell	Symbol	T		Pro	pagation D	elay Paran	neter	
Pin Name Input Loading Factor (lu)  A 1  Pin Name Output Driving Factor (lu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.									Path
Pin Name Input Loading Factor (lu)  A 1  Pin Name Output Driving Factor (tu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.									
Pin Name Input Loading Factor (tu)  A 1  Pin Name Cutput Driving Factor (tu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.			0.988	0.034	0.744	0.023	0.034	8	AIOX
Pin Name Input Loading Factor (tu)  A 1  Pin Name Cutput Driving Factor (tu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.			l	l	i	Ì		1	
Pin Name Input Loading Factor (tu)  A 1  Pin Name Cutput Driving Factor (tu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.			i		1				
Pin Name Input Loading Factor (tu)  A 1  Pin Name Cutput Driving Factor (tu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.					1	1	{		
Pin Name Input Loading Factor (tu)  A 1  Pin Name Cutput Driving Factor (tu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.						1	[		
Pin Name Input Loading Pactor (lu)  A 1  Pin Name Pactor (lu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.		D	1		}		ļ		
Pin Name Input Loading Pactor (lu)  A 1  Pin Name Pector (lu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delements of the worst case operating condition are given by the maximum delements.		x				i			
Pin Name Input Loading Factor (Iu)  A 1  Pin Name Output Driving Factor (Iu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.		)		l		ŀ			
Pin Name Input Loading Factor (Iu)  A 1  Pin Name Output Driving Factor (Iu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.						ł	1		
Pin Name Input Loading Factor (Iu)  A 1  Pin Name Output Driving Factor (Iu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.			<u> </u>						
Pin Name Coutput Driving Factor (Iu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.			Paramete	er				Symbol	Typ (ns) *
Pin Name Coutput Driving Factor (Iu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.									
Pin Name Coutput Driving Factor (Iu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.			]						
Pin Name Coutput Driving Factor (Iu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.			1						
Pin Name Coutput Driving Factor (Iu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.									
Pin Name Output Driving Factor (lu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.	Pin Name	Input Loading	1						
Pin Name Pactor (lu)  X  36  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.			4						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.	A	1					- 1		
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.									
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum dela multiplier.							- 1		
Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delamultiplier.  * Minimum values for the typical operating condition are given by the maximum delamultiplier.  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delamultiplier.	Pin Name	Output Driving	1						
Minimum values for the typical operating condition.     The values for the worst case operating condition are given by the maximum delamultiplier.      Minimum values for the typical operating condition are given by the maximum delamultiplier.			4				- 1		
The values for the worst case operating condition are given by the maximum dela multiplier.	^	30	Minimus	m values fo	r the typical	operating (	condition		
			The val	ues for the				given by th	e maximum delay
0-N4P-E0   Sheet 1/1			multiplie	er.					
0-N4P-E0   Sheet 1/1									
0-N4P-E0   Sheet 1/1									
0-N4P-E0   Sheet 1/1									
0-N4P-E0   Sheet 1/1									
0-N4P-E0   Sheet 1/1									
0-N4P-E0   Sheet 1/1									
0-N4P-E0   Sheet 1/1									
0-N4P-E0   Sheet 1/1									
0-N4P-E0   Sheet 1/1									
0-N4P-E0   Sheet 1/1									
0-N4P-E0   Sheet 1/1									
0-N4P-E0   Sheet 1/1									
0-N4P-E0   Sheet 1/1									
0-N4P-E0   Sheet 1/1									
0-N4P-E0 I Sheet 1/1 I									
	10-N4P-E0	Sheet 1/1							Page 4-3



#### **OR Family**

Page	Unit Celi Name	Function	Basic Cells
3–55	R2P	Power 2-input OR	2
3–56	R3P	Power 3-input OR	3
3–57	R4P	Power 4-input OR	3
3-58	R8P	Power 8-input OR	6

3

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL SI	PECIFICA	ATION		" CG10	" Version
Cell Name	Function							Number of B
R2P	Power 2-input 0	OR						2
Cell	Symbol	T		Pro	pagation D	elay Paran	neter	
			ıp .			dn		Path
		t O	KCL	t O	KCL	KCL2	CDR2	
		0.488	0.034	0.713	0.028	0.039	8	A to X
A1 A2	<b>)</b> —×	Paramete	er				Symbol	Typ (ns) *
		1						
Pin Name	Input Loading Factor (lu)	]						
A	1					-	ĺ	
Pin Name	Output Driving Factor (lu)							
х	36					L_		
							given by th	e maximum delay
010-R2P-E0	Sheet 1/1	and the second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second s						Page 5-1

EIIIIT	SU CMOS GATE ARE	TIMIT VAS	CELLS	PECIFIC	ATION		" CG10 "	Version
Cell Name	Function	ICT OINT	JLLL S	LOIFIU	TION		, 53,5	Number of BC
R3P	Power 3-input C	R						3
Cel	Symbol			Pro	pagation D		neter	
			IP KCI	• 6		tn KCI3	CDB2	Path
A1 ——— A2 ——— A3 ———	<b>)</b> —×	0.563	0.034	1.150	0.034	0.045	8	A to X
		Paramete	7			<u>'                                    </u>	Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)						1	
A	1 Output Driving							
Pin Name	Factor (lu)					- 1	1	
x	36		ues for the		operating o		given by the	maximum delay
C10-R3P-E0	Sheet 1/1							1 5: 5 6
								Page 5-2

Power 4-input OR	FILIT	SU CMOS GATE ARE	TIMI VAS	CELLS	PECIFICA	ATION		" CG10	" Version
Cell Symbol  To KCL to KCL2 CDR2  Path  10 KCL 10 KCL2 CDR2  Path  1.575 0.039 0.056 8 A to X  Parameter  Parameter  Parameter  Symbol Typ (na)*  Typ (na)*  Pin Name Input Loading Factor (tu)  A 1  Pin Name Factor (tu)  X 36  *Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	Cell Name	Function	IAT ONT	OLLE G	LOI 107	411014		00.0	Number of BC
Pin Name   Input Loading Factor (lu)   X   36   Minimum values for the typical operating condition are given by the maximum delay multiplier.	R4P	Power 4-input C	OR						3
Pln Name Input Leading Factor (lu)  A 1  Pln Name Output Driving Factor (lu)  X 36  Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10_R4P_E0 Sheet 1/1	Cell	Symbol			Proj			neter	
Pin Name Input Loading Pactor (tu)  A 1  Pin Name Output Driving Factor (tu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.					10			CDDO	Path
Pin Name Input Leading Factor (tu) A 1  Pin Name Output Driving Pactor (tu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10-R4P-E0 Sheet 1/1									A to Y
Pin Name Output Driving Factor (lu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10-R4P-E0 Sheet 1/1	A2 —— A3 ——	×							
Pin Name Output Driving Factor (tu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10-R4P-E0  Sheet 1/1	Pin Name	Input Loading							
Pin Name Output Driving X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10-R4P-E0 Sheet 1/1			1						
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  **C10-R4P-E0** Sheet 1/1									
Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10—R4P—E0 Sheet 1/1	Pin Name	Factor (lu)					j		
C10-R4P-E0   Sheet 1/1			The val	ues for the v	the typical worst case	operating o	condition. ondition are	given by th	ne maximum delay
010 1141 20 1 011000 111	C10_B4P_F0 \	Sheet 1/1							
I Page 5–3	<u> </u>	Oneet I/1							Page 5-3

511117	SU CMOS GATE AR	DAV LINIT	CELLO	DECIEIC	ATION		" CG10	" Version
Cell Name	Function Function	HAT UNI	CELL 3	FECIFIC/	ATION		Caro	Number of BC
R8P	Power 8-input (	OR						6
Cel	l Symbol							
1			KCL	t O	KCL	dn L KCIO	CDR2	Path
		0.613	0.034	1.675	0.045	0.056	8	A to X
A1 ————————————————————————————————————	×	Paramete					Symbol	Typ (ns) *
Pin Name	Input Loading							
	Factor (lu)	┨				l	1	
Pin Name	Output Driving Factor (Iu) 36			r the typical				
		The vali multiplie		worst case	operating o	ondition are	given by the	maximum delay
Equivalent Circuit A1 A2 A3 A4 A5 A6 A7 A8	×							
C10-R8P-E0	Sheet 1/1							
								Page 5-4

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#### **EXNOR/EXOR Family**

Page	Unit Cell Name	Function	Basic Cells
3–61	X1N	Exclusive NOR	3
3–62	X1B	Power Exclusive NOR	4
3–63	X2N	Exclusive OR	3
3-64	X2B	Power Exclusive OR	4
365	X3N	3-input Exclusive NOR	5
3–66	ХЗВ	Power 3-input Exclusive NOR	6
3-67	X4N	3-input Exclusive OR	5
3-68	X4B	Power 3-input Exclusive OR	6

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG10	* Version
Cell Name	Function							Number of BC
X1N	Exclusive NOR							3
Cel	Symbol			Pro	pagation D	elay Paran	neter	
			JP 1401			in		Path
		t 0 0.725	KCL 0.122	0.600	0.073	0.090	CDR2	A to X
A1 ————————————————————————————————————	<b>₽</b>							
		Paramete	er				Symbol	Typ (ns) *
	I land to the							
Pin Name	input Loading Factor (lu)					-		
A	2							
	Output Driving							
Pin Name	Factor (lu)							
X	18						given by th	e maximum delay
Equivalent Circuit				Function	on Table			
A1				Ir	puts (	Output		
~ TTV	<u></u>	×		A1	A2	х		
		^		н	н	Н		
				L	н	L		
				Н	L	L		
				L	L	Н		
					·			
C10-X1N-E0	Sheet 1/1							
								Page 6-1

Cell Name   Function   Propagation Delay Parameter	FILIIT	SU CMOS GATE ARE	RAY LINIT	CELLS	PECIFIC	ATION		" CG10	" Version
Cell Symbol  Tup  Tup  To KCL  10 KCL  10 KCL  0.931  0.034  1.106  0.028  0.051  7  A to X   Parameter  Propagation Delay Parameter  ton  To KCL  0.028  0.051  7  A to X   Parameter  Propagation Delay Parameter  To KCL  COR2  Path  A to X  Parameter  Symbol  Typ (ne)  Pin Name  Propagation Delay Parameter  To KCL  COR2  Path  A to X  Parameter  Symbol  Typ (ne)  Propagation Delay Parameter  To Color  To Color  Path  A to X  Parameter  Symbol  Typ (ne)  Propagation Delay Parameter  To Color  Path  A to X  Parameter  Symbol  Typ (ne)  Propagation Delay Parameter  To Color  Path  A to X  Parameter  Symbol  Typ (ne)  Propagation Delay Parameter  To Color  Path  A to X  Parameter  Symbol  Typ (ne)  Propagation Delay Parameter  To Color  Path  A to X  Parameter  Symbol  Typ (ne)  Propagation Delay Parameter  To Color  Path  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X  A to X	Cell Name		OINI	OLLL O	2011 107				Number of BC
Pin Name Input Loading Factor (tu)  X  Pin Name Coutput Driving Factor (tu)  X  36  Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum de multiplier.  Equivalent Circuit  Function Table  Input Loading Factor (tu)  X  A1  A2  Path  Input Loading Factor (tu)  X  A1  A2  Function Table  Inputs  Output  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A1  A2  A3  A4  A4  A4  A4  A4  A4  A4  A4  A4	X1B	Power Exclusive	NOR						4
Pin Name Input Loading Factor (tu)  A 2  Pin Name Practor (tu)  A 2  - Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum de multiplier.  Equivalent Circuit  A1 A2 X  H H H H  L H L  H L  H L  H L  H L	Cell	Symbol			Pro			neter	
Plin Name Input Loading Factor (tu)  A 2  Plin Name Practor (tu)  X 36  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum de multiplier.  Function Table    Input Coding Factor (tu)					10			CDB2	Path
Pin Name Input Loading Factor (lu)  A 2  Pin Name Output Driving Factor (lu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum de multiplier.  Equivalent Circuit  A1 A2 X  H H H H  L H L  H L  H L  H L  H L									A to X
Pin Name  Factor (lu)  A  2  Pin Name  Output Driving Factor (lu)  X  36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum de multiplier.  Equivalent Circuit  Function Table  Inputs Output A1  A2  X  H  H  H  L  H  L  H  L  H  L  H  L	l i	<b>&gt;</b> —×	Paramete	of .				Symbol	Typ (ns) °
Pin Name  Pin Name  Pin Name  Output Driving Factor (iu)  X  36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum de multiplier.  Equivalent Circuit  Function Table  Inputs Output A1 A2 X H H H H L H L H L H L H L H L H L H L H	Din Name	Input Loading							
Pin Name Output Driving Factor (Iu)  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum de multiplier.  Equivalent Circuit  Function Table  inputs Output A1									
A1	Pin Name	Output Driving Factor (lu)	The val	ues for the v	the typical	operating o	condition.	e given by the	e maximum delay
A1	Familyada a Ciramia				Firmati	aa Tabla			
A2 X H H H L H L H L L									
X H H H L L H L L									
L H L H L L			<b>&gt;</b>	· x	<u> </u>	+			
H L L	L	$$ $\mathcal{V}$	•			++			
					<b> </b>	+	<del></del>		
					ļ				
					لــــٰـ	لــــــــــــــــــــــــــــــــــــــ	لــــــ		
0.0 240 50 1 01 01 01	010 VID 50 1	01							
C10–X1B–E0 Sheet 1/1 Page 6	C10-X1B-E0	Sneet 1/1							Page 6–2

FILLET	CH ONOC CATE ADD	AV LIAUT	OFIL O	סבסובוס	ATION		L * CC10	* Version
Cell Name	SU CMOS GATE ARF	TAY UNII	CELLS	PECIFICA	ATION		CGIO	Number of BC
X2N	Exclusive OR							3
Cel	Symbol			Pro	pagation D		neter	
		10	IP KCL	i O	KCL	In KCL2	CDR2	Path
		0.694	0.122	0.731	0.073	0.090	4	A to X
A1 ————————————————————————————————————	<b>)</b> —×	Paramete	er				Symbol	Typ (ns) °
Pin Name A	Input Loading Factor (lu) 2							
Pin Name	Output Driving Factor (Iu) 14							
			ues for the v		operating o		given by the	e maximum delay
Equivalent Circuit				Function	on Table			
A1 -10-				In	puts C	Output		
A2 + 16°				A1	A2	×		
	——\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	· X		Н	н	L		
L	——D			L	Н	Н		
				Н	L	Н		
				1	1.1			
				<u> </u>				
C10-X2N-E0	Sheet 1/1							T Boss 6 C
								Page 6-3

EII III	SU CMOS GATE ARF	DAV LINIT	CELLE	DECIFIC	ATION		" CG10	" Version
Cell Name	Function	TAT UNI	CELL S	PECIFICA	TION		- CG10	Number of BC
X2B	Power Exclusive	OR						4
Cel	Symbol			Pro		elay Paran	eter	
		t O	KCL	t O	KCL	in KCL2	CDR2	Path
		0.894	0.034	1.025	0.028	0.039	7	A to X
A1 ————————————————————————————————————	<b>)</b> —×	Paramete	or .				Symbol	Typ (ns) °
Pin Name	Input Loading							
	Factor (lu)					1		
A	2					-		
Pin Name	Output Driving Factor (lu)							
×	36						ŀ	
^	55	Minimul     The val     multiplie		r the typical worst case	operating o	condition.	given by the	maximum delay
Equivalent Circuit				Function	on Table			
A1 — C					<del></del>			
A2 + D	7 .					Output		
<u> </u>	<b>─ ─ ─ ─</b>	<b>&gt;</b> —	· x	A1	A2	×		
	\\rightarrow\'	•		H	H	-		
				<u> </u>	<del>                                     </del>	<del>                                      </del>		
				Н.	L	<u> </u>		
				L	<u> </u>			
1								
}								
C10-X2B-E0	Sheet 1/1							
								Page 6-4

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL SI	PECIFICA	TION		"	CG10	" Version
Cell Name	Function								Number of BC
X3N	3-input Exclusiv	e NOR							5
Cel	l Symbol	l		Prop	agation		aramet	er	
		t O	JP KCL	tdn t0 KCL KCL2 CDR2		CDR2	Path		
		1.700	0.122	1.450	0.073	0.0		4	A to X
						"		•	
							l		
		l				1			
	_						l		
A1 ————————————————————————————————————	<b>₽</b>								
A3 —	)								
•	_								
		Paramete	er				Syr	nbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)							1	
Α	2						l		
	Output Driving								
Pin Name	Factor (lu)								
X	18	* Minimu	m values for	the typical	operating	condition	on.		
		The val	ues for the v					ven by th	e maximum delay
		multiplie	er.						
Equivalent Circuit				Function	n Table				
A2 —					Inputs		Output	1	
A3 —				A1	A2	A3	X	1	
A1	<b>Њ</b> ⊶			Н	H	н	L	1	
01				Н	н	L	н	1	
				Н	L	н	н	1	
				н		L	L	1	
				L	Н	Н	Н	1	
				L	Н	L	L		
				L	L	н	L	1	
				L	L	L	Н		
				L	<u> </u>		l	1	
C10-X3N-E0	Sheet 1/1								Page 6 F
									Page 6-5

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELLS	PECIFICA	ATION		T	" CG10	" V	ersion
Cell Name	Function									Number of BC
X3B	Power 3-input E	Exclusive	NOR							6
Cel	Symbol	Propagation Delay Parameter								
		t O	KCL	t O	KCL	dn KC	12	CDR2	-	Path
		1.650	0.034	2.119	0.028	0.0		7	<u> </u>	A to X
A1 ————————————————————————————————————										
						<u> </u>			_	
		Paramete	r				S	mbol	<del> </del>	Typ (ns) *
Pin Name	Input Loading Factor (lu)									
A	2									
Pin Name	Output Driving Factor (lu)									
X	36		ues for the	r the typical worst case				given by th	l	aximum delay
Equivalent Circuit				Function	on Table					
A <sup>2</sup> ————————————————————————————————————					Inputs		Outpo	ıt .		
~	10 1			A1	A2	АЗ	х			
A1	#D > ×			н	Н	н	L			
	- ·			н	н	L	н			
				Н	L	н	Н			
				Н	L	L	L			
				L	Н	н	Н	7		
				ī	Н	L	L	7		
				L	L	Н	L	1		
				L	L	L	н	7		
				•						
C10-X3B-E0	Sheet 1/1								Т	Page 6-6

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELL S	PECIFICA	ATION			" CG10	" Version
Cell Name	Function								Number of BC
X4N	3-input Exclusiv	e OR			pagation				5
Cel	l Symbol								
		t O	IP KCL	t O	KCL	tdn KC	L2	CDR2	Path
		1.763	0.122	1.581	0.073	0.0		4	A to X
A1 ————————————————————————————————————	<b>)</b> —×	Paramete	·r				Sy	mbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)								
Α	2								
Pin Name	Output Driving Factor (lu)								
		* Minimur The valu multiplie		the typical worst case o	operating operating	condition condition	on. on are g	iven by th	e maximum delay
Equivalent Circuit				Function	on Table				
A2 A3					Inputs		Outpu	t	
~ -10	10			A1	A2	А3	х		
A1	#D×			н	н	н	н		
				Н	Н	L	L	7	
				н	L	н	L	1	
				Н	L.	L	Н	1	
				-	Н	н	L	1	
				L	н	L	н	1	
				1		Н	Н	1	
					L	L	L	_	
C10-X4N-E0	05-144								
FIN VAN LA	Sheet 1/1								

FILIT	SU CMOS GATE ARF	PAV LINIT	CELLS	PECIFIC	ATION			" CG10 "	Version
Cell Name	Function	TAT OIVIT	OLLLO	LOII 107	THOIT			00.0	Number of BC
X4B	Power 3-input E	Exclusive	e OR						6
Cel	l Symbol		ter						
		t O	KCL	t O	KCL	dn KC	12 1	CDR2	Path
		1.544	0.034	1.956	0.028	0.0		7	A to X
A1	A								
A2 A3	×								
		Paramete	er				S	mbol	Typ (ns) *
	,								
Pin Name	Input Loading Factor (lu)								
A	2								
Pin Name	Output Driving Factor (lu)								
X	36	* Minimu The val multiplie	ues for the	r the typical worst case	operating o	condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condition condit	on. on are (	given by the	maximum delay
Equivalent Circuit				Function	on Table				
A2					Inputs		Outpu	ıt	
A3 — 11	10 ,			A1	A2	АЗ	X		
A1	# <b>&gt;</b>	×		Н	Н	Н	Н		
				Н	Н	L	L		
				Н	L	Н	L		
				Н	L	L	Н	]	
				L	Н	Н	L		
				L	н	L	н		
				L	L	н	н	4	
				L	L	L	L		
C10-X4B-E0	Sheet 1/1								<del></del>
									Page 6–8

# AND-OR-Inverter Family (AOI)

Page	Unit Cell Name	Function	Basic Cells
3–71	D23	2-wide 2-AND 3-input AOI	2
3–72	D14	2-wide 3-AND 4-input AOI	2
3-73	D24	2-wide 2-AND 4-input AOI	2
3-74	D34	3-wide 2-AND 4-input AOI	2
3-75	D36	3-wide 2-AND 6-input AOI	3
3-76	D44	2-wide 2-OR 2-AND 4-input AOI	2

ELLIIT	SHICKOS CATE ADS	DAV LIAIT	CELL C	DECIFIC	ATION		" CG10	" Version
Cell Name	SU CMOS GATE ARE	TAT UNII	CELL SI	PECIFICA	ATION		CG10	Number of BC
D23	2-wide 2-AND	3—input	AOI					2
Cell	Symbol			Pro		elay Param	eter	
			KCL	t O	KCL	MCL2	CDBs	Path
		0.456	0.122	0.425	0.079	ROLZ	CDR2	A to X
		0.231	0.093	0.231	0.051	0.067	4	B to X
			!			[		
						1		
A1 —								
Ã2	. Ar							
В ———	×							
				,		1		
	i	Paramete	er				Symbol	Typ (ns) *
						1		
	Input Loading					- 1		
Pin Name	Factor (lu)					İ		
A B	1							
В	1							
						İ		
Pin Name	Output Driving Factor (lu)							
х	14							
		* Minimu	n values for	the typical	operating o	condition.		
		The vale multiplie		worst case	operating o	ondition are	given by th	e maximum delay
		Шапарие						
C10-D23-E0	Sheet 1/1							Dec. 7.4
								Page 7-1

FILIT	SU CMOS GATE ARE	DAV HAH	CELLS	DECIEIC	ATION		" CG10 "	Version
Cell Name	Function	TAT UNI	CELLS	FECIFICA	ATION		Caro	Number of BC
D14	2-wide 3-AND	4–input	AOI					2
Cel	Symbol							
		tup tdn  10 KCL 10 KCL KCL2				CDR2	Path	
		0.563	0.122	0.438	0.107	0.118	4	A to X
		0.200	0.084	0.225	0.051	0.067	4	B to X
		1						
						ŀ		
					İ			
A1 —		l		l			]	
A2	7							
A3 ——					ĺ			
В	×				}			
	D					1		
				<u> </u>	<u> </u>	<u> </u>		
		Paramete	er			<del></del>	Symbol	Typ (ns) *
		İ						
		1						
Pin Name	Input Loading Factor (lu)							
<b></b>							l	
A B	1						ļ l	
		l					1	
Pin Name	Output Driving	1					İ	
×	Factor (lu)	-					1	
^	14	• Minimu	m values fo	r the typical	operating	condition		
		The val	ues for the				given by the	maximum delay
		multipli	er.					
	L	<u> </u>						
C10-D14-E0	Sheet 1/1							Page 7-2
								1 aye 1-2

FILIIT	SU CMOS GATE AR	RAY LINIT	CELLS	PECIFICA	ATION		" CG10	" Version
Cell Name	Function	TATE OITH	OLLLO	2011 107	THOIT			Number of BC
D24	2-wide 2-AND	4-input	AOI					2
	l I Symbol	T		Pro	pagation D	elay Paran	neter	
			ıb		to	In		Path
		10	KCL	t 0	KCL	KCL2	CDR2	
		0.338	0.093	0.388 0.519	0.079 0.079			A to X B to X
A1)	7 ~							
	×							
B1)	J 1							
		Paramete	er				Symbol	Typ (ns) *
		1						
		1						
		1						
	r	4						
Pin Name	Input Loading Factor (lu)							
A B	1	1						
В	1					l		
		4						
Pin Name	Output Driving Factor (lu)					l		
X	14					L		
		* Minimur	m values for	the typical	operating o	ondition.	airea bu sh	a mavimum dalau
		multiplie		worst case (	operating o	oncition are	given by in	e maximum delay
		<u> </u>						
C10-D24-E0	Sheet 1/1							Page 7–3

D34   3-wide 2-AND 4-input AOI	Path A to X B to X
Cell Symbol   Propagation Delay Parameter   tup   tdn	Path A to X
tup tdn  10 KCL 10 KCL KCL2 CDR2  0.719 0.172 0.456 0.084	A to X
0.719 0.172 0.456 0.084 0.084	A to X
0.719   0.172   0.456   0.084   7	
0.388 0.147 0.269 0.051 0.067 4	
$\begin{vmatrix} A_1 \\ A_2 \end{vmatrix} \rightarrow \begin{vmatrix} A_1 \\ A_2 \end{vmatrix} \rightarrow \begin{vmatrix} A_1 \\ A_2 \end{vmatrix} \rightarrow \begin{vmatrix} A_1 \\ A_2 \end{vmatrix} \rightarrow \begin{vmatrix} A_1 \\ A_2 \end{vmatrix} \rightarrow \begin{vmatrix} A_1 \\ A_2 \end{vmatrix} \rightarrow \begin{vmatrix} A_1 \\ A_2 \end{vmatrix} \rightarrow \begin{vmatrix} A_1 \\ A_2 \end{vmatrix} \rightarrow \begin{vmatrix} A_1 \\ A_2 \end{vmatrix} \rightarrow \begin{vmatrix} A_1 \\ A_2 \end{vmatrix} \rightarrow \begin{vmatrix} A_1 \\ A_2 \end{vmatrix} \rightarrow \begin{vmatrix} A_1 \\ A_2 \end{vmatrix} \rightarrow \begin{vmatrix} A_1 \\ A_2 \end{vmatrix} \rightarrow \begin{vmatrix} A_1 \\ A_2 \end{vmatrix} \rightarrow \begin{vmatrix} A_1 \\ A_2 \end{vmatrix} \rightarrow \begin{vmatrix} A_1 \\ A_2 \end{vmatrix} \rightarrow \begin{vmatrix} A_1 \\ A_2 \end{vmatrix} \rightarrow \begin{vmatrix} A_1 \\ A_2 \end{vmatrix} \rightarrow \begin{vmatrix} A_1 \\ A_2 \end{vmatrix} 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B1	
B2 ————————————————————————————————————	
Parameter Symbol	Typ (ns) *
Pin Name Input Loading	
Pactor (IU)	
A 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Dia Name Output Driving	
Factor (lu)	
x 10	
Minimum values for the typical operating condition.  The values for the worst case operating condition are given by the maximum.	imum delav
multiplier.	
C10-D34-E0   Sheet 1/1	
	Page 7-4

							I :: 0010	
Cell Name	SU CMOS GATE ARF	RAY UNII	CELLS	PECIFICA	ATION		" CG10	" Version Number of BC
D36	3-wide 2-AND	6-input	AOI					3
Cell	Symbol			neter				
		t O	KCL	t O	KCL	In KCL2	CDR2	Path
		0.481	0.118	0.450	0.079	KOL	ODINE	A to X
		0.613	0.118	0.544	0.079			B to X
		0.731	0.118	0.638	0.079			C to X
A1	٦							
B1 —	4							
B2	×							
C1 —	]							
C2 —		Paramete	er			L	Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)							
A B	1					l		
С	1							
Pin Name	Output Driving							
X	Factor (lu)							
	-	* Minimur	n values for	the typical	operating o	condition.	aiven by th	e maximum delay
		multiplie		WO131 C030	operating of	orionion are	given by an	o maximum odiay
C10 D26 E0 1	Chaot 1/1							
C10-D36-E0	Sheet 1/1							Page 7-5

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELLS	PECIFIC	ATION		" CG10	" Version			
Cell Name	Function	Function									
D44	2-wide 2-OR 2-	-AND 4	–input A	OI				2			
Cel	Symbol			Pro	pagation D		eter				
		t O	KCL	t O	KCL	in KCL2	CDR2	Path			
		0.650 0.644 0.619	0.172 0.172 0.172 0.122	0.488 0.400 0.300	0.079 0.079 0.051	0.062	4	A to X B to X C to X			
A1 A2 B C	<u>Dr</u> b—×										
		Paramete	er		L	٦ :	Symbol	Typ (ns) *			
Pin Name	Input Loading Factor (lu)										
A B C	1 1										
Pin Name	Output Driving Factor (lu)										
×	10	* Minimui The vali multiplie		r the typical worst case	operating o	condition. condition are	given by th	e maximum delay			
C10-D44-E0	Sheet 1/1			······································				Page 7–6			

# OR-AND-Inverter Family (OAI)

	Unit Cell		Basic
Page	Name	Function	Cells
3–79	G23	2-wide 2-OR 3-input OAI	2
3-80	G14	2-wide 3-OR 4-input OAI	2
3–81	G24	2-wide 2-OR 4-input OAI	2
3-82	G34	3-wide 2-OR 4-input OAI	2
3-83	G44	2-wide 2-AND 2-OR 4-input OAI	2

FILUT	SU CMOS GATE ARF	TIMIT VAS	CELLS	PECIFIC	ATION		" CG10	* Version
Cell Name	Function	TAT OIT	OLLLO	2011 107	111011		1	Number of BC
G23	2-wide 2-OR 3-	2						
Cell	Symbol							
		tup tdn tdn t0 KCL KCL2 CDR2						Path
A1	Чъ— ×	0.450 0.175	0.122 0.067	0.344 0.344	0.079 0.079			A to X B to X
В		i	!					
		Paramete	<u></u>		L	L	Symbol	Typ (ns) *
Pin Name	input Loading Factor (lu)							
A B	1							
Pin Name	Output Driving Factor (Iu)							
X								
242 222 52	Observed							
C10-G23-E0	Sheet 1/1							Page 8-1

Cell Name	SU CMOS GATE ARI	" CG10 " \	Version Number of BC						
	Function								
G14	2-wide 3-OR 4	2							
	l Symbol	neter							
		t	Path						
		t O	KCL	t O	KCL	KCL2	CDR2		
		0.750	0.177	0.406	0.079			A to X	
		0.156	0.067	0.406	0.079	l		B to X	
		ļ	1			}			
						l			
		Ì	1			l			
A1 ——		ļ	l						
A2	٦								
A3 ————						1			
В ———	Ыр— ×	1	l .						
8	$\neg \nu$	1					<u> </u>		
}		Paramete	<b>∍</b> r				Symbol	Typ (ns) *	
		l							
		l							
1									
1		1							
	Input Loading	ł				- 1			
Pin Name	Factor (lu)	l							
A B	1	1				1			
В	1	ł				- 1			
		l				ı			
Pin Name	Output Driving	1				1			
	Factor (lu)	4					ļ		
×	10	Minimu		- the history					
			m values to ues for the	worst case	operating of operating of operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating of the operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operating operat	ondition are	given by the r	naximum delay	
		multiplier.							
	L	l							
1									
1									
1									
C10-G14-E0	Sheet 1/1								
								Page 8-2	
								L	

ELLUT	SU CMOS GATE ADI	DAV HAH	CELLS	DECIEIC	ATION		" CG10	" V4	reion
Cell Name	Function	E ARRAY UNIT CELL SPECIFICATION "CG10"							
G24	2-wide 2-OR 4	2-wide 2-OR 4-input OAI							
Cell	Symbol	Propagation Delay Parameter							
	10	IP KCL	KCL	fn KCL2 CDR2			Path		
		0.313	0.122	t 0 0.438	0.079	11022	90.112		A to X
		0.563	0.122	0.375	0.079				B to X
		i							
A1 ——	_								
A2 -	у—×						i		
В1 ——	راب ^ السرام								
B2 —	-								
		Paramete	я				Symbol		Typ (ns) *
						1			
Pin Name	Input Loading Factor (lu)								
Α									
A B	1					- 1			
		4							
Pin Name	Output Driving Factor (lu)								
×	10								
		Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay.							
		multiplie		WOIST CASE	operating o	JI MILION WE	given by un		Almoni Golay
		<u> </u>							
C10-G24-E0	Sheet 1/1								
									Page 8-3

FILIT	SH CMOS CATE AD	DAV LINIT	CELLS	DECIFIC	ATION		" CG10 "	Version	
Cell Name	SU CMOS GATE ARI	0010	Number of BC						
G34	3-wide 2-OR 4		2						
Cel	Symbol		Propagation Delay Parameter						
		t O	KCL	t O	KCL	in KCL2	CDR2	Path	
		0.594	0.122	0.438	0.107		00.12	A to X	
		0.438	0.080	0.281	0.090			B to X	
		l							
A1	7								
A2 ————	4								
B1	þ×	1							
B2	<del>-</del> -D	İ							
		Paramete	<u> </u>				Symbol	Typ (ns) *	
		İ							
	Input Loading	1							
Pin Name	Factor (lu)	]				l	l		
A B	1	İ							
	•	ļ							
Din Name	Output Driving	1							
Pin Name	Factor (lu)	4							
×	10	Minimu	m values fo	r the typical	operating of	condition.			
		The val	ues for the	worst case	operating o	ondition are	given by the r	naximum delay	
		multiplie	er.						
			***************************************						
C10-G34-E0	Sheet 1/1								
								Page 8-4	

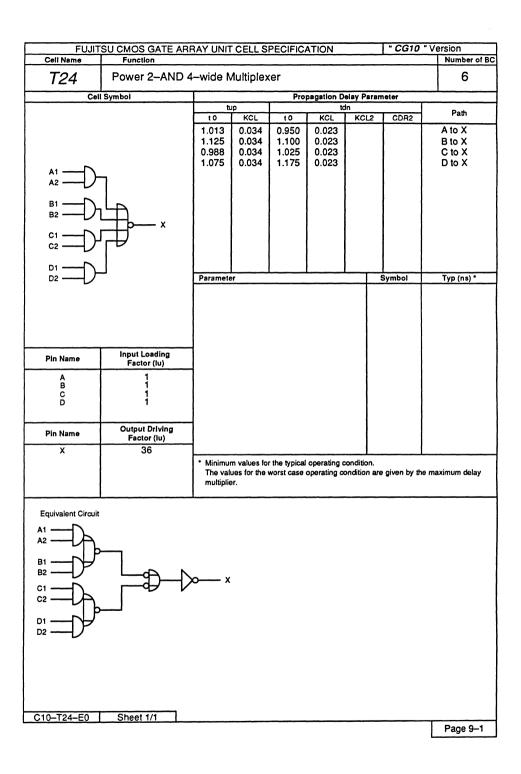
FILIIT	SU CMOS GATE ARF	RAY LINIT	CELLS	PECIFICA	ATION		" CG10	" Version
Cell Name	Function	711 01111		2011 107			1	Number of BC
G44	2-wide 2-AND	2						
Cell	Symbol							
		tup tdn tdn t0 KCL KCL2 CDR						Path
		0.456	0.122	0.538	0.107	ROLZ	CDR2	A to X
		0.269	0.122	0.388	0.107	ĺ		B to X
		0.313	0.067	0.325	0.079			C to X
		}						
A1	_						1	
A2	D1 V						l i	
В — —	<u> </u>							
ū.							1	
							1	
		Paramete	er				Symbol	Typ (ns) *
		1						
		}				- 1		
	Input Loading							
Pin Name	Factor (lu)							
A B	1 1	1						
B C	1	İ						
J	•	l						
Pin Name	Output Driving Factor (lu)							
x	14							
		* Minimu	m values for	r the typical	operating o	ondition.		
The values for the worst case operating condition are given by the r								
multiplier.								
C10-G44-E0	Sheet 1/1							
210 277 20	J., J., 1, 1							Page 8-5

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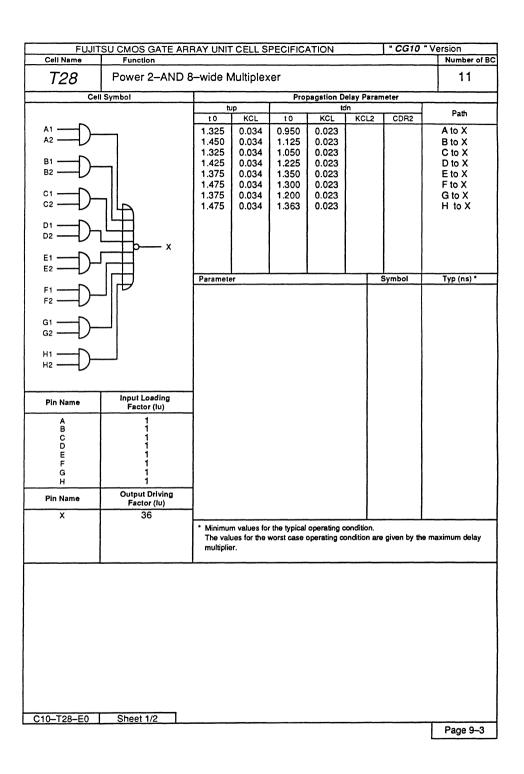
# **Multiplexer Family**

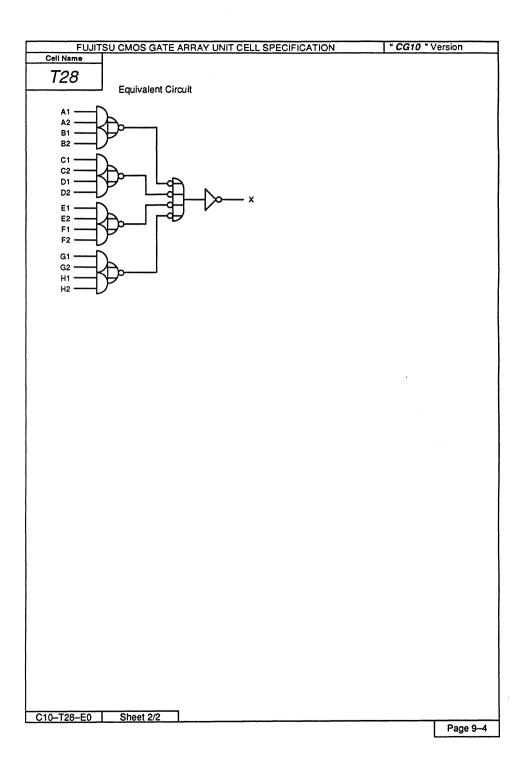
Page	Unit Cell Name	Function	Basic Cells
3–87	T24	4:1 Power 2-AND 4-wide Multiplexer	6
3-88	T26	6:1 Power 2-AND 6-wide Multiplexer	10
3–89	T28	8:1 Power 2-AND 8-wide Multiplexer	11
3-91	T32	2:1 Power 3-AND 2-wide Multiplexer	5
3-92	T33	3:1 Power 3-AND 3-wide Multiplexer	8
3–93	T34	4:1 Power 3-AND 4-wide Multiplexer	9
3-94	T42	2:1 Power 4-AND 2-wide Multiplexer	6
3-95	T43	3:1 Power 4-AND 3-wide Multiplexer	10
3-96	T44	4:1 Power 4-AND 4-wide Multiplexer	11
3-97	T54	4:1 Power 4-2-3-2-AND 4-wide Multiplexer	10
3–98	U24	4:1 Power 2-OR into 4-wide Multiplexer	6
3–99	U26	6:1 Power 2-OR 6-wide Multiplexer	9
3-100	U28	8:1 Power 2-OR 8-wide Multiplexer	11
3-101	U32	2:1 Power 3-OR 2-wide Multiplexer	5
3-102	U33	3:1 Power 3-OR 3-wide Multiplexer	7
3-103	U34	4:1 Power 3-OR 4-wide Multiplexer	9
3-104	U42	2:1 Power 4-OR 2-wide Multiplexer	6
3–105	U43	3:1 Power 4-OR 3-wide Multiplexer	9
3–106	U44	4:1 Power 4-OR 4-wide Multiplexer	11

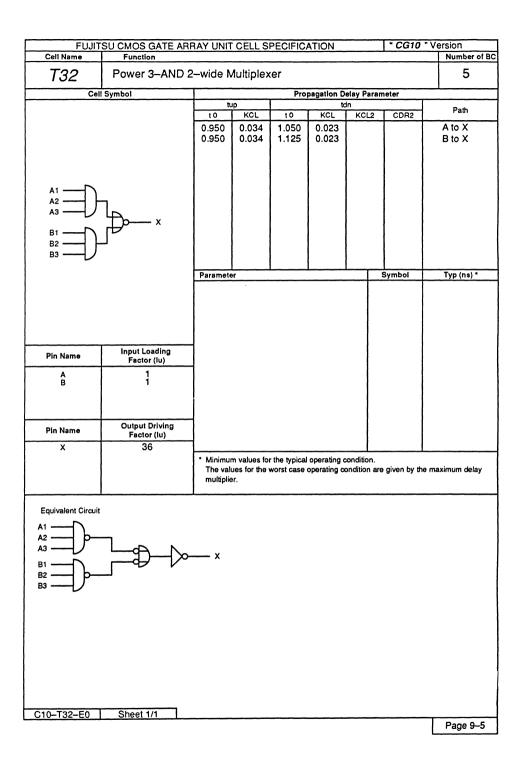
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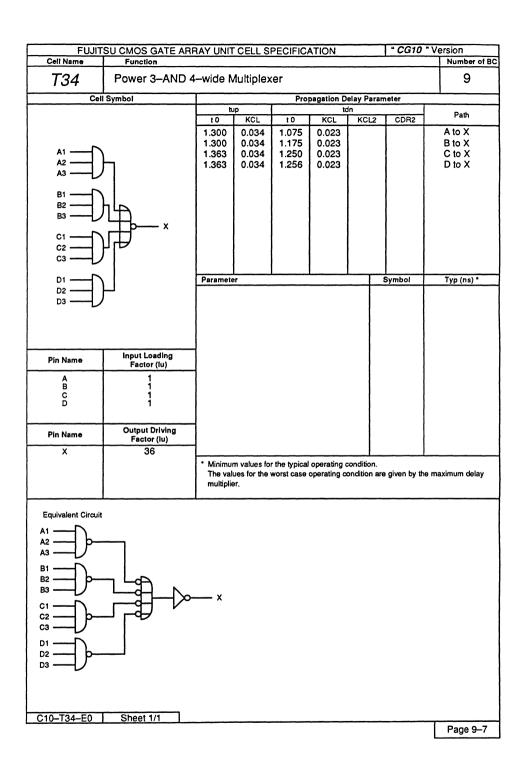
FUJIT Cell Name	SU CMOS GATE ARE	RAY UNIT	CELLS	PECIFIC	ATION		" CG10 "	Version Number of BC
T26	Power 2-AND 6	-wide N	/lultiplex	er				10
Cell	l   Symbol			Pro	pagation D	elay Paran	neter	
		t O	JP KCL	10	KCL	fn KCL2	CDR2	Path
A1		1.175 1.294 1.175 1.275 1.188 1.288	0.034 0.034 0.034 0.034 0.034 0.034	0.981 1.131 1.038 1.200 1.150 1.300	0.023 0.023 0.023 0.023 0.023 0.023			A to X B to X C to X D to X E to X F to X
C1 C2 D1 D2 D2	×	7.200	0.004		0.020			
							1	
E1	<b>-</b>	Paramete	er				Symbol	Typ (ns) *
F1	F2 —— ) ——							
Pin Name	Input Loading Factor (lu)							·
A B C D E F	1 1 1 1							
Pin Name	Output Driving Factor (lu)							
x	36						given by the	maximum delay
Equivalent Circuit A1 A2 B1 B2 C1 C2 D1 D2 E1 E2 F1 F2		о— х						
C10-T26-E0	Sheet 1/1				····			Page 9-2



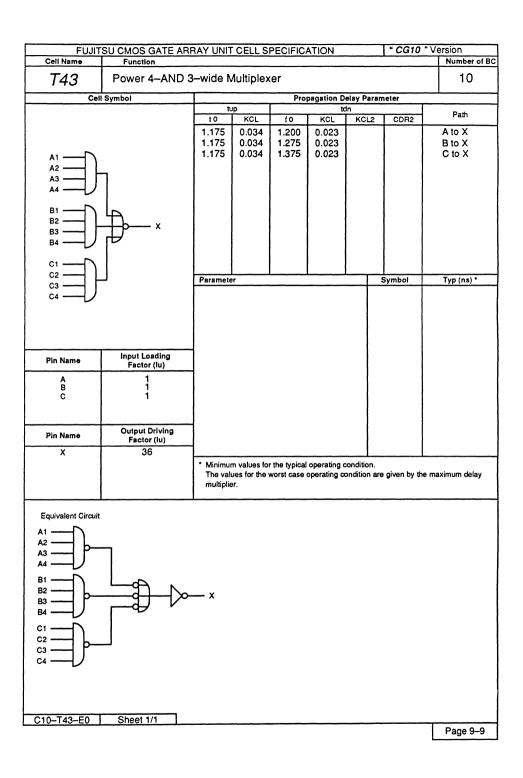


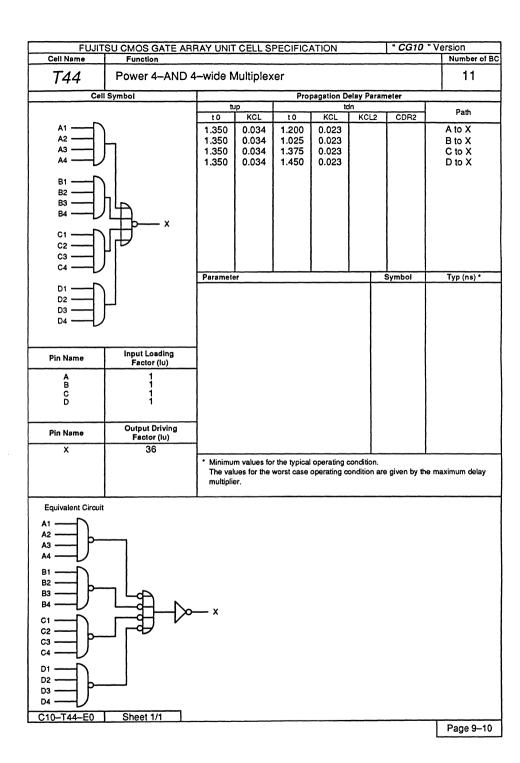


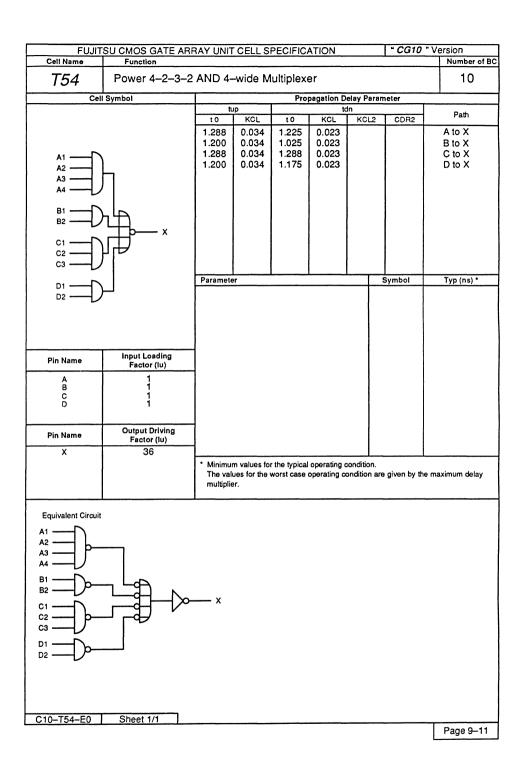
F	**************************************	5 432 1 15 115		DERVEIR			L # 0010 "	Varria -
Cell Name	SU CMOS GATE AR Function	HAY UNII	CELLS	PECIFICA	ATION		" CG10 "	Number of BC
T33	Power 3-AND 3	3-wide N	/lultiplex	er				8
Cel	i Symbol	Ι		Pro	pagation D	elay Paran	neter	
		t O	JP KCL	10	KCL	In KCL2	CDR2	Path
		1.094	0.034	1.038	0.023	ROLL	ODRE	A to X
		1.094	0.034	1.113	0.023			B to X
		1.094	0.034	1.219	0.023			C to X
A1 —		1						
A2	7	1				i		
	1	}						
B1 B2	——×						1 1	
В3 —— /	<del>     </del>	į					1 1	
c1 —								
C2	J						<u> </u>	
		Paramete	r				Symbol	Typ (ns) *
		ļ				l		
		ł					- 1	
							1	
	Input Loading	-				ı	1	
Pin Name	Factor (lu)	<u> </u>					1	
A B	1	1						
Č	i	l					1	
							1	
Pin Name	Output Driving	1						
X	Factor (lu)	į					l	
^	36	Minimus	m values for	the typical	operating o	ondition.		
		The val	ues for the	worst case	operating o	ondition are	given by the	maximum delay
		multiplie	er.					
: 								
C10-T33-E0	Sheet 1/1							
J.U								Page 9-6



<u> </u>		242///	0511.0	DEGIEIO	ATION		" CG10 "	Varaian
Cell Name	SU CMOS GATE ARI	HAY UNI	CELLS	PECIFICA	ATION		CGIU	Version Number of BC
T42	Power 4-AND 2	2-wide N	/lultiplex	er				6
Cel	l Symbol			Pro	pagation D		neter	
		t O	KCL	t O	KCL	In KCL2	CDR2	Path
		1.000	0.034	1.175	0.023	11000	331112	A to X
		1.000	0.034	1.250	0.023			B to X
A1								
A2 — _	<del>_</del>							
A3		l						
	×							
B1 B2								
Вз —		1						
B4		Paramete	er			<u> </u>	Symbol	Typ (ns) *
						1	Ì	
Pin Name	Input Loading Factor (lu)							
A B	1							
_						- 1		
		l				-	1	
Pin Name	Output Driving	1				1		
×	Factor (lu) 36							
			n values for					
		The val		worst case	operating of	ondition are	given by the	maximum delay
		<u> </u>						
Equivalent Circuit								
A1 —								
A2	_							
A4	<u> </u>	v						
B1 —		— x						
B2 —— ——	J							
B4 ——								
C10-T42-E0	Sheet 1/1							
U10-142-EU	Ollege I/ I							Page 9-8

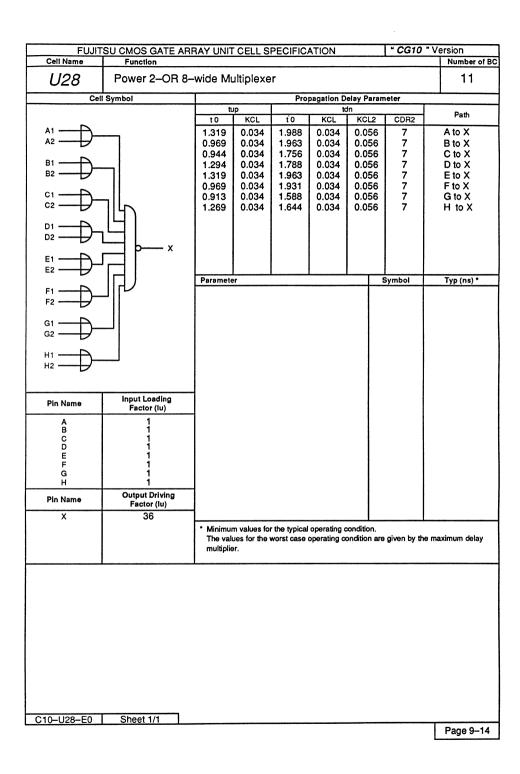






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Cell Name	SU CMOS GATE ARF	AT UNI	OELL S	COIFIU	TION		<u> </u>	Number of BC
U24	Power 2–OR 4–	wide M	ultiplexe	r				6
Cel	Symbol			Pro	pagation D		eter	
		t O	KCL	t O	KCL	in KCL2	CDR2	Path
		1.250	0.034	1.125	0.028	0.045	7	A to X
		0.900	0.034	1.094	0.028	0.045	7	B to X
		1.188 0.863	0.034 0.034	1.113 1.063	0.028 0.028	0.045 0.045	7 7	C to X D to X
A1 —	<b>—</b>	0.000	0.00		0.020	0.0.0		
A2								
B1 —	4 L							
B2	ЧЬх							
C1 —	깁							
C2 —								
D1 -	┙							
D2		Paramete	er				Symbol	Typ (ns) *
						Ì		
						İ		
	I					1		
Pin Name	Input Loading Factor (lu)					- [		
A B	1							
C	1 1							
D	1							
	Output Driving						į	
Pin Name	Factor (lu)							
×	36	* Minimu	m values for	the typical	operating	ondition.		
		<ul> <li>Minimum values for the typical operating condition.</li> <li>The values for the worst case operating condition are given by the maximum deta</li> </ul>						
		multiplie	er.					
				***************************************				
]								
0.001:								
C10-U24-E0	Sheet 1/1							Page 9-12

EUUT	SU CMOS GATE ARI	DAV HAUT	CELL C	DECIFIC	ATION		" CG10	" Version
Cell Name	Function	HAT UNII	CELLS	PECIFICA	ATION		CG10	Number of BC
U26	Power 2-OR 6-	-wide Mu	ultiplexe	r				9
Cel	l Symbol			Pro	pagation D		neter	
		t O	IP KCL	t O	KCL	In KCL2	CDR2	Path
		1.250	0.034	1.463	0.028	0.045	7	A to X
A1 ————————————————————————————————————		0.969	0.034	1.413	0.028	0.045	7	B to X
A2 —		1.275	0.034	1.500	0.028	0.045	7	C to X
В1 ——		0.988 1.025	0.034 0.034	1.500 1.613	0.028 0.028	0.045 0.045	7 7	D to X E to X
B2 —	7	1.313	0.034	1.613	0.028	0.045	7	FtoX
C1 ——	14						1	
C2	141						l	
	□						ľ	
D1 D2	'႕ㅣ							
02 <del>- D</del>	\frac{1}{\rm 1}						1	
E1	_]							
E2 -		Paramete	er				Symbol	Typ (ns) *
F1 —		Ì				į		
F2		1						
		· <b>¦</b>						
Pin Name	Input Loading Factor (lu)							
A B	1	l				:		
C D	1	ļ						
D E		ł						
Ē	1							
Pin Name	Output Driving Factor (lu)							
x	36	Minimul	m values for	r the typical	operating of	ondition.		<u> </u>
		The val	ues for the v				given by th	e maximum delay
		multiplie	er.					
			·		<del></del>			
C10-U26-E0	Sheet 1/1							Page 9–13



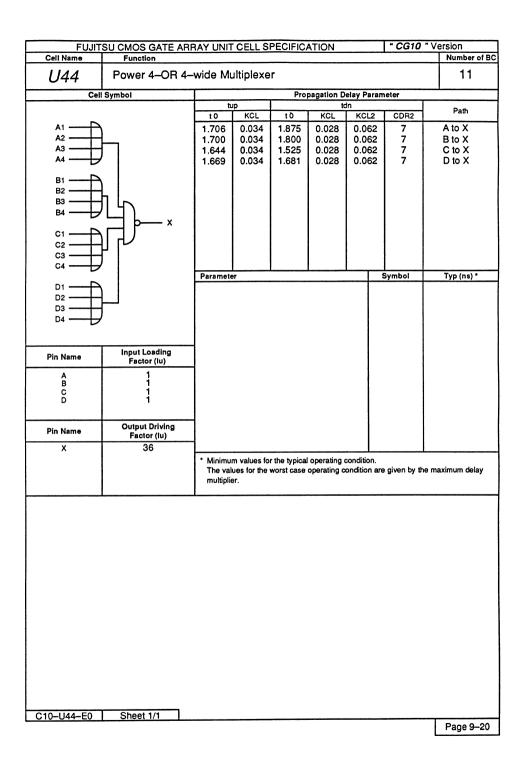
FILLE		5 A V . I II II II	0511.0	5501510			L# 0040	#\/i
Cell Name	SU CMOS GATE ARI	HAY UNII	CELLS	PECIFIC	ATION		CG10	" Version Number of BC
U32	Power 3–OR 2–	-wide Mu	ultiplexe	r				5
Cel	Symbol			Pro		elay Paran	neter	
			ıp			dn L voi o	0000	Path
		1.344	KCL 0.034	1.038	0.028	0.045	CDR2	A to X
		1.319	0.034	1.038	0.028	0.045	7 7	B to X
			0.00			0.0.0	ı i	2.07.
		ł						
		1						
A1 ——								
A2	7	1						
A3 ————————————————————————————————————	Ъ <u> </u>	]			}			
B1 —	<sub>1</sub>							
B2	J							
В3 ———								
		Paramete	er			:	Symbol	Typ (ns) *
		4						
Pin Name	Input Loading Factor (lu)							
A B	1 1	1				Ė		
В	1	ŀ				- 1		
		ļ						
Pin Name	Output Driving Factor (lu)							
X	36	1						
^		* Minimu	m values for	r the typical	operating o	condition.		
		The val	ues for the v				given by th	e maximum delay
		multiplie	er.					
	<u> </u>							
C10-U32-E0	Sheet 1/1							
	1							Page 9-15

511.05					. =		" CG10 "	V
Cell Name	SU CMOS GATE ARI	RAY UNIT	CELL S	PECIFICA	ATION		" CG10 "	Version Number of BC
U33	Power 3–OR 3-	-wide Mu	ultiplexe	r				7
Cel	l Symbol			Pro	pagation D		neter	
		t O	KCL	t O	KCL	fn KCL2	CDR2	Path
		1.425 1.406 1.444	0.034 0.034 0.034	1.425 1.488 1.575	0.028 0.028 0.028	0.062 0.062 0.056	7 7 7	A to X B to X C to X
A1 -		1.444	0.004	1.575	0.020	0.050	'	010 /
A2 A3	]							
B1 B2 B3								
C1								
C3 —		Paramete	er				Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)							
A B C	1 1 1							
Pin Name	Output Driving Factor (lu)							
×	36	ļ						
							given by the	maximum delay
	**************************************	<del></del>			· · · · · · · · · · · · · · · · · · ·			
C10-U33-E0	Sheet 1/1					<del></del>		Page 9–16
								raye 9-16

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELL S	PECIFIC	ATION		" CG10	"Ve	rsion
Cell Name	Function						·····		Number of BC
U34	Power 3-OR 4-	wide Mı	ultiplexe	r					9
	l Symbol	ı —		Pro	pagation D	elav Paran	neter		
			dτ		to	n			Path
		10	KCL	tò	KCL	KCL2	CDR2		
		1.319	0.034	1.863 1.875	0.034 0.034	0.056	7 7		A to X B to X
A1 ——	١	1.200	0.034	1.525	0.034	0.056	7		C to X
A2 ————————————————————————————————————	h	1.319	0.034	1.681	0.034	0.056	7		D to X
		<u> </u>							
B1 B2	<u> </u>								
B3	חאר						ļ		
	☐ Þ— ×					İ			
C1 C2	71-J7								
C3 —	<i>!</i>								
5:		Donomote				L			Tun (na) \$
D1 —	$\Box$	Paramete	#F				Symbol	_	Typ (ns) *
D3 —	1								
1									
	l' i								
Pin Name	Input Loading Factor (lu)								
A B	1								
C D	1 1								
D	1								
	Output Driving								
Pin Name	Factor (lu)								
x	36							<u> </u>	
			m values for				aiven hv th	ne man	imum delay
		multiplie			operating of		, giron by a		din delay
									i
C10-U34-E0	Shoot 1/1								
U10-U34-E0 ]	Sheet 1/1							$\top$	Page 9–17
								<u> </u>	. ago 5 ,,

FUJIT	SU CMOS GATE AR	RAY UNIT	CELLS	PECIFIC	ATION		" CG10	" Version
Cell Name	Function							Number of B
U42	Power 4–OR 2-	-wide Mı	ultiplexe	r				6
Cel	l Symbol			Pro	pagation D		neter	
			ib			in	1	Path
		t 0	KCL	t 0	KCL	KCL2	CDR2	A to X
		1.625	0.034 0.034	1.069 1.025	0.028 0.028	0.045 0.045	7	B to X
		1.501	0.054	1.025	0.020	0.043	′	Biox
A1 ——								
A2								
A3	7						1	
A4	7							
	ן >—-×						İ	
B1 B2	ا						i	
B3								
B4 ————————————————————————————————————								
		Paramete	er				Symbol	Typ (ns) *
		1						
		4						
Pin Name	Input Loading Factor (lu)					- 1		
Α	<del> </del>	1						
A B	1					i		
	Output Driving	1						
Pin Name	Factor (lu)	j						
X	36							
		* Minimu	m values fo	the typical	operating o	condition.		
		The val		worst case	operating o	ondition are	e given by th	e maximum delay
		) monupin	21.					
C10-U42-E0	Sheet 1/1							

ELLIT	SU CMOS GATE ARF	DAV LINIT	CELLS	DECIEIC	ATION		* CG10	" Version
Cell Name	Function Function	IOI UNII	VLLL 3	LOIFIO	TION			Number of BC
U43	Power 4–OR 3–	wide Mu	ultiplexe	r				9
Cell	Symbol							
		t O	KCL	t O	KCL	MCL2	CDR2	Path
		1.606	0.034	1.331	0.034	0.045	7	A to X
		1.638	0.034	1.413	0.034	0.045	7	B to X
A1 ——		1.688	0.034	1.494	0.034	0.045	7	C to X
A2	_							
A3 A4								
A D							1	
B1 —	7				Ì			
B2 B3	b×							
B4	$\mathcal{A}$							
_								
C1 C2								
C3		Paramete	er				Symbol	Typ (ns) *
C4								
		1						
	Input Loading	1						
Pin Name	Factor (lu)	1						
A B	1	l						
C	1							
						İ		
	Contact Database	ł				1		
Pin Name	Output Driving Factor (lu)	ŀ						
x	36							
		• Minimu	m values for	the typical	operating o	condition.		
		The val		worst case	operating o	ondition are	given by th	e maximum delay
C10-U43-E0	Sheet 1/1							15
								Page 9-19



## **Clock Buffer Family**

Page	Unit Cell Name	Function	Basic Celis
3-109	K1B	True Clock Buffer	2
3-110	K2B	Power Clock Buffer	3
3–111	КЗВ	Gated Clock (AND) Buffer	2
3-112	K4B	Gated Clock (OR) Buffer	2
3-113	K5B	Gated Clock (NAND) Buffer	3
3-114	KAB	Block Clock (OR) Buffer	3
3–115	KBB	Block Clock (OR x 10) Buffer	30
3-117	VIL	Inverting Clock Buffer	2

FILIT	SU CMOS GATE ARF	PAY LINIT	CELLS	PECIFIC	ATION		" CG10	" Version
Cell Name	Function	IAT OIL	OLLLO	LOITIO	411014			Number of BC
K1B	True Clock Buffe	er					_	2
	   Symbol	r		Pro	pagation D	elav Paran	neter	L
		tı	up		to	in		Path
		t O	KCL	t O	KCL	KCL2	CDR2	
		0.450	0.034	0.538	0.023			A to X
		ŀ						
		1						
		l						
Α	>×							
	V						ļ	
		<u></u>	l		l	<u> </u>	<u></u>	
		Paramete	er				Symbol	Typ (ns) *
		1						
						ł		
Pin Name	Input Loading Factor (lu)							
Α	1	1						
		Į						
Pin Name	Output Driving Factor (lu)	1						
x	36							
		* Minimu	m values for	the typical	operating o	condition.	a aiwaa by th	e maximum delay
		multipli		WOISt Case	operating G	ondition are	y given by u	e maximum delay
		<u> </u>						
Equivalent Circuit								
A1 — DO—	-d>×							
~~~~~	^							
C10-K1B-E0	Sheet 1/1							
010-K10-E0	Officer I/I							Page 10-1

CILUT	OULDWOOD OATE ADD		-0511.0	DE OVEVO	4.T.O.L		# CC10 "	Varaina
Cell Name	SU CMOS GATE ARF	RAY UNII	CELLS	PECIFICA	ATION		" CG10 "	Number of BC
K2B	Power Clock Bu	ffer						3
Cel	l Symbol			Pro	pagation D	elay Param	eter	
		t O	ip KCL	t O	to KCL		CDR2	Path
Α	<b>&gt;</b> — ×	0.663	0.017	0.750	0.017		Symbol	A to X
Pin Name	Input Loading							
	Factor (lu)					1		
A Pin Name	Output Driving Factor (lu) 55							
^	33		ues for the		operating o		given by the	maximum delay
Equivalent Circuit	<b>—</b> ×							
C10-K2B-E0	Sheet 1/1							1 Barris 12 5
								Page 10-2

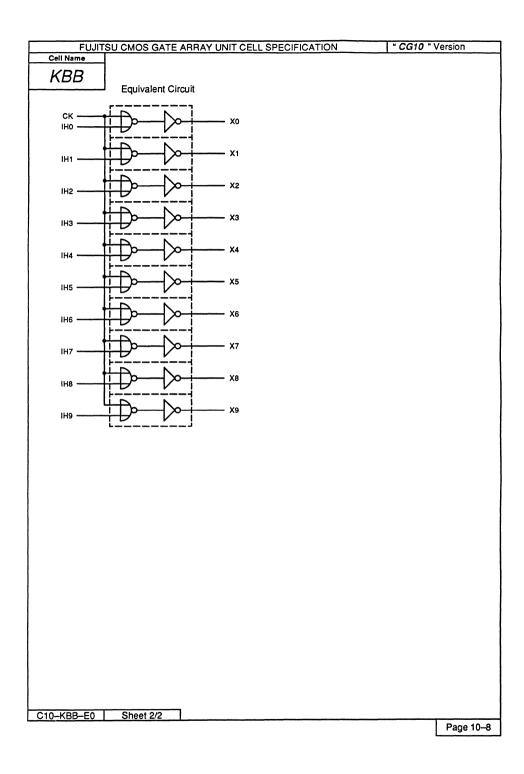
Cell Name   Function   Rated Clock (AND) Buffer   2    Call Symbol   Propagation Delay Parameter   10   KCL   10   KCL   KCL   CDR2   Path   10   KCL   10   KCL   KCL   CDR2   Path   10   KCL   KCL   CDR2   Path   10   KCL   KCL   CDR2   Path   10   KCL   KCL   KCL   CDR2   Path   10   KCL   KCL   KCL   CDR2   Path   10   KCL   KCL   KCL   CDR2   Path   10   KCL   KCL   KCL   KCL   CDR2   Path   10   KCL   KCL   KCL   KCL   CDR2   Path   10   KCL	FILIT	SU CMOS GATE ARE	DAY LIND	CELLS	PECIFIC	ATION		" CG10	" Version
Call Symbol  Tup	Cell Name		TAT OIL	OLLL O	LOII 107	411014		1 0070	Number of BC
Pin Name Input Leading Factor (lu)  A 1  Pin Name Output Driving Factor (lu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A1  A2  * Minimum values for the worst case operating condition are given by the maximum delay multiplier.	КЗВ	Gated Clock (Al	ND) Buf	fer					2
Pin Name Input Loading Factor (tu)  A 1  Pin Name Cutput Driving Factor (tu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A1  A2  * Minimum values for the values for the typical operating condition are given by the maximum delay multiplier.	Cell	Symbol			Pro			neter	
Parameter Symbol Typ (ns)*  Parameter Symbol Typ (ns)*  Pin Name Input Leading Factor (tu)  A 1  Pin Name Output Driving Pactor (iii)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A1					10				Path
Pin Name Input Loading Factor (Iu)  A 1  Pin Name Output Driving Factor (Iu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A1	A1 x						ROLE	ODAZ	A to X
Pin Name Input Loading Factor (Iu)  A 1  Pin Name Output Driving Factor (Iu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A1									
Pin Name Input Loading Factor (Iu)  A 1  Pin Name Output Driving Factor (Iu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A1			Paramete	<u></u>		L	<del></del>	Symbol	Typ (ns) *
Pin Name Output Driving Factor (lu)  X 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A1 A2  X									:
Pin Name  Output Driving Factor (fu)  X  36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A1  A2  X	Pin Name	input Loading Factor (iu)							
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A1	A								
Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Equivalent Circuit  A1	Pin Name	Output Driving Factor (lu)	ļ						
A1 X	х	36	The val	ues for the v	r the typical worst case	operating o	condition. condition are	a given by th	e maximum delay
Page 10–3	A1								

EIIIT	SU CMOS GATE ARF	AV LINIT	CELLS	PECIFIC	ATION		" CG10 "	Version
Cell Name	Function	INI UNII	JLLL S	LOIFIU	TION		00,0	Number of BC
K4B	Gated Clock (OF	R) Buffe	r		magnessadas (p) PI Ali Paliku			2
Cel	Symbol			Proj	pagation D		eter	
			ib	10		ln KCI O	CDDO	Path
A1 ————————————————————————————————————	<b>—</b> ×	t 0 0.488	0.034	0.713	0.028	0.039	8 8	A to X  Typ (ns) *
Di Nama	Input Loading							
Pin Name	Factor (lu)					Ì		
Pin Name	1 Output Driving Factor (lu) 36							
×	36		ues for the	r the typical worst case			given by the	maximum delay
Equivalent Circuit A1 A2	<b>-</b>							
C10-K4B-E0	Sheet 1/1							Page 10-4

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG10 " Version								
Cell Name	Function							Number of BC
K5B	Gated Clock (N/	AND) Bu	uffer					3
Cell	Symbol			Pro	pagation D		neter	
		t O	KCL	i o	KCL	In KCL2	CDR2	Path
		0.713	0.034	0.925	0.023	KOLZ	ODAZ	A to X
A1 A2	D•— ×	Paramete	न व				Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)							
A	1					- 1		
Pin Name	Output Driving Factor (lu) 36							
			ues for the		operating o		given by th	e maximum delay
Equivalent Circuit A1 A2	<b>→</b>	x						
C10-K5B-E0	Sheet 1/1							<del></del>
								Page 10-5

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELLS	PECIFICA	ATION		" CG10	" Version
Cell Name	Function							Number of BC
KAB	Block Clock (OF	R) Buffei	•					3
	   Symbol	r		Pro	pagation D	elav Paran	neter	
00.11	- Cymosi	tı	ρ	. 110		in	J. C. C.	Path
		t O	KCL	t O	KCL	KCL2	CDR2	
		0.675	0.017	1.156	0.017		1 1	A to X
	_							
A1	D ×							
A2	P							
			·			Ì		
l		Paramete	er				Symbol	Typ (ns) *
						ı		
Pin Name	Input Loading Factor (lu)						Ì	
A	1							
ĺ .	•					ı	j	
							į	
							1	
Pin Name	Output Driving Factor (lu)							
×	55					1	1	
			m values fo					
		The val multiplie		worst case	operating o	ondition are	given by the	e maximum delay
		malapile	JI.					
Equivalent Circuit								
	N .							
A1	<b>d</b> >×							
	•							
								•
C10-KAB-E0	Sheet 1/1							
								Page 10-6

ELLUT	SU CMOS GATE ARF	AV LINIT	CELLS	DECIEIC	ATION		" CG10 '	'Version
Cell Name	Function Function	IAT ONL	OLLL 3	- ECITIO	ATION			Number of BC
KBB	Block Clock Buff	ier (OR	x 10)					30
Cell	Symbol			Pro	pagation D		neter	
		t O	KCL	t O	KCL to	KCL2	CDR2	Path
		0.838 0.675	0.017 0.017	1.300 1.156	0.017 0.017			CK to X IH to X
ск ——	xo							
IH1 ————————————————————————————————————	X1 X2 X3							
1H4	X4 X5 X6							
1H7 1H8 1H9	X7 X8 X9	Paramete	er				Symbol	Typ (ns) °
Pin Name	Input Loading Factor (lu)							
CK IH	10 1							
Pin Name	Output Driving Factor (lu)							
X	55		ues for the v		operating coperating co		given by the	maximum delay
C10-KBB-E0	Sheet 1/2							Page 40. 7
								Page 10-7



FUJIT	SU CMOS GATE ARI	RAY UNIT	CELLS	PECIFIC	ATION		" CG10	* Version
Cell Name	Function							Number of BC
V1L	Inverting Clock	Buffer						2
Cell	Symbol	ļ		Pro	pagation D		neter	
		10	KCL	t O	KCL	n KCL2	CDR2	Path
			0.017	0.419	0.017			A to X
Α	<b>&gt;</b> — х	Paramete	er				Symbol	Typ (ns) °
Pin Name	Input Loading Factor (lu)							
Α	4							
Pin Name	Output Driving Factor (lu)							
X	55						given by th	e maximum delay
C10-V1L-E0	Sheet 1/1							Page 10-9

## Scan Flip-flop (Positive Edge Type) Family

Page	Unit Cell Name	Function	Basi Cells
3–121	SDH	Scan D Flip-flop with 2:1 Multiplex with Clear and Clock Inhibit	14
3–124	SDJ	Scan D Flip-flop with 4:1 Multiplex with Clear and Clock Inhibit	15
3–127	SDK	Scan D Flip-flop with 3:1 Multiplex with Clear and Clock Inhibit	16
3-130	SJH	Scan J-K F with Clear and Clock Inhibit	16
3–133	SDD	Scan D Flip-flop with 2:1 Multiplex, Preset Clear, and Clock Inhibit	16
3–137	SDA	Scan 1-input D Flip-flop with Clock Inhibit	12
3-140	SDB	Scan 1-input D Flip-flop with Clock Inhibit	42
3-144	SHA	Scan 1-input D Flip-flop with Clock Inhibit	68
3–147	SHB	Scan 1-input D Flip-flop with Clock Inhibit and Q Output	62
3–150	SHC	Scan 1-input D Flip-flop with Clock Inhibit and XQ Output	62
3–153	SHJ	Scan D Flip-flop with 2:1 Multiplex and Clock Inhibit	78
3–156	SHK	Scan D Flip-flop with 3:1 Multiplex and Clock Inhibit	88
3–159	SFDM	Scan 1-input D Flip-flop with Clock Inhibit	10
3-162	SFDO	Scan 1-input D Flip-flop with Clear and Clock Inhibit	11
3–165	SFDP	Scan 1-input D Flip-flop with Clear, Preset, and Clock Inhibit	12
3-169	SFDR	Scan 4-input D Flip-flop with Clear and Clock Inhibit	36
3–173	SFDS	Scan 4-input D Flip-flop with Clock Inhibit	31
3-177	SFJD	Scan J–K Flip-flop with Clock Inhibit	14

	<u>TSU CMOS GATE AR</u>	HAY UNI	CELLS	PECIFIC	ATION		CG10	" Version
Cell Name	Function							Number of E
SDH	SCAN 2-input	DFF with	Clear 8	& Clock-	-Inhibit			14
Ce	II Symbol			Pro	pagation D	elay Paran	neter	
			ab dr			in		Path
		t 0	KCL	t O	KCL	KCL2	CDR2	
[		2.325 1.469 2.369	0.034 0.034 0.034	1.863 1.344 0.669	0.023 0.034 0.023	0.045 0.067 0.045	7 7 7	CK, IH to Q CK, IH to XQ CL to Q, XQ
A1 ————————————————————————————————————	— °							
		Paramete					Symbol	Typ (ns) *
	CL	Clock Pulse Width					t cw	3.4
	01	Clock Pause Time					t cwH	2.9
		Data Setup Time					t <sub>SD</sub>	2.4
			Data Hold Time					0.7
Pin Name	Input Loading		ulse Widt				tLW	2.9
	Factor (lu)		elease Ti	me			t REM	1.9
A1, A2 CK IH CL SI A, B	1 1 3 1 2	Clear H	old Time				t inh	1.0
Pin Name	Output Driving Factor (lu)	]						
Q XQ	36 36						given by th	e maximum delay

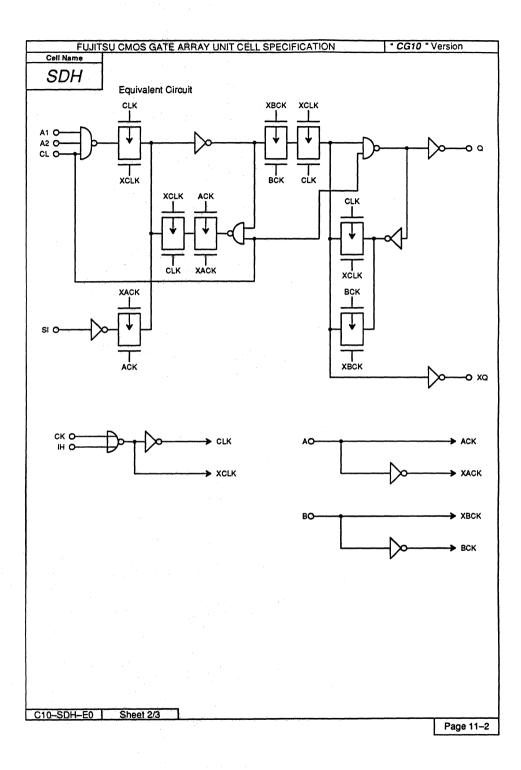
## Function Table

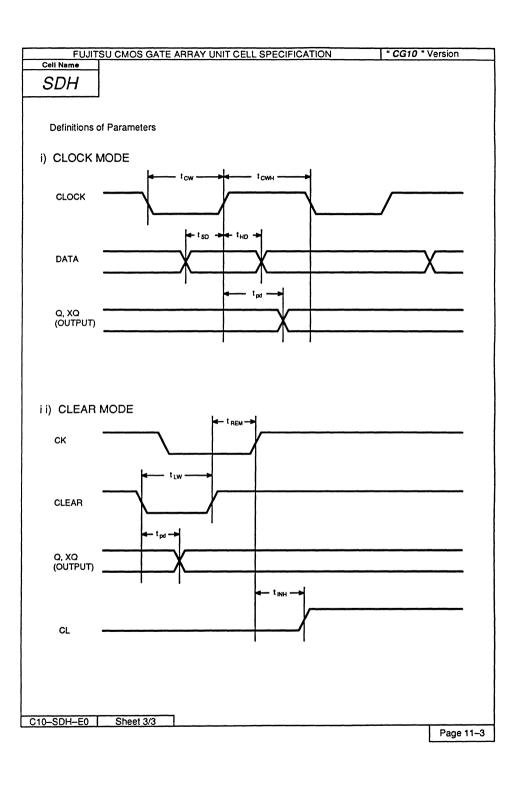
MODE				OUTPUT				
MODE	CLK	CL	D	Α	В	SI	a	ΧQ
CLEAR	Х	L	х	х	x	X	L	Н
CLOCK	L to X	н	Di	L	L	х	Di	Di
CLOCK	Н	Н	х	L	L	х	Q <sub>0</sub>	XQ <sub>0</sub>
20411	Н	Н	х	L to H to L	н	Si	Qo	XQο
SCAN	Н	Н	Х	LHt	L to H	X	Si	Si

Note : CLK = CK + IH D = A1 x A2

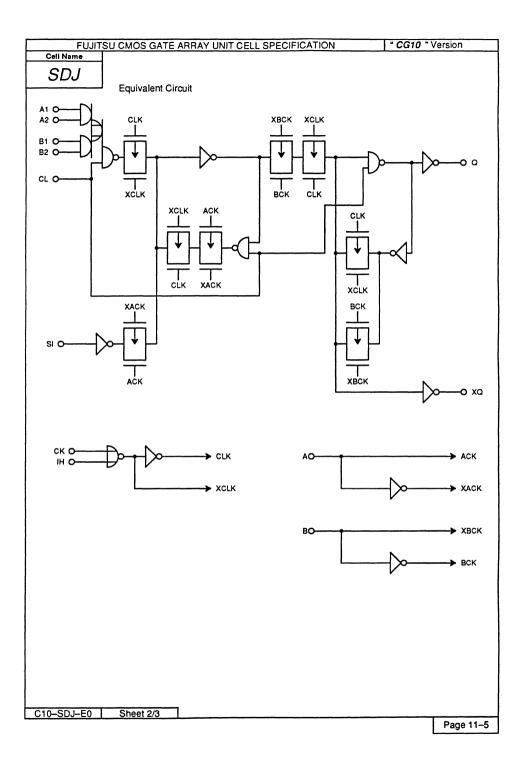
C10-SDH-F0	Sheet 1/3

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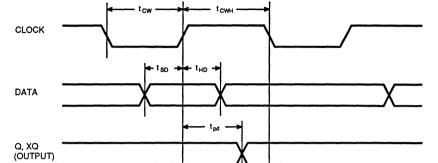


SCAN 4-input DFF with Clear & Clock-Inhibit   15	Cell Name			S G/	TE AR	RAY UNI	T CELL S	PECIFIC	ATION		- CG10	" Version Number of		
Cell Symbol					input [	OFF with	n Clear	& Clock-	-Inhibit					
To   KCL   10   KCL   CDR2   Path			wmbol			т		Pro	nagation D	elav Paran	neter			
1.719   0.034   1.888   0.022   0.045   7   CK, IH to X   1.475   0.034   1.338   0.034   0.067   7   CK, IH to X   2.338   0.034   0.063   0.023   0.045   7   CK, IH to X   2.338   0.034   0.663   0.023   0.045   7   CL to C, X   CL to			,,			1	up					Doth		
1.475   0.034   1.338   0.034   0.067   7   CK, IH to XX							+	+			CDR2			
2.338   0.034   0.663   0.023   0.045   7   CL to Q, XQ														
A1														
Parameter   Symbol   Typ (ns)			_			1	1	İ				·		
Parameter   Symbol   Typ (ns)*			<u> </u>	— a		1	}							
Parameter   Symbol   Typ (ns)*														
Parameter   Symbol   Typ (ns)*		$\dashv$					1							
Parameter   Symbol   Typ (ns)*	ск —	-					l							
Parameter   Symbol   Typ (ns)*		_	- 1				l	-						
Parameter   Symbol   Typ (ns)*		7	L				ļ		:					
Clock Pulse Width   1cw   3.4	в —	-d	×0				<u> </u>							
Clock Pause Time		کے						ith						
Data Setup Time		ا												
Data Hold Time		С	L			D-11- C	2.8							
Pin Name														
Pin Name														
A1, A2	Pin Name	.												
B1, B2	A1, A2	$\neg \dagger$		1	-,									
IH CL 3 SI A, B 2  Pin Name Output Driving Factor (Iu)  Q 36 XQ 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Function Table    NODE	B1, B2													
Pin Name	IH			1										
Pin Name	SI	- 1		1							İ			
Function Table  Function Table  INPUT  CLK CL D A B SI Q XQ  CLEAR X L X X X X X L H  CLOCK  L to H H Di L L X Di Di  CLOCK  H H X L to H to L H Si Q <sub>0</sub> XQ <sub>0</sub> SCAN  H H X L to H to L H X Si Si  Note: CLK = CK + IH  D = (A1 x A2) + (B1 x B2)	A, B					]								
**Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  **Function Table**    MODE	Pin Name	.												
Function Table    MODE	Q				·						airea her she			
MODE	XQ			36				worst case	operating o	onomon are	given by u	e maximum oeiay		
MODE						İ								
CLK   CL   D   A   B   SI   Q   XQ	Function Ta	able												
CLK   CL   D   A   B   SI   Q   XQ				11	IPUT			OUTPUT	7					
CLEAR $X$ L $X$ X X X L H  CLOCK $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	MODE	CLK	CL	D	A	В	SI	Q XQ	1					
CLOCK    L to H	CLEAR			×		x	x	L H	-					
CLOCK  H H X L L X Q <sub>0</sub> XQ <sub>0</sub> SCAN  H H X L to H to L H Si Q <sub>0</sub> XQ <sub>0</sub> H H X L H to L to H X Si Si  Note: CLK = CK + IH  D = (A1 x A2) + (B1 x B2)									$\dashv$					
SCAN	CLOCK								$\dashv$					
Note : CLK = CK + IH   D = (A1 x A2) + (B1 x B2)		<del> </del>												
Note : CLK = CK + IH D = (A1 x A2) + (B1 x B2)	SCAN								닉					
D = (A1 x A2) + (B1 x B2)		Н_	Н	X	L F	1 10 L 10 H	<u>^                                    </u>	э Si						
						Note : C			. B2)					
10_SD LE0   Sheet 1/3							U = (A1 X	MZ) + (B1 )	DZ)					
10_SD LEO Sheet 1/3														
10_SD LEO   Sheet 1/3														

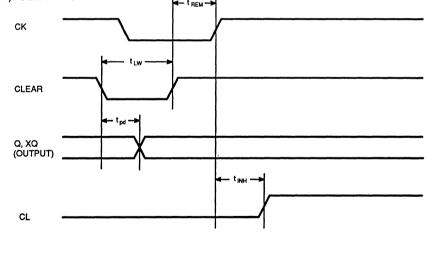


**Definitions of Parameters** 

i) CLOCK MODE



ii) CLEAR MODE



C10-SDJ-E0 Sheet 3/3

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J

FUJIT	SU CMOS GATE AR	RAY UNIT	CELLS	PECIFICA	ATION		" CG10	" Ver	rsion
Cell Name	Function								Number of BO
SDK	SCAN 6-input I	DFF with	Clear 8	& Clock-	-Inhibit				16
Cell	Symbol			Pro	pagation D	elay Paran	neter		
			קר			in			Path
		10	KCL	t O	KCL	KCL2	CDR2		
A1 ————————————————————————————————————	a	2.313 1.450 2.338	0.034 0.034 0.034	1.875 1.350 0.638	0.023 0.034 0.023	0.045 0.067 0.045	7 7 7	CK	(, IH to Q (, IH to XQ . to Q, XQ
B —d	р— хо		L						
7 7		Paramete					Symbol		Typ (ns) *
L.	لـــا		ulse Widt				tcw		3.4 2.9
	Ĭ	Clock P	ause Tim	ie			t cwn		2.9
	 CL	Data Se	tup Time				t <sub>SD</sub>		3.2
	02		old Time				t HD		0.4
		Data in	na mne				• HU		
Pin Name	Input Loading	Clear P	ulse Widt	h			tLW		2.9
Pin Name	Factor (lu)		elease Ti	me			t REM		1.9
A1, A2	1	Clear H	old Time				t inh		1.0
B1, B2 C1, C2 CK IH CL SI A, B	B1, B2 1 C1, C2 1 CK 1 IH 1 CL 3 SI 1 A, B 2								
Pin Name	Output Driving Factor (lu)	Minimum values for the typical operating condition.							
Q XQ	36 36	The values for the worst case operating condition are given by the maximum delay multiplier.							imum delay

## Function Table

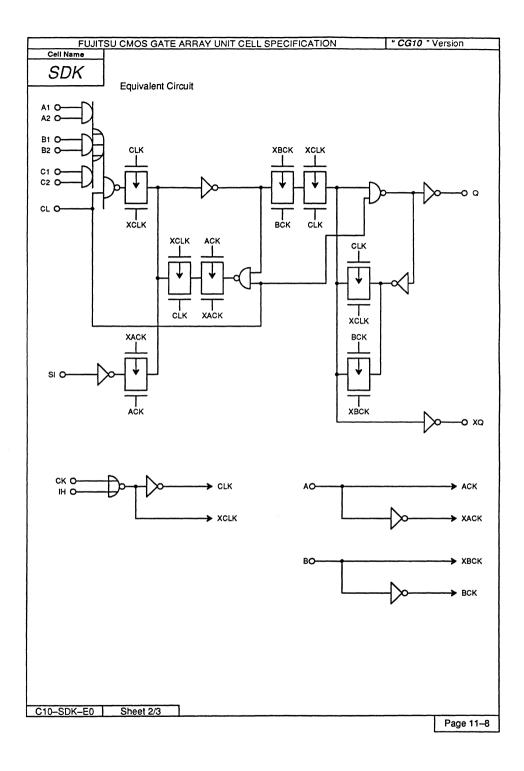
MODE			11	NPUT			OUT	PUT
MODE	CLK	CL	D	Α	В	SI	Q	XQ
CLEAR	Х	L	х	х	х	х	L	н
CLOCK	L to H	Н	Di	L	L	х	Di	Di
CLOCK	Н	Н	х	L	L	х	Q <sub>0</sub>	XQο
00411	Н	Н	х	L to H to L	н	Si	Q <sub>0</sub>	XQ <sub>0</sub>
SCAN	Н	н	Х	LH	to L to I	٠x	Si	Si

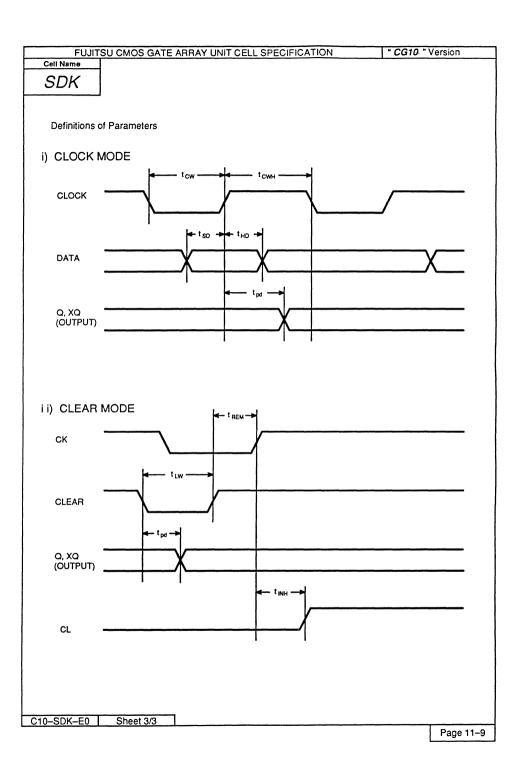
Note : CLK = CK + IH

D = (A1 x A2) + (B1 x B2) + (C1 x C2)

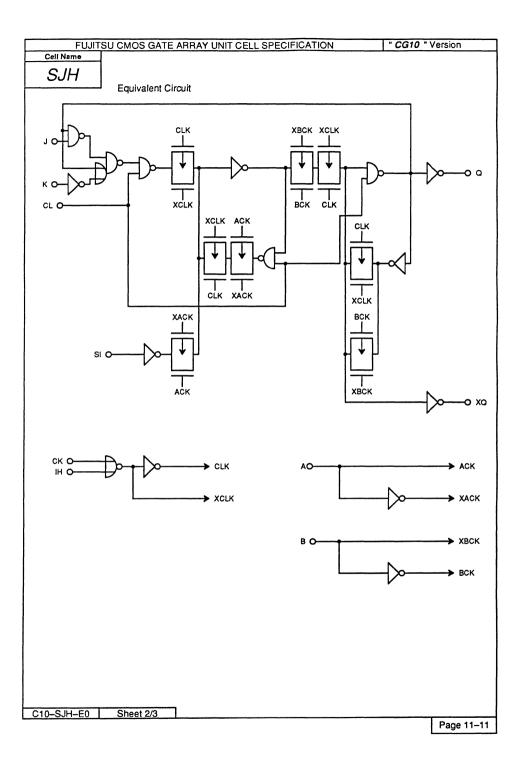
C10-SDK-E0 Sheet 1/3

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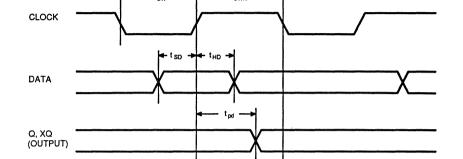




				E AR	RAY UN	IT CEL	L SP	ECIFICA	ATION		" CG10	" V			
Cell Name			ction										Number of		
SJH		SCA	N J–K	(FF v	vith Cle	ar & C	Cloc	k–Inhib	it				16		
	Cell Sy	mbol			I			Prop	pagation D	elay Paran	neter		I		
						tup	$\perp$			in KOLO	0000		Path		
					2.650	0.03	_	t 0 2.106	KCL 0.023	0.045	CDR2	-	K, IH to Q		
					1.475			1.350	0.034	0.043	7		K, IH to XC		
					2.350	0.03	34	0.869	0.023	0.045	7	0	L to Q, XQ		
							- 1								
J	_	7	_									l			
к —	<b>-</b> d		<u> </u>				1								
ск —	-				1		- 1					Ì			
IH —— SI ——					İ	İ									
A	-	L	— хо		İ										
В —	<b>-</b> q	٢	^u			İ	- [					1			
	7				Parameter Symbo								Typ (ns) *		
	CL					Pulse V					tcw		3.4		
	J.				Clock	Pause	Time	)			t cwn	2.9			
					Data S	t sp	2.8								
						Setup T					t sp		3.0		
		Inpu	t Loadin	a	Data	lold Tin	ne (J	i, N)			t HD	-	0.4		
Pin Name			ctor (lu)			Pulse V					tLW	2.9			
J,K CK			1		Clear	Release Hold Ti	e Tin	ne			t REM t INH	-	1.9		
IH					Cicari	1010 111	1110				INH				
SI			1 3 1 2		1										
A, B			2		1										
Pin Name			out Drivi		1							l			
	_	Fa	ctor (lu)		• Minim	um voluc	o for	the trainel	operating o			i			
Q XQ			36 36								given by th	ne ma	ximum delay		
					multip	lier.									
	L				<u> </u>										
Function Ta	ble														
MODE				INPUT				OU	TPUT						
MODE	CLK	CL	J	к	Α	В	SI	a	XQ						
CLEAR	х	L	х	х	Х	х	x	L	Н						
	LtoH	Н	L	L	L	L	x	L	Н						
l f	L to H	н	Н	Н	L	L	x	Н	L						
CLOCK	L to H	Н	L	Н	L	L	x	Q <sub>0</sub>	XQο						
	L to H	Н	Н	L	L	L	x	XQ <sub>0</sub>							
<del> </del>	н	н	<u> </u>		L	L	$\frac{\hat{x}}{x}$	- Q <sub>0</sub>	XQ <sub>0</sub>						
<b></b>					L to H to L		^ Si	+	XQ <sub>0</sub>						
SCAN	Н	H	×					Q <sub>0</sub>							
I SCAN L	н	н	Х	X	LHI	o L to H	^	Si	Si						
SCAN															
SCAN	.,						ı	Note : CLK	= CK+I	4					



## i) CLOCK MODE

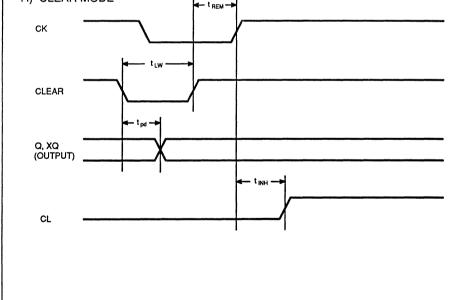


FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION

" CG10 " Version

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## ii) CLEAR MODE



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C10-SJH-E0 Sheet 3/3

FUJIT	SU CMOS GATE AF	RAY UNIT	CELLS	PECIFIC	ATION		" CG10	" Version
Cell Name	Function							Number of E
SDD	SCAN 2-input	DFF with	Clear,	Preset	& Clock	–Inhibit		16
Cel	l Symbol	T		Pro	pagation D	elay Parar	neter	
		tı	ıρ		to	dn		Path
		t 0	KCL	t O	KCL	KCL2	CDR2	
	PR 	2.313 1.656 2.813 2.400	0.034 0.034 0.034 0.034	2.013 1.338 0.638 1.469	0.023 0.034 0.023 0.034	0.045 0.067 0.045 0.067	7 7 7	CK, IH to Q CK, IH to XQ CL to Q, XQ PR to Q, XQ
A1 ————————————————————————————————————	- a - xa	Paramete	er -				Symbol	Typ (ns) *
	1	Clock P	ulse Wid		tcw	3.4		
	CL		ause Tim				t cwn	2.9
			etup Time old Time				t spt	3.4 0.7
Pin Name	Input Loading	Clear P	ulse Widt	h			t <sub>LW</sub>	3.2
FIII Name	Factor (lu)		elease Ti	me			t REM	1.9
A1, A2	1	Clear H	old Time				t inn	1.0
CK IH		Droget !	Pulse Wid	de la			A	4.3
CL	1 3 3		Release				t pw t rem	2.4
PR SI	3		Hold Time				t INH	0.7
A, B	2	Preset Hold Time						
Pin Name	Output Driving Factor (lu)							
Q XQ	36 36	<ul> <li>Minimum values for the typical operating condition.</li> <li>The values for the worst case operating condition are given by the maximum delay multiplier.</li> </ul>						

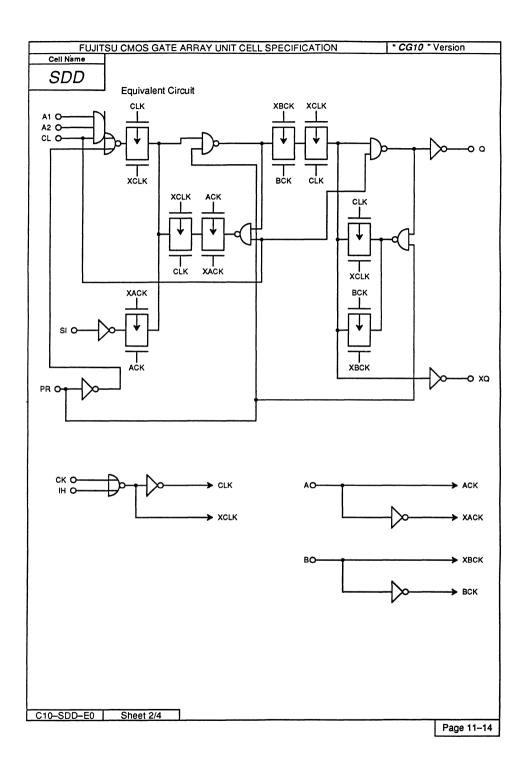
## Function Table

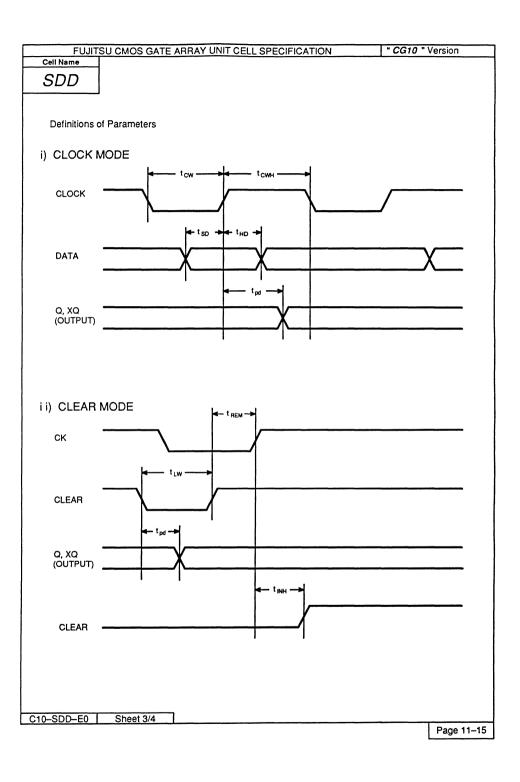
MODE				INPUT	•			OUT	PUT
MODE	CLK	CL	PR	D	Α	В	SI	a	XQ
CLEAR	Х	L	Н	х	x	X	X	L	н
PRESET	Х	Н	L	х	×	X	Х	Н	L
	L to H	н	Н	Di	L	L	х	Di	Di
CLOCK	Н	н	Н	Х	L	L	X	Qo	XQο
SCAN	н	Н	н	х	LtoHtoL	н	Si	Q٥	XQο
SCAN	Н	Н	н	х	L H to	L to H	X	Si	Si
CL/PR	Х	L	L	х	x	Х	х	Prohi	bited

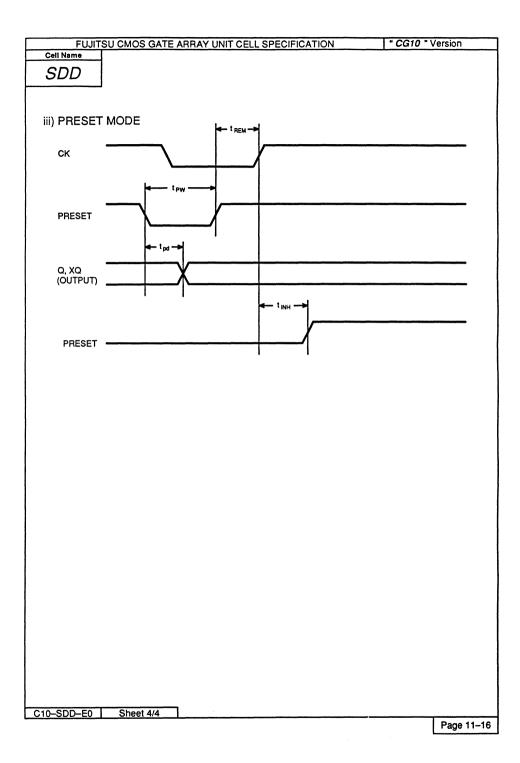
Note : CLK = CK + IH D = A1 x A2

C10-SDD-E0 Sheet 1/4

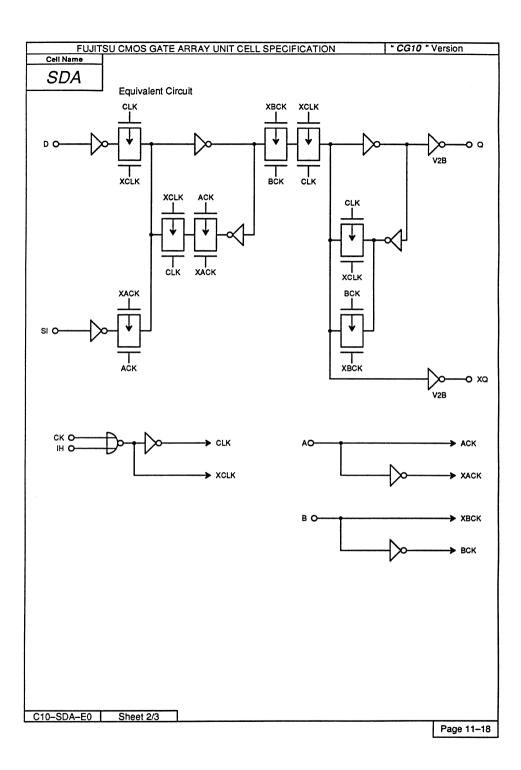
Page 11-13

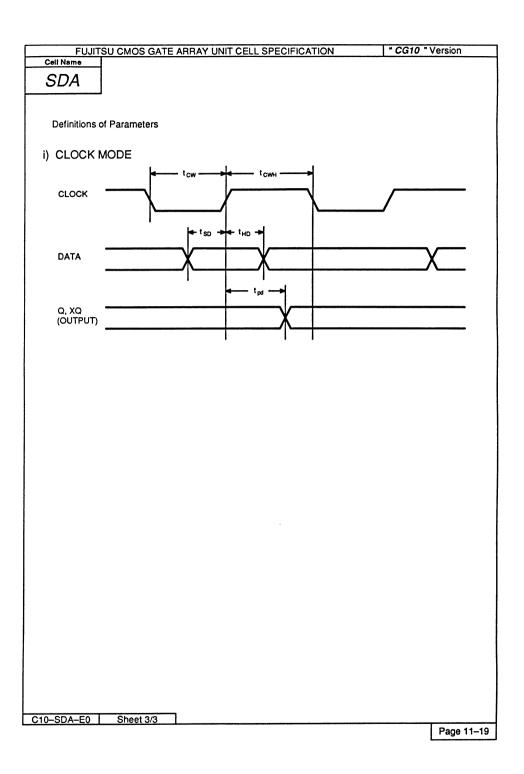


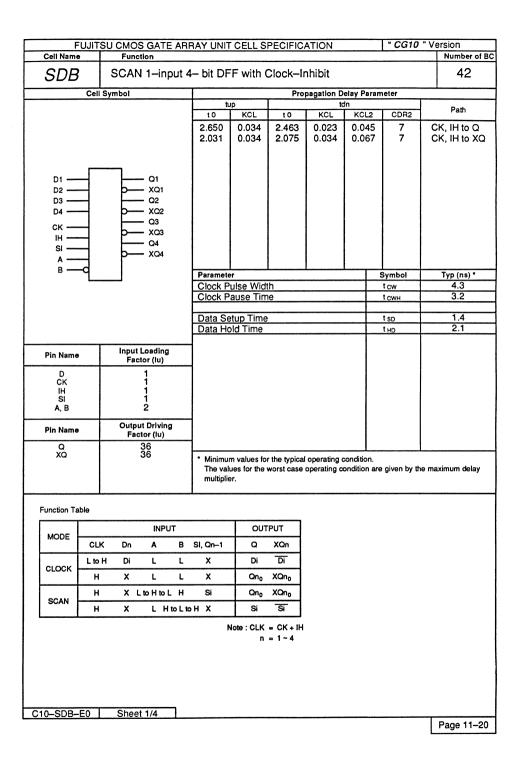


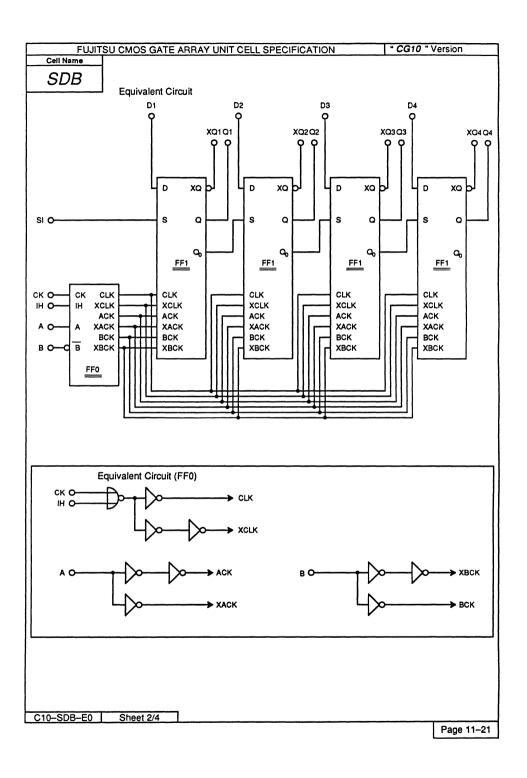


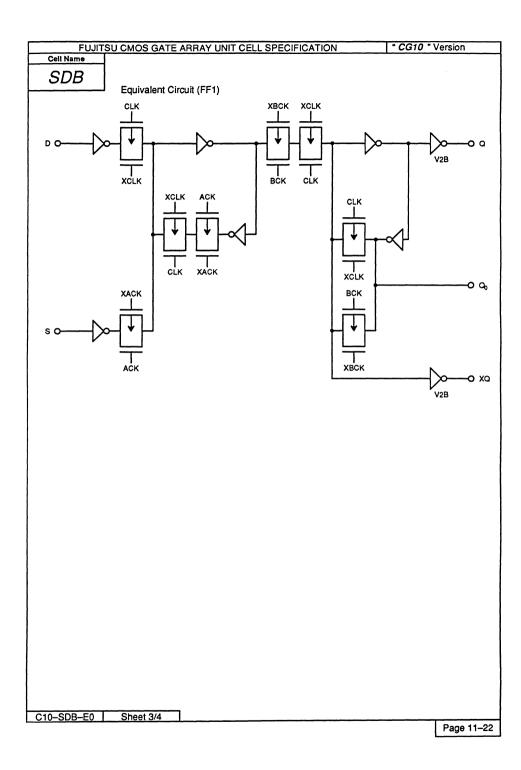
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG10" Version  Cell Name Function Number of BC  SDA SCAN 1-input DFF with Clock-Inhibit 12													
												Number of B	
SDA	.	SCA	N 1–ir	put D	FF wit	h Clock-	-Inhibit					12	
	Cell :	Symbol					Pro	pagation D		neter			
				ļ	t O	tup   KCL	1		dn L KOLO	1 0000	1	Path	
				ŀ	1.988	0.034	1.875	0.023	KCL2 0.045	CDR2	-	K, IH to Q	
				l	1.456	0.034	1.356	0.023	0.045	7		K, IH to XQ	
				1	1.400	0.004	1.000	0.004	0.007	1	١٦	nt, ii i to xq	
				i					l				
				- 1									
D —	_	<u> </u>	— a	- 1			ł	ł		l			
ск —	$\dashv$	1		l									
IH —	-	ı											
SI				l			l						
В	-d	þ-	— xq				l			İ			
-													
				[	Parame		Symbol		Typ (ns) *				
						Pulse Wid				tcw	<u> </u>	3.4	
				}	CIOCK	Pause Tim	ie			t CWH	-	2.9	
				ŀ	Data S	etup Time	·			tsp	<u> </u>	2.2	
						old Time				t HD	0.9		
									- 1				
Pin Name	.		it Loadin ictor (lu)						- 1				
D			1						- 1				
CK	1		1	- 1					-				
IH Si	-		1	- 1									
A, B	- 1		Ż						- 1				
		Out	put Drivir	na									
Pin Name			ctor (lu)						- 1				
Q	1		36	- 1									
XQ	- 1		36			m values fo							
					ne va multipl		worst case	operating o	ondition are	e given by tr	ie ma	ximum delay	
Function Ta	hle												
T T					— т	OUTOU							
MODE	CLK		INP A	В	SI	Q )	(Q						
<del>                                     </del>	L to F		<del></del> -	L	X		Di						
CLOCK	CLOCK H X L L												
SCAN	Н	х	L to H to	LH	Si	Q <sub>0</sub> >	(Q <sub>0</sub>						
SCAN	Н	х	LH	to L to I	нх	Si	Si						
					Mari	o · CI K = 4							
					NO	e:CLK = (	>r + ı⊓						
10-SDA-I	E0	She	et 1/3	1									
											- 1	Page 11-17	

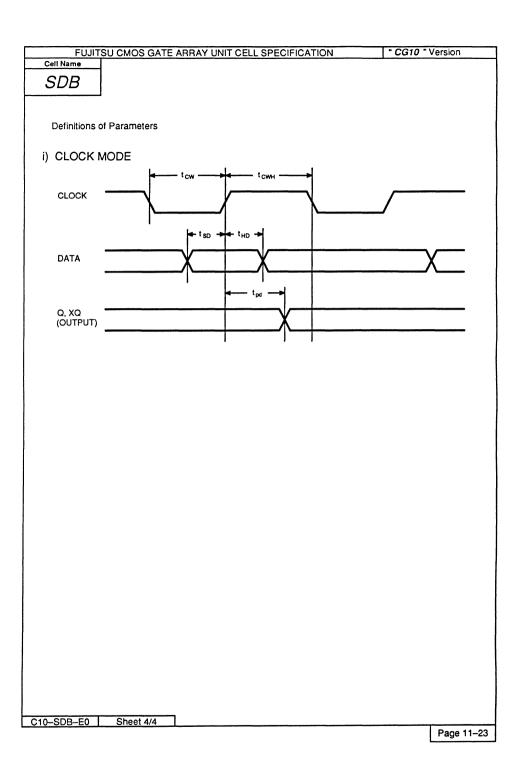




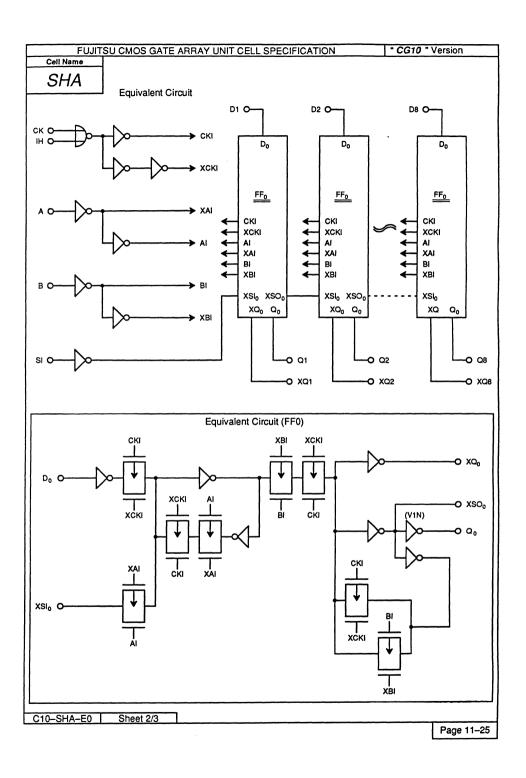






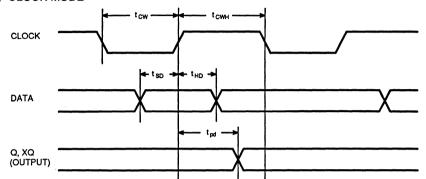


				ATE A	RRAY	UNIT	CELL S	PECIFICA	ATION		" CG10	" Ve	
Cell Name	•	Fu	nction										Number of BC
SHA				-input	8–bi	t DFI	with C	Clock-In					68
	Cell	Symbol						Pro	pagation D		neter		
ŀ					<u> </u>	tu	KCL	10	KCL	in KCIO	CDDa		Path
						950	0.067	2.950	0.051	0.056	CDR2	-	K, IH to Q
	Г		_			575	0.067	2.500	0.031	0.036	4		K, IH to XQ
D1 —			— a		-		0.007	2.000	0.070	0		ľ	,,
D3	_	F	a		İ								
D4	$\dashv$	þ-	— x		į								
D5	_		a		l								
D6 —		P	x		ł								
D8 —		5		+ 24	1			1					
		F	Q		į								
İ	- 1	þ	x					1					
		F	œ		i								
СК —		2	x					<u> </u>					
SI —	_	b-		, 27		ramete					Symbol		Typ (ns) *
A	-	F	a	3			ulse Wid ause Tin				t cw t cwh		4.5 3.5
В —	<b>-</b> q	Þ	— x	28	<u>  U   </u>	OCK F	ause IIII	16		-	CWH	_	0.0
							tup Time	)			tsD		1.2
					Da	ta Ho	old Time			_	t HD		2.1
			ut Load	lin a	$\dashv$							ŀ	
Pin Name	'		actor (										
D			1		7								
CK IH	I		1		- 1								
SI	I		- 1		1								
A B			1		1							1	
			tput Dri	lvina	$\dashv$					1			
Pin Name	•		actor (							- 1			
Q			18 18									<u> </u>	
XQ			10					r the typical					
<b>\</b>						he vali nultiplie		worst case	operating o	ondition are	given by th	e ma	aximum delay
						p.110							
F													
Function Ta	aDIO												
Mode	<u> </u>		Inputs			Ou	utputs						
141000	CLK	Dn	А	В	Si	Qn	XQn						
	F	Di	L	L	х	Di	Di						
CLOCK	Н	х	L	L	X Hold								
SCAN	Н	х	Л	н	Si	l I	Hold						
SCAN	Н	×	L	ъ	X	Si	Si						
					Note :	CLK	= CK + IH						
						n	= 1~8						
C10-SHA-	-E0	Sh	eet 1/3	3 ]								_	B
												L	Page 11-24



Definitions of Parameters

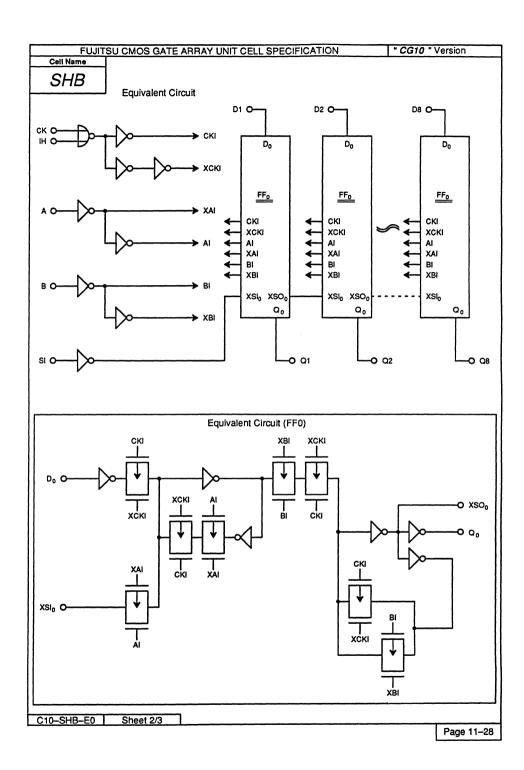
i) CLOCK MODE

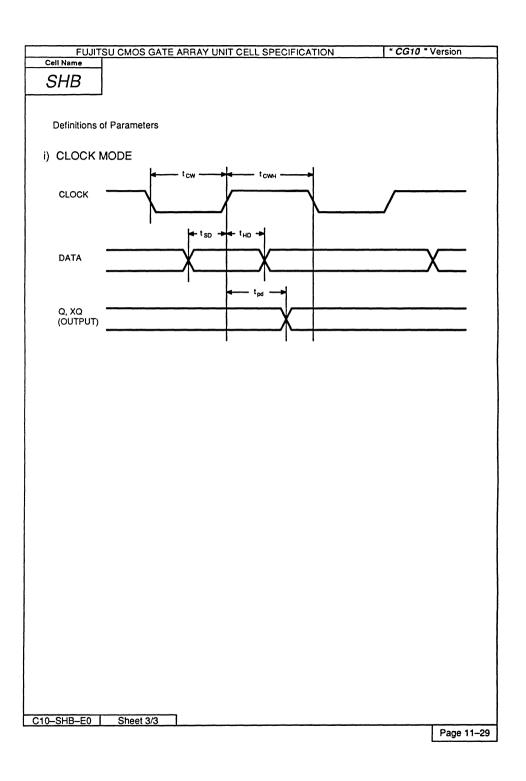


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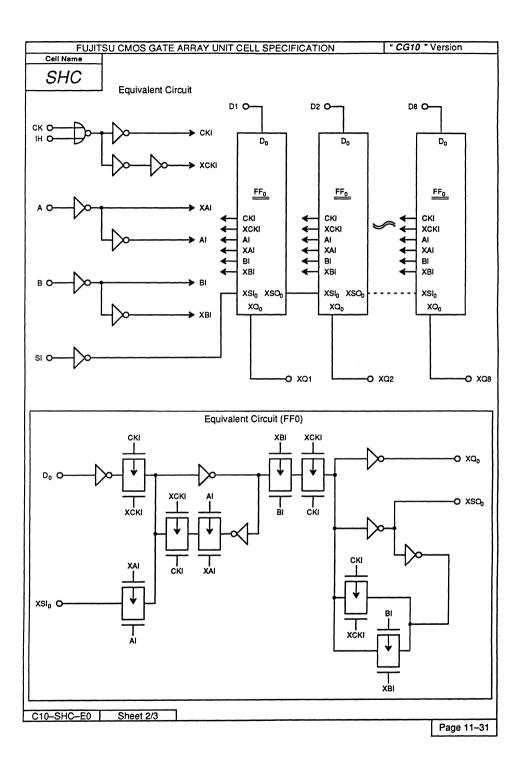
C10-SHA-E0 | Sheet 3/3 | Page 11-26

F	UJITS	SUCM	OS G	ATF AI	RRAY	UNIT	CELLS	PECIFIC	ATION		" CG10	- V	ersion	
Cell Name			nction	· · · · · ·	11.17.1	<u> </u>	OLLE O	. 2011 107	111011		1		Number of BC	
SHB	}	SC	AN 1-	-input	8–bi	t DFI	with C	lock-In	hibit & (	Q Outpu	ıt		62	
	Cell	Symbol						Pro	pagation D		neter			
					$\vdash$	tu t O	KCL	to	KCL	In KCL2	CDR2	1	Path	
						700	0.067	2.763	0.051	0.056	4	7	CK, IH to Q	
D1 — D2 — D3 — D4 — D5 — D6 — D7 — D8 — D8 — D6 — D7 — D8 — D8 — D7 — D8 — D8 — D8 — D8			a a a a a a	2 3 4 5 6 7				:						
ск —	7				Parameter									
SI — A —					Parameter Symbol Clock Pulse Width tow								Typ (ns) *	
B	-d						ulse Wid ause Tim				tcw	4.5 3.5		
					۳	OUR P	t CWH	3.5						
					Da	ata Se	tup Time				t sp	1.2		
					Da	ata Ho	ld Time				t HD	<u> </u>	2.1	
Pin Name	, ]	Inp	out Load	ing u)	1									
D CK IH SI A B			1 1 1 1											
Pin Name	,	Ou	tput Dri	ving	$\dashv$									
Q			18	<u> </u>	1	Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.								
Function Ta	able													
			Inputs			Outp	ut							
Mode	CLK	Dn	Α	В	SI	Qn	7							
	f	Di	L	L	х	Di	7							
CLOCK	Н	х	L	L	X	Holo								
SCAN	н	х	Л	н	Si	Holo								
	Н	X	L	ਪ	X	Si								
				Note	CLK n	= CK + = 1 ~ 8								
C10-SHB-	E0	Sh	eet 1/3											
												I	Page 11-27	



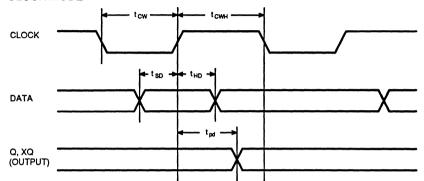


		HIT	SILCM	08.6	ATE A	BRAV	LIMIT	CELLS	PECIFIC	ATION		" CG10	" V	ersion
Cell	l Name			inction	11L A	nnai	OIVII	OLLL 3	FEOIFIC	ATION		0070		Number of BC
S	HC		sc	AN 1-	-input	8 <b>–</b> bi	t DFF	with C	lock-In	hibit & )	(Q Out	out		62
		Cell	Symbol						Pro	pagation D		neter		
						-	to tu	KCL	10	KCL	In KCL2	CDR2		Path
1							613	0.067	2.563	0.073	0.101	4	-	K, IH to XQ
1						-	۱	0.007		0.07.0		<u> </u>		,
0	01 — 02 — 03 —		0000	— x	Q1 Q2 Q3 Q4									
0	05 — 06 —	=	000	— x	25 26 27									
D	ов — ж —		5		28									
	H —	$\dashv$												
1	SI						ramete					Symbol		Typ (ns) *
1	В —	-d	j					ulse Widt ause Tim				tcw		4.5 3.5
		<u> </u>				10,	JUN PE	JUSE IIII	<u> </u>		-	t cwH		0.0
								tup Time				t so		1.2
						Di	ita Ho	ld Time				t <sub>HD</sub>		2.1
Pin	Name		Inp F	ut Load	ling u)									
١.	D CK	i		1		-								
1	łΗ	į		1										!
	SI A	l		1		-								
	В	- 1		1										
Pin	Name		Ou	tput Dri	iving lu)									
,	XQ			18		٦		es for the	r the typical worst case			given by th	e ma	ximum delay
							·							
Funct	tion Ta	ble					,	_						
M	ode			Inputs	;	,	Outpu	1						
L		CLK	Dn	A	В	SI	XQn							
016	оск	£	Dn	L	L	×	Di	╛						
		н	х	L	L	х	Hold	]						
		Н	х	Л	Н	Si	Hold	٦						
sc	CAN	Н	х	L	ъ	×	Si	7						
				L		: CLK	= CK+ = 1~8							
}														
-	2012	F0 1	OI:	201 1 1										
C10-S	SHU-	<u>=0  </u>	Sh	eet 1/3									Т	Page 11-30
													L	. ugo 11-00



Definitions of Parameters

i) CLOCK MODE

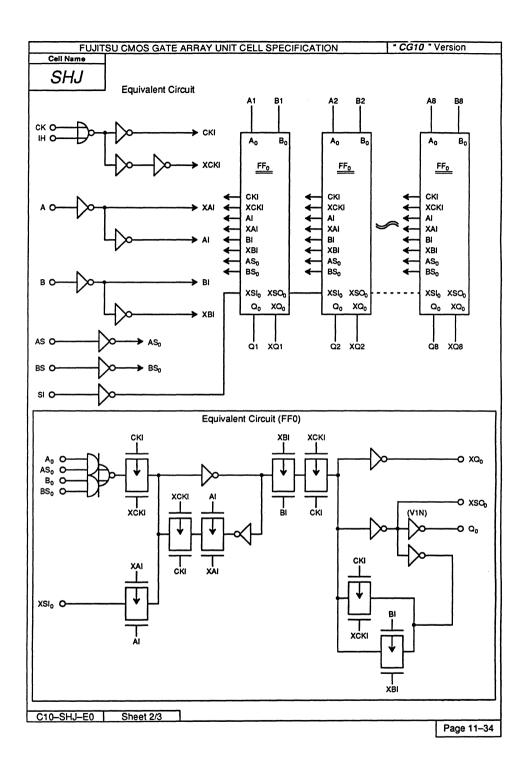


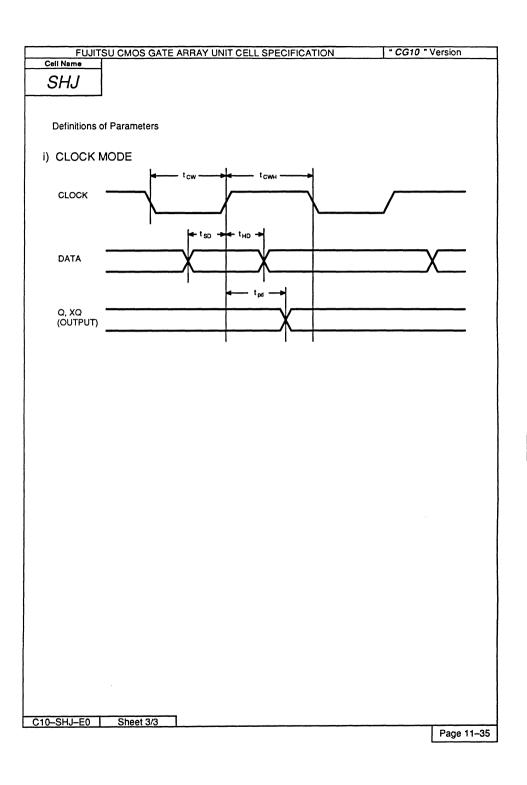
3

C10-SHC-E0 Sheet 3/3

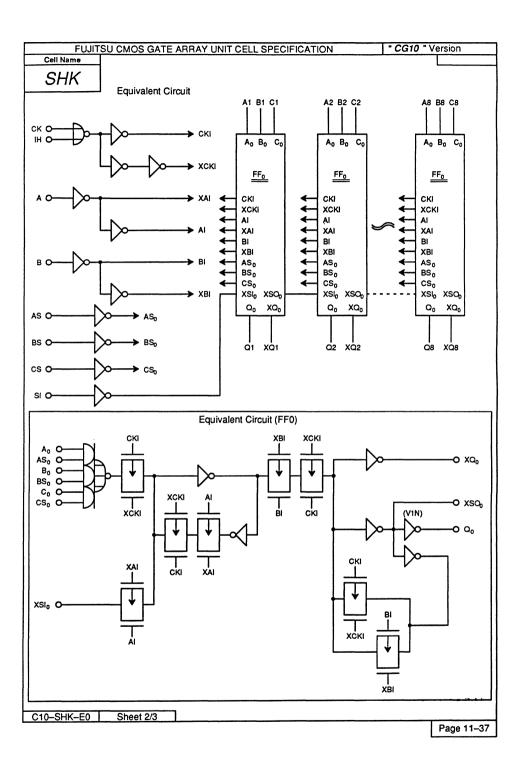
Page 11-32

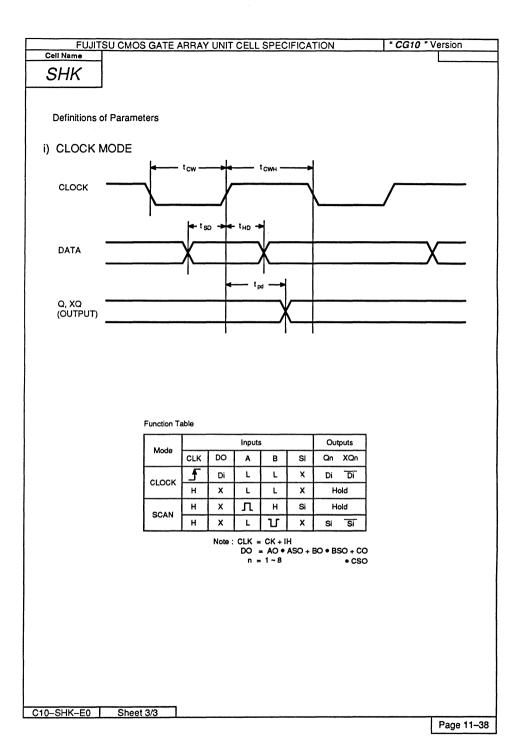
1	FUJITS	SU CM	IOS G	ATE AF	RAY	UNIT	CELL	SPECIFIC	ATION		" CG10	" V	ersion
Cell Nam	e	Fı	unction										Number of BC
SHJ				-bit DF	Fw	ith C	lock-Ir	nhibit & 2					78
	Cell	Symbol	<u> </u>		_			Pro	pagation D		neter		
					<u> </u>	tu				dn			Path
A1					_	t 0	KCL	t 0	KCL	KCL2	CDR2	<u> </u>	NC 1111 0
A1 —			Q			013	0.067		0.045	0.067	4		CK, IH to Q
B1 —	7	۲		Q1	2.	575	0.067	2.500	0.062	0.112	4	C	K, IH to XQ
A2 —			Q		1			1		l		ŀ	
B2 — A3 —		۲	_ ^	Q2 2				1		ĺ			
B3 —				3 Q3				1		l		l	
A4 —		Ľ						ļ				ŀ	
B4		h		Q4				Ì		l		ł	
A5	_	ᄃ	Q					ł					
B5	_	Ь		Q5				1		1	i	ŀ	
A6		-	<u> </u>	6				ł		l			
B6 —	-	þ	x	Q6	1			1	1				
A7 —	$\dashv$	⊢	<u> </u>	7					!	1			
B7	$\dashv$	þ		<b>Q</b> 7	_				<u> </u>	<u> </u>	<u> </u>		
A8 —			a		_	ramete					Symbol		Typ (ns) *
B8 —		Р	X	<b>Q</b> 8			ulse Wi				tcw	<u> </u>	4.5
AS -	-d	- 1			CI	ock P	ause Ti	me			t CMH		3.5
BS —	-d				<u> </u>		T:						1.9
ск —	-	- 1					tup Tim				t <sub>SD</sub>		2.0
IH —	$\dashv$	1			100	ila no	ld Time				t HD		2.0
sı —	$\dashv$	- 1			1								
Α —	-	- 1			1								
В —	-q	- 1			1								
					1							ł	
				d)	4								
Pin Name	•		ut Load		1							ŀ	
An Po			1	-/	٦								
An, Bn (n=1~8)	j		'		1								
AS, BS			1		1								
CK IH	- 1		1		1					i			
SI			i		1								
A, B	- 1		1		1					1			
	-+	011	tput Dr	ivina	1								
Pin Name	•		Factor (										
Q			18					or the typical					
a xa			18 18			'he valu nultiplie		worst case	operating o	ondition are	given by th	e ma	aximum delay
	ļ				1 "	ioiupiie	••						
Function Ta	able												
r	г					_							
Mode	<u> </u>		Inputs	; 		0.	tputs						
	CLK	DO	Α	В	SI	Qn	XQn						
	F	Di	L	L	×	Di	Di						
CLOCK	뉴	X	L		×		lold						
	<u> </u>	_^_				<u> </u>	1010						
6044	н	Х	Л	н	Si	L +	lold						
SCAN	Н	х	L	ਪ	×	Si	Si						
	<u> </u>	<u> </u>	L			L							
			Not	e : CLK	= CK	+ IH	) \PO =						
					= AC = 1 ~		• BO + C BSO						
						-							
C10-SHJ-	E0	Sh	eet 1/3										
													Page 11-33
												_	



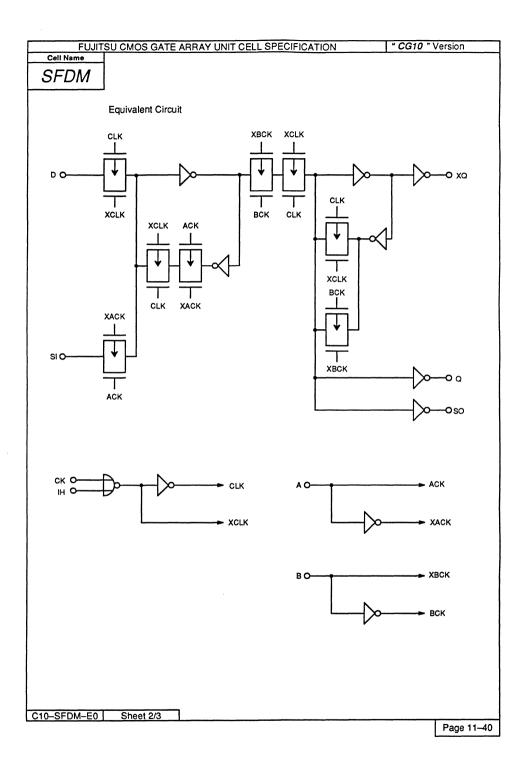


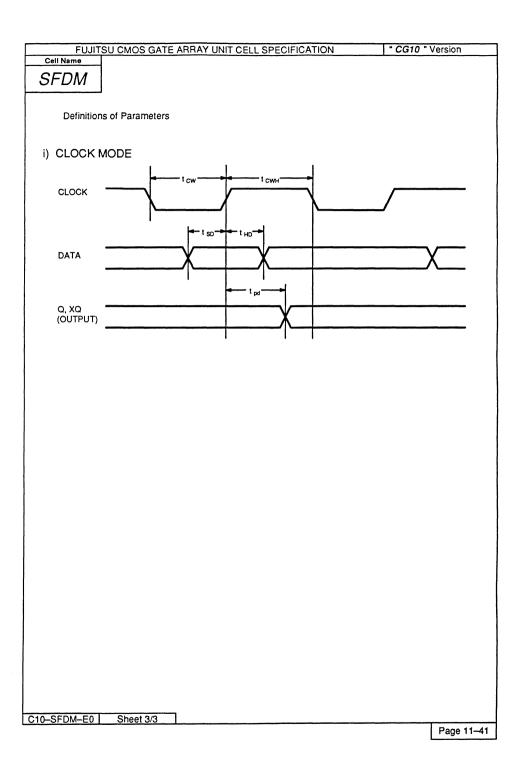
FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG10	" Ve	ersion
Cell Name	Function		<u> </u>	<u> </u>	111011				Number of BC
SHK	SCAN 8-bit DFF	with C	lock–Ini						88
Cell	Symbol			Proj	pagation D		meter		
		tı.				in			Path
		t 0	KCL	t O	KCL	KCL2	CDR2	_	
A1 —	Q1	2.900	0.067	2.875	0.051	0.056			K, IH to Q
B1 —	D XQ1	2.550	0.067	2.500	0.073	0.101	4	С	K, IH to XQ
A2						1	1 1		
B2	Q2					1			
C2	D XQ2					1	1 1		
A3							1 1		
В3 ——	—— ОЗ						1 1		
С3 ——	р xaз					1	1 1		
A4	Q4					l	1 1		
B4	l l					I			
C4	р хо <sub>4</sub>								
A5	Q5		:						
B5	D XQ5	Paramete	<u> </u>	L	L	<del> </del>	Symbol		Typ (ns) *
A6 —	ρ— λ <b>ω</b>		ulse Wid	h			tow		4.5
B6	Q6		ause Tim				tcwh		3.5
C6	b xae	Olocki	4050 1111				· cwa		
A7		Data Se	tup Time	·			t <sub>SD</sub>		2.4
В7 ——	Q7	Data Ho					t <sub>HD</sub>		1.9
C7	р хат								
A8	Q8								
B8	ı					- 1			
C8 —	p xos								
AS —d						- 1	1		
BSq						•			
csq						- 1			
ск —	l					- 1	1		
H						- 1	Į.		
SI						İ			
A B						1			
°-4_									
						- 1			
Din Name	Input Loading								
Pin Name	Factor (lu)								
An, Bn, Cn	1					- 1			
(n=1 ~ 8)	4								
AS, BS, CS CK						l			
H H	1					l			
SI	1					1			
A, B	•					ļ			
Pin Name	Output Driving Factor (lu)								
a	18 18			r the typical			m airma bu 4	<b></b> -	vimum dalau
XQ	18	multiplie		worst case	operaung o	oridition a	re given by the	o 1118	Annum Geray
( l									
C10 C11/ F0 1	Sheet 1/3								
C10-SHK-E0	SHEEL 1/3							Т	Page 11-36
								L	1 age 11-00

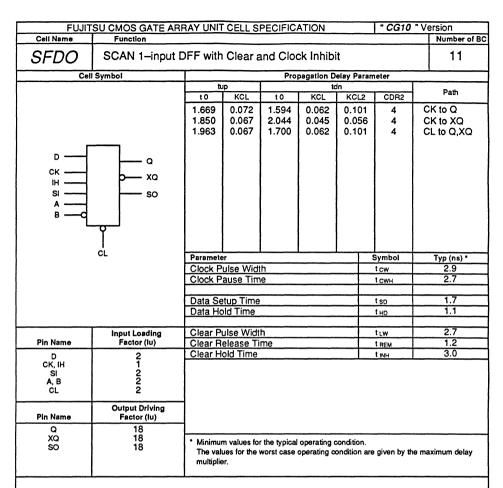




	11117	SUCM	108 G	ATE A	DDAV	LIMIT	CELLS	PECIFIC	ATION		" CG10	" Ve	rsion		
Cell Name			unction	<u> </u>	I I I	OIVII	OLLLO	1 2011 101	THON		1 00.0	Ì	Number of BC		
SFDN	1	SC	AN 1-	-input	DFF	with	Clock-						10		
	Cell	Symbo	·					Pro	pagation D		neter				
					$\vdash$	tu t 0	KCL	10	KCL	fn KCL2	CDR2		Path		
					1.	444 831	0.067 0.067	1.481 1.806	0.056 0.045	0.095 0.056	4 4		CK to Q CK to XQ		
D — CK — IH — SI — A — B —			<b></b> :	a xa so											
						ramete		14			t cw		Typ (ns) *		
							ulse Wid ause Tim				t cwH		2.5 2.5		
						Data Setup Time t sp									
						Data Setup Time         t sp         1.0           Data Hold Time         t нp         0.9									
					ے ل	110 110	id Time				· AD				
Pin Name	.		out Load Factor (												
D CK IH SI A, B			2 1 1 2 2												
Pin Name			tput Dr Factor (												
a so			18 18		1		es for the	r the typical worst case			e given by th	e ma	ximum delay		
Function Ta	ıble														
			inputs	;		O	utputs								
Mode	CLK	D	A	В	SI	Q, SC	) XQ								
	£	Di	L	L	х	Di	Di								
CLOCK	Н	×	L	L	×		Hold								
	Н	×	л	н	Si										
SCAN	Н	x	L	u	×	Si	Si								
Note : CLK = CK + IH  C10-SFDM-E0   Sheet 1/3															
U.U UI UIVI	1	0.1										T	Page 11-39		
												L_			







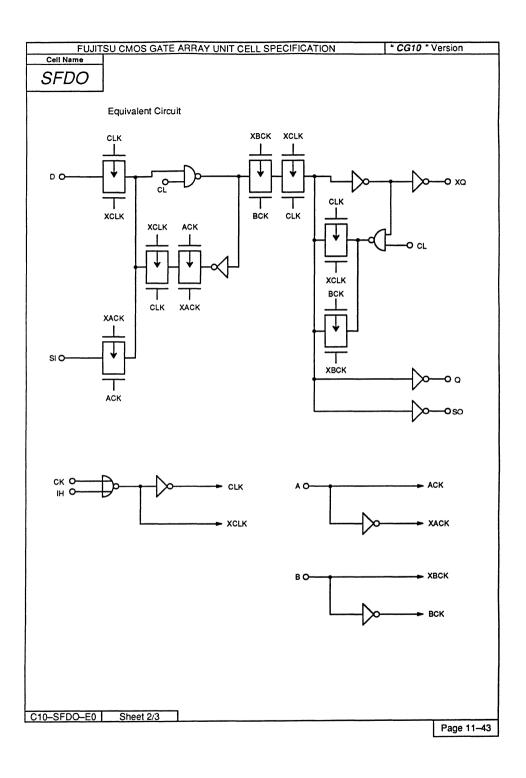
#### Function Table

Mode			Input	s			Outp	outs
Mode	CLK	CL	D	A	В	SI	Q, SO	XQ
	<b>F</b>	Н	Di	L	L	Х	Di	Di
CLOCK	Н	Н	Х	L	L	Х	Ho	old
	х	L	Х	Х	Х	Х	L	н
SCAN	Н	Н	Х	ζ	н	Ö	Но	d
SCAN	Н	н	х	٦	V	Х	Si	Şi

Note : CLK = CK + IH

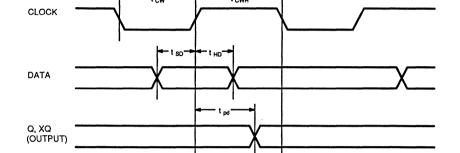
C10-SFDO-E0 | Sheet 1/3

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### i) CLOCK MODE

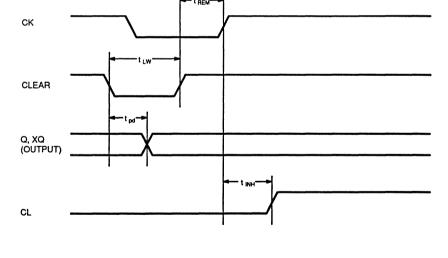
**SFDO** 



" CG10 " Version

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION
Cell Name

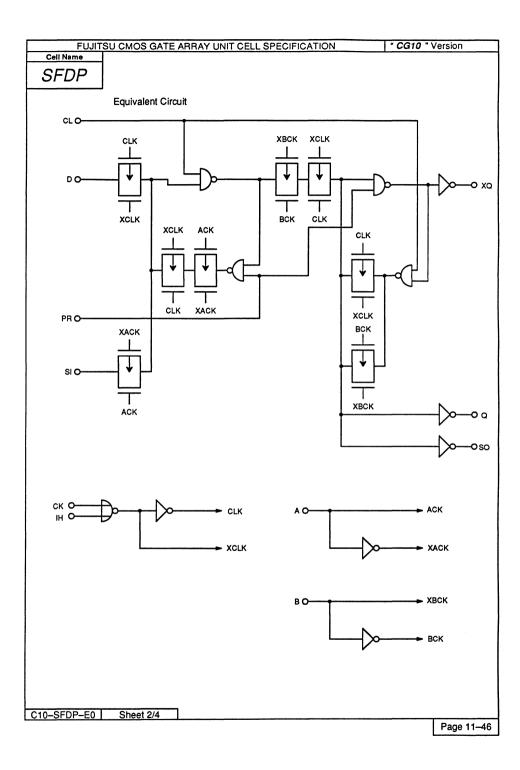
### ii) CLEAR MODE

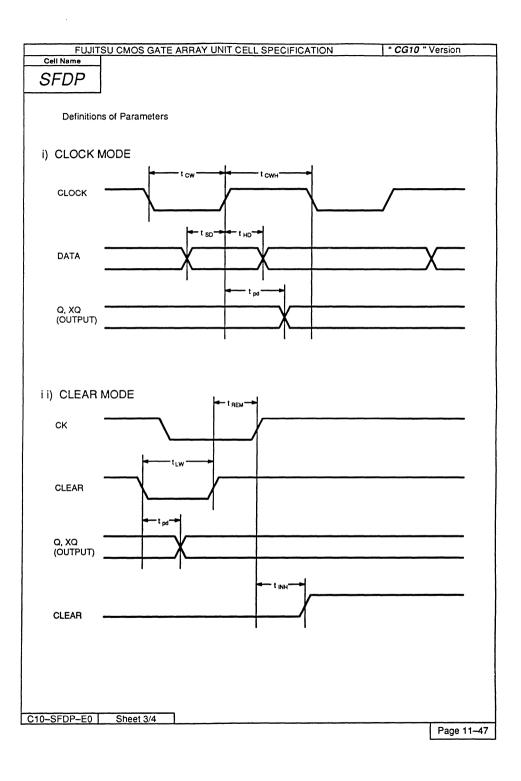


C10-SFDO-E0 | Sheet 3/3 | Page 11-44

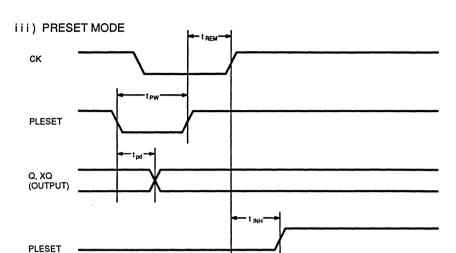
F	UJITS	SU CN	IOS G	ATE A	RRAY	UNIT	CELL	SPECIFIC	ATION		" CG10	" V	ersion
Cell Nam	е	F	unction										Number of BC
SFDI				-inpu	DFF	with	Clea	r, Preset,					12
	Cell	Symbo						Pro	pagation D		meter		
					<u> </u>	t O		10		dn KOLO	1 0000	1	Path
							KCL		KCL	KCL2	CDR2	-	K to Q
						.688 .231	0.072		0.062 0.045	0.101	4	1	K to XQ
		PR				269	0.067		0.062	0.101	4		L to Q,XQ
		-				844	0.072		0.045	0.056	4		R to Q,XQ
D -		٩											
ск -				a									
IH -			þ—	XQ		l		i					
SI -				so									
A -						ŀ							
В -	<b>-</b> •												
	_	7	,			- 1						l	
		1			Pa	ramete	·		I	<del></del>	Symbol	<del>                                     </del>	Typ (ns) *
		CL					ılse W	idth			tcw	$\vdash$	2.9
							ause T				t cwн		2.7
							tup Tin				t sp	<u> </u>	1.7
					10	ata Ho	ld Tim	<u>e</u>			t HD	-	1.1
Input Loading Clear Pulse Width t Lw 2.7													
Pin Name	,		Factor (				elease				t REM		1.2
D			2		CI	ear Ho	old Tim	ne		t inn		3.0	
CK, IH SI			2 1 2 2 2		-		Vilaa V	/: JAL		$-\!\!\!\!+\!\!\!\!\!-$		_	3.9
A, B			2				Pulse V	Time			t PW	-	0.6
CL, PR	1		2				old Ti				t INH	_	3.9
			utput Di							<del></del>			
Pin Name	-		Factor	(lu)	_								
Q XQ	- 1		18 18		-								
so			18					for the typical			e civen by th	ne ma	ximum delay
	- 1					nultiplie					- g , -		
Function Ta	able												
Mode				Inputs			·	Outputs	]				
	CLK	CL	PR	D	A	В	SI	Q,SO XQ	4				
	<u> </u>	Н	Н	Di	L	L	X	Di Di	4				
	Н	H	н	×	L	L	X	Hold	4				
CLOCK	×	L	н	X	×	×	×	LH	4				
	X	Н	L	X	×	×	×	H L	4				
	X	L	L	X	X	×	X	Prohibited	4				
SCAN	Н	Н	Н	X	Л	Н	Si	Hold	4				
H   H   X   L   🛈   X   Si 🔻													
							Note : 0	CLK = CK+	IH				
10 0500	E0 1												
10-SFDP	<u>-E0</u>	Sh	eet 1/4	4									

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**Definitions of Parameters** 



3

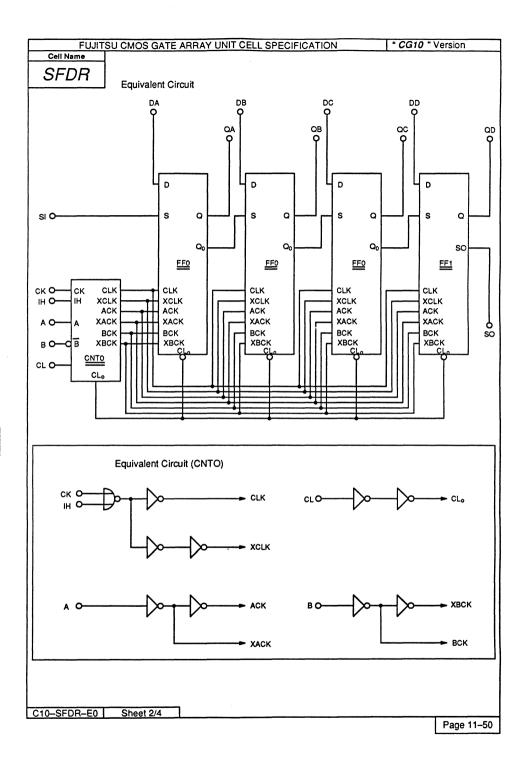
C10-SFDP-E0 | Sheet 4/4 | Page 11-48

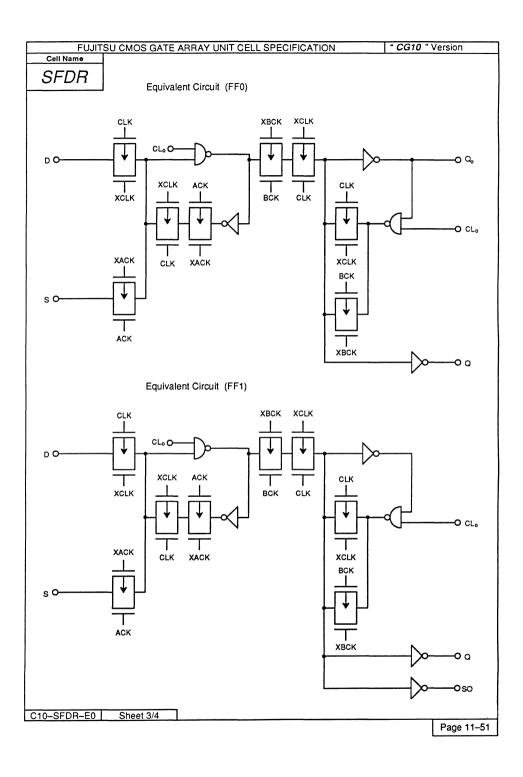
	FUJIT	SU CN	IOS G	ATE A	RRAY	/ UNIT	CELL S	PECIFIC	ATION			" CG10	" V	ersion
Cell Nam	е	F	unction											Number of
SFD	R	sc	AN 4	–inpu	t DFF	with	Clear	and Clo	ck Inhibi	it				36
	Cell	Symbo	ı					Pro	pagation D	elay Pa	aram	eter		
					-	tı.				dn L KOL	_	0000		Path
					<u> </u>	t 0	KCL	t 0	KCL	KCL	-	CDR2	<del>  _</del>	N/ 4= 0
					2	.325	0.072	2.344	0.062 0.062	0.10		4		K to Q L to Q
					- 1	_	_	2.400	0.002	0.1	12	-	١,	L 10 Q
	_		1							l				
DA -				QA						l				
DB -				QB	- 1					i				
DC -			ì	QC QD	- 1									
DD -				QD	İ					ļ				
CK -	$\dashv$				ı					ł				
IH -														
SI - A -				so	ł					l				
В-					İ									
	L	-	j		Ļ	Parameter Symbol								
		Ĭ				Parameter Symbol Clock Pulse Width								Typ (ns) * 3.2
		CL				Clock Pulse Width tow								3.5
		OL			ľ	Clock Pause Time town								
					Data Setup Time t so									0.7
					D	ata Ho	ld Time					t HD		1.5
				<del></del>	Clear Pulse Width tuw								3.2	
Pin Name	.		put Loa Factor (						-		t REM	-	1.8	
D				,								t inh		3.6
ск, ін			2 1 2 1											
SI A, B			2		- 1									
ČL			i											
	-		utput Di	lving	$\dashv$									
Pin Name	.		Factor											
Q			18 18											
so			18		•	Minimur	n values for	r the typical	operating of	onditio	n.			
	1							worst case	operating o	ondition	n are	given by th	e ma	ximum delay
	ı				۱ '	multiplie	r.							
Function Ta	able													
	Γ		Input	s			Outputs							
Mode	CLK	CL	D	Α	В	SI	On, SO							
	1	н	Di	L	L	х	Di							
CLOCK	Н	н	х	L	L	х	Hold							
	×	L	×	×	×	×	L							
SCAN	н	Н	X	л	H .	Si	Hold							
	Н	Н	×	L	ប	×	Si							
					Note	: CLK	= CK + IH							

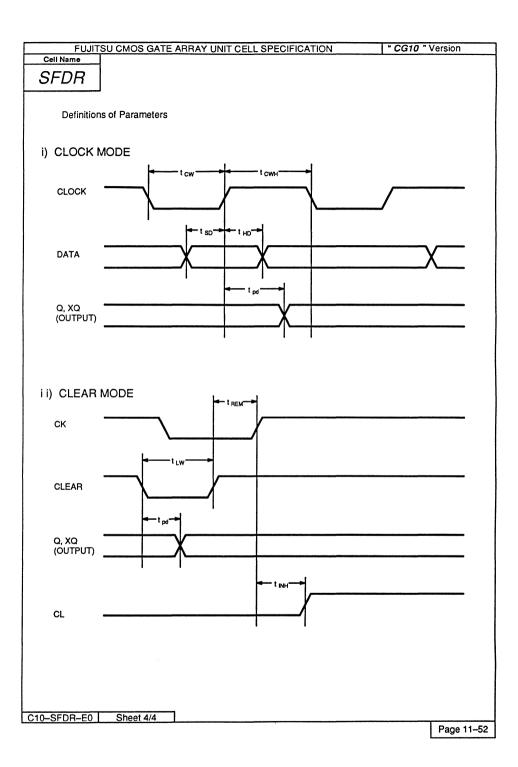
Sheet 1/4

C10-SFDR-E0

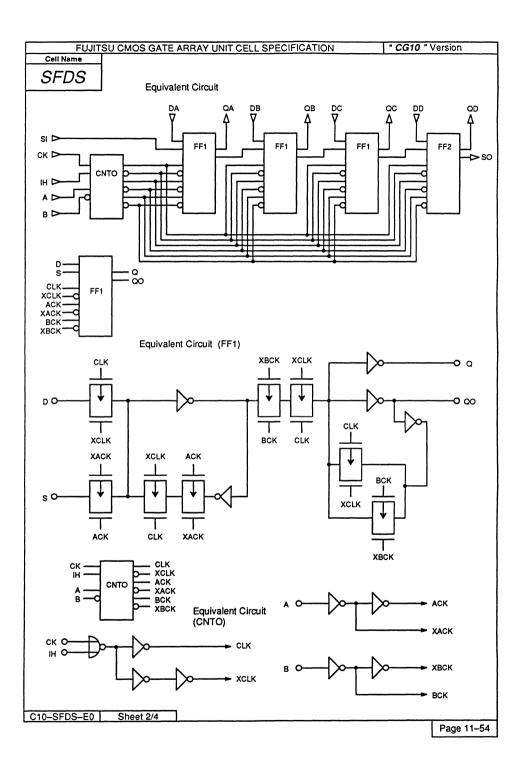
Page 11-49

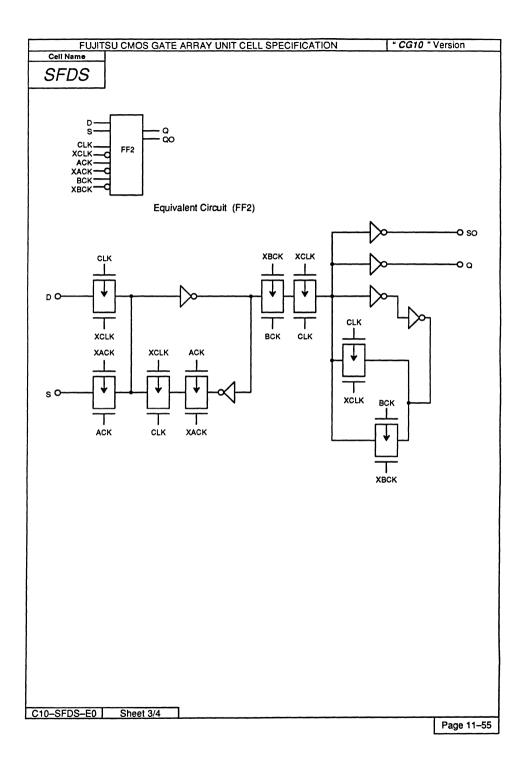






	III II TS	LLCM	08 G	ATE AL	DDAV	LIMIT	CELLS	SPECIFICA	ATION		" CG10	* V	ersion
Cell Name			nction	AIE AI	nhAi	UNIT	CELL 3	SPECIFIC/	ATION		Caro		Number of BC
SFDS	S	SCA	AN 4-	-input	DFF	with	Clock	Inhibit					31
	Cell	Symbol						Pro	pagation D		neter		
					<u> </u>	tu	p KCL	10		in KCI 2	CDR2	-	Path
					1.	919 056	0.067 0.067	1.888	0.056 0.056	0.090 0.090	4 4		( to QA~QC ( to QD
DA DB DC DD CK SI A B			······ (	DA DB DC DD									
						amete			·		Symbol		Typ (ns) *
						ock P	ulse Wic	ith no			tcw	-	2.9
					Clock Pause Time t cwh							<del>                                     </del>	2.0
					Da	ta Se	tup Tim	е			t <sub>SD</sub>		0.0
					Da	ita Ho	ld Time				t HD	<u> </u>	1.4
Pin Name D CK, IH SI A, B	•		eut Load Factor (1 2 1 2										
Di- No-			tput Dr		7								
Pin Name Q SO	•		18 18 18	iu)	1		ues for the	or the typical worst case			e given by th	ne ma	aximum delay
Function Ta	able												
			Inputs	;		Out	outs						
Mode	CLK	Dn	Α	В	SI	Qn,	so						
	<u>f</u>	Di	L	L	×	٥	ni l						
CLOCK	Н	×	_	L	×	Но							
	н	×	元	Н	^ Si	Ho							
SCAN	Н	X	J.L	T U	X	<del> </del>	Si						
	<u> </u>				te: CLI	L	 K + IH						
C10-SFDS	-E0 ]	Sh	eet 1/4										
												L	Page 11-53

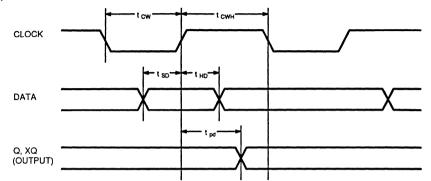




**SFDS** 

**Definitions of Parameters** 

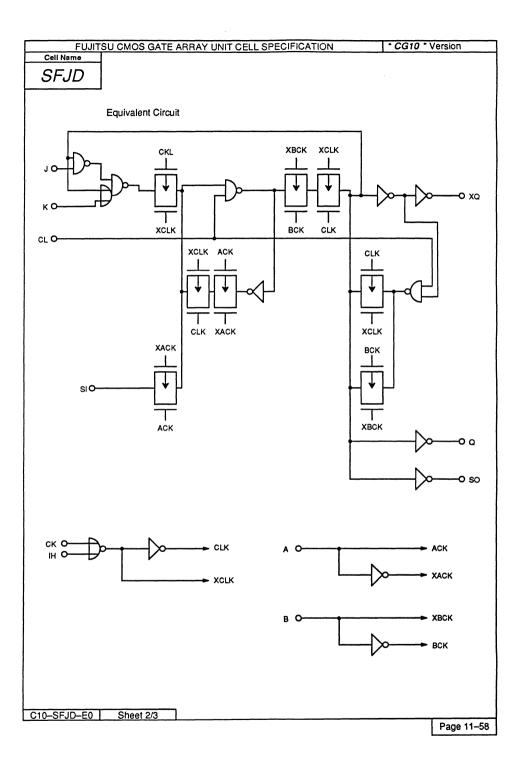
i) CLOCK MODE

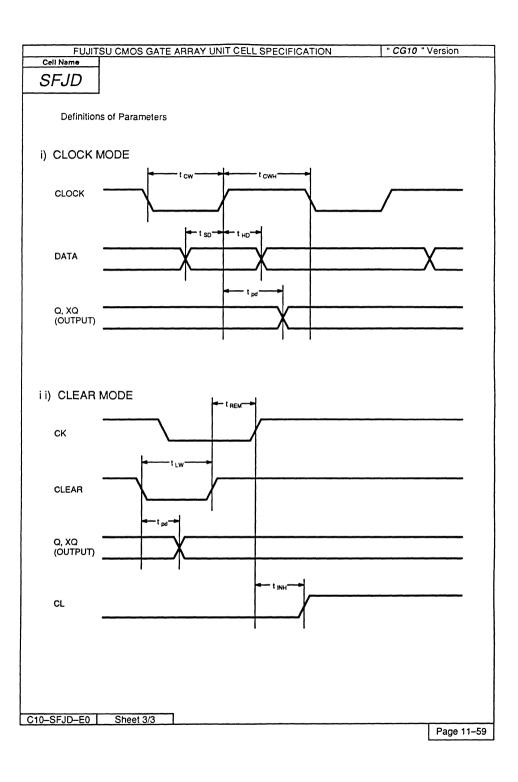


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C10-SFDS-E0 Sheet 4/4

	UJIT	SU CM	10S G	ATE A	RRAY	UNIT	CELL	SPECIFIC	ATION		" CG10	" V	
Cell Nam	•		unction										Number of
SFJL	)	SC.	AN J-	-K FF	with	Cloc	k Inhi	bit					14
	Cell	Symbo						Pro	pagation D	elay Paran	neter		·
						tu				dn			Path
					_	t O	KCL	t 0	KCL	KCL2	CDR2	_	
						.025	0.072		0.067	0.112	4		K to Q
						163	0.067		0.045	0.056	4		K to XQ
					[ ]	.750	0.067	1.544	0.051	0.095	4	١٠	L to Q,XQ
J - K - CK - IH - SI - A -			<b>—</b>	a xa so									
В -	<b>-</b> ₫_	٦											
		1			Pa	ramete	r	Symbol	$\vdash$	Typ (ns) *			
		CL					ulse W	idth			tcw		2.7
					Clock Pause Time town								3.1
					Data Setup Time         (J)         t sp           Data Hold Time         (J)         t нр							-	2.4
					10	ata Ho	ia I im	e (J)			t HD		0.4
		Int	put Loa	dina	10:	ata Se	tup Tir	ne (K)			t <sub>SD</sub>	-	2.0
Pin Name	,		Factor (				ld Tim			t HD		0.1	
J, K			1										
CK, IH SI			1 2				ulse W				t Lw	├	2.7
A, B CL			222				elease old Tim				t REM	<del> </del>	1.3 2.7
Pin Name Q XQ SO	•		18 18 18 18		'		es for th	for the typica			e given by th	ne ma	aximum delay
Function Ta	able								<del></del>				
Mode	<u> </u>	T 61		Inputs	г.	r -	T 6:	Outputs	$\dashv$				
	CLK	CL	J	К	A .	В	SI	Q, SO X	<u>-</u>				
	1	Н	L H	L	L	L	X	Hold Toggle	-				
0.00:	누			<del> </del>	<del> </del>	ļ	ļ		$\dashv$				
CLOCK	1	Н	L	Н	L	<u> </u>	×	L H					
	5	Н	Н	L	L	L	X	H L					
	Н	Н .	X	X	L	L	X	Hold					
	×	L	×	×	<u>×</u>	×	×	L F	<u>'</u>				
SCAN	н	Н	X	X	Ţ	H	Si	Hold					
L	Н	Н	х	×	L	<u>Г</u>	X	Si Si					
							Note:	CLK = CK	⊦ IH				
10-SFJD	-E0	Sh	eet 1/3	3								Т	Page 11-5
												L	. ago 11-0





3

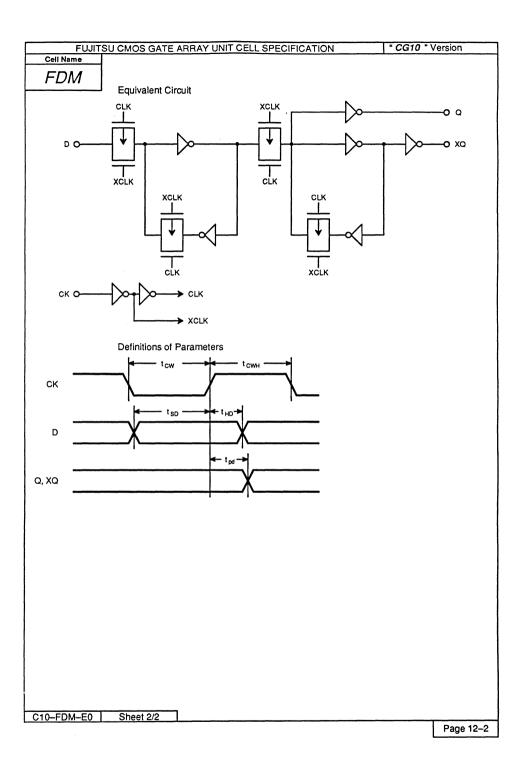
# 3

## Non-scan Flip-flop Family

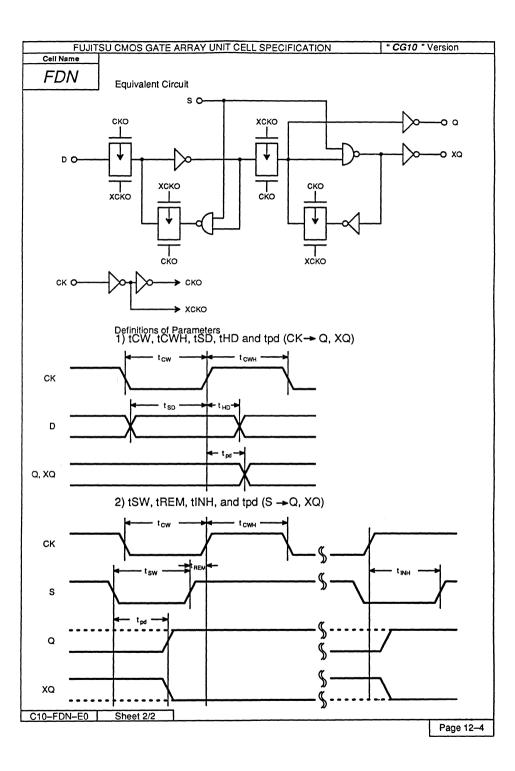
Page	Unit Cell Name	Function	Basic Cells
3–183	FDM	Non-scan D Flip-flop	6
3–185	FDN	Non-scan D Flip-flop with Set	7
3–187	FDO	Non-scan D Flip-flop with Reset	7
3–189	FDP	Non-scan D Flip-flop with Set and Reset	8
3-192	FDQ	Non-scan 4-bit D Flip-flop	21
3-194	FDR	Non-scan 4-bit D Flip-flop with Clear	26
3-197	FDS	Non-scan 4-bit D Flip-flop	20
3-199	FD2	Non-scan Power D Flip-flop	7
3-201	FD3	Non-scan Power D Flip-flop with Preset	8
3-203	FD4	Non-scan Power D Flip-flop with Clear and Preset	9
3-205	FD5	Non-scan Power D Flip-flop with Clear	8
3–207	FJD	Non-scan Positive Edge Clocked Power J-K Flip-flop with Clear	12

3

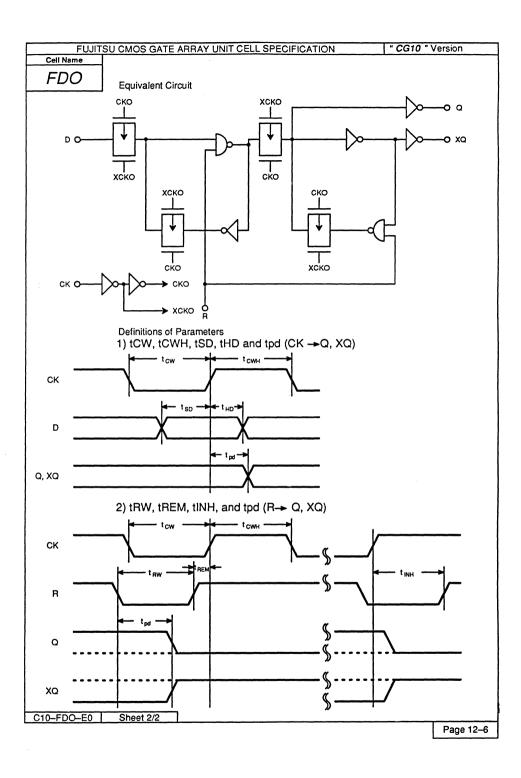
FILIIT	SU CMOS GATE AR	RAY LINIT	CELLS	PECIFIC	ATION		" CG10	" Version
Cell Name	Function	HAT CIVI	<u> </u>	1 2011 107	111011		1 00.0	Number of BC
FDM	Non-SCAN DF	F						6
Cell	Symbol			Pro	pagation D		neter	
		t O	KCL	t O	KCL	in KCL2	CDR2	Path
		1.094	0.067	1.125	0.051	KULZ	CDR2	CK to Q
		1.350	0.067	1.475	0.051			CK to XQ
D ——	°							
	р— хо						1 1	
L_							]	
		1					1 1	
		Paramete					Symbol	Typ (ns) *
			ulse Widt				t cw t cwH	2.5
		Clock Pause Time						2.5
		Data Se	tup Time				tsp	1.4
		Data Ho	t <sub>HD</sub>	1.0				
	Input Loading	-					]	
Pin Name	Factor (lu)							
D	2 1	1					1	
ск	1	}					1	
		1					l	
		]						
Pin Name	Output Driving Factor (lu)							
Q		1				1		
ΧQ	18 18	* Minimus The value multiplie	ues for the	r the typical worst case	operating o	ondition.	given by the	e maximum delay
Function Table								
Inputs	Outputs							
D CK	Q XQ							
н↑	H L							
∟ ↑	LH							
C10-FDM-E0	Sheet 1/2							
								Page 12-1



• /	Fu			RAY UNIT	CELL S	PECIFICA	ATION		" CG10	" Version	
	Non	nction								Number of Bo	
Cell	.,,	-SCA	N DF	with SI	ET					7	
	Symbol					Pro	pagation D		neter		
				t O	KCL	t O	KCL	in KCL2	CDR2	Path	
	s 			1.125 1.538 1.400	0.067 0.067 0.067	1.094 1.513 0.669	0.051 0.045 0.045	0.067	4	CK to Q CK to XQ S to Q, XQ	
		— a — ха									
										Typ (ns) *	
									t <sub>CW</sub>	2.5 2.5	
				CIOCK P	ause IIM	le			r CMH	2.5	
				Data Se	tup Time				t <sub>SD</sub>	1.4	
				Data Ho	t HD	1.0					
	Inn	ut Loadir	na	Set Puls	se Width				tsw	2.5	
	F	actor (lu	)	Set Rele	t REM	0.2					
		2 1		Set Hole	d Time				t <sub>INH</sub>	2.4	
,	Ou F	actor (lu	ing )	* Minimum values for the typical operating condition.							
		18				worst case	operating o	ondition are	given by th	e maximum delay	
able		r		7							
nputs		Ou	tputs	1							
D	ск	Q	XQ	_							
×	х	Н	L	1							
н	1	н	L	1							
	1	L	н	1							
	able nputs D	o Our F	Input Loadin Factor (lu)  2 2 1  Output Drivi Factor (lu) 18 18  able  nputs Output Drivi Factor (lu) 18 18	Input Loading Factor (lu)  2 2 1  Output Driving Factor (lu) 18 18  Able  Apputs Outputs D CK Q XQ X X H L	Paramete Clock P Clock P Clock P Data Se Data Ho  Input Loading Factor (lu) Set Rele 2 1  Output Driving Factor (lu) 18 18 18  Minimur The valumultiplie  able Inputs D CK Q XQ X X H L	Parameter  Clock Pulse Width Clock Pause Time Data Setup Time Data Hold Time  Input Loading Factor (lu)  2 1  Output Driving Factor (lu)  18 18 18  Ninimum values for the multiplier.  Able Inputs D CK Q XQ X X H L	Parameter Clock Pulse Width Clock Pause Time Data Setup Time Data Hold Time  Input Loading Factor (lu)  2 1  Output Driving Factor (lu)  18 18 18  Ninimum values for the typical The values for the worst case multiplier.  Able Inputs D CK Q XQ X X H L	Parameter Clock Pulse Width Clock Pause Time  Data Setup Time Data Hold Time  Set Pulse Width Set Release Time (S)  2 1  Output Driving Factor (lu)  18 18 18  * Minimum values for the typical operating or multiplier.  * Minimum values for the worst case operating or multiplier.	Parameter Clock Pulse Width Clock Pause Time Data Setup Time Data Hold Time  Input Loading Factor (lu) Set Release Time (S) Set Hold Time  Output Driving Factor (lu)  18 18 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are multiplier.  able Inputs Outputs D CK Q XQ X X H L	Parameter Symbol Clock Pulse Width tow Clock Pause Time town  Data Setup Time tsp Data Hold Time thp  Input Loading Factor (Iu) Set Release Time (S) trem  2 2 1  Output Driving Factor (Iu)  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the multiplier.  * Minimum values for the typical operating condition are given by the multiplier.	



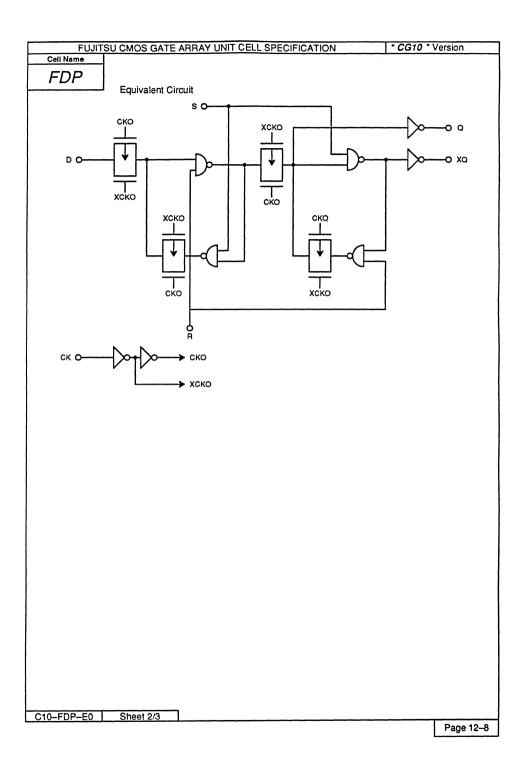
FUJIT	SU CM	OS GA	TE ARF	RAY UNIT	CELL S	PECIFIC	ATION		" CG10	" Versi	on
Cell Name		nction									umber of BO
FDO	Non	-SCA	N DFF	with R	ESET						7
Cel	Symbol					Pro	pagation D		neter		
					KCL	<del>                                     </del>	KCL	n KCL2			Path
				1.206 1.350 1.250	0.067 0.067 0.067	1.113 1.613 1.025	0.056 0.051 0.056	KOLZ	CDR2	CK	to Q to XQ o Q, XQ
р —	D R	— a — ха		Paramete Clock P	er ulse Widi	ih.			Symbol tcw		p (ns) * 2.5
					ause Tim				t cwh		2.5
				0.00	<u> </u>				20111		
				Data Se	tup Time				t <sub>SD</sub>		1.4
				Data Ho	old Time				t HD		1.0
	ln-	ut Loadii	20	Recet D	ulse Wid	th		-	t RW		2.5
Pin Name		actor (lu		Reset B	Release T	t REM		0.6			
D		2 2 1		Reset H	lold Time				t INH		2.1
R CK	Ou	1 tput Drivi	ing								
Pin Name		actor (lu		* Minimus	n values for	the trained	anaratina a	ondition.			
Q XQ		18 18			ues for the		operating o		given by the	e maxim	ım delay
Function Table											
Inputs		Ou	tputs								
R D	ск	a	ΧQ	]							
L X	Х	L	н	I							
н н	<b>↑</b>	н	L								
H L	1		Н								
				_							
C10-FDO-E0	She	eet 1/2	]_							Pa	ge 12–5

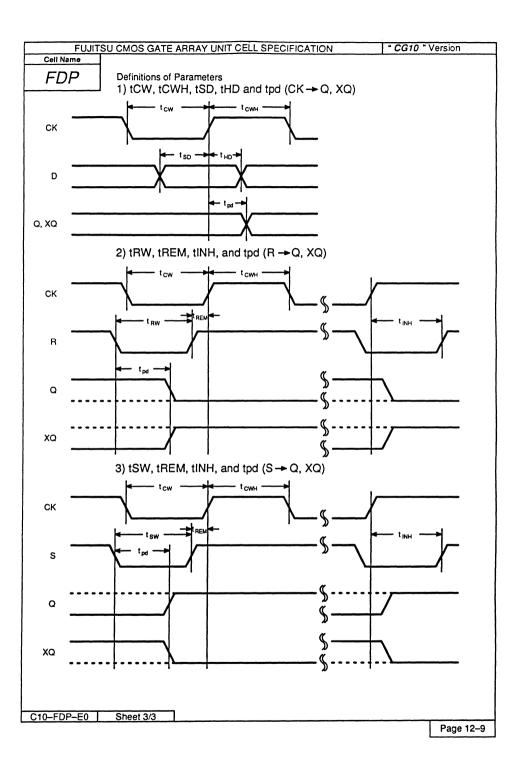


Cell Name			MOS GA	TE AR	RAY UNIT	CELLS	PECIFIC	ATION		* CG10 '	" Version Number of E
FDP				N DFI	with S	et and F	Reset				8
	Cei	Symbo	01		<del>                                     </del>	JD QI	Pro	pagation D	elay Parai In	meter	
					t O	KCL	i O	KCL	KCL2	CDR2	Path
		s I			1.225 1.531 1.400 1.588	0.067 0.067 0.067 0.067	1.100 1.563 0.994 0.631	0.056 0.051 0.056 0.051			CK to Q CK to XQ R to Q, XQ S to Q, XQ
D —			a xa	ı							
		Ř			Paramete					Symbol	Typ (ns) *
						ulse Wid				tow	2.5 2.5
					CIOCK	t cwn	2.5				
						tup Time				t <sub>SD</sub>	1.4
					Data Ho	old Time				t HD	1.0
		In	put Load	ina	Set Pul	2.5					
Pin Name	•		Factor (I	1) 8		ease Tim	e (S)			t sw	0.2
D			2		Set Hol	2.4					
S			2 2 2 1		Boast F	Vilaa VACid	4h				2.5
R CK			1			Pulse Wid Release T				t REM	0.6
						lold Time				t inn	2.1
Pin Name	•	0	utput Dri Factor (I								
Q			18	<u> </u>							
XQ			18	~~~~~		ues for the		operating o		e given by the	maximum delay
Function Ta	able										
	Inp	uts		Out	puts						
		D	СК	a	ΧQ						
S	R			L	Н						
S	R L	×	Х	_							
ļ		×	×	н	L						
H	L H	x	x	н	- 1						
H L L	L H L	x x	x x	H Inhil	oited						
H	L H	x	x	н	- 1						

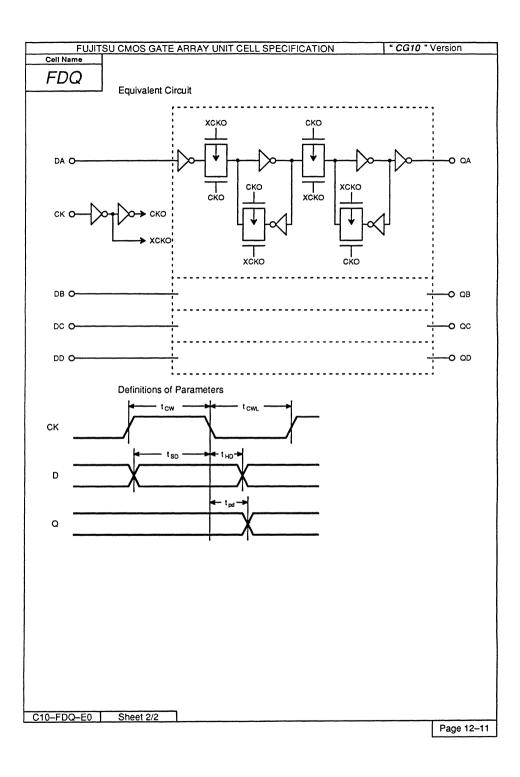
C10-FDP-E0 | Sheet 1/3

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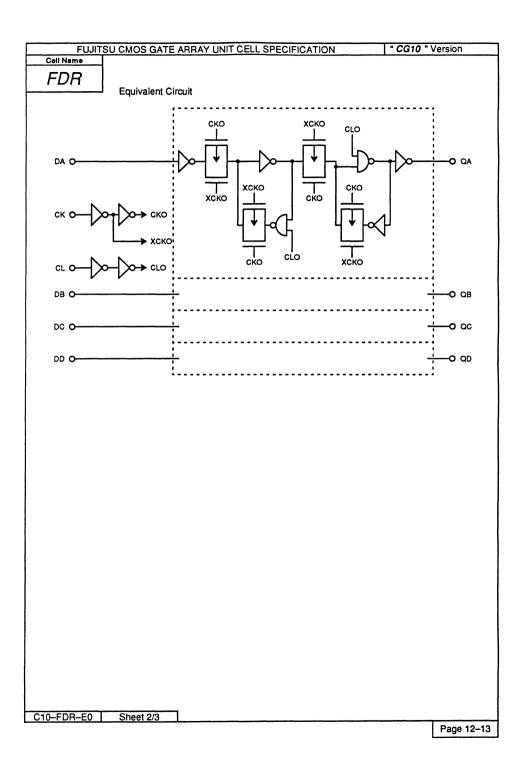


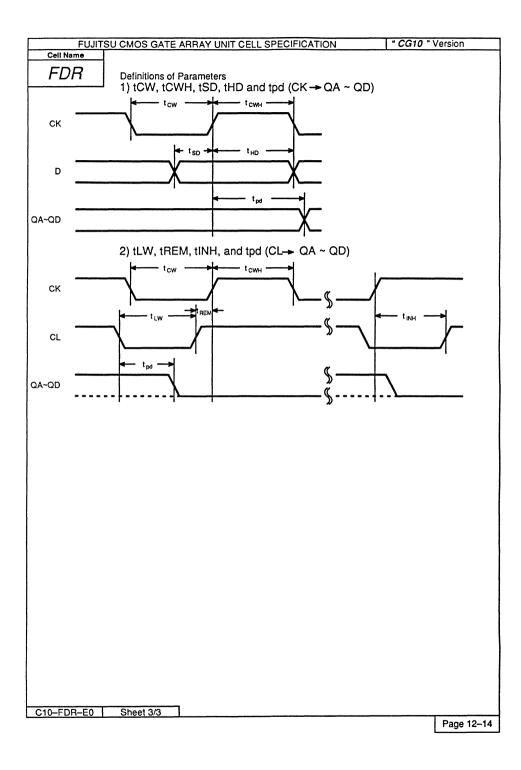


	SU CMOS GATE AF	RRAY UNIT	CELLS	PECIFIC	ATION		" CG10 "	
Cell Name	Function							Number of BC
FDQ	Non-SCAN 4-	bit DFF						21
Cell	Symbol	T		Pro	pagation D	elav Paran	neter	
		tı	ıb			in		D-#
		t 0	KCL	t O	KCL	KCL2	CDR2	Path
		2.106	0.067	1.713	0.045		] ]	CK to Q
}		1						
		1						
DAD	BDCDD	1						
1								
1 -	느ㅋ							
	QA QB							
ск — ф	QC	1						
	QD	1						
•							<u> </u>	
		Paramete					Symbol	Typ (ns) *
		Clock P	ulse Wid ause Tim	in			t cwL	2.5 2.5
		CIOCKI	1 CWL					
			tup Time				t <sub>SD</sub>	0.7
		Data Ho	old Time				t HD	1.8
	Input Loading	-					ŀ	
Pin Name	Factor (lu)							
D CK	1	7						
ск	1	1				1	1	
}						1	]	
							l	
Pin Name	Output Driving	7					ļ	
Q	Factor (lu)	-						
"	10	* Minimu	m values fo	r the typical	operating of	ondition.		
							given by the	maximum delay
		multiplie						
Function Table								
·	T Outsut							
Input	Output							
CK D	0							
↓ н	н							
	L							
1								
}								
C10-FDQ-E0	Sheet 1/2							
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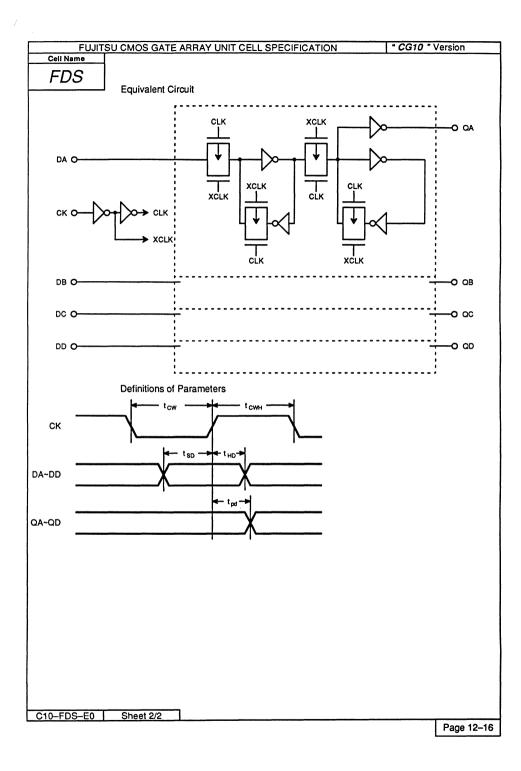


	EI I IIT	'C11	CMOS G	ATE ADD	RAY UNIT	CELLS	DECIEIC	ATION		" CG10 "	Version
Cell Nam	•	L	Function		IOI OIVII	OELL S	FEOIFIC	TION			Number of BC
FDF	?	١	lon-SC	AN 4-b	it DFF v	vith CLE	AR				26
	Cel	Syn	nbol				Pro	pagation D	elay Paran	eter	
						ip qu			in		Path
1					10	KCL	10	KCL	KCL2	CDR2	
-					1.650	0.067	2.263 1.363	0.045 0.045		l	CK to Q CL to Q
					-	_	1.363	0.045		i i	CLIOQ
						l		ł		l 1	
	DAD	BDC	DD		i	l					
		Ш	ı		İ	İ					
I	۲,		ጎ		İ	[					
	1			QA QB		1					
ск —	-		1	QC QC		1					
				QD	l	1					
1	L	<del>Q</del>			1	1					
1		1			L					L	
1		ĊL			Paramete					Symbol	Typ (ns) *
ł						ulse Wid				tcw	2.5
l					CIOCK P	ause Tim	ie			t cwH	2.5
İ					Data Se	tup Time				t sp	0.7
1						old Time				t HD	1.8
Pin Name	Pin Name Input Loading Factor (lu)			ding		ulse Widt				t <sub>LW</sub>	2.5
	Pactor (IU)				elease Ti old Time	me			t REM	1.0 2.9	
D CK		١	1		Olear Flora Time					INH	
CL			1						1	}	
		1			l				1		
ļ		├-	Outros D	1.1						1	
Pin Name	•	ļ	Output Dr Factor (		l					j	
a			18								
		l				m values fo					
		İ					worst case	operating o	ondition are	given by the	maximum delay
					multiplie	<b>∌</b> r.					
		<b></b>			·				~~~~		
Function T	able				_						
	Inpu	ıts		Output							
СК	D		CL	a							
×	×		L	L							
	١ι		н	L							
1	H		н	н	1						
			п	- 17	l						
1											
1											
1											
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											1 ago 12-12

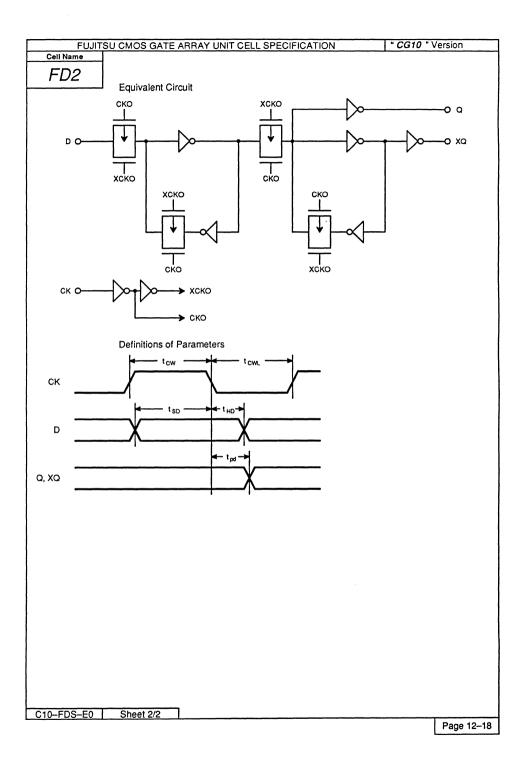




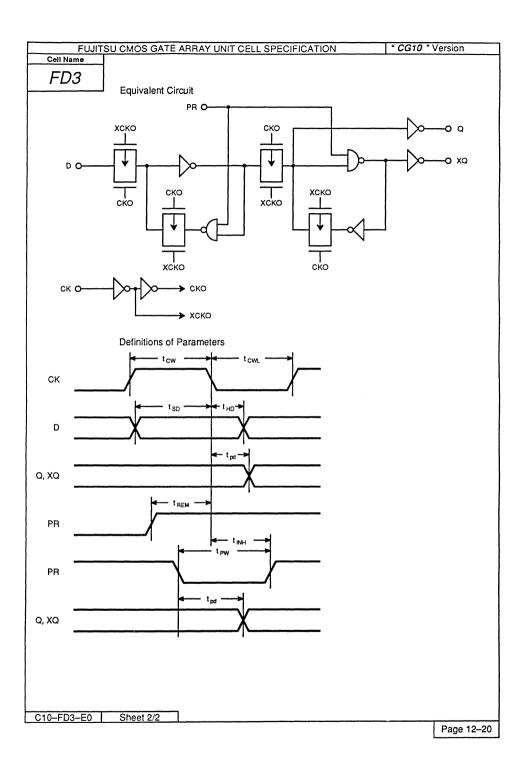
F	UJITS	U CMOS GA	ATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG10	" Versio	n
Cell Name		Function									mber of BC
FDS	-	Non-SC/	AN 4-b	it DFF							20
	Cell	Symbol				Pro	pagation D		neter		
				t O	KCL	t O	KCL to	In KCL2	CDR2	F	ath
ск ——	DADE	(	QA QB	1.894	0.067	1.531	0.051			СК	to Q
			9D	Clock P	ulse Widt ause Tim etup Time	е			Symbol tcw tcw+	2	(ns) * 2.5 2.5
				Data Ho	old Time				t HD		1.6
Pin Name		Input Load Factor (I									
D CK		2 1									
Pin Name		Output Dri Factor (									
a		18			ues for the		operating o		e given by th	e maximu	m delay
Function Ta	ble										
inp	uts	Outputs									
СК	D	a									
1	L	L									
↑	н	н									
C10-FDS-	E0	Sheet 1/2								- 1	
										Pag	e 12–15



Cell Name	SU CMOS G	ATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG10	" Version
ED0	Function								Number of BC
FD2	Non-SC	AN Pov	ver DFF						7
Cell	Symbol				Proj	pagation D	elay Parar	neter	
				ib			In		Path
			10	KCL	t O	KCL	KCL2	CDR2	
			1.031	0.034	1.075	0.028	0.056	7	CK to Q
			1.594	0.034	1.463	0.023	0.039	7	CK to XQ
								1 1	
								1 1	
								1 1	
D —	°								
ск — с									
	b x	2						1	
L	^	<b>~</b>						1 1	
			<u> </u>					1	
			Paramete		<u> </u>			Symbol	Typ (ns) *
				ulse Widt			—-}	tcw	2.5 2.5
			Clock P	ause Tim	е			t cwL	2.5
			Data Setup Time					t <sub>SD</sub>	1.4
			Data Ho	old Time		<del></del>		t HD	1.0
			Data inc	no mino				. 40	
D1 . M	Input Load	ling	i						
Pin Name	Factor (	lu)					1		
O	2 1								
СК	1						1	1	
							-		
			}				1		
	0.44.0-						i		
Pin Name	Output Dr Factor (	iving lu)					1	ļ	
0		/					- 1		
Q XQ	36 36		* Minimur	n values for	the typical	operation o	ondition		
								given by the	e maximum delay
			multiplie					•	•
			L						
For Mark Take									
Function Table			_						
	Outp	outs	]						
Inputs			i						
Inputs CK D	a	XQ	l						
CK D									
		L H							



F	UJIT	SU CMOS G	ATE ARE	RAY UNIT	CELL S	PECIFIC	ATION		" CG10	" Ve	ersion
Cell Name		Function									Number of BC
FD3		Non-SC	AN Pov	ver DFF	with Pr	eset					8
	Cell	Symbol				Pro	pagation D		neter		
				t O	KCL	t O	KCL	In KCL2	CDR2		Path
				1.069	0.025	1.081	0.023	0.056	7	-	CK to Q
i				1.750	0.025	1.563	0.023	0.039	7		CK to XQ
				1.494	0.025	0.569	0.023	0.039	7		PR to Q, XQ
										Ì	
		PR 			!						
		Y			ļ						
D	$\Box$	¬。	)	l	l						
ск —	٦										
CK	٦٩				1						
	1.	р— х	Q	l	İ						
				į	l						
				Paramete	<u> </u>	L	L		Symbol		Tim (no) 8
					ulse Wid	h			t cw		Typ (ns) * 2.5
					ause Tim				t cwL		2.5
					etup Time				t <sub>SD</sub>	<u> </u>	1.4
				Data Hold Time							1.0
Din Name	Pin Name Input Loading				Pulse Wid	ith			t pw		2.5
	Factor (lu)				Release T				t REM		0.2
D CK		2 1 2		Preset Hold Time					t INH	<u> </u>	2.4
PR	- 1	ż									
		0		l				ĺ			
Pin Name	,	Output Di Factor	riving (lu)					1			
Q XQ		36 36	·	[							
XQ	- 1	36			m values fo						
				The val multiplie		worst case	operating o	ondition are	given by th	e ma	ximum delay
				Indiapile	J1.						
Function Ta	able										
	Inpu	ts	Out	puts							
PR	СК	D	Q	ΧQ							
L	×	×	н	L							
н	↓	н	н	L							
]	1			l							
Н	*	L	L	н	l						
C10-FD3-	EO I	Sheet 1/2	2								
0.0.00	<u> 1</u>	Q.7001 17								T	Page 12-19
										L	<u> </u>

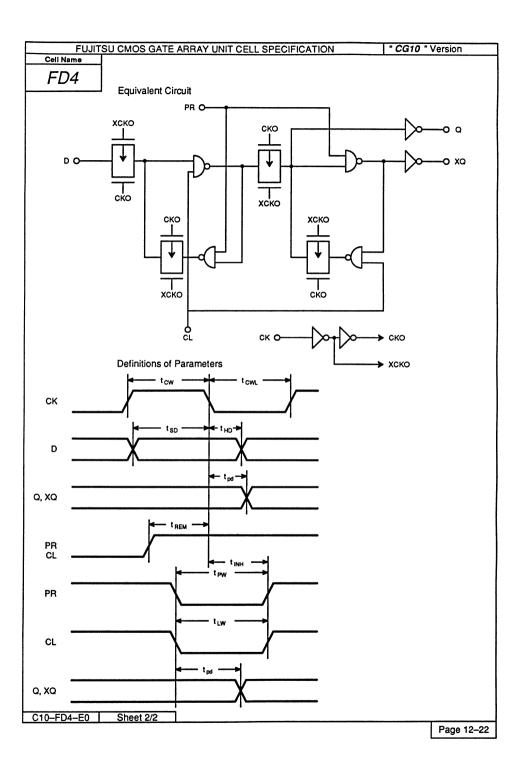


FUJIT	TSU CMOS GATE AF	RRAY UNIT	CELL S	PECIFIC	ATION		" CG10	" Version
Cell Name	Function							Number of
FD4	Non-SCAN Po	wer DFF	with CI	ear and	Preset			9
Ce	II Symbol	T		Pro	pagation D	elay Paran	neter	
		tı	φ			dn		Path
		t O	KCL	t O	KCL	KCL2	CDR2	
<sub>0</sub> —	PR O	1.188 1.756 1.544 1.556	0.030 0.025 0.025 0.030	1.075 1.700 0.913 0.575	0.028 0.023 0.028 0.023	0.056 0.039 0.056 0.039	7 7 7 7	CK to Q CK to XQ CL to Q, XC PR to Q, XC
ск — сь			ulse Wid				Symbol tow	Typ (ns) * 2.5 2.5
		Clock Pause Time tcw.						
		Data Se	tup Time				t sp	1.4
		Data Ho	old Time				t HD	1.0
	Input Loading	Preset I	Pulse Wid	ith			t pw	2.5
Pin Name	Factor (lu)		Release				t REM	0.2
D	2		Hold Time				tinh	2.4
CK	2							
CL PR	2 2		ulse Wid				tıw	2.5
FFI	1		elease Ti	me			t REM	0.6
		Clear H	old Time				t inh	2.1
Pin Name	Output Driving Factor (lu)							
a xa	Q 36				operating o		given by the	e maximum delay

	Inp	uts		Out	puts
PR	CL	СК	D	σ	ΧQ
L	н	x	×	н	L
н	L	×	x	L	н
Н	н	1	н	н	L
н	Н	↓	L	L	н

C10-FD4-E0 Sheet 1/2

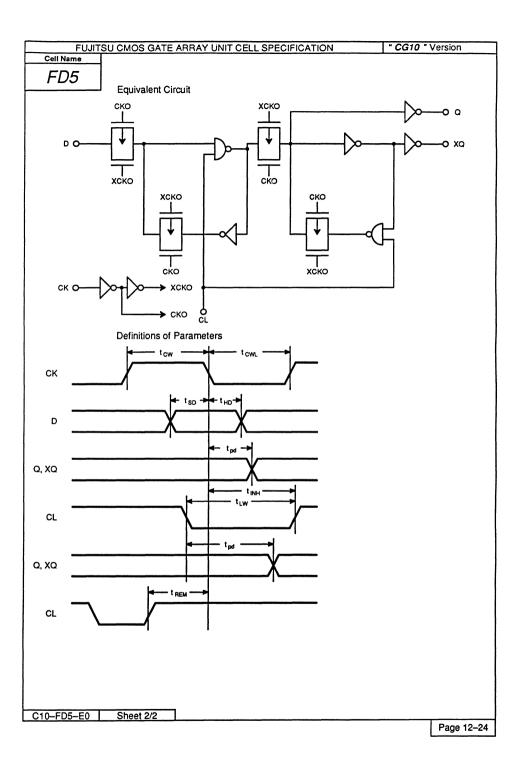
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F	UJITS	U CMOS G	ATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG10	" Version
Cell Name	•	Function								Number of B
FD5	1	Non-SC	AN Pov	ver DFF	with CL	EAR				8
	Cell S	Symbol				Pro	pagation D	elay Para	meter	
					ıρ			in		Path
				1.175 1.606 1.475	0.034 0.034 0.034	1.069 1.606 0.950	0.028 0.023 0.028	0.056 0.039 0.056	7 7 7	CK to Q CK to XQ CL to Q, XQ
D — СК —	-[	~ ×	a a				:			
	Ċ	L		Paramete					Symbol	Typ (ns) *
					ulse Widt				t cw	2.5
				Clock P	ause Tim	ie			t cwl	2.5
				Data Sc	etup Time				t sp	1.4
					old Time				t HD	1.0
				Data in	JIG TITLE				• 110	
		Input Loa	dina	Clear P	ulse Wid	th			tıw	2.5
Pin Name	'	Factor (		Clear R	elease Ti	me			t REM	1.0
D		2		Clear H	old Time				t inn	2.9
CK	]	1						- 1		
CL		2								
		Output Dr	ivina							i
Pin Name		Factor		]						
αŝ		36 36		ļ						
ΧQ		30							e given by th	e maximum delay
Function Ta	uble			I					***************************************	
	inputs		Out	puts						
CL	СК	D	α	ΧQ						
	Х	×	L	Н						
L										
H	† †	н	н	L						

C10-FD5-F0	Sheet 1/2

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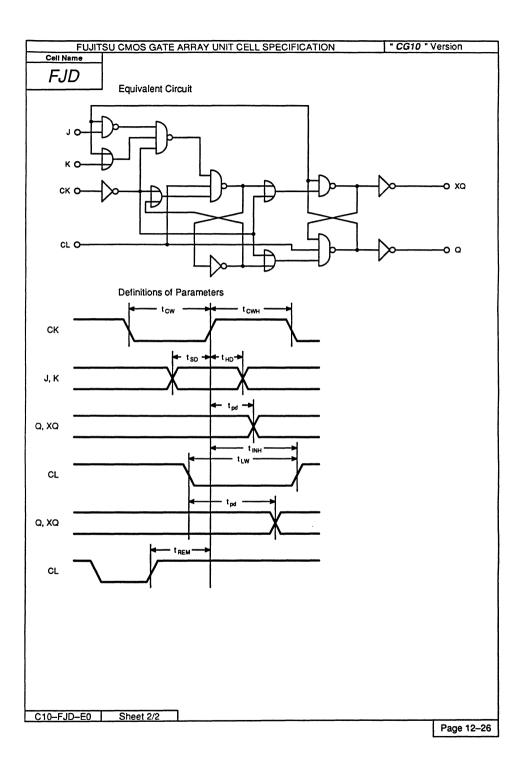


FUJI	TSU CMOS GATE AF	RAY UNIT	CELL S	PECIFICA	ATION		" CG10	" Version
Cell Name	Function							Number of Bo
FJD	Non-SCAN Po	sitive ed	ge clock	ed Pow	er JKFf	with C	lear	12
Ce	Il Symbol	T		Pro	pagation D	elay Parar	neter	
		tı	ρ		to	in		Path
		t O	KCL	t O	KCL	KCL2	CDR2	
J — ск — к	~ ×a	2.750 2.769 1.500	0.034 0.034 0.034	1.850 1.550 0.806	0.028 0.028 0.028	0.045 0.045 0.045	7 7 7	CK to Q CK to XQ CL to Q, XQ
	c'L	Paramete	er		·		Symbol	Typ (ns) *
		Clock P	ulse Wid	h			t cw	3.5
		Clock P	ause Tim	е			t cwn	3.5
			up Time				t <sub>SD</sub>	1.6
		J, K Ho	ld Time				t HD	8.0
	1	Class D	ulaa Mid	<u> </u>			•	2.5
Pin Name	Input Loading Factor (lu)		<u>ulse Wid</u> elease Ti				t LW	1.6
			old Time	1116			t INH	2.9
CL J K CK	2 1 1 1 1	Olean II	Old Tillle				• 11477	
Pin Name	Output Driving Factor (Iu)	]						
xa 	Q 36 XQ 36		m values for ues for the v				given by th	e maximum delay

	Inp	uts		Out	outs
CL	СК	J	к	Q	XQ
L	н	×	×	L	н
Н	1	L	L	∞	XQ0
н	1	L	н	L	н
н	1	н	L	н	L
н	1	н	н	XQ0	Q0

C10-FJD-E0 Sheet 1/2

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# 3

## **Scan Counter Family**

Page	Unit Cell Name	Function	Basic Cells
3–211	SC7	Scan 4-bit Synchronous Binary Up Counter with Parallel Load	62
3–216	SC8	Scan 4-bit Synchronous Binary Down Counter with Parallel Load	66
3–221	SC43	Scan 4-bit Synchronous Binary Up Counter with Asynchronous Clear	59
3-225	SC47	Scan 4-bit Synchronous Binary Up/Down Counter	78

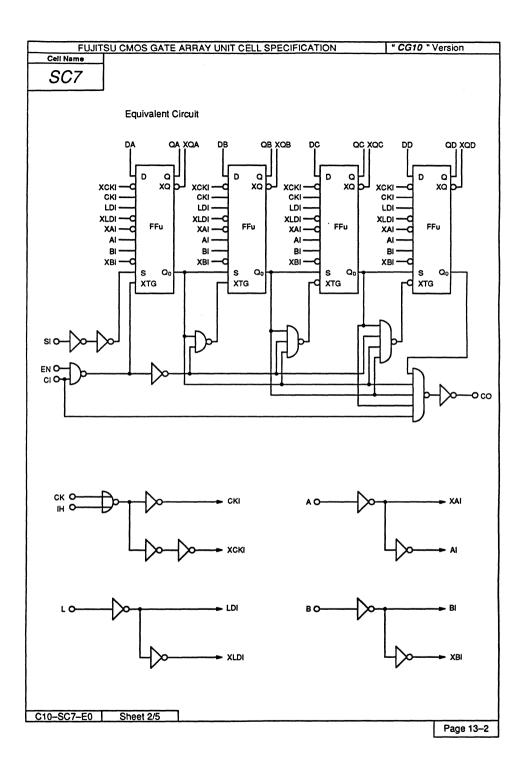
	SU CMOS GATE AR	HAT UNII	CELL S	PECIFICA	ATION		CGIO	" Version
Cell Name	Function							Number of
SC7	SCAN 4-bit Syl Up Counter with	nchronol n Paralle	us Binar I Load	У				62
Cell	Symbol	T		Pro	pagation D	elay Para	meter	
		tı	ıp		to	in		Path
		t O	KCL	tÖ	KCL	KCL2	CDR2	Pan
		2.063	0.034	1.906	0.034	0.084	7	CK,IH to Q
		3.613	0.034	3.338	0.034	0.084	7	CK,IH to XC
		4.875	0.034	3.269	0.023	_	-	CK,IH to CC
DA	l	1.250	0.034	0.625	0.023	_	-	CI to CO
DB —	QA						1	
DC —	р хо <sub>л</sub>							
DD —	OB_	1						
	р— хов							
ск——	oc							
#	D	Paramete				<u> </u>	Symbol	Typ (ns) *
r — d	D XQD		ulse Widt	h			tcw	4.5
	EN CO		ause Tim				tcw	4.5
			ause int				· CWH	
ă——		Data Se	tup Time				t sp	1.3
:;—d			ld Time				t HD	2.1
<u> </u>								
			etup Time				t st	4.0
		Load Ho	old Time				t HL	2.3
Pin Name	Input Loading	CI Setu	o Time				t sc	4.5
	Factor (lu)	CI Hold	Time				t HC	1.7
D	. 1							
CK IH	1	EN Setu					t se	4.5 1.7
im L	i	EN Hold	ııme				t HE	1./
ČĪ	2 1	Ì						
EN Si	1	1						
A,B		1						
		1						
Pin Name	Output Driving Factor (lu)							
a	36	1						
XQ CO	XQ 36		Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.					

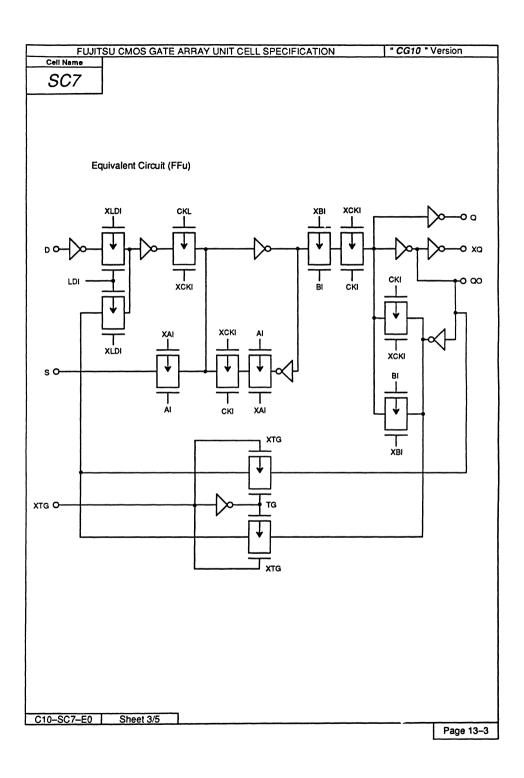
Mode	Inputs											
	CI	EN	L	CLK	Dn	Α	В	SI	On			
сьоск	x	×	L	5	Di	L	L	×	Di			
	Н	Н	н	F	х	L	L	×	Count Up			
	L	×	Н	F	×	L	L	×				
	×	L	н	F	×	L	L	×	No Count			
22411	×	×	×	н	×	Л	Н	Si	]			
SCAN	х	х	х	Н	х	L	V	х	Si			

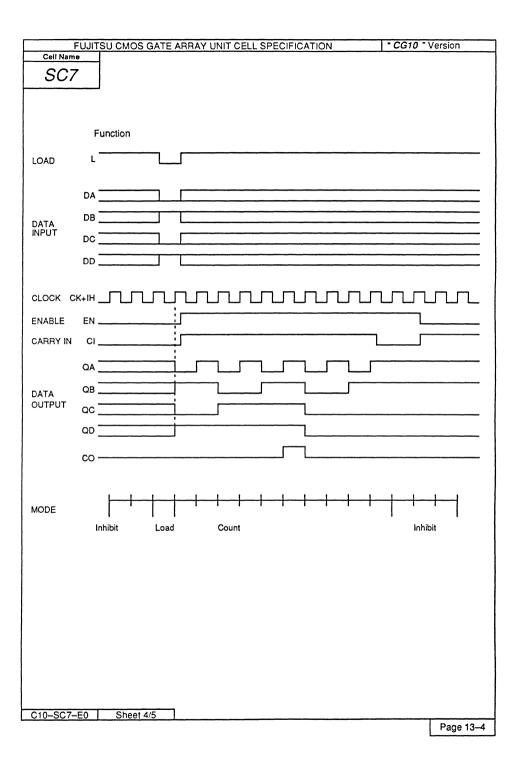
Note : CLK = CK + IH n = A ~ D

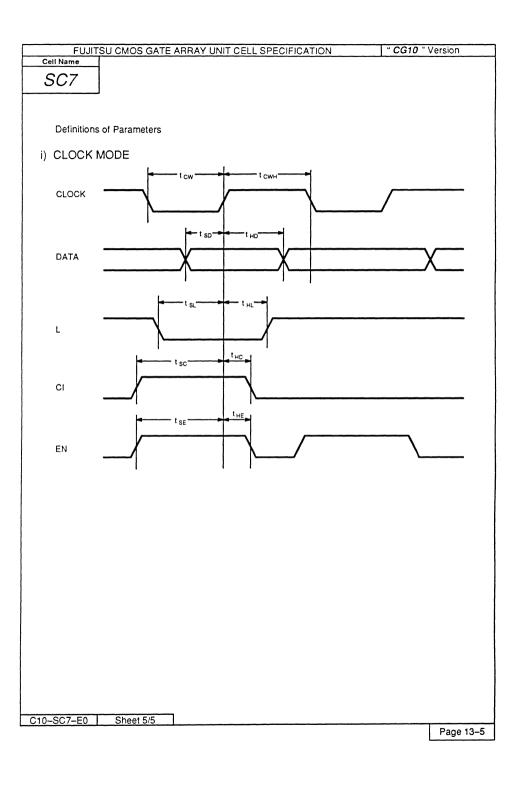
C10-SC7-E0 Sheet 1/5

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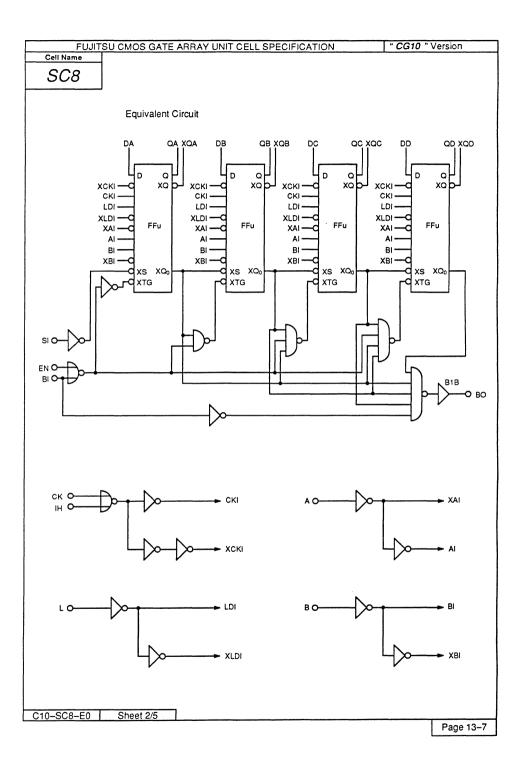


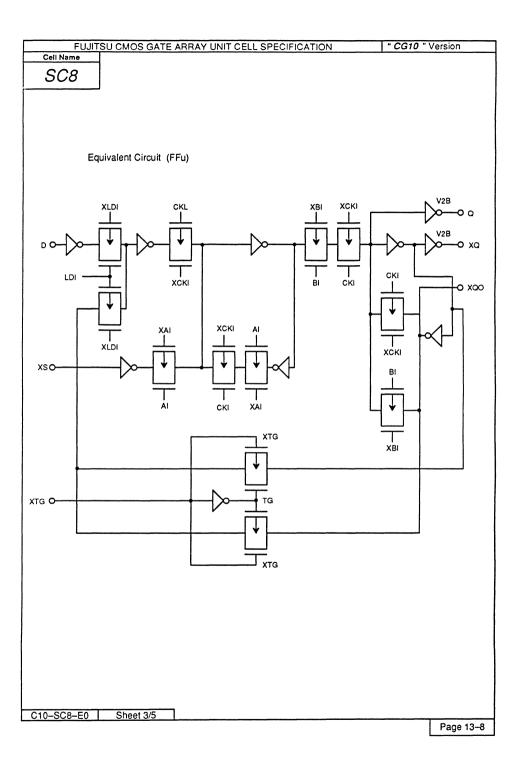


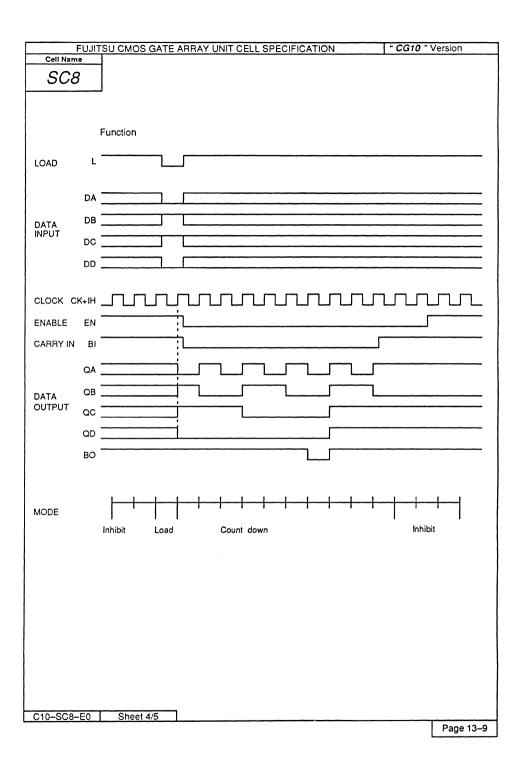




FUJI	SU CM	1OS G	ATE A	RRAY	UNIT	CELL	SPEC	IFICA	TION			" CG10	" Ve	ersion	
Cell Name	F	unction												Number of B	
SC8	SC.	AN 4 wn Co	-bit S ounter	ynch with	ronou Para	is Bina Illel Lo	aly ad							66	
Ce	Symbo		Propagation De								aram	eter			
					tup tdn									Path	
					10	KCL		0	KCL	KCL		CDR2	_		
					2.106   0.030   1.988   0.034   0.073   7     2.750   0.025   2.700   0.023   -   -							K,IH to Q			
						0.025			0.023 0.023	_		_		K,IH to XQ K,IH to BO	
. r		-   4.006   0.034   5.231   0.023   -     0.931   0.034   1.419   0.023   -							_		BI to BO				
DA —		-	- QA	"		0.00	"		0.020					D. 10 DO	
DC —		P-	- XQA												
DD —		_	- QB - XQB	1				Ì		İ					
ск ——		F		1											
IH —										<u> </u>					
rd	QD				ramete		-141-				_	Symbol		Typ (ns) *	
BI — Q		ρ-	- XOD			ulse Wi ause Ti						t cw t cwh		4.3	
SI —		b	- во	۳	OCK I	1036 11	me			T CWH					
A						tup Tin						1.3			
в—		1		Di	ata Ho	ld Time	<del>}</del>					t HD		2.1	
		_		17	ad Se	tun Tin	ne				_	t sı.	-	4.0	
					Load Setup Time Load Hold Time							t HL		2.3	
Pin Name		out Loa Factor (			EN Setup Time         t se           EN Hold Time         t HE							5.1 1.2			
D	<del>                                     </del>	1	,	<del>    -</del>											
СK	) i					BI Setup Time								5.1	
IH L		1		BI	BI Hold Time							t HB		1.2	
BI EN		2													
SI		1		-											
A,B		1		1											
Pin Name		tput D													
<u> </u>		Factor 36	(lu)	-											
XQ		36 36		1.	Minimur	n values	for the	typical	operation	conditio					
ВО		36		'	<ul> <li>Minimum values for the typical operating condition.</li> <li>The values for the worst case operating condition are given by the maximum delay</li> </ul>										
				'	nultiplie	r.									
	<u> </u>														
Function Table															
Mode		γ		uts	<del></del>			Outputs							
BI	EN	L.	CLK	Dn Di	A .	B	SI	ļ	On Di						
, 1 .	X	L			L			├							
X	+		F	Х	L	L	×	Count	Down						
CLOCK L	L	H		y	1 1				i						
CLOCK X	Н	Н	f	X	L		Y	No.	Sount						
CLOCK X	H X	н	<u>f</u>	Х	L	L	X Si	No C	Count						
CLOCK X	Н	Н	f			L			Count						
CLOCK X H SCAN X	H X X	H H X	<b>4</b>	x	Υ	ь Г	Si X Note: C		Si CK + IH						
CLOCK X H SCAN X	H X X	H H X	н н	x	Υ	ь Г	Si X Note: C	:LK =	Si CK + IH						





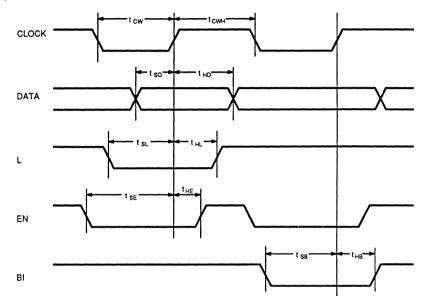


FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION

" CG10 " Version

Page 13-10

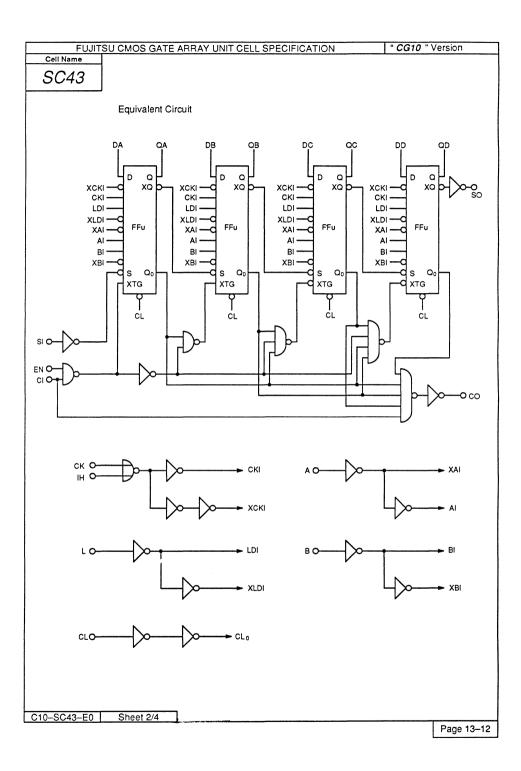
i) CLOCK MODE

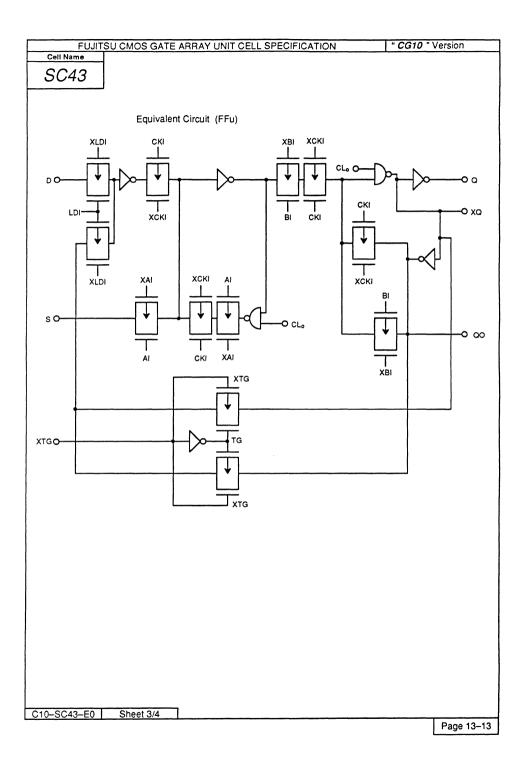


3

C10-SC8-E0 Sheet 5/5

Cell Name		ITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG10" Version													
	•		nction										Number of B		
SC43	3			-bit Sy nchror			s Bina r	ry Up					59		
	Cell	Symbol							Prop	agation De		neter			
					<u> </u>	tup		<del> </del>		td		T 0000	Path		
						0	KCL	t'		KCL	KCL2	CDR2	CICATIO		
			2.669   0.067   2.569   0.045   0.067   3.219   0.067   3.438   0.045   0.067							4	CK to Q CK to CO				
DA -	_	- 1		2A	3.	_	0.067	1.6		0.045	0.067 0.067	4	CL to Q		
DB -		-		ΣВ	1.	138	0.067	0.7		0.045	0.067	4	CI to CO		
DC —		H		C		-	_	2.2		0.045	0.067	4	CL to CO		
DD —		ŀ	<del></del> (	D D		i		1							
ск <del>-</del>					1	i		1		1					
iH —	-				1	l									
L	<b>-</b> q	ĺ			- 1	- 1									
CI — EN —				0	-			1				į.			
si —		- 1	5	80	-			1							
A		1				l				ļ					
в —	<b>-</b> •				Pa	ameter		ــــــــــــــــــــــــــــــــــــــ			1	Symbol	Typ (ns) *		
	<u> </u>	ᡨ					Ise Wi	dth				tcw	3.2		
					CI	ock Pa	use Ti	me				t cwн	4.6		
		CL					up Tim					t <sub>SD</sub>	1.2		
							d Time			t HD	1.4 1.9				
							ld Time			t st t HL	1.5				
		Inp	ut Load	ling			Time					tsc	2.5		
Pin Name	,	Factor (Iu) CI Hold Time										t HC	1,1		
D	1		2 1				p Time			t se	2.5				
CK, IH L, CL, SI			1			Hold	Ise Wid	lth.		t HE t LW	1.1 3.9				
EN	- 1		1				lease 1			t REM	0.9				
A, B, CI			2			Clear Hold Time							3.6		
Di N			tput Dri												
Pin Name Q	<del>'</del>		actor (	u)	-										
co			18		l	* Minimum values for the trained energing and distant									
so			18			Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay.									
						nultiplier		,	•						
	L														
	able														
Function Ta					1				_						
					Inputs					Outputs	·				
Function Ta	CI	EN	CL	CLK	L	Dn	Α	В	SI	Outputs Qn, SO	4				
	CI	EN X	CL L	CLK		Dn X	A X	В	SI X	<del> </del>	4				
				×	L	<u> </u>	1			Qn, SO	4				
Mode	х	×	L	х	L X	х	х	х	X	Qn, SO					
	X X H X	x	H H	X 4 H	L X L H	X Di X X	X L	X L	X X X	Qn, SO L Di Count U	- - - -				
Mode	X X H	X X H	H H	× <u>•</u>	X L H	X Di X	X L L	X L L	x x x x	Qn, SO L Di	- - - -				
Mode	X X H X X	X X H X L	1 H H H	х н х	L X L H H	X Di X X X	X L L L	X L L L	x x x x x	Qn, SO  L  Di  Count U <sub>I</sub>	- - - -				
Mode	X X H X X L X	X X H X L X	H H H H	х  н х х	L X L H H H	X Di X X X X	х L L L	X L L L	X X X X X X Si	On, SO  L  Di  Count Up  No Count	- - - -				
Mode	X X H X X	X X H X L	1 H H H	х н х	L X L H H	X Di X X X	X L L L	X L L L	x x x x x	Qn, SO  L  Di  Count U <sub>I</sub>	- - - -				
Mode	X X H X X L X	X X H X L X	H H H H	х  н х х	L X L H H H	X Di X X X X	х L L L	L L L L H	X X X X X X Si X	On, SO  L  Di  Count Up  No Count	P H				
Mode	X H X X L X	X X H X L X X	H H H H	х Н Х Х Н	L X L H H H	X Di X X X X	х L L L	L L L L H	X X X X X X Si X	On, SO L Di Count Up No Count Hold Si = CK + I	P H		Page 13–11		

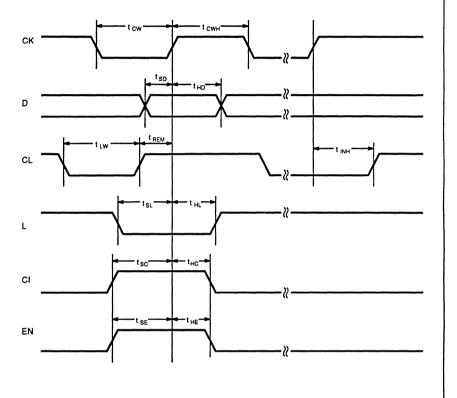




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**Definition of Parameters** 

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION



C10-SC43-E0

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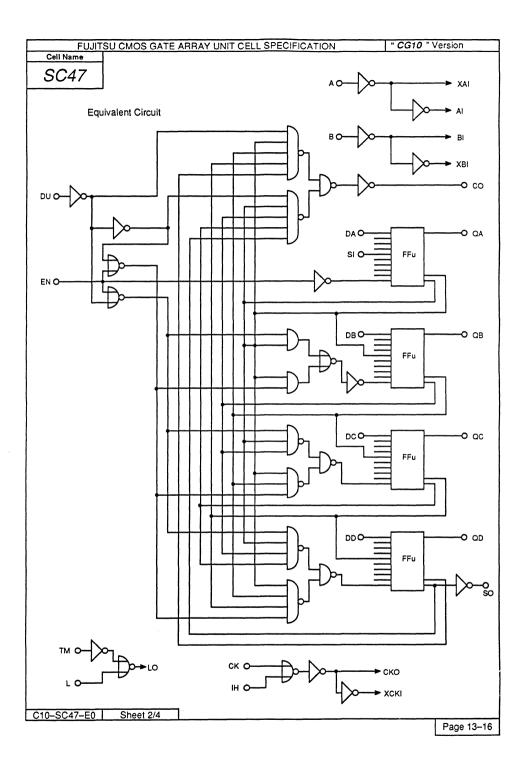
	SU CMOS GATE AR	RAY UNIT	CELL S	PECIFIC	ATION		" CG10	" Version	
Cell Name	Function							Number of BO	
SC47	SCAN 4-bit Sy	nchronou	us Binar	y Up/Do	own Co	unter		78	
Cell	Symbol								
		tı	J <b>p</b>		dn		Path		
		t 0	KCL	t O	KCL	KCL2	CDR2	raui	
DA DB DC DD CK TH CT TM EN DU		2.813 3.825 5.375 1.469	0.067 0.067 0.067 0.067	2.938 5.438 6.781 1.838	0.101 0.045 0.135 0.045	0.140 - 0.179 -	4 - 4 -	CK to Q CK to CO L to Q DU to CO	
SI ————————————————————————————————————	SI — SO			Parameter Clock Pulse Width Clock Pause Time Data Setup Time					
			old Time			t HD	1.4		
		EN Setu				t se	4.9		
	Input Loading	EN Hold	ut Setup 7	Time			t HE	0.5 5.5	
Pin Name	Factor (lu)		it Hold Ti				t HU	0.4	
D CK, IH, TM, L EN	2 1 3 1	Load Pu Clear R	ulse Widt elease Ti old Time	n		t LW t REM	12.0 2.3 9.5		
DU, A, B SI	1 2	J Clear H	old Tillie			t inn	9.0		
Pin Name	Output Driving Factor (lu)								
а 80 CO	18 18 18	<ul> <li>Minimum values for the typical operating condition.</li> <li>The values for the worst case operating condition are given by the maximum delamultiplier.</li> </ul>							

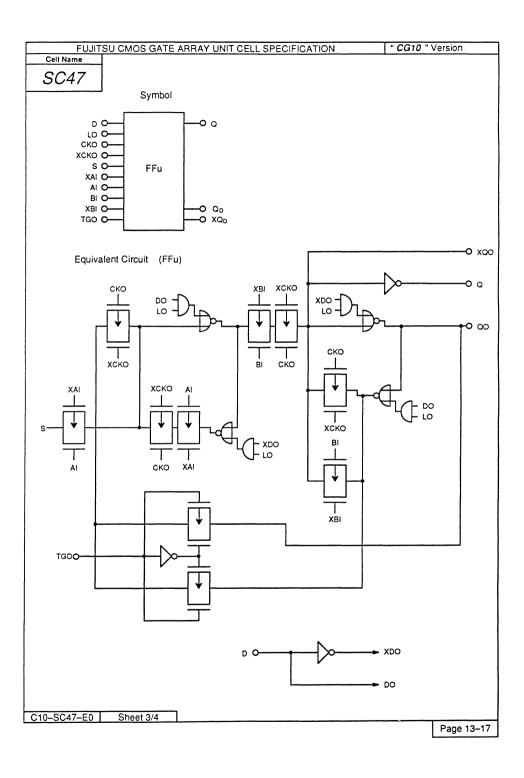
Mode		Outputs							
Mode	CLK	ГO	EN	DU	Dn	Α	В	SI	Qn, SO
	5	L	Н	Х	х	L	L	х	No Count
CLOCK	5	L	L	н	Х	L	L	Х	Count Down
	<b>F</b>	L	L	L	Х	L	L	Х	Count Down
	х	Н	Х	Х	Di	L	L	Х	Di
	Н	L	Х	Х	х	L	L	х	No Count
SCAN	Η	×	×	×	х	Л	Н	Si	Hold
	н	Х	Н	х	Х	L	U	Х	Si

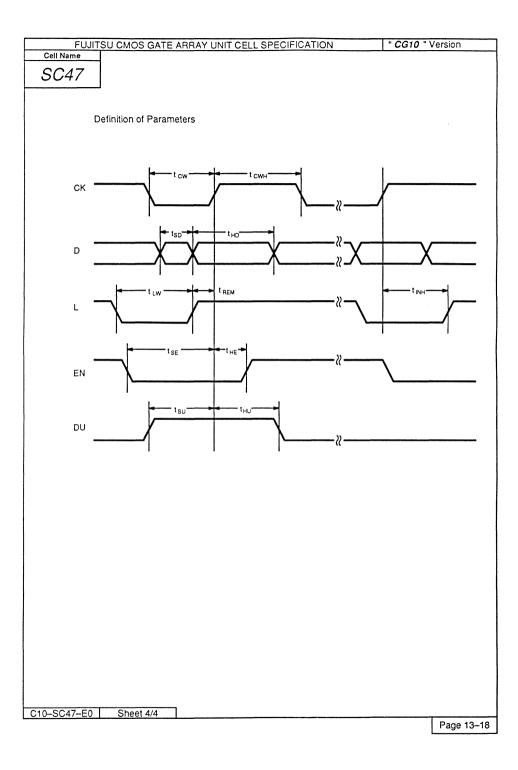
Note : CLK = CK + IH  $LO = TM \bullet L$  $n = A \sim D$ 

C10-SC47-E0 Sheet 1/4

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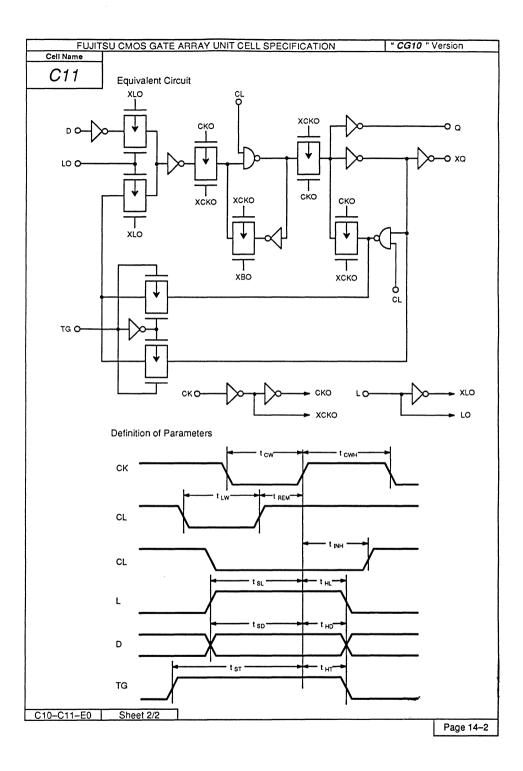
# **Non-scan Counter Family**

Page	Unit Cell Name	Function	Basic Cells
3–231	C11	Non-scan Flip-flop for Counter	11
3-233	C41	Non-scan 4-bit Binary Asynchronous Counter	24
3-236	C42	Non-scan 4-bit Binary Synchronous Counter	32
3-239	C43	Non-scan 4-bit Binary Synchronous Up Counter	48
3-243	C45	Non-scan 4-bit Binary Synchronous Up Counter	48
3-247	C47	Non-scan 4-bit Binary Synchronous Up/Down Counter	68

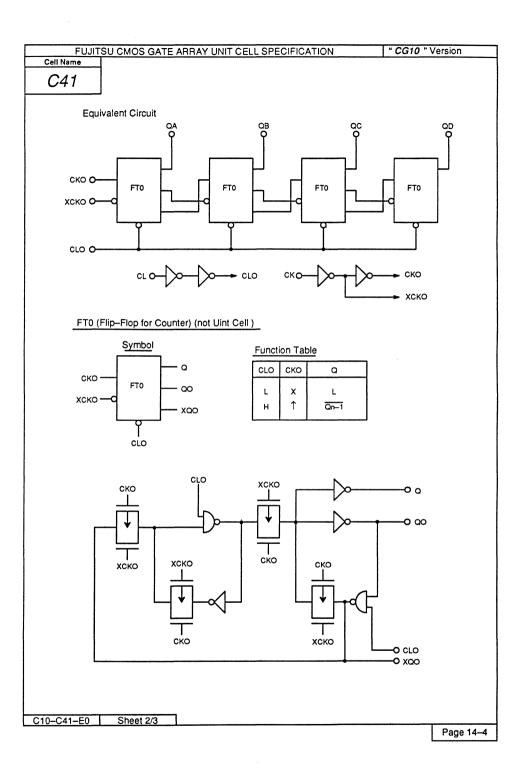
3

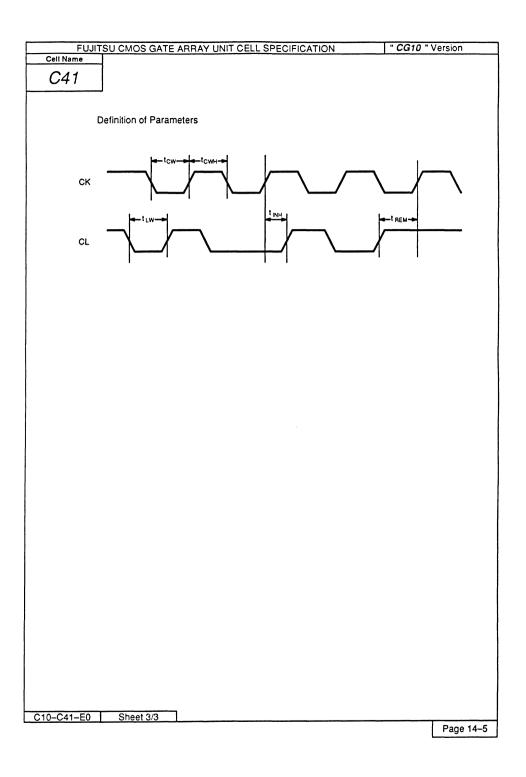
	FII	IITSI	LCMOS	GAT	E ARE	RAV I IN	IT CELL 9	SPECIFIC	ATION		" CG10	" V	ersion
Cell	Name		Func			IAT OIL	II OLLE	DI LON 10	ATION		1 00.0		Number of BC
C	11		Non-S	SCAN	l Flip	-Flop	for Cour	iter					11
		Cell S	ymbol					Pro	pagation D	elay Para	meter		I
						t O	tup KCL	10	KCL	dn KCL2	CDR2	-	Path
						1.188		1.094	0.056	KCL2	CDHZ	-	CK to Q
						1.581	0.067	1.856	0.056	1		ı	CK to XQ
	D	-				1.638	0.067	1.081	0.056		Ì	(	CL to Q,XQ
	L —	┨	-	<del>-</del> a						l			
		-								<b>]</b>			
(	ск —	$\dashv$											
_			L	VO									
	TG —		<u></u>	— xa									
		Ц,	<del>,</del> —					1		ĺ			
						Parame	105	<u> </u>	<u> </u>	L	Symbol	-	Typ (ns) *
		(	ĊL.				Pulse Wid	dth			t cw	$\vdash$	2.5
							Pause Tir				t cwn		2.7
						Cloar	Pulse Wid	ith			tıw	<u> </u>	2.5
							Release 7				t REM	<del>                                     </del>	0.7
						Clear	Hold Time				t inju		0.4
Pin I	Pin Name Input Loading Factor (lu)			'	Load	Setup Tim	Δ /	(CK)		t sı.	-	1.5	
				Load Hold Time (CK)					t HL		0.4		
	L G			2 2 1		D-t- C	\ Ti		(0)(1)				1.6
C	CK	- 1		2			Setup Tim Hold Time		(CK) (CK)		t <sub>SD</sub>	-	0.4
Pin t	Vame		Outpu	t Drivin tor (lu)	g		tup Time Id Time		(CK) (CK)		t st t HT		1.9 0.0
		$\top$				10110	no rime		OIN	L	· HI	L	0.0
X	a :a			18 18				or the typica					
						multip		worst case	operating o	ondition ar	e given by th	ne ma	ximum delay
	Functi	on T	able										
	L	D	TG	CL	СК		(Q <sub>0</sub> )						
	<u> </u>		+	CL	- CK	<del>   "</del>	(40)						
	х	х	X	L	×		-						
	н	н	×	Н	1	+	4						
	Н	L	X	Н	1	$\parallel \parallel \parallel$	1						
	L	×		Н.	<b> </b>	11	Q <sub>0</sub> )						
		l	i -	i	1	$11 - \cdot$							
	L	X	Н	Н	'	<sup>u</sup> (	Q <sub>0</sub> )						
1													
C10-C	11-E0		Sheet	1/2	٦								

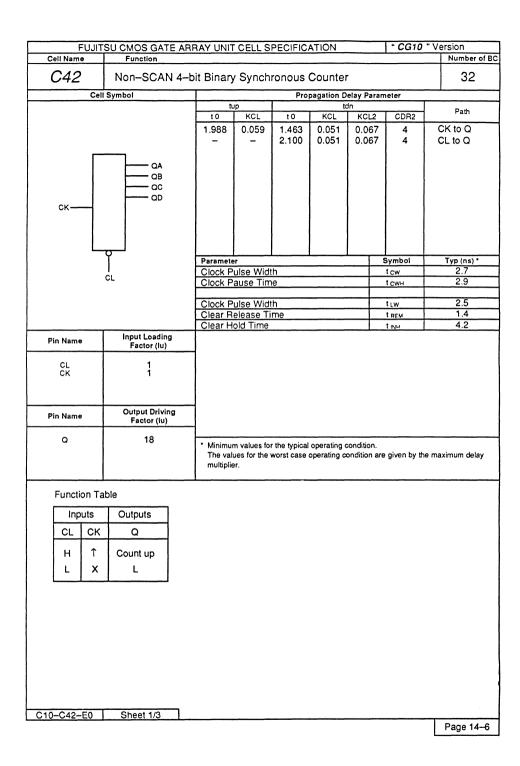
Page 14-1

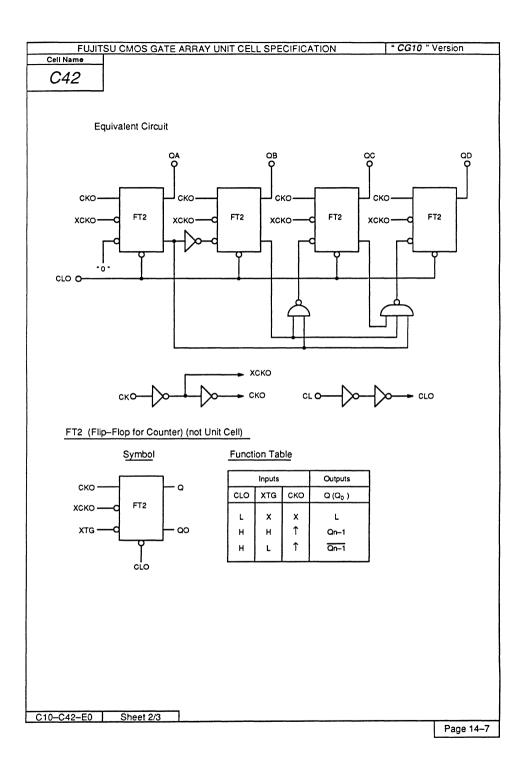


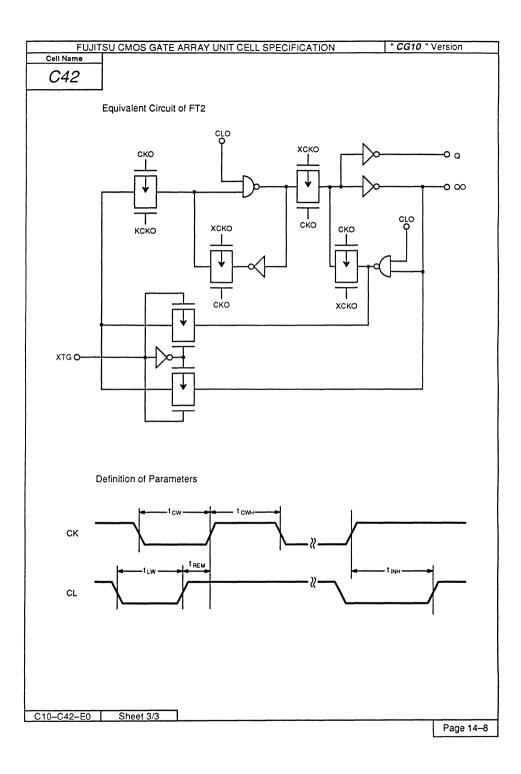
		ELLIIT	SU CMOS GATE	ADD	TUALLVAC	CELLS	DECIEIC	ATION		" CG10	" \/	ersion
Cel	ii Nam	e	Function	Anr	TAT UNIT	OELL 3	r Lon Io	ATION		0070		Number of BC
C	241	ļ	Non-SCAN	4-b	it Binary	Async	hronous	Counte	er			24
		Cell	Symbol				Pro	pagation D		eter		· · · · · · · · · · · · · · · · · · ·
					t 0	KCL	t'O	KCL	NCL2	CDR2		Path
	ск—		QA QB QC QD		1.250 2.294 3.206 4.125	0.059 0.059 0.059 0.059 -	1.163 2.050 2.969 3.875 2.619	0.056 0.056 0.056 0.056 0.056	- - - -	1 1 1 1		CK to QA CK to QB CK to QC CK to QD CL to Q
		L			Paramete	r			1 :	Symbol		Typ (ns) *
			 CL		Clock P	ulse Widt	h			tcw		2.7
		•	JL		Clock P	ause Tim	e			t cwн		2.9
					Clear Pi	ulse Widt	h			tıw		2.5
					Clear R	<u>elease Ti</u> old Time	me			t REM t INH		1.4 4.2
Din	Name	T	Input Loading		Clear	old fille				LINH		4.2
		-	Factor (lu)									
	CK		1									
Pin	Name		Output Driving Factor (lu)	3								
	Q		18			ues for the v	the typical worst case			given by th	e ma	aximum delay
F	uncti	on Tat	ole		L							
Г	Inp	uts	Output									
F	CL	СК	Q									
		<u> </u>										
	Н .	l	Count up									
L	L	X	L									
ı												
C10-	C41_	F0	Sheet 1/3	٦								
<u> </u>	<del></del>	<u>-</u>	JJ. 110								T	Page 14-3











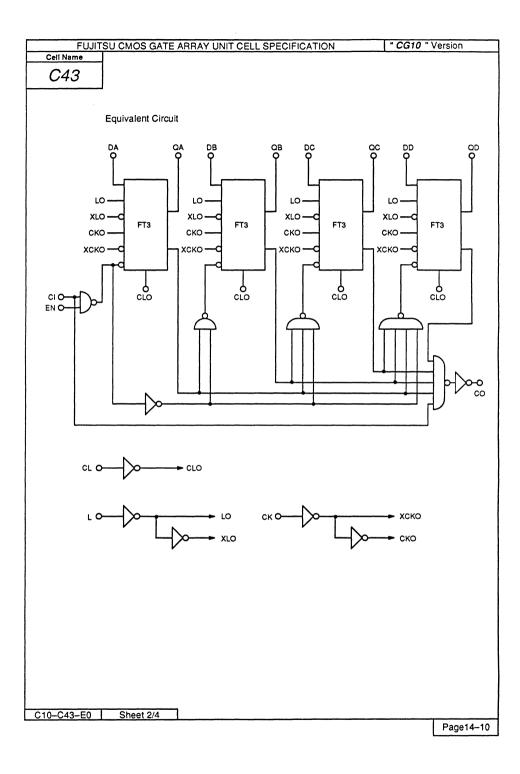
FUJIT	SU CMOS GATE ARI	RAY UNIT	CELL S	PECIFIC	ATION		" CG10	" Version	on
Cell Name	Function							Nu	umber of BC
C43	Non-SCAN 4-t	oit Binar	y Synch	ronous	Up Cou	nter			48
Cel	Symbol			Pro	pagation D	elay Paran	neter		
		tı	qι		to	dn			Path
		t O	KCL	t O	KCL	KCL2	CDR2		
DA — DB — DC — DD — CK — CI — CI	OA OB OC OD	1.850 3.500 1.000 - -	0.067 0.067 0.067 - -	1.500 2.225 0.506 2.425 1.650	0.051 0.045 0.045 0.051 0.045			CI to CL t	o CO o CO o Q o CO
	1	Parameter					Symbol		(ns) *
	CL		ulse Widt				t cw		3.0
			ause Tim				t cwn		4.2 1.7
			etup Time				t <sub>SD</sub>		1.9
			etup Time	······			tsL		2.8
			old Time				t HL		0.9
	Input Loading	CI Setu					tsc		2.7
Pin Name	Factor (lu)	CI Hold					t HC		0.6
			Jp Time				t se		2.7
D L.EN	1	EN Hold	d Time				t HE		0.6
CK,CL		Clear P	ulse Widt	h			tLW		3.5
CI	1 2		elease Ti	me			1 REM		1.2
		Clear H	old Time				t inh		5.2
Pin Name	Output Driving Factor (Iu)								
co					operating o		given by th	e maximu	ım delay

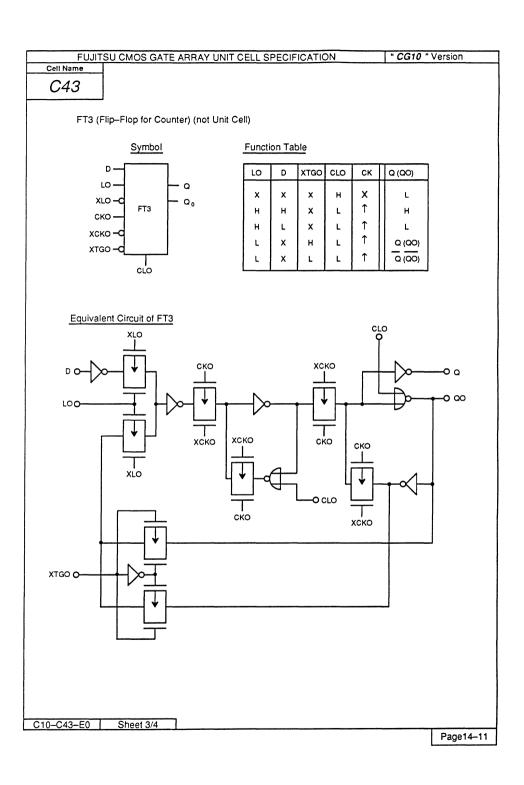
		Inj	outs			Outputs
CL	L	D	EN	CI	СК	Q
L	х	х	х	х	х	L
Н	L	н	х	х	1	н
н	L	L	х	Х	1	L
Н	н	Х	Х	L	Х	No Counting
н	Н	х	L	Х	х	No Counting
н	н	Х	н	Н	1	Count up

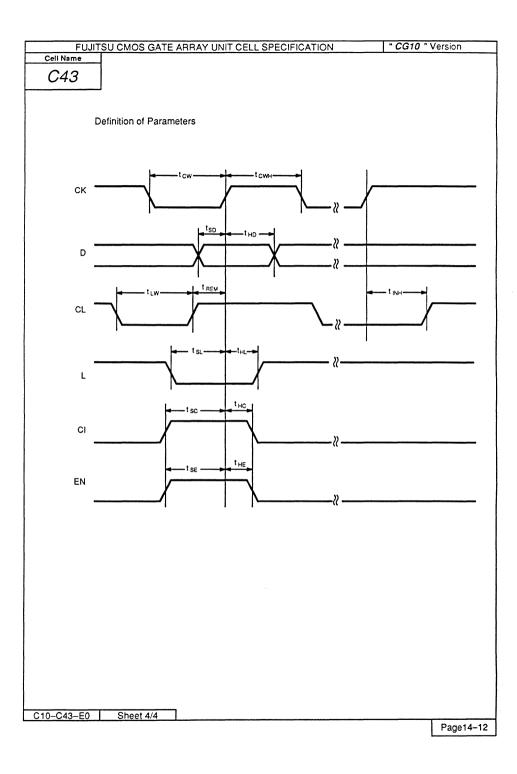
Note: The CO output produces a high level output data when the counter overflows.

C10-C43-E0 | Sheet 1/4

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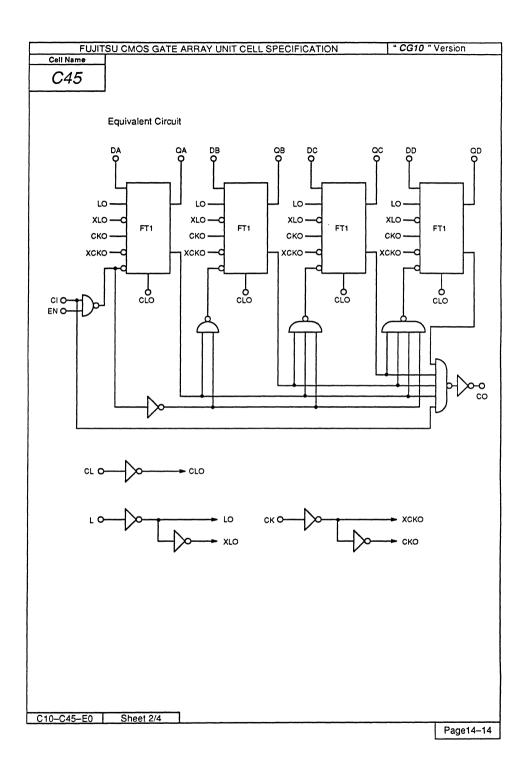
	SU CMOS GATE AR	RAY UNIT	CELL S	PECIFIC/	ATION		" CG10	" Version	
Cell Name	Function							Number of B	
C45	Non-SCAN 4-	oit Binary	Synch:	ronous	Up Cou	nter		48	
Cel	l Symbol	T		Pro	pagation D	elay Paran	arameter		
	· · · · · · · · · · · · · · · · · · ·	tı	JP qu			dn		D-#	
		t O	KCL	t Ö	KCL	KCL2	CDR2	Path	
DA DB DC DD L CK EN CI	ОА — ОВ — ОС — ОD	1.669 3.169 1.194	0.059 0.072 0.072	1.169 1.763 0.850	0.051 0.051 0.051	0.073	4	CK to Q CK to CO CI to CO	
		Parameter					Symbol t <sub>CW</sub>	Typ (ns) *	
	CL		Clock Pulse Width					2.5 2.9	
			Clock Pause Time Data Setup Time					2.4	
			old Time				t <sub>SD</sub>	1.4	
			etup Time	······································			t st	3.2	
			old Time				t HL	1.4	
Di- M	Input Loading	CI Setu					tsc	4.2	
Pin Name	Factor (lu)	CI Hold	Time				t HC	1.2	
	4		up Time				t se	4.2	
D L.EN	1	EN Hold					t HE	1.2	
CK,CL	1 1		etup Time	<del>}</del>			tsa	2.4	
CI	Ź	Clear H	old Time				t HR	1.3	
Pin Name	Output Driving Factor (lu)	1							
Q CO					operating o		given by th	e maximum delay	

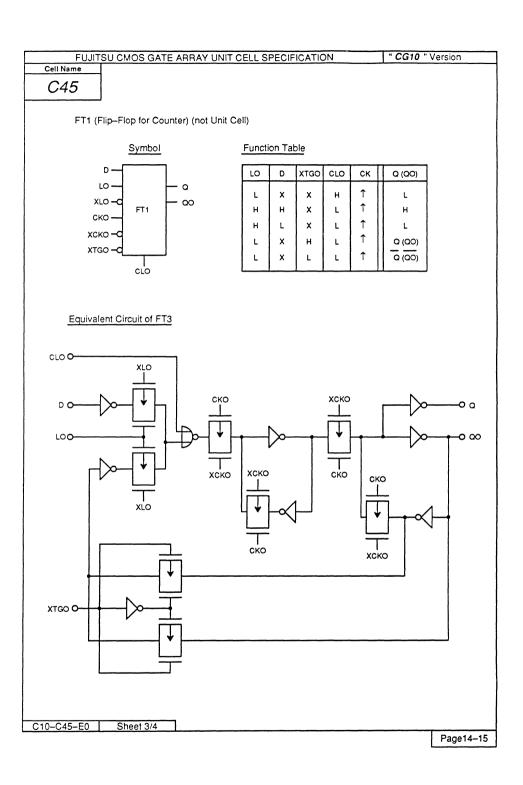
		In	outs			Outputs
CL	L	D	EN	CI	СК	Q
L	х	х	х	х	1	L
Н	L	Н	х	х	1	н
Н	L	L	Х	х	1	L
Н	н	х	х	L	х	No Counting
Н	Н	х	L	х	х	No Counting
н	Н	Х	Н	Н	1	Count up

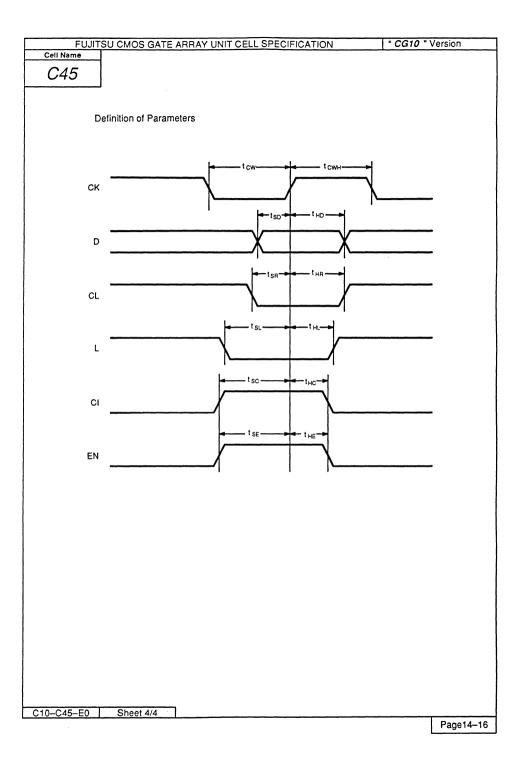
Note: The CO output produces a high level output data when the counter overflows.

C10-C45	5-E0	Sheet 1/4

Page14-13







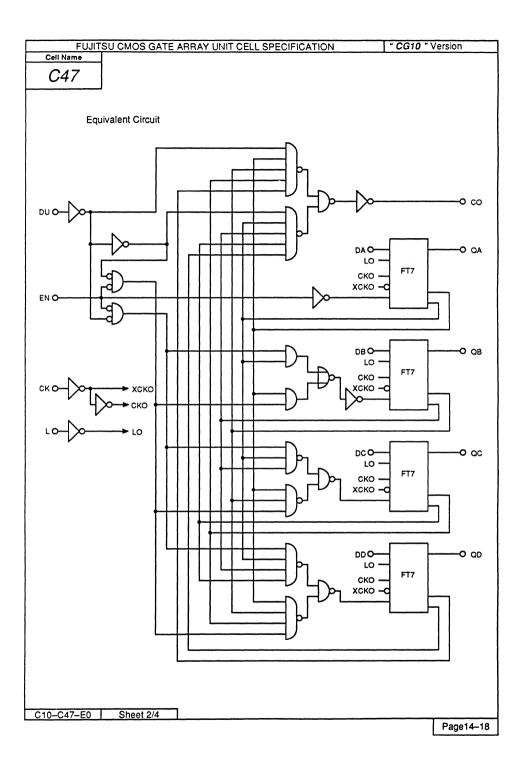
	SU CMOS GATE AF	RAY UNIT	CELL S	PECIFICA	ATION		" CG10	" Version
Cell Name	Function							Number of B
C47	Non-SCAN 4-	bit Binary	/ Synch	ronous	Up/Dow	n Cou	nter	68
Cel	Symbol			Pro	pagation D	elay Paran	neter	
		tı	קנ		to	dn		Path
		t O	KCL	t 0	KCL	KCL2	CDR2	Faui
		2.494	0.067	2.244	0.090	0.140	4	CK to Q
		3.381	0.046	3.825	0.045	-	ļ	CK to CO
Г		3.131	0.067	3.463	0.090	0.140	4	L to Q
DA —	QA	1.544	0.046	1.881	0.045	-		DU to CO
DC DD CK EN CD DU	OB ab	Paramete	er				Symbol	Typ (ns) •
			ulse Widt				tcw	3.5
		Clock P	Clock Pause Time				t cwH	5.6
							t <sub>SD</sub>	
			Data Setup Time Data Hold Time					0.5 1.2
		Dala Ho	na rime				t <sub>HD</sub>	1.2
	Input Loading	DU Setu	ın Time			-+	t su	3.4
Pin Name	Factor (lu)	DU Hold					t HU	0.5
D	4							
Ĺ	1 2 1	EN Setu	p Time				t se	3.2
DU		EN Hold	d Time				t HE	0.8
CK EN	1 3							
			elease Tir	ne			t REM	1.5
Pin Name	Output Driving Factor (lu)	Load Ho	old Time				t INH	7.0
		Load Pu	Ise Width	1		_	tıw	2.9
a co				the typical	operating o			e maximum delay

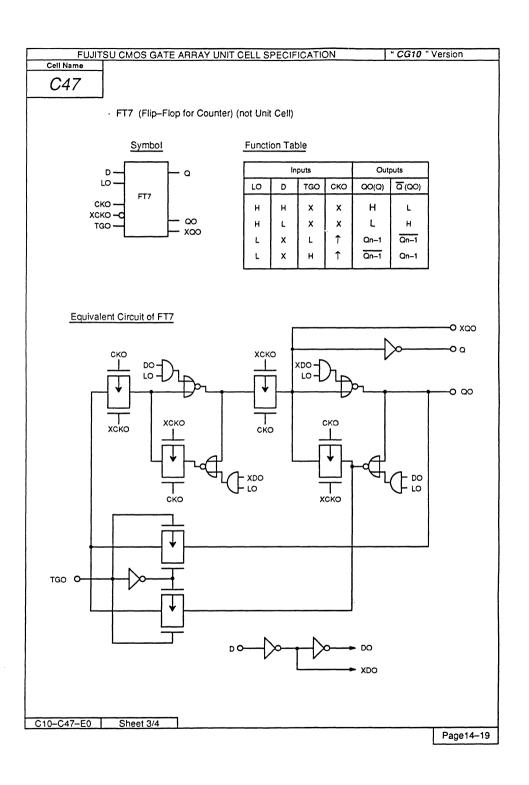
		Inputs			Outputs
Q	L	EN	DU	СК	Q
Н	L	х	х	х	Н
L	L	Х	х	х	L
X	н	Н	Х	1	No Counting
х	н	L	L	1	Count Up
x	н	L	Н	1	Count Down

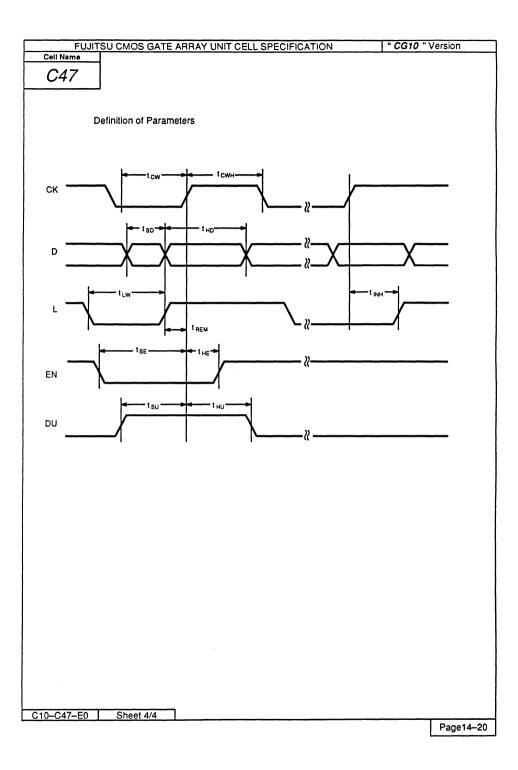
Note: The CO output produces a low level output pulse when the counter overflows or underflows.

C10-C47-E0 Sheet 1/4

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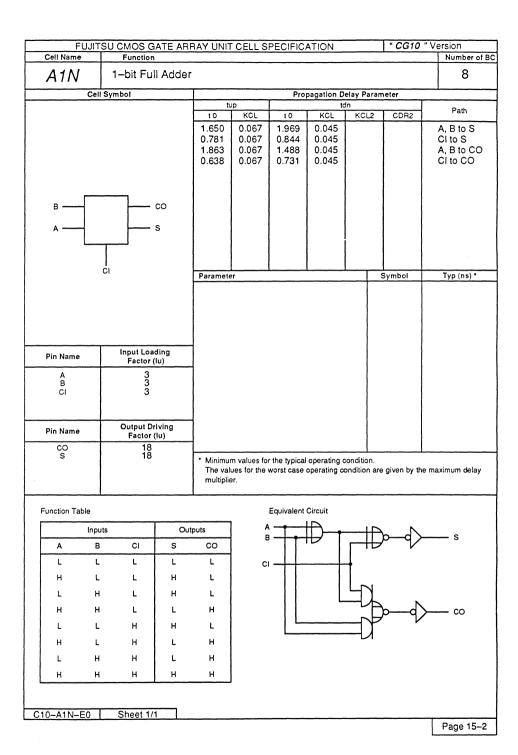


# 3

# **Adder Family**

D	Unit Cell	Function	Basic
Page	Name	Function	Cells
3-253	A1A	1-bit Half Adder	5
3-254	A1N	1-bit Full Adder	8
3-255	A2N	2-bit Full Adder	16
3-257	A4H	4-bit Binary Full Adder with Fast Carry	48

FUJIT	SU CMOS GATE AR	RAY UNIT	CELL S	PECIFICA	ATION		" CG10	" Version
Cell Name	Function							Number of BC
A1A	1-bit Half Adde	r						5
Cel	l Symbol			Pro	pagation D		eter	
		10	KCL	t O	KCL	in KCL2	CDR2	Path
_		0.763 0.681 0.700 0.794	0.034 0.034 0.034 0.034	0.900 0.913 0.781 0.719	0.023 0.023 0.023 0.023			A to S B to S A to CO B to CO
В —	co							
A —	s							
L								
		Paramete	er		l		Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)							
A B	2 2							
Pin Name	Output Driving Factor (lu)							
co s	36 36		ues for the		operating o		given by the	e maximum delay
Function Table				Equivalent	Circuit			
A B	co s	]				<b>₽</b>	N	
L L	į.		-				$\sim$	5 s
L H	I L H							
H L	. L н				14	<u> </u>	<u> </u>	co
н н	HL	J			$-\nu$			
C10-A1A-E0	Sheet 1/1							
								Page 15-1

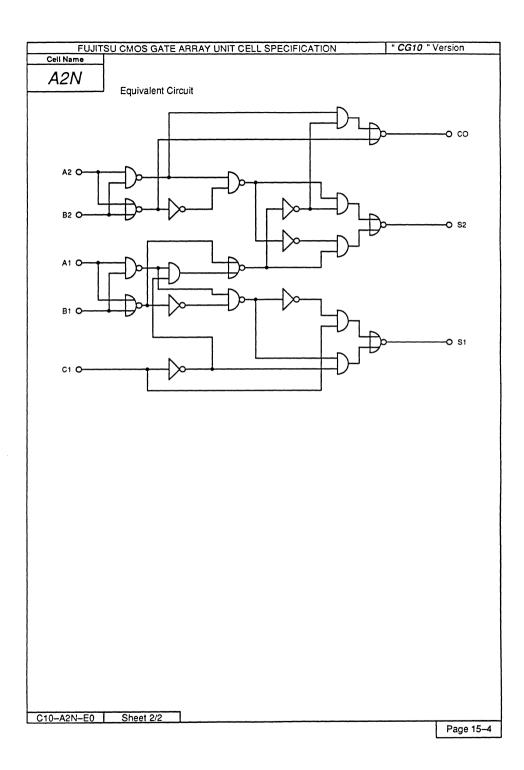


FUJI	<u> ISU CMOS GATE AR</u>	RAY UNIT	CELLS	PECIFICA	ATION		" CG10	" Version
Cell Name	Function							Number of B
A2N	2-bit Full Adde	r						16
Ce	li Symbol			Proj	pagation D	elay Paran	eter	
		tı	)p			in		Path
		t O	KCL	t'O	KCL	KCL2	CDR2	raui
		1.781	0.122	1.756	0.079	-		A1 to CO
		1.713	0.122	1.794	0.079	-	1	B1 to CO
		0.988	0.122	0.850	0.051	0.067	4	A2 to CO
		0.919	0.122	0.850	0.051	0.067	4	B2 to CO
		1.744	0.122	1.613	0.079	-		CI to CO
B2	co	1.856	0.093	1.719	0.079	-		A1 to S1
A2		1.856	0.093	1.719	0.079	-	1	B1 to S1
B1 ——	S2	0.738	0.093	0.744	0.079	-	]	CI to S1
A1	S1	1.763	0.093	1.719	0.079	-	]	A1 to S2
L.,		1.944	0.093	1.844	0.079	-		A2 to S2
		1.694	0.093	1.756	0.079	-		B1 to S2
	I Cl	1.944	0.093	1.844	0.079	-		B2 to S2
	CI	1.725	0.093	1.575	0.079	-		CI to S2
		Paramete	er				Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)	1						
		┪					ļ	
A, B Cl	2 2						ļ	
σ,	-	1				}		
		1						
						ļ		
Pin Name	Output Driving Factor (lu)							
S	14 14							
co	14		ues for the		operating o		given by the	maximum delay

		la a	uts				Out	puts		
		inp	uts			CI = L			CI = H	
	A1	B1	A2	B2	S1	S2	co	S1	S2	CO
	Ĺ	L	L	L	L	L	L	Н	L	L
	Н	L	L	L	н	L	L	L	н	L
	L	Н	L	L	Н	L	L	L	н	L
1	Н	Н	L	L	L	Н	L	Н	Н	L
1	L	L	н	L	L	Н	L	н	н	L
i	Н	L	Н	L	Н	Н	L	L	L	н
1	L	н	Н	L	Н	Н	L	L	L	н
1	Н	н	Н	L.	L	L	н	н	L	н
1	L	L	L	н	L	н	L	Н	Н	L
	Н	L	L	н	н	Н	L	L	L	н
	L	н	L	н	н	Н	L	L	L	н
ĺ	н	н	L	н	L	L	н	н	L	н
1	L	L	н	н	L	L	н	н	L	н
1	Н	L	н	н	н	L	н	L	Н	н
1	L	н	Н	н	н	L	н	L	н	н
	Н	Н	Н	Н	L	н	Н	Н	н	Н

C10-A2N-E0 | Sheet 1/2

Page 15-3



	<u>TSU CMOS GATE AR</u>	RAY UNIT	CELLS	PECIFIC.	ATION		" CG10	" Version
Cell Name	Function							Number of B
A4H	4-bit Binary Fu	ll Adder	with Fas	st Carry				48
Ce	II Symbol			Pro	pagation D	elay Paran	neter	
			αp			dn		Path
		10		10	KCL	KCL2	CDR2	raui
		0.738	0.093	1.019	0.079	-		CI to S1
		1.656	0.122	1.919	0.079	-		CI to S2
		1.894	0.122	1.863	0.079	-	i	CI to S3
В4 ——	co	1.963	0.122	2.213	0.079	-	l	CI to S4
A4	S4	1.794	0.067	2.006	0.045	-	ŀ	CI to CO
В3 —		2.381	0.093	2.119	0.079			A1, B1 to S1
A3	S3	1.981	0.093	1.925	0.079	_		A1, B1 to S2
B2		2.138	0.122	2.406	0.079	_		A1, B1 to S3
A2	S2	2.344	0.122	2.450	0.079	_	1	A1, B1 to S4
B1		2.063	0.067	2.363	0.045	_	ĺ	A1, B1 to CO
A1	S1	1 2.000	0.007	2.000	0.0,0			711,511000
		1.931	0.122	2.106	0.079	_		A2, B2 to S2
		2.288	0.122	2.250	0.079	_		A2, B2 to S3
	CI	2.338	0.122	2.531	0.079	-		A2, B2 to S4
		2.419	0.067	2.394	0.045	-		A2, B2 to CO
	Input Loading	1.756	0.122	1.781	0.079			A3, B3 to S3
Pin Name	Factor (lu)	2.400	0.122	2.525	0.079			A3, B3 to S4
^		2.375	0.122	2.388	0.075	_	[	A3, B3 to CO
A B	2 2 2	2.373	0.007	2.500	0.043	_		A3, B3 10 CC
CI	2	1.813	0.093	1.881	0.051	0.067	4	A4, B4 to S4
		2.288	0.067	2.194	0.045	_		A4, B4 to CO
			L	L	لــــــــــــــــــا	L	L	<u> </u>
Pin Name	Output Driving Factor (lu)							
СО	18	1						
S1, S3, S4	14							
S2	18							
	1	1						

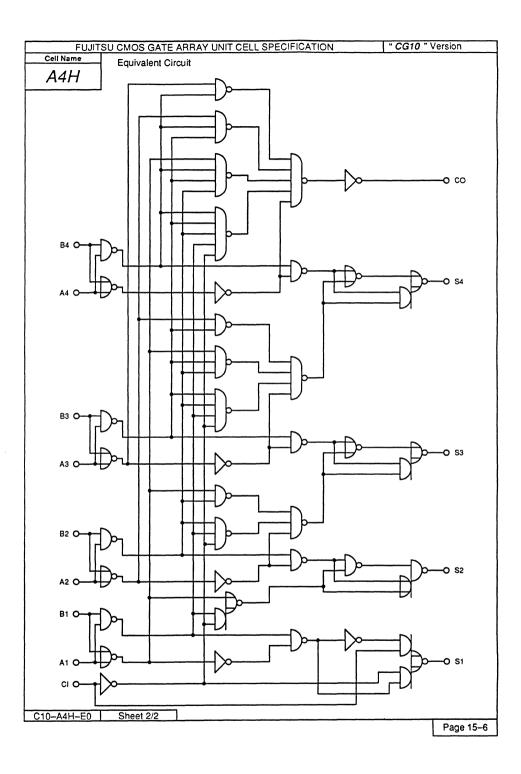
Function	Table
----------	-------

							Out	puts		
	1	inp	uts			CI = L			CI = H	
						C2 = L			C2 = H	
	A1	B1	A2	B2	S1	S2	C2	S1	52	C2
	A3	В3	A4	B4	S3	S4	co	S3	S4	co
	L	L	L	L	L	L	L	Н	L	L
	Н	L	L	L	н	L	L	L	н	L
	L	н	L	L	н	L	L	L	н	L
	н	Н	L	L	L	Н	L	н	н	L
	L	L	н	L	L	н	L	н	н	L
	Н	L	Н	L	н	Н	L	L	L	н
	L	Н	н	L	н	Н	L	L	L	Н
	Н	Н	Н	L	L	L	н	н	L	н
	L	L	L	н	L	н	L	н	н	L
	н	L	L	н	н	н	L	L	L	н
	L	н	L	н	н	н	L	L	L	н
	н	н	L	н	L	L	н	н	L	н
	L	L	н	н	L	L	н	н	L	н
	н	L	н	н	н	L	н	L	н	н
	L	н	Н	н	н	L	н	L	н	н
	н	Н	Н	н	L	Н	н	Н	н	Н
c	10-A4H	-E0	St	eet 1/2						

### Note:

Input conditions at A1, A2, B1, B2 and CI are used to determine outputs S1 and S2 and the value of the internal carry C2.
The values at C2, A3, B3, A4 and B4 are then used to determine outputs S3, S4 and CO.

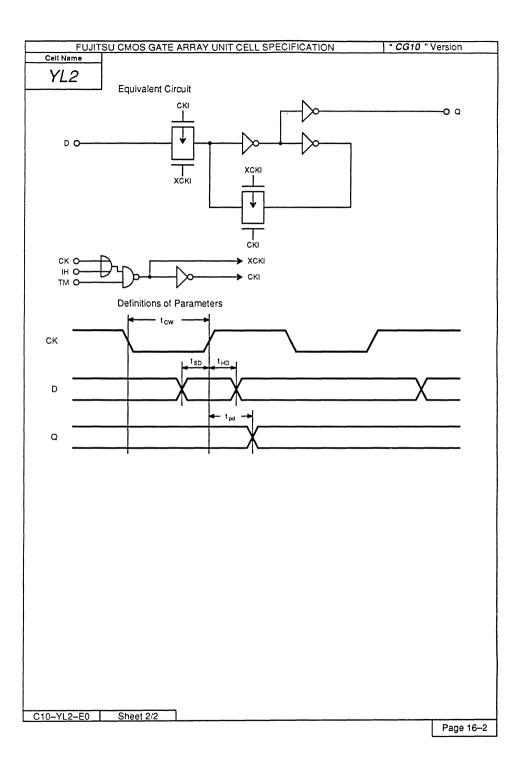
Page 15-5



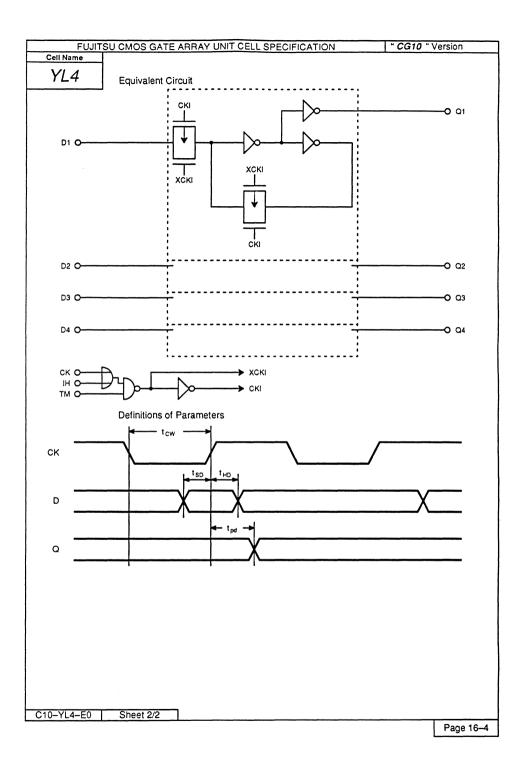
## **Data Latch Family**

	Unit Cell		Basic
Page	Name	Function	Cells
3–261	YL2	1-bit Data Latch with TM	5
3-263	YL4	4-bit Data Latch with TM	14
3-265	LTK	Data Latch	4
3–267	LTL	1-bit Data Latch with Clear	5
3-269	LTM	4-bit Data Latch with Clear	16
3–272	LT1	S-R Latch with Clear	4
3-274	LT4	4-bit Data Latch	14

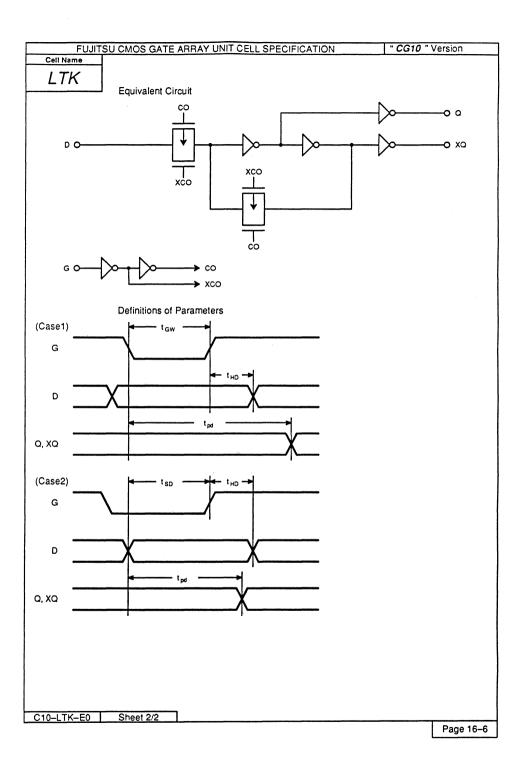
	Fl Name	JJITS			E ARR	AY UNI	CELL S	PECIFICA	ATION		" CG10	" V	ersion Number of B	
	12			unction oit Data	Latch	with T	——— М						5	
		Cell	Symbo	)1	—— <u> </u>			Pro	pagation D	elav Para	meter			
			,				up		to	In			Path	
D · CK · IH · TM ·	<u> </u>			)— a		1.706 0.725	0.034 0.034	1.756 0.800	0.023 0.023	KCL2	CDR2		CK, IH to Q	
					1		<u> </u>				<u> </u>			
					-	Paramete	er				Symbol	-	Typ (ns) *	
						Clock F	ulse widt	h			tcw		4.3	
					ŀ	Data Se	etup Time				tsp	2.0		
						Data H	old Time				t <sub>HD</sub>		1.6	
		Т	In	put Loadin										
Pin N	lame			Factor (lu)										
C II TI	K H			2 1 1 1							!			
Pin N	lame	_	0	utput Drivi Factor (lu)	ng									
C	2			36							e given by th	ne ma	aximum delay	
Note : The			must	be kept LO	W during	the SCAN	Mode.							
	Inp	out		Output	W- 3									
ТМ	ΙH	СК	D	a	Mode									
L	х	х	D	D	SCAN									
Н	Н	х	Х	Q <sub>0</sub>										
н	х	н	х	Q <sub>0</sub>	LATCH	1								
	L	L	D	D										
н						<del>-</del>								
Н С10-Y		. <u>.                                   </u>		neet 1/2	_									



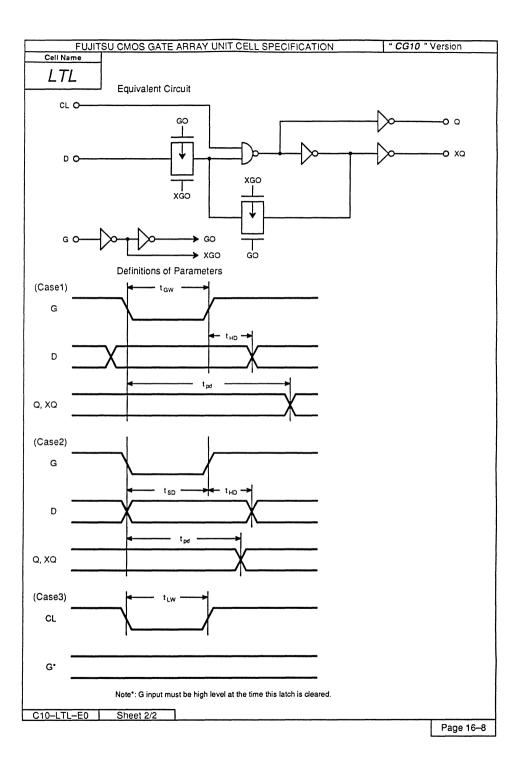
	FI	LUTS	SILCA	AOS GAT	F ARR	AY LINI	T CELL S	PECIFICA	ATION		" CG10	" V	ersion
Cell I	Name			unction		11 0111			*******		1		Number of B
Y	_4		4-1	oit Data	Latch	with T	M						14
		Cell	Symbo	oi				Pro	pagation D	elay Parai	meter	CD	
					1		tup		to		1 0000		Path
					F	2.081	0.034	2.144	0.023	KCL2	CDR2		K, IH to Q
D1 D2 D3 D4 CK IH				01 02 03 03 04		O.688  Paramet	0.034	0.806	0.023		Symbol	2 (	Typ (ns) * 4.5
					ŀ	Data S	etup Time	(D)			t <sub>SD</sub>		1.2
						Data H	old Time	(D)			t HD		2.5
C II	Name O K H M			put Loadin Factor (lu) 2 1 1 1									
Pin N	lame		0	utput Drivi Factor (Iu)	ng								
(	3			36							e given by th	e ma	aximum delay
Note : The			l must	be kept LO	W during	the SCAN	Mode.						
	1	out		Output	I	٦							
		out	-		Mode								
TM	IH	СК	Dn	Qn		4							
L	X	×	D	D	SCAN	_							
н	н	Х	×	Qn <sub>0</sub>		1							
H X H X Qno LATO					LATCH								
н	L	L	О	D									
n = 1 ~	4					_							
C10-Y	L4-E	0	St	neet 1/2	<u> </u>							<u> </u>	Page 16–3



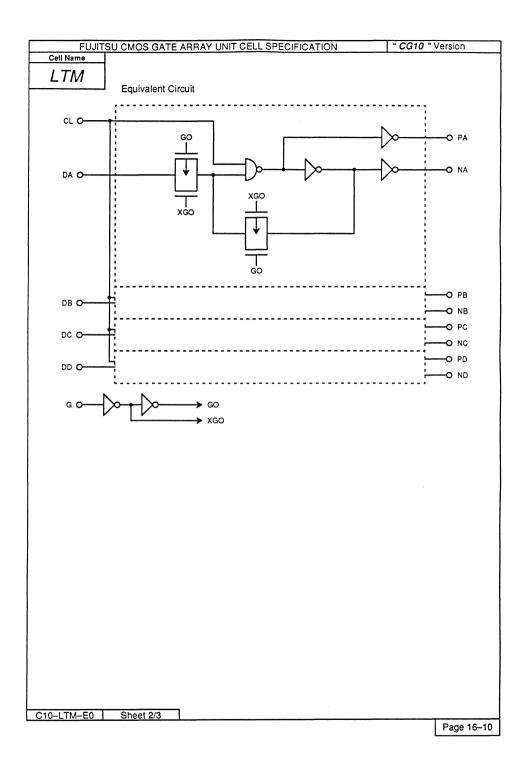
	TSU CMOS GATE AR	RAY UNIT	CELL S	PECIFIC	ATION		" CG10		
Cell Name	Function							Nu	mber of BC
LTK	Data Latch								4
С	ell Symbol			Pro	pagation D	elay Parar dn	neter		
		t O	KCL	10	KCL	KCL2	CDR2		Path
D	o	0.644 0.906 1.094 1.325	0.067 0.067 0.067 0.067	0.719 1.019 1.138 1.463	0.045 0.045 0.045 0.045			D to G t	o Q o XQ o Q o XQ
	<b>р</b> — хо								
						L	<u> </u>	<del></del>	/= -\ C
		G Input	r Pulse Wi	dth			Symbol t Gw		(ns) * 2.5
		Data Se Data Ho	tup Time	t so t HD	1.0 1.5				
		Data 110	na mne				· HO		
Pin Name	Input Loading	+							
	Factor (lu)	4							
D G	2								
Pin Name	Output Driving Factor (lu)								
a xa	18 18		ues for the v		operating o		e given by th	e maximu	m delay
Function Table									
Inputs	Outputs								
D G	Q XQ								
х н	Q <sub>0</sub> XQ <sub>0</sub>								
H L	H L								
LL	L H								
C10-LTK-E0	Sheet 1/2								
OIO LIN-LU	1 011000 1/2							Pag	ge 16–5

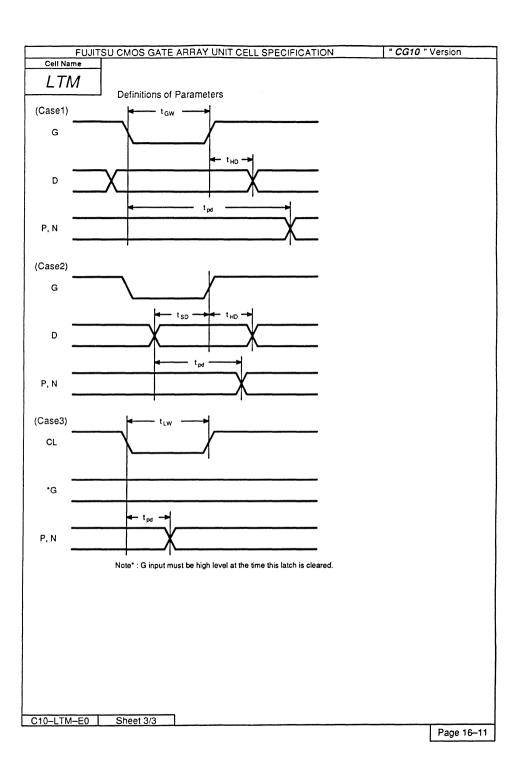


	FUJIT	SU CM	OS GAT	E ARR	AY UNIT	CELLS	PECIFICA	ATION		" CG10	" V	ersion
Cell N	ame		nction									Number of BC
L7	L	1-b	it Data	Latch	with CI	ear						5
	Cel	l Symbol					Pro	pagation D		neter		
					t O	KCL	ť0	KCL	in KCL2	CDR2		Path
					0.869 0.738 0.950 1.225 1.388	0.067 0.067 0.067 0.067 0.067	0.531 0.763 1.069 1.200 1.569	0.051 0.051 0.051 0.051 0.051			0	EL to Q, XQ to Q to XQ i to Q i to XQ
D - G -												
		CL			Paramete		dth			Symbol		Typ (ns) *
				}	G input	Pulse Wi	utn			t GW		2.5
						tup Time				t sp		0.9
						Data Hold Time						0.4
						Clear Pulse Width						2.5
Pin N	Pin Name Input Loading Factor (lu)				Olear	JISC VVIGE				t <sub>LW</sub>		
	D 2											
G Cl			1									
Pin N	ame		tput Drivi actor (lu)									
X	2		18 18		Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						iximum delay	
Functio	n Table											
	Inputs		Out	puts	]							
CL	D	G	a	XQ	1							
L	X	н	L	н	1							
н	x	н	Q <sub>0</sub>	XQ								
Н	н	L	Н Н	L L								
			ŀ		1							
Н	L	L	L	Н	J							
C40 17	L-E0	She	et 1/2									
CIU-LI												Page 16-7

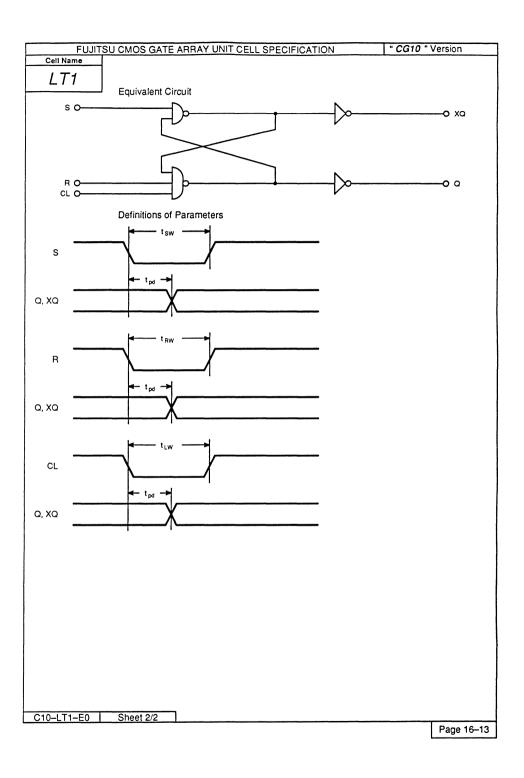


	F	UJIT	SU CM	OS GAT	E ARR	RAY UNIT	CELLS	PECIFICA	ATION		" CG10	" Version
Cell	Nam			nction								Number of B0
L7	TM	1	4-b	it Data	Latch	with CI	ear					16
		Cell	Symbol					Proj	pagation D		neter	
						t O	KCL	t O	KCL	fn KCL2	CDR2	Path
DA DB DC DD			— PA O— NA — PB O— NB			0.963 0.763 1.000 1.631 1.706	0.067 0.067 0.067 0.067 0.067	0.606 0.806 1.119 1.531 1.969	0.045 0.045 0.045 0.045 0.045	NOCE	00112	CL to P, N D to P D to N G to P G to N
	G PC PC PD NC PD ND				Paramete G Input	er Pulse Wi	dth			Symbol t <sub>GW</sub>	Typ (ns) * 2.5	
	CL					Clear P	ulse Widt	h			t <sub>LW</sub>	2.5
						Data Setup Time Data Hold Time					t so	1.0
	Dia Name Input Loading					Data Hold Time					t HD	1.5
	Factor (lu)			<b>.</b>								
	Ğ CL			2 1 4								
Pin I	Name	,		tput Drivir	g							
	P N			18 18							given by th	e maximum delay
Functi	ion Ta	able										
	ı	nputs		Outp	outs	7						
С	L	D	G	Р	N	1						
	-	×	н	L	Н	1						
н	4	×	н	Po	No							
		н	L	Н	L							
"		L	Ĺ	"	н							
<u> </u>						_						
C10-L	TM-	-F0	She	eet 1/3	7							

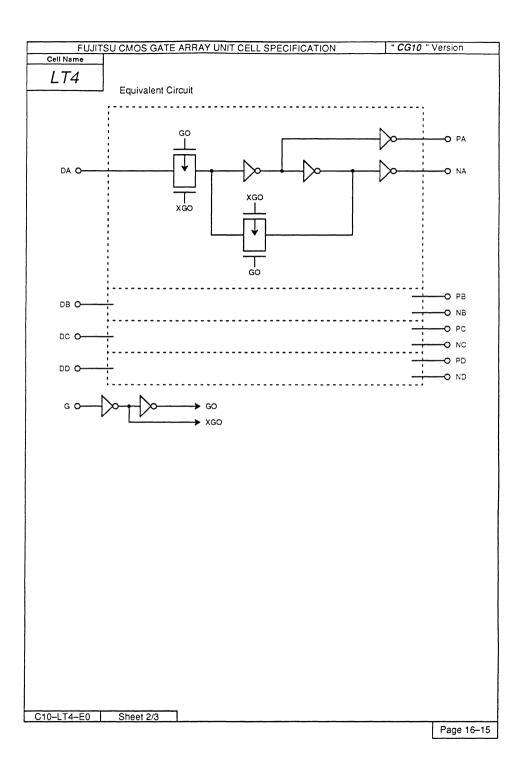


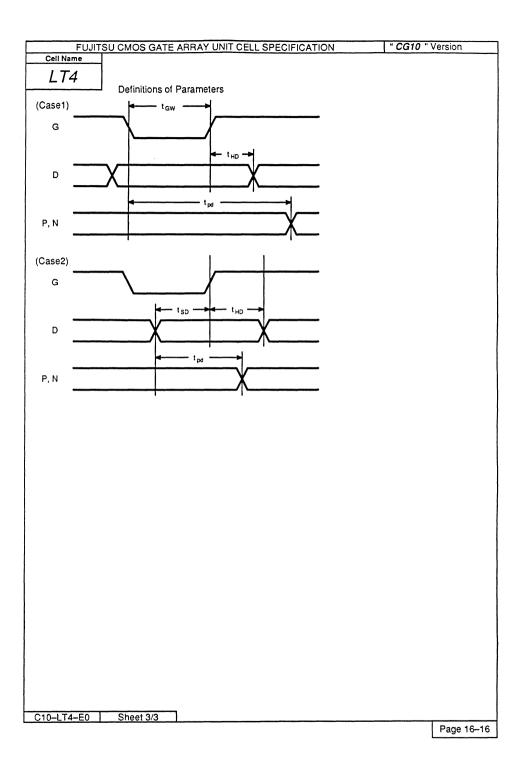


	FILLUT	SILCM	08 647	EARE	AV LINIT	CELL S	DECIEIC	ATION		" CG10	" Ve	rsion
Cell Nam			nction	EARF	AT UNIT	CELLS	PECIFICA	ATION		CG10	Ĭ	Number of BC
LT1	•	S-F	R Latch	with (	CLEAR							4
	Cel	i Symbol					Pro	pagation D		neter		
					t O	KCL	t'O	KCL	ln KCL2	CDR2		Path
					1.100	0.067	0.550	0.045	KOLZ	ODAZ	s	to Q, XQ
					0.975	0.067	0.650	0.045			R	to Q, XQ
ŀ					0.900	0.067	0.575	0.045		1 1	C	L to Q, XQ
										]		
s -			<u> —</u> а									
3-	٩		u									
		L										
R -	_ <sub>4</sub> _	۳	— хо									
		Ĭ										
		CL			Paramete					Symbol		Typ (ns) *
					Set Puls	se Width				tsw		2.5
					Reset P	ulse Wid	th			t RW		2.5
										t <sub>LW</sub>		2.5
					Olear I	dise Widt	<u></u>			LLW		
Pin Nam	Pin Name Input Loading Factor (Iu)			g						1		
s												
S R CL			1									
""			•						1			
									1			
Pin Nam	e	F	tput Drivi actor (lu)	ng					l			
Q XQ			18 18						l	l		
^~			10					operating o		given by the	ma	ximum delav
					multiplie			opolating o	orrondorr are	given by aic	, ,,,,,,	Amilioni delay
		<u> </u>										
Function T	able											
	Inputs		Out	puts	7							
CL	s	R	a	XQ	1							
L	н	Н	L	н	1							
н	н	н	a <sub>o</sub>	XQο								
Н	н	L	L	н								
Н	L	н	Н	L								
Н	L	L	Inhil	oited								
					J							
C10-LT1-	-E0	She	eet 1/2								_	
												Page 16-12



FLUIT	SU CMOS GATE ARF	RAY UNIT	CELLS	PECIFIC	ATION		" CG10 '	" Version
Cell Name	Function			. 2011 10/				Number of BC
LT4	4-bit Data Latch	)						14
Cel	Symbol			Pro	pagation D		neter	
		t O	KCL	t O	KCL	in KCL2	CDR2	Path
		1.563 1.563 0.656 0.875	0.067 0.067 0.067 0.067	1.425 1.906 0.738 1.000	0.045 0.045 0.045 0.045	NOLE	OBNZ	G to P G to N D to P D to N
DA —— DB —— DC —— DD —— G ——C	DB — D— NA — PB — PB — NB — PC						Symbol	Typ (ns) •
		G input	Pulse Wi	dth			t GW	2.5
		Data Se	tup Time				tsp	1.0 1.5
		Dala HC	na rime	t <sub>HD</sub>	1.3			
							}	
Pin Name	Input Loading Factor (Iu)					į		
D G	2 1							
	Output Driving							
Pin Name	Factor (lu)						l	
P N	18 18		ues for the		operating co		given by the	maximum delay
Function Table								
Inputs	Outputs							
D G	P N							
нн	Po No							
LH	Po No							
н	H L							
	LH							
C10-LT4-E0	Sheet 1/3							
								Page 16-14





# **Shift Register Family**

Page	Unit Cell Name	Function	Basic Cells
3–279	FS1	4-bit Serial-in Parallel-out Shift Register	18
3-281	FS2	4-bit Shift Register with Synchronous Load	30
3-283	FS3	4-bit Shift Register with Asynchronous Load	34
3-286	SR1	4-bit Serial-in Parallel-out Shift Register with Scan	36

Cell Name	TSU CMOS GATE AF						<u> </u>	Number of
FS1	4-bit Serial-in	Parallel-	out Shif	t Regist	ter			18
Ce	II Symbol			Pro	pagation D		neter	
			IP KCL			dn		Path
		10		10	KCL	KCL2	CDR2	CK to Q
sp — с ск — с		1.513	0.067	1.963	0.051	0.067	4	CK to Q
		Paramete	r				Symbol	Typ (ns) *
		Clock P	ulse Widt	h			t cw	2.5
		0.0						
		SD Setu					tssp	0.4
		SD Hold	Time				tHSD	0.2
		Clock		C ≤16	hu		t cwt**	3.7
	Input Loading	Pause	16	< C ≤32			t cwL**	5.3
Pin Name	Factor (lu)	Time	32	< C ≦48	lu		t CWL**	6.9
SD CK	1		ues for the	r the typical worst case			given by the	maximum delay
Pin Name	Output Driving Factor (lu)	**The value of towl. depends on the load(c) connected to the output terminals, QA, QB, QC and QD.						
Q	16							

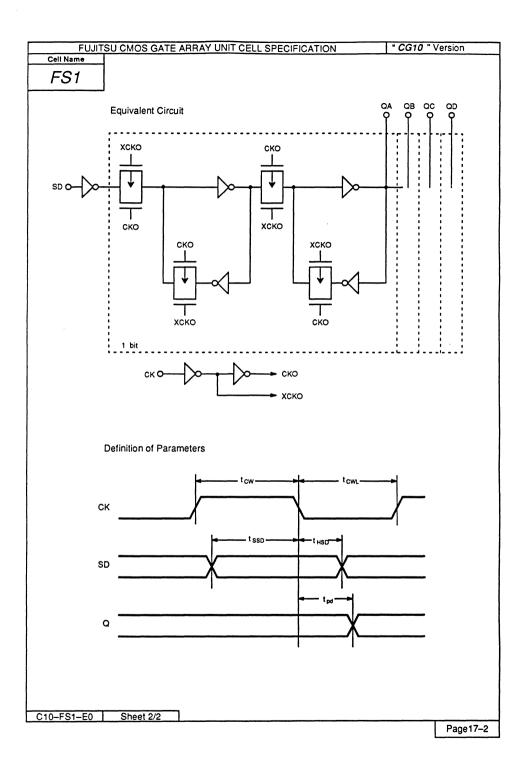
Inp	outs		Outputs							
SD	СК	QA	QB	QC	QD					
SD	<b>↓</b>	SD	QAn	QBn	QCn					

NOTE: • SD = H or L

 QAn, QBn and QCn are levels of QA, QB, and QC respectively, before the falling edge of CK, i.e. 1 bit shift by the falling edge of CK.

C10-FS1-E0 | Sheet 1/2

Page17-1



Cell Name	SU CMOS GATE AF	111711 01111	OLLL O	LOITIO	111011		" CG10 "	Number of
FS2	4-bit Shift Re	egister wi	th Sync	hronous	Load			30
Cell	Symbol	T		Pro	pagation D	elay Parar	neter	
		tu	q		to	dn		Path
		t O	KCL	t O	KCL	KCL2	CDR2	
		1.450	0.067	1.963	0.051	0.067	4	CK to Q
PA PB PC PD SD CK C	QA QB QC QD	Paramete Clock P	er ulse Widt	h			Symbol t <sub>CW</sub>	Typ (ns) * 2.5
		SD Setup Time					tssp	1.8
		SD Hold					t HSD	0.8
		Load Se	tup Time				t <sub>SL</sub>	2.7
		Load Ho					t HL	0.4
		2000 110	710 (11110					
		P Setup	Time				t sp	2.3
Pin Name	Input Loading	P Hold	Гime				t HP	1.0
7 III IVUIIC	Factor (Iu)							
ск	1	Clock		C ≤16			t cwL**	3.7
SD	1	Pause		< C ≦32			t cwL**	5.3
L P	1	Time	] 32	< C ≦48	lu		t cwL**	6.9
Pin Name	Output Driving Factor (lu)	Minimum values for the typical operating condition.     The values for the worst case operating condition are given by the maximum delay multiplier.						
Q	16	"The value of towl depends on the load(c) connected to the output terminals, QA, QB, QC and QD.						

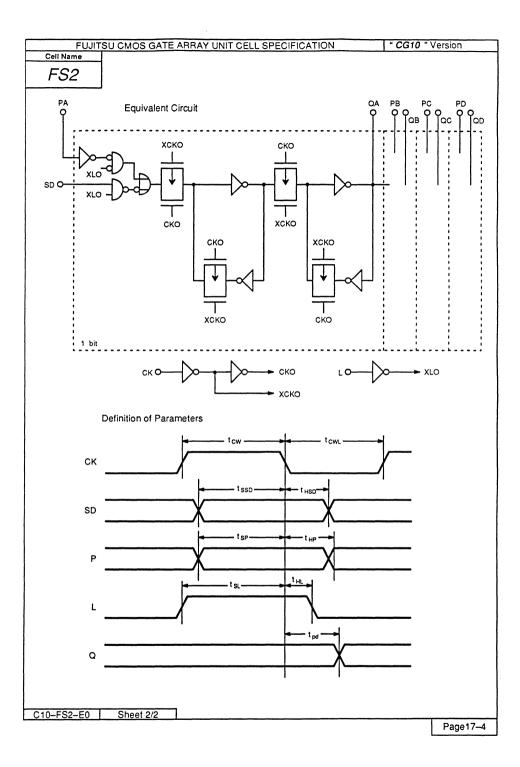
	Inp	outs		Outputs						
SD	L	Р	СК	QA	QB	QC	QD			
SD	L	×	<b>→</b>	SD	QAn	QBn	QCn			
х	Н	Р	<b>\</b>	PA	РВ	PC	PD			

NOTE: • SD = H or L

- QAn, QBn and QCn are levels of QA, QB, and QC respectively, before the falling edge of CK, i.e. 1 bit shift by the falling edge of CK.
- P represents PA, PB, PC and PD.

C10-	-FS2-E0	Sheet	1/2

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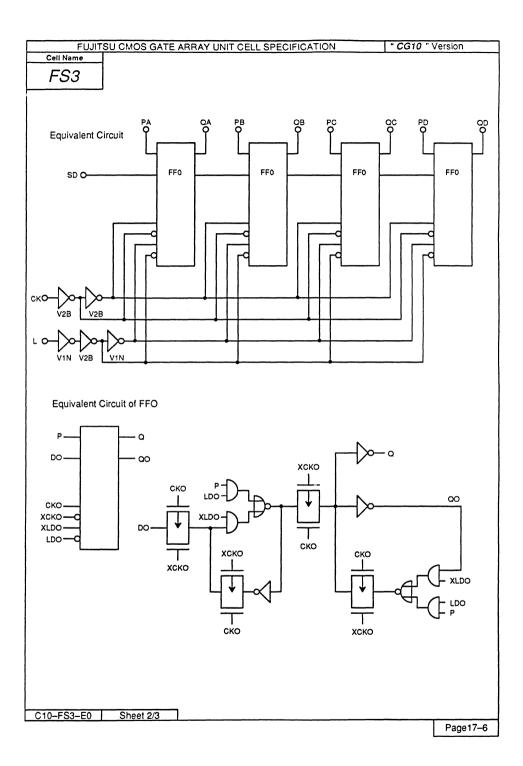


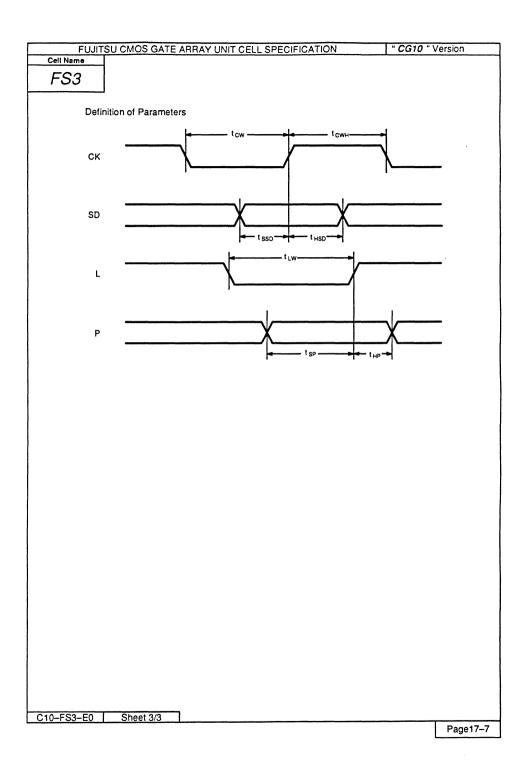
FUJIT	SU CMOS GATE ARI	RAY UNIT	CELL S	PECIFIC	ATION		" CG10	" Version
Cell Name	Function							Number of BO
FS3	4-bit Shift Regis	ster with	Asynch	ronous	Load			34
Cell	Symbol			Pro	pagation D	elay Paran	neter	
		t 0	JP KCL	t O	KCL to	dn KCL2	CDR2	Path
PA————————————————————————————————————	PB — QB — QC PD — QD — QD — QD		0.072 0.072 0.072	1.325 2.188 1.888	0.062 0.062 0.062			CK to Q L to Q P to Q
		Paramete					Symbol	Typ (ns) * 2.5
		Clock Pulse Width Clock Pause Time					t cwH	2.5
		Clock Pause Time					CWH	2.5
		Load Pulse Width					t <sub>LW</sub>	3.9
		SD Setu	ın Time				tssp	0.7
Pin Name	Input Loading Factor (lu)	SD Hold					t HSD	1.1
		P Setup	Time				tsp	0.2
CK SD	2	P Hold					t HP	1.5
Pin Name	2 2 1 2 Output Driving Factor (lu)							
a	18	Minimum values for the typical operating condition.     The values for the worst case operating condition are given by the maximum delay multiplier.						e maximum delay

	In	outs		Outputs
L	Р	SD	СК	Q
L	L	Х	х	L
L	Н	Х	Х	н
н	х	L	1	L
Н	Х	Н	1	Н

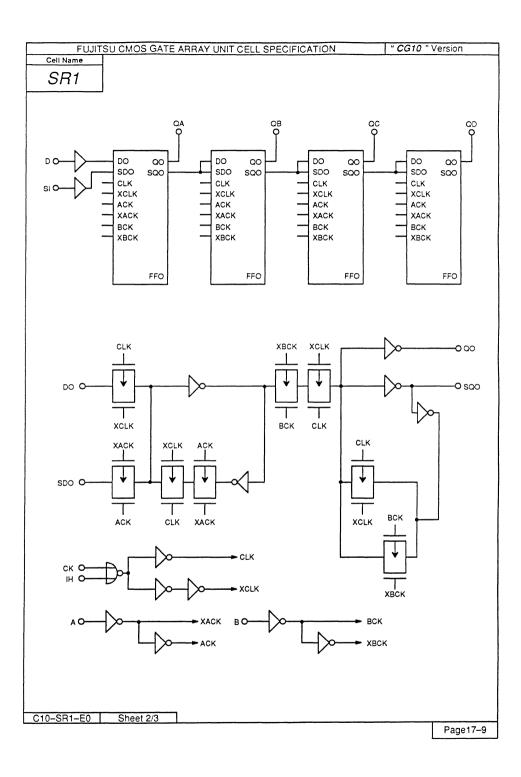
C10-FS3-E0 Sheet 1/3

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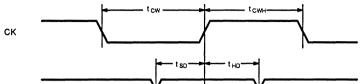
FILLIT	SH CMOS GATE AD	DAV LINIT	CELLS	DECIFIC	ATION	<del></del>	L " CG10	" Version	
Cell Name	SU CMOS GATE AR	HAT UNII	CELL SI	CG10	Number of BC				
SR1	4-bit Serial-in Parallel-out Shift Register with SCAN								
Cell	Symbol	Propagation Delay Parameter							
		t		Path					
		t 0	KCL	t 0	KCL	KCL2	CDR2	CK to Q	
D	—— QA —— QB —— QC —— QD	2.044	0.038	2.106	0.039	0.062	7	CK to Q	
å—q									
		Paramete		<u> </u>			Symbol	Typ (ns) * 3.5	
			ulse Widt ause Tim				t cw	3.5	
		Data Se	tup Time				tsD	2.1	
		Data Ho	old Time				t HD	1.0	
	Input Loading	1							
Pin Name	Factor (lu)								
D C II Ø	1 1 1								
A,B Pin Name	1 Output Driving Factor (Iu)								
_									
Q	36						given by the	e maximum delay	
C10-SR1-E0	Sheet 1/3							Page17–8	



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SR1

Definition of Parameters



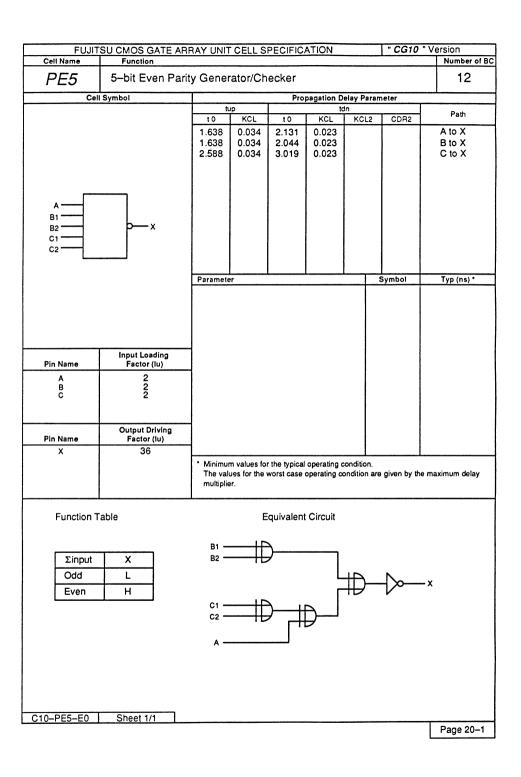
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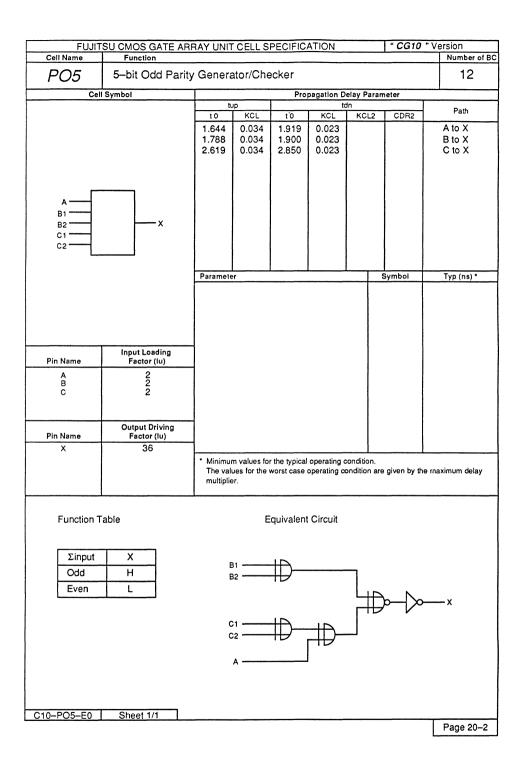
3-288

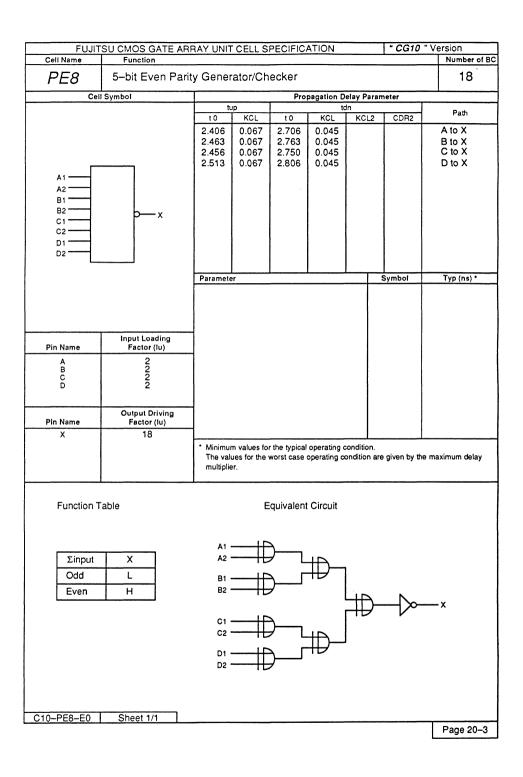
C10-SR1-E0 | Sheet 3/3

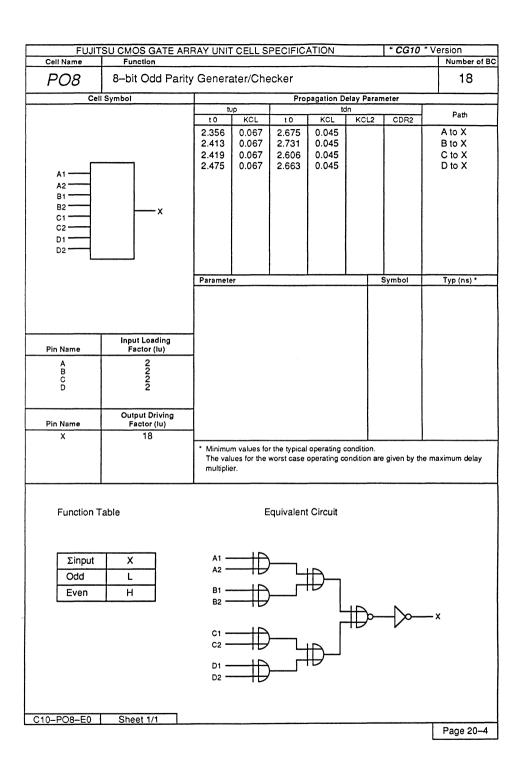
# Parity Generator/Selector/Decoder Family

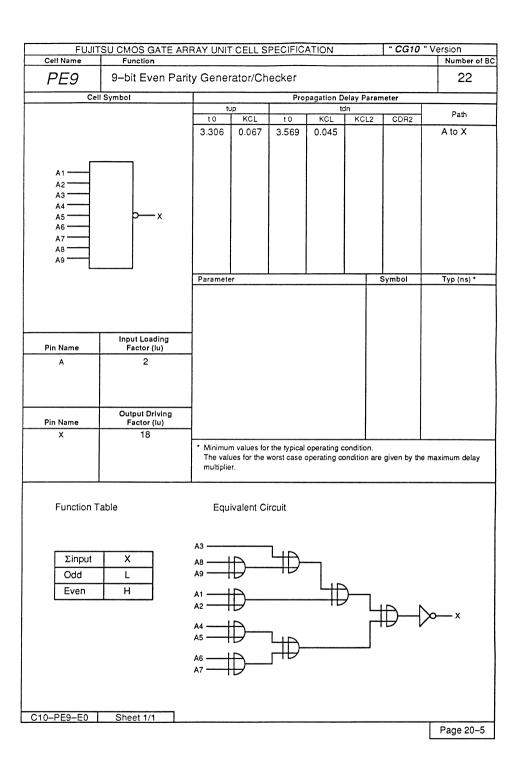
Page	Unit Cell Name	Function	Basic Cells
Parity Gen	erators/Ch	eckers	
3-291	PE5	5-bit Even Parity Generator/Checker	12
3–292	PO5	5-bit Odd Parity Generator/Checker	12
3–293	PE8	8-bit Even Parity Generator/Checker	18
3-294	PO8	8-bit Odd Parity Generator/Checker	18
3–295	PE9	9-bit Even Parity Generator/Checker	22
3–296	PO9	9-bit Odd Parity Generator/Checker	22
Data Selec	tor		
3–297	P24	2:1 Data Selector	12
Decoders			
3-298	DE2	2:4 Decoder	5
3-299	DE3	3:8 Decoder	15
3-301	DE4	2:4 Decoder	8
3–302	DE6	3:8 Decoder	30
Selectors			
3-304	T2B	2:1 Selector	2
3-305	T2C	2:1 Selector	4
3-307	T2D	2:1 Selector	2
3-308	T2E	2:1 Selector	5
3-309	T2F	2:1 Selector	8
3-311	T5A	4:1 Selector	5
3-313	V3A	1:2 Selector	2
3-314	V3B	1:2 Selector	4
Magnitude	Comparate	or	
3–315	MC4	Magnitude Comparator	42

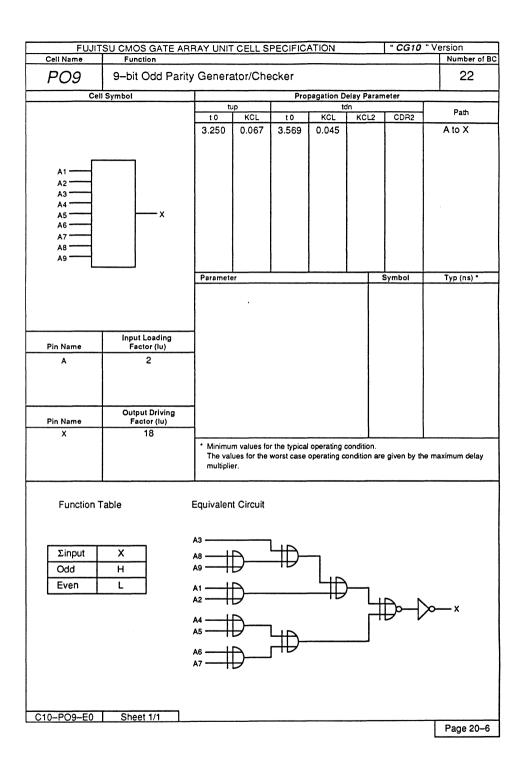


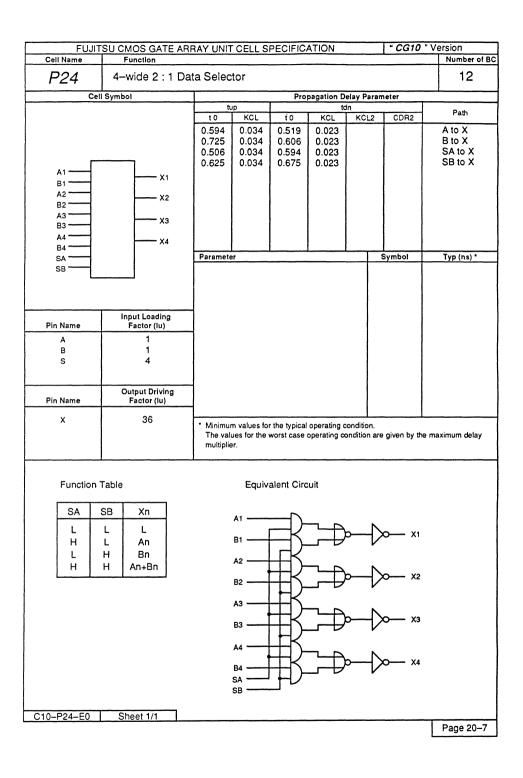


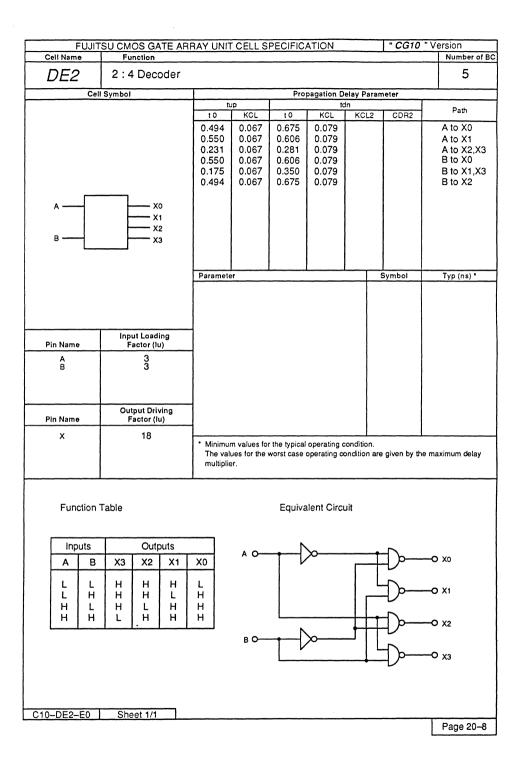










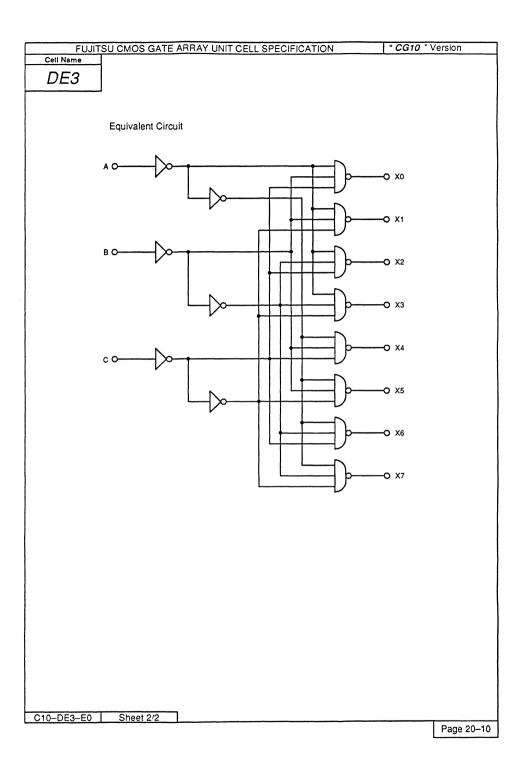


	SU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG10 " Ve									
Cell Name	Function							Number of E		
DE3	3:8 Decoder							15		
Ce	II Symbol		Propagation Delay Parameter							
			ap qu		Path					
		t 0	KCL	t O	KCL	KCL2	CDR2			
		0.900	0.067	1.044	0.107			A to X0~X3		
		1.525	0.067 0.067	1.525 1.075	0.107 0.107		1 1	A to X4~X7 B to X0~X3		
		1.456	0.067	1.556	0.107		1	B to X4~X7		
A —	X0 X1	0.769	0.067	1.113	0.107			C to X0~X3		
^	1.394	0.067	1.594	0.107		1 1	C to X4~X7			
_	X2 X3						1 1			
В ——	X4									
	X5						1 1			
c —	X6									
1	X7									
						L	<u> </u>			
		Paramete	er				Symbol	Typ (ns) *		
		1				1				
	Input Loading	1								
Pin Name	Factor (lu)	]								
A	1					-				
В	1					- 1				
С	1									
		ļ				1				
	Output Driving	ł				ĺ				
Pin Name	Factor (lu)									
	14	<u> </u>								
X	14		m values for							
				worst case	operating $\alpha$	ondition a	re given by th	e maximum delay		
	1	multiplie	er.							

	Inputs		Outputs								
Α	В	С	X0	X1	X2	Х3	X4	X5	X6	X7	
L L L H H H H				H	H H H H H H H	H H H H H H H	H H H L H H H	H H H H H H	H H H H H L H	* # # # # # # .	

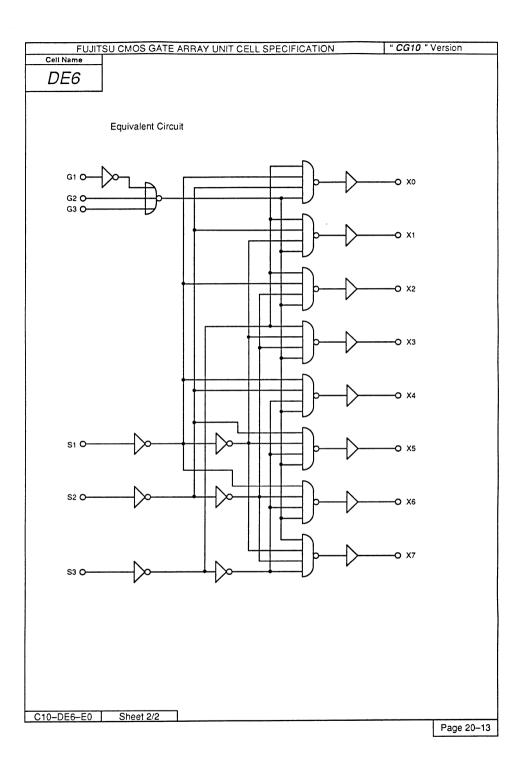
C10-DE3-E0 Sheet 1/2

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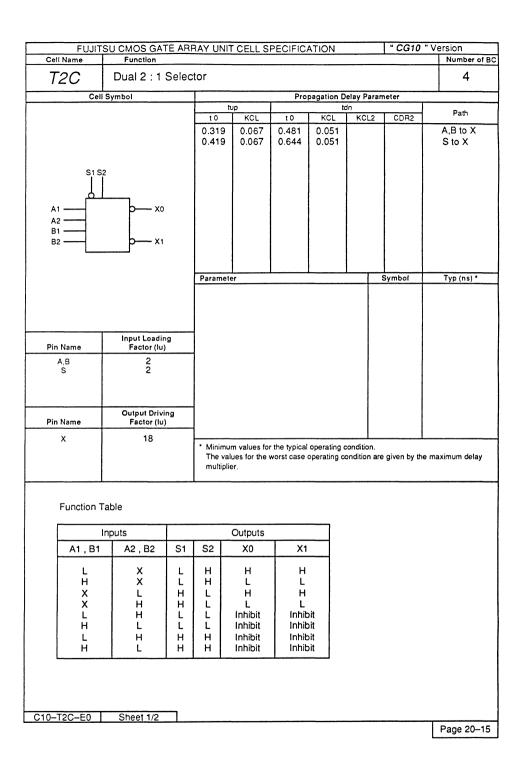


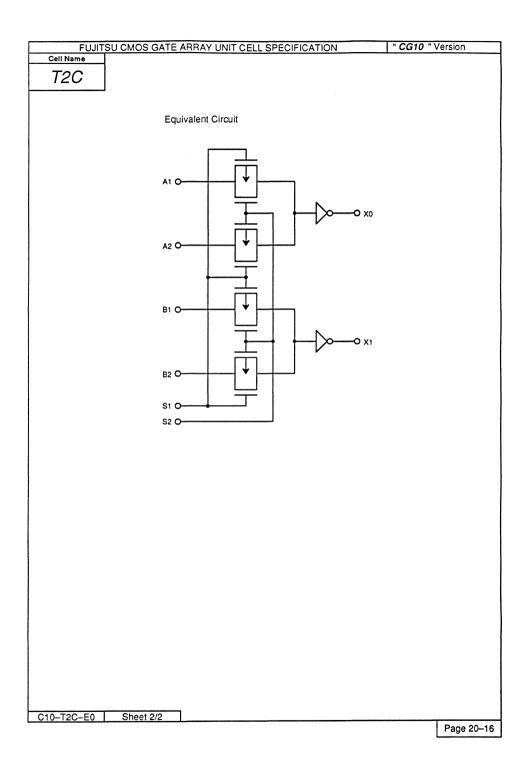
	ELLUT	6110	MOS	CATE	ADD	AV LINIT	CELLS	PECIFICA	ATION		" CG10	" Version
Cell Na	me	300	Functio	n .	Ann	AT UNIT	CELL S	PECIFICA	ATION		CG10	Number of BC
DE	4	2	2 : 4 Decoder with Enable									
	Cel	Symb	ol					Pro	pagation D		eter	
					}	t O	KCL	tdn tdn KCL KCL		MCL2	CDR2	Path
A — X0 D— X1 D— X2 D— X3						0.744 0.067 0.913 0.107 0.538 0.067 0.694 0.107 0.669 0.067 0.713 0.107						G to X A to X B to X
i					-	Paramete	er				Symbol	Typ (ns) *
Pin Na	me		nput Lo Factor									
A B G			3 3 1									
Pin Na	me	۱-,	Output I		$\dashv$							
×			14				ues for the	r the typical worst case			given by the	e maximum delay
Fund	ction Ta	ble							Equivale	nt Circuit	l	
<del></del>							G.		>			
G H	A X	B X	Х3 Н	X2 H	X1 H	н	Α.		>>   		D-	— хо
L L L	L H H	L H H	H H L	H L H	HLHH	H H H	— x1					
							В	<del></del>	×			— X2 — X3
C10-DE	4–E0	<u> </u>	heet 1	/1								Page 20-11

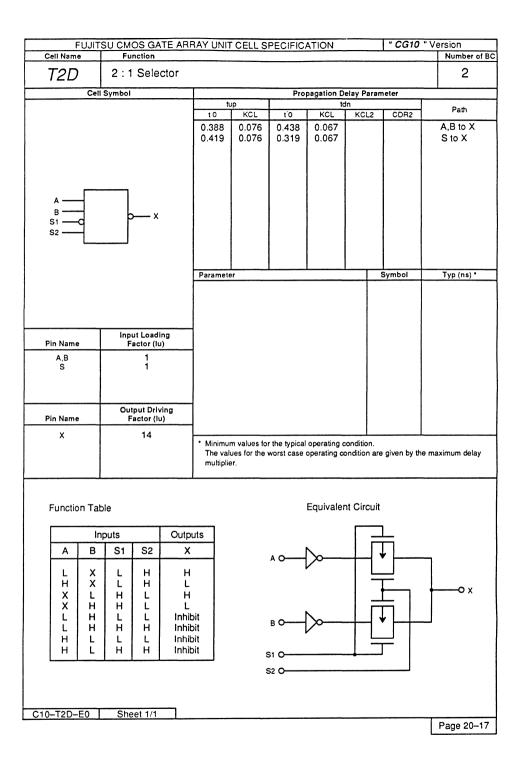
FUJIT	SU CMOS GATE AR	RAY UNIT	CELLS	PECIFI	CAT	ION		٦.	CG10 "	Version
Cell Name	Function									Number of BC
DE6	3:8 Decoder w	ith Enab	le							30
Cel	l Symbol	ļ		P	ropaç	gation D		aramet	er	
		t O	KCL	f O	<b>—</b>	KCL	dn KCL	2	CDR2	Path
		1.906 1.806	0.067 0.067	3.719 2.050		0.045 0.045				G to X S to X
G1 G2 G3 S1 S2 S3	G2 X1 G3 X2 S1 X3 S2 X4 Y5									
		Paramete	r	·				Sy	mbol	Typ (ns) *
	Input Loading									
Pin Name	Factor (Iu)	4					-		ŀ	
G S										
Pin Name	Output Driving Factor (Iu)									
х	18								ven by the	maximum delay
Function Tab	ile									
G1 G2+	-G3 S3 S2 S1	X7	X6 X	5 X4	ХЗ	X2	X1	X0		
X H		Н	H F		H	H H	H H	H H		
H L	.   L L H	H	H F	н н	Н	H H	H L	L H		
H		H H H H L	H	1 H 1 L 1 H	H	H H H	H	H H H H H H		
C10-DE6-E0	Sheet 1/2								]	Page 20–12

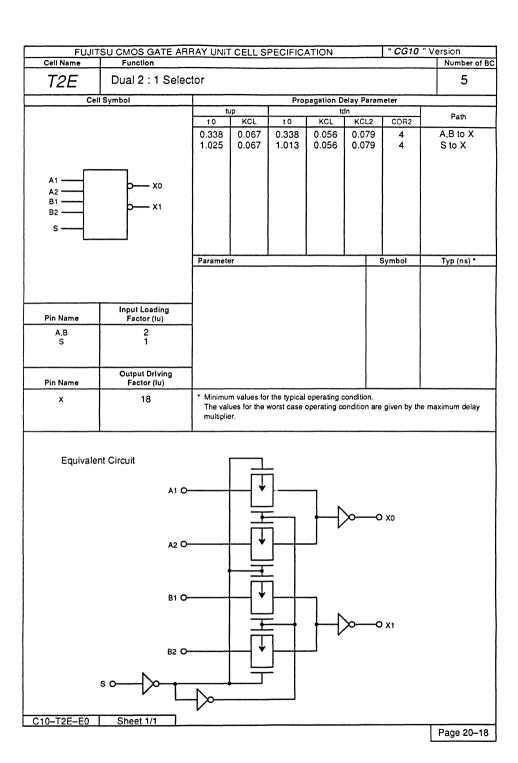


Cell Na			MOS G		RAY UNIT	CELLS	PECIFIC	ATION		" CG10	" Version Number of BC
T21			1 Sel								2
		l Symbo	ol				Pro	pagation D	elay Paran	neter	
						ıp		to	dn		Path
					0.325	KCL 0.067	t 0 0.488	0.051	KCL2	CDR2	A,B to X
					0.381	0.067	0.619	0.051			S to X
ļ											
	_		1								
A — B —											
S1 —	<b>-</b> d		þ	K							
S2 —											
					Paramete	l er	L	L	<u> </u>	Symbol	Typ (ns) *
										l	
Pin Na	Input Loading Pin Name Factor (lu)										
A,B											
			•								
Di- N-		0	utput Di								
Pin Nar	me	<del> </del>	Factor 18	iu)							
^			10				r the typical				
					multipli		worst case	operating o	ondition are	e given by the	e maximum delay
		<u> </u>									
Func	tion Ta	ble						Equivale	nt Circuit		
	1	outs	-	Output	s		ſ		_		
	В	S1	S2	X	_	А		$oldsymbol{ol}}}}}}}}}}}}}}}}$			
L	H	L	н	н	-	^					
H   X	H	L	H	L H				T			о—— о х
X	H	Н	L	L				Ţ	=		- • •
	H	H	L	Inhibi Inhibi		R	<b>-</b>	↓			
H	L	L	L	Inhibi	:				]		
Н	L	Н	Н	Inhibi		S1	$\longrightarrow$		_		
						S2					
C10-T2E	3-E0	SI	neet 1/	1							
											Page 20-14

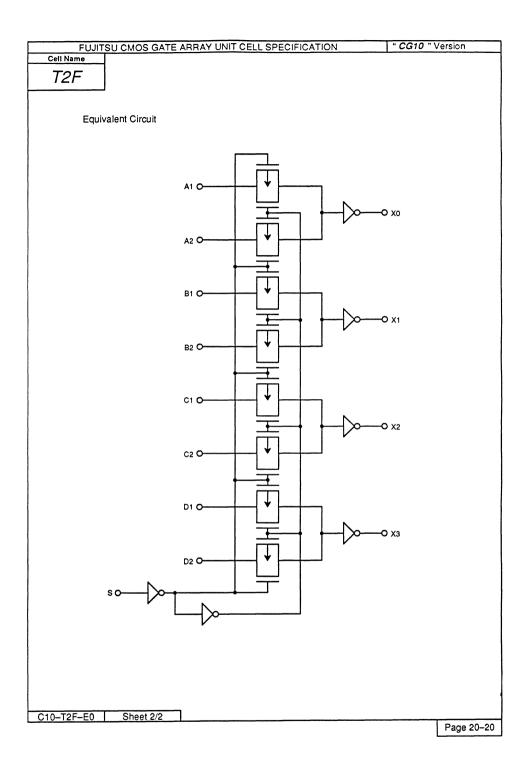








F	CHICAGO CATE ADI	2 A V 1 1 1 1 1 7	. 0511 0	DEOLEIO	TION		" CC10	" \/.	oroion 7
Cell Name	SU CMOS GATE ARE	HAY UNII	CELLS	PECIFICA	ATION		" CG10	V (	Number of BC
T2F	2:1 Selector								8
Cel	l Symbol			Pro	pagation D	elay Paran	neter		
			JP VCI			dn KCLO	CDD0		Path
		0.338	KCL 0.067	t 0 0.338	KCL 0.056	0.079	CDR2	Δ	,B,C,D to X
		1.025	0.067	1.013	0.056	0.079	4	^	S to X
A1 —		· ·				İ			
A2	þ— ×∘	l							
B1	b x1	1							
B2 ————————————————————————————————————	Γ	1							
C2	p x₂								
D1	<b>р—— х</b> з								
D2		1							
s —									
		Paramete	r				l Symbol	-	Typ (ns) *
							,		76 311-7
	Input Loading	-							
Pin Name	Factor (Iu)								
A,B,C,D S	2 1	ļ				- 1			
3	'								
	Output Driving	-							
Pin Name	Factor (lu)	j							
x	18					L_			
			m values for				aiven by th	e ms	aximum delay
		multiplie		WOISt Case	operating a	orianion are	given by a		ixiiidiii Gelay
									1
									İ
									1
									ļ
C10-T2F-E0	Sheet 1/2						-,		D 00 45
								L	Page 20-19



							•		
FUJIT Cell Name	SU CMOS GATE ARI	RAY UNIT	CELLS	PECIFIC	ATION		" CG10	" V	ersion Number of BC
T5A	4:1 Selector		***************************************						5
Cel	I Symbol	1		Pro	pagation D	elay Parar	neter		
		tup tdn							Path
,		t O	KCL	t O	KCL	KCL2	CDR2		
S1 S2 S3 S4 A1		0.625 0.625 0.350	0.097 0.097 0.097	0.625 0.525 0.338	0.090 0.090 0.090				A,B to X S1~4 to X S5~6 to X
B1 ————————————————————————————————————			er				Symbol		Typ (ns) *
		Paramete					<u> </u>		.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,
Pin Name	Input Loading Factor (lu)								
A.B S	1 1								
Pin Name	Output Driving Factor (lu)								
×	9	Minimum values for the typical operating condition.     The values for the worst case operating condition are given by the multiplier.						e ma	ximum delay

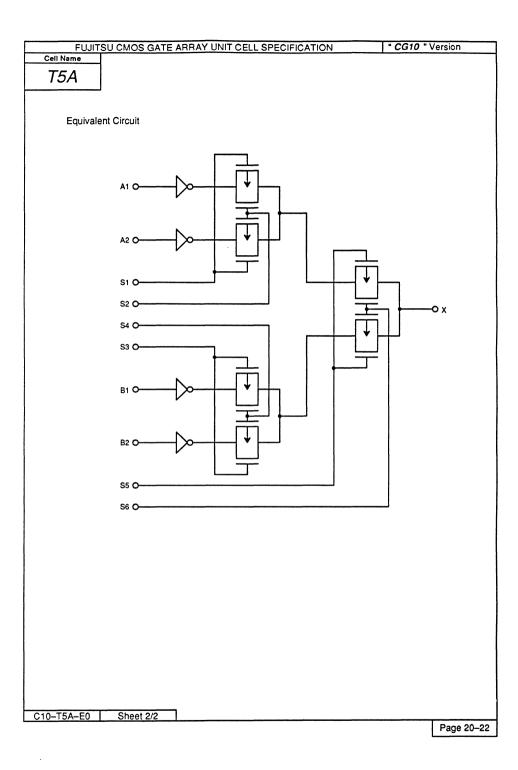
#### Function Table

Inputs											
A1	A2	B1	B2	S1	S2	S3	S4	S5	S6	X	
H	LΗ	L	LΗ	TIT	IIJJ	IIrr	T T L L		######	111111	

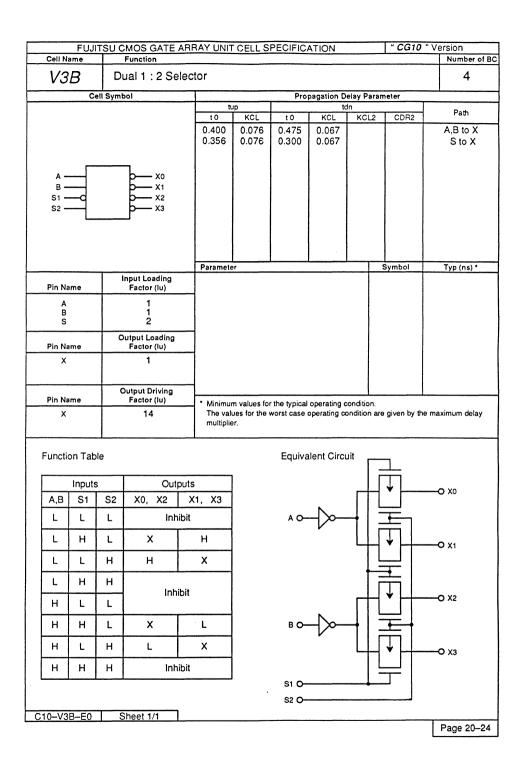
A1 $\neq$ A2 to S1=S2 or S5=S6 Inhibit B1 $\neq$ B2 to S3=S4 or S5=S6 Inhibit A1,A2 $\neq$ B1,B2 or S5=S6 Inhibit

C10-T5A-E0 | Sheet 1/2

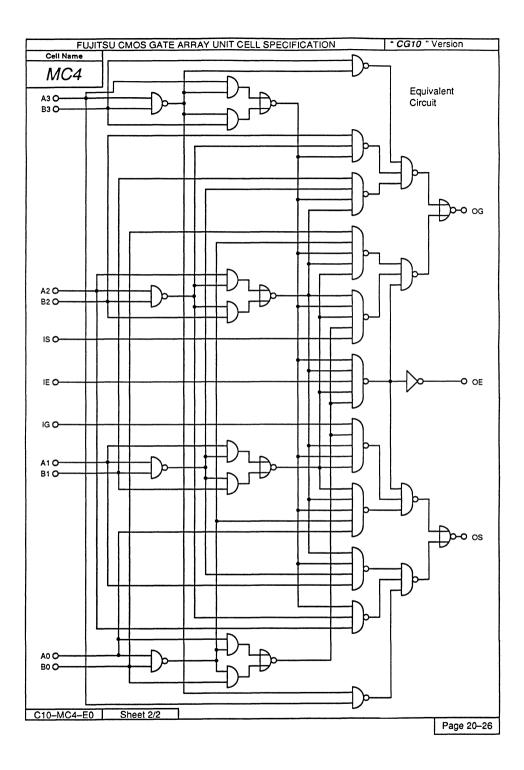
Page 20-21



				ATE AR	RAY UNIT	CELL S	PECIFIC	ATION		" CG10	" Version
Cell Nam			nction					<del></del>			Number of
V3A	.	1:2	Sele	ctor							2
	Cell	Symbol					Pro	pagation D		neter	
					t O	KCL	t O	KCL	MCL2	CDR2	Path
A — X0 S1 — X0 S2 — X1			0.388 0.344	0.076 0.076	0.438 0.281	0.067 0.067			A to X S to X		
G <sub>2</sub>					Paramete	er				Symbol	Typ (ns) *
Pin Name	.		ut Load actor (i								
A S			1 1								
Pin Name		Outp	out Loa actor (I	ding u)	1						
х		i	1	·							
Pin Name								operating o			
X			14		The val		worst case	operating o	ondition are	given by the	e maximum delay
Function	on Tab	le						Equivaler	nt Circuit		
	Input	s	Out	puts				-			
Α	S1	S2	X0	X1					<u></u>		
L	L	L	Int	ibit					↓  -		XO
L	Н	L	х	Н					닏		
L	L	Н	Н	x		A O-	<del> </del> >>-	<del> </del>			
L	Н	Н						Щ	$-\Box$	<del> </del> -	X1
Н	L	L	Int	nibit					무		
Н	Н	L	×	L			61 O 62 O				
Н	L	Н	L	Х							
Н	Н	Н	Inh	ibit							
			et 1/1								
10-V3A-											



FUJI	TSU CMOS	GATE ARE	RAY UNIT	CELL SF	PECIFICA	ATION		" CG10 "	Version	_
Cell Name	Funct									er of BC
MC4	4-bit !	Magnitude	Compai	rator					42	2
C	ell Symbol				Pro		elay Param	eter		
			t O	KCL	t O	KCL to	n KCL2	CDR2	Path	
A3 B3 B2 A2 B1 A3 B0		og oe os	3.306 3.363 1.475 1.206 3.238 3.294 1.406 1.331 3.556 3.488 1.338	0.122 0.122 0.122 0.122 0.122 0.122 0.122 0.122 0.122 0.067 0.067	3.950 3.881 1.738 1.506 4.081 4.013 1.869 1.444 2.725 2.781 0.894	0.045 0.045 0.045 0.045 0.045 0.045 0.045 0.045 0.051 0.051	0.062 0.062 0.062 0.062 0.062 0.062 0.062 0.062 0.067 0.067	4 4 4 4 4 4 4 4 4 4 4 4	A to C B to C IE to A to C B to C IE to A to C IE to IS to C A to C IE to IS to C	OS OS OS OG OG OG OE OE
			Parameter	<del>1</del>			S	ymbol	Typ (ns	·) •
	·									
Pin Name		oading or (lu)								
A	1	3 3						j		
B IE	[	1						-		
IG	ł	1								
IS	1	1						- 1		
Pin Name		t Driving or (lu)								
OE		18								
og os		10 10		es for the v		operating co		given by the	maximum d	elay
Function Ta	ıble									
	Compari	ng Inputs		Ca	ascading	Inputs		Outputs	3	]
A3, B3	A2, B2	A1, B1	A0, B0	IG (A>B)	IS (A <b< td=""><td>IE (A=B)</td><td>OG (A&gt;B)</td><td>OS (A<b)< td=""><td>OE (A=B)</td><td></td></b)<></td></b<>	IE (A=B)	OG (A>B)	OS (A <b)< td=""><td>OE (A=B)</td><td></td></b)<>	OE (A=B)	
A3>B3 A3 <b3 A3=B3 A3=B3 A3=B3 A3=B3 A3=B3 A3=B3 A3=B3 A3=B3 A3=B3 A3=B3</b3 	X X A2>B2 A2=B2 A2=B2 A2=B2 A2=B2 A2=B2 A2=B2 A2=B2 A2=B2 A2=B2	X X X X A1>B1 A1=B1 A1=B1 A1=B1 A1=B1 A1=B1 A1=B1	X X X X X A0>B0 A0>B0 A0=B0 A0=B0 A0=B0 A0=B0	X X X X X X X H L	X X X X X X X L H H L	X X X X X X H L L	H L H L L H L L H			
C10-MC4-E0	Sheet	1/2							·,	
									Page 2	0–25

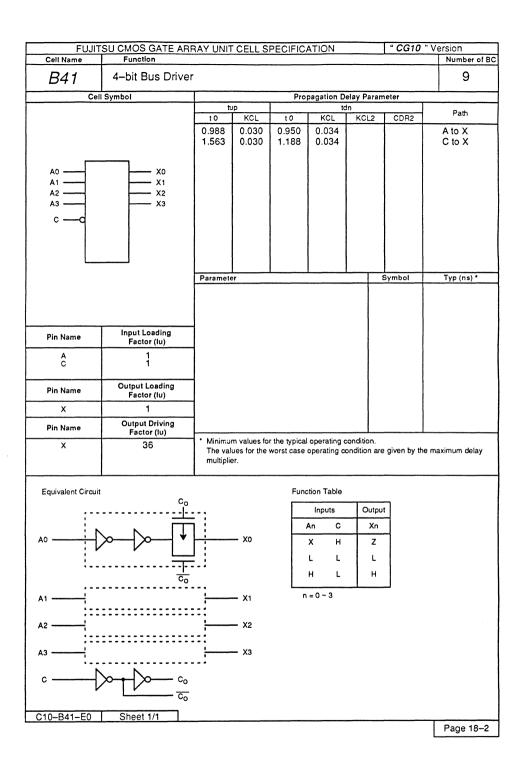


# **Bus Driver Family**

Page	Unit Cel Name	l Function	Basic Cells
3–319	B11	1-bit Bus Driver	5
3-320	B41	4-bit Bus Driver	9

3

EILIT	SU CMOS GATE ARF	TIVIT AV	CELLS	PECIFIC	ATION		" CG10	" Version
Cell Name	Function Function	INT UNIT	OELL 3	FEOIFIC	711011			Number of BC
B11	1-bit Bus Driver							5
				Dee	ti D	elay Param		
Cell	Symbol	tı	ıb	Pro		dn Param	leter	
		t O	KCL	t'O	KCL	KCL2	CDR2	Path
		0.931	0.038	0.869	0.028			A to X C to X
		0.738	0.038	0.606	0.028			Clox
A0	xo							
∘ —d								
		Paramete	<u></u>				Symbol	Typ (ns) *
		Faramete	-1				Jymbol .	7,45 (113)
						- 1		
						ł		
Pin Name	Input Loading							
	Factor (lu)					İ		
A C	1							
						ļ		
Pin Name	Output Loading Factor (lu)					ł		
x	1							
Pin Name	Output Driving Factor (lu)							
х	36		m values for				given by th	e maximum delay
		multiplie		Worst Case	operating G	ondition are	given by a	e maximum celay
Equivalent Circuit				Fund	tion Table			
	c <sub>o</sub>				Inputs	Output		
ĸ.	,				40 C	XO	]	
A0	➣┦➣┦╻╻		- xo		х н	Z	7	į
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					H L	Н		
N				<u> </u>			J	
c ————————————————————————————————————	<u>~</u> -~ <u>~</u>							
	$\frac{1}{c_0}$							
C10-B11-E0	Sheet 1/1							Page 18-1
								Fage 10-1



# 3

# Clip Cells

Page	Unit Cell Name		Function	Basic Cells
3–323	Z00	0 Clip		0
3-324	Z01	1 Clip		0

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG10" V							" Version	
Cell Name	Function							Number of BC
<i>Z00</i>	0 Clip							0
Cel	Symbol			Prop	pagation D		neter	
		t O	KCL	t O	KCL	MCL2	CDR2	Path
2	×				NO_	11002	05/12	
						L		
		Paramete	er				Symbol	Typ (ns) *
	land Lordin							
Pin Name	Input Loading Factor (lu)					- 1		
Pin Name X	Output Driving Factor (Iu) 200							
		<ul> <li>Minimur The value multiplie</li> </ul>		the typical worst case o	operating operating of	condition. ondition are	given by the	e maximum delay
C10-700 E0	Sheet 1/4							
C10-Z00-E0	Sheet 1/1							Page 19-1

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG10 '	' Version
Cell Name	Function							Number of BC
Z01	1 Clip							0
Cel	Symbol			Pro	pagation D		neter	
		t 0	KCL KCL	t O	KCL	KCL2	CDR2	Path
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						1		
7	<del></del>					1		
<b>\</b>	\/							
	Ĭ							
	X					1		
						L	<u> </u>	
		Paramete	er				Symbol	Typ (ns) *
							1	
							1	
Pin Name	Input Loading Factor (Iu)							
	racioi (iu)						-	
							1	
							1	
Pin Name	Output Driving						1	
X	Factor (lu) 200							
^	200	* Minimu	m values for	the typical	operating of	ondition.	L	
		The val	ues for the v				given by the	maximum delay
		multiplie	er.					
	L							
C10-Z01-E0	Sheet 1/1							
								Page 19–2

Page	Unit Cell Name	Function	Basic Cells
Input Bu	ffers		
3-329	I1B	Input Buffer (Inverter)	5
3-330	I1BU	I1B with Pull-up Resistance	5
3-331	I1BD	I1B with Pull-down Resistance	5
3-332	12B	Input Buffer (True)	4
3-333	I2BU	I2B with Pull-up Resistance	4
3-334	I2BD	I2B with Pull-down Resistance	4
3–335	IKB	Clock Input Buffer (Inverter)	4
3-336	IKBU	IKB with Pull-up Resistance	4
3–337	IKBD	IKB with Pull-down Resistance	4
3-338	IKC	CMOS Interface Clock Input Buffer (Inverter)	4
3–339	IKCU	IKC with Pull-up Resistance	4
3–340	IKCD	IKC with Pull-down Resistance	4
3–341	ILB	Clock Input Buffer (True)	6
3–342	ILBU	ILB with Pull-up Resistance	6
3–343	ILBD	ILB with Pull-down Resistance	6
3–344	ILC	CMOS Interface Clock Input Buffer (True)	6
3–345	ILCU	IKC with Pull-up Resistance	6
3–346	ILCD	IKC with Pull-down Resistance	6
3–347	I1C	CMOS Interface Input Buffer (Inverter)	5
3–348	I1CU	I1C with Pull-up Resistance	5
3–349	I1CD	I1C with Pull-down Resistance	5
3–350	I2C	CMOS Interface Input Buffer (True)	4
3–351	I2CU	I2C with Pull-up Resistance	4
3–352	I2CD	I2C with Pull-down Resistance	4
3–353	IIS	Schmitt Trigger Input Buffer (CMOS, Inverter)	8
3–354	IISU	I1S with Pull-up Resistance	8
3–355	IISD	I1S with Pull-down Resistance	8
3–356	12S	Schmitt Trigger Input Buffer (CMOS, True)	8
3–357	I2SU	I2S with Pull-up Resistance	8
3–358	I2SD	I2S with Pull-down Resistance	8
3–359	I1R	Schmitt Trigger Input Buffer (TTL, Inverter)	8
3–360	IIRU	I1R with Pull-up Resistance	8
3–361	I1RD	I1R with Pull-down Resistance	8
3–362	I2R	Schmitt Trigger Input Buffer (TTL, True)	8
3–363	I2RU	I2R with Pull-up Resistance	8
3–364	I2RD	I2R with Pull-down Resistance	8
Output B	luffers		
3-365	O1B <sup>1</sup>	Output Buffer (Inverter)	3
3-366	O1BF <sup>2</sup>	Output Buffer (Inverter)	3
			Continued on next page

 $<sup>{}^{1}</sup>I_{OL} = 3.2 \text{ mA}$  ${}^{2}I_{OL} = 8 \text{ mA}$  ${}^{3}I_{OL} = 12 \text{ mA}$ 

Page	Unit Cell Name	Function	Basic Cells
Output B	uffers		
3-367	O1L <sup>3</sup>	Power Output Buffer (Inverter)	3
3-368	O1R1	Output Buffer (Inverter) with Noise Limit Resistance	5
3-369	O1RF <sup>2</sup>	Output Buffer (Inverter)	5
3-370	O1S <sup>3</sup>	Power Output Buffer (Inverter) with Noise Limit Resistar	nce 5
3-371	O2B <sup>1</sup>	Output Buffer (True)	2
3-372	O2BF <sup>2</sup>	Output Buffer (True)	2
3-373	O2L <sup>3</sup>	Power Output Buffer (True)	2
3-374	O2R <sup>1</sup>	Output Buffer (True) with Noise Limit Resistance	4
3-375	O2RF <sup>2</sup>	Output Buffer (True) with Noise Limit Resistance	4
3-376	O2S <sup>3</sup>	Power Output Buffer (True) with Noise Limit Resistance	4
3-377	O4T <sup>1</sup>	3-state Output Buffer (True)	4
3-378	O4TF <sup>2</sup>	3-state Output Buffer (True)	4
3-379	O4W <sup>3</sup>	Power 3-state Output Buffer (True)	4
3-380	O4R <sup>1</sup>	Output Buffer (True) with Noise Limit Resistance	5
3–381	O4RF <sup>2</sup>	3-state Output Buffer (True) with Noise Limit Resistance	5
3–382	O4S <sup>3</sup>	Power 3-state Output Buffer (True) with Noise Limit Resistance	5
3–383	O2S2 <sup>4</sup>	High Power Output Buffer (True) with Noise Limit Resistance	6
3–384	O4S2 <sup>4</sup>	High Power Output Buffer (True) with Noise Limit Resistance	7
Bidirectio	nal I/O Buf	fers (Buses)	
3-385	H6T <sup>1</sup>	3-state Output and Input Buffer (True)	8
3-386	H6TU	H6T with Pull-up Resistance	8
3-387	H6TD	H6T with Pull-down Resistance	8
3-388	H6TF <sup>2</sup>	3-state Output and Input Buffer (True)	8
3-389	H6TFU	H6TF with Pull-up Resistance	8
3-390	H6TFD	H6TF with Pull-down Resistance	8
3-391	H6W <sup>3</sup>	Power 3-state Output and Input Buffer (True)	8
3-392	H6WU	H6W with Pull-up Resistance	8
3-393	H6WD	H6W with Pull-down Resistance	8
3-394	H6C <sup>1</sup>	3-state Output and CMOS Interface Input Buffer (True)	8
3-395	H6CU	H6C with Pull-up Resistance	8
3–396	H6CD	H6C with Pull-down Resistance	8
3-397	H6CF <sup>2</sup>	3-state Output and CMOS Interface Input Buffer (True)	8
3-398	H6CFU	H6CF with Pull-up Resistance	8
3-399	H6CFD	H6CF with Pull-down Resistance	8
3–400	H6E <sup>3</sup>	Power 3-state Output and CMOS Interface Input Buffer (True)	8
3–401	H6EU	H6E with Pull-up Resistance	8

Continued on next page

 $<sup>^{1}</sup>I_{OL} = 3.2 \text{ mA}$   $^{2}I_{OL} = 8 \text{ mA}$   $^{3}I_{OL} = 12 \text{ mA}$   $^{4}I_{OIL} = 24 \text{ mA}$ 

Page	Unit Cell Name	Function	Basic Cells
Bidirectio	nal I/O Buff	fers (Buses)	
3-402	H6ED	H6E with Pull-down Resistance	8
3–403	H6S <sup>1</sup>	3-state Output and Schmitt Trigger Input Buffer (CMOS, True)	12
3-404	H6SU	H6S with Pull-up Resistance	12
3-405	H6SD	H6S with Pull-down Resistance	12
3–406	H6R <sup>1</sup>	3-state Output and Schmitt Trigger Input Buffer (TTL, True)	12
3-407	H6RU	H6R with Pull-up Resistance	12
3-408	H6RD	H6R with Pull-down Resistance	12
3–409	H8T <sup>1</sup>	3-state Output with Noise Limit Resistance (True Input Buffer	e) and 9
3-410	H8TU	H8T with Pull-up Resistance	9
3-411	H8TD	H8T with Pull-down Resistance	9
3–412	H8TF <sup>2</sup>	3-state Output with Noise Limit Resistance (True Input Buffer	e) and
3-413	H8TFU	H8TF with Pull-up Resistance	
3-414	H8TFD	H8TF with Pull-down Resistance	
3-415	H8W <sup>3</sup>	Power 3-state Output and Input Buffer (True)	9
3-416	H8WU	H8W with Pull-up Resistance	9
3-417	H8WD	H8W with Pull-down Resistance	9
3–418	H8C <sup>1</sup>	3-state Output with Noise Limit Resistance and CMOS Interface Input Buffer (True)	9
3-419	H8CU	H8C with Pull-up Resistance	9
3-420	H8CD	H8C with Pull-down Resistance	9
3–421	H8CF <sup>2</sup>	3-state Output with Noise Limit Resistance (True Input Buffer	e) and
3-422	H8CFU	H8CF with Pull-up Resistance	
3-423	H8CFD	H8CF with Pull-down Resistance	
3–424	H8E <sup>3</sup>	Power 3-state Output with Noise Limit Resistance and CMOS Interface Input Buffer (True)	e 9
3-425	H8EU	H8E with Pull-up Resistance	9
3-426	H8ED	H8E with Pull-down Resistance	9
3–427	H8S <sup>1</sup>	3-state Output with Noise Limit Resistance and Schmitt Trigger Input Buffer (True)	13
3-428	H8SU	H8S with Pull-up Resistance	13
3-429	H8SD	H8S with Pull-down Resistance	13
3–430	H8R <sup>1</sup>	3-state Output with Noise Limit Resistance and Schmitt Trigger Input Buffer (True)	13
3-431	H8RU	H8R with Pull-up Resistance	13
3-432	H8RD	H8R with Pull-down Resistance	13
3-433	H8W2 <sup>4</sup>	High Power 3-state Output and Input Buffer	11
			Continued on next page

Page	Unit Cell Name	Function	Basic Cells
Bidirecti	onal I/O Buf	iers (Buses)	
3-434	H8W1	H8W2 with Pull-up Resistance	11
3-435	H8W0	H8W2 with Pull-down Resistance	11
3–436	H8E2 <sup>4</sup>	High Power 3-state Output with Noise Limit Resistance and Input Buffer (True)	11
3-437	H8E1	H8E2 with Pull-up Resistance	11
3-438	H8E0	H8E2 with Pull-down Resistance	11

 $<sup>{}^{1}</sup>I_{OL} = 3.2 \text{ mA}$   ${}^{2}I_{OL} = 8 \text{ mA}$   ${}^{3}I_{OL} = 12 \text{ mA}$   ${}^{4}I_{OIL} = 24 \text{ mA}$ 

FUJIT	SU CMOS GATE ARI	RAY UNIT	CELL S	PECIFICA	ATION		" CG10 '	' Version
Cell Name	Function							Number of BC
I1B	Input Buffer (In	verter)						5
Cel	l Symbol	I		Pro	pagation D	elay Param	neter	
			קנ			in		Path
		10	KCL	t 0	KCL	KCL2	CDR2	X to IN
		1.000	0.017	0.963	0.023			X to IN
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		Paramete	er		L	٠	Symbol	Typ (ns) *
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		1						
Pin Name	Input Loading Factor (lu)	1						
		1						
		İ						
	Output Driving	1				i		
Pin Name	Factor (lu)	-						
IN	36	• Minimu	m values fo	t the tunion	Lancratina		L	
		The val	ues for the	worst case	operating o	ondition are	given by the	maximum delay
		multipli	er.					
	1	1						
C10-I1B-E0	Sheet 1/1							
								Page 21-1

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG10" Vei								ersion	
Cell Name	Function								Number of BC
	Input Buffer (Inv	verter)							5
I1BU	with Pull-up Res	sistance	)						3
Cell Symbol Propagation Delay Parameter								·	
			ıρ		tx	nt			Path
		t O	KCL	t O	KCL	KCL2	CDR2		
		1.000	0.017	0.963	0.023	l			X to IN
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		Paramete	L er	L	<u> </u>	<del>'                                    </del>	Symbol		Typ (ns) *
						[			
						1			
	Input Loading	1							
Pin Name	Factor (lu)								
						1			
		ŀ							
	Output Driving	l							
Pin Name	Factor (lu)					1			
IN	36								
	30	* Minimu	m values fo	r the typica	loperating	condition.			
		The val	ues for the				re given by th	e ma	aximum delay
		multipli	er.						
	L	L							
C10-I1BU-E0	Sheet 1/1								
								- [	Page 21-2

FILIT	SUCMOS GATE ARE	SU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG10" Version							
Cell Name	Function	0							
	Input Buffer (Inv	verter)						Number of BC	
I1BD	with Pull-down	Resistar	nce					5	
Cell	Symbol	Γ		Proj	pagation D	elay Paran	neter		
		t.			t	dn		Path	
		t O	KCL	t O	KCL	KCL2	CDR2		
		1.000	0.017	0.963	0.023	ł		X to IN	
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		Paramete	эт				Symbol	Typ (ns) *	
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		İ							
						-	1		
						1			
	Input Loading	l				- 1			
Pin Name	Factor (lu)					- 1			
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	Output Driving					İ			
Pin Name	Factor (iu)	l				1			
IN	36	L							
""	30	• Minimu	n values for	the typical	operating	condition.			
		The val	ues for the				given by the	maximum delay	
		multiplie	er.						
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C10-I1BD-E0	Sheet 1/1								
								Page 21-3	

CG10 * Vec   Vec	ersion
Cell Symbol   Propagation Delay Parameter   tup   tdn	
Propagation Delay Parameter	Number of BC
tup tdn  10 KCL 10 KCL KCL2 CDR2  0.663 0.017 1.150 0.023	4
x ————————————————————————————————————	
x — IN	Path
x —— IN	X to IN
	, , , , , , , , , , , , , , , , , , ,
Parameter Symbol	
ļ	Typ (ns) *
i i	
Input Loading	
Pin Name Factor (Iu)	
Output Driving	
Pin Name Factor (Iu)	
IN 36 * Minimum values for the typical operating condition.	
The values for the worst case operating condition are given by the ma	aximum delay
multiplier.	•
C10-I2B-E0   Sheet 1/1	
	Page 21-4

FUJIT	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG10" Ve								ion
Cell Name	Function								lumber of BC
I2BU	Input Buffer (Tru with Pull-pu Res	Je)						$\top$	4
	Symbol	, statice		Pror	pagation D	elay Par	ameter		
		tu			tc	in			Path
		t 0	KCL	't O	KCL	KCL2	CDR2		
		0.663	0.017	1.150	0.023			Х	to IN
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		Paramete	<b>31</b>			$\dashv$	Symbol		yp (ns) *
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		1							
<b>.</b>	Input Loading	ļ							
Pin Name	Factor (lu)	ľ							
	l '	ļ							
-									
	Output Driving								
Pin Name	Factor (lu)	į							
IN	36	<b> </b>							
			m values fo						sum dol
		The val multiplie		worst case	operating c	ondition .	are given by th	maxin	ium oelay
	L	L							
C10-I2BU-E0	Sheet 1/1							<del></del>	
								ΙP	age 21-5

	SU CMOS GATE ARF	RAY UNIT	CELL S	PECIFICA	ATION		" CG10 "	
Cell Name	Function							Number of BC
I2BD	Input Buffer (Tru	ue)						4
	with Pull-down I	Resistar	nce					
Cell	Symbol			Proj	pagation D		neter	
		t O	KCL	t O	KCL	fn KCL2	CDR2	Path
						NOL2	CDN2	X to IN
		0.663	0.017	1.150	0.023	ł	1 1	X 10 114
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		Paramete	Ļ		L	L	Symbol	Typ (ns) *
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	Input Loading					1	l	
Pin Name	Factor (lu)					l	1	
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	Output Driving					l	I	
Pin Name	Factor (lu)					i	į.	
IN	36							
",			m values fo					
				worst case	operating c	ondition are	given by the	maximum delay
		multiplie	er.					
		<b></b>						
C10-I2BD-E0	Sheet 1/1				-			
								Page 21-6

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL SI	PECIFICA	ATION		" CG10	* Ver	sion
Cell Name Function									Number of BC
IKB	Clock Input Buff	er (Inve	erter)						4
Cel	l   Symbol			Pro	pagation D	elay Paran	neter		
			KCL	10	KCL to	ln KCL2	0000		Path
		1.540	0.006	t 0 1.010	0.005	KCL2	CDR2	<del></del> ,	X to CI
		1.540	0.000	1.010	0.000			ĺ	
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		Paramete	H			<u> </u>	Symbol	-	Typ (ns) *
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	Input Loading	1							
Pin Name	Factor (lu)	Į							
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	Output Driving	1							
Pin Name	Factor (lu)	l							
CI	200	* Minimu	m values fo	the traine	apprating (	ondition.		L	
		The val	ues for the	worst case	operating o	ondition are	given by th	e maxi	imum delay
		multipli	er.						
	1	·							
C10-IKB-E0	Sheet 1/1								
									Page 21-7

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG10" Ver							Version	
Cell Name	Function	MT UNII	UELL SI	FECIFICA	ATION		1 0010	Number of BC
IKBU	Clock Input Buffe with Pull-up Res	er (Inve	erter)				7	4
Cell	Symbol	Sistance	<u></u>	Pro	pagation D	elay Paran	neter	
			ıp		tc	nt		Path
		t O	KCL	t O	KCL	KCL2	CDR2	
		1.540	0.006	1.010	0.005		1 1	X to CI
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		Paramete	<b>*</b>				Symbol	Typ (ns) *
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	Input Loading					1	İ	
Pin Name	Factor (lu)					1	ľ	
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							-	
	Output Driving							
Pin Name	Factor (lu)	l					ŀ	
CI	200							
		The val	m values follows for the	r me typica worst case	operating o	condition. condition ar	e given by the	e maximum delay
		multipli					• •	•
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C10-IKBU-E0	Sheet 1/1							
								Page 21_8

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION							" CG10 " Version	
Cell Name	Function	AT UNII	UNIT CELL SPECIFICATION					Number of BC
		or (Inverter)						
IKBD	Clock Input Buffe	er (mverter)						4
	with Pull-down Resistance Propagation Delay Parameter							
Cell Symbol		Propagation Delay Pa					ineres.	
		t O	KCL	t O	KCL	KCL2	CDR2	Path
_		1.540	0.006	1.010	0.005			X to CI
		1.540	0.000	1.010	0.000	ŀ	1 1	
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		Paramete	L	L		<u> </u>	Symbol	Typ (ns) *
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Pin Name	Input Loading Factor (Iu)						1	
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	Output Driving	1					1	
Pin Name	Factor (lu)						ł	
CI	200							
<b>.</b>		* Minimum values for the typical operating condition.						
		The values for the worst case operating condition are given by the maximum delay						
	multiplier.							
C10-IKBD-E0	Sheet 1/1							
								Page 21-9

FILIIT	SU CMOS GATE ARE	GATE ARRAY UNIT CELL SPECIFICATION " CG10" \								
Cell Name	Function	01111	JEEL O						Number of BC	
IKC	CMOS Interface	Clock I	nput Bu	ffer (Inv	erter)				4	
Cell	Symbol		·	Pro	pagation D		neter			
			ıp			dn KOLO	I 0000		Path	
		1 220	KCL	· t 0	KCL	KCL2	CDR2	-	X to CI	
		1.320	0.006	0.960	0.005				X 10 C1	
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		Paramete	<del>2</del> 7				Symbol	<del> </del>	Typ (ns) *	
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	Input Loading					1		l		
Pin Name	Factor (lu)					I		ĺ		
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Pin Name	Output Driving Factor (lu)									
		1						l		
CI	200	* Minimu	m values fo	r the typical	operating	condition.		·		
		The val	ues for the				e given by th	e ma	aximum delay	
		multipli	er.							
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C10-IKC-E0	Sheet 1/1		······							
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FILIT	SU CMOS GATE ARE	RAY LINIT	CELLS	PECIFIC	ATION		" CG10	" Version
Cell Name	Function	IAT ONL	OLLE 3	ECIFICA	ATION		00.0	Number of BC
	CMOS Interface	Clock I	nput Bu	ffer (Inv	erter)			
IKCU	with Pull-up Re	sistance	. <sub>-</sub> u					4
	Symbol	1		Pro	pagation D	elay Paran	neter	
		tı	dr.			n	T	
		t O	KCL	t 0	KCL	KCL2	CDR2	Path
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		Paramet	er	L	L		Symbol	Typ (ns) *
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	Input Loading	1				1		
Pin Name	Factor (lu)					l		
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Pin Name	Output Driving Factor (lu)							
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CI	200			. 4				
		The va	m values fo	r the typica worst case	operating o	condition ar	e aiven by the	e maximum delay
		multipli		WOID! 0000	opolating o	0110110111 411	s given ey an	o maximom colay
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C10-IKCU-E0	Sheet 1/1							
	JIEELI/I							Dog 01 11
								Page 21-11

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL SI	PECIFICA	ATION		" CG10	" Version
Cell Name	Function	Ola alı I	A D.	H /1				Number of BC
IKCD	CMOS Interface	Clock	nput Bu	πer (inv	ener)			4
	with Pull-down	Hesistai	nce					
Cell	Symbol			Proj	pagation D		eter	
			IP			in		Path
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		Paramete	×				Symbol	Typ (ns) *
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Pin Name	Input Loading Factor (lu)	į						
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		1						
	Output Driving	1				i		
Pin Name	Factor (lu)	l						
CI	200							
O.	200	Minimu	m values fo	r the typical	operating	condition.		
		The val	ues for the	worst case	operating c	ondition are	given by the	maximum delay
		multipli	er.					
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C10-IKCD-E0	Sheet 1/1							
210-100D-E0	I SHEELI/I							

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG10" Version												
Cell Name	Function	MT UNII	OELL SI	-EUIFIU	ATION		1 2010		Number of BC			
		0. /Tm:	-\						6			
ILB	Clock Input Buff	er (Iru	e)						'			
Cell	Symbol			Proj	pagation D		neter					
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		0.530	KCL 0.006	1.300	KCL 0.005	KCL2	CDR2	-	X to CI			
		0.530	0.006	1.300	0.005				X 10 C1			
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		Paramete	<u> </u>		L	Ц	Symbol	-	Typ (ns) *			
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Die Neese	Input Loading	]										
Pin Name	Factor (lu)	ł										
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	Output Driving	1				1						
Pin Name	Factor (lu)											
CI	200							<u> </u>				
		* Minimu	m values fo	r the typical	operating	condition.	: <b>b s</b> t					
		multipli		worst case	operating c	onomon are	e given by tr	e ma	aximum delay			
: 												
C10-ILB-E0	Sheet 1/1											
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	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG10			
Cell Name	Function Clock Input Buffe	or (Tru	9)					Number of BC		
ILBU	with Pull-up Res	sistance	= <i>j</i>					6		
	Symbol	1.0.01.00		Pro	pagation D	elay Para	meter			
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		t 0	KCL	t O	KCL	KCL2	CDR2			
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		Paramete	BY				Symbol	Typ (ns) *		
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	Input Loading	1					ĺ			
Pin Name	Factor (lu)	[					ŀ			
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Pin Name	Output Driving Factor (lu)						ŀ			
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CI	200	• Minimu	m values fo	r the typical	operating	condition				
		The val	lues for the				re given by the	e maximum delay		
		multipli	er.							
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C10-ILBU-E0	Sheet 1/1									
								Page 21-14		

FULITISU CMOS GATE ARRAY UNIT CELL SPECIFICATION  Cell Name  Function  (Cell Name  Function  (Cell Name  (Cell Symbol)  Cell Symbol  Cell Symbol  Cell Symbol  Cell Symbol  Cell Symbol  For the propagation Delay Parameter    Do   NCL   10   NCL   CDR   NcL   CDR	FILUT	SU CMOS GATE ARE	RAY UNIT	CELLS	PECIFIC	ATION		" CG10	" Ve	ersion
Call Symbol Parameter    Symbol   Propagation Delay Parameter   Path		Function			LOII 10/	711014		1	Ì	
Cell Symbol  Tup to	IIRD	Clock Input Buff	er (Tru	e)						6
Parameter  CI  To KCL 10 KCL 1			Resista	nce						U
Parameter  CI  Parameter  Symbol  Typ (na)*  Pin Name  Pin Name  Cutput Driving Factor (lu)  Pin Name  A minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10-ILBD-E0   Sheet 1/1	Cell	Symbol	<del>                                     </del>		Pro			neter		
Parameter Symbol Typ (ns)*  Pin Name Pactor (tu)  CI 200  *Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10-ILBD-E0   Sheet 1/1					't 0			CDR2		Path
Pin Name Input Loading Factor (lu)  Pin Name Seator (lu)  CI 200  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.										X to CI
Pin Name Input Loading Factor (lu)  Pin Name Seator (lu)  CI 200  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						1	1	1 1		
Pin Name Input Loading Factor (lu)  Pin Name Seator (lu)  CI 200  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.			j					1 1		
Pin Name Input Loading Factor (lu)  Pin Name Seator (lu)  CI 200  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.			l				ĺ			
Pin Name Input Loading Factor (lu)  Pin Name Seator (lu)  CI 200  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	1							1 1		
Pin Name Input Loading Factor (lu)  Pin Name Seator (lu)  CI 200  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.			ł							
Pin Name Input Loading Factor (lu)  Pin Name Seator (lu)  CI 200  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	x	cı								
Pin Name   Input Loading   Factor (lu)    Pin Name   Output Driving   Factor (lu)    CI   200   * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10-ILBD-E0   Sheet 1/1				i						
Pin Name   Input Loading   Factor (lu)    Pin Name   Output Driving   Factor (lu)    CI   200   * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10-ILBD-E0   Sheet 1/1						<b>!</b>	1	1		
Pin Name   Input Loading   Factor (lu)    Pin Name   Output Driving   Factor (lu)    CI   200   * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10-ILBD-E0   Sheet 1/1							İ			
Pin Name   Input Loading   Factor (lu)    Pin Name   Output Driving   Factor (lu)    CI   200   * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10-ILBD-E0   Sheet 1/1			<u> </u>			<u> </u>	L			T
Pin Name  Output Driving Factor (Iu)  CI  200  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10—ILBD—E0   Sheet 1/1			Paramete	er .				Symbol		Typ (ns) -
Pin Name  Output Driving Factor (Iu)  CI  200  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10—ILBD—E0   Sheet 1/1								l		
Pin Name  Output Driving Factor (Iu)  CI  200  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10—ILBD—E0   Sheet 1/1							1	j		
Pin Name  Output Driving Factor (Iu)  CI  200  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10—ILBD—E0   Sheet 1/1			İ							
Pin Name  Output Driving Factor (Iu)  CI  200  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10—ILBD—E0   Sheet 1/1							į.	ŀ		
Pin Name Pactor (tu)  CI 200  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10—ILBD—E0 Sheet 1/1	Dia Nama	input Loading	1							
Pin Name Factor (Iu)  CI 200  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10—ILBD—E0 Sheet 1/1	Pin Name	ractor (IU)	1							
Pin Name Factor (Iu)  CI 200  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10—ILBD—E0 Sheet 1/1			İ							
Pin Name Factor (Iu)  CI 200  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10—ILBD—E0 Sheet 1/1							1			
Pin Name Factor (Iu)  CI 200  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10—ILBD—E0 Sheet 1/1			l					į		
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  **C10—ILBD—E0   Sheet 1/1		Output Driving	1				1			
Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10—ILBD—E0   Sheet 1/1	Pin Name	Factor (lu)	l							
The values for the worst case operating condition are given by the maximum delay multiplier.  C10—ILBD—E0   Sheet 1/1	CI	200						i		
C10–ILBD–E0   Sheet 1/1			1 171111110					e aiven by the	e ma	ximum delav
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	C10-II BD-F0	Sheet 1/1								
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ELLIT	CHICMOS CATE ADE	TIMIL VAC	CELL C	DECIFIC	ATION		" CG10	* Vc	reion
Cell Name									Number of BC
ILC	CMOS Interface	Clock I	nput Bu	ffer (Tru	ie)				6
Cell	Symbol	T		Proj	pagation D	elay Parar	neter		
		tı			to	in nt			Path
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		Paramete	<b>9</b> 7				Symbol		Typ (ns) *
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	Input Loading	1						l	
Pin Name	Factor (iu)	j							
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Pin Name	Factor (lu)	1						l	
CI	200	• Minimu	m values fo	r the typica	operating (	condition		L	
		The val	ues for the				e given by th	e ma	ximum delay
		multipli	er.						
	<u> </u>								
C10-ILC-E0	Sheet 1/1								
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FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG10" Vei											
Cell Name	Function	IAT ON	OLLL SI	ECIFICA	TION		00.0	<del>- ĭï</del>	Number of BC		
	CMOS Interface	Clock I	nput Bu	ffer (Tru	ie)				6		
ILCU	with Pull-up Res	sistance	,	•	•			- 1	0		
Cell	Symbol			Proj	pagation D	elay Paran	neter				
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		Paramete	<b>3</b> 4				Symbol	<del> </del>	Typ (ns) *		
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	Input Loading					1					
Pin Name	Factor (lu)					1					
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Pin Name	Output Driving Factor (lu)										
CI	200	* Minimu	m values fo	the typical	operating	condition					
		The val	ues for the				e given by th	ne max	imum delay		
		multipli	er.								
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C10-ILCU-E0	Sheet 1/1										
								1	Page 21-17		

	SU CMOS GATE ARF	RAY UNIT	Version					
Cell Name	Function							Number of BC
ILCD	CMOS Interface	Clock I	nput Bu	ffer (Tr.	ıe)			6
ILUD	with Pull-down I	Resistar	nce					
Cell	Symbol			Pro	pagation D	elay Parar	neter	
		tı	ιp			dn		
		t O	KCL	t O	KCL	KCL2	CDR2	Path
		0.900	0.006	1.550	0.005			X to CI
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		Paramete	<u></u>	L	L		Symbol	Typ (ns) *
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	Input Loading							
Pin Name	Factor (lu)					1	i	
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						- 1		
Di- N	Output Driving						1	
Pin Name	Factor (lu)	1						
CI	200							
			m values fo					
				worst case	operating o	ondition ar	e given by the	maximum delay
		multiplie	er.					
		L						
C10-ILCD-E0	Sheet 1/1							
								Page 21-18

Call Symbol  Call Symbol  Call Symbol  Dip   Propagation Delay Parameter   Path      10   KCL   10   KCL   COR2   Path	FUJIT Cell Name	SU CMOS GATE ARF	RAY UNIT	CELL S	PECIFICA	ATION		" CG1	0 "\	/ersion Number of BC
tup KCL 10 KCL KCL2 CDR2 Path  0.600 0.017 0.100 0.017 X to IN  Parameter Symbol Typ (ns)*  Pin Name Pactor (lu)  IN 36 **Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I1C–E0 Sheet 1/1			Input B	uffer (I	nverter)				-	
10   KCL   10   KCL   KCL2   CDR2   Faul	Cell	Symbol			Proj			rameter		
Parameter Symbol Typ (ns)*  Pin Name Pactor (tu)  Pin Name Output Driving Factor (tu)  IN 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	1		t O	I KCI	10			2 CDB2	-	Path
Pin Name Input Loading Factor (tu)  Pin Name Sector (tu)  IN 36  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.									1	X to IN
Pin Name Input Loading Factor (tu)  Pin Name Sector (tu)  IN 36  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.										
Pin Name Input Loading Factor (tu)  Pin Name Sector (tu)  IN 36  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.										
Pin Name Input Loading Factor (tu)  Pin Name Sector (tu)  IN 36  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.										
Pin Name Input Loading Factor (tu)  Pin Name Sector (tu)  IN 36  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.										
Pin Name Input Loading Factor (tu)  Pin Name Sector (tu)  IN 36  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.		>> IN						1		
Pin Name   Coutput Driving Factor (Iu)    Pin Name   Pactor (Iu)    IN   36   Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	۲									
Pin Name   Coutput Driving Factor (Iu)    Pin Name   Pactor (Iu)    IN   36   Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.										
Pin Name   Coutput Driving Factor (Iu)    Pin Name   Pactor (Iu)    IN   36   Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.										
Pin Name  Output Driving Factor (Iu)  IN  36  Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I1C–E0  Sheet 1/1			Paramete	er .				Symbol	1	Typ (ns) *
Pin Name  Output Driving Factor (Iu)  IN  36  Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I1C–E0  Sheet 1/1										
Pin Name  Output Driving Factor (Iu)  IN  36  Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I1C–E0  Sheet 1/1										
Pin Name  Output Driving Factor (Iu)  IN  36  Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I1C–E0  Sheet 1/1										
Pin Name  Output Driving Factor (Iu)  IN  36  Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I1C–E0  Sheet 1/1		Innut Loading								
Pin Name    Sector (Iu)	Pin Name	Factor (lu)								
Pin Name    Sector (Iu)										
Pin Name    Sector (Iu)										
Pin Name    Sector (Iu)										
Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I1C–E0 Sheet 1/1	Din Name	Output Driving								
Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I1C–E0 Sheet 1/1										
C10–I1C–E0   Sheet 1/1		30	141111111111111	m values fo	r the typical	operating o	condition	1.		
					worst case	operating o	ondition	are given by	tne m	aximum oeiay
			L							
I Dago 24 40	C10-I1C-E0	Sheet 1/1								Page 21-19

P11117	CHICKOS CATE ADD	AVIDUT	CELLO	DECIFIC	ATION		1 " CG10	" Version
FUJIT: Cell Name	SU CMOS GATE ARR	AT UNIT	OELL SI	ECIFICA	TION		1 5610	Number of BC
I1CU	CMOS Interface with Pull-up Res	Input Busistance	uffer (Ir	nverter)				5
	Symbol			Prot	pagation D	elay Para	meter	
		tu			tc	in		Path
		t 0	KCL	·t0	KCL	KCL2	CDR2	
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		Paramete	<u> </u>		<u> </u>	Ц	Symbol	Typ (ns) *
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Pin Name	Input Loading Factor (lu)	ļ						
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	Output Driving	ļ				-		
Pin Name	Factor (Iu)	1						
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			m values for lues for the	uie typica: worst case	operating o	ondition a	re given by the	e maximum delay
		multiplie			_		•	-
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C10-I1CU-E0	Sheet 1/1							
								Page 21-20

	SU CMOS GATE ARF	RAY UNIT	CELL SI	PECIFICA	ATION		" CG10 "	
Cell Name	Function	Inni A D	h					Number of BC
I1CD	CMOS Interface with Pull-down	Input E	suπer (l	nverter)				5
	Symbol	11031314			pagation De	slav Paran	neter	
			qu		td	in		Path
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		0.600	0.017	0.100	0.017			X to IN
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		Paramete	er				Symbol	Typ (ns) *
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Pin Name	Input Loading Factor (lu)	Į					I	
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	Output Driving	1					j	
Pin Name	Factor (Iu)	ļ					-	
IN	36	<b> </b>					i	
			m values for				n aire - to -	. maybarran dele
	!	The val multiplie		worst case	operating c	undition are	e given by the	maximum delay
		L						HT-LL-CO-CO-CO-CO-CO-CO-CO-CO-CO-CO-CO-CO-CO-
C10-I1CD-E0	Sheet 1/1							
CIU-IICD-EU	SHEEL 1/1							Page 21-21
								rage 21-21

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL SI	PECIFICA	ATION		" CG10 "	
Cell Name	Function					····		Number of BC
I2C	CMOS Interface	Input B	uffer (T					4
Cell	Symbol			Pro	pagation D		eter	
			ıp			in		Path
		t 0	KCL	t 0	KCL	KCL2	CDR2	V4- 111
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		Paramete	L	l	<u> </u>	L	Symbol	Typ (ns) *
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Pin Name	Input Loading Factor (lu)	ļ						
riii Naine	ractor (tu)	1						
		l						
		ł					ŀ	
	Output Driving	1						
Pin Name	Factor (lu)	ļ					ł	
IN	36							
		* Minimu	m values fo	r the typical	l operating	condition.	-to book	
		multipli		worst case	operating c	ondition are	given by the	maximum delay
		mulapin	ы.					
C10-I2C-E0	Sheet 1/1							

FILIT	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG10" Version									
Cell Name	Function			LOFIC	ATION		1 00,0	Number of BC		
I2CU	CMOS Interface	Input B	uffer					4		
	with Pull-up Res	sistance	(True)							
Cell	Symbol		ıp.	Pro	pagation D	elay Paran In	neter			
		t O	KCL	t O	KCL	KCL2	CDR2	Path		
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	Input Loading						l			
Pin Name	Factor (lu)					}				
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	Output Driving						ŀ			
Pin Name	Factor (lu)						j			
IN	36						1			
		* Minimu	m values fo	r the typical	l operating	condition.	airea brithe	e maximum delay		
		multipli		WOISI Case	operating c	Ondition are	given by the	e maximum delay		
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C10-I2CU-E0	Sheet 1/1									
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FULITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION   **CG10** *Version   **Invalence of Bio	ELLUT	SU CMOS GATE ARE	AV LINIT	CELLS	PECIFIC	ATION		" CG10 "	Version
Call Symbol	Cell Name	Function	AT ONT	CELL SI	- ECIFICA	ATION		0070	
No			Input B	uffer	ıe)				
No   No   No   No   No   No   No   No	Cell	Symbol	100.010.	.00 (1	Proj	pagation D	elay Paran	neter	
Parameter  Parameter  Parameter  Symbol Typ (ns)  Pin Name Cutput Driving Factor (lu)  IN 36  Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						tc	dn		Path
Pin Name   Input Leading Factor (Iu)    Pin Name   Pactor (Iu)    Pin Name   Pactor (Iu)    IN   36   Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							KCL2	CDR2	
Pin Name Input Loading Factor (tu)  Pin Name Factor (tu)  IN 36  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2CD—E0 Sheet 1/1			0.575	0.017	0.831	0.023		1 1	X to IN
Pin Name Input Loading Factor (tu)  Pin Name Factor (tu)  IN 36  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2CD—E0 Sheet 1/1						l			
Pin Name Input Loading Factor (tu)  Pin Name Factor (tu)  IN 36  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2CD—E0 Sheet 1/1					'	1	1	1 1	
Pin Name Input Loading Factor (tu)  Pin Name Factor (tu)  IN 36  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2CD—E0 Sheet 1/1						l	l	1 1	
Pin Name Input Loading Factor (tu)  Pin Name Factor (tu)  IN 36  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2CD—E0 Sheet 1/1					'	1	l		
Pin Name Input Loading Factor (tu)  Pin Name Factor (tu)  IN 36  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2CD—E0 Sheet 1/1						j		1 1	
Pin Name Input Loading Factor (tu)  Pin Name Factor (tu)  IN 36  • Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2CD—E0 Sheet 1/1	_								
Pin Name   Input Loading Factor (Iu)    Pin Name   Output Driving Factor (Iu)    IN   36   Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.	x	>— IN					l	1 1	
Pin Name   Input Loading Factor (Iu)    Pin Name   Output Driving Factor (Iu)    IN   36   Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							1		
Pin Name   Input Loading Factor (Iu)    Pin Name   Output Driving Factor (Iu)    IN   36   Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							Ì		
Pin Name   Input Loading Factor (Iu)    Pin Name   Output Driving Factor (Iu)    IN   36   Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.						l	l	1 1	
Pin Name   Input Loading Factor (Iu)    Pin Name   Output Driving Factor (Iu)    IN   36   Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.							l		
Pin Name   Input Loading Factor (Iu)    Pin Name   Output Driving Factor (Iu)    IN   36   Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.			Paramete	¥	L	A	1	Symbol	Typ (ns) *
Pin Name  Cutput Driving Factor (Iu)  IN  36  Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2CD–E0  Sheet 1/1									
Pin Name  Cutput Driving Factor (Iu)  IN  36  Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2CD–E0  Sheet 1/1							i	1	
Pin Name  Cutput Driving Factor (Iu)  IN  36  Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2CD–E0  Sheet 1/1							1		
Pin Name  Cutput Driving Factor (Iu)  IN  36  Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2CD–E0  Sheet 1/1								1	
Pin Name  Cutput Driving Factor (Iu)  IN  36  Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2CD–E0  Sheet 1/1									
Pin Name  Cutput Driving Factor (Iu)  IN  36  Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2CD–E0  Sheet 1/1		· Input Loading						1	
Pin Name IN 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2CD–E0  Sheet 1/1	Pin Name	Factor (lu)							
Pin Name IN 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2CD–E0  Sheet 1/1								ļ	
Pin Name IN 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2CD–E0  Sheet 1/1									
Pin Name IN 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2CD–E0  Sheet 1/1								1	
Pin Name IN 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2CD–E0  Sheet 1/1								I	
Pin Name IN 36  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2CD–E0  Sheet 1/1		Output Debilar						l	
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  **C10–I2CD–E0   Sheet 1/1	Pin Name	Factor (lu)							
* Minimum values for the typical operating condition.  The values for the worst case operating condition are given by the maximum delay multiplier.  Which is a second sec			1					ļ	
The values for the worst case operating condition are given by the maximum delay multiplier.	liN .	36	Minimu	m values fo	r the typica	loperating	condition.		
C10–I2CD–E0   Sheet 1/1			The val	ues for the				e given by the	maximum delay
			multipli	er.					
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	C10 12CD 50	Choot 1/1							
	C10-12CD-E0	Sneet 1/1					-		Page 24 04

FILIT	SH CMOS GATE ARE	RRAY UNIT CELL SPECIFICATION "CG10" V							
Cell Name	Function Function	., . i O(41)	JELE SI	LOII IC/	711014		1 00,0		er of BC
I1S	Schmitt Trigger I (CMOS Type, In	nput Bu	ıffer					8	
	Symbol	1011017		Pro	pagation D	elav Para	meter		
		tı	ıp			in .	1	D	
		t 0	KCL	· t 0	KCL	KCL2	CDR2	Path	
		2.438	0.067	1.675	0.045		1 1	X to II	N
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×—	<i>0</i> — IN								
		Paramete	эт				Symbol	Typ (n	s) •
Di- Norman	Input Loading					l			
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Din Nama	Output Driving								
Pin Name	Factor (lu)								
IN	18	* Minimu	m values fo	e tha trais-1	l aparatia a	nondition.			····
					operating of operating c		re given by th	e maximum e	delav
		multiplie					- 2		,
		L							
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C10-I1S-E0	Sheet 1/1								
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FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG10" Vers									
	SU CMOS GATE ARE	RAY UNIT	CELL SI	PECIFICA	ATION		" CG10	" Version	
Cell Name	Function		.46-					Number of	. RC
I1SU	Schmitt Trigger I	nput Bu	iner	D	oloto			8	
	(CMOS Type, In	verter) V	with Pull	-nb we	SISIANCE	d ala:: *	ometer.		
Cell	Symbol	tu	,n 1	Prop	pagation D	<b>elay Par</b> dn	ameter T	·	
		10	KCL	t O	KCL	KCL2	CDR2	Path	
		2.438	0.067	1.675	0.045		<del>                                     </del>	X to IN	
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			m values for						
				worst case	operating c	ondition a	are given by th	e maximum delay	•
		multiplie	<b>ʊ</b> ſ.						
C10-I1SU-E0	Sheet 1/1				·			· · · · · · · · · · · · · · · · · · ·	
								Page 21-	26

EILIIT	• V6	ersion							
Cell Name	SU CMOS GATE ARE						1 00.0	ij	Number of BC
I1SD	Schmitt Trigger (CMOS Type, In	Input Bu	uffer		_				8
		verter)	with Pul	l-down	Resista	nce			J
Cel	l Symbol	<del> </del>		Proj	pagation D		meter		
		10	KCL	t O	KCL	n KCL2	CDR2	1	Path
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Pin Name	Input Loading Factor (lu)					- 1			
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	Output Driving	1							
Pin Name	Factor (lu)	}				İ		l	
IN	18							L	
			m values fo						الماماء مدينساند
		multipli		WOISI Case	operaung o	ondition at	re given by ii	re ma	ximum delay
	<u> </u>	<u> </u>							
C10-I1SD-E0	Sheet 1/1								
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FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG10 " Vers								Version
Cell Name	Function	MI UNII	OELL S	- EUIFIU	TION		0010	Number of BC
I2S	Schmitt Trigger I (CMOS Type, Tr	Input Bu	ıffer					8
	Symbol	ue)		Proi	pagation D	elav Param	eter	
			ıρ		to	ln		Path
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		Paramete	er				Symbol	Typ (ns) *
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	Input Loading						ı	
Pin Name	Factor (lu)							
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Pin Name	Output Driving Factor (lu)							
IN	18	* Minimu	m values fo	r the typical	operating	condition.		
		The val	ues for the	worst case	operating c	ondition are	given by the	maximum delay
		multipli	er.					
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								,
C10-I2S-E0	Sheet 1/1							
010-123-EU	JIICELI/I							Page 21–28

Cell Name   Function   Schmitt Trigger Input Buffer   (CMOS Type, True) with Pull-up Resistance   Schmitt Trigger Input Buffer   (CMOS Type, True) with Pull-up Resistance   Schmitt Trigger Input Buffer   Schmitt Tri	ELLIIT	SUCMOS GATE ARE	ZAV LINIT	CELLS	DECIEIC	MOLTA		" CG10	" Version
Schmitt Trigger Input Buffer (CMOS Type, True) with Pull—up Resistance   Schmitt Trigger True) with Pull—up Resistance   Schmitt True) with Pull—up Resistance   Schmitt Trigger True) with Pull—up Resistance   Schmitt True) with Pull—up Resistance   Schmitt True) with Pull—up Resistance   Schmitt True) with Pull—up Resistance   Schmitt True) with Pull—up Resistance   Schmitt True) with Pull—up Resistance   Schmitt True) with Pull—up Resistance   Schmitt True) with Pull—up Resistance   Schmitt True) with Pull—up Resistance   Schmitt True) with Pull—up Resistance   Schmitt True) with Pull—up Resistan	Cell Name	Function	TAT CITI	OLLL S	rECIFIC/	ATION		1 0070	Number of BC
Cell Symbol  To KCL 10 KCL KCL2 CDR2 Path  1.550 0.067 1.925 0.056 Symbol Typ (ns)?  Parameter Symbol Typ (ns)?  Parameter Symbol Typ (ns)?  Pin Name Pactor (tu)  IN 18  **Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10-12SU-E0 Sheet 1/1			Input Bu	ıffer					
No   NCL   10   NCL   COR2   Path   1.550   0.067   1.925   0.056   No   No   No   No   No   No   No   N		(CMOS Type, T	rue) with	n Pull–u	p Resis	tance			0
Plin Name    Output Driving Factor (tu)   Niminum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.    Niminum values for the worst case operating condition are given by the maximum delay multiplier.   Niminum values for the worst case operating condition are given by the maximum delay multiplier.   Niminum values for the worst case operating condition are given by the maximum delay multiplier.   Niminum values for the worst case operating condition are given by the maximum delay multiplier.   Niminum values for the worst case operating condition are given by the maximum delay multiplier.   Niminum values for the worst case operating condition are given by the maximum delay multiplier.   Niminum values for the worst case operating condition are given by the maximum delay multiplier.   Niminum values for the worst case operating condition are given by the maximum delay multiplier.   Niminum values for the worst case operating condition are given by the maximum delay multiplier.   Niminum values for the worst case operating condition are given by the maximum delay multiplier.   Niminum values for the worst case operating condition.   Niminum values for the worst case operating condition.   Niminum values for the worst case operating condition.   Niminum values for the worst case operating condition.   Niminum values for the worst case operating condition.   Niminum values for the worst case operating condition.   Niminum values for the worst case operating condition.   Niminum values for the worst case operating condition.   Niminum values for the worst case operating condition.   Niminum values for the worst case operating condition.   Niminum values for the worst case operating condition.   Niminum values for the worst case operating condition.   Niminum values for the worst case operating condition.   Niminum values for the worst case operating condition.   Niminum values for the worst case operating condition.   Niminum val	Cel	l Symbol	ļ		Pro			neter	
Plin Name   Input Loading   Pactor (Iu)    IN 18   Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.					••			CDB2	Path
Pin Name   Input Loading   Factor (Iu)    Pin Name   Factor (Iu)    IN							KOLZ	OBNZ	X to IN
Pin Name Input Loading Pin Name Pactor (Iu)  IN 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–12SU–E0 Sheet 1/1			1.550	0.007	1.323	0.050			X 10
Pin Name Input Loading Pin Name Pactor (Iu)  IN 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–12SU–E0 Sheet 1/1							1		
Pin Name Input Loading Pin Name Pactor (Iu)  IN 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–12SU–E0 Sheet 1/1			1						
Pin Name Input Loading Pin Name Pactor (Iu)  IN 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–12SU–E0 Sheet 1/1			l			i	l		
Pin Name Input Loading Pin Name Pactor (Iu)  IN 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–12SU–E0 Sheet 1/1									
Pin Name Input Loading Pin Name Pactor (Iu)  IN 18  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–12SU–E0 Sheet 1/1	1	<b>&gt;</b>	1						
Pin Name   Input Loading   Factor (Iu)    Pin Name   Output Driving   Factor (Iu)    IN	x—	IN	1	[		l	l		
Pin Name   Input Loading   Factor (Iu)    Pin Name   Output Driving   Factor (Iu)    IN							1		
Pin Name   Input Loading   Factor (Iu)    Pin Name   Output Driving   Factor (Iu)    IN			ł	1		}			
Pin Name   Input Loading   Factor (Iu)    Pin Name   Output Driving   Factor (Iu)    IN			1	l		l	ļ	l	
Pin Name   Input Loading   Factor (Iu)    Pin Name   Output Driving   Factor (Iu)    IN			Paramet	L	L	L	L	Symbol	Tyn (ne) *
Pin Name			1 aramet	<u> </u>				- Cyllidol	77P (113)
Pin Name			ļ						
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Pin Name Pin Name Pin Name Pin Name Pactor (Iu)  **Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  **C10–I2SU–E0   Sheet 1/1			1						
Pin Name  IN  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2SU–E0  Sheet 1/1	Pin Name	Factor (lu)	4						
Pin Name  IN  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2SU–E0  Sheet 1/1		1	1						
Pin Name  IN  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2SU–E0  Sheet 1/1			1						
Pin Name  IN  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2SU–E0  Sheet 1/1			ł						
Pin Name  IN  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  C10–I2SU–E0  Sheet 1/1			4				İ		
IN  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  **C10–I2SU–E0  Sheet 1/1	Pin Name		1				ļ		
* Minimum values for the typical operating condition.  The values for the worst case operating condition are given by the maximum delay multiplier.  **C10-I2SU-E0   Sheet 1/1			1						
C10–I2SU–E0   Sheet 1/1	II V	10	• Minimu	m values fo	r the typica	loperating	condition.		
C10-I2SU-E0   Sheet 1/1			The val	lues for the				given by the	ne maximum delay
			multipli	er.					
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I D 04 6	C10-I2SU-E0	Sheet 1/1							T =
Page 21–2									Page 21-29

CUUT	CHICKOS GATE ADD	ARRAY UNIT CELL SPECIFICATION " CG10" V						
Cell Name	Function Function	AT ONIT	CELL SI	ECIFICA	ATION		0070	Number of BC
I2SD	Schmitt Trigger I	nput Bu	iffer	own Do	oiotopo			8
	(CMOS Type, Tr	ue) witi	i Full—di	OWII Ne	pagation D	elev Peren		L
	i Syllibol	tu	10		to to		10101	
		t O	KCL	· t 0	KCL	KCL2	CDR2	Path
		1.550	0.067	1.925	0.056			X to IN
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		Paramete	<u> </u>		L	<u> </u>	Symbol	Typ (ns) *
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	Input Loading						1	
Pin Name	Factor (lu)						1	
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· ···	Output Driving							
Pin Name	Factor (lu)						1	
IN	18							
	,,,	* Minimu	m values fo	r the typical	operating of	condition.		
		The val	ues for the				given by the	maximum delay
		multiplie	er.					
	l	L						
C10-I2SD-E0	Sheet 1/1							
<u> </u>								Page 21–30

FUUT	CHICAGO CATE ADD	DAY LINUT	CELL C	DECITIO	ATION		* CG10	" Version	
Cell Name	SU CMOS GATE ARP	TAY UNIT	CELL SI	PECIFICA	ATION		<u> </u>	Number of BC	
	Schmitt Trigger	Input Bu	ıffer						
I1R	(TTL Type, Inve	rter)						8	
Cel	Symbol			Pro	pagation D		eter		
		1 0	KCL	t 0	KCL	ln KCL2	CDR2	Path	
		2.800	0.067	1.475	0.045	KOLZ	CORZ	X to IN	
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		Paramete	er				Symbol	Typ (ns) *	
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	Input Loading	1							
Pin Name	Factor (lu)	}				- 1			
		l				l			
	Output Driving								
Pin Name	Factor (lu)	ł				1			
IN	18								
					operating of				
		nultiplie		worst case	operating o	ondition are	given by th	e maximum delay	
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010 110 50	Charter 1								
C10-I1R-E0	Sheet 1/1							Page 21 21	
								Page 21-31	

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG10" Ver								" Version
Cell Name	Function							Number of BC
I1RU	Schmitt Trigger I (TTL Type, Inver	nput Buter) with	iffer n Pull–u	p Resis	tance			8
Cell	Symbol			Pro	pagation D		neter	
			ib			ln		Path
		t 0	KCL	t 0	KCL	KCL2	CDR2	
		2.800	0.067	1.475	0.045			X to IN
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Pin Name	Factor (lu)					ļ		
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	Output Driving	l				ŀ		
Pin Name	Factor (Iu)	ł				ı		
IN	18	• Minimu						L
		The val	m values to lues for the	r me typica worst case	l operating operating of	condition. ondition are	e given by th	e maximum delay
		multipli						•
<b></b>	<u> </u>	I						
C10-I1RU-E0	Sheet 1/1							
								Page 21-32

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL SI	PECIFICA		" CG10	" Version	
Cell Name	Function							Number of BC
I1RD	Schmitt Trigger I	Input Bu	ıffer					8
	(TTL Type, Inve	rter) with	n Pull–d					٥
Cell	Symbol			Proj	pagation D		meter	
			KCL	10	KCL	in KCL2	CDR2	Path
		t 0		1.475		KCL2	CDRZ	X to IN
		2.800	0.067	1.4/5	0.045			A 10 IIV
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		Paramete	l er			<del></del>	Symbol	Typ (ns) *
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	Input Loading	1				İ		
Pin Name	Factor (lu)	1						
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	Output Driving	}				- 1	İ	1
Pin Name	Factor (lu)	1				l		
IN	18	<del> </del>					i	
				r the typical			ro airean bu the	e maximum delay
		multiplie		WOISI Case	operating o	orioruori ai	e given by tre	maximum delay
C10-I1RD-E0	Sheet 1/1							
								Page 21-33

FUJIT	ITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG10" V									
Cell Name	Function							Number of BC		
I2R	Schmitt Trigger I (TTL Type, True	Input Bu )	ıffer					8		
Cell	Symbol			Proj	pagation D		ameter			
			JP			in		Path		
		t 0	KCL	t 0	KCL	KCL2	CDR2	X to IN		
		1.400	0.067	2.325	0.073			A to IN		
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		Paramete	96				Symbol	Typ (ns) *		
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	Input Loading									
Pin Name	Factor (lu)									
		ļ								
	Output Driving					- 1				
Pin Name	Factor (lu)	ļ								
IN	18	Minimu								
		14111111111	m values to ues for the	r the typical worst case	operating o	condition :	are given by th	e maximum delay		
		multipli					<b>3 3</b>	,		
	L	L								
C10-I2R-E0	Sheet 1/1									
								Page 21-34		

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG10 " Version												
Cell Name	Function	MY UNII	CELL SI	PECIFICA	ATION		LGIU	V	Number of BC			
	Schmitt Trigger	nput Bi	ıffer									
I2RU	Schmitt Trigger (TTL Type, True	) with P	ull–up F	Resistan	ce				8			
Cel	Symbol			Proj	pagation D	elay Paran	neter					
			ι <b>ρ</b>			in			Path			
		t O	KCL	· t 0	KCL	KCL2	CDR2					
		1.400	0.067	2.325	0.073				X to IN			
			1				1					
x	<i>D</i> IN											
		l					[ ]					
		Paramete	er	Symbol		Typ (ns) *						
		}				l						
Pin Name	Input Loading Factor (lu)					1						
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		l				1						
	Output Driving	1				1						
Pin Name	Factor (lu)					ı						
IN	18											
			m values fo						i			
		multipli		worst case	operating o	ondition ar	e given by th	e ma	aximum delay			
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C10-I2RU-E0	Sheet 1/1							Т	Deep 04 05			
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FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG10" Ver									
Cell Name	Function	AT UNIT	CELL SI	PECIFICA	ATION		<u> </u>	Number of BC	
		nnud Di						Number of BC	
I2RD	Schmitt Trigger I (TTL Type, True	nput bu	mer da	- Dania				8	
	(TTL Type, True	) Willi P	ull-uow	ii nesis	lance				
Cell	Symbol			Proj	pagation D		neter		
		t O	KCL	t O	KCL	In KCL2	CDR2	Path	
						NOLE	OBNZ	X to IN	
		1.400	0.067	2.325	0.073		1	Y 10 IIA	
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		Paramete	×			<u> </u>	Symbol	Typ (ns) *	
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	11					- 1	1		
Pin Name	Input Loading Factor (lu)					- 1			
	7 40101 (10)						1		
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						- 1			
	Output Driving					- 1			
Pin Name	Factor (lu)					- 1	i		
IN	18						L		
			m values fo						
				worst case	operating c	ondition are	given by the	maximum delay	
		multiplie	er.						
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C10-I2RD-E0	Sheet 1/1								
								Page 21-36	

	SU CMOS GATE AR	HAY UNIT	CELL S	PECIFICA	ATION		" CG10 "	
Cell Name	Function							Number of B
01B	Output Buffer (	IOL=3.2	mA, Inv	erter)				3
Ce	li Symbol			Pro	pagation De	elay Paran	neter	
			р		to			Path
		0.760	KCL 0.036	1.010	KCL 0.079	KCL2	CDR2	OT to X
от ——	x	(2.92)		(5.75)	0.079		Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)	-						
ОТ	2							
Pin Name	Output Driving Factor (lu)	-						
			ues for the		l operating o		e given by the	maximum delay

Note: 1. The unit of KCL is ns/pF.

- 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-O1B-E0 | Sheet 1/1

	THUTCH ON COATE ADDRAWN TO THE ODERS OF TOOL											
	SU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG10" Vers											
Cell Name		OI 0	A le					-	-	Number of BC		
O1BF	Output Buffer (I	UL=8m/	A, Inver							3		
Cell	Symbol	ļ		Proj	pagation D		ramet	er				
		t O	KCL	t O	KCL	n KCL2	2	CDR2		Path		
		0.850	0.036	0.980	0.039					OT to X		
		(3.01)		(3.32)			į					
1					·							
от	>×						-					
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		Paramete	97			$\dashv$	Syı	mbol		Typ (ns) *		
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	Input Loading											
Pin Name	Factor (lu)											
ОТ	2											
Di- N	Output Driving											
Pin Name	Factor (lu)					1						
			m values fo									
		The val		worst case	operating c	ondition	are gi	iven by th	e ma	ximum delay		
	L	morapii	<del> </del>									
Note: 1. The	e unit of KcL is ns/pF.											
2. Ou	tput load capacitance	of 60 pF	is used fo	r Fujitsu':	s logic sir	nulatio	n.					
3. The	e parameters in paren	theses ar	e the valu	ies applie	ed to the s	simulat	tion.					
C10_O1BE_E0	Sheet 1/1											

FILIIT	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG10 " Version											
Cell Name	Function	IAT OIVIT	OLLL O	LONIO	111011					Number of BC		
O1L	Power Output Bu	uffer (IC	)L=12m	A, Inve	rter)					3		
Cell	Symbol			Proj	pagation D	elay Pa	ram	eter				
		t.				in				Path		
		t O	KCL	10	KCL	KCL	2	CDR2				
от —	<b>&gt;</b> 0—×	0.870 (2.31)	0.024	1.100 (2.66)	0.026					OT to X		
		Paramete	arameter Symbol Ty									
Pin Name	Input Loading Factor (lu)											
ТО	2											
Pin Name	Output Driving Factor (iu)					Ì						
			ues for the	r the typical worst case				given by the	e ma	ximum delay		
2. Ou	e unit of KCL is ns/pF.  put load capacitance of parameters in parent											

C10-O1L-E0

Sheet 1/1

	011 01100 0175 155				. = . 0		" CG10	* > / '
FUJII	SU CMOS GATE ARE	AY UNI	CELL S	PECIFICA	ATION		] " CG10	" Version
Cell Name	Function	01 00	A I	\				Number of BC
01R	Output Buffer (Id	JL=3.21	mA, inv	ener)				5
	with Noise Limit	Hesista	nce					
Cell	Symbol			Pro	pagation D		ameter	
			ib			in		Path
		t O	KÇL	t O	KCL	KCL2	CDR2	OT 1. V
		1.770	0.036	4 310	0.080		1 1	OT to X
		(3.93)		(9.11)		1	] ]	
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		Paramete	er				Symbol	Typ (ns) *
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	Input Loading					- 1	1	
Pin Name	Factor (lu)					- 1		
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<u> </u>	Output Driving	1				- 1		
Pin Name	Factor (lu)	}				l		
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		Minimu	m values fo	r the typical	loperating	condition	1.	
								e maximum delay
		multipli	er.					
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Note: 1. Th	e unit of KCL is ns/pF.							
1	•				-  !'-	mulati-	_	
	tput load capacitance							
3. Th	e parameters in paren	theses ar	e the valu	ies applie	ed to the	simulat	ion.	
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C10-O1R-E0	Sheet 1/1							
								Page 21-40

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG10" Version										ersion
Cell Name	Function									Number of BC
O1RF	Output Buffer (I with Noise Limit	OL=8m/ Resista	A, Inver	ter)						5
Cell	Symbol			Proj	pagation D	elay Pa	rame	eter		
			ıр		tc	in				Path
		t 0	KCL	t O	KCL	KCL	2	CDR2		
		1.824	0.036	5.013	0.044	1	- 1	1		OT to X
		(3.99)		(7.66)		١	١			
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		Paramete	er e				S	ymbol		Typ (ns) *
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	Input Loading									
Pin Name	Factor (lu)	l				]			ĺ	
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	Output Driving					- 1			1	
Pin Name	Factor (lu)								1	
		<u> </u>							Ц	
				r the typical				aiuaa bu th		aximum delay
		multiplie		WOISI Case	operating c	Official	are	given by in	e m	aximum delay
Note: 1 Th	unit of Koulia no/-F									
	e unit of KCL is ns/pF.									
2. Ou	tput load capacitance	of 60 pF i	s used fo	r Fujitsu's	s logic sir	nulatio	n.			
3. The	e parameters in parent	heses are	e the valu	es applie	d to the	simula	tion			
	·			• •						
C10-O1RF-E0	Sheet 1/1									
									- 1	Page 21-41

FILIIT	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION "CG10" Version										
Cell Name	Function	IAT UNIT	JLLL OI	LOII IO	111011			Number of BC			
015	Power Output Br			A, Inve	rter)			5			
Cell	Symbol			Prop	pagation D	elay Param	eter				
			ip			ln	2222	Path			
		t 0	KCL	t 0	KCL	KCL2	CDR2	OT to X			
		1.992 (3.44)	0.024	5.660 (7.70)	0.034			01.00			
		(5.77)		(7.70)							
1											
от —	>>—×										
L							1				
							]				
1											
					<u> </u>	L	L				
		Paramete	97				Symbol	Typ (ns) *			
						l					
						l					
	Input Loading						1				
Pin Name	Factor (lu)					İ	- 1				
ОТ	1					İ					
						1					
							Ì				
Pin Name	Output Driving Factor (lu)					l					
7 III Namo	1 80:01 (10)										
		Minimu	m values fo	r the typical	operating	condition.					
		The val	ues for the				given by the	e maximum delay			
		multipli	er.								
		<u> </u>					***************************************				
	e unit of KCL is ns/pF.										
2. Ou	tput load capacitance	of 60 pF i	is used fo	r Fujitsu's	s logic sir	nulation.					
3. The	e parameters in parent	heses ar	e the valu	ies applie	d to the	simulation	٦.				
	•										
C10-O1S-E0	Sheet 1/1										
								Page 21_42			

Cell Symbol  Cell	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG10 " Version											
Parameter    Note: 1. The unit of KCL is ns/pF.   2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.   3. The parameters in parentheses are the values applied to the simulation.   2. Call   2								·	Number of BC			
Parameter    Note: 1. The unit of KCL is ns/pF. 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.	O2B	Output Buffer (I	OL=3.2	mA, Tru	e)				2			
Plin Name  Input Loading Factor (tu)  Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Note: 1. The unit of KcL is ns/pF. 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation.	Cel	l Symbol			Pro			neter				
Parameter  Parameter  Parameter  Symbol Typ (ne)*  Pin Name Factor (tu)  OT 6  Input Loading Factor (tu)  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Note: 1. The unit of KcL is ns/pF.  2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.  3. The parameters in parentheses are the values applied to the simulation.					10			CDB2	Path			
Plin Name Input Loading Factor (tu) OT 6  Pin Name Parameter Symbol Typ (ns)*  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Note: 1. The unit of KcL is ns/pF. 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation.	1		0.500		0.803				OT to X			
Pin Name  OT  6  Pin Name  Output Driving Factor (tu)  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Note: 1. The unit of KCL is ns/pF. 2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation. 3. The parameters in parentheses are the values applied to the simulation.	от —	×	Paramete				Symbol	Typ (ns) *				
Pin Name  Output Driving Factor (Iu)  * Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Note: 1. The unit of KcL is ns/pF.  2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.  3. The parameters in parentheses are the values applied to the simulation.	Pin Name											
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.  Note: 1. The unit of KcL is ns/pF.  2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.  3. The parameters in parentheses are the values applied to the simulation.	ОТ	6										
Note: 1. The unit of KcL is ns/pF.  2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.  3. The parameters in parentheses are the values applied to the simulation.	Pin Name	Output Driving Factor (lu)										
Output load capacitance of 60 pF is used for Fujitsu's logic simulation.     The parameters in parentheses are the values applied to the simulation.			The val	ues for the				e given by the	e maximum delay			
C10O2BE0   Sheet 1/1	Note: 1. The unit of KcL is ns/pF.  2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.  3. The parameters in parentheses are the values applied to the simulation.											
	C10-O2B-E0	Sheet 1/1							Page 21–43			

	SU CMOS GATE ARP	RAY UNIT	" CG10 " V					
Cell Name	Function							Number of BC
O2BF	Output Buffer (IC	DL=8mA	A, True)					2
Cell	Symbol			Pro	pagation D		neter	
			ip			in		Path
		t O	KCL	t 0	KCL	KCL2	CDR2	
		0.590 (2.75)	0.036	0.773 (3.12)	0.039			OT to X
от	<b>&gt;</b> x							
		Paramete	×				Symbol	Typ (ns) *
Pin Name	Input Loading Factor (Iu)							
ОТ	6							
Pin Name	Output Driving Factor (iu)							
			ues for the		operating o		e given by the m	aximum delay
l	e unit of KCL is ns/pF.							
	tput load capacitance of e parameters in parent	•			-		n.	

C10-O2BF-E0 | Sheet 1/1

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELL SI	PECIFICA	NOITA		" CG10	"Ve	rsion
Cell Name	Function							$\dashv$	Number of BC
O2L	Power Output B	uffer (10	DL=12m						2
Cell	Symbol			Pro	pagation D		eter		
		t O	KCL	·t0	KCL	n KCL2	CDR2		Path
		0.610	0.024	0.893	0.026	NOL	ODINE		OT to X
		(2.05)	0.024	(2.46)	0.020				C. 10 A
		, ,		` '					
]									
				<b>'</b>		1	1		
от	x			}					
						1	1		
				(		1			
		Paramete	97				Symbol		Typ (ns) *
						ļ			
	Input Loading								
Pin Name	Factor (lu)					- 1			
ОТ	6					ļ			
						-			
						l			
	Output Driving					- 1			
Pin Name	Factor (lu)								
								<u> </u>	
				r the typical			aiven hy th	e ma	ximum delay
		multipli		Worst Gase	operating o	onarion ar	given by an		Aimoni dolay
	L	L							
Note: 1. The	e unit of KcL is ns/pF.								
2. Ou	tput load capacitance	of 60 pF i	is used fo	r Fujitsu':	s logic sir	nulation.			
3. Th	e parameters in parent	heses ar	e the valu	es applie	d to the	simulation	٦.		
	•			• • •					
1									
1									
C10-O2L-E0	Sheet 1/1								

CUUT	CHICHOC CATE ADD	AV LINIT	CELLS	DECIFIC	ATION		" CG10 "	Vorcion
Cell Name	SU CMOS GATE ARE	AT UNI	CELLS	reciric/	ATION		<u> </u>	Number of BC
O2R	Output Buffer (I	OL=3.2	mA, Tru	e)				4
	with Noise Limit	Hesista	ince			-1 D		
Cei	ТЭУПОО	<u> </u>	dr dr	Proj	pagation D	dn Paran	1eter	
		t O	KCL	t O	KCL	KCL2	CDR2	Path
от —	x	1.383 (3.55)	0.036	3.335 (8.14)	0.080			OT to X
		Paramete	L	L	L	<del>'                                    </del>	Symbol	Typ (ns) *
Pin Name	Input Loading Factor (lu)						l	
ОТ	2							
Pin Name	Output Driving Factor (lu)		na anggala panaka					
		Minimu     The val     multipli	ues for the	r the typical worst case	operating operating o	condition. ondition are	given by the	maximum delay
2. Ou	e unit of KcL is ns/pF. tput load capacitance of e parameters in parent						n.	
C10-O2R-E0	Sheet 1/1							Page 21-46

				550.50			T# 0046	
FUJIT Cell Name	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFIC	ATION		* CG10	Number of BC
	Output Buffer (I	$\Omega I = 8mA$	True					
<i>02RF</i>	with Noise Limit	Resista	ince					4
Cell	Symbol	I		Pro	pagation D	elay Pa	rameter	
			ıb dı			n		Path
		t O	KCL	10	KCL	KCL	2 CDR2	
		1.437	0.036	4.038	0.044	l		OT to X
		(3.60)		(6.68)				
1					1			
			1					
			1	l	Ì	Ì		
/				1		ł		
от —	>×							
				1				
			ļ	l		ļ		
						İ		
			<u> </u>	<u> </u>	<u> </u>	١		<del> </del>
		Paramete	er			-+	Symbol	Typ (ns) *
						1		
						- [		
	Input Loading	1				1		
Pin Name	Factor (lu)	]				l		į
ОТ	2							
						1		
						ŀ		
		1				1		
Pin Name	Output Driving Factor (lu)					1		
		İ				İ		
		Minimus	m values fo	r the typical	operating	conditio	n.	
		The val	ues for the					he maximum delay
		multiplie	er.					
		<b>L</b>						
Material Th								
	unit of KcL is ns/pF.							
2. Ou	tput load capacitance	of 60 pF i	s used fo	r Fujitsu's	s logic sin	nulatio	on.	
3. The	e parameters in paren	theses are	e the valu	ies applie	d to the s	simula	tion.	

C10-O2RF-E0 | Sheet 1/1

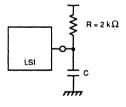
FUJIT	SU CMOS GATE ARF	RAY UNIT	CELL S	PECIFICA	ATION		" CG10 "	Version
Cell Name	Function							Number of BC
025	Power Output Bowith Noise Limit	uffer (IC	DL=12m	A, True	)			4
Call	Symbol Symbol	nesisia	lice	Droi	pagation D	elay Paran		<u></u>
	- Cyllidor	tı	ıb	1 710,		dn	1	·
		t O	KCL	t O	KCL	KCL2	CDR2	Path
от —	x	1.605 (3.05)	0.024	4.685 (6.73)	0.034			OT to X
		Paramete	86				Symbol	Typ (ns) *
Pin Name OT Pin Name	Input Loading Factor (lu)  2  Output Driving Factor (lu)							
			lues for the	or the typica worst case			e given by the	maximum delay
2. Ou	e unit of KCL is ns/pF. tput load capacitance e parameters in paren	of 60 pF					n.	

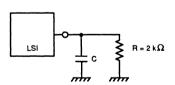
Page 21-48

C10-O2S-E0

Sheet 1/1

FUJI	TSU CMOS GATE AF	RAY UNIT	CELL	SPECIFIC.	ATION		" CG10	* Version
Cell Name	Function							Number of B0
O4T	Tri-state Outpu	ıt Buffer	(IOL=	3.2mA, T	rue)			4
Ce	ell Symbol	T		Pro	pagation D	elay Pa	rameter	
		t	ηþ			in		Path
		t O	KCL	t O	KCL	KCL	2 CDR2	
от	×	0.639 (2.98)	0.036	1.460 (6.66)	0.080			OT to X
·	c	10	L to	Z KCL	to	Z to	KCL KCL	C to X
		1.78 (13.9		•	1.17 (6.57		0.083	
Pin Name	Input Loading Factor (lu)							
οτ	6 2							
С	2	10	H to	KCL	10	Z to	KCL	
		2.12	<del>,  </del>	NOL	0.70	$\overline{}$	0.037	
Pin Name	Output Driving Factor (lu)	(13.9		•	(6.57		0.037	





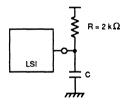
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

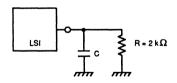
Note: 1. The unit of KCL is ns/pF.

- 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-O4T-E0 | Sheet 1/1

FUJIT	<u>ISU CMOS GATE AR</u>	RAY UNIT	CELL S	PECIFIC	ATION		" CG10	" Version
Cell Name	Function							Number of B
O4TF	Tri-state Outp	ut Buffer	(IOL=8	mA, Tru	ıe)			4
Ce	II Symbol			Pro	pagation D	elay Para	meter	
			dr.		to			Path
		10	KCL	· t 0	KCL	KCL2	CDR2	
от ——	×	0.693	0.036	(5.21)	0.044			OT to X
	c	10	L to Z	KCL	tO	ZtoL	KCL	C to X
		2.14 (15.6		•	1.57! (4.44		0.044	
Pin Name	Input Loading Factor (lu)							
от	6 2							
С	2	10	H to Z	KCL	10	Z to H	KCL	
		<u> </u>	<del></del>	NOL	<del> </del>	<del>- +</del>		
Pin Name	Output Driving Factor (lu)	2.12 (15.6		•	0.70 (4.44		0.037	





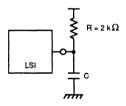
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

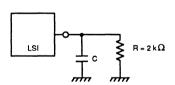
Note: 1. The unit of KCL is ns/pF.

- 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-O4TF-E0 Sheet 1/1

FUJIT	ISU CMOS GATE AR	RAY UNIT	CELL S	PECIFIC.	ATION		" CG10 '	
Cell Name	Function							Number of B
04W	Power Tri-state	Output	Buffer	(IOL=12	2mA, Tn	ne)		4
Ce	II Symbol			Pro	pagation D	elay Para	meter	
		tu				in		Path
		t O	KCL	t O	KCL	KCL2	CDR2	
от —	×	0.804 (2.37)	0.024	2.620 (4.83)	0.034			OT to X
			L to Z	L		Z to L		
		t 0		KCL	t O		KCL	C to X
		2.566 (16.44		•	1.219 (4.60		0.052	
Pin Name	Input Loading Factor (Iu)							
OT	6 2							
С	2	10	H to Z	KCL	10	Z to H	KCL	
				NOL				
Pin Name	Output Driving Factor (Iu)	2.544 (16.44		•	0.80 (4.60		0.025	





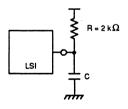
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

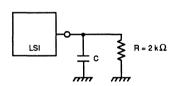
Note: 1. The unit of KCL is ns/pF.

- 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-O4W-E0 | Sheet 1/1

FUJIT	SU CMOS GATE AR	RAY UNIT	CELL S	PECIFIC	ATION		" CG10	" Version
Cell Name	Function							Number of BC
O4R	Tri-state Outpu with Noise Limi			.2mA, T	rue)			5
Cel	I Symbol	T		Pro	pagation D	elay Par	ameter	
			ıp			in		Path
		t O	KCL	10	KCL	KCL2	CDR2	
		1.177 (3.52)	0.036	3.190 (8.39)	0.080			OT to X
от	x							
			L to Z			Z to		<b>a</b>
		10		KCL	t O		KCL	C to X
		1.73		٠	3.57 (8.97		0.083	
Pin Name	input Loading Factor (lu)							
οT	2 2	<u> </u>			ļ			
С	2	10	H to Z	KCL	to	Z to	H KCL	
			<del>.  </del>	NOL	<del> </del>	$\overline{}$	0.037	
Pin Name	Output Driving Factor (lu)	1.86		•	1.30 (8.97		0.037	





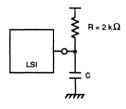
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

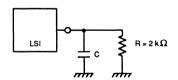
Note: 1. The unit of KCL is ns/pF.

- 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-O4R-E0 | Sheet 1/1

FUJIT	SU CMOS GATE AR	RAY UNIT	CELL S	PECIFICA	ATION		" CG10 "	' Version
Cell Name	Function							Number of B
O4RF	Tri-state Outp with Noise Lim	ut Buffer it Resista	(IOL=8 ance	mA, Tru	ie)			5
Ce	II Symbol	T		Pro	pagation D	elay Paras	meter	
		tu	P		tdn			Path
		t O	KCL	10	KCL	KCL2	CDR2	Pam
от ——	×	1.231 (3.57)	0.036	4.073 (6.94)	0.044			OT to X
	С		L to Z			Z to L		
		10		KCL	10		KCL	C to X
		2.24 (15.6		•	3.98 (6.84		0.044	
Pin Name	Input Loading Factor (lu)							
ОТ	2 2							
С	2	10	H to Z	KCL	10	Z to H	KCL	
				NUL	<del> </del>			
Pin Name	Output Driving Factor (lu)	1.860		•	1.30 (6.84		0.037	





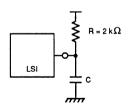
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

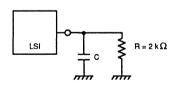
Note: 1. The unit of KCL is ns/pF.

- 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-O4RF-E0 Sheet 1/1

FUJI	TSU CMOS GATE AR	RAY UNIT	CELL S	PECIFICA	ATION		" CG10	" Version
Cell Name	Function							Number of BC
<i>04S</i>	Power Tri-state with Noise Limi	Output t Resista	Buffer ince	(IOL=12	2mA, Tn	ne)		5
Ce	eli Symbol	T		Pro	pagation D	elay Para	ameter	
	**************************************	tı	JP	T		in		D-45
		t O	KCL	t O	KCL	KCL2	CDR2	Path
от	×	1.477 (3.04)	0.024	4.770 (6.98)	0.034			OT to X
			L to Z	1		Z to l		***************************************
		t 0		KCL	t 0		KCL	C to X
		2.600 (16.3		•	3.75 (7.14		0.052	
Pin Name	Input Loading Factor (Iu)	]						
OT	2 2	<u> </u>					i	
С	2	10	H to Z	KCL	10	Z to F	KCL	
				NOL				
Pin Name	Output Driving Factor (lu)	(16.3		•	1.40 (7.14		0.025	





- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of KCL is ns/pF.

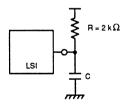
- 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

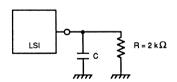
C10-O4S-E0 | Sheet 1/1

6 Path to X
ath
to X
(ns) *
m delay

C10-O2S2-E0 | Sheet 1/1

	SU CMOS GATE AR	MAY UNII	UELL S	FECIFICA	AHON		1 0010	" Version
Cell Name	Function		5 "	//OL 0.4				Number of B
<i>O4S2</i>	Power Tri-stat with Noise Lim	e Output it Resist	Buffer	(IOL=24	·mA, Iru	ne)		7
Cel	Symbol	T		Proj	pagation D	elay Par	emeter	
		tı	ıρ		to	In		Path
		t O	KCL	t O	KCL	KCL2	CDR2	
от ——	×	3.050 (4.16)	0.017	10.400 (12.81)	0.037			OT to X
	C		L to Z			Z to		
		10		KCL	t O		KCL	C to X
		4.80 (18.5		•	9.00: (11.6		0.041	
Pin Name	Input Loading Factor (iu)							
от	2 2				ļ			
С	2	10	H to Z	KCL	t O	Z to	KCL	
			_  -	NOL				
Pin Name	Output Driving Factor (lu)	3.62 (18.5		•	2.00 (11.6		0.020	





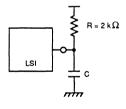
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

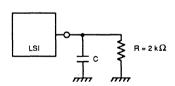
Note: 1. The unit of KCL is ns/pF.

- 2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-O4S2-E0 | Sheet 1/1

FUJI	TSU CMOS GATE AR	RAY UNIT	CELLS	PECIFICA	ATION		" CG10	" Version
Cell Name	Function							Number of BO
H6T	Tri-state Outpu	it & Input	Buffer	(IOL=3	.2mA, T	rue)		8
Ce	Il Symbol			Pro	pagation D		meter	
			р		to			Path
		t O	KCL	10	KCL	KCL2	CDR2	
		0.663	0.017	1.150	0.023		1	X to IN
		(3.70)	0.036	1.460 (8.26)	0.080			OT to X
		(3.70)		(0.20)			1	
	/	1						
IN —	<b>-</b> <h< td=""><td></td><td></td><td>1</td><td> </td><td></td><td>   </td><td></td></h<>			1				
	N 1							
OT	-			į.	ļ I		1	
	M			1	1			
		1	l		ļ		1 1	
	C	<u> </u>	L to Z	1		Z to L		
		t O		KCL	t O		KCL	C to X
		1.78			1.17	0	0.083	
		(17.7	2)		(8.23	()		
	Input Loading	1						
Pin Name	Factor (lu)	4						
OT C	6 2	<b></b>	H to Z		-	Z to H		
·	_	10	1	KCL	10	T	KCL	
		2.12	0		0.70	0	0.037	
Pin Name	Output Driving Factor (lu)	(17.7		-	(8.23			
IN	36					1		
	1	1	1		1	1	ì	





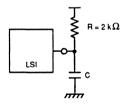
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

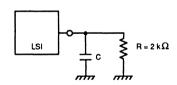
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H6T-E0	Sheet 1/1

FUJI	ISU CMOS GATE AR	RAY UNIT	CELL	SPECIFICA	ATION		" CG10	" Version		
Cell Name	Function							Number of B		
H6TU	Tri-state Outpu with Pull-up Re			r (IOL=3	.2mA, T	rue)		8		
Ce	Cell Symbol Propagation Delay Parameter									
		tı	ip		to	n		Path		
		t O	KCL	t O	KCL	KCL2	CDR2	ram		
		0.663 0.639 (3.70)	0.017 0.036		0.023 0.080			X to IN OT to X		
IN	×		L to			Z to L				
		10	- 10	KCL	10	_ <u></u>	KCL	C to X		
		1.78 (17.72		•	1.17 (8.23		0.083			
Pin Name	Input Loading Factor (Iu)									
οτ	6 2	ļ	H to			Z to H				
С	2	10	H 10	KCL	10		KCL			
		2.12	<u>,                                    </u>		0.70		0.037			
Pin Name	Output Driving Factor (lu)	(17.72		•	(8.23		0.037			
IN	36									





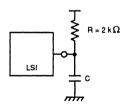
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

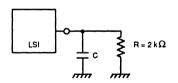
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H6TU-E0 | Sheet 1/1

FUJIT	SU CMOS GATE ARI	TINU YAS	CELLS	PECIFICA	ATION		" CG10	" Version
Cell Name	Function							Number of BC
H6TD	Tri-state Output with Pull-down			(IOL=3	.2mA, T	rue)		8
Ce	ll Symbol			Pro	pagation D	elay Para	meter	
			ıp			dn		Path
		10	KCL	10	KCL	KCL2	CDR2	
in			0.017 0.036	1.150 1.460 (8.26)	0.023 0.080			X to IN OT to X
	C	10	L to Z	KCL	10	Z to L	KCL	C to X
		1.78		*	1.170	,	0.083	0.10 X
Pin Name	Input Loading Factor (lu)							
ОТ	6							
С	2	H to Z Z to H						
		10		KCL	t 0		KCL	
Pin Name	Output Driving Factor (lu)	2.120 (17.72		•	0.700 (8.23)		0.037	
IN	36							





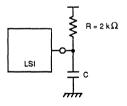
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

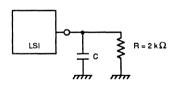
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H6TD-E0 Sheet 1/1

	TSU CMOS GATE AR	RAY UNIT	CELL	SPECIFIC.	ATION		" CG10	" Version
Cell Name	Function							Number of B
H6TF	Tri-state Outp	ut & Inpu	it Buffe	er (IOL=8	mA, Tr	ie)		8
Ce	II Symbol			Pro	pagation D	elay Pa	rameter	
			ıp qı			dn		Path
		0.663	KCL	10	KCL	KCL	2 CDR2	
			0.017 0.036		0.023 0.044			X to IN OT to X
от	×							
	· ·		L to	z		Z to	L	The second of th
		t O		KCL	t O		KCL	C to X
		2.14 (19.8		*	1.57 (5.32		0.044	
Pin Name	Input Loading Factor (lu)					j		
OT C	6 2		H to	7	<del> </del>	I	<u>.</u>	
Ü	1	10		KCL	10		KCL	
		2.12	2		0.70	0	0.037	
Pin Name	Output Driving Factor (lu)	(19.8		•	(5.32		5.507	
IN	36							

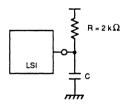


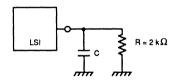


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C10-H6TF-E0 Sheet 1/1

FUJIT	SU CMOS GATE AR	RAY UNIT	CELL	SPECIFIC	ATION		" CG10	" Version
Cell Name	Function							Number of B
H6TFU	Tri-state Outpo with Pull-up R			er (IOL=8	mA, Tr	ie)		8
Cell	Symbol			Pro	pagation D	elay Par	ameter	
		tup tdn						Path
		t 0	KCL	10	KCL	KCL2	CDR2	raui
OT X		0.663 0.693 (3.76)	0.017 0.036		0.023 0.044			X to IN OT to X
	Ü		L to			Z to		
		10		KCL	10		KCL	C to X
		2.14 (19.8		•	1.57 (5.32		0.044	
Pin Name	Input Loading Factor (lu)		}					
OT C	6 2		H to	7	<del> </del>	Z to	<del></del>	
Ŭ	_	10		KCL	t O		KCL	
		2.12	n		0.70		0.037	
Pin Name	Output Driving Factor (lu)	(19.8		•	(5.32		0.007	
IN	36							





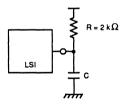
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

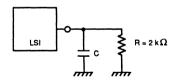
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H6TFU-E0 Sheet 1/1

	SU CMOS GATE AR	" Version						
Cell Name	Function							Number of B
H6TFD	Tri-state Outpour	ut & Inpu i Resista	it Buffe ince	r (IOL=8	mA, Tr	ie)		8
Ce	I Symbol	T		Pro	pagation D	elay Para	ameter	
		tı	ıp qı		to	in		Path
		t O	KCL	· t 0	KCL	KCL2	CDR2	raui
IN X		0.663 0.693 (3.76)	0.017 0.036	1.150 2.343 (6.09)	0.023 0.044			X to IN OT to X
	С		L to Z		<del> </del>	Z to I		
		t O		KCL	t O		KCL	C to X
		2.14 (19.8		•	1.57 (5.32		0.044	
Pin Name	Input Loading Factor (Iu)	]				İ		
οŢ	6 2	<u></u>	H to 2		<b> </b>	Z to H		
С	2	10	H 10 4	KCL	10		KCL	
		<del></del>		NOL	<del> </del>			
Pin Name	Output Driving Factor (lu)	2.12 (19.8		•	0.70 (5.32		0.037	
IN	36	1						

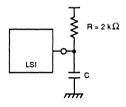


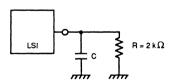


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KcL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C10-H6TFD-E0 Sheet 1/1

	TSU CMOS GATE AR	RAY UNIT	CELL S	PECIFIC	ATION		" CG10	" Version
Cell Name	Function							Number of BC
H6W	Power Tri-state	Output	& Input	Buffer	(IOL=12	2mA, T	rue)	8
Ce	ell Symbol							
			р			in		Path
		10 KCL 0.663 0.017		10	KCL	KCL2	CDR2	V. 91
	OT X		0.017 0.024	1.150 2.620 (5.51)	0.023 0.034			X to IN OT to X
	С		L to Z			Z to L		
		t O		KCL	t O		KCL	C to X
		2.560 (20.7		•	1.219 (5.64		0.052	
Pin Name	Input Loading Factor (lu)						i	
οT	6 2	ļ	H to Z		ļ	Z to H		
С	2	10	H 10 Z	KCL	10	210 H	KCL	
		2.540	$\overline{}$		0.80	<u>,                                    </u>	0.025	
Pin Name	Output Driving Factor (lu)	(20.7		•	(5.64		0.025	
IN	36							





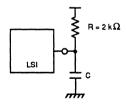
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

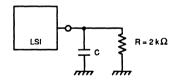
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H6W-E0 | Sheet 1/1

FUJIT	SU CMOS GATE ARI	RAY UNIT	CELL	SPECIFIC.	ATION		" CG10	" Version
Cell Name	Function							Number of BC
H6WU	Power Tri-state with Pull-up Re	Output sistance	& Inp	ut Buffer	(IOL=12	2mA,	True)	8
Cell	Symbol			Pro	pagation D	elay Pa	rameter	
			ıp qı			tdn		Path
		10	KCL	t O	KCL	KCL	2 CDR2	
or x		0.663 0.804 (2.85)	0.017 0.024		0.023			X to IN OT to X
	C	10	L to	Z KCL	10	Z to	KCL KCL	C to X
		2.56 (20.7		•	1.21 (5.64		0.052	
Pin Name	input Loading Factor (lu)							
OT	6 2	<b> </b>	H to	7	<b> </b>	Z to	. U	
С	4	10		KCL	10		KCL	
			<del>,  </del>	- NOL	0.80		0.025	
Pin Name	Output Driving Factor (lu)	2.54 (20.7		•	(5.64		0.025	
IN	36							





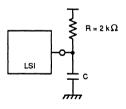
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

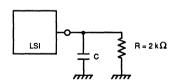
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H6WU-E0 | Sheet 1/1

FUJIT	SU CMOS GATE ARI	RAY UNIT	CELL S	PECIFICA	ATION		" CG10	" Version
Cell Name	Function							Number of BC
H6WD	Power Tri-state with Pull-down	Output Resistar	& Input	Buffer	(IOL=12	2mA, T	rue)	8
Cell	Symbol			Pro	pagation D	olay Para	meter	
			JP .	ļ	to			Path
		10	KCL	10	KCL	KCL2	CDR2	
		0.663 0.804 (2.85)	0.017 0.024	1.150 2.620 (5.51)	0.023 0.034			X to IN OT to X
ot								
	C		L to Z	KCL		Z to L	KCL	04- 7
		2.566 (20.7		*	1.21 (5.64		0.052	C to X
Pin Name	Input Loading Factor (lu)	1						
OT C	6 2	ļ	H to Z			Z to H		
C	2	10	7 10 2	KCL	10	210 11	KCL	
		2.54			0.80	<del>,  </del>	0.025	
Pin Name	Output Driving Factor (lu)	(20.7		•	(5.64		0.023	
IN	36							





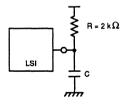
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

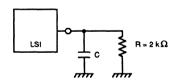
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H6WD-E0 | Sheet 1/1

FUJII	SU CMOS GATE AR	RAY UNIT	CELI	L SF	PECIFICA	ATION			" CG10 "	
Cell Name	Function									Number of B
H6C	Tri–state Outpi True)	ut & CMC	OS In	ter	face Inp	ut Buffe	er (IC	DL=	3.2mA,	8
Cel	Symbol				Prop	agation De	elay Pa	rame	ter	
		tup tdn							Path	
		t 0	KCI	L	t O	KCL	KCL	2	CDR2	Path
от х		0.575 0.639 (3.70)	0.01 0.03		0.831 1.460 (8.26)	0.023 0.080				X to IN OT to X
	С		Lto	٥Z			Z to			
		t 0			KCL	10			KCL	C to X
		1.780 (17.72			•	1.170 (8.23)		0	0.083	
Pin Name	Input Loading Factor (lu)									
OΤ	6 2									
С	2	10	н 1	o Z	KCL	t O	Z to		KCL	
					KCL					
Pin Name	Output Driving Factor (lu)	2.120 (17.72			•	0.700 (8.23)		U	0.037	
IN	36									

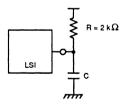


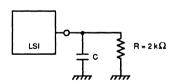


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C10-H6C-E0 | Sheet 1/1

	<u>TSU CMOS GATE AR</u>	RAY UNIT	CELL	SPECIFIC	ATION		" CG10	" Version
Cell Name	Function							Number of B
H6CU	Tri-state Output & with Pull-up Resis	CMOS I tance	nterfa	ice Input	Buffer (	IOL=	3.2mA, Tru	e) 8
Ce	il Symbol			Pro	pagation D	elay Pa	rameter	
		tı	р			in		Path
		t 0	KCL	10	KCL	KCL	2 CDR2	raui
ot x		0.575 0.639 (3.70)	0.01 0.03		0.023 0.080			X to IN OT to X
	С		L to			Z to		
		t O		KCL	t O		KCL	C to X
		1.780 (17.72		•	1.170 (8.23		0.083	
Pin Name	Input Loading Factor (lu)	]						
οτ	6 2		H to		<del> </del>	Z to		
С	-	10	7 10	KCL				
			-+	KCL	10	$\neg$		
Pin Name	Output Driving Factor (lu)	2.120 (17.72		•	0.700 (8.23		0.037	
IN	36							





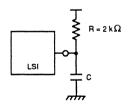
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

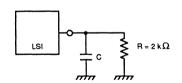
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H6CU-E0 | Sheet 1/1

	FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION " CG10" Version  Cell Name Function Number													
								Number of BC						
	Tri-state Output & with Pull-down Res			ce Input E	Buffer (	IOL=3	3.2mA, Tr	<sub>1e)</sub> 8						
Č	eli Symbol			Pro	pagation D	elay Par	rameter							
		tı.	ıp			fn nt		Path						
		t O	KCL	10	KCL	KCL2	CDR2							
IN X		0.575 0.639 (3.70)	0.017 0.036		0.023 0.080			X to IN OT to X						
	С		L to			Z to		0 to Y						
		<u> </u>		KCL	t 0		KCL	C to X						
		1.780 (17.72		•	1.170 (8.23		0.083							
Pin Name	Input Loading Factor (lu)													
OT C	6 2		H to	7		Z to	ш							
	2	10	1 10	KCL										
				KCL	0.700	$\overline{}$	0.037							
Pin Name	Output Driving Factor (lu)	2.120 (17.72		•	0.700 (8.23		0.037							
IN	36													





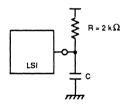
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

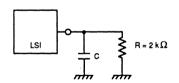
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H6CD-E0 | Sheet 1/1

FUJIT	SU CMOS GATE AR	RAY UNIT	CEL	L SF	PECIFICA	ATION		" CG10	7 "Version
Cell Name	Function								Number of B
H6CF	Tri-state Outpo (IOL=8mA, Tru	ut & CM( e)	OS Ir	nter	face In	out Buffe	er		8
Cel	l Symbol	T							
		tup				to	In		Path
		10	КС	L	t 0	KCL	KCL	2 CDR2	Faui
IN	×	0.575 0.693 (3.76)	0.03		0.831 2.343 (6.09)	0.023 0.044			X to IN OT to X
	Ċ		L	οZ			Zto		<del> </del>
		10			KCL	t O		KCL	CtoX
		2.140 (19.83			•	1.57! (5.32		0.044	
Pin Name	Input Loading Factor (lu)								
от	4 2						لا		4
С	2	10	н	to Z	KCL	to	Z to	KCL	4
		2.120	`		NOL	0.70		0.037	1
Pin Name	Output Driving Factor (lu)	(19.83			•	(5.32		0.037	
IN	36								



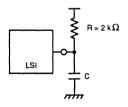


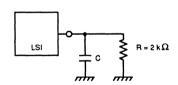
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C10-H6CF-E0 Sheet 1/1

" CG10 " Version FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION Number of BC Cell Name Function Tri-state Output & CMOS Interface Input Buffer (IOL=8mA, True) H6CFU 8 with Pull-up Resistance Cell Symbol Propagation Delay Parameter Path KCL KCL2 CDR2 t 0 KCL t 0 0.575 0.017 0.831 0.023 X to IN OT to X 0.693 0.036 2.343 0.044 (3.76)(6.09)Z to L L to Z KCL t O KCL C to X t O 1.575 0.044 2.140 (19.83)(5.32)Input Loading Pin Name Factor (lu) OT C 42 H to Z Z to H t O KCL t O KCL 2.120 0.700 0.037 Output Driving (19.83)(5.32)Pin Name Factor (lu) IN 36

These values are subject to external loading condition.
 Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:

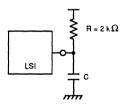


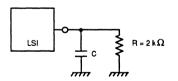


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C10-H6CFU-E0 Sheet 1/1

	SU CMOS GATE AR	RAY UNIT	CEL	L SI	PECIFICA	ATION		" CG10	) " V	
Cell Name	Function									Number of Bo
H6CFD	Tri-state Output with Pull-down			erfa	ace Inpu	ut Buffer	· (IOL	_=8mA, Tr	ue)	8
Cel	Symbol	T			Proj	pagation D	elay Pa	rameter		
		tı	tup tdn						J	Path
		t 0	KC	7	t 0	KCL	KCL	2 CDR2	1	rain
OT —	7		0.03		0.831 2.343 (6.09)	0.023 0.044				X to IN OT to X
	Ü		Lt	o Z			Z to			
		t 0			KCL	t O		KCL	]	C to X
		2.140 (19.83			•	1.575 (5.32		0.044		
Pin Name	Input Loading Factor (lu)	]								
OT	4 2								4	
С	2		- Н	to Z	1401	ļ	Z to		4	
		10			KCL	t0		KCL	-	
Pin Name	Output Driving (19 Pin Name Factor (Iu)				•	0.700 (5.32		0.037		
IN	36									

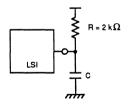


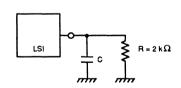


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C10-H6CFD-E0 Sheet 1/1

FUJIT	SU CMOS GATE ARI	RAY UNIT	CELL	SPECIFIC	ATION		" CG10	" Version
Cell Name	Function							Number of BC
H6E	Power Tri-state Input Buffer (IC	e Output DL=12m	. & CN A, Tru	IOS Inter e)	face			8
Ce	l Symbol			Pro	pagation D	elay Pa	rameter	
20 000		tı	ıp			n		Path
		t O	KCL	`t0	KCL	KCL	2 CDR2	raui
и ОТ	\ <sup>7</sup>		0.017 0.024		0.023 0.034			X to IN OT to X
	Ċ		L to	Z KCL	t O	Z to	L KCL	C to X
		2.560 (20.71)		•	1.219 (5.64)		0.052	Clox
Pin Name	Input Loading Factor (lu)							
от	6							
С	2	<del></del>	H to	Z KCL		Z to	H KCL	
		t O	-+	KUL	10			
Pin Name	Output Driving Factor (lu)	2.540 (20.71		•	0.800 (5.64		0.025	
IN .	36			•				

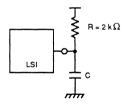


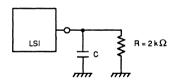


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C10-H6E-E0 | Sheet 1/1

	TSU CMOS GATE AR	HAT UNIT	CELL	SPECIFIC	ATION		1 0010	" Version
Cell Name	Function							Number of E
H6EU	Power Tri-stat	e Output DL=12m/	: & CI Tru	MOS Inter e) with Pr	face JII–up R	esista	ince	8
Ce	II Symbol			Pro	pagation D	elay Pa	rameter	
		tup tdn						
		t 0	KCL	. t0	KCL	KCL	2 CDR2	Path
ın —— от ——			0.01 0.02		0.023 0.034			X to IN OT to X
	Ċ		L to	Z	<del>                                     </del>	Z to	L	
		t 0		KCL	t 0		KCL	C to X
		2.560 (20.71		•	1.219 (5.64		0.052	
Pin Name	Input Loading Factor (Iu)		į					
ОТ	6 2				<u> </u>			
С	2		H to		<del> </del>	Z to		
	1	10		KCL	10		KCL	
Pin Name	Output Driving Factor (lu)	2.540 (20.71		٠	0.800 (5.64		0.025	
IN	36							





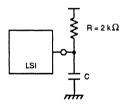
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

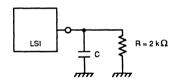
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H6EU-E0 | Sheet 1/1

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFIC	ATION		" CG10	" Version
Cell Name	Function							Number of BC
H6ED	Power Tri-state Input Buffer (IO	Output L=12m/	& CM	OS Inter ) with Pu	face III-down	Resis	tance	8
Ce	II Symbol				pagation D			
		tı	ıρ			in		Path
		t O	KCL	t O	KCL	KCL2	CDR2	
IN	~		0.017 0.024	0.831 2.620 (5.51)	0.023 0.034			X to IN OT to X
	c	10	L to Z	KCL	to	Z to L	KCL	C to X
		2.560 (20.71		•	1.219 (5.64		0.052	
Pin Name	Input Loading Factor (lu)							
ОТ	6 2					L		
С	2	<del></del>	H to Z			Z to H		
		t O		KCL	t O		KCL	
Pin Name	Output Driving Factor (lu)	2.540 (20.71		•	0.800 (5.64		0.025	
IN	36							

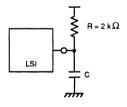


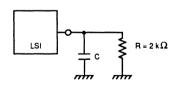


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C10-H6ED-E0 | Sheet 1/1

FUJI	SU CMOS GATE AR	RAY UNIT	CELL	SPECIFICA	ATION		" CG10	" Version	
Cell Name	Function							Number of Bo	
H6S	Tri-state Output (IOL=3.2mA, C	ut & Sch MOS Ty	mitt Ti pe, Ti	rigger Inp rue)	ut Buffe	r		12	
Ce	II Symbol	I	Propagation Delay Parameter						
		t.			to			Path	
		10	KCL	10	KCL	KCL2	CDR2		
	IN —		0.067 0.036		0.056 0.080			X to IN OT to X	
от	×		L to	7		Z to L			
		10	- 10	KCL	t O	7101	KCL	C to X	
		1.78 (17.7		•	1.17 (8.2		0.083		
Pin Name	Input Loading Factor (lu)								
от	6 2		H to			Z to H			
С	2	10	H 10	KCL	10	2 to H	KCL		
				NOL		<u>.                                    </u>			
Pin Name	Output Driving Factor (lu)	2.12 (17.7		•	0.70 (8.2		0.037		
IN	18								





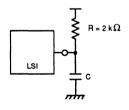
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

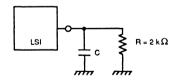
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H6S-E0 | Sheet 1/1

FUJI	SU CMOS GATE AR	RAY UNIT	CELLS	PECIFIC	ATION		" CG10	" Version
Cell Name	Function							Number of BC
H6SU	Tri-state Output (IOL=3.2mA, C	ut & Sch MOS Ty	mitt Trig	gger Inp ie) with i	ut Buffe Pull–up	r Resis	tance	12
Ce	ll Symbol	I		Pro	pagation D	elay Par	ameter	
		tı	ıρ		to			Path
		t O	KCL	10	KCL	KCL2	CDR2	
in	×		0.067 0.036	1.925 1.460 (8.26)	0.056 0.080			X to IN OT to X
	Ċ	10	L to Z	KCL	t0	Z to I	L KCL	C to X
		1.78		•	1.170 (8.23)		0.083	0.07
Pin Name	input Loading Factor (lu)							
OΤ	6 2							
С	] 2	10	H to Z	KCL	10	Z to I	H KCL	
				NOL	<del> </del>			
Pin Name	Output Driving Factor (Iu)	2.12 (17.7		•	0.70 (8.2		0.037	
IN	18							

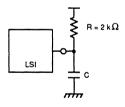


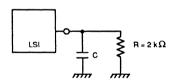


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C10-H6SU-E0 Sheet 1/1

	SU CMOS GATE AR	MAT UNIT	CELI	<u> </u>	ECIFICA	ATION			CG10	" Version
Cell Name	Function									Number of E
H6SD	Tri-state Outpi (IOL=3.2mA, C	ut & Sch MOS Ty	mitt T pe, T	rigo rue	ger Inp ) with f	ut Buffe Pull–dov	r vn R	esis	stance	12
Cel	Symbol	Τ			Proj	pagation D	elay Pa	ram	eter	
		tı	tup tdn							Path
		t 0	KCI	- 1	t 0	KCL	KCL	2	CDR2	ram
IN ————————————————————————————————————			0.06 0.03		1.925 1.460 (8.26)	0.056 0.080				X to IN OT to X
	C	10	L to		KCL	to	Zt	o L	KCL	C to X
			1.780 (17.72)		•	1.17 (8.2		(	0.083	
Pin Name	Input Loading Factor (lu)	1								
от	6 2							L		
С	2	10	Нt		KCL	10	Z to	Н	KCL	
					NOL	<u> </u>				
Pin Name	Output Driving Factor (lu)	2.12 (17.7			•	0.70 (8.2		,	0.037	
IN	18	]								





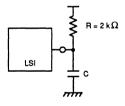
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

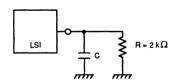
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H6SD-E0 Sheet 1/1

FUJI	TSU CMOS GATE AR	RAY UNIT	CELL	SPECIFIC	ATION		" CG10	" Version
Cell Name	Function							Number of BC
H6R	Tri-state Outp (IOL=3.2mA, T	ut & Sch TL Type	mitt Ti	igger Inp )	ut Buffe	r		12
Ce	II Symbol	T			pagation D	elay Pa	rameter	
		tı.	ıp	T	tc	in		Path
		t O	KCL	t O	KCL	KCL	2 CDR2	Pan
	_	1.400 0.639 (3.70)	0.067 0.036		0.073 0.080			X to IN OT to X
ot	×							
		10	L to	Z KCL	to	Z to	KCL	C to X
		1.78		•	1.17 (8.2		0.083	C 10 X
Pin Name	input Loading Factor (lu)							
QΤ	6 2				ļ	ــــــــــــــــــــــــــــــــــــــ		
С	2	10	H to	Z KCL	10	Z to	KCL	
			_	NOL	<del> </del>			
Pin Name	Output Driving Factor (lu)	2.12 (17.7		•	0.70 (8.2		0.037	
IN	18							





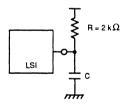
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

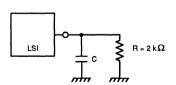
Note: 1. The unit of KcL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H6R-E0 | Sheet 1/1

FUJIT	ISU CMOS GATE AR	RAY UNIT	CELL	. SPECIFIC	ATION		" CG10	" Version
Cell Name	Function							Number of B
H6RU	Tri-state Outp (IOL=3.2mA, T	ut & Sch TL Type	mitt T , True	rigger Inp e) with Pu	ut Buffe II–up Re	r sista	ince	12
Ce	I Symbol	T			pagation D			
		tı.	ıp		t	dn		Path
		t0 KCL		t 0	KCL	KCL	2 CDR2	rath
IN —— ОТ ——	×	1.400 0.639 (3.70)	0.06 0.03		0.073 0.080			X to IN OT to X
	С	<b> </b>	L to	Z	<del> </del>	Z to	) L	
		t O		KCL	10		KCL	C to X
		1.78 (17.7		•	1.17 (8.2		0.083	
Pin Name	Input Loading Factor (Iu)	]						
ΟT	6 2				ļ	لا		
С	2		H to	KCL	10	Z to	KCL	
				NOL .	<del></del>			
Pin Name	Output Driving Pin Name Factor (Iu)		0 2)	•	0.70 (8.2		0.037	
IN	18							





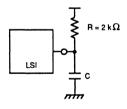
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

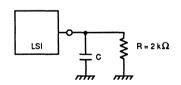
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H6RU-E0 Sheet 1/1

FUJIT	<u>SU CMOS GATE AR</u>	RAY UNIT	CELL S	SPECIFICA	ATION		" CG10	" Version
Cell Name	Function							Number of BC
H6RD	Tri-state Outpo (IOL=3.2mA, T	ut & Sch TL Type	mitt Tri , True)	gger Inp with Pul	ut Buffe I–down	r Resis	tance	12
Cell	Symbol	T	·		pagation D			
		tı.			to		Path	
		t 0	KCL	10	KCL	KCL2	CDR2	
	_	1.400 0.639 (3.70)	0.067 0.036	2.325 1.460 (8.26)	0.073 0.080			X to IN OT to X
ot —	×		L to Z			Z to		
		t O		KCL	t O		KCL	C to X
		1.78 (17.7		*	1.17 (8.2		0.083	
Pin Name	Input Loading Factor (lu)	1						
οτ	6 2	ļ	H to Z		<u> </u>			
С	2	10	H to 2	KCL	10	Z to I	KCL	
		2.12	_	.,,,,,	0.70	<u>.                                    </u>	0.037	
Pin Name	Output Driving Factor (Iu)	(17.7		•	(8.2		0.037	
IN	18							





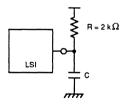
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

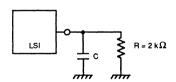
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H6RD-E0 | Sheet 1/1

FUJIT	SU CMOS GATE AR	RAY UNIT	CELLS	PECIFICA	ATION		" CG10	" Version
Cell Name	Function							Number of BC
H8T	Tri-state Outp & Input Buffer	ut with N (IOL=3.2	oise Lii mA, Tr	nit Resi: ue)	stance			9
Cei	I Symbol	T			pagation D	elay Para	meter	
		tı	ıp		to	Path		
		t O	KCL	t O	KCL	KCL2	CDR2	
	4	0.663 1.177 (4.24)	0.017 0.036	1.150 3.190 (9.99)	0.023 0.080			X to IN OT to X
от —	×		L to Z			Z to L		
		10		KCL	t O		KCL	C to X
		1.73 (17.6		•	3.57 (10.6		0.083	
Pin Name	Input Loading Factor (Iu)							
οτ	2 2	ļ	H to Z		ļ	Z to H	,	
С	2	10	H 10 Z	KCL	10	2 10 F	KCL	
					1.30	_		
Pin Name	Output Driving Factor (lu)	1.86		•	(10.6		0.037	
IN	36							





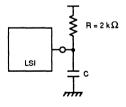
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

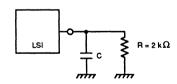
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-	H8T-E0	Sheet 1/1

FUJIT	SU CMOS GATE AR	RAY UNIT	CELL S	PECIFICA	ATION		" CG10	" Version
Cell Name	Function							Number of BO
H8TU	Tri-state Outp	ut with N (IOL=3.2	oise Lir mA, Tr	nit Residue) with	stance Pull-up	Resis	stance	9
Cell	Symbol			Pro	pagation De	elay Para	meter	
			ıρ		td	ln		Path
		t O	KCL	· t 0	KCL	KCL2	CDR2	
	1	0.663 1.177 (4.24)	0.017 0.036	1.150 3.190 (9.99)	0.023 0.080			X to IN OT to X
ot	×							
		10	L to Z	KCL	10	Ztol	KCL	C to X
		1.73		*	3.57! (10.63		0.083	CIOX
Pin Name	Input Loading Factor (lu)	]						
OT C	2 2	ļ	H to Z			Z to F		
C	2	10	H 10 Z	KCL	to	2 10 1	KCL	
		-	_	NOL	<del></del>	_		
Pin Name	Output Driving Factor (lu)	1.86 (17.6		•	1.30 (10.6		0.037	
IN	36	]						





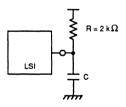
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

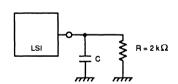
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H8TU-E0 Sheet 1/1

FUJIT	SU CMOS GATE AR	RAY UNIT	CELLS	PECIFIC	ATION		" CG10	" Version
Cell Name	Function							Number of BC
H8TD	Tri-state Outpo & Input Buffer	ut with N IOL=3.2	oise Li mA, Tr	mit Residue) with	stance Pull-do	wn Res	sistance	9
Cel	l Symbol			Pro	pagation D	elay Parar	neter	
			ıp			In		Path
		0.663	KCL	t O	KCL	KCL2	CDR2	
	IN —		0.017 0.036	1.150 3.190 (9.99)	0.023 0.080			X to IN OT to X
ot —	× ×							
•	Ç		L to Z			ZtoL		
		10		KCL	10		KCL	C to X
		1.73 (17.6		•	3.57 (10.6		0.083	
Pin Name	Input Loading Factor (Iu)							
OT C	2 2		H to Z		ļ <u>.</u>	Z to H		
C		10	102	KCL	10		KCL	
		1.86	<u> </u>		1.30		0.037	
Pin Name	Output Driving Factor (lu)	(17.6		•	(10.6		0.007	
IN	36							





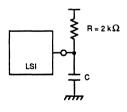
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

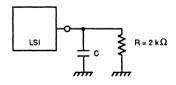
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H8TD-E0 Sheet 1/1

FUJI	TSU CMOS GATE AR	RAY UNIT	CELLS	PECIFIC	ATION		" CG10	" Version		
Cell Name	Function							Number of BC		
H8TF	Tri-state Outp & Input Buffer	ut with N (IOL=8m	oise Li	mit Resi	stance			9		
Ce	II Symbol	T	.,		pagation D	elay Para	meter			
		tı	ıp.	1	to	DI				
		t O	t0 KCL		KCL	KCL2	CDR2	Path		
ın <del></del>	IN X		0.663 1.231 (4.30)		1.231 0.036		0.023 0.044			X to IN OT to X
ОТ	×	10	L to Z	KCL	tO	Z to l	- KCL	C to X		
		2.24(19.7)		•	3.98 (7.72		0.044			
Pin Name	Input Loading Factor (Iu)	]								
от	2 2				ļ					
С	2	10	H to Z	KCL	10	Z to F	KCL			
			<del>   -</del>	NOL	<del> </del>	<del>.  </del>				
Pin Name	Output Driving Factor (lu)	1.860		*	1.30 (7.72		0.037			
IN	36									

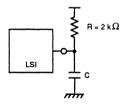


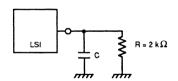


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C10-H8TF-E0 | Sheet 1/1

Cell S				nit Resis	stanco			Number of BC					
	& Input Buffer (			nit Resis	Tri-state Output with Noise Limit Resistance								
Cell (	Symbol												
		L		Pro	pagation D	elay Parai	meter						
		tu			to			Pa#:					
		10	KCL	t O	KCL	KCL2	CDR2	·					
OT	~ 1		0.017 0.036	1.150 4.073 (7.82)	0.023 0.044			X to IN OT to X					
	·	L to Z			Z to L								
		t 0		KCL	10		KCL	C to X					
		2.240 (19.76		•	3.98 (7.72		0.044						
Pin Name	Input Loading Factor (lu)												
от	2 2				ļ								
c	2	10	H to Z	KCL	10	Z to H	KCL						
		<del></del>		ROL									
Pin Name	Output Driving Factor (lu)	1.860 (19.76		•	1.30 (7.72		0.037						
IN	36												





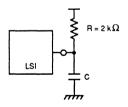
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

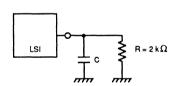
Note: 1. The unit of KcL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H8TFU-E0 Sheet 1/1

FUJI	<u>TSU CMOS GATE AR</u>	RAY UNII	CELL S	SPECIFIC	ATION		" CG10	" Version
Cell Name	Function							Number of BC
H8TFD	Tri-state Outp & Input Buffer					n Res	sistance	9
Ce	II Symbol			Pro	pagation D	elay Par	ameter	
			ip			in		Path
		0.663	KCL	t 0	KCL	KCL2	CDR2	
			0.017 0.036	1.150 4.073 (7.82)	0.023 0.044			X to IN OT to X
ot ——	×							
	Ċ		L to Z	<u> </u>		Z to	1	
		10		KCL	t O	T	KCL	C to X
		2.240 (19.70		•	3.98 (7.72		0.044	
Pin Name	Input Loading Factor (lu)	]						
OT	2 2							
С	2	10	H to Z	KCL	10	Z to	H KCL	
				NOL	<del> </del>			
Pin Name	Output Driving Factor (lu)	1.860		•	1.30 (7.72		0.037	
IN	36							





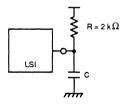
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

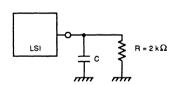
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H8TFD-E0 Sheet 1/1

FUJI	TSU CMOS GATE AR	RAY UNIT	CELI	<u> SP</u>	ECIFICA	ATION			" CG10	" Version
Cell Name	Function									Number of B
H8W	Power Tri-stat & Input Buffer	e Output (IOL=12r	with	No rue	ise Lim	it Resis	tanc	е		9
Ce	Il Symbol	Ì.				pagation D	elay Pa	arame	ter	
		t	ıρ		tdn			Path		
		10	KCI		· t 0	KCL	KCI	2	CDR2	Pain
IN	×	0.663 1.477 (3.52)	0.01 0.02		1.150 4.770 (7.66)	0.023 0.034				X to IN OT to X
	°	10	L to		KCL	t O	Z to		KCL	C to X
	Input Loading	2.600 (20.64			•	3.75 (8.18			0.052	
Pin Name	Factor (lu)					}		İ	1	
ОТ	2 2	1								
Ċ	2		Ht				Z to			
		t O			KCL	t O		<u> </u>	KCL	
Pin Name	Output Driving Factor (lu)	2.29 (20.6			•	1.40 (8.18		0	.025	
IN	36									





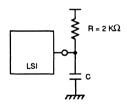
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

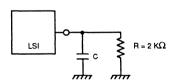
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H8W-E0 | Sheet 1/1

Cell Name H8WU	U CMOS GATE ARR Function Power Tri-state & Input Buffer (I	Output	with NonA, Tru	oise Lim e) with I Proj	nit Resis Pull-up pagation D	Resis elay Par In	tance ameter	Number of BC
	& Input Buffer (I	to 0.663 1.477	nA, Tru  RCL  0.017	e) with I	Pull—up pagation D	Resis elay Par In	tance ameter	
Cell S	iymbol	t 0 0.663 1.477	KCL 0.017	t 0	tc	ln .		
	7	t 0 0.663 1.477	KCL 0.017					
		0.663 1.477	0.017		KCL			Path
	1	1.477				KCL2	CDR2	
IN ———	~		0.024	1.150 4.770 (7.66)	0.023 0.034			X to IN OT to X
от	×		L to Z			Z to		
		t O	L to Z	KCL	10	2 10	KCL	C to X
		2.600 (20.64		•	3.75 (8.18		0.052	
Pin Name	Input Loading Factor (lu)							
०	2 2					Z to		
c	۷	10	H to Z	KCL	10	Z 10 1	KCL	
		2.290	$\overline{}$	1102	1.40		0.025	
Pin Name	Output Driving Factor (lu)	(20.64		•	(8.18		0.025	
IN	36							





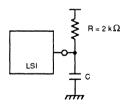
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

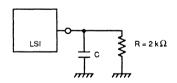
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H8WU-E0 Sheet 1/1

FUJIT	SU CMOS GATE AR	RAY UNIT	CELLS	PECIFIC	ATION		" CG10	" Version
Cell Name	Function							Number of BC
H8WD	Power Tri-stat & Input Buffer	e Output (IOL=12)	with N	oise Lim ue) with	nit Resis Pull-dov	tance vn Re	esistance	9
Cel	Symbol	T		Pro	pagation D	elay Par	ameter	
			ıp		tdn			Path
		t O	KCL	t O	KCL	KCL2	CDR2	
	IN —		0.017 0.024	1.150 4.770 (7.66)	0.023 0.034			X to IN OT to X
ot —	×							
	С	-	L to Z	I		Z to		
		t O		KCL	t O		KCL	C to X
		2.60 (20.6-		•	3.75 (8.18		0.052	
Pin Name	Input Loading Factor (lu)							
OT C	2 2		H to Z			Z to		
C	2	10	H 10 Z	KCL	10	- Z 10	KCL	
		2.29	$\overline{}$		1.40	$\overline{}$	0.025	
Pin Name	Output Driving Factor (lu)	(20.6		•	(8.18		0.025	
IN	36							





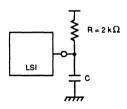
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

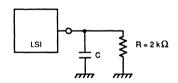
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H8WD-E0 | Sheet 1/1

FUJIT	SU CMOS GATE AR	RAY UNIT	CELL	SPECIFIC	ATION		" CG10	" Version
Cell Name	Function							Number of BC
H8C	Tri-state Outpo	ut Buffer ace Inpu	with h	Noise Limer (IOL=3	it Resis .2mA, T	tance rue)	!	9
Ce	II Symbol	T		Pro	pagation D	elay Pa	rameter	
		, t				in		Path
		0.575	KCL	10	KCL	KCL	2 CDR2	
	IN —		0.017 0.036		0.023 0.080			X to IN OT to X
ot ——	×							
		1.730 (17.65)			Z to L			<b>.</b>
				*	3.57 (10.6		КСL 0.083	C to X
Pin Name	Input Loading Factor (Iu)	1						
OT C	2 2		H to	7	<del> </del>	Z to	ш	
C	2	10	7 10	KCL	10		KCL	
		1.86	$\overline{}$		1.30		0.037	
Pin Name	Output Driving Factor (lu)	(17.6		•	(10.6		0.007	
IN	36							





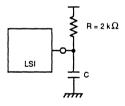
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

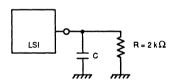
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H8C-E0 | Sheet 1/1

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL S	PECIFICA	ATION		" CG10	" Version
Cell Name	Function	<u> </u>					·	Number of BC
H8CU	Tri-state Outpu Interface Input	it Buffer Buffer (I	w/ Nois OL=3.2	se Limit mA, Tru	Resista ie) w/ Pu	nce & C ull-up F	CMOS Resistan	ce 9
Ce	II Symbol	Propagation Delay Parame					neter	
		t		tdn			,	Path
		0.575	KCL	10	KCL	KCL2	CDR2	
	IN OT X		0.017 0.036	0.831 3.190 (9.99)	0.023 0.080			X to IN OT to X
1			L to Z			ZtoL		
		t 0		KCL	10		KCL	C to X
		1.730 (17.65		•	3.57! (10.63		0.083	
Pin Name	Input Loading Factor (lu)							
OT C	2 2		H to Z		ļ	Z to H		
C	2	10	H 10 Z	KCL	10	210 11	KCL	
		1.860	$\neg +$		1.30	<u>,                                    </u>	0.037	
Pin Name	Output Driving Factor (lu)	(17.6		•	(10.6		0.007	
IN	36							





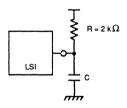
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

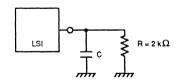
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H8CU-E0 Sheet 1/1

	SU CMOS GATE ARE	RAY UNIT	CELL	SPECIFIC	ATION		" CG10	" Version
Cell Name	Function							Number of BC
H8CD	Tri-state Output I Interface Input Bu							nce 9
Cell	Symbol			Pro	pagation D	elay Pa	rameter	
			ip			in		Path
		t O	KCL	· t 0	KCL	KCL	2 CDR2	
			0.017 0.036	1	0.023 0.080			X to IN OT to X
ot—	*		L to			Z to		
		10	L 10	KCL	10	-	KCL	C to X
		1.730		*	3.57 (10.6	5	0.083	0.10 X
Pin Name	Input Loading Factor (lu)							
οτ	2 2		H to	7		Z to	н	
Ŭ	_	10	1110	KCL	10		KCL	
		1.86	<u>,                                    </u>		1.30		0.037	
Pin Name	Output Driving Factor (lu)	(17.6		•	(10.6		0.007	
IN	36							





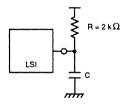
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

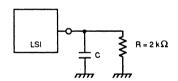
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H8CD-E0 Sheet 1/1

	TSU CMOS GATE AR	DAT UNIT	OLLL	SECTIO.	ATION		1 2010	" Version Number of Bo
Cell Name		4 D. #			'A D ' '			Number of Bo
H8CF	Tri-state Outp	n Britter	with I	voise Lim	it Hesisi	ance		9
11001	& CMOS Interf	ace Inpu	t Buff					
Ce	ll Symbol			Pro	pagation D	elay Para	meter	
		tı				in		Path
		10	KCL	t O	KCL	KCL2	CDR2	
		0.575	0.017		0.023		i l	X to IN
		1.231	0.036		0,044		1 1	OT to X
		(4.30)		(7.82)			1 1	
	1						1 1	
IN	<b>-</b> < h			1	1		1 1	
ľ	\ 7							
от—	x	1	1	i			1 1	
٠. ا	6	1	l				1 [	
•		1	i	1			1 1	
	1	1	ł	ł			1	
	С	ļ	L to	<del>_</del>		Z to L		
		to	<u></u>	KCL	10	T	KCL	C to X
		2.240	,		3.980	·	0.044	• .•
		(19.76		•	(7.72		0.044	
		1	1		1		1	
		]			1	i		
	Input Loading	l				- 1	1	
Pin Name	Factor (lu)	4				İ	į	
от	2 2				<b></b>			
С	2		H to			Z to H		
		10		KCL	t O		KCL	
	0.4.101.1	1.860		_	1.30		0.037	
Pin Name	Output Driving Factor (lu)	(19.76	7)	•	(7.72	,		
IN	36	1	1			- 1		
IN	36		l		l	- [	I	
						- 1		
	1	I	- 1		1			





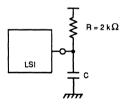
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

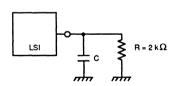
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H8CF-E0 | Sheet 1/1

FUJII	ISU CMOS GATE AR	RAY UNII	CELL	SPECIFIC	ATION		- 00	110	Version
Cell Name	Function								Number of B
H8CFU	Tri-state Output Interface Input B							:e	9
Ce	II Symbol	T			pagation D				<del></del>
			T	D. 4					
		t O	KCL	t O	KCL	KCI	2 CDF	12	Path
ın ——— от ———	×	0.575 1.231 (4.30)	0.017 0.036		0.023 0.044				X to IN OT to X
	С	<b> </b>	L to	Z Z		Z to	, L	$\dashv$	
		t O		KCL	t O		KCL		C to X
		2.240 (19.76		•	3.98 (7.72		0.044		
Pin Name	input Loading Factor (lu)	]							
от	2 2	ļ			ļ				
С	2	10	H to	KCL	10	Z to	KCL	$\dashv$	
			$\overline{}$	ROL	1.30		0.037		
Pin Name	Output Driving Factor (lu)	1.860		•	(7.72		0.037		
IN	36								

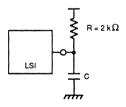


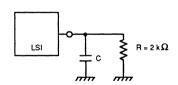


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C10-H8CFU-E0 Sheet 1/1

FUJI	TSU CMOS GATE AR	RAY UNIT	CELLS	PECIFIC	ATION		" CG10	" Version
Cell Name	Function							Number of BC
H8CFD	Tri-state Output Interface Input B	Buffer w uffer (IO	/ Noise L=8mA	Limit R , True) v	esistano w/ Pull—	e & CN down F	MOS Resistanc	e 9
Ce	II Symbol	Propagation Delay Paramet						
		tı	ıp		to			Path
		t O	KCL	t O	KCL	KCL2	CDR2	raui
IN	$\prec$	0.575 1.231 (4.30)	0.017 0.036	0.831 4.073 (7.82)	0.023 0.044			X to IN OT to X
от	x		L to Z			Z to L		
		t 0		KCL	t 0		KCL	C to X
		2.240 (19.76		•	3.980 (7.72		0.044	
Pin Name	Input Loading Factor (Iu)	]					i	
от	2 2		H to Z			Z to H		
С	2	10	H 10 Z	KCL	10	2 10 H	KCL	
	1	1.860	<del>,                                    </del>	NOL	1.300	$\overline{}$	0.037	
Pin Name	Output Driving Factor (Iu)	(19.76		•	(7.72		0.037	
IN	36							

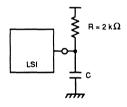


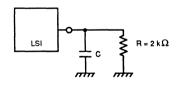


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C10	) <del>-</del> H	8CF	D-E0	Sheet	1/1

FUJI	<u>TSU CMOS GATE AR</u>	RAY UNIT	CELLS	SPECIFIC	ATION		" CG10	" Version
Cell Name	Function							Number of B
H8E	Power Tri-stat & CMOS Interf						tance	9
Ce	II Symbol	T						
		tı	ıp		<u>↓</u> to			Path
		t O	KCL	t O	KCL	KCL	2 CDR2	raui
	4	0.575 1.477 (3.52)	0.017 0.024	0.831 4.770 (7.66)	0.023 0.034			X to IN OT to X
от——	×							
		10	L to Z	KCL	10	Z to	KCL	0 to V
				KCL				C to X
		2.60 (20.6		•	3.75 (8.18		0.052	
Pin Name	Input Loading Factor (Iu)							
οŢ	2 2	ļ			<b> </b>	لـــــا		
С	2	10	H to Z	KCL	10	Z to	KCL	
				NOL	<del> </del>			
Pin Name	Output Driving Factor (lu)	2.29 (20.6		•	1.40 (8.18		0.025	
IN	36							





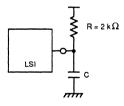
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

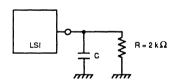
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H8E-E0 Sheet 1/1

	ISU CMOS GATE AR	HAT UNII	CELL	SPECIFIC	ATION		CGIU	" Version
Cell Name	Function							Number of B
H8EU	Power Tri-state Interface Input B							
Ce	II Symbol	pagation D		ameter				
		t.				dn		Path
		t O	KCL	. t 0	KCL	KCL2	CDR2	
	1	0.575 1.477 (3.52)	0.01 0.02		0.023 0.034			X to IN OT to X
OT X								
			L to	KCL	10	Z to l	- KCL	C to X
		10	-	KUL	<del></del>			C 10 X
		2.600 (20.6-		•	3.75 (8.18		0.052	
Pin Name	Input Loading Factor (lu)							
OT C	2 2		H to	. 7	<del> </del>	Z to h		
C	_	10		KCL	to		KCL	
			$\overline{}$		<del></del>		0.025	
Pin Name	Output Driving Factor (lu)	2.290		•	1.40		0.025	
IN	36							





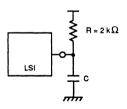
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

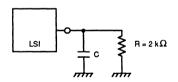
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H8EU-E0 Sheet 1/1

FILIIT	SU CMOS GATE ARF	TIMIL VAS	CELL	SPECIFIC	ATION		1 " CG10	" Version
Cell Name	Function	101111	JLLL	OI LOII IO	311014		1 0070	Number of BC
H8ED	Power Tri-state ( Interface Input Bu	Output E offer (IO	Buffer L=12r	w/ Noise nA, True)	Limit Re w/ Pull-	sistar dowr	nce & CMo n Resistan	os o
Cel	i Symbol							
			Р			in		Path
		t O	KCL	10	KCL	KCL2	CDR2	
		0.575 1.477 (3.52)	0.017 0.024		0.023 0.034			X to IN OT to X
от —	×							
			L to			Z to		21.14
		2,600	$\rightarrow$	KCL	3.75	-	KCL 0.052	C to X
		(20.6-		*	(8.18		0.032	
Pin Name	Input Loading Factor (lu)							
οŢ	2 2				<b></b>			
C	2	to	H to	KCL	10	Z to	KCL	
			$\overline{}$			<del></del>		
Pin Name	Output Driving Factor (lu)	2.29 (20.6		•	1.40 (8.18		0.025	
IN	36							

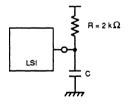


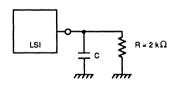


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KcL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C10-H8ED-E0 | Sheet 1/1

FUJI	TSU CMOS GATE AR	RAY UNIT	CELI	L SF	PECIFICA	ATION			" CG10	" Version
Cell Name	Function									Number of BC
H8S	Tri-state Output (IOL=3.2mA, C	ıt & Sch MOS Ty	mitt 1 pe, 1	rig rue	ger Inp	ut Buffe Noise Li	r mit F	Resi	stance	13
Ce	II Symbol	1			Proj	pagation D	elay Pa	erame	ter	
		tı		In			Path			
		t O	KCI	L	t 0	KCL	KCI	2	CDR2	raui
	4	1.550 1.177 (4.24)	0.06 0.03		1.925 3.190 (9.99)	0.056 0.080				X to IN OT to X
ot —	×									
		10	L to		KCL	10	Z to		KCL	C to X
					KUL					CIOX
		1.73 (17.6			•	3.57 (10.6		0	0.083	
Pin Name	Input Loading Factor (lu)									
OT C	2 2	<b> </b>	— <u> </u>	- 7			Zto			
C	4	10	- 1		KCL	t O			KCL	
					NOL					
Pin Name	Output Driving Factor (lu)	1.86 (17.6			•	1.30 (10.6			).037	
IN	18									





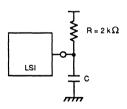
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

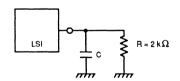
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H8S-E0 | Sheet 1/1

FUJI	TSU CMOS GATE ARE	RAY UNIT	CEL	_ SI	PECIFICA	ATION			" CG10	" Ve	ersion
Cell Name	Function										Number of BC
H8SU	Tri-state Output & Type, True) w/ No	Schmitt se Limit	Trig Res	ger ista	ance w/	Pull-up	Res	ista	ance	os	13
C	ell Symbol				Proj	pagation D	elay Pa	ram	eter		
			ıp				ln				Path
		t O	KC	_	10	KCL	KCL	2	CDR2		
IN	<b>√</b> h	1.550 1.177 (4.24)	0.06 0.03		1.925 3.190 (9.99)	0.056 0.080					X to IN OT to X
от											
		10	Lto	5 Z	KCL	t O	Z to	L	KCL	İ	C to X
					NOL						CIOX
		1.73 (17.6			•	3.57 (10.6			0.083		
Pin Name	Input Loading Factor (lu)										
οτ	2 2			o Z		ļ	Z to				
С	2	10	- H I	0 2	KCL	t 0	210	Н	KCL		
					NOL						
Pin Name	Output Driving Factor (lu)	1.86 (17.6			•	1.30 (10.6			0.037		
IN	18				:						
		<u> </u>				<u> </u>				L	

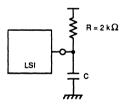


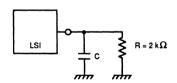


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C10-H8SU-E0 | Sheet 1/1

	TSU CMOS GATE AR	HAT UNIT	CELL S	PECIFICA	ATION		LG10	" Version				
Cell Name	Function							Number of B				
H8SD	Tri-state Output & Type, True) w/ No	Schmitt ise Limit	Trigge Resista	r Input E ance w/	Buffer (IC Pull-dov	DL=3.2 wn Res	mA, CMC sistance	DS 13				
C	ell Symbol		Propagation Delay Parameter									
		tı.			to			Path				
		t O	KCL	10	KCL	KCL2	CDR2					
IN		1.550 1.177 (4.24)	0.067 0.036	1.925 3.190 (9.99)	0.056 0.080			X to IN OT to X				
от	×		L to Z			Z to L						
		t 0		KCL	t 0		KCL	C to X				
		1.73 (17.6		•	3.57 (10.6		0.083					
Pin Name	Input Loading Factor (lu)											
οŢ	2 2	<b></b>	H to Z		<b> </b>	Z to H						
С	4	10	H to Z	KCL	10	∠ to H	KCL					
				ROL		<u>,                                    </u>						
Pin Name	Output Driving Factor (lu)	1.86		•	1.30 (10.6		0.037					
IN	18					İ						





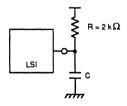
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

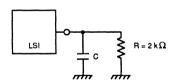
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H8SD-E0 | Sheet 1/1

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL	SF	PECIFICA	ATION		$\neg$	" CG10	" Version
Cell Name	Function									Number of B
H8R	Tri-state Outpu (IOL=3.2mA, T	t & Sch	mitt T , True	rig e) v	ger Inpi vith Noi	ut Buffe se Limit	r Res	ista	nce	13
Cell	Symbol	elay Pa	rame	ter						
		tı.					in			Path
		10	KCL	-	· t0	KCL	KCL	2	CDR2	
IN	<b>-</b> €h	1.400 1.177 (4.24)	0.06 0.03		2.325 3.190 (9.99)	0.073 0.080				X to IN OT to X
от	×									
		10	L to		KCL	10	Z to		KCL	C to X
		1.73 (17.6			•	3.57 (10.6			.083	C 10 X
Pin Name	Input Loading Factor (lu)									
OT	2 2			_						
С	2	10	H to		KCL	t O	Z to		KCL	
			,		or	1.30	<del>,  </del>		.037	
Pin Name	Output Driving Factor (lu)	1.86 (17.6			•	(10.6		U	.03/	
IN	18									

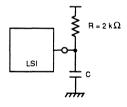


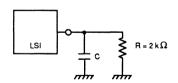


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C10-H8R-E0 | Sheet 1/1

	SU CMOS GATE AR	INAT CIVIT	OLL	- 01 1	LO11 107	TION			00.0		ersion
Cell Name	Function									_	Number of B
H8RU	Tri-state Output Type, True) w/ N	& Schm oise Lim	itt Tri it Re	gge sista	ance w	/ Pull–u	p Re	sista	ance	TL	13
Ce	il Symbol		Propagation Delay Parameter								
		tup				to					Path
		t 0	t0 KCL			KCL	KCL	2	CDR2		raui
IN			0.06 0.03	6	2.325 3.190 (9.99)	0.073 0.080					X to IN OT to X
	C		L to				Z to				
		10		<u> </u>	CL	t O			KCL		C to X
		1.73 (17.6			•	3.57 (10.6		0.	.083		
Pin Name	Input Loading Factor (lu)	]									
ΟT	2 2						ليـــــــــــــــــــــــــــــــــــــ				
С	2	<del></del>	H to		(CL		Z to		KCL		
		10			VOL.	t O					
Pin Name	Output Driving Factor (lu)	1.86			•	1.30 (10.6		0.	.037		
IN	18										

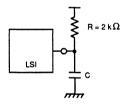


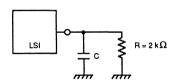


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C10-	-H8R	U-E0	Sheet 1/1	

FUJIT	SU CMOS GATE ARF	RAY UNIT	CEL	L SI	PECIFICA	ATION			" CG10	" V	ersion
Cell Name	Function										Number of BC
H8RD	Tri-state Output Type, True) w/ No	& Schm bise Lim	itt Tri it Re	gg sis	tance w	/ Pull-d	own	Re	sistance	L ∋	13
Cell	Symbol				Prop	pagation D	elay Pa	aram	eter		
		tı.	ıρ				In				Path
		t O	KC	L	t O	KCL	KCL	2	CDR2		raui
IN	×	1.400 1.177 (4.24)	0.00		2.325 3.190 (9.99)	0.073 0.080					X to IN OT to X
	•		Lt	o Z			Z to	o L			
		t O			KCL	10			KCL	ŀ	C to X
		1.73 (17.6			•	3.57 (10.6			0.083		
Pin Name	Input Loading Factor (lu)										
OT	2 2	ļ		_			لبيب	Ļ			
С	2	<u> </u>	Н:	o Z	KCL	10	Z to	Н	KCL		
		t O			NUL		_	<u> </u>		l	
Pin Name	Output Driving Factor (lu)	1.86 (17.6			•	1.30 (10.6			0.037		
IN	18										

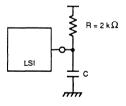


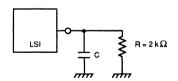


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C10-H8RD-E0 | Sheet 1/1

FUJIT	SU CMOS GATE ARE	RAY UNIT	CELL	_ SI	PECIFICA	ATION		" CG10	" Version
Cell Name	Function								Number of BC
H8W2	Power Tri-state & Input Buffer (I	Output OL=24r	with	No ru	oise Lim e)	it Resis	tanc	е	11
Cel	l Symbol								
	t O	tup			to	Path			
			KCL		· t 0	KCL	KCI	2 CDR2	
и −−−− п	×	0.663 3.050 (4.50)	0.01 0.01		1.150 10.400 (13.55)	0.023 0.037			X to IN OT to X
	С		L to	2 7	L		Z to		
		t O	1		KCL	t O		KCL	C to X
		4.800 (22.74			•	12.49 (9.01		0.041	
Pin Name	Input Loading Factor (Iu)								
OT C	2 2		Hto	- 7			Z to	. 14	
C	4	10	- H 10	<i>5</i> <u>∠</u>	KCL	t O	T	KCL	
			,		1101	2.00	$\overline{}$	0.020	
Pin Name	Output Driving Factor (lu)	3.620 (22.74			•	(12.4		0.020	
IN	36								





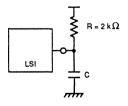
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

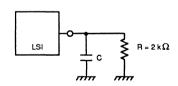
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H8W2-E0 | Sheet 1/1

FUJIT	SU CMOS GATE ARF	RAY UNIT	CELL	SPECIFICA	ATION		" CG10	" Version
Cell Name	Function							Number of BC
H8W1	Power Tri-state & Input Buffer (I	Output OL=24r	with InA, Tr	Noise Limue) with I	it Resis Pull-up	tanc Resis	e stance	11
Cel	Symbol			Proj	pagation D	elay Pa	rameter	
		tup			to	Path		
		10	KCL	10	KCL	KCL	2 CDR2	
	1	0.663 3.050 (4.50)	0.017 0.017		0.023 0.037			X to IN OT to X
от —	×							
			L to 2			Z to		
		t O		KCL	t O		KCL	C to X
		4.800 (22.74		•	12.49 (9.01		0.041	
Pin Name	Input Loading Factor (Iu)							
OT C	2 2	ļ	H to	7	<del> </del>	Z to	L	
		t O	11 10	KCL	to		KCL	
		3.620	$\overline{}$		2.00		0.020	
Pin Name	Output Driving Factor (lu)	(22.74		•	(12.4		0.020	
IN	36							





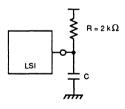
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

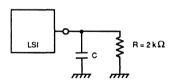
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H8W1-E0 Sheet 1/1

FUJI	ISU CMOS GATE ARI	TINU YAF	CELL	. SPECIFIC	ATION		" CG10	" Version
Cell Name	Function							Number of B0
H8W0	Power Tri-state & Input Buffer (	e Output IOL=24r	with nA, T	Noise Lir	nit Resis Pull–do	stanc wn R	e esistance	11
Ce	II Symbol			Pre	pagation D	elay Pa	arameter	
			tup			dn	Path	
		t O	KCL	. to	KCL	KCI	2 CDR2	
IN	×	9.663 3.050 (4.50)	0.01 0.01					X to IN OT to X
	c	t O	L to	Z KCL	to	Zt	o L KCL	C to X
		4.80 (22.7		•	12.49 (9.0		0.041	
Pin Name	Input Loading Factor (lu)							
OT C	2 2		H to	. 7	<del> </del>	Z to	L	
C	2	10		KCL	1 10		KCL	
		3.62	<del>,  </del>	1,72	2.00		0.020	
Pin Name	Output Driving Factor (lu)	(22.7		•	(12.4		0.020	
IN	36						:	

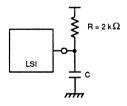


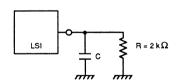


- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.
- Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
  - 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
  - 3. The parameters in parentheses are the values applied to the simulation.

C10-H8W0-E0 | Sheet 1/1

FUJIT	SU CMOS GATE AR	RAY UNIT	CELL S	PECIFICA	ATION	***************************************	" CG10	" Version		
Cell Name	Function							Number of BC		
H8E2	Power Tri-state & CMOS Interfa	e Output ace Inpu	w/ Noi t Buffer	se Limit (IOL=2	Resista 4mA, Tr	nce rue)		11		
Cell	Symbol		Propagation Delay Parameter							
	· · · · · · · · · · · · · · · · · · ·		tup tdn					Path		
		t O	KCL	t O	KCL	KCL2	CDR2			
	_	0.575 3.050 (4.50)	0.017 0.017	0.831 10.400 (13.55)	0.023 0.037			X to IN OT to X		
ot —	×		L to Z			Z to L				
		10	L to Z	KCL	10	2 to L	KCL	C to X		
		4.80		*	12.49 (9.01		0.041	C IO X		
Pin Name	Input Loading Factor (lu)	]								
OT C	2 2		H to Z			Z to H				
Ÿ	-	10	11.02	KCL	10		KCL			
		3.62	,		2.00	0	0.020			
Pin Name	Output Driving Factor (lu)	(22.7		•	(12.4		0.020			
IN	36									





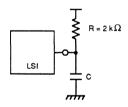
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

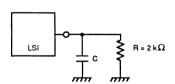
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H8E2-E0 | Sheet 1/1

FUJI	TSU CMOS GATE AR	TINU YAF	CELL	SPECIFICA	ATION		" CG10	" Version
Cell Name	Function							Number of BC
H8E1	Power Tri-state & CMOS Input	e Output Buffer (I	w/ No OL=2	oise Limit 4mA, Tru	Resista e) w/ Pu	ance ull-up	Resistanc	e 11
Ce	II Symbol				pagation D			
			ıp			dn		Path
		10	KCL	10	KCL	KCL	2 CDR2	
	_	0.575 3.050 (4.50)	0.017 0.017		0.023 0.037			X to IN OT to X
ot	×							
		10	L to	KCL KCL	10	Z to	KCL	C to X
		4.800		*	12.49 (9.01	90	0.041	0.10 %
Pin Name	Input Loading Factor (lu)							
OT	2 2	<u> </u>	H to	7		<u> </u> Z to		
C	C 2		H 10	KCL	10		KCL	
		3.62	1		2.00		0.020	
Pin Name	Output Driving Factor (Iu)	(22.7		•	(12.4		0.020	
IN	36							





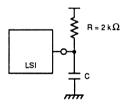
- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

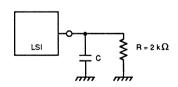
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H8E1-E0   Sheet 1/1
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FUJI	<u> ISU CMOS GATE AR</u>	RAY UNIT	CELL	SPECIFICA	ATION		" CG10	" V ∈	ersion
Cell Name	Function								Number of B
H8E0	Power Tri-state & CMOS Input B	Output Buffer (IC	w/ Noi: )L=24:	se Limit F nA, True	Resistar ) w/ Pul	nce I-dow	n Resistar	nce	11
Ce	ii Symbol			Pro	pagation D	elay Pa	rameter		
			ıp			ın			Path
		t 0	KCL	· t0	KCL	KCL	2 CDR2		
	1	0.575 3.050 (4.50)	0.017 0.017		0.023 0.037				X to IN OT to X
ot ——	×								
		10	L to 2	KCL	10	Z to	KCL		C to X
		4.80		*	12.49 (9.01	90	0.041		0.10 %
Pin Name	Input Loading Factor (lu)	]							
OT C	2 2	-	H to :	7	<del> </del>	Z to	Н		
J		10	11.0	KCL	10		KCL		
		3.62	<u>,                                    </u>		2.00	+	0.020	l	
Pin Name	Output Driving Factor (lu)	(22.7		•	(12.4		0.020		
IN	36								





- (a) Measurement of tpd at LZ and ZL.
- (b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

- 2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
- 3. The parameters in parentheses are the values applied to the simulation.

C10-H8E0-E0 | Sheet 1/1

## 3

## **Appendix A: General AC Specifications**

Mimimum/maximum Delay Multipliers (Recommended Operating Conditions, Ta = 0 to 70°C,  $V_{DD}$  = 5  $V_{\pm}5\%$ 

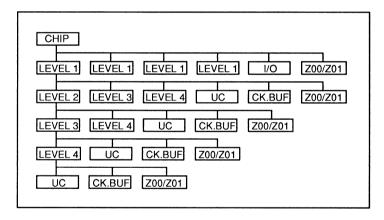
Delay Multipliers	Min.	Max.	
Pre-layout Simulation	0.35	1.65	
Post-layout Simulation	0.40	1.60	

### **Appendix B: Hierarchical Structure**

Hierarchical blocks (or Functional Logic Blocks) within other hierarchical blocks are user-defined groups of cells laid out in close proximity to each other in both X and Y dimensions of the array.

The hierarchical method of design allows circuit sections to be placed within the array at positions relative to each other. This is made possible by the designer's defining and placing functional logic blocks within the hierarchy and thus controlling path lengths.

There are five levels of hierarchy, also referred to as Functional Logic Blocks (FLBs). The design rules regarding what may and what must appear at certain levels are condensed in the diagram below.



All I/O buffers and their associated circuitry must be defined immediately beneath the chip level with the FLB1 blocks. Nothing but I/O buffers may be so defined. If pull-up or pull-down cells (A01s or X00s) are required for unused inputs of the I/O buffers, they must also be defined at this level. Unit cells (UC) may be defined at each level.

For optimum delay characteristics, Level 2 blocks should be defined under each of the Level 1 blocks, Level 3 Blocks under Level 2 blocks, and so on. Unit cells should be defined under Level 4.

## **Appendix C: Estimation Tables for Metal Loading**

### CG10272 (2700-gate device)

			Cloc	Clock Net					
N <sub>DI</sub>	C <sub>L</sub> (lu)	N <sub>DI</sub>	CK20, CK40	CK60, CK80					
			C <sub>L</sub> (lu)	C <sub>L</sub> (lu)					
1	2.3	1	8.3	12.9					
2	4.9	2	8.3	12.9					
3	6.7	3	15.8	24.9					
4	7.8	4	15.8	24.9					
5	8.5	5	23.3	36.9					
6	9.3	6	23.3	36.9					
7	10.2	7	30.7	48.9					
8	10.5	8	30.7	48.9					
9	10.8	9	34.7	55.2					
10	11.0	10	34.7	55.2					
11	11.0	11	35.0	55.5					
12	11.3	12	35.0	55.5					
13	11.4	13	35.4	55.9					
14	11.7	14	35.4	55.9					
15	11.7	15	35.4	55.9					
16 – 30	12.7	16 – 30	35.8	56.3					
31 – 50	14.4	31 – 50	38.8	59.3					
51 – 75	14.8	51 – 80	42.8	63.3					
76 – 100	16.3								

### CG10342 (3400-gate device)

			Cloc	k Net
N <sub>DI</sub>	C <sub>L</sub> (lu)	N <sub>DI</sub>	CK20, CK40	CK60, CK80
			C <sub>L</sub> (lu)	C <sub>L</sub> (lu)
1	2.8	1	8.9	14.0
2	5.9	2	8.9	14.0
3	8.0	3	16.9	27.3
4	9.3	4	16.9	27.3
5	10.3	5	24.9	40.4
6	11.2	6	24.9	40.4
7	12.2	7	32.9	53.5
8	12.7	8	32.9	53.5
9	13.0	9	41.0	66.8
10	13.4	10	41.0	66.8
11	13.4	11	41.4	67.2
12	13.5	12	41.4	67.2
13	13.7	13	41.8	67.7
14	14.0	14	41.8	67.7
15	14.0	15	41.8	67.7
16 – 30	15.2	16 – 30	42.3	68.0
31 – 50	17.4	31 – 50	45.4	71.2
51 – 75	17.9	51 – 80	49.5	75.3
76 – 100	19.7			

Continued on next page

# Appendix C: Estimation Tables for Metal Loading

### CG10492 (4900-gate device)

			Cloc	k Net
N <sub>DI</sub>	C <sub>L</sub> (lu)	N <sub>DI</sub>	CK20, CK40	CK60, CK80
			C <sub>L</sub> (lu)	C <sub>L</sub> (lu)
1	3.3	1	9.7	15.8
2	7.2	2	9.7	15.8
3	9.7	3	18.5	30.7
4	11.3	4	18.5	30.7
5	12.5	5	27.3	45.5
6	13.5	6	27.3	45.5
7	14.8	7	36.2	60.4
8	15.4	8	36.2	60.4
9	15.8	9	44.9	75.3
10	16.2	10	44.9	75.3
11	16.2	11	53.8	90.2
12	16.4	12	53.8	90.2
13	16.5	13	54.2	90.5
14	17.0	14	54.2	90.5
15	17.0	15	54.2	90.5
16 – 30	18.4	16 – 30	54.7	91.0
31 – 50	21.0	31 – 50	57.9	94.3
51 – 75	21.7	51 – 80	62.3	98.7
76 – 100	23.8			

### CG10572 (5700-gate device)

	C <sub>L</sub> (lu)	N <sub>DI</sub>	Clock Net		
N <sub>DI</sub>			CK20, CK40	CK60, CK80	
			C <sub>L</sub> (lu)	C <sub>L</sub> (lu)	
1	3.8	1	10.0	16.7	
2	8.2	2	10.0	16.7	
3	11.1	3	19.4	32.6	
4	12.9	4	19.4	32.6	
5	14.4	5	28.6	46.5	
6	15.5	6	28.6	46.5	
7	17.0	7	38.1	64.5	
8	17.6	8	38.1	64.5	
9	18.1	9	46.7	79.6	
10	18.5	10	46.7	79.6	
11	18.5	11	60.6	101.0	
12	18.8	12	60.6	101.0	
13	18.9	13	60.9	101.7	
14	19.5	14	60.9	101.7	
15	19.5	15	60.9	101.7	
16 – 30	21.1	16 – 30	61.5	102.7	
31 – 50	24.1	31 – 50	64.6	107.9	
51 – 75	24.8	51 – 80	69.4	115.9	
76 – 100	27.3				

Continued on next page

## **Appendix C: Estimation Tables for Metal Loading**

### CG10672 (6700-gate device)

				***************************************	Clock Net	
N <sub>Dt</sub>	Within Block	N <sub>DI</sub>	Inter-Block	N <sub>DI</sub>	CK20, CK40	CK60, CK80
	C <sub>L</sub> (lu)		C <sub>L</sub> (lu)		C <sub>L</sub> (lu)	C <sub>L</sub> (lu)
1	2.0	1	4.4	1	12.4	16.5
2	4.4	2	9.5	2	18.7	31.0
3	5.9	3	12.8	3	30.2	46.7
4	6.9	4	15.0	4	36.5	61.2
5	7.7	5	16.7	5	_	
6	8.3	6	18.0	6		_
7	9.0	7	19.7	7		
8	9.4	8	20.4	8		_
9	9.7	9	21.0	9	_	_
10	9.9	10	21.5	10		
11	9.9	11	21.5	11	_	_
12	10.0	12	21.8	12		_
13	10.3	13	22.0	13	_	
14	10.5	14	22.7	14		_
15	10.5	15	22.7	15	<b> </b>	_
16 – 30	11.4	16 – 30	24.5	16 – 30	_	_
31 – 50	13.0	31 – 50	28.0	31 – 50	_	_
51 – 75	13.3	51 – 80	28.8	51 – 80	_	_
76 – 100	14.7	76 – 100	31.7			

#### CG10103 (10000-gate device)

					Clock Net	
N <sub>DI</sub>	Within Block	N <sub>DI</sub>	Inter-Block	N <sub>DI</sub>	CK20, CK40	CK60, CK80
	C <sub>L</sub> (lu)		C <sub>L</sub> (lu)		C <sub>L</sub> (lu)	C <sub>L</sub> (lu)
1	2.8	1	5.3	1	14.8	19.7
2	5.9	2	11.5	2	22.3	37.2
3	8.0	3	15.5	3	36.2	56.0
4	9.3	4	18.2	4	43.7	73.4
5	10.3	5	20.0	5	_	_
6	11.2	6	21.7	6	-	
7	12.2	7	23.7	7	_	
8	12.7	8	24.7	8	-	
9	13.0	9	25.3	9	_	
10	13.4	10	26.0	10		_
11	13.4	11	26.0	11	_	_
12	13.5	12	26.3	12	-	
13	13.7	13	26.7	13	_	
14	14.0	14	27.3	14	_	_
15	14.0	15	27.3	15	-	_
16 – 30	15.2	16 – 30	29.5	16 – 30	-	
31 - 50	17.4	31 – 50	33.9	31 – 50	-	_
51 75	17.9	51 – 80	34.8	51 – 80	_	_
76 – 100	19.7	76 – 100	38.2		_	-

Continued on next page

### **Appendix C: Estimation Tables for Metal Loading**

### CG10133 (13000-gate device)

					Clock Net		
N <sub>DI</sub>	Within Block	N <sub>DI</sub>	Inter-Block	N <sub>DI</sub>	CK20, CK40	CK60, CK80	
	C <sub>L</sub> (lu)		C <sub>L</sub> (lu)		C <sub>L</sub> (lu)	C <sub>L</sub> (lu)	
1	3.3	1	6.2	1	17.2	22.9	
2	7.2	2	13.5	2	25.9	43.4	
3	9.7	3	18.2	3	42.2	65.4	
4	11.3	4	21.3	4	51.0	85.9	
5	12.5	5	23.5	5	_	_	
6	13.5	6	25.4	6			
7	14.8	7	27.8	7			
8	15.4	8	28.9	8		_	
9	15.8	9	29.7	9	_	_	
10	16.2	10	30.4	10			
11	16.2	11	30.4	11	_	_	
12	16.4	12	30.8	12	_		
13	16.5	13	31.3	13	_		
14	17.0	14	32.0	14	_		
15	17.0	15	32.0	15	-		
16 – 30	18.4	16 – 30	34.7	16 – 30	_	_	
31 – 50	21.0	31 – 50	39.7	31 – 50	_	_	
51 <i>–</i> 75	21.7	51 – 80	40.8	51 – 80	_		
76 – 100	23.8	76 – 100	44.8				

<sup>&</sup>quot;Inter-Block" tables must be applied to a net which has an inter-block connection. If a net, for example, has three  $N_{Dl}$  in a block and one  $N_{Dl}$  in a different block,  $N_{Dl}$  = 4 of the "Inter-Block" table must be applied.

### Appendix D: Available Package Types

**CG10 CMOS Available Package Types** 

	CG10272	CG10342	CG10492	CG10572	CG10692	CG10103	CG10133
DIP (Dual In-line P	ackage)		anteres de la compar en la comparación de	trional rational	Najari, Kiri		
DIP28	•	•	•	•			
DIP40	•	•	•	•	•	_	_
DIP42	•	•	•	•	•		_
DIP48	•	•	•	•	•	_	_
SH-DIP (Shrink Du	ial In-line P	ackage)		1 1 1 1 1 1 1 1 1		Ngayanaka atomba sa	a dayle year
SH-DIP42	•	•	•	•	•		
SH-DIP64	•	•	•	•	•	_	_
QFP (Quad Flat Pa	nckage)						
QFP48	•	•	•			-	-
QFP64	•	•	•	•	•	•	
QFP80	•	•	•	•	•	•	_
QFP100	•	•	•	•	•	•	
QFP120	•	•	•	•	•	•	•
QFP160	_	_	•	•	•	•	•
QFP196	_	_		_	_		•
SQFP (Shrink Qua	d Flat Pack	age)		3 (6 (6 (6 (7 (7 (6 (			
SQFP64	•	•	_		_		
SQFP100	•	•	•	_	_	_	_
SQFP176	_		_		_	•	•
SQFP208	_	_	_	_	_		•
PGA (Pin Grid Arr	ay Package	)		Kay a salah da da da da da da da da da da da da da	Tar. Sentandah	vi Vi	on a profession of sol
PGA64	•	•	•	•	•	•	•
PGA88	•	•	•	•	•	•	•
PGA135	•	•	•	•	•	•	•
PGA179		_	•	•	•	•	•
PGA208	_	_	_	_		•	•
PGA256		_	_	_	_	•	•
PGA-50 mil (Pin C	irid Array P	ackage-50 mi	I)			National Control	
PGA256	_	_	_	_	_		•
PLCC (Plastic Lea	ded Chip C	arriers)					
PLCC68	•						
1 20008			1		1		

### **Appendix E: TTL 7400 Function Conversion Table**

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
7400	Quad 2-input NAND	4 x N2N	4
7401	Quad 2-input NAND, Open Collector Outputs	T24 multiplexer	6
7402	Quad 2-input NOR	4 x R2N	4
7403	Quad 2-input NAND, Open Collector Outputs	T24 multiplexer	6
7404	Hex Inverter	6 x VIN	6
7405	Hex Inverter, Open Collector Outputs	R6B	5
7406	Hex Inverter/Buffer, Open Collector Outputs	R6B	5
7407	Hex Buffer, Open Collector Outputs	2 x N3N into R2N	5
7408	Quad 2-input AND	4 x N2P	8
7409	Quad 2-input AND, Open Collector Outputs	N8P	6
7410	Triple 3-input NAND	3 x N3N	6
7411	Triple 3-input AND	3 x N3P	9
7412	Triple 3-NAND, Open Collector Outputs	T33	7
7413	Dual 4-input NAND, Schmitt Trigger	2 x (4 x I2R to N4N)	68
7414	Hex Schmitt Trigger Inverter	6 x l1R	48
7415	Triple 3-input AND, Open Collector Outputs	N8P to N2P	8
7418	Dual 4-input NAND, Schmitt Trigger	2 x (4 x I2R to N4N)	68
7419	Hex Schmitt Trigger Inverter	6 x l1R	48
7420	Dual 4-input NAND	2 x N4N	4
7421	Dual 4-input AND	2 x N4P	6
7422	Dual 4-input NAND, Open Collector Outputs	2 x N4N + N2P	6
7423	Expanded Dual 4-input NOR with Strobe	R4P to D23 + R4P to R2N	9
7424	Quad Schmitt Trigger 2-input NAND	8 x 12R + 4 x N2N	68
7425	Dual 4-input NOR with Strobe	2 x (R4P + R2N)	8
7426	Quad 2-input NAND, High Voltage Output	4 x N2N	4
7427	Triple 3-input NOR	3 x R3N	6
7428	Quad 2-input NOR Buffer	4 x R2N	4
7430	8-input NAND	N8B	6
7432	Quad 2-input OR	4 x R2P	8
7433	Quad 2-input NOR Buffer, Open Collector	A DON MAD	7
7434	Outputs Hex Noninverter	4 x R2N + N4P 6 x B1N	6
7434 7435			5
7435 7437	Hex Noninverter with Open Collector Outputs	2 x N3N into R2N 4 x N2B	5 12
	Quad 2-input NAND Buffer	4 X N2B	12
7438/9	Quad 2-input NAND Buffer, Open Collector	A NON . NAD	-7
7440	Outputs	4 x N2N + N4P	7
	Dual 4-input NAND Buffer BCD to Decimal Decoder	2 x N4B (N4N if not power)	8(4)
7442 7443	EX3 to Decimal Decoder	4 x V2B + 10 x N4N	24 24
7443 7444	4 to 10 Line Decoder	4 x V2B + 10 x N4N 4 x V2B + 10 x N4N	24
7444 7445	BCD to Decimal Decoder/driver (30V)	4 x V2B + 10 x N4N 4 x V2B + 10 x N4N	24
7445 7446	BCD to 7-segment Decoder/Driver (30V)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
7440 7447	BCD to 7—segment Decoder/Driver (30V) BCD to 7—segment Decoder/Driver (15V)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
7447 7448		4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
7448 7449	BCD to 7–segment Decoder/Driver BCD to 7–segment, Open Collector Outputs	4 x V 1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P 4 x V 1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
7449 7450	Dual 2-input, 2-wide AOI (One Expandable)	D36 + D24	5 5
7450 7451	AOI	2 x D24	4
7451 7452	Expandable 4-wide AND-OR	N3N + D36 + V1N into N3N	8
7452 7453	Expandable 4-wide AND-ON  Expandable 4-wide AOI	D36 + D23 into N2P	7
7453 7454	4-wide AOI	2 x N3N + 2 x N2N + N4N + V1N	9
7454 7455	2-wide 4-input AOI	742	6
7455 7460	Dual 4-input AOI Dual 4-input Expander	142 2 x N4P	6
7460 7461		2 x N4P 3 x N3P	6
7461 7462	Triple 3-input Expander		8
7462 7464	4-wide AND-OR Expander	2 x N3N + 2 x N2N + N4N	10
	4-2-3-2 AOI	T54 T54	10
7465	4-2-3-2 AOI (Open Collector)	104	10

Continued on next page

### **TTL 7400 Function Conversion Table**

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
7470	AND-gated positive-edge JK FF with Preset		
.4.0	and Clear	3 x V1N + 2 x N3N + N2N + R2N + FJD	21
	or:	FD4 + 2 x N2N + R2N + V1N + R2P + D24	17
7471	AND-gated RS M/S FF with Preset		• • • • • • • • • • • • • • • • • • • •
	and Clear	FD4 + 2 x N3N + 2 x D23 + 2 x V1N	19
	or:	LT1+ 2 x N4N + N2P	10
7472	AND-gated JK M/S FF with Preset		
	and Clear	V1N + 2 x N3N + N2N + R2N + FJD	19
	or:	FD4 + N3P + N3N + V1N + D24	17
7473	Dual JK FF with Clear	2 x FJD	24
7474	Dual positive-edge D-FF with Preset and		
	Clear	2 x FDP	16
7475	4-bit Bistable Latch	LTM	16
7476	Dual JK FF with Preset and Clear	2 x (FJD + N2N + R2N + V1N)	30
7477	4-bit Bistable Latch	LTM	16
7478	Dual JK FF with Preset and Common	2 x (FJD + N2N + R2N + V1N)	30
7480	Clear and Clock Gated Full Adder	A1N	8
7480 7482	2-bit Binary Full Adder	A2N	8 16
7482 7483	4-bit Binary Full Adder with Fast Carry	A2N A4H	48
7484	4-bit Magnitude Comparator	MC4	46 42
7486	Quad 2-input XOR	4 x X2N	12
7487	4-bit True/Complement Zero/One Element	4 x N2N + V1N + 4 x N2N	17
7489	64-bit (16 x 4) Memory	2 x DE6 + V1N + 16 x LT4	298
7400	o4-bit (10 x 4) Memory	+ 5 x (V2B + T5A) + 10 x V2B	230
7490	Decade Counter	2 x (FDP + FDO + N2P + N2N + R2N) + V1N	39
, 400	(Different Implementation)	4 x N2P + 2 x R2P + N2N + C41 + LT1	41
7491	8-bit Shift Register	2 x FDS + V1N	41
7492	Divide-by-12 Counter	4 x FDO + 2 x V1N + 2 x R2N + N2N	33
7493	4-bit Binary Counter	C41 + N2N (for the resets)	25
7494	4-bit Shift Register, 2 asynchronous Presets	FS3 ,	34
	4-bit Shift Register, 2 asynchronous		
	Presets, Full Implementation	4 x FDP + 4 x D24 + 2 x V1N	42
7495	4-bit Parallel-access Shift Register	FS2 + D24 + 2 x V1N	34
7496	5-bit Shift Register	5 x FDP + 5 x N2N + V1N(clock)	46
7497	Synch 6-bit Binary Rate Multiplier	FDR + 2 x FDO + 3 x V1N + 2 x N2N	122
		+ 2 x N3N + 2 x N4N + 5 x N6B + 3 x N8B	
		+ R2B + X2N + 5 x X1B.	
7498	4-bit Data Selector/Storage Register	FDQ + T2F + 4 x V1N	33
7499	4-bit Universal Shift Register	FS2 + LTK + 2 x D24 + 4 x V1N	42
74100	8-bit Bistable Latch	2 x YL4 + 2 x V1N	30
74101	AO-gated JK Negative-Edge FF,	EDO WILL O DOG	
74400	with Preset	FD3 + V1N + 3 x D24	15
74102	AND-gated JK Negative-Edge FF with	ED4 DO4 NOD NON	
74103	Preset and Clear Dual JK FF with Clear	FD4 + D24 + N3P + N3N	16
74103	or:	2 x FJD + 2 x V1N (for clock)	26
74106	or. Dual JK Negative-Edge FF with Preset	2 x (FD5 + D24 + V1N)	22
74100	and Clear	2 x (FD4 + D24 + V1N)	24
74107	Dual JK FF with Clear	2 x (FJD + 2 x V1N)	22
74108	Dual JK Negative-Edge FF with Preset	EN (100 FEX VIII)	22
	and Common Clear and Clock	2 x (FD4 + D24 + V1N)	24
74109	Dual JK Positive-Edge FF with Preset and		
	Clear	2 x (FDP + V1N + D24)	22
74110	AND-gated JK M/S FF with Data	=	
	Lockout	FDP + D24 + N3P + N3N	15
74111	Dual JK WS FF with Data Lockout	2 x (FDP + D24 + V1N)	22
74112	Dual JK Negative-Edge FF with Preset	,	
	and Clear	2 x (FD4 + D24 + V1N)	24

### **TTL 7400 Function Conversion Table**

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
74113	Dual JK Negative-Edge FF with Preset	2 x (FD3 + D24 + V1N)	22
74114	Dual JK Negative-Edge FF with Preset and		
	Common Clear and Clock	2 x (FD4 + D24 + V1N)	24
74116	Dual 4-bit Latch with Clear	2 x LTM	32
74120	Dual Pulse Synchronizer/Driver	2 x (N2P + LT1 + 4 x N3N + 2 x N2N + 2 x V1N)	36
74125	Quad Bus Buffer with 3-state Output	B41	9
74126	Quad Bus Buffer with 3-state Output	B41 + 4 x V1N	13
74132	Quad 2-input NAND Schmitt Trigger	4 x (2 x I2R + N2N)	68
74133	13-input NAND	2 x N4N + N3N + N2N into R4P	10
74134	12-input NAND with 3-state Outputs	NCB + O4R	15
74135	Quad 3-input EXOR/EXNOR	4 x X4N	20
74136	Quad 2-input EXOR with Open-Collector		
	Outputs	4 x X2N + R4N	14
74137	3-line to 8-line Decoder with Address		
	Latch	3 x LTK into DE6	42
74138	3-line to 8-line Decoder with Enable	DE6	30
74139	Dual 2-line to 4-line Decoder	2 x DE4	16
74141	BCD-to-Decimal Decoder	4 x V2B + 10 x N4N	24
74145	BCD-to-decimal Decoder	4 x V1N + 10 x N4N	24
74147	10-line to 4-line BCD Priority Encoder	3 x N4N + 3 x N3N + 2 x N2N + 2 x N2P	36
, 414,	10 mic to 4 mic Bob i Honty Encoder	+ 3 x R2N + R4N + 13 x V1N	00
74148	8-line to 3-line Octal Priority Encoder	N9B + 2 x N2N + R2P + R4N + 4 x N3N	40
74140	online to online Octar Phonty Encoder	+ 2 x N4N + G44 + 12 x V1N	40
74150	1-to-16 Multiplexer	DE3 + 2 x U28 + D24 + 2 x V1N	41
74150	1-to-8 Multiplexer with Strobe	DE3 + U28 + N2N + V1N	28
74151		DE3 + U28 + N2N + V1N	26 26
74152	1to-8 Multiplexers Dual 4-line to 1line Selector/Multiplexer	DE2 + 028 DE2 + 2 x U24 + 2 x R2N	19
74154	4-line to 16-line Decoder/Demultiplexer	2 x DE6 + V1N	61
74155	or: Dual 2-line to 4-line Decoder/Demultiplexer	2 x DE4 + N2P + 16 x R2P	50
74156	(Totem Pole) Dual 2-line to 4-line Decoder/Demultiplexer	8 x N3N + 2 x R2N + 5 x V1N	23
74150	(Open Collector)	8 x N3N + 2 x R2N + 5 x V1N	23
74157	Quad 2-line to 1-line multiplexer	T2F + 4 x R2N + B1N	13
74158	Quad 2-line to 1-line multiplexer	IZI TAXIIZIATOIN	10
	(Inverter Data Outputs)	4 x D24 + V1N + 2 x R2N	11
74159	4-line to 16-line Demultiplexer	2 x DE6 + V1N (without open collector)	50
74160	Synchronous 4-bit Counter	4 x C11 + K1B + 2 x V2B + V1N + B1N+	62
	(Decimal with Direct Clear)	N2K + 2 x R3N + R4N + 3 x R2N + N2N	,
74161	Synchronous 4-bit Counter (Binary	VALIET I THE	
	with Direct Clear)	C43	48
74162	Synchronous 4-bit Counter	<del></del>	
• • •	(Decimal with Synchronous Clear)	C45 + D36 + N3P + 2 x R2N + B1N	57
74163	Synchronous 4-bit Counter (Binary	OTO I DOOT HOLT EXHERT DIR	37
. +100	with Synchronous Clear)	C45	48
74164	8-bit Parallel Output Serial Shift	V-10	40
, 4104	Register, Asynchronous Clear	2 x FDR + N2P	54
74165	Register, Asynchronous Clear 8-bit Shift Register	2 x FDR + N2P 2 x FDS + 8 x D24 + 11 x V1N + K4B + R2P	54 71
74165 74166	8-bit Shift Register	2 x FDS + 8 x D24 + 11 x V IN + K4B + H2P 2 x FDR + 8 x D24 + 10 x V1N + K4B	71 80
74166 74168		2 X FUR + 0 X U24 + 1U X V IN + N4D	80
74108	4-bit Up/Down Synchronous Counter	A w C44 · A w T00 · 7 · NON · O · NON · DON	0"
	(Decade)	4 x C11 + 4 x T32 + 7 x N2N + 2 x N3N + R2N + 7 x V2B + K1B	85
74169	4-bit Up/Down Synchronous Counter		
	(Binary)	C47	68
74170	4-by-4 Register File	4 x (YL4 + B1N + V1N + U24) + 2 x DE4	104
74171	Quad D-FF with Clear	FDR + 4 x V1N	30
74172	16-bit (8 x 2) Register File	3 x DE6 + 4 x FDS + 16 x (N2N + G34 +	348
	( E/ Hogistor i no	+ V1N + 2 x R2P + 4 x U28) + 2 x V1N + 2 x R2P	340

### **TTL 7400 Function Conversion Table**

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
74173	4-bit D-type Register		
	(3-state Output)	FDR + 2 x R2N + B41 + 6 x V1N + K1B + 4 x D24	53
74174	Hex D-FF (Single Output)	FDR + 2 x FDO	40
74175	Quad D-FF (with Clear)	FDR + 4 x V1N	30
74176	Presettable Decade/Binary Counter	4 x FDP + 2 x R2N + 5 x N2N + 4 x N3N + K1B	49
74177	Presettable Binary Counter	4 x FDP + 5 x N2N + 4 x N3N + K1B	47
74178	4-bit Universal Shift Register	FS2	30
74179	4-bit Universal Shift Register		
	(Direct Clear)	FS2 + 9 x N2N + B1N	40
74180	9-bit Odd/Even Parity Checker	PO8 + 2 x D24 + V1N	23
74181	ALU/Function Generator	5 x V1N + 5 x T32 + 4 x D36 + 8 x X2N + 3 x T54 +	
		N6B + N4B + 2 x N2N + 2 x N4P	11
74182	Look-ahead Carry Generator	R4P + 2 x V1N + 2 x T44 + T33 + D24	36
74183	Dual Carry-save Full Adder	2 x A1N	16
	•	=	
74184	BCD-to-binary Code Converter	These devices are ROM based	
74185	Binary-to-BCD Code Converter	These devices are ROM based	
74190	Synch Up/Down Counter (BCD)	4 x FDP + 4 x X2N + K1B + 3 x V1N + 3 x N3N	
		+ 9 x N2N + 2 x T32 + T43	
74191	Synch Up/Down Counter (Binary)	C47	68
74192	Up/Down Dual Clock Counter (BCD)	4 x C11 + 4 x V2B + N6B + 2 x N3N + R2N + T32 + T42 + T43	79
74193	Up/Down Dual Clock Counter (Binary)	4 x C11 + 2 x N6B + 4 x V2B + R2N + D24 + T32 + T42	72
74194	4-bit Bidirectional Universal Shift Register	FDR + 6 x V1N + R2N + 4 x D36 + D23 + B1N	48
74195	4-bit Parallel Access Shift Register	FS2 + D24 + 2 x V1N	34
74196	Preset Decade/Binary Counter/Latch	4 x FDP + 2 x R2N + 5 x N2N + 4 x N3N + K1B	49
74197	Preset Binary Counter/Latch	4 x FDP + 5 x N2N + 4 x N3N + K1B	47
74198	8-bit Bidirectional Universal Shift Register	2 x FDR + D24 + 10 x V1N + R2N + 8 x D36	89
74199	8-bit Bidirectional Universal Shift		
	Register (JK Serial Input)	2 x FS2 + D24 + 3 x V1N + B1N + R2N + 8 x N2P	83
	or:	2 x FDR + 7 x D24 + T33 + 11 x V1N + R2N	85
74246	BCD-to-7-Segment Decoder/Driver	EXTENT X DET TOO THE THEIR	•
	(30V, Active Low Open Collector)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
74247	BCD-to-7-Segment Decoder/Driver	IT ATTENT TO ATTOM TO ATTEN	•
	(15V, Active Low Open Collector)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
74248	BCD-to-7-Segment Decoder/Driver	TATEL HANGEN TO ANOTHER TO ANGLE	٥.
, -,2-40	(Internal Pull-up)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
74249	BCD-to-7-Segment Decoder/Driver	TA 4 114 T 11 A 14214 T 10 A 14014 T 4 A 140F T 5 A 142F	3.
17240	(Open Collector)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
74260	Open Collector)  Dual 5-input NOR	2 x R6B	10
74265	Quad Complementary Output Element	2 x A6B B1N + V1N	,,,
74266	Quad 2–EXNOR, Open Collector	4 x X1N	12
74266 74273	Octal D-type FF with Clear	* ********	52
	Quad J–K FF	2 x FDR	
74276		4 x (FDP + V1N + D24) + 2 x B1N	46
74347	BCD-to-7-Segment Decoder/Driver	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53

Name	Function Page No.
A1A	1-bit Half Adder 3–253
A1N	1-bit Full Adder
A2N	2-bit Full Adder 3–255
A4H	4-bit Binary Full Adder with Fast Carry
BD3	Delay Cell
BD4	True Delay Buffer
BD5	Delay Cell
BD6	Delay Cell
B11	1-bit Bus Driver 3–319
B41	4-bit Bus Driver
B1N	True Buffer
C11	Non-scan Flip-flop for Counter
C41	Non-scan 4-bit Binary Asynchronous Counter
C42	Non-scan 4-bit Binary Synchronous Counter
C43	Non-scan 4-bit Binary Synchronous Up Counter
C45	Non-scan 4-bit Binary Synchronous Up Counter
C47	Non-scan 4-bit Binary Synchronous Up/Down Counter
DE2	2:4 Decoder
DE3	3:8 Decoder
DE4	2:4 Decoder with Enable
DE6	3:8 Decoder with Enable
D14	2-wide 3-AND 4-Input AOI
D23	2-wide 2-AND 3-Input AOI 3–71
D24	2-wide 2-AND 4-Input AOI
D34	3-wide 2-AND 4-Input AOI
D36	3-wide 2-AND 6-Input AOI
D44	2-wide 2-OR 2-AND 4-Input AOI
FDM	Non-scan D Flip-flop
FDN	Non-scan D Flip-flop with Set
FDO	Non-scan D Flip-flop with Reset
FDP	Non-scan D Flip-flop with Set and Reset
FDQ	Non-scan 4-bit D Flip-flop
FDR	Non-scan 4-bit D Flip-flop with Clear
FDS	Non-scan 4-bit D Flip-flop
FD2	Non-scan Power D Flip-flop
FD3	Non-scan Power D Flip-flop with Preset
FD4	Non-scan Power D Flip-flop with Clear and Preset
FD5	Non-scan Power D Flip-flop with Clear
FJD	Non-scan Positive Edge Clocked Power J-K Flip-flop with Clear
FS1	4-bit Serial-in Parallel-out Shift Register
	Continued on next page

Name	Function Page No.
FS2	4-bit Shift Register with Synchronous Load
FS3	4-bit Shift Register with Asynchronous Load
G14	2-wide 3-OR 4-Input OAI
G23	2-wide 2-OR 3-Input OAI
G24	2-wide 2-OR 4-Input OAI
G34	3-wide 2-OR 4-Input OAI
G44	3-wide 2-AND 2-OR 4-Input OAI
H6C	3-state Output (I <sub>OL</sub> = 3.2 mA) and CMOS Interface Input Buffer (True)
H6CD	H6C with Pull-down Resistance
H6CF	3-state Output (I <sub>OL</sub> = 8 mA) and CMOS Interface Input Buffer (True)
H6CFD	3-state Output (I <sub>OL</sub> = 8 mA) and CMOS Interface Input Buffer (True) with Pull-down Resistance
H6CFU	3-state Output (I <sub>OI</sub> = 8 mA) and CMOS Interface Input Buffer (True)
	with Pull-up Resistance
H6CU	H6C with Pull-up Resistance
H6E	Power 3-state Output (I <sub>OL</sub> = 12 mA) and CMOS Interface Input Buffer (True)
H6ED	H6E with Pull-down Resistance
H6EU	H6E with Pull-up Resistance
H6R	3-state Output (I <sub>OL</sub> = 3.2 mA) and Schmitt Trigger Input Buffer (TTL type, True) 3-40
H6RD	H6R with Pull-down Resistance
H6RU	H6R with Pull-up Resistance
H6S	3-state Output (I <sub>OL</sub> = 3.2 mA) and Schmitt Trigger Input Buffer (CMOS type, True) 3-40
H6SD	H6S with Pull-down Resistance
H6SU	H6S with Pull-up Resistance
H6T	3-state Output (I <sub>OL</sub> = 3.2 mA) and Input Buffer (True)
H6TD	H6T with Pull-down Resistance
H6TF	3-state Output (I <sub>OI</sub> = 3.2 mA) and Input Buffer (True)
H6TFD	3-state Output (I <sub>OL</sub> = 3.2 mA) and Input Buffer (True) with Pull-down Resistance 3–39
H6TFU	3-state Output (I <sub>OL</sub> = 3.2 mA) and Input Buffer (True) with Pull-up Resistance 3–38
H6TU	H6T with Pull-up Resistance
H6W	Power 3-state Output (I <sub>OL</sub> = 12 mA) and Input Buffer (True)
H6WD	H6W with Pull-down Resistance
H6WU	H6W with Pull-up Resistance
H8C	3-state Output Buffer (I <sub>OL</sub> = 3.2 mA) with Noise Limit Resistance and CMOS Interface Input Buffer (True)
H8CD	H8C with Pulf-down Resistance
H8CF	3-state Output (I <sub>OL</sub> = 8 mA) with Noise Limit Resistance and CMOS
11001	Interface Input Buffer (True)
	Continued on next page

Name	Function	Page No.
H8CFD	3-state Output (I <sub>OL</sub> = 8 mA) with Noise Limit Resistance and CMOS Interface Input Buffer (True) with Pull-down Resistance	3–423
H8CFU	3-state Output (I <sub>OL</sub> = 8 mA) with Noise Limit Resistance and CMOS Interface Input Buffer (True) with Pull-up Resistance	3–422
H8CU	H8C with Pull-up Resistance	
H8E	Power 3-state Output Buffer (I <sub>OL</sub> = 12 mA) with Noise Limit Resistance and CMOS Interface Input Buffer (True)	3–424
H8ED	H8E with Pull-down Resistance	
H8EU	H8E with Pull-up Resistance	
H8E0	H8E2 with Pull-down Resistance	
H8E1	H8E2 with Pull-up Resistance	
H8E2	High Power 3-state Ouput (I <sub>OL</sub> = 12 mA) with Noise Limit Resistance and Input Buffer (CMOS type, True)	
H8R	3-state Output Buffer (I <sub>OL</sub> = 3.2 mA) with Noise Limit Resistance and	
	Schmitt Trigger Input Buffer (TTL type, True)	3–430
H8RD	H8R with Pull-down Resistance	
H8RU	H8R with Pull-up Resistance	3–431
H8S	3-state Output Buffer (I <sub>OL</sub> = 3.2 mA) with Noise Limit Resistance and Schmitt Trigger Input Buffer (CMOS type, True)	3–427
H8SD	H8S with Pull-down Resistance	
H8SU	H8S with Pull-up Resistance	
H8T	3-state Output Buffer (I <sub>OL</sub> = 3.2 mA) with Noise Limit Resistance and Input	0 420
	Buffer (True)	3–409
H8TD	H8T with Pull-down Resistance	
H8TF	3-state Output (I <sub>OL</sub> = 8 mA) with Noise Limit Resistance and Input Buffer (True)	
H8TFD	3-state Output (I <sub>OL</sub> = 8 mA) with Noise Limit Resistance and Input Buffer (True) with Pull-down Resistance	3–414
H8TFU	3-state Output (I <sub>OL</sub> = 8 mA) with Noise Limit Resistance and Input	
	Buffer (True) with Pull-up Resistance	3–413
H8TU	H8T with Pull-up Resistance	
W8H	Power 3-state Output Buffer (I <sub>OL</sub> = 12 mA) with Noise Limit Resistance and Input Buffer (True)	
H8WD	H8W with Pull-down Resistance	
H8WU	H8W with Pull-up Resistance	
H8W0	H8W2 with Pull-down Resistance	
H8W1	H8W2 with Pull-up Resistance	
H8W2	High Power 3-state Output Buffer (I <sub>OL</sub> = 12 mA) with Noise Limit	
•	Resistance and Input Buffer (TTL type, True)	3–433
IKB	Clock Input Buffer (Inverter)	
IKBD	IKB with Pull-down Resistance	3–337
IKBU	IKB with Pull-up Resistance	3–336
	Continued on	next page

Name	Function	Page No.
IKC	CMOS Interface Clock Input Buffer (Inverter)	3–338
IKCD	IKC with Pull-down Resistance	3–340
IKCU	IKC with Pull-up Resistance	3–339
ILB	Clock Input Buffer (True)	3–341
ILBD	ILB with Pull-down Resistance	3–343
ILBU	ILB with Pull-up Resistance	3–342
ILC	CMOS Interface Clock Input Buffer (Inverter)	3–344
ILCD	IKC with Pull-down Resistance	3–346
ILCU	IKC with Pull-up Resistance	3–345
I1B	Input Buffer Inverter	3–329
I1BD	I1B with Pull-down Resistance	3–331
I1BU	I1B with Pull-up Resistance	3–330
I1C	CMOS Interface Input Buffer (Inverter)	3–347
I1CD	I1C with Pull-down Resistance	3–349
I1CU	I1C with Pull-up Resistance	3–348
I1R	Schmitt Trigger Input Buffer (TTL Type, Inverter)	3–359
I1RD	I1R with Pull-down Resistance	3–361
I1RU	I1R with Pull-up Resistance	3–360
I1S	Schmitt Trigger Input Buffer (CMOS Type, Inverter)	3–353
I1SD	I1S with Pull-down Resistance	3–355
I1SU	I1S with Pull-up Resistance	3–354
I2B	Input Buffer (True)	3–332
I2BD	I2B with Pull-down Resistance	3–334
I2BU	I2B with Pull-up Resistance	3–333
I2C	CMOS Interface Input Buffer (True)	3–350
I2CD	I2C with Pull-down Resistance	3–352
I2CU	I2C with Pull-up Resistance	3–351
I2R	Schmitt Trigger Input Buffer (TTL Type, True)	3–362
I2RD	I2R with Pull-down Resistance	3–364
I2RU	I2R with Pull-up Resistance	3–363
12\$	Schmitt Trigger Input Buffer (CMOS Type, True)	3–356
I2SD	I2S with Pull-down Resistance	3–358
I2SU	I2S with Pull-up Resistance	
KAB	Block Clock (OR) Buffer	3–114
KBB	Block Clock (OR x 10) Buffer	3–115
K1B	True Clock Buffer	3–109
K2B	Power Clock Buffer	3–110
КЗВ	Gated Clock (AND) Buffer	3–111
K4B	Gated Clock (OR) Buffer	3–112
	Continued	

Name	Function	Page No.
K5B	Gated Clock (NAND) Buffer	<b>3–1</b> 13
LTK	Data Latch	3–265
LTL	1-bit Data Latch with Clear	3–267
LTM	4-bit Data Latch with Clear	3–269
LT1	S-R Latch with Clear	3–272
LT4	4-bit Data Latch	3–274
MC4	4-bit Magnitude Comparator	3–315
NCB	Power 12-Input NAND	3–29
NGB	Power 16-Input NAND	3–30
N2B	Power 2-Input NAND	3–18
N2K	Power 2-Input NAND	3–19
N2N	2-Input NAND	3–17
N2P	Power 2-Input AND	3–49
N3B	Power 3-Input NAND	3–21
N3K	Power 3-input NAND	3–29
N3N	3-Input NAND	3–20
N3P	Power 3-Input AND	3–50
N4B	Power 4-Input NAND	3–24
N4K	Power 4-input NAND	3–25
N4N	4-Input NAND	3–23
N4P	Power 4-Input AND	3–51
N6B	Power 6-Input NAND	3–26
N8B	Power 8-Input NAND	3–27
N8P	Power 8-Input AND	3–52
N9B	Power 9-Input NAND	3–28
O1B	Output Buffer (I <sub>OL</sub> = 8mA, Inverter)	3–365
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Name	Function Page No.
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SFJD	Scan J-K Flip-flop with Clock Inhibit
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### Fujitsu Limited (Japan)

Fujitsu Limited was founded as a telecommunications equipment manufacturer in 1935, and today is not only one of Japan's leading telecommunications companies, but also one of the world's largest computer manufacturers.

This leadership has resulted, at least in part, from the superb quality of the company's semiconductors and electronic components. Manufactured by the company's Electronics Devices Operations Group, these vital electronic devices also contribute to the high reliability and performance of products made by many other manufacturers around the world.

Today, Fujitsu is one of the world's top manufacturers of semiconductors and electronic components. In Japan, Fujitsu's R&D laboratories for semiconductor and electronic components are situated in Kawasaki and Mie, and manufacturing works are located in Iwate, Aizu, Wakamatsu and Suzaka. Fujitsu also has six affiliated manufacturing works in the country. Overseas facilities in the U.S, Europe, and Asia also help to meet the growing global demand for Fujitsu semiconductors and electronic components.

Fujitsu enforces strict quality control at all stages of production, from materials selection through manufacturing to final testing. As a result, Fujitsu's electronic devices are known for their extremely high reliability and excellent cost-to-performance ratio.

Fujitsu manufactures a full line of semiconductors and electronic components to meet the diverse applications of a wide variety of customer. Backed by Fujitsu's extensive R&D commitment equal to over 10 percent of annual sales, Fujitsu's electronic devices stay on the cutting edge of electronics technology.

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### Fujitsu Microelectronics, Inc. (U.S.A.)

Fujitsu Microelectronics, Inc. (FMI), with headquarters in San Jose, California, was established in 1979 as a wholly-owned Fujitsu Limited subsidiary for the marketing, sales, and distribution of Fujitsu integrated circuit and component products. Since 1979, FMI has grown to three marketing divisions, two manufacturing divisions and a subsidiary. FMI offers a complete array of semiconductor products for its customers throughout North and South America.

The Advanced Products Division (APD) is responsible for the complete product development cycle, from design through operations support and worldwide marketing and sales. Products are the result of both internal development and external relationships, such as joint development agreements, technology licenses, and joint ventures. The SPARC™ RISC processor was developed by both APD and Sun Microsystems, Inc.

In addition to designing and selling a full line of SPARC processors and peripheral chips, APD also designed and is selling the EtherStar™ LAN controller — the first VLSI device to integrate both StarLAN™ and Ethernet® protocols into one device. The core of APD's EtherStar chip was the result of APD's cooperative venture with Ungermann-Bass.

The Microwave and Optoelectronics Division (MOD) markets GaAs FETs and FET power amplifiers, lightwave and microwave devices, optical devices, emitters, and SI transistors.

The largest FMI marketing division is the Integrated Circuits Division (ICD) which markets the following standard devices, components, and ASICs.

### **Memory Products**

DRAMS EPROMS EEPROMS NOVRAMS

CMOS masked ROMs CMOS SRAMs BiCMOS SRAMs Bipolar PROMs ECL RAMs

STRAMs (self-timed RAM) Hi-Rel PROMs and SRAMs

Memory cards Memory modules

Continued on next page

Telecommunication Products PLLs

Prescalers

Piezo-electric devices

CODECs VCOs

Telephone ICs Modems

Microprocessor Products 4-bit microcontrollers

DSPs

Logic Products Ultra high-speed ECL/ECL

TTL Translator circuits

Analog Products Linear ICs

**Transistors** 

Hybrid Products Thick- and Thin-film

Custom modules Stepper motor drivers

**Special Purpose Controller** 

**Products** 

SCSI controllers

Serial protocol controllers Video controllers (TV text, CRT, and picture-in-picture)

ASIC Products CMOS gate arrays

ECL gate arrays BiCMOS gate arrays GaAs gate arrays CMOS standard cells

ASIC Gallery™ (SuperMacros™, Compiled Cells)
ASICOpen™ CAD Software Framework (ViewCAD™,
a design and verification tool that integrates with

third-party CAD tools)

Third-party EWS (engineering workstation) support

Customer support and customer training for ASIC products are available through the following FMI design centers:

San Jose Gresham Dallas Chicago Atlanta Boston

Continued on next page

FMI's manufacturing divisions are in San Diego, California and Gresham, Oregon. The San Diego Manufacturing Division assembles and tests memory devices. In 1988, the Gresham Manufacturing Division began manufacturing ASIC products and DRAM memories. This facility, when completed, will have one million square feet of manufacturing—the largest Fujitsu manufacturing plant outside Japan.

FMI's subsidiary, **Fujitsu Components of America**, markets connectors, keyboards, thermal printers, plasma displays, and relays.

### Fujitsu Electronic Devices Europe:

Fujitsu Mikroelektronik GmbH (West Germany) Fujitsu Microelectronics Limited (U.K.) Fujitsu Microelectronics Italia S.R.L (Italy) Fujitsu Microelectronics Ireland, Ltd. (Ireland)

Fujitsu Mikroelektronik GmbH (FMG) was established in June 1980 in Frankfurt, West Germany, as Fujitsu's European headquarters and is a totally owned subsidiary of Fujitsu Limited, Tokyo. Fujitsu Microelectronics Limited (FML) is a sister company based in Maidenhead, England and dedicated to serving the U.K., Ireland, and Scandanavia. Fujitsu Microelectronics Italia (FMIL) is based in Milan, Italy and serves Italy, Spain, Portugal, and the rest of Southern Europe. Together, FMG, FML, and FMIL supply the European market with a full range of semiconductors and electronic components. Sales offices are located in Munich, Frankfurt, Stuttgart, Paris, Eindhoven, Milan, Maidenhead, and Stockholm.

Fujitsu Microelectronics Ireland, Ltd. (FME) was established in 1980, in Dublin, Ireland, as Fujitsu's European Assembly Center for integrated circuits. FME produces DRAMs, EPROMs, and other LSI memory products.

Fujitsu has two European VLSI design centers, both in the U.K. The Manchester Design Centre, in operation since 1983, is equipped with two mainframe computers and linked by satellite to production plants in Japan and the U.S. Staffed with a team of experienced engineers, the center is involved in the design of VLSI standard products, Super Macros, CAD tools and ASICs. In 1990, a second design center was set up in London to deal mainly with the design of telecommunication ICs and mixed analog/digital devices.

### **Fujitsu Worldwide Locations**

Fujitsu also boasts a Euro-wide network of ASIC design centers that are located in Stockholm, Copenhagen, Maidenhead, Paris(2), Eindhoven(2), Frankfurt, Munich(2), Zurich, Milan, and Madrid. Fujitsu has further demonstrated its commitment to the European market by announcing the setting up of a full wafer fabrication plant in Newton Aycliffe in the North of England. The new plant is due to start production of 4 megabyte DRAMs and ASICs in 1991.

The range of semiconductor products offered by FMG, FML, and FMIL for the European market includes:

Memory Products

DRAMS SRAMS EPROMS EEPROMS Mask ROMS Bipolar PROMS Video RAMS ECL RAMS Memory modules Memory cards

**ASIC Products** 

CMOS gate arrays
BiCMOS gate arrays
Bipolar (ECL) gate arrays
Gallium Arsenide gate arrays
CMOS standard cells
ECL gate masterslice devices
Wide range of ASIC design software

**Microprocessor Products** 

4-Bit Microcontrollers

4- 8- and 16-bit F<sup>2</sup>MC™ flexible Microcontrollers

32-Bit SPARC™ RISC microprocessors

32-Bit GMICRO™ TRON-based CISC microprocessors

Hybrid ICs SCSI controllers

**Telecommunication Products** 

Prescalers
PLLs
CODECs
LAN devices
ISDN products
Piezo-electric devices

The range of electronic components offered by FMG, FML, and FMIL is comprised of relays, connectors, keyboards, thermal printers, and plasma displays.

### **Fujitsu Worldwide Locations**

### Fujitsu Microelectronics Asia PTE Ltd. (Singapore)

Fujitsu Microelectronics Asia PTE Ltd. (FMAP) opened in August 1986, in Hong Kong, as a wholly-owned Fujitsu subsidiary for sales of electronic devices to the Asian, Australian, and Southwest Pacific markets. In 1990, FMAP moved to a new location in Singapore.

FMAP offers memory, ASIC, microprocessor, and telecommunication products along with Fujitsu's wide range of electronic components.

SPARO<sup>TM</sup> is a trademark of Sun Microsystems, Inc. Etherneft\* is a registered trademark of Xerox Corporation. EtherStar<sup>TM</sup> is a trademark of Puljitsu Microelectronics, Inc. Start.ANI<sup>TM</sup> is a trademark of AT&T. Genoro I<sup>TM</sup> is a trademark of Hitlach SuperMacro<sup>TM</sup> is a trademark of Fujitsu Microelectronics, Inc. ASICOpen I<sup>TM</sup> is a trademark of Fujitsu Microelectronics, Inc. ViewCAD<sup>TM</sup> is a trademark of Fujitsu Microelectronics, Inc.

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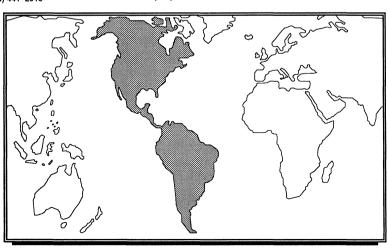
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## Δ

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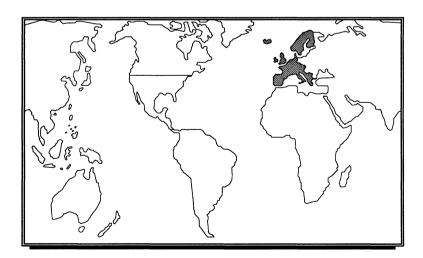
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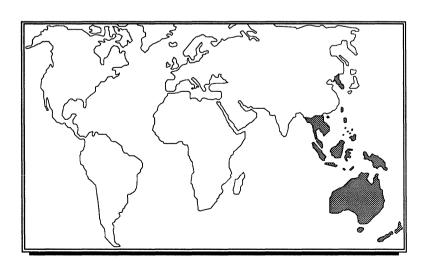
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