CTμL9956

DUAL 2-INPUT BUFFER

COMPLEMENTARY TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

+15°C TO +55°C TEMPERATURE RANGE

GENERAL DESCRIPTION — The CTμL 9956 dual 2-input power AND gate is a low impedance non-inverting level setting circuit intended to drive high fanout, and may be used as a 50Ω line driver. The input threshold and output levels are compatible with any other CTμL elements. The output of the CTμL 9956 may be tied with any other CTμL element to perform the wired OR function.

CTμL 9956 is packaged in the versatile Jedec TO-116 Dual In-Line Package* which is a hermetically sealed ceramic package intended for low cost insertion techniques.

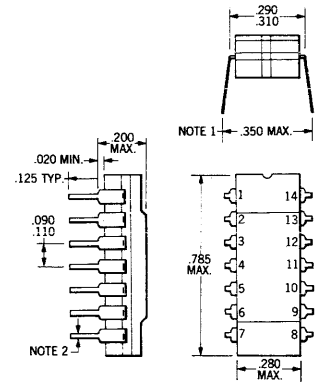
CTμL 9956 is designed to operate over a commercial ambient temperature range of +15 to +55°C. Power supplies are 4.5 volts ± 10% and −2 volts ± 10%. Typical power dissipation per gate is 60 mW and is designed to increase with fanout. Typical propagation delay 14 ns.

*Fairchild patent pending.

PHYSICAL DIMENSIONS

TYPICAL DUAL IN-LINE PACKAGE

In Accordance With
JEDEC (TO-116) Outline

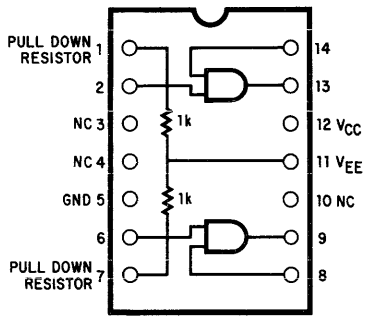


NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

FEATURES:

- Power Supplies are +4.50 V ±10% and −2.00 V ±10%.
- High Fan-Out Capability . . . 25.
- Two Optional Pull Down 1.0 k Resistors for Optimum Speed.
- Low Power Dissipation.
- Low Propagation Delay.
- Logic Swing of 3.0 V.

CONNECTION DIAGRAM



TOP VIEW

PURCHASING INFORMATION

- Use the ten letter code U6A995679X for ordering purposes.
- All units are marked CTμL 995679 and date code, unless otherwise specified.

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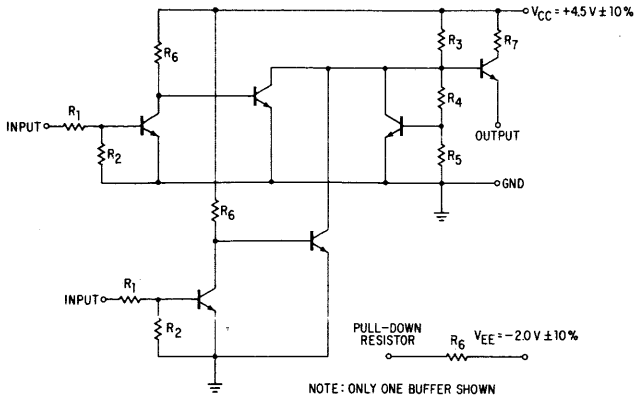
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD COMPLEMENTARY TRANSISTOR MICROLOGIC® IC

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

Maximum Current in or out of a Pin	100 mA
Maximum Chip Temperature	150°C
Maximum Power Dissipation	1.0 Watt
Maximum Voltage Applied to any Input Pin	10 Volts
Maximum Negative Voltage Applied to any Input Pin	−4.0 Volts
Maximum Voltage Applied to Output Pin	6.0 Volts

DC TESTS

TEST (at T_A = 25°C)	LIMITS				CONDITIONS			
	MIN.	TYP.	MAX.	UNITS	V_{CC}	V_{EE}	LOAD TO V_{EE}	COMMENTS
ONE Level Output	2.25	2.60		Volts	4.05	Note 1	[2]F.O. = 25	Inputs simultaneously to 1.25 V
ONE Level Output	2.46			Volts	4.95	Note 1	F.O. = 1	Inputs simultaneously to 1.25 V
ONE Level Output		2.70	3.20	Volts	4.95	Note 1	Internal 1 k	Inputs simultaneously to 3.5 V
ZERO Level Output		−0.45	−0.36	Volts	4.05	−1.8 V	F.O. = 1	Inputs to 0.8 V sequentially, unused input to 3.5 V
Input Current		5.30	6.40	mA	4.05	Note 1	No Load	Inputs to 3.5 V simultaneously, guarantees input loading ≤ 1.5 AND-OR gate loads
Input Pull Down Resistor	0.8	1.0	1.2	kΩ	4.05	−2.2 V	No Load	3.5 V applied to pull down resistor
Positive Supply Current			69.2	mA	4.95	−2.2 V	No Load	One input to 3.5 V, other inputs to GND.
Output Rising Delay, t_{dr}		12.0	18.0	ns	4.50	Note 1	F.O. = 25	See t_{pd} test circuit, page 4
Output Falling Delay, t_{df}		12.0	18.0	ns	4.50	Note 1	F.O. = 25	See t_{pd} test circuit, page 4

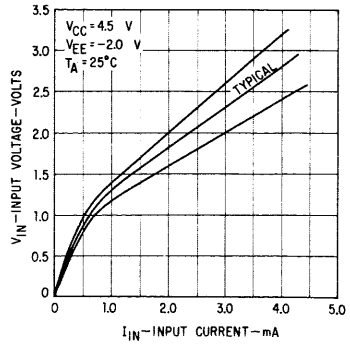
NOTES:

(1) Value of V_{EE} is non-critical: $-2.20\ V \leq V_{EE} \leq -1.80\ V$

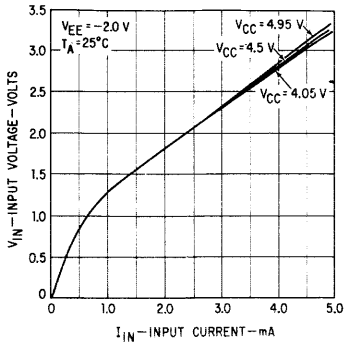
(2) F.O. = Fan Out; F.O. = 25 equivalent to 64 Ω to −2.20 V under worst case conditions
F.O. = 1 equivalent to 2.4 kΩ to −1.80 V under worst case conditions

INPUT CHARACTERISTICS

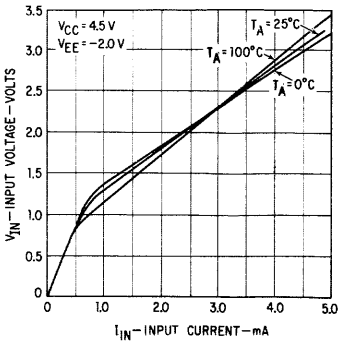
TOLERANCE VARIATION OF PARAMETERS



AS A FUNCTION OF POSITIVE SUPPLY VOLTAGE

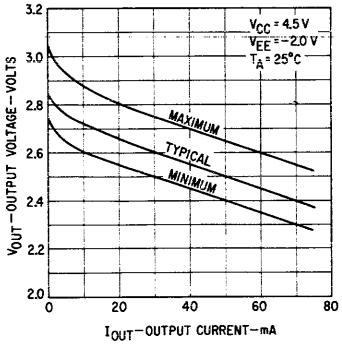


AS A FUNCTION OF TEMPERATURE

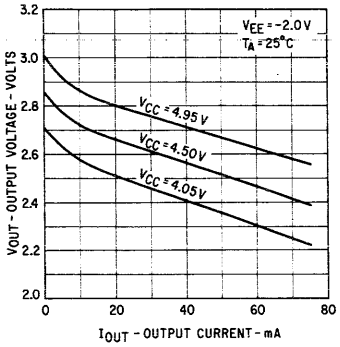


OUTPUT CHARACTERISTICS

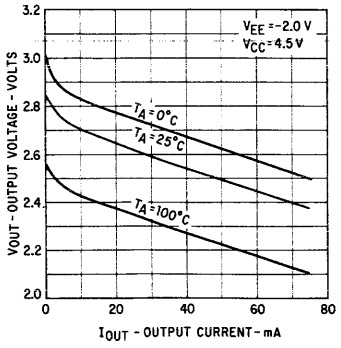
TOLERANCE VARIATION OF PARAMETERS



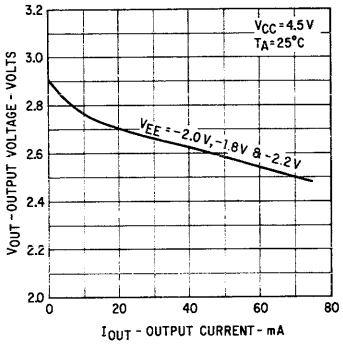
AS A FUNCTION OF POSITIVE SUPPLY VOLTAGE



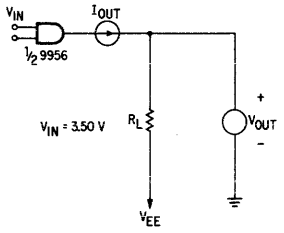
AS A FUNCTION OF TEMPERATURE



AS A FUNCTION OF NEGATIVE SUPPLY VOLTAGE

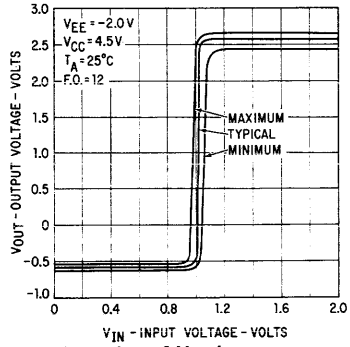


SCHEMATIC DIAGRAM



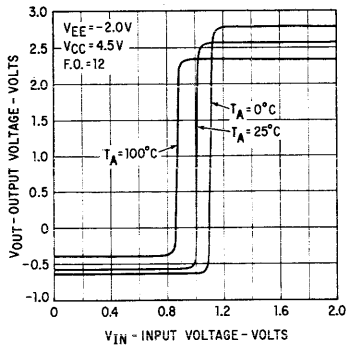
TRANSFER CHARACTERISTICS

TOLERANCE VARIATION OF PARAMETERS

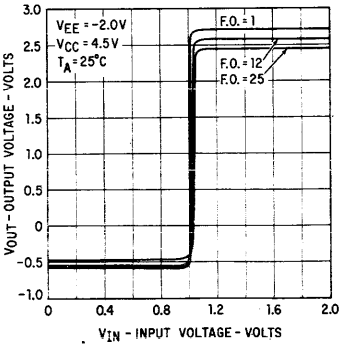


NOTE: Variation of V_{EE} does not alter transfer characteristics.

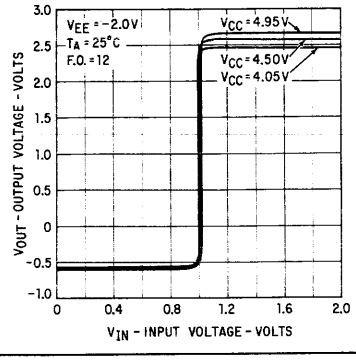
AS A FUNCTION OF TEMPERATURE



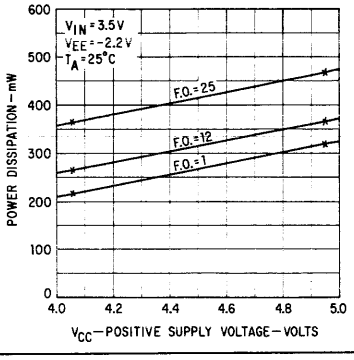
AS A FUNCTION OF FAN-OUT



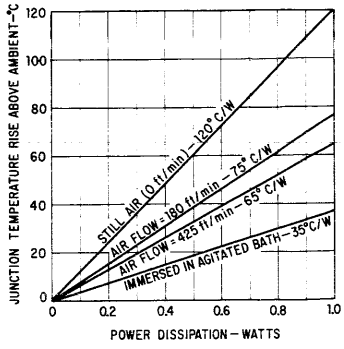
AS A FUNCTION OF POSITIVE SUPPLY VOLTAGE



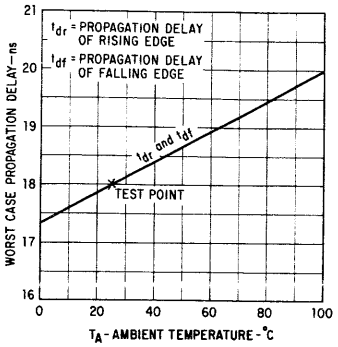
WORST CASE POWER DISSIPATION VERSUS POSITIVE SUPPLY VOLTAGE



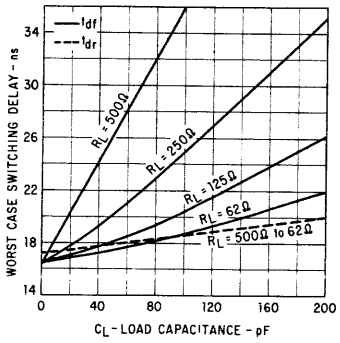
WORST CASE JUNCTION TEMPERATURE VERSUS POWER DISSIPATION



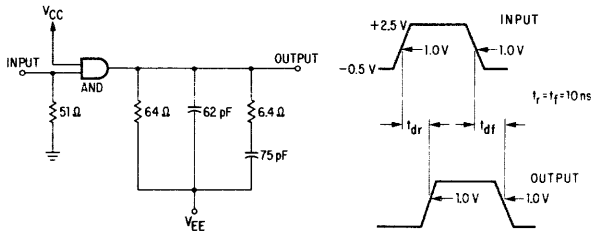
WORST CASE PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE



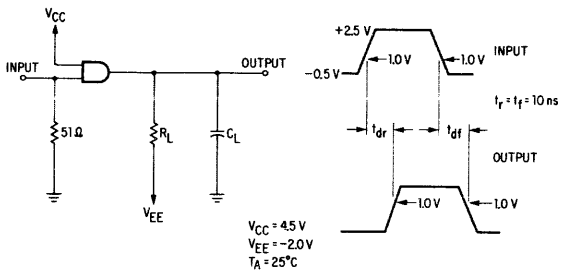
WORST CASE PROPAGATION DELAY VERSUS LOAD CAPACITANCE AS A FUNCTION OF LOAD RESISTANCE



t_{PD} TEST CIRCUIT



t_{PD} TEST CIRCUIT FOR ABOVE



APPLICATION INFORMATION

The electrical specification tests are performed under conditions chosen to emphasize the worst case results and could be considered as conservative limits. The output ONE level at worst case is guaranteed to drive a fanout of 25 AND-OR gates. The maximum input current assures that 9956 input presents a load of not more than 1.5 AND-OR gate input.

INTERFACING — The CTμL 9956 buffer could serve as an excellent interfacing link between external signals coming from other logic forms or peripheral equipments and the CTμL Family logic.

PULL DOWN RESISTORS — Two pull down 1 kΩ resistors are built into the package with one end tied to the negative power supply (V_{EE}). When the 9956 input is driven by a single AND-OR gate, the 1 kΩ resistors should be connected to the same input pin. This will improve the 9956 output rise and fall time. The pull-down resistor may be also connected to the CTμL 9956 output, which will improve the output falling delay when the fanout is low.

LINE DRIVER — The CTμL 9956 could be used as a line driver. To drive a 50 Ω line, a 68 Ω resistor should be connected from the output to ground. This will reduce the fanout capability by 15.

WIRED-OR — A powerful feature of the CTμL 9956 Buffer is that the output may be tied together with the output of any other element in the CTμL family to form the positive OR function at the tie point. When two or more CTμL 9956 outputs are tied for the OR function, a pull-down resistor must be used.

UNUSED INPUTS — Unused inputs to the AND-OR Gate will effectively inhibit the gate output, and therefore, must be tied to the most positive voltage level. The unused input may be tied directly to $+V_{CC}$ or through a resistor not greater than 600 Ω. Tying an unused input to an active input is not recommended.

SHORT CIRCUIT PROTECTION — The CTμL 9956 Gate output is protected by a limiting resistor at the output and may sustain prolonged short circuit to ground at V_{CC} not greater than 5 volts. Excessive destructive heat may develop when more than one output in a single package is short circuited to ground. Short circuiting the output to the −2 volts supply should be avoided.

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