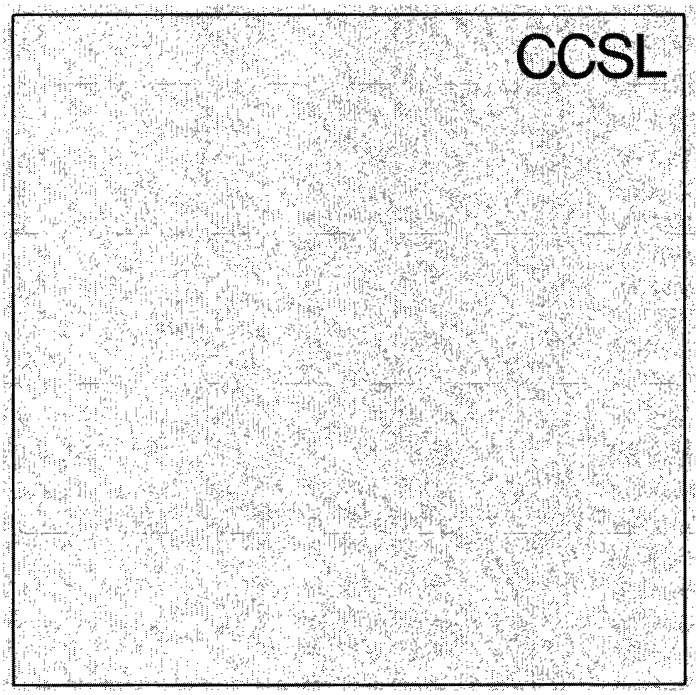

CCSL

COMPATIBLE CURRENT SINKING LOGIC NUMERICAL INDEX

CROSS REFERENCE — CCSL AND SPECIAL CIRCUITS

Function	LPDTμL Typ Tpd 65 MHz	DTμL Typ Tpd 25 MHz	TTμL Typ Tpd 10 MHz	CCSL MSI	HLLDTμL	RTμL Typ Tpd 15 MHz	LPRTμL Typ Tpd 40 MHz	MμL	CTμL Typ Tpd 3.0 MHz	CμL	Special
Gate											
Hex Inverter NAND Gate	F, D	F, D, C	FP, F, D		D						
Quad 2-input NAND Gate	F, D	F, D, C	FP, F, D								
Triple 3-input NAND Gate	F, D	F, D, C	FP, F, D								
Dual 4-input NAND Gate	F, D	F, D, C	FP, F, D								
8-input NAND Gate			FP, F, D								
Dual 2-wide Expandable AND/NOR Gate			F, FP, D								
4-wide Expandable AND/NOR Gate			F, FP, D								
Dual 4-input Power Gate	F, C, D	F, C, D	F, FP, D								
3-input NOR Gate						C, F					
4-input NOR Gate						C, F	C				
Dual 2-input NOR Gate						C, F, E	C		D		
Dual 3-input NOR Gate						C, F					
Quad Inverter NOR Gate						C, F					
2-2-3 Input AND Gate									D		
Dual 4-input AND Gate									D		
Dual Output, 8 Input AND Gate									D		
3-3-1 Input AND Gate									D		
Quad 1 AND Gate									D		
3 Output Quad 2 Input AND/OR Gate									D		
2 Output Quad 2 Input AND/OR Gate									D		
Buffer						C, FP, E	C		D		
Dual 2 Input									D		
Dual Buffer							C				
Counter Adapter						F, C					
Decoders						**Typ Tpd 10 MHz**			**Typ Tpd 25 MHz**	**Typ Tpd 2 MHz**	
1 of 10 Decoder				F, D							
1 of 16 Decoder				F, D							
7 Segment Decoder				F, D							
Multiplexers											
Dual 4-input Multiplexer				F, D							
8-input Multiplexer				F, D							
Dual 8-input Multiplexer				F, D							
Counters											
BCD Up/Down Counter				F, D							
Decade Counter				F, D							
Hexidecimal Counter				F, D							
Hexidecimal Up/Down Counter				F, D							
Registers											
4 Bit Shift Register				F		D					
Dual 8 Bit Shift Register				D							
Adders & Comparators											
Dual Full Adder				F, D							
Dual Four-bit Comparator				F, D							
Half Adder						F, C	C				
Adder							C				

Legend: F = Flat Pak FP = Fairpak® D = Dip C = TO - 5 E = TO - 5 Epoxy

CROSS REFERENCE — CCSL AND SPECIAL CIRCUITS

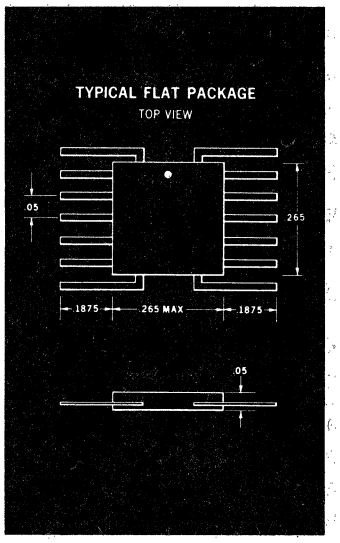
Function	LPDTμL Typ Tpd 65 MHz	DTμL Typ Tpd 25 MHz	TTμL Typ Tpd 10 MHz	CCSL MSI	HLLDTμL	RTμL Typ Tpd 15 MHz	LPRTμL Typ Tpd 40 MHz	MμL	CTμL Typ Tpd 3.0 MHz	CμL	Special
Memory & Latches											
Dual 4 Input Latch				F, D							
16-bit Memory Cell				F, D							
256 Bit ROM				F, D							
Dual 4-bit Latch									D		
Buffer Memory										D	
Decimal DEC/DR										D	
Micromatrices											
32 Gate Customizable Array		F, D									
48 Gate Customizable Array			F, D								
96 Gate Customizable Array			F, D								
Kit Parts											
4501		D									
4522			D								
Gate Expanders	**Typ Tpd 130 MHz**	**Typ Tpd 20 MHz**	**Typ Tpd 25 MHz**			**Typ Tpd 30 MHz**	**Typ Tpd 20 MHz**		**Typ Tpd 15 MHz**		
Expander	F, C, D	F, C, D	FP, F, D				C				
Binary Elements											
RS Flip Flop							C				
Buffered JK Flip Flop	F, D	F, C, D	FP, F, D			F, C, E	C		D		
Dual Flip Flop		F, D	FP, F, D								
AC Coupled Flip Flop		F, C, D									
Type D Flip Flop							C				
Dual Rank Flip Flop									D		
One Half Shift Register With Inverter						F, C					
One Half Shift Register Without Inverter						F, C					
Interface Functions		**Typ Tpd 100 MHz**									**Typ Tpd 2 MHz**
Line Receiver											F, D
Line Driver											F, D
CCSL to MOS											F, D
MOS to CCSL											F, D
Multivibrators											
AC Coupled One Shot		F, C, D									
Retriggerable One Shot			F, D								

Legend: F = Flat Pak FP = Fairpak® D = Dip C = TO - 5 E = TO - 5 Epoxy

DTμL COMPOSITE DATA SHEET

DIODE-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

Diode Transistor Micrologic (DTμL) is the first diode transistor logic circuit expressly designed for integrated circuit technology. As a consequence, DTμL requires only one power supply, which may vary over a wide range without impairing circuit performance. High tolerance to electrical noise, along with ample drive capability is characteristic. Indeed, the designer may exchange one for the other to strike the balance most appropriate to the situation at hand. DTμL is completely characterized and specified over the entire military temperature range of -55°C to +125°C.



CONTENTS OF THIS SPECIFICATION

The optimum operating supply voltage for the full military temperature range is 5.0 volts. The data of this specification enumerated on pages 2 and 3 and the loading rules on page 8 are valid for supply voltages ranging from 4.5 to 5.5 volts. Power dissipation may be reduced by using V_{CC} = 4 V without sacrificing noise immunity or speed if operating temperature is held to a minimum of -20 C, or if fanout is restricted. The Fairchild epitaxial integrated circuit process also permits an operating supply voltage of 6.0 volts over the full temperature range with a slight decrease in fanout or noise immunity at temperatures in excess of 100 C. (See page 8).

For guidance, when designing outside the limits guaranteed by the tests given on pages 2 and 3, graphs of minimum and maximum limits of circuit operation are shown on Pages 6 and 7. These graphs will permit the designer to optimize fanout, noise immunity, supply voltage and temperature for the specific application. Examples using these graphs are given on Page 7.

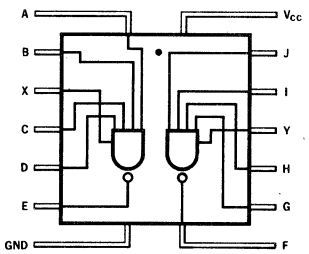
Very extensive noise threshold and propagation delay data are given in the individual DTμL 930 and 931 specification sheets (available on request). Additional propagation delay data is given on Pages 4 and 5 of this specification. Specific characteristics of the Dual Buffer and the Dual Power Gate may be found in the individual DTμL 932 and DTμL 944 specification, while data concerning the effects of input extension appear in the individual DTμL 933 specification.

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Supply Voltage (V_{CC}), -55°C to +125°C, continuous		+8 Volts
Supply Voltage (V_{CC}), pulsed, <1sec		+12 Volts
Output Current, into outputs	DTμL 932, 944	100 mA
Output Current, into outputs	DTμL 930, 931, 946, 962	30 mA

Input Forward Current	-10 mA
Input Reverse Current	1 mA
Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C

DTμL 930 DUAL GATE
DTμL 932 DUAL BUFFER
DTμL 944 DUAL POWER GATE

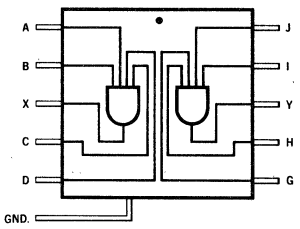


POSITIVE (NAND) LOGIC

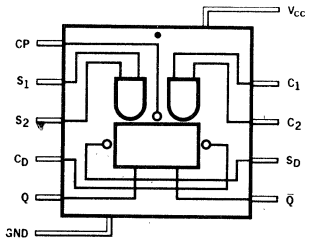
$E = \overline{A \cdot B \cdot C \cdot D \cdot (X)}$

$F = \overline{G \cdot H \cdot I \cdot J \cdot (Y)}$

DTμL 933 DUAL EXTENDER



DTμL 931 CLOCKED FLIP-FLOP



J-K MODE TRUTH TABLE

t_n		t_{n+1}
S_2	C_2	Q
0	0	Q_n
0	1	0
1	0	1
1	1	Q_n

R-S MODE TRUTH TABLE

t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	Undetermined

X - Either a one or a zero can be present

"1" more positive than "0"

For J-K Mode Operation:
Connect S_1 to $\overline{Q}$ and C_1 to Q

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

TEST SEQUENCES — DTμL ELEMENTS 930, 931, 932, 933

Abbreviated Test Sequences for the DTμL family of elements are shown below. The ground pin is grounded on all tests. Page 3 of this composite gives a glossary of terms used, tables of test conditions and limits, and LTPD percentages by group.

DTμL 930 & 932 ELEMENTS

NOTE: Both elements are dual "NAND" gates; therefore, the test sequences for each are identical. Tests on each side of the dual are identical; therefore, matching test and pin numbers are shown in parentheses.

Test No.	LTPD** Group	Notes	FORCING CONDITIONS: Pin A (G)	Pin B (H)	Pin C (I)	Pin D (J)	Pin X (Y)	Pin E (F)	V_{CC}	Sense	LIMITS: Min.	Max.
1, (2)	A		V_{IH}	V_{IH}	V_{IH}	V_{IH}		I_{OL}	V_{CCL}	V_E (V_F)		V_{OL}
3, 4, 5, 6 (7, 8, 9, 10)	B	1, 3	V_{IL}	V_{IL}	V_{IL}	V_{IL}		I_{OH}	V_{CCL}	V_E (V_F)	V_{OH}	
11, (12)	C		V_R	GND	GND	GND			V_{CCH}	I_A I_G		I_R
13, (14)	C		GND	V_R	GND	GND			V_{CCH}	I_B I_H		I_R
15, (16)	C	3	GND	GND	V_R	GND			V_{CCH}	I_C I_J		I_R
17, (18)	C	3	GND	GND	GND	V_R			V_{CCH}	I_D I_J		I_R
19, (20)	D		V_F	V_R	V_R	V_R			V_{CCH}	I_A (I_G)		I_F
21, (22)	D		V_R	V_F	V_R	V_R			V_{CCH}	I_B (I_H)		I_F
23, (24)	D	3	V_R	V_R	V_F	V_R			V_{CCH}	I_C (I_I)		I_F
25, (26)	D	3	V_R	V_R	V_R	V_F			V_{CCH}	I_D (I_J)		I_F
27, (28)	C		GND					V_{CEX}	V_{CEX}	I_E (I_F)		I_{CEX}
29, (30)	B	2	GND					GND	V_{CCH}	I_E (I_F)	I_{SC}	I_{SC}
31	E								V_{PD}	I_{VCC}		I_{PDH}
32	E		GND						V(max)	I_{VCC}		I(max)
33, (34)	E	3					V_X	I_{OH}	V_{CCL}	V_E (V_F)	V_{OH}	
35, 36	F	t_{pd+}, t_{pd-} — See table of test circuit conditions and limits, Page 3.										

NOTES: 1. V_{IL} applied individually to 1 input each test. Other inputs open. 2. I_{SC}(max) only for 930; I_{SC}(min) only for 932. ** See LTPD group, Page 5.

3. Delete these tests for 10-pin TO-5 package: 6, 9, 10, 16, 17, 18, 24, 25, 26, 33.

DTμL 931 ELEMENT

Test No.	LTPD** Group	Notes	FORCING CONDITIONS: CP	C_1	C_2	S_1	S_2	C_D	S_D	Q	$\bar{Q}$	V_{CC}	Sense	LIMITS: Min.	Max.
1	C		V_R	GND	GND	GND	GND					V_{CCH}	I_{CP}		I_{RCP}
2, 3, 4, 5	C	1	GND	V_R	V_R	V_R	V_R					V_{CCH}	I_{C_1}, I_{C_2}, I_{S_1}, I_{S_2}		I_R
6, 7, 8, 9	D	3		V_F	V_F	V_F	V_F					V_{CCH}	I_{C_1}, I_{C_2}, I_{S_1}, I_{S_2}	2/3 I_F	
10, 25	D	2	CP, b		V_{IL}		V_{IL}					V_{CCH}	I_{CP}		I_{FCP}
11, 12	B	2	CP, a	V_{IL}	V_{IL}	V_{IH}	V_{IH}			*I_{OH}		V_{CCL}	V_Q	V_{OH}	
13, 14	B	2	CP, a	V_{IH}	V_{IH}	V_{IL}	V_{IL}				*I_{OH}	V_{CCL}	V_Q	V_{OH}	
15	A		CP, c	GND						*	I_{OL}	V_{CCL}	V_Q		V_{OL}
16	A		CP, c			GND				I_{OL}	*	V_{CCL}	V_Q		V_{OL}
17	E		GND	GND	GND	GND	GND					V(max)	I_{VCC}		I(max)
18	E											V_{PD}	I_{VCC}		I_{PDH}
19	B		CP, a			GND	GND	V_{IH}	V_{ILS}	I_{OH}		V_{CCL}	V_Q	V_{OH}	
20	B		CP, a	GND	GND			V_{ILS}	V_{IH}		I_{OH}	V_{CCL}	$V_{\bar{Q}}$	V_{OH}	
21	C		CP, a			GND	GND	V_R				V_{CCH}	I_{CD}		I_R
22	C		CP, a	GND	GND				V_R			V_{CCH}	I_{SD}		I_R
23	D				*		GND	V_F	GND		GND	V_{CCH}	I_{CD}		I_{FS}
24	D				GND			GND	V_F	GND		V_{CCH}	I_{SD}		I_{FS}
25, 26	F	t_{pd+}, t_{pd-} — See table of test circuit conditions and limits, Page 3.													

NOTES: 1. V_R applied individually to 1 input each test. Other inputs open. 2. V_{IL} applied individually to 1 input each test. Other inputs open. 3. V_F applied individually to 1 input each test. Other inputs open. * Momentary Ground. ** See LTPD group, page 5.

DTμL 933 ELEMENT

Test No.	LTPD** Group	Notes	FORCING CONDITIONS: Pin A (G)	Pin B (H)	Pin C (I)	Pin D (J)	Pin X (Y)	Sense	LIMITS: Min.	Max.
1, 2, 3, 4 (5, 6, 7, 8)	B	1	GND	GND	GND	GND	I_{FD}	V_X (V_Y)	V_{FD}	V_{FD}
11, (12)	A		V_R	GND	GND	GND		I_A (I_G)		I_R
13, (14)	A		GND	V_R	GND	GND		I_B (I_H)		I_R
15, (16)	A		GND	GND	V_R	GND		I_C (I_I)		I_R
17, (18)	A		GND	GND	GND	V_R		I_D (I_J)		I_R
19, (20)	A						V_R	I_X (I_Y)		5 I_R

NOTE 1. GND applied individually to 1 input each test. Other inputs open. ** See LTPD group, page 5.

GLOSSARY OF TERMS USED WITH DTμL

In General, Subscripts are used as follows:

- O = output
- I = input
- R = reverse, applying to high inputs.
- F = forward, applying to low inputs.
- L = low, applying to a low signal level or when used with V_{CC} to low V_{CC} value.
- H = high, applying to a high-signal level or when used with V_{CC} to high V_{CC} value.

Non-operational Terms:

- V(max) = Maximum rated V_{CC} pin voltage.
- I(max) = Maximum rated current into V_{CC} pin, with V(max) applied.
- V_{PD} = V_{CC} pin voltage applied during power dissipation test.
- I_{PD} = Current into V_{CC} pin with V_{PD} applied. I_{PDL} means gate or buffer inputs are low or 931 clock pin input is low. I_{PDH} means the inputs are high.
- V_R = Input reverse (high) voltage for input diode leakage test.
- I_R = Reverse input diode current with V_R applied to input.
- I_{RCP} = Reverse 931 clock pin input leakage current with V_R applied to input.
- V_{CEX} = Output transistor collector to emitter voltage. With output pull-up resistor connected, $V_{CEX} = V_{CC}$ to avoid drop across output pull-up resistor.

Operational Terms:

- V_{IL} = Input low (threshold) voltage.
- V_{OL} = Output low voltage, with rated fanout current I_{OL} into output.
- I_{CEX} = Output transistor collector to emitter leakage current with V_{CEX} applied to output.
- V_{FD} = Forward diode drop in 933 Element.
- I_{FD} = Forward diode current in 933 Element.
- V_{IH} = Input high (threshold) voltage.
- V_{OH} = Output high voltage, with high output current (I_{OH}) flowing out of output.
- V_F = Forward (low) input voltage, for forward input current (I_F) test. V_F is usually ground.
- I_F = Forward input diode current, for unit input load. Also shown will be 2/3 I_F, I_{FCP}, and I_{FS}.
- I_{OL} = Output low current.
- I_{OH} = Output high current, flowing out of output in V_{OH} test.
- I_{SC} = Short circuit output current to ground, with one or more inputs low. I_{SC} minimum confirms output ability to pull up capacitive loads; I_{SC} maximum confirms subtraction of fanout rules when "OR"ing outputs.
- V_{CCL} = Low V_{CC} pin voltage. Used for V_{OL} (I_{OL}) and V_{OH} (I_{OH}) tests.
- V_{CCH} = High V_{CC} pin voltage. Used for V_{IF} - I_F input forward diode current tests.
- CP_x = Clock Pin, pulsed. The subscript if any refers to pulse waveshape. Used in testing binary elements. (See page 5).
- $V_{CP\,TH}$ = Input Clock Pin threshold voltage (low). With Clock Pin at or below $V_{CP\,TH}$, the 931 "master" Flip-Flop holds the proper "slave" (output) Flip-Flop output high.
- V_X = Input low (threshold) voltage extendable inputs.

TABLE OF CONDITIONS & LIMITS, TPD TESTS (See Test Circuits, Page 5)

(V_{CC} = 5 V, T = 25°C)

		R	C_2	Min.	Max.
t_{pd+}	930	3.9 K	30 pf	25 nsec	80 nsec
t_{pd-}	930	400 Ω	50 pf	10 nsec	30 nsec
t_{pd+}	932	510 Ω	500 pf	25 nsec	80 nsec
t_{pd-}	932	150 Ω	500 pf	15 nsec	40 nsec
t_{pd+}	930	400 Ω	50 pf	15 nsec	40 nsec[1]
t_{pd-}	930	3.9 K	20 pf	5 nsec	20 nsec[1]
t_{pd+}	932	150 Ω	500 pf	20 nsec	65 nsec[1]
t_{pd-}	932	510 Ω	200 pf	8 nsec	30 nsec[1]

(V_{CC} = 5 V, T = 25°C)

		R	C_2	Min.	Max.
t_{pd+}	931	3.9 K	30 pf	35 nsec	75 nsec
t_{pd-}	931	400 Ω	30 pf	35 nsec	75 nsec
t_{pd+}	931	400 Ω	30 pf	20 nsec	50 nsec[1]
t_{pd-}	931	3.9 K	30 pf	30 nsec	70 nsec[1]

NOTE 1: Correlating limit provided as design information only.

TABLE OF TEST LIMITS

		-55°C		+25°C		+125°C	
	Units	Min.	Max.	Min.	Max.	Min.	Max.
V_{OL}	Volts		.40		.40		.45
V_{OH}	Volts	2.5		2.6		2.5	
I_R	μA		2.0		2.0		5.0
I_{RCP}	μA		20.0		20.0		30.0
1 I_F	mA		-1.60		-1.60		-1.50
2/3 I_F	mA		-1.07		-1.07		-1.00
I_{FCP}	mA		-3.4		-3.40		-3.00
I_{CEX}	μA				50.0		
I_{SC} 930	mA		-1.34	-.60	-1.34		-1.30
I_{SC}(min) 932	mA	-16.		-18.		-16.	
V_{FD}	Volts	.85	.98	.70	.82	.50	.65
I(max) 930	mA				5.50		
I(max) 931	mA				14.5		
I(max) 932	mA				6.0		
I_{PDH} 930	mA				6.50		
I_{PDH} 931	mA				11.0		
I_{PDH} 932	mA				26.6		
5 I_R	μA		10.0		10.0		25.
I_{FS}	mA		-1.20		-1.20		-1.10

TABLE OF FORCING CONDITIONS

	Units	-55°C	+25°C	+125°C		Units	-55°C	+25°C	+125°C		Units	-55°C	+25°C	+125°C
V(max)	Volts	--	8	--	V_{CEX}	Volts		4.5		I_{OL} 932	mA	34	36	32
V_{PD}	Volts	--	5	--	I_{OH}	mA	-.12	-.12	-.12	I_{OH} 932	mA	-2.0	-2.5	-4.0
V_{CCH}	Volts	5.5	5.5	5.5	I_{OL} 930	mA	11.4	12.0	10.8	V_{HL}	Volts	1.4	1.10	.80
V_{CCL}	Volts	4.5	4.5	4.5	I_{FD}	mA	2	2	2	V_{IH}	Volts	2.1	1.9	1.7
V_R	Volts	4.0	4.0	4.0	V_{ILS}	Volts	1.40	1.10	.80	$V_{CP\,TH}$	Volts	1.10	.95	.75
V_F	Volts	0	0	0	I_{OL} 931	mA	10.0	10.6	9.5	V_X	Volts		1.80	

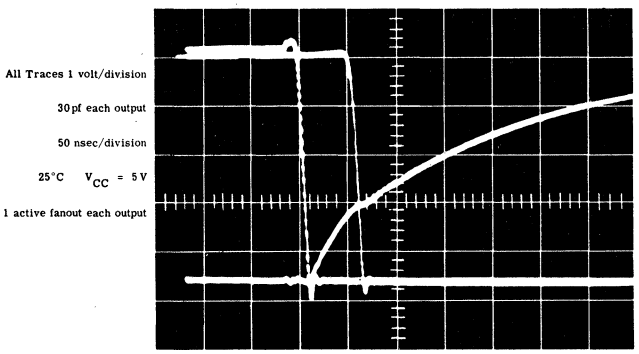
ADDITIONAL DELAY TIME CHARACTERIZATION INTO CAPACITIVE LOADS

The individual specifications on DTμL 930 and DTμL 931 give extensive delay characterizations as functions of V_{CC}, temperature, fanout and ratio of active to inactive fanout. For each fanout, active or inactive, 5 pf wiring capacity was added. This page will show the effects of greater wiring capacities.

Most delay attributable to capacitive loads is associated with the positive going output. Two R-C time constants are seen in the positive going output, as shown in the pictures below. In the 1st time period, from the saturated low level to threshold, the R of the R-C time constant can be given by 6 KΩ in parallel with $\frac{3.75\,K\Omega}{\text{active fanout}}$. Above the threshold which occurs at about 1.4 to 1.5 volts at 25°C, the R of the 2nd R-C time constant is 6 KΩ and the rate of the voltage rise above threshold is slow. The logic signal propagates through at the threshold level; so voltage rise above threshold does not affect speed. By noting that both rise domains drive toward V_{CC}, the voltage rise waveform may be calculated. DTμL 930, 932, 933, and 931 inputs (except CP) are ~ 2 pf per input for active or inactive fanout; the remaining capacitance is from board, wiring, and connectors.

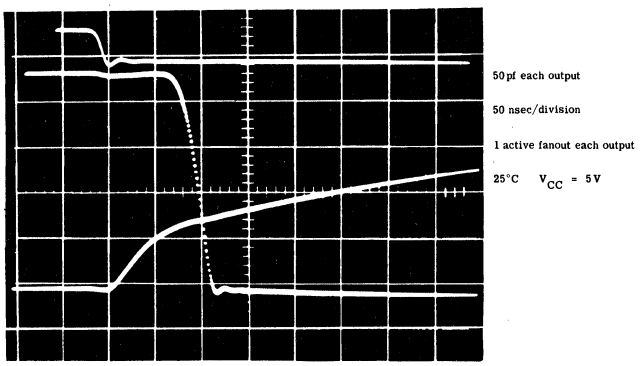
The t_{pd} average curves, with 1 active fanout, Fig. 1 below, and the typical maximum toggling frequency curve, Fig. 2, give the prediction of capacitive effects on switching speeds. For frequency division or ripple carry counting, use of 3 KΩ external resistors tied from output to V_{CC} in the least significant bit will increase the maximum frequency. In Fig. 1 each output has 1 active fanout, which is worst case.

DTuL 930 — INVERTER PAIR DELAY



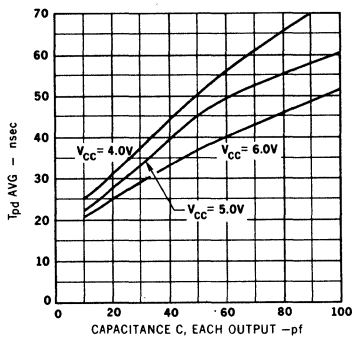
1st Negative Going Trace - Input to 1st Gate
Positive Going Trace - Output of 1st Gate = Input to 2nd Gate
2nd Negative Going Trace - Output of 2nd Gate

DTuL 931 — DIVIDING BY 2



Upper Trace - Input to CP (5 volts/division)
Positive Going Trace - Output Going High (1 volt/division)
Negative Going Trace - Output Going Low (which starts Going low as the positive Going Trace reaches threshold) (1 volt/division).

FIG. 1
T_{pd} AVERAGE VS. CAPACITY (DTμL 930, 25°C)



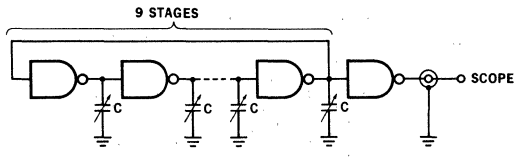
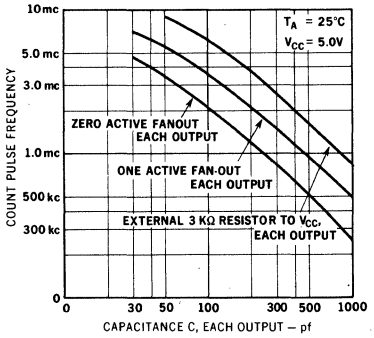
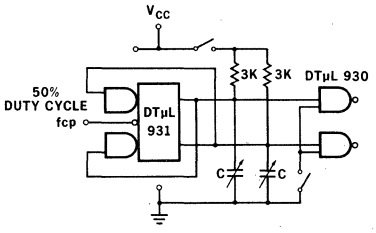


FIG. 2
TYPICAL MAXIMUM BINARY COUNTING RATE VS. CAPACITY





DT μL 930 TIME DELAYS VS. CAPACITIVE LOADS

FIG. 3

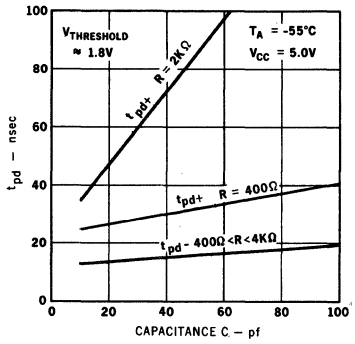


FIG. 4

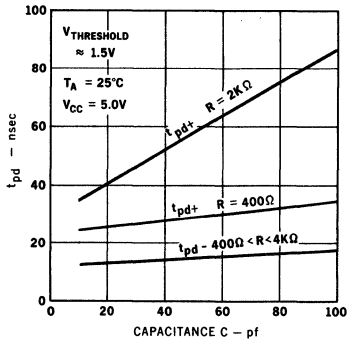
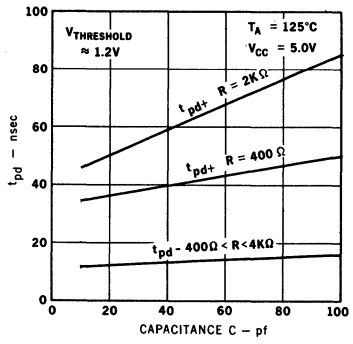
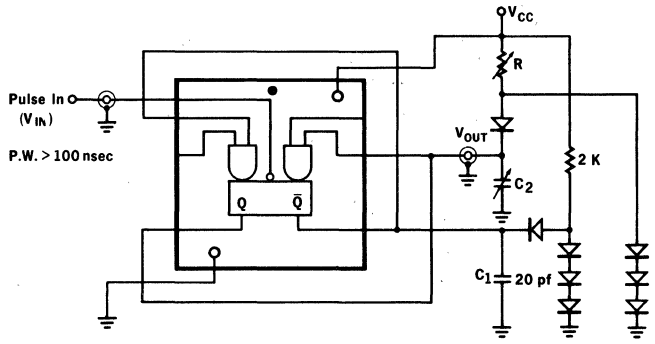


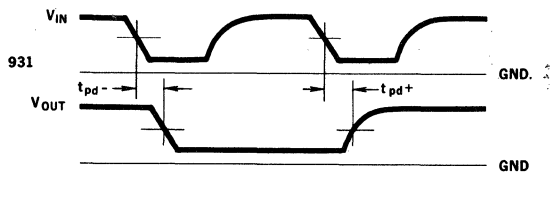
FIG. 5



t_{pd} test circuit for 930 & 932 used (see below)

Tpd TEST CIRCUIT DTuL 931

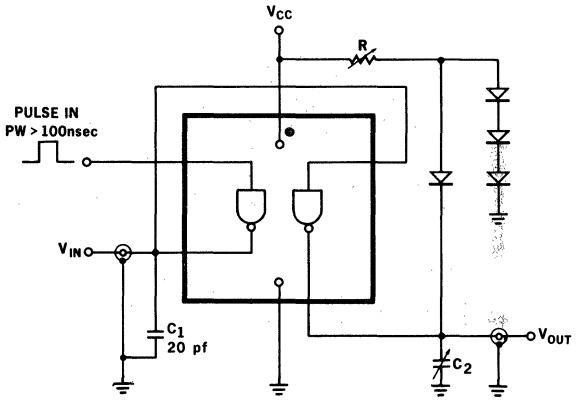


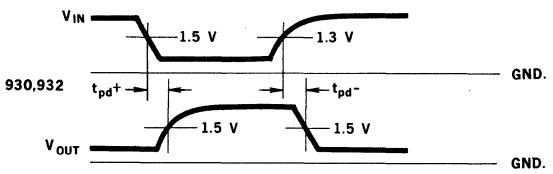


C_1 and C_2 includes probe and jig capacitance

$V_{Threshold}$ = 1.5 V at 25°C; at other temperatures $V_{Threshold}$ will be stated.

Tpd TEST CIRCUIT DTuL 930, 932





T_{pd} - of 930, 932, and 946 elements will be read from input at 1.3 V.

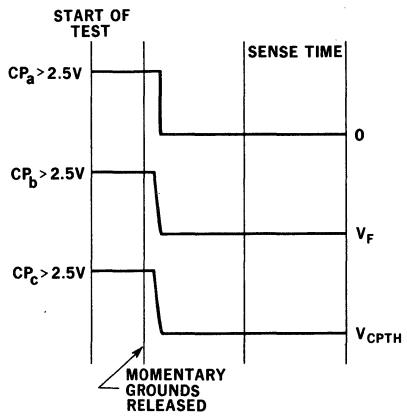
All diodes FD600 or equivalent.

TABLE OF LTPD's

(These apply to the test sequence on page 2)

Group	-55°C	+25°C	+125°C
A	15%	10%	15%
B	-	10%	15%
C	-	10%	15%
D	-	10%	15%
E	-	10%	15%
F	-	10%	-

CLOCK PIN WAVEFORMS
(For 931 Test Sequence, Page 2)



MINIMUM-MAXIMUM DC CURVES I_F VS. V_F & V_{CC}

FIG. 1
-1 I_F DTμL 930, 932, 944, 946, 962
MAXIMUM VS. TYPICAL
(V_F = 0V & V_F = .750V T_A = −55°C & +25°C)

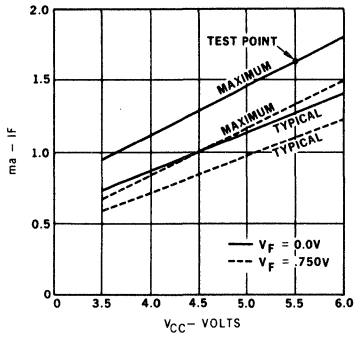
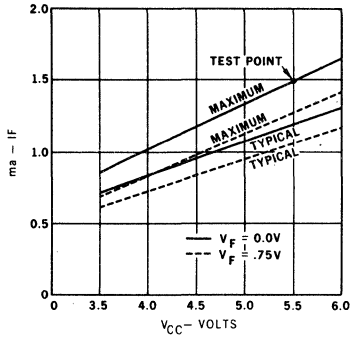


FIG. 2
-1 I_F DTμL 930, 932, 944, 946, 962
MAXIMUM VS. TYPICAL
(V_F = 0V & V_F = .750V T_A = +125°C)



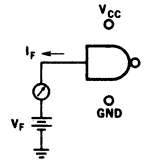
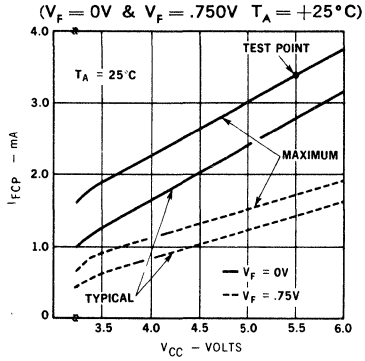
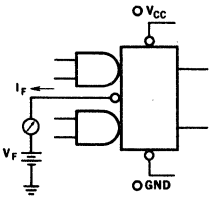


FIG. 3
I_{FCP} DTμL 931
MAXIMUM VS. TYPICAL
(V_F = 0V & V_F = .750V T_A = +25°C)



Note that with V_F = 0 and Inputs S_1, S_2, C_1, and C_2 at V_{OL}, I_{FCP} current is summed through three diodes—both input AND Gate diodes and one of the Clock-coupling transistor emitters. As the Clock Pin voltage (V_F) rises to approach V_{OL}, current starts to flow into one of pins S_1, S_2, C_1, or C_2 (since all of these pins high is not an allowed logic state). Also when the collector of the Clock-coupling transistor rises (the collector is at V_{CE}(sat) + V_F), current flows into the low output of the cross-connected output Flip-Flop. Therefore, I_{FCP} equal to 2 I_F is a conservative rating and test current is much higher than will flow "in use."



OUTPUT LOW CURRENT VS. V_{CC} OR V_{OL} FOR 930 AND 931 ELEMENTS

FIG. 4
I_{OL} VS. V_{CC}
(T_A = +25°C, V_{OL} = .400V)

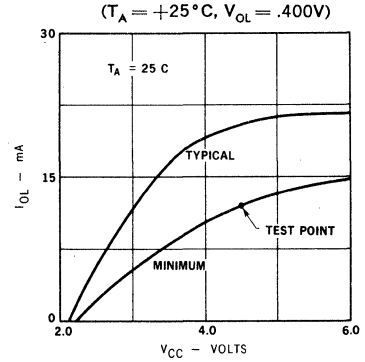


FIG. 5
I_{OL} VS. V_{CC}
(T_A = −55°C, V_{OL} = .400V)

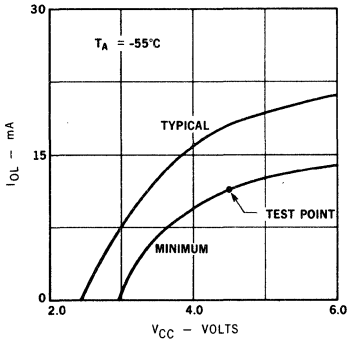
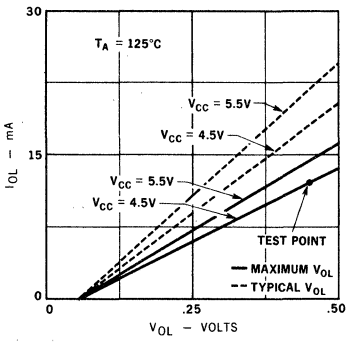
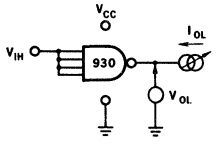
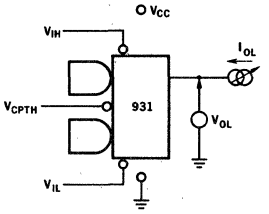


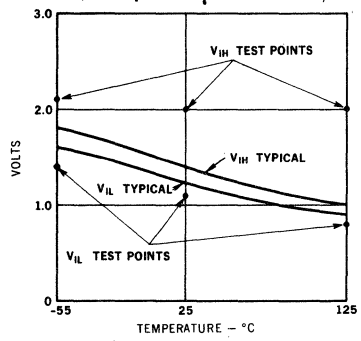
FIG. 6
I_{OL} VS. V_{OL} VS. V_{CC}
TYPICAL VS. MAXIMUM (T_A = +125°C)



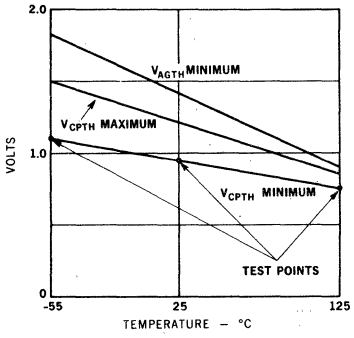




DT μL INPUT THRESHOLDS VS. TEMPERATURE (except DT μL 931 CP)



DT μL CLOCK PIN THRESHOLDS VS. TEMPERATURE



DEFINITIONS OF 931 CLOCK PIN THRESHOLDS

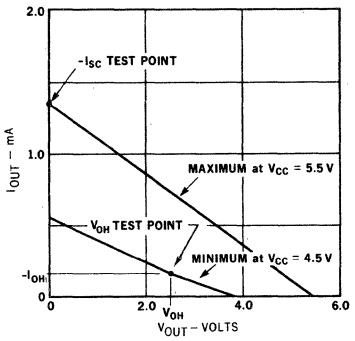
$V_{AG\,TH}$(min) With CP at or above $V_{AG\,TH}$(min), the clocked inputs will control the state of the "master" Flip-Flop, with V_{CC} and clocked inputs worst case.

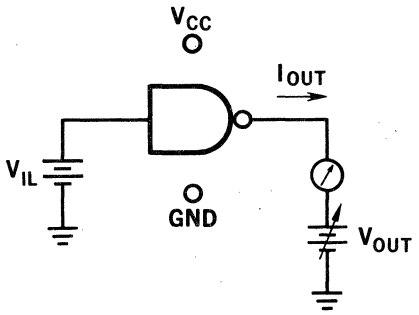
$V_{CP\,TH}$(min) With CP at or below $V_{CP\,TH}$(min), the "master" Flip-Flop will control the output Flip-Flop, with V_{CC} and outputs worst case.

$V_{CP\,TH}$(max) With CP at or above $V_{CP\,TH}$(max), the "master" Flip-Flop will not control the output Flip-Flop, with V_{CC} and outputs worst case.

OUTPUT CURRENT VS. OUTPUT VOLTAGE FOR DTμL 930 AND 931 ELEMENTS

FIG. 9

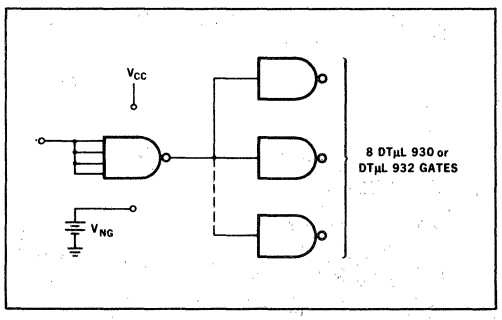




EXAMPLES OF USES FOR THE MINIMUM–MAXIMUM DC CURVES (Pages 6 & 7)

EXAMPLE 1.

A low DTμL 930 output at -55°C fans out to 8 inputs of DTμL 930 or 932. V_{CC} = 5 V. Positive DC ground noise (V_{NG}) of 350 mV is applied to the 1st 930. Its output may thus rise to .75 Volt (V_{NG} + V_{OL}). 4.65 Volts (V_{CC} - V_{NG}) remain from V_{CC} pin to ground pin; this is above V_{CCL} = 4.50 V, and test I_{OL} is conservative. Maximum current flowing in each input of the 8 930/932's is given by Fig. 1 on Page 4 with V_F = 0.75 V and V_{CC} = 5 V; the current (I_F) is less than 1.25 mA and total current ($\leq$8 x 1.25 = 10 mA) is less than the I_{OL} test current used at -55°C to saturate the low output. Above the 350 mV of V_{NG} already applied, the difference between the common node voltage ($\leq$.75 V) and the low input threshold (V_{IL} = 1.40 V) of the 8 930/932's is still $\geq$350 mV, allowing for signal noise to be superposed above ground noise.



EXAMPLE 2.

The I_F and I_{OL} curves on Page 6 may be expressed in analytical form, as follows

$$I_F \text{ (930 and 932)} \leq \frac{V_{CC} - V_F - V_{FD}}{3\,K\Omega} \quad T_A < 25°C$$

For T_A greater than 25°C, the 3 KΩ rises by 0.12%/°C to approximately 3.36 KΩ at +125°C. V_{FD} is the temperature dependent silicon forward diode drop and is about 0.70 V at 25°C and 1 mA. $\Delta V_{FD}/°C$ is roughly 1.8 mV/°C.

The ratio of I_{OL}, on 930 and 931 (Figs. 4, 5, and 6) at V_{CC} below test V_{CC}, to I_{OL} at test V_{CC} can be given by

$$\frac{I_{OL} \text{ @ } -55°C}{\text{Test } I_{OL} \text{ @ } V_{CCL} = 4.5\,V} \geq \frac{V_{CC} - 3.0\,V}{4.5\,V - 3.0\,V}$$

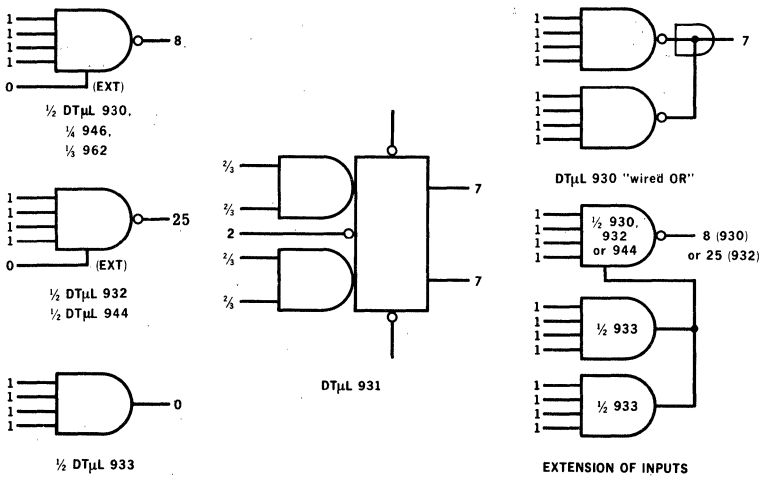
and by

$$\frac{I_{OL} \text{ @ } 25°C}{\text{Test } I_{OL} \text{ @ } V_{CCL} = 4.5\,V} \geq \frac{V_{CC} - 2.3\,V}{4.5\,V - 2.3\,V}$$

Since, at 25°C, $I_{OL} \geq$ 12 mA at V_{CCL} = 4.5 V is guaranteed by the Page 2 and 3 specifications, I_{OL} at V_{CC} pin to GND pin voltage of 3.6 V is $\left(\frac{3.6 - 2.3}{4.5 - 2.3}\right)$12 mA = 7.1 mA.

The similar expression for the 932 gives a very conservative value due to the phase splitter gain. Above V_{CCL}, I_{OL} is limited by V_{OL} with an essentially resistive $\left(\frac{V_{OL}}{I_{OL}} \text{ saturation resistance}\right)$ slope. Fig. 6 at +125°C shows this, with V_{CC} having relatively small effect.

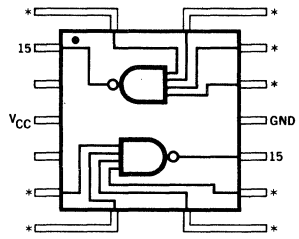
SUGGESTED INPUT–OUTPUT LOADING FACTORS



The number of elements that may be driven by an output terminal may consist of any combination of elements whose summation of input loading does not exceed the output terminal driving capability.

RULES FOR USE OF TTμL 103 AND 104 WITH DTμL

($4V < V_{CC} < 6V$)



* = 2 input loads for fan-in = 1 to DTμL output driver.
* = 3 input loads for fan-in ≥ 2 to DTμL output driver.
* = 1 input load to TTμL output driver.

These input loads are primarily determined by inverse beta leakage at the TTμL inputs at +125°C. For special cases where improved loading rules may be required, please consult the Fairchild Sales representative.

The TTμL makes an excellent output interface driver for DTμL. TTμL outputs can be tied thru external loads to 8 or 10 V separate voltage supplies, to obtain output levels up to 6 or 8 volts.

MISCELLANEOUS RULES

1. Outputs of DTμL 930 may be tied together for the "wired OR" function ($\overline{ABCD \cdot GHIJ} = \overline{ABCD} + \overline{GHIJ}$). Subtract 1 unit fanout for each added gate. Subtract 5 fanouts for six added gates.

2. Outputs of DTμL 932 may not be tied together for the "wired OR" function.

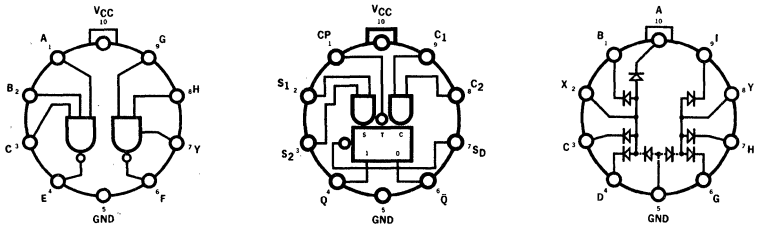
3. Extension of inputs with the DTμL 933 does not affect quiescent loading of the supplemented element (DTμL 930 or 932). However, capacitance due to wiring to the DTμL 933 will affect noise tolerance and propagation delay, and thus establish a fanin limit for the particular application. Please refer to the typical curves on the DTμL 933 Dual Extender Element preliminary specifications.

4. For operation with a nominal supply voltage of 4.0 volts from -55°C to +125°C, reduce element fanout as follows: DTμL 930 = 5, DTμL 931 = 5, DTμL 932 = 18. If temperature is maintained above -20°C, no fanout reduction is necessary.

5. For operation with a nominal supply voltage of 6.0 volts from -55°C to +125°C, reduce element fanout as follows: DTμL 930 = 6, DTμL 931 = 6, DTμL 932 = 20. If ambient temperature remains below +100°C or if worst case Noise Threshold is considered to be 250 mV, no fanout reduction is necessary. Except as noted, these rules apply over the entire military temperature range with a supply voltage of 4.5 to 5.5 volts. These rules also permit a 50°C temperature differential between individual elements. These rules guarantee a worst case signal-line or ground Noise Threshold of at least 350 mV. Practical Noise Thresholds exceed 500 mV.

6. All rules for DTμL 930 apply to DTμL 946 and DTμL 962.

10 LEAD TO–5 PACKAGE PIN LOCATIONS



DTμL 930 DUAL GATE
DTμL 932 DUAL BUFFER
DTμL 944 DUAL POWER GATE

DTμL 931
CLOCKED FLIP-FLOP

DTμL 933
DUAL EXTENDER

PURCHASING INFORMATION

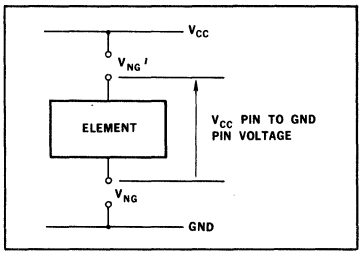
9YXXX5Z

Y = 1 for 14 pin CERPAK
Y = 5 for 10 pin TO-5
XXX = 930
931
932
933
Z = 1 for -55°C to +125°C operation

(cont'd)

EXAMPLE 3.

The test sequences on Page 2 and tables of conditions and limits on Page 3 use two values of V_{CC}, V_{CCL} and V_{CCH}. With a nominal 5 volts V_{CC}, for example, and assuming $\Delta V_{CC} = \pm .2$ V, testing at $V_{CCL} = 4.5$ V and $V_{CCH} = 5.5$ V allows simulation of ±0.3V ground noise V_{NG} or V_{CC} line noise V_{NG}'. Since there is gain associated with V_{NG} (refer to DTμL 930 and 931 specifications), particularly at lower temperatures and V_{CC} values; the test guarantees of output low current and voltage are the worst case test conditions to simulate worst case ground noise. Much better numbers could be shown, for example, in the ratio of output current to input current (I_{OL}/I_F) if both I_{OL} and I_F were measured at identical V_{CC} values and if input current was sunk into $V_F = V_{OL}$, the worst case low output level, or even into $V_F = V_{IL}$, the input threshold value. However, the test values would then guarantee only signal line noise immunity, where there is no gain associated with V_{NS}. By use of the Minimum/Maximum DC curves on Page 6 or by the Example 2 equations, limits for the single V_{CC} testing approach could be recovered. More important, each design or components engineer can develop the fanout, power, and noise margin tradeoffs for this unique application.



DTμL 932 DUAL BUFFER ELEMENT
DTμL 944 DUAL POWER GATE ELEMENT
DIODE TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

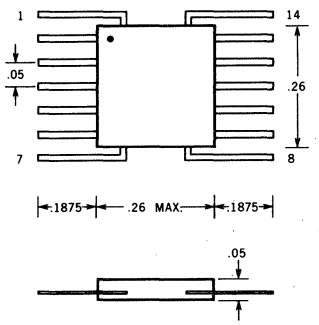
GENERAL DESCRIPTION - The DTμL 932 Dual Buffer Element and the DTμL 944 Dual Power Gate Element are dual 4-input inverting drivers for use with the Fairchild Diode-Transistor Micrologic Family or any similar DTL logic circuits. The fan-in of either element may be extended with the use of the DTμL 933 Element. Input thresholds and currents are the same as other DTμL gate elements.

Both DTμL 932 and DTμL 944 Elements have typical saturation resistances of 5 ohms which allow output currents of up to 100 mA. The DTμL 932 features an emitter-follower output pull-up, which provides a high fan-out device with superior capacitance-driving capability.

The DTμL 944 features an output with no internal pull-up. Thus, 944 outputs may be tied together for the "wired-OR" function, or may drive inputs with logic thresholds of 4 to 6 volts. The 944 is intended as a high fan-out gate interface driver, or low-power lamp driver. An external pull-up resistor may return to the nominal DTμL V_{CC} supply of 5 volts or to other supplies up to 12 volts. These supplies may be located near the output or at the far end of an open transmission line or twisted pair interconnection.

Complete test specifications, typical and worst-case DC curves, t_{pd} curves, and suggested loading rules are included in these specifications.

TYPICAL FLAT PACKAGE
TOP VIEW

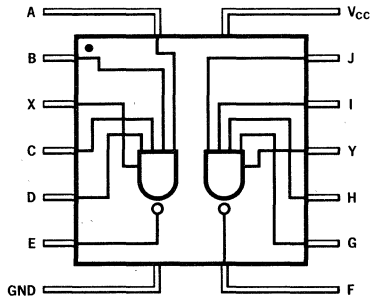


PART NO's
9X93251—932 ELEMENT
9X94451—944 ELEMENT
X = 3 CERPAK
X = 5 10 PIN TO-5

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Supply Voltage (V_{CC}), -55°C to +125°C, Continuous	+8.0 Volts	Input Reverse Current	5.0 mA
Supply Voltage (V_{CC}), pulsed, < 1.0 sec.	+12 Volts	Operating Ambient Temperature	-55°C to +125°C
Output Current, into Outputs, Continuous	150 mA	Storage Temperature	-65°C to +150°C
Output Current, into Outputs, pulsed, <30 milliseconds	300 mA	Operating Junction Temperature (See note A on page 2)	+175°C Maximum
Input Forward Current	-10 mA		

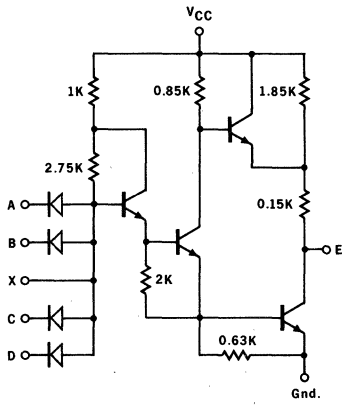
LOGIC DIAGRAM (TOP VIEW)



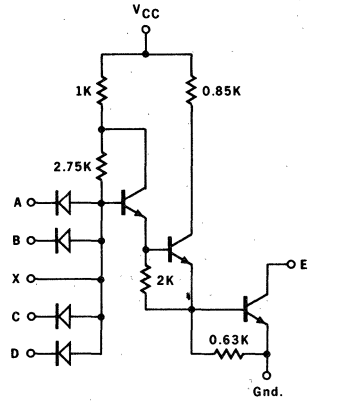
POSITIVE (NAND) LOGIC
$E = \overline{A \cdot B \cdot C \cdot D \cdot (X)}$
$F = \overline{G \cdot H \cdot I \cdot J \cdot (Y)}$

NEGATIVE (NOR) LOGIC
(symbol not shown)
$E = \overline{A+B+C+D+(X)}$
$F = \overline{G+H+I+J+(Y)}$

SCHEMATIC DIAGRAM OF THE DTμL 932 ELEMENT
(ONE SIDE ONLY)



SCHEMATIC DIAGRAM OF THE DTμL 944 ELEMENT
(ONE SIDE ONLY)



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TEST SEQUENCE DTμL 932 AND DTμL 944 ELEMENTS

NOTE: Both elements are dual "NAND" gates; therefore, the test sequences for each are identical. Tests on each side of the dual are identical; therefore, matching test and pin numbers are shown in parentheses.

Test No.	LTPD Group	Notes	Pin A (G)	Pin B (H)	Pin C (I)	Pin D (J)	Pin X (Y)	Pin E (F)	V_{CC}	Sense	Limits Min.	Limits Max.
1, (2)	A		V_{IH}	V_{IH}	V_{IH}	V_{IH}		I_{OL}	V_{CCL}	$V_E(V_F)$		V_{OL}
3, 4, 5, 6, (7, 8, 9, 10)	B	1,3	V_{IL}	V_{IL}	V_{IL}	V_{IL}		I_{OH}	V_{CCL}	$V_E(V_F)$	V_{OH}	
11, (12)	C		V_R	GND	GND	GND			V_{CCH}	$I_A(I_G)$		I_R
13, (14)	C		GND	V_R	GND	GND			V_{CCH}	$I_B(I_H)$		I_R
15, (16)	C		GND	GND	V_R	GND			V_{CCH}	$I_C(I_I)$		I_R
17, (18)	C		GND	GND	GND	V_R			V_{CCH}	$I_D(I_J)$		I_R
19, (20)	D		V_F	V_R	V_R	V_R			V_{CCH}	$I_A(I_G$		I_F
21, (22)	D		V_R	V_F	V_R	V_R			V_{CCH}	$I_B(I_H)$		I_F
23, (24)	D		V_R	V_R	V_F	V_R			V_{CCH}	$I_C(I_I)$		I_F
25, (26)	D		V_R	V_R	V_R	V_F			V_{CCH}	$I_D(I_J)$		I_F
27, (28)	C	3	GND					V_{CEX}	V_{CEX}	$I_E(I_F)$		I_{CEX}
29, (30)	B	2,3	GND					GND	V_{CCH}	$I_E(I_F)$	I_{SC}	
31	E								V_{PD}	I_{VCC}		I_{PDH}
32	E	2	GND						$V_{(max)}$	I_{VCC}		$I_{(max)}$
33, (34)	E	3					V_X	I_{OH}	V_{CCL}	$V_E(V_F)$	V_{OH}	
35, 36	F		t_{pd+}, t_{pd-} See Table of test circuit conditions and limits.									
35, 36, 37, 38 (39, 40, 41, 42)	B	1,4	V_{IL}	V_{IL}	V_{IL}	V_{IL}		V_{CEX}	V_{CCH}	$I_E(I_F)$		I_{CEX}
43, (44)	B	4					V_X	V_{CEX}	V_{CCH}	$I_E(I_F)$		I_{CEX}
45, (46)	B	4	GND					I_{CE}	V_{CCH}	$V_E(V_F)$	LV_{CE}	

NOTES:
(1) V_{IL} applied individually to 1 input each test. Other inputs open.
(2) Apply GND to both pins A and G.
(3) DTμL 932 only.
(4) DTμL 944 only.
(5) On 10 Pin TO-5 units, pins D, X, I and J are omitted. Thus tests 6, 9, 10, 16, 17, 18, 24, 25, 26, 33, 38, 41, 42 and 43 do not apply.

TEST LIMITS—DTμL 932 AND DTμL 944

	Units	-55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max
V_{OL}	Volts		0.4		0.4		0.45
V_{OH}	Volts	2.6		2.5		2.5	
I_R	μA		2.0		2.0		5.0
1 I_F	mA		-1.6		-1.6		-1.5
I_{CEX}932	μA		50				
I_{SC}(min)932	mA	-16		-18		-16	
$I_{(max)}$932&944	mA				6.0		
I_{PDH}944	mA				20		
I_{PDH}932	mA				26.6		
I_{CEX}944	mA		0.05		0.1		0.2
LV_{CE}944	Volts				6.0		

CONDITIONS AND LIMITS, t_{pd} TESTS

(V_{CC} = 5.0 V, T_A = 25°C)

		R	C_2	Min.	Max.	
t_{pd+}	944	510 Ω	20 pF	15 ns	50 ns	
t_{pd-}	944	150 Ω	100 pF	10 ns	35 ns	
t_{pd+}	932	510 Ω	500 pF	25 ns	80 ns	
t_{pd-}	932	150 Ω	500 pF	15 ns	40 ns	
t_{pd+}	944	150 Ω	20 pF	10 ns	35 ns	(Note 1)
t_{pd-}	944	510 Ω	20 pF	5.0 ns	20 ns	(Note 1)
t_{pd+}	932	150 Ω	500 pF	20 ns	65 ns	(Note 1)
t_{pd-}	932	510 Ω	200 pF	8.0 ns	30 ns	(Note 1)

NOTE: Correlating limit provided as design information only.

FORCING CONDITIONS

	Units	-55°C	+25°C	+125°C
$V_{(max)}$	Volts	--	8.0	--
V_{PD}	Volts	--	5.0	--
V_{CCH}	Volts	5.5	5.5	5.5
V_{CCL}	Volts	4.5	4.5	4.5
V_R	Volts	4.0	4.0	4.0
V_F	Volts	0	0	0
V_{CEX}	Volts	4.5	4.5	4.5

	Units	-55°C	+25°C	+125°C
I_{OL}944	mA	36	40	36
I_{OL}932	mA	34	36	32
I_{OH}932	mA	-2.0	-2.5	-4.0
V_{IL}	Volts	1.4	1.1	0.8
V_{IH}	Volts	2.1	1.9	1.7
V_X	Volts		1.8	
I_{CE}944	mA		5.0	

NOTE A:
Allow 200°C/Watt θ_{J-A} for TO-5; 300°C/Watt θ_{J-A} for cerpak. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for cerpak. Heat removal in cerpak is highly dependent upon contact surfaces or air flow and on lead attachment and Thermal paths thru leads, as well as number of soldered leads.

MINIMUM/MAXIMUM AND TYPICAL DC CURVES

FIG. 1. $-1\ I_F$ DTμL932, 944 MAXIMUM VS. TYPICAL ($T_A = -55°C$ & $+25°C$)

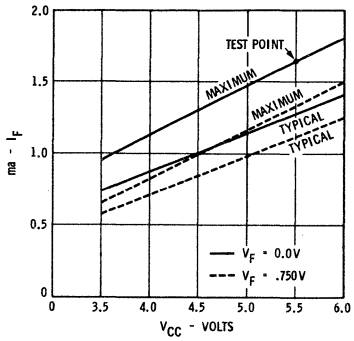


FIG. 2. DTμL INPUT THRESHOLDS VS. TEMPERATURE (932, 944)

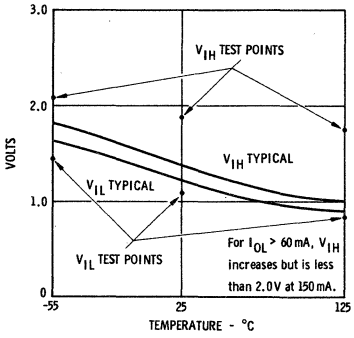


FIG. 3. TYPICAL POWER DISSIPATION PER SIDE VS. SUPPLY VOLTAGE (OUTPUT NOT LOADED) (932, 944)

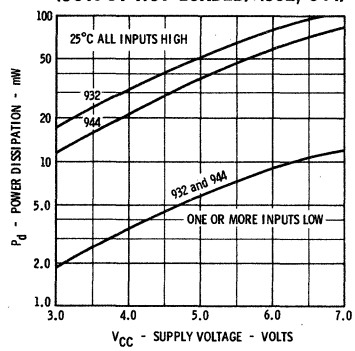


FIG. 4. TYPICAL OUTPUT CURRENT WITH INPUTS LOW (932)

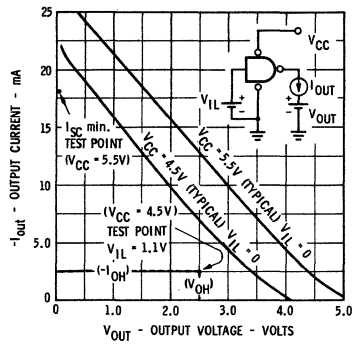


FIG. 5. TYPICAL OUTPUT LOW CURRENT VS. SUPPLY VOLTAGE (−55°C and +25°C) (932)

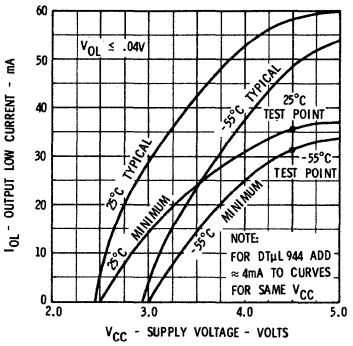


FIG. 6. TYPICAL OUTPUT LOW CURRENT VS. OUTPUT VOLTAGE (932)

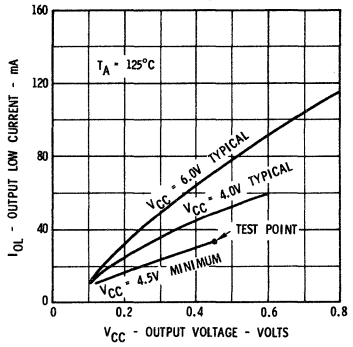
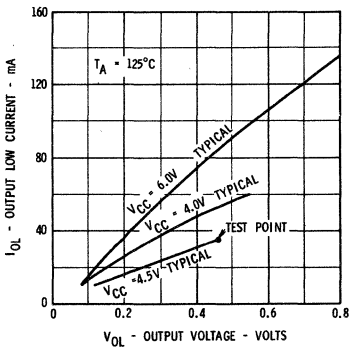


FIG. 7. TYPICAL OUTPUT LOW CURRENT VS. OUTPUT VOLTAGE (944)



t_{pd} CURVES

FIG. 8. TYPICAL $t_{pd}-$ VS. CAPACITY (932, 944)

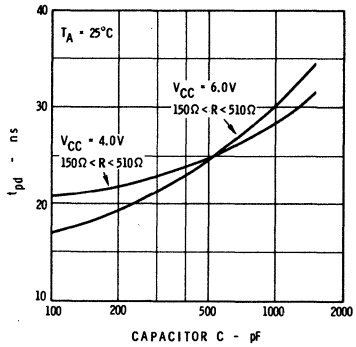


FIG. 9. TYPICAL $t_{pd}+$ VS. CAPACITY (944)

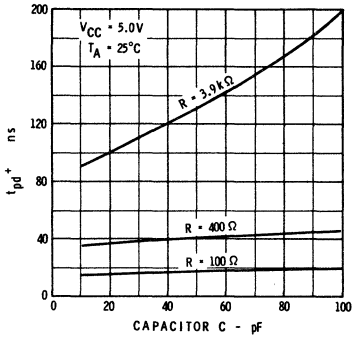
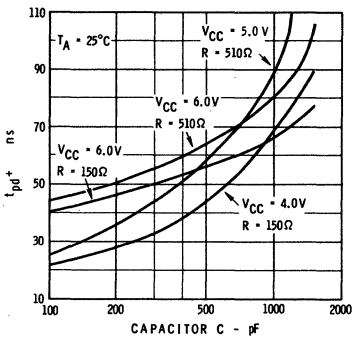
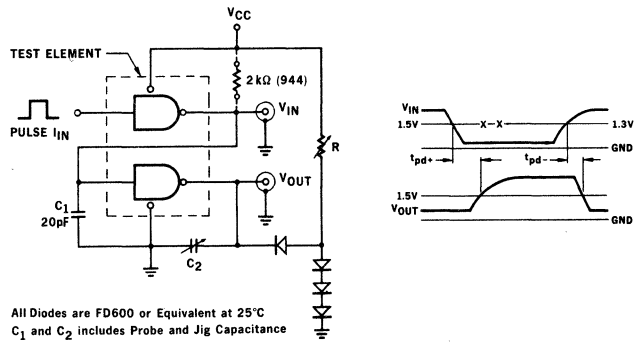


FIG. 10. TYPICAL $t_{pd}+$ VS. CAPACITY (932)

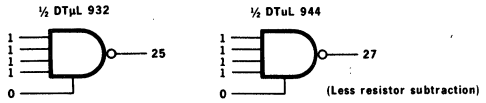


t_{pd} TEST CIRCUIT FOR DTμL 932 ELEMENT



NOTE:
The same circuit is used on the DTμL944 element except that all diodes are omitted. The resistor R is tied to capacitor C and the Test Output. A 2 kΩ resistor is used to load the input gate.

SUGGESTED INPUT-OUTPUT LOADING FACTORS (Please refer to DTμL Composite Data Sheet for complete family rules).



INPUT LOAD FACTORS FOR OTHER DTμL ELEMENTS

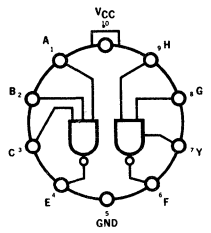
1 - DTμL930, 946, 932, 944 inputs
2 - DTμL931, 945, 948 CP pin
2/3 - DTμL931, 945, 948 S_1 S_2 C_1 C_2
3/4 - DTμL 931 S_D C_D pins
2 - DTμL945, 948 S_D C_D pins
1 - TTμL103, 104 when driven by DTμL932 or 944 with external resistor $\leq 510\,\Omega$.

MISCELLANEOUS RULES

1. DTμL932 may not be output "OR"ed.
2. For increased current, inputs and outputs of 1/2 DTμL932 or 1/2 DTμL944 may be paralleled up to 4 common outputs. Each combined input = 4 loads. Combined output = 100 loads.
3. DTμL944 may be output "OR"ed.
4. An external resistor should be used with DTμL944. With external R to 5 volt V_{CC} ±0.5 V; subtract output loads as follows:

R = 2k	-	2 loads
R = 1k	-	4 loads
R = .510k	-	8 loads

10 LEAD TO-5 PACKAGE

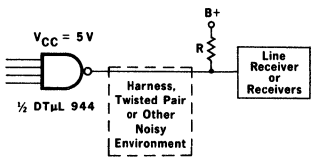


DTμL 930 DUAL GATE
DTμL 932
DUAL BUFFER
DTμL 944
DUAL POWER GATE

MISCELLANEOUS APPLICATIONS

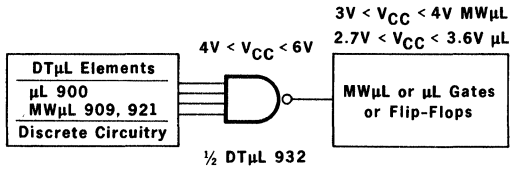
NOTE: In some of these applications, use of the elements is made within the design of the element but beyond the guaranteed test limits on page 2. Consult your Fairchild sales representative for additional information and/or selection requirements.

INTERFACING



B^+ up to 12 volts. Line Receiver may have nominal low level ≤ 1 volt; nominal threshold ≈ 4 V and nominal high level ≥ 8 V, for example. Resistor selected should be as low as possible consistent with required low input level of receiver, number of receivers, and power dissipation of system. For a guaranteed V_{OH} level above 6 volts, an LV_{CE} selection may be desirable; for use of resistor that requires the 944 to sink more than 40 mA (at V_{OL} above .40 volt), a high current I_{OL} - V_{OL} selection may be desirable.

DRIVING μL AND MWμL

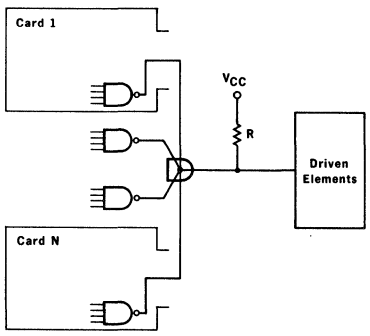


Rules: With $V_{CC} > 4.5$ V a 932 will drive 25-unit μLogic loads or 100 MWμL unit loads.

Derate DTμL output drive by 25% for DTμL932 $V_{CC} = 4$ V.

Refer to DTμL932 Output Current vs Output Voltage curve, Page 3, for matching to μL-MWμL $I_{AVAILABLE}$ requirements.

POWER GATING



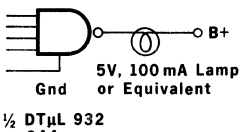
Each output driver is 1/2 DTμL944. Note that the DTμL944 is a direct high fan-out replacement for DTμL930, except that an external resistor must be used.

LAMP DRIVING

Suggested Ratings $T_A \leq 75°C$

Power Dissipation TO-5 400 mW Maximum

Power Dissipation Cerpak 240 mW Maximum



Maximum "hot" lamp current	
120 mA TO-5	one side only ON
100 mA Cerpak	one side only ON
90 mA TO-5	both sides ON
75 mA Cerpak	both sides ON

"Cold" lamp current is limited by saturation resistance, emitter resistance, and base current to about 200 to 250 mA.

The most significant thermal time constants for 932 and 944:

TO-5 Package 50 ms Cerpak 100 ms

Thermal time constant is measured by forward diode drop in one gate with power pulsed into opposite gate. A high current β selection is desirable in this application.

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DTμL933 DUAL FOUR-INPUT EXTENDER ELEMENT

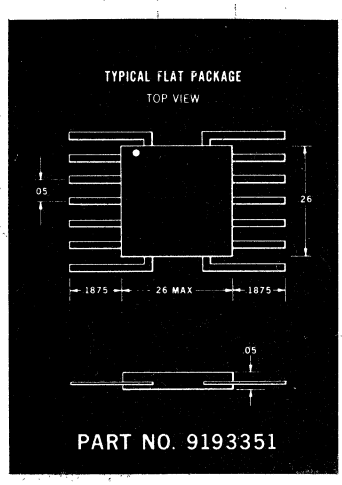
FAIRCHILD DIODE-TRANSISTOR MICROLOGIC

The DTμL 933 is a Dual Input-Extender consisting of two independent diode arrays identical in every respect to the input diodes of the DTμL Gate and Buffer elements. DTμL 933 elements may be used to extend fan-in capability to more than 20 without adversely affecting the noise immunity or load driving capability of the element to which they are connected.

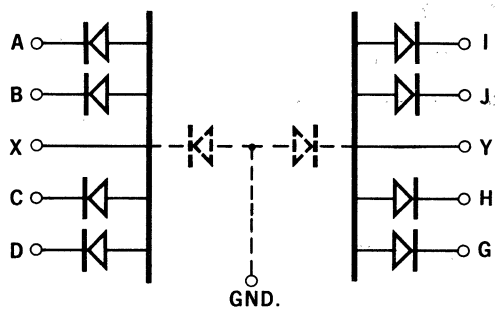
Good practice dictates that extension interconnection paths be as short as possible to minimize the effects of distributed capacitance on circuit performance. The effects of capacitance are summarized on the back page.

Typical input capacitance of DTμL 933 is 2 pf and output capacitance is 5 pf.

For complete test sequence and test values, please refer to the composite DTμL specification

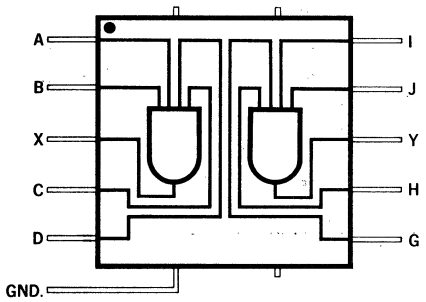


SCHEMATIC DIAGRAM

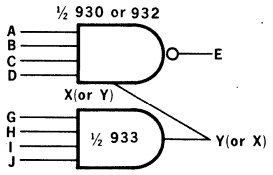


FLAT PACKAGE LAYOUT

(TOP VIEW)



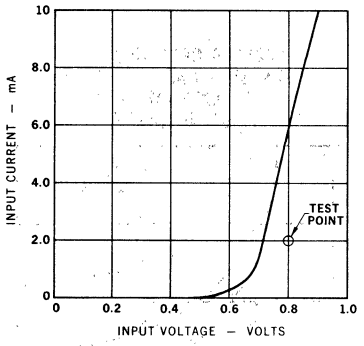
LOGIC EXAMPLE



POSITIVE LOGIC $E = \overline{A\,B\,C\,D\,G\,H\,I\,J}$

NEGATIVE LOGIC $E = \overline{A + B + C + D + G + H + I + J}$

FORWARD VOLTAGE VS. FORWARD CURRENT + 25°C



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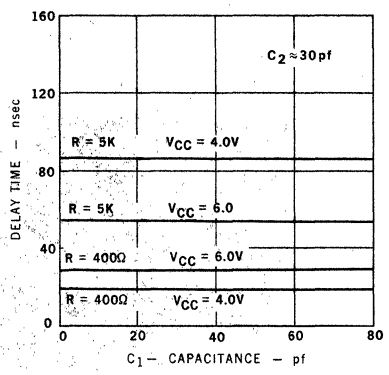
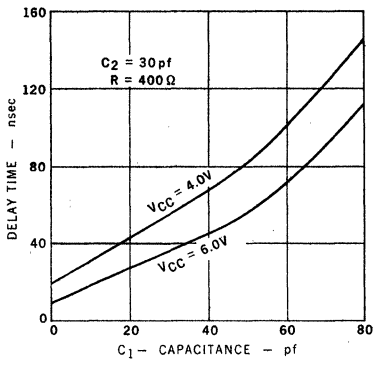
Typical Curves to Show the Effects of Extender Pin Capacitance (Resulting From the Use of DTμL 933) on Time Delay of DTμL 930 Dual Gate and DTμL 932 Dual Buffer
+ 25°C

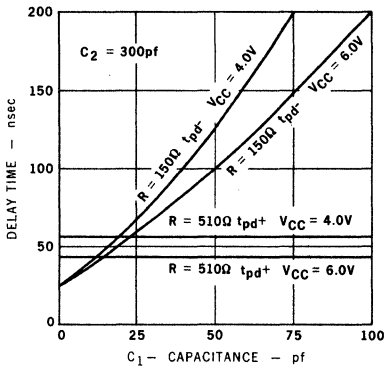
DTμL 930 tpd + VS. EXTENDER PIN CAPACITANCE



DTμL 930 tpd – VS. EXTENDER PIN CAPACITANCE



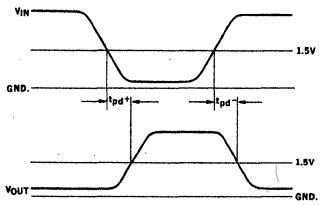
DTμL 932 TIME DELAY VS. EXTENDER PIN CAPACITANCE

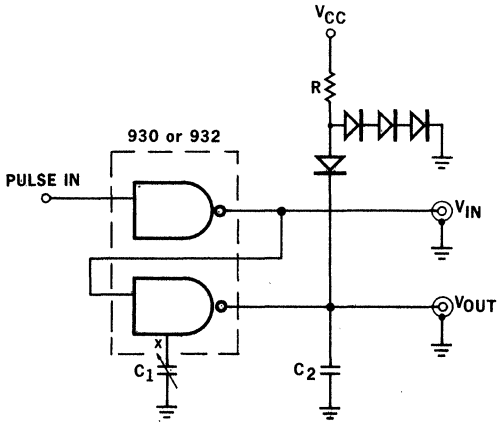


t_{pd}- at R = 5 KΩ is slightly lower.

TEST CONDITIONS

WAVESHAPES



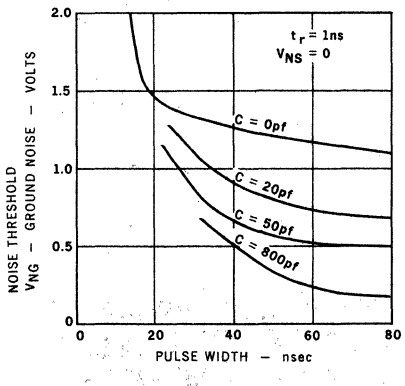


Diodes are FD600

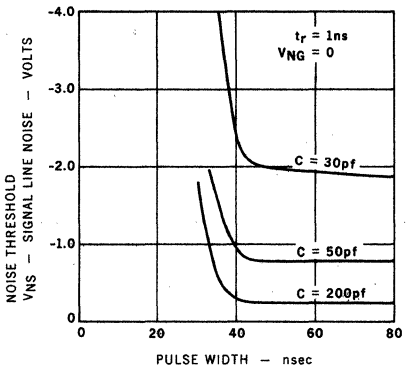
C_1 represents the summation of the DTμL 933Dual Extender Element output capacitances (~5 pf per output) and associated board, connector and wiring capacitances.

Typical Curves to Show the Effects of Extender Pin Capacitance on Noise Threshold of DTμL 930 Dual Gate
+ 25°C

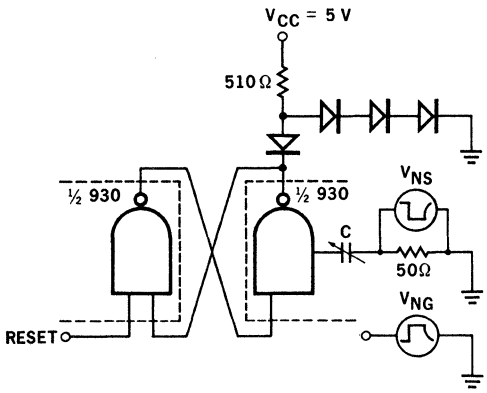
PULSED GROUND NOISE THRESHOLD AS A FUNCTION OF EXTENDER PIN CAPACITANCE



PULSED SIGNAL LINE NOISE THRESHOLD AS A FUNCTION OF EXTENDER PIN CAPACITANCE



TEST CONDITIONS



Diodes are FD600

4501

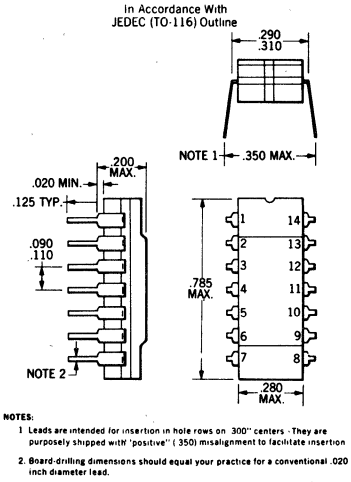
CCSL MICROMATRIX™ QUARTER-CELL

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 4501 consists of a single 4-input DTμL gate designed for use in breadboarding the 4500 Micromatrix™. It corresponds to one of the 32 quarter-cells available in the 4500 Micromatrix array. Logic flexibility is offered with pin options for interconnections of four independent elements. These elements are a) 4-diode cluster, b) non-inverting amplifier, c) common emitter inverting amplifier and d) load resistor.

PHYSICAL DIMENSIONS

TYPICAL DUAL IN-LINE PACKAGE



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

FEATURES

- **Offers 4500 Micromatrix breadboarding capability**
- **Compatible with all CCSL devices**

ABSOLUTE MAXIMUM RATINGS

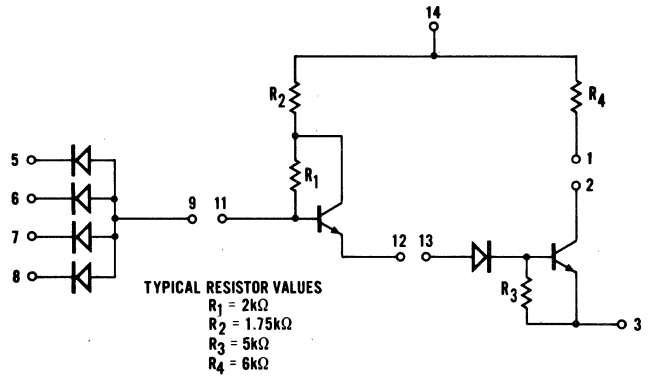
V_{CC} Pin Potential to Ground Pin	−.5 V to +7 V
Input Voltage	−.5 V to +5.5 V
Voltage Applied to Outputs	−.5 V to +V_{CC} Value
Storage Temperature	−65°C to +150°C
Temperature (ambient) under Bias	−55°C to +125°C

ORDER INFORMATION

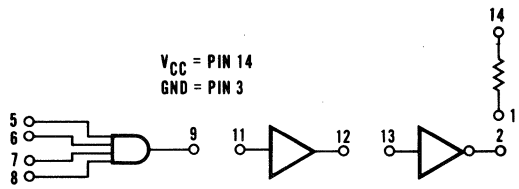
Specify A6A45015XX, where 5XX is 51X for −55°C to +125°C temperature range or 59X for the 0°C to +75°C temperature range.

To order 4500 design kit, specify A6A4501KTX

CIRCUIT SCHEMATIC (PIN NUMBERS)



LOGIC DIAGRAM (PIN NUMBERS)



313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V = 10\%$) Connected as NAND gate with pull-up resistor
MILITARY TEMPERATURE RANGE

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.6		2.6	3.4		2.5		Volts	$V_{CC} = 4.5$ V $I_{OH} = -180\ \mu A$ V_{IL} on any input
V_{OL}	Output Low Voltage		0.4		0.22	0.4		0.4	Volts	$V_{CC} = 5.5$ V $I_{OL} = 8$ mA $V_{CC} = 4.5$ V $I_{OL} = 6.2$ mA
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.3			1.0		0.7	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		1.6		1.18	1.6		1.6	mA	$V_{CC} = 5.5$ V $V_F = 0.4$ V
			1.24		0.91	1.24		1.24	mA	$V_{CC} = 4.5$ V $V_F = 0.4$ V
I_R	Input Leakage Current					2		10	μA	$V_R = 4$ V, GND on other inputs
P_D	Power Dissipation					15.5			mW	$V_{CC} = 5$ V Inputs open, pull-up connected
						8.8			mW	$V_{CC} = 5$ V Any input grounded

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0$ V = 5%) Connected as NAND gate with pull-up resistor
INDUSTRIAL TEMPERATURE RANGE

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.6		2.6	3.65		2.5		Volts	$V_{CC} = 4.75$ V $I_{OH} = -180\ \mu A$ V_{IL} on any input
V_{OL}	Output Low Voltage		0.45		0.22	0.45		0.45	Volts	$V_{CC} = 5.25$ V $I_{OL} = 9.6$ mA $V_{CC} = 4.75$ V $I_{OL} = 8.5$ mA
V_{IH}	Input High Voltage	2.0		1.9			1.8		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.1			1.0		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		1.6		1.09	1.6		1.6	mA	$V_{CC} = 5.25$ V $V_F = 0.45$ V
			1.41		0.96	1.41		1.41	mA	$V_{CC} = 4.75$ V $V_F = 0.45$ V
I_R	Input Leakage Current					5		10	μA	$V_R = 4$ V, GND on other inputs
P_D	Power Dissipation					16.5			mW	$V_{CC} = 5$ V Inputs open, pull-up connected
						9			mW	$V_{CC} = 5$ V Any input grounded

Loading and interconnections for 4501 are identical to 4500 Micromatrix array except for Note 3.

LOADING RULES

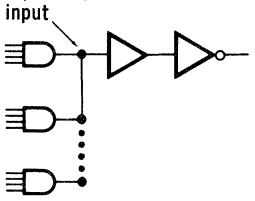
Connected as NAND gate with pull-up resistor

Fan-in 1 DTμL unit load

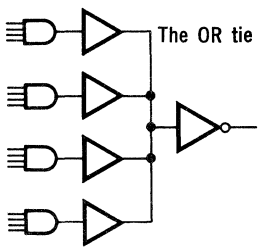
Load	Fan-out 51X	59X
DTL	5	6
TTL	3	3

INTERCONNECTION RULES

Expanding the input



Maximum fan-in — 20 inputs corresponding to 5 diode clusters.
Fan-out — same as NAND gate.



If OR tie is utilized, 4501 fan-out is restricted to 3 unit loads for 51X temperature range operation (4 unit loads for 59X temperature range.) (Note 3.)

Maximum of 4 OR ties allowed.

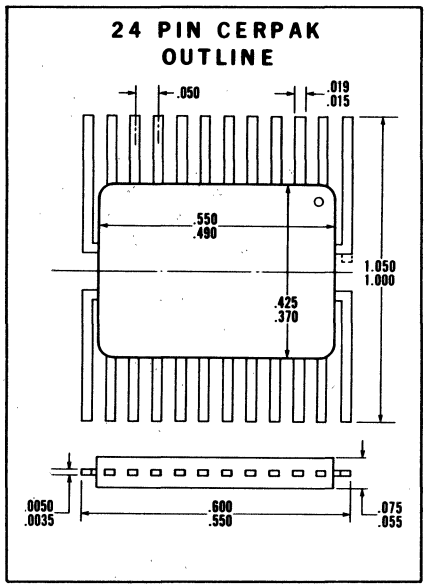
Note 3: Fan-out of 5 (6 for 59X temperature range) with OR tie used, can be maintained if temperature range of operation is limited to +15°C to +125°C (+15°C to +75°C for 59X temperature range.)

4510

CCSL MICROMATRIX™ DUAL 4-BIT COMPARATOR

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 4510 consists of two independent 4-bit comparators useful in many decision making control applications, such as digital printers. Each comparator is capable of accepting two 4-bit inputs and provides a high level output signal when they are identical. An output latch stores the compared output when the strobe pin is high. Outputs may be "Wire ANDed" to expand comparison capability.
The circuit is produced with two layer metal interconnections using the Fairchild 4500 Bipolar Micromatrix™ Array.



FEATURES

- **ASYNCHRONOUS AND SYNCHRONOUS OUTPUTS**
- **OPTIONAL LATCH STORAGE OF OUTPUT**
- **EXPANDABLE IN GROUPS OF 4 BITS**
- **TYPICAL POWER DISSIPATION OF 250 mW**
- **CCSL COMPATIBLE**
- **ALL CERAMIC "HERMETIC" 24 PIN CERPAK**
- **MEMBER OF 4500 MICROMATRIX™ ARRAY FAMILY**
- **TWO LAYER METAL INTERCONNECTIONS**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Voltage Applied to Output for High Output State	−0.5 V to +V_{CC} Value
Output Current Into Low Output State	20 mA
Input Voltage (D.C.)	−0.5 V to +5.5 V

ORDER INFORMATION — Specify A3M45105XX for flat package, where 5XX is 51X for −55°C to +125°C temperature range or 59X for the 0°C to +75°C temperature range.

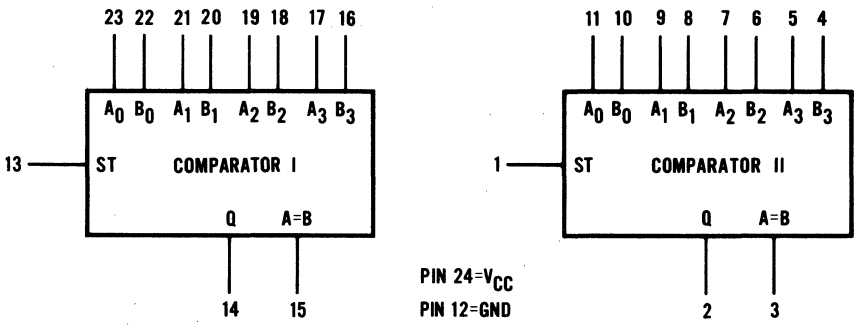


Fig. 1 — 4510 DUAL 4-BIT COMPARATOR LOGIC DIAGRAM

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V = 10\%$)
MILITARY TEMPERATURE RANGE

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Q Output High Voltage	2.6		2.6	3.4		2.5		Volts	$I_{OH} = -180\ \mu A$; V_{IL} on any two inputs
	A = B Output High Voltage	2.6		2.6	3.4		2.5		Volts	$I_{OH} = -240\ \mu A$; $V_{CC} = 4.5\ V$
V_{OL}	Output Low Voltage Q and A = B Output		0.4		0.22	0.4		0.4	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 6.4\ mA$; $V_{CC} = 4.5\ V$ $I_{OL} = 5.0\ mA$; V_{ST} = GND for A = B output only
	Output Low Voltage A = B Output Only		0.4		0.22	0.4		0.4	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 4.8\ mA$; $V_{CC} = 4.5\ V$ $I_{OL} = 3.7\ mA$; $V_{ST} = 4\ V$
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.3			1.0		0.7	Volts	Guaranteed input low threshold for all inputs
$2\ I_F$	Input Load Current		3.2		2.36	3.2		3.2	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$
			2.43		1.82	2.48		2.48	mA	$V_{CC} = 4.5\ V$ $V_F = 0.4\ V$
$1.5\ I_F$	A = B Output Load Current For "Wired AND"		2.4		1.77	2.4		2.4	mA	$V_{CC} = 5.5\ V$; $V_F = 0.4\ V$; V_{ST} = GND
			1.86		1.37	1.86		1.86	mA	$V_{CC} = 4.5\ V$; $V_F = 0.4\ V$; V_{ST} = GND
$2.5\ I_F$			4.0		2.95	4.0		4.0	mA	$V_{CC} = 5.5\ V$; $V_F = 0.4\ V$; $V_{ST} = 4\ V$
			3.1		2.28	3.1		3.1	mA	$V_{CC} = 4.5\ V$; $V_F = 0.4\ V$; $V_{ST} = 4\ V$
I_R	Input Leakage Current					20		20	μA	$V_R = 4\ V$, GND on other inputs
t23+ 15+	Comparison Switching Speed				50				ns	$V_{CC} = 5\ V$
t23− 15−	A_O to A = B				50				ns	$C_L = 15\ pF$ @ Pin 15

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V = 5\%$)
INDUSTRIAL TEMPERATURE RANGE

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Q Output High Voltage	2.6		2.6	3.65		2.5		Volts	$I_{OH} = -180\ \mu A$; V_{IL} on any two inputs
	A = B Output High Voltage	2.6		2.6	3.65		2.5		Volts	$I_{OH} = -300\ \mu A$; $V_{CC} = 4.75\ V$
V_{OL}	Output Low Voltage Q and A = B Output		0.45		0.22	0.45		0.45	Volts	$V_{CC} = 5.25\ V$ $I_{OL} = 8.0\ mA$; $V_{CC} = 4.75\ V$ $I_{OL} = 6.25\ mA$; V_{ST} = GND for A = B output only
	Output Low Voltage A = B Output Only		0.45		0.22	0.45		0.45	Volts	$V_{CC} = 5.25\ V$ $I_{OL} = 6.4\ mA$; $V_{CC} = 4.75\ V$ $I_{OL} = 5.0\ mA$; $V_{ST} = 4\ V$
V_{IH}	Input High Voltage	2.0		1.9			1.8		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.1			1.0		0.8	Volts	Guaranteed input low threshold for all inputs
$2\ I_F$	Input Load Current		3.2		2.18	3.2		3.2	mA	$V_{CC} = 5.25\ V$ $V_F = 0.45\ V$
			2.82		1.92	2.82		2.82	mA	$V_{CC} = 4.75\ V$ $V_F = 0.45\ V$
$1.5\ I_F$	A = B Output Load Current For "Wired AND"		2.4		1.65	2.4		2.4	mA	$V_{CC} = 5.25\ V$; $V_F = 0.4\ V$; V_{ST} = GND
			2.11		1.44	2.11		2.11	mA	$V_{CC} = 4.75\ V$; $V_F = 0.4\ V$; V_{ST} = GND
$2.5\ I_F$			4.0		2.64	4.0		4.0	mA	$V_{CC} = 5.25\ V$; $V_F = 0.4\ V$; $V_{ST} = 4\ V$
			3.52		2.4	3.52		3.52	mA	$V_{CC} = 4.75\ V$; $V_F = 0.4\ V$; $V_{ST} = 4\ V$
I_R	Input Leakage Current					20		20	μA	$V_R = 4\ V$, GND on other inputs
t23+ 15+	Comparison Switching Speed				50				ns	$V_{CC} = 5\ V$
t23− 15−	A_O to A = B				50				ns	$C_L = 15\ pF$ @ Pin 15

FUNCTIONAL DESCRIPTION

ASYNCHRONOUS — Fig. 2 shows the detailed logic representation of the comparator and latch (½ 4510). Whenever the 4-bit data word on lines A is identical to the 4-bit data word on lines B the A = B output is high. If data word A is not equal to data word B the A = B output is low.

SYNCHRONOUS — The strobe (ST) and the latch output (Q) provide storage capability of the A = B output. This function is shown in Table 1. When ST is high, Q_N equals the A = B output. When ST is low, $Q_N = Q_{N-1}$.

TABLE 1

TRANSITION TABLE FOR LATCH OUTPUT (Q)

ST	Q_N
Low	Q_{N-1}
High	A = B

DETAILED LOGIC DIAGRAM

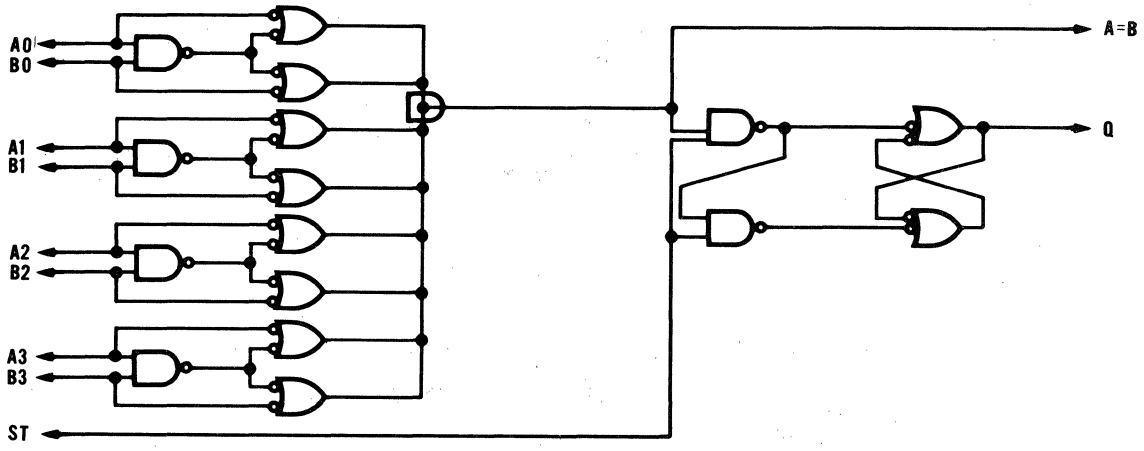
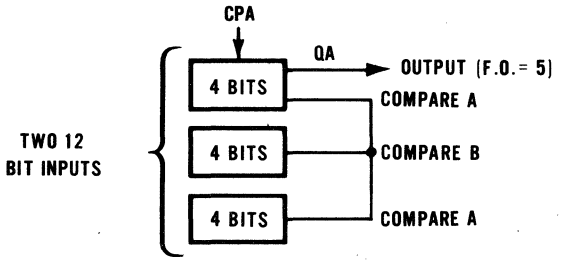


Fig. 2

SUGGESTED COMPARATOR EXPANSION METHODS



The internal "wired OR" COMPARE node uses two pull-up resistors for improved rise time, and drives an internal gate. Two COMPARE outputs may be "wire OR'd" externally to provide a 12 bit comparator as shown in Figure 3. This may be expanded further by using additional gates.

Fig. 3

4510 EQUIVALENT CIRCUITS

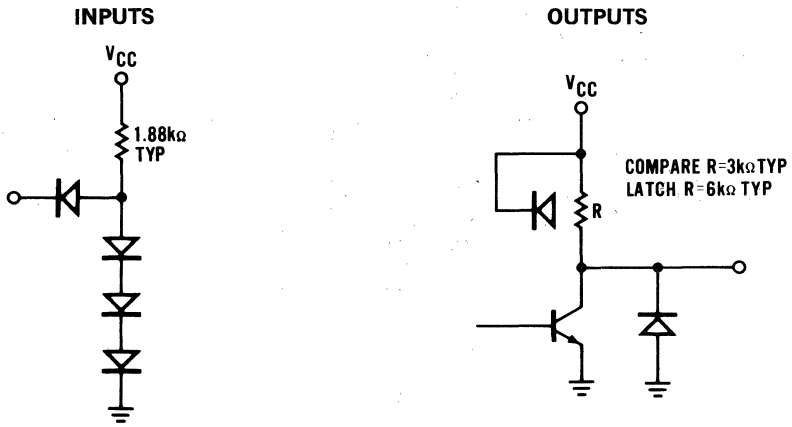


Fig. 4

LOADING RULES

INPUT LOADING RULES (FAN-IN)
DTμL UNIT LOADS

	51X	59X
Data Inputs	2.0	2.0
Strobe Inputs	2.0	2.0
"Wired AND" A = B Outputs (ST GND)	1.5	1.5
A = B Outputs (ST High)	2.5	2.5

OUTPUT DRIVE CAPABILITY (FAN-OUT)

	DTμL LOADS				TTμL LOADS			
	ST = GND		ST = HIGH		ST = GND		ST = HIGH	
	51X	59X	51X	59X	51X	59X	51X	59X
Q OUTPUT	4.0	5.0	4.0	5.0	3.0	3.0	3.0	3.0
A = B Outputs	4.0	5.0	3.0	4.0	4.0	5.0	3.0	4.0
(1) "Wired AND" 2	2.5	3.5	1.5	2.5	2.5	3.5	1.5	2.5
(1) "Wired AND" 3	1.0	2.0	0	1.0	1.0	2.0	0	1.0

(1) "Wired AND" 2 and 3 means the number of compare outputs (A = B) that are connected together. The result of this "Wired AND" connection, logically, is a high level true "AND" gate.

4-BIT COMPARATOR AND LAMP/RELAY DRIVER

One-half of a 4510 dual comparator drives a discrete driver so that when $A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, and $A_3 = B_3$ the lamp will light or the relay operate. This circuit might also be used for a digital printer solenoid driver. The ST input is connected through a 2 kΩ resistor to V_{CC} so that Q and A = B may be paralleled for additional driver base current.

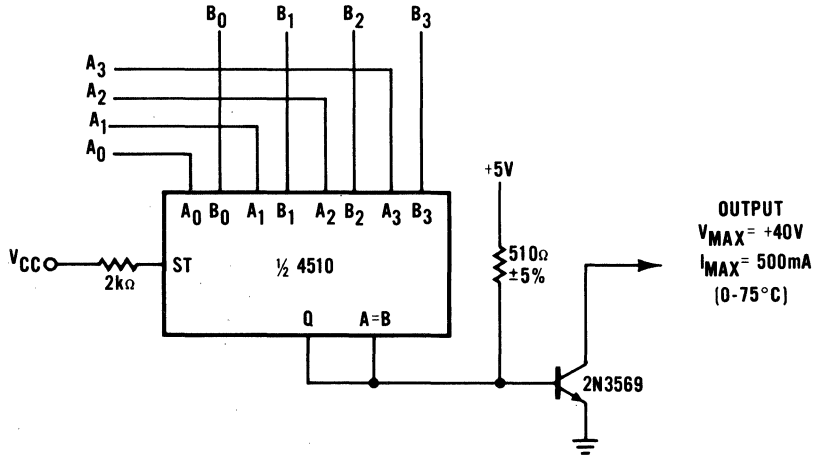


Fig. 5

4601

TTL MICROMATRIX™ ARRAY INTERNAL QUARTER-CELL

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 4601 is a single 4-4 AND-OR-INVERT (AOI) TTμL gate to be used for breadboarding logic designs planned for the 4600 or 4700 Micromatrix™ arrays. The 4601 corresponds to one of the quarter-cell gate elements that are intended for internal (on-chip) usage on the 4600 or 4700 arrays. Standard family TTμL gates such as the 9002 through 9008 may be used to breadboard the quarter-cells having external drive capability. The TTμL 9006 may be used to extend the 4601 at the OR tie points.

FEATURES

- **"INTERNAL" TYPE LOGIC GATES FOR BREADBOARDING 4600 OR 4700 MICROMATRIX ARRAY DESIGNS**
- **CCSL COMPATIBLE**
- **OR EXTENDABLE WITH TTμL 9006**
- **FANOUT = 7 INTERNAL LOADS OR 4.5 EXTERNAL LOADS**
- **"WIRED-AND" OUTPUT CAPABILITY**
- **INPUT CLAMP DIODES FOR RINGING ATTENUATION**

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential Referenced to Ground	−0.5 V to 7 V
Input Voltage Applied to Input	−0.5 V to 5.5 V
Voltage Applied to Output When Output is High	V_{CC}
Input Current Into Inputs	5 mA
Current Into Output When Output is Low	30 mA
Lead Temperature (soldering, 60 seconds)	300°C

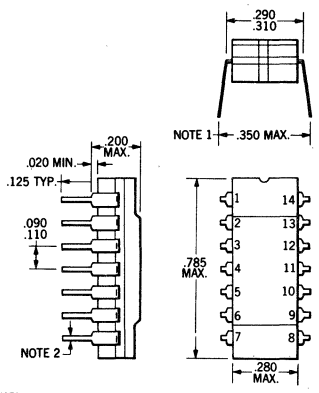
ORDER INFORMATION — Specify A6A46015XX where 5XX is 51X for −55°C to +125°C temperature range and V_{CC} = 5 V ±10%; and 59X for 0°C to 75°C temperature range and V_{CC} = 5 V ±5%.

To order the 4600 Design Kit, specify A6A4600KTX. For the 4700 Design Kit, specify A6A4700KTX.

PHYSICAL DIMENSIONS

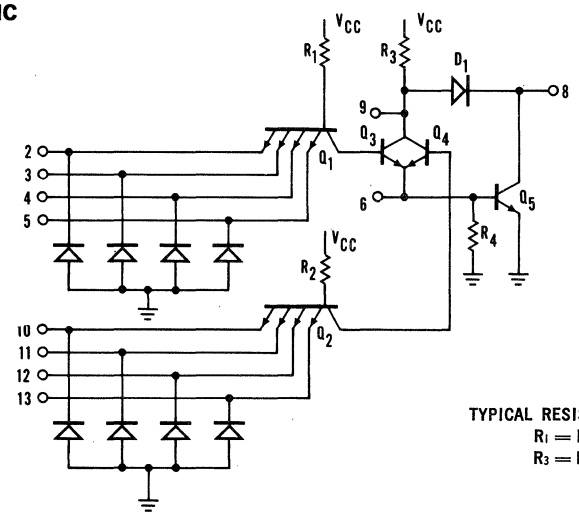
TYPICAL DUAL IN-LINE PACKAGE

In Accordance With
JEDEC (TO-116) Outline



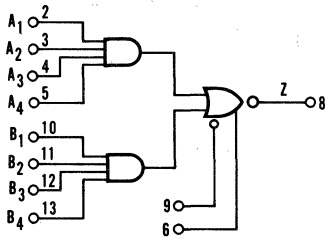
NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

CIRCUIT SCHEMATIC



TYPICAL RESISTOR VALUES
$R_1 = R_2 = 4\ K\Omega$
$R_3 = R_4 = 1.5\ K\Omega$

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND
PIN 1 = NOT USED

Logic Equation: $Z = \overline{A_1A_2A_3A_4 + B_1B_2B_3B_4 + \ldots}$ *

* More terms are provided with OR extension

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

TTL MICROMATRIX™ ARRAY INTERNAL QUARTER-CELL 4601

ELECTRICAL CHARACTERISTICS:

Temperature Range: 0°C to +75°C
Supply Voltage Range: 5 V ±5%

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	75°C MIN.	75°C MAX.	UNITS	CONDITIONS	
V_{OH}	Output High Voltage	2.3		2.3	2.8		2.3		V	V_{CC} = 4.75 V, I_{OH} = −600 μA V_{IL} On Inputs	
V_{OL}	Output Low Voltage Internal Loading		0.6		0.42	0.6		0.6	V	V_{CC} = 5.25 V, I_{OL} = 10.7 mA V_{CC} = 4.75 V, I_{OL} = 9.3 mA	
	Output Low Voltage External CCSL Loading		0.4		0.3	0.4		0.4	V	V_{CC} = 5.25 V, I_{OL} = 7.3 mA V_{CC} = 4.75 V, I_{OL} = 6.4 mA	
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed Input High Threshold For All Inputs	
V_{IL}	Input Low Voltage		0.8			0.8		0.8	V	Guaranteed Input Low Threshold For All Inputs	
I_F	Input Load Current Internal V_F Level		−1.52 −1.33		−1.00 −0.87	−1.52 −1.33		−1.52 −1.33	mA mA	V_{CC} = 5.25 V V_{CC} = 4.75 V	V_F = 0.6 V
	Input Load Current External CCSL V_F Level		−1.60 −1.41		−1.08 −0.91	−1.60 −1.41		−1.60 −1.41	mA mA	V_{CC} = 5.25 V V_{CC} = 4.75 V	V_F = 0.45 V
I_R	Input Leakage Current				5.0	60		60	μA	V_{CC} = 5.25 V, V_R = 4.5 V	
P_D	Power Dissipation				21 11	30 16			mW mW	Inputs Open Inputs Grounded	V_{CC} = 5.0 V

ELECTRICAL CHARACTERISTICS:

Temperature Range: −55°C to +125°C
Supply Voltage Range: 5 V ±10%

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	−55°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	125°C MIN.	125°C MAX.	UNITS	CONDITIONS	
V_{OH}	Output High Voltage	2.3		2.3	2.55		2.3		V	V_{CC} = 4.5 V, I_{OH} = −600 μA V_{IL} On Inputs	
V_{OL}	Output Low Voltage Internal Loading		0.55		0.42	0.55		0.55	V	V_{CC} = 5.5 V, I_{OL} = 10.7 mA V_{CC} = 4.5 V, I_{OL} = 8.2 mA	
	Output Low Voltage External CCSL Loading		0.4		0.3	0.4		0.4	V	V_{CC} = 5.5 V, I_{OL} = 7.3 mA V_{CC} = 4.5 V, I_{OL} = 5.6 mA	
V_{IH}	Input High Voltage	2.0		1.7			1.4		V	Guaranteed Input High Threshold For All Inputs	
V_{IL}	Input Low Voltage		0.8			0.8		0.7	V	Guaranteed Input Low Threshold For All Inputs	
I_F	Input Load Current Internal V_F Level		−1.52 −1.17		−1.04 −0.8	−1.52 −1.17		−1.52 −1.17	mA mA	V_{CC} = 5.5 V V_{CC} = 4.5 V	V_F = 0.55 V
	Input Load Current External CCSL V_F Level		−1.60 −1.24		−1.1 −0.85	−1.60 −1.24		−1.60 −1.24	mA mA	V_{CC} = 5.5 V V_{CC} = 4.5 V	V_F = 0.4 V
I_R	Input Leakage Current				5.0	60		60	μA	V_{CC} = 5.5 V, V_R = 4.5 V	
P_D	Power Dissipation				21 11	30 16			mW mW	Inputs Open Inputs Grounded	V_{CC} = 5.0 V

LOADING RULES

FAN-OUT (See table):

The internal or "on-chip" fan-out of the 4601 is specified with reduced noise margins since on-chip noise is low. If the 4601 is used specifically for off-chip driving, the maximum fan-out must be reduced to maintain CCSL noise margins.

EXTENSION:

Extension at the 4601 OR extender pins 9 and 6 may be accomplished with TTμL 9006 dual 4 input extender elements. A maximum of 10 extenders (5-9006's) may be tied to the 4601 pins. (See Fig. 1)

WIRED "AND":

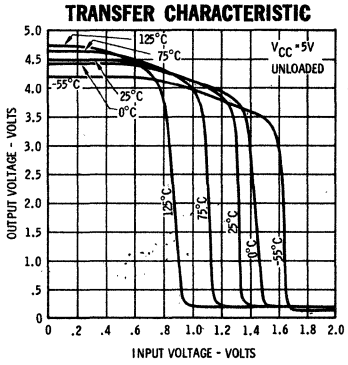
Since the 4601 internal gates have resistive pull-ups, the AND tie of outputs is allowed. (See Fig. 4). Breadboarding of the combined outputs is:
FAN-OUT=7 − (3) (number of outputs tied together − 1)
For "on array" usage optional pull-up resistors allow fan-out as summarized below:

FAN-OUT TABLE

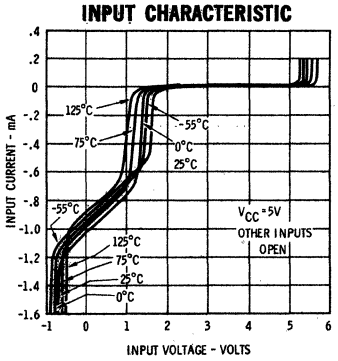
LOADING TYPE	FAN-OUT
INTERNAL	7
TTμL	4.5
DTμL	4.5
LPDTμL	45

TYPICAL INPUT-OUTPUT CHARACTERISTICS

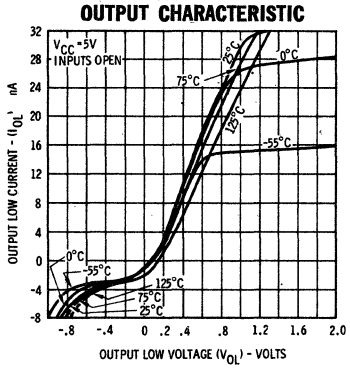
TRANSFER CHARACTERISTIC



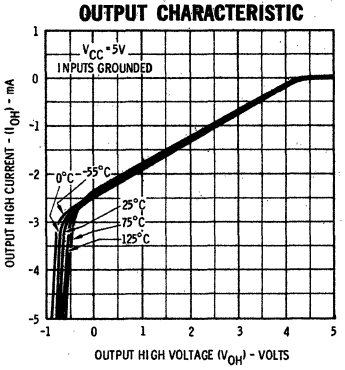
INPUT CHARACTERISTIC



LOW LEVEL OUTPUT CHARACTERISTIC



HIGH LEVEL OUTPUT CHARACTERISTIC



TYPICAL APPLICATIONS

EIGHT INPUT DIGITAL MULTIPLEXER USING "OR" EXTENSION

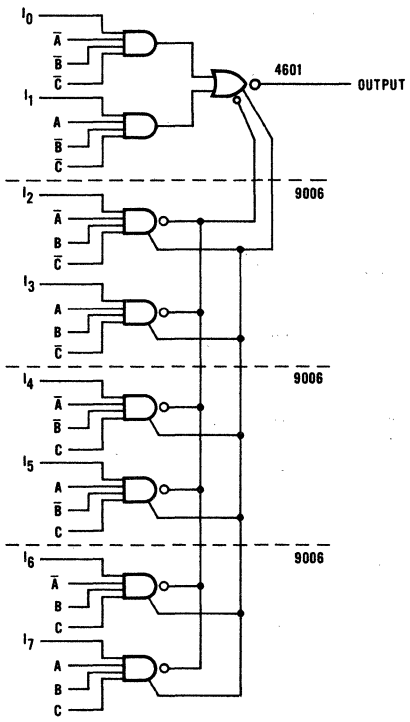


Fig. 1

Three bit address A B C selects an input (I_0, I_1 . . . I_7) which is presented at the output in inverted form. The 4601 is OR-expanded using 3-9006 extender elements.

GATED LATCH USING TWO 4601

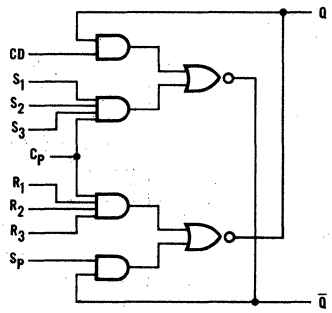


Fig. 2

4610

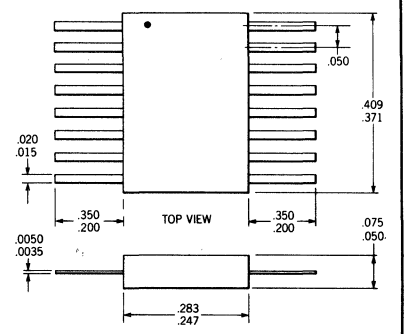
DUAL TWO-VARIABLE FUNCTION GENERATOR

TTL MICROMATRIX™ ARRAY CIRCUIT

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION—The 4610 is a Dual Two-Variable Function Generator useful for non-arithmetic operations and variable decision making control in central processor units. Each circuit, controlled by a common 4-bit word, can select one of 16 possible Boolean functions performed on the two variable inputs. An alternate input select configuration increases circuit flexibility and allows simultaneous generation of two separate output functions from a single pair of variables. **The circuit is produced with two layer metal interconnection using the Fairchild 4600 TTL Micromatrix™ Array.**

FLAT PACKAGE



FEATURES

- **EXPANDABLE IN GROUPS OF 2 BITS**
- **MEMBER OF 4600 MICROMATRIX ARRAY FAMILY**
- **CCSL COMPATIBLE**
- **ALL CERAMIC "HERMETIC" 16-PIN FLAT PACK**
- **TWO LAYER METAL INTERCONNECTIONS**
- **SIMULTANEOUS FUNCTIONS OF 1 PAIR OF VARIABLES**

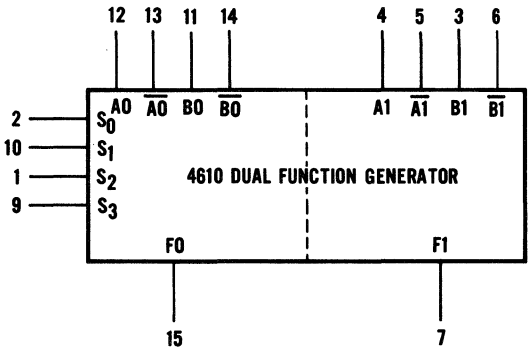
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Case) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs (Output high)	Gnd to +V_{CC} value
Input Voltage (DC) (See Note 1)	−0.5 V to +5.5 V
Input Current (DC) (See Note 1)	−30 mA to +5 mA
Current into Output (Output low)	+30 mA

Note 1—either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

ORDER INFORMATION — Specify A3L46105XX for Flat package, where 51X is for −55°C to +125°C (Case) temperature range or 59X for the 0°C to +75°C (Case) temperature range.

FIG. 1 — 4610 DUAL TWO-VARIABLE FUNCTION GENERATOR



Pin 16 = V_{CC}
Pin 8 = Gnd

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ELECTRICAL CHARACTERISTICS ($T_C = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4			2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -1.2\ mA$
V_{OL}	Output Low Voltage		0.45			0.45		0.45	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 12.8\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 9.92\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		.75	Volts	Guaranteed input low threshold for all inputs
I_F (See Loading Rules Note 1)	Input Load Current		−1.60		−1.1	−1.60		−1.60	mA	$V_{CC} = 5.5\ V$ $V_F = 0.45\ V$
	One Low Level Unit Load		−1.24		−0.85	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$
I_R (See Loading Rules Note 2)	Input Leakage Current				5.0	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
P_D	Power Dissipation				375	500			mW	$V_{CC} = 5.0\ V$, Inputs open
t_{I2}	Avg. Propagation Delay				20				ns	$V_{CC} = 5.0\ V$ $C_L = 20\ pf$, $R_L = 1\ k$

ELECTRICAL CHARACTERISTICS ($T_C = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Q Output High Voltage	2.4		2.4			2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -1.2\ mA$
V_{OL}	Output Low Voltage		0.45			0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 12.8\ mA$ $V_{CC} = 4.75\ V$, $I_{OL} = 11.3\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (See Loading Rules Note 1)	Input Load Current		−1.60		−1.08	−1.60		−1.60	mA	$V_{CC} = 5.25\ V$ $V_F = 0.45\ V$
	One Low Level Unit Load		−1.41		−0.91	−1.41		−1.41	mA	$V_{CC} = 4.75\ V$
I_R (See Loading Rules Note 2)	Input Leakage Current					60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
P_D	Power Dissipation				375	500			mW	$V_{CC} = 5.0\ V$, Inputs open
t_{I2}	Avg. Propagation Delay				20				ns	$V_{CC} = 5.0\ V$ $C_L = 20\ pf$, $R_L = 1\ k$

FUNCTION GENERATOR DESCRIPTION

A detailed logic representation of the common control (S_0, S_1, S_2, S_3) and one of the two output function blocks is shown in Figure 2. The Truth Table implemented by the function generator shows the functions of input variables A and B with the 16 possible combinations of S_0, S_1, S_2, and S_3 (refer to Table 1). Note that any desired output function may be chosen active level high or active level low.

FUNCTION GENERATOR TRUTH TABLE WITH INPUT VARIABLES ACTIVE HIGH

S_0	S_1	S_2	S_3	FUNCTION (ACTIVE LOW)	FUNCTION (ACTIVE HIGH)
L	L	L	L	$A + B$	$\overline{A} \cdot \overline{B}$
L	H	L	L	$A + \overline{B}$	$\overline{A} \cdot B$
H	L	L	L	$\overline{A} + B$	$A \cdot \overline{B}$
H	H	L	L	$\overline{A} + \overline{B}$	$A \cdot B$
L	L	L	H	$\overline{A} \cdot \overline{B}$	$A + B$
L	H	L	H	$\overline{A} \cdot B$	$A + \overline{B}$
H	L	L	H	$A \cdot \overline{B}$	$\overline{A} + B$
H	H	L	H	$A \cdot B$	$\overline{A} + \overline{B}$
L	L	H	L	$A \oplus B$	$A \oplus \overline{B}$
L	H	H	L	$A \oplus \overline{B}$	$A \oplus B$
H	L	H	L	1	0
H	H	H	L	0	1
L	L	H	H	A	$\overline{A}$
L	H	H	H	B	$\overline{B}$
H	L	H	H	$\overline{A}$	A
H	H	H	H	$\overline{B}$	B

TABLE 1

DETAILED LOGIC DIAGRAM

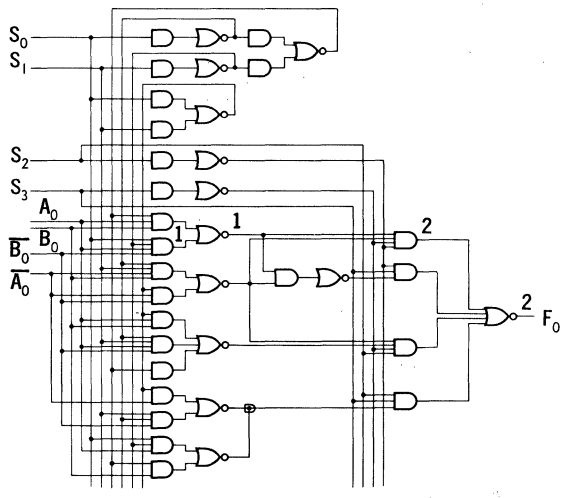


FIG. 2

Circuit flexibility can be increased by using S_2, S_3, A and B inputs as controls and S_0, S_1 as the input variables. In this mode of operation two separate output functions are performed simultaneously on a single pair of variables S_0 and S_1. Refer to Table 2 below for complete truth table.

For example, if it is desired to obtain the active high functions $\overline{S}_0 \cdot S_1$ and $S_0 \cdot \overline{S}_1$ simultaneously, S_2, S_3 are set low, A_0 low, B_0 high, A_1 high, and B_1 low. The function $\overline{S}_0 \cdot S_1$ will appear at the F_0 output; likewise function $S_0 \cdot \overline{S}_1$ will appear at the F_1 output.

FUNCTION GENERATOR TRUTH TABLE WITH INPUT VARIABLES ACTIVE HIGH WHERE A, B, S_2, S_3 ARE USED AS CONTROL INPUTS AND S_0, S_1 ARE INPUT VARIABLES ON WHICH THE FUNCTIONS ARE PERFORMED.

S_2	S_3	A	B	FUNCTION (ACTIVE LOW)	FUNCTION (ACTIVE HIGH)
L	L	L	L	$S_0 + S_1$	$\overline{S}_0 \cdot \overline{S}_1$
L	L	L	H	$S_0 + \overline{S}_1$	$\overline{S}_0 \cdot S_1$
L	L	H	L	$\overline{S}_0 + S_1$	$S_0 \cdot \overline{S}_1$
L	L	H	H	$\overline{S}_0 + \overline{S}_1$	$S_0 \cdot S_1$
L	H	L	L	$\overline{S}_0 \cdot \overline{S}_1$	$S_0 + S_1$
L	H	L	H	$\overline{S}_0 \cdot S_1$	$S_0 + \overline{S}_1$
L	H	H	L	$S_0 \cdot \overline{S}_1$	$\overline{S}_0 + S_1$
L	H	H	H	$S_0 \cdot S_1$	$\overline{S}_0 + \overline{S}_1$
H	L	L	L	$S_0 \oplus S_1$	$S_0 \oplus \overline{S}_1$
H	L	L	H	$\overline{S}_1$	S_1
H	L	H	L	$\overline{S}_1$	S_1
H	L	H	H	$S_0 \oplus S_1$	$S_0 \oplus \overline{S}_1$
H	H	L	L	S_0	$\overline{S}_0$
H	H	L	H	$S_0 \oplus S_1$	$S_0 \oplus \overline{S}_1$
H	H	H	L	$S_0 \oplus \overline{S}_1$	$S_0 \oplus S_1$
H	H	H	H	$\overline{S}_0$	S_0

TABLE 2

Note that by varying control lines S_2, S_3, A and B that any pair of S_0 and S_1 min terms, max terms, or symmetric function can be generated.

LOADING RULES

Input Loading Rules (Fan-in)

1. I_F is defined as one low level unit load. The multipliers to determine low level unit loads for individual inputs are:

INPUT	MULTIPLIER
S_1	8
S_0	6
S_2, S_3	5
A_0, A_1, B_0, B_1, $\overline{B_0}$, $\overline{B_1}$	4
$\overline{A_0}$, $\overline{A_1}$	3

2. I_R is defined as one unit high level load. The multipliers to determine high level unit loads for individual inputs are:

INPUT	MULTIPLIER
S_1	8
S_0	6
A_0, A_1, S_2, S_3	5
$\overline{B_0}$, $\overline{B_1}$, B_0, B_1	4
$\overline{A_0}$, $\overline{A_1}$	3

FAN OUT

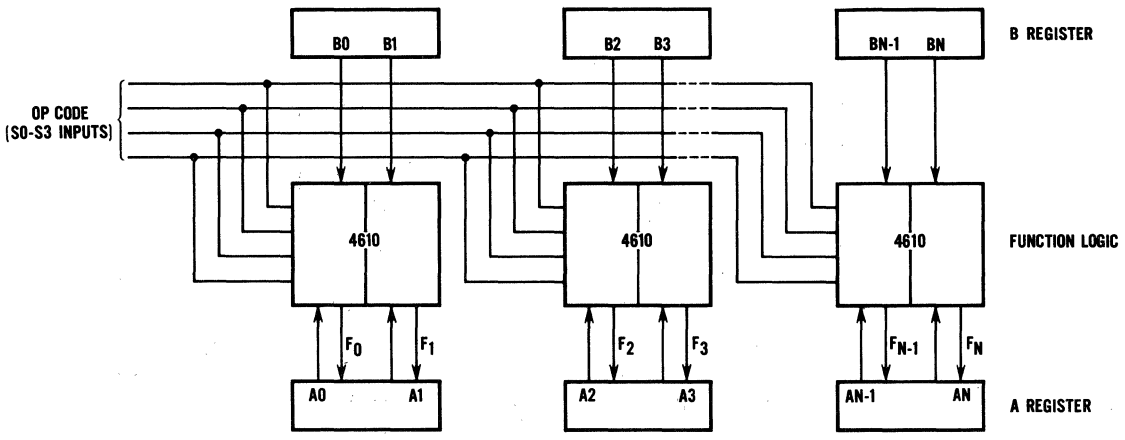
	LEVEL	
OUTPUT	HIGH	LOW
F_0	20	8
F_1	20	8

APPLICATIONS

A Typical Processor Application is the transfer and logical operation control between two registers (A and B). The function generators are controlled by a 4-bit operation code field, S_0, S_1, S_2, and S_3. The operation code repertoire includes the 16 operations listed below.

AND $\overline{A}$ and $\overline{B}$ to A	OR A and B to A
AND $\overline{A}$ and B to A	OR A and $\overline{B}$ to A
AND A and $\overline{B}$ to A	OR $\overline{A}$ and B to A
AND A and B to A	OR $\overline{A}$ and $\overline{B}$ to A
Exclusive OR A and $\overline{B}$ to A	Complement A
Exclusive OR A and B to A	Transfer $\overline{B}$ to A
Reset A	No Operation
Set A	Transfer B to A

FIG. 3



TRANSISTOR-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

A FAIRCHILD *COMPATIBLE CURRENT SINKING LOGIC* PRODUCT

MILITARY TEMPERATURE RANGE: −55°C to 125°C

GENERAL DESCRIPTION

The Fairchild Transistor-Transistor Micrologic® Integrated Circuit family (TTμL) combines a high fanout, high noise immunity, low power dissipation and good capacitive load driving capability with low propagation delay times.

The circuits are fabricated within a silicon monolithic substrate using standard Fairchild Planar† Epitaxial processes.

TTμL elements are available in two hermetically sealed ceramic packages; the Dual In-Line Package (DIP), designed for automated and low cost insertion techniques, and the 14 lead CERPAK® flat package.

Worst case curves of important device characteristics are offered to assist the designer in achieving maximum system reliability. For additional information refer to Application note No. 131.

FEATURES

- Single power supply requirement; 5 volts optimum, 4.5 to 5.5 volt range.
- Reliable operation over the full military temperature range of −55°C to 125° C.
- Guaranteed fanout of 10 TTμL loads over the full temperature and supply voltage range.
- Guaranteed minimum of 0.4 volt noise immunity at the temperature extremes.
- Typical "one" level noise immunity of 1.3 volts and "zero" level noise immunity of 0.8 volt.
- Typical power dissipation of 11 mW per gate at a 50% duty cycle.
- Typical logic gate propagation delays of 6 ns for 15 pF, 11 ns for 150 pF of capacitance.
- The unique output pull-up circuitry gives a higher output "one" level and can provide more output high current at low temperatures than conventional pull-ups.
- The input threshold of 1.5 volts and V_{CC} of 5 volts provides easy interfacing with the Fairchild DTμL family, and other DTL and TTL circuits.
- Nand gate pin configurations are compatible with DTμL.

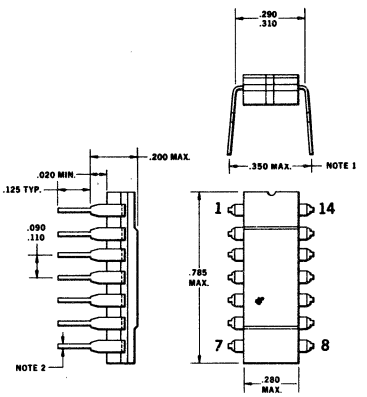
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} pin potential to ground	−.5 to +8 V
Input Voltage	−1.5 to +5.5 V
Gate Output Voltage, Inputs Low	−.5 to +V_{CC} value
Gate Current Into Output Terminal, Inputs High (except 9009)	50 mA
Gate Current Into Output Terminal, Inputs High 9009	100 mA
Flip-Flop Output Voltage when output is normally high	−.5 to +V_{CC} value
Flip-Flop Current Into Output Terminal when output is normally low	50 mA

ORDER INFORMATION

To order Transistor-Transistor Micrologic elements specify U31XXXX-51X for Flat package and U6AXXXX51X for Dual In-Line package where XXXX is the four-digit number denoting the specific element desired.

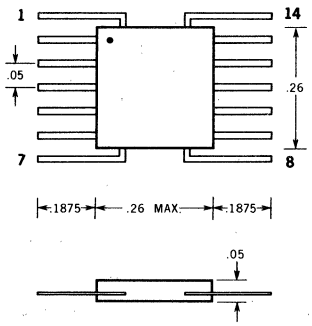
DUAL IN-LINE PACKAGE
TO-116



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

FLAT PACKAGE

TOP VIEW



Flat-pack and Dual-in-line have same pin configurations.

† Planar is a patented Fairchild process.

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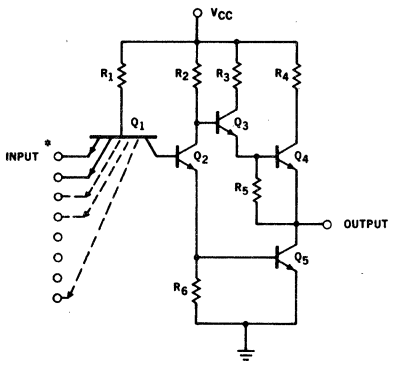
GATE ELEMENTS — 9002, 9003, 9004, 9007

All TTμL gates are positive logic NAND gates and negative logic NOR gates. A variety of gate combinations is available which provides the system designer the utmost in logic flexibility and reduces package requirements to a minimum.

BASIC GATE CIRCUIT



TYPICAL RESISTOR VALUES
$R_1 = R_5 = 4\ k\Omega$
$R_2 = 1.5\ k\Omega$
$R_3 = 150\ \Omega$
$R_4 = 80\ \Omega$
$R_6 = 1.25\ k\Omega$

*Number of inputs depends on the gate.

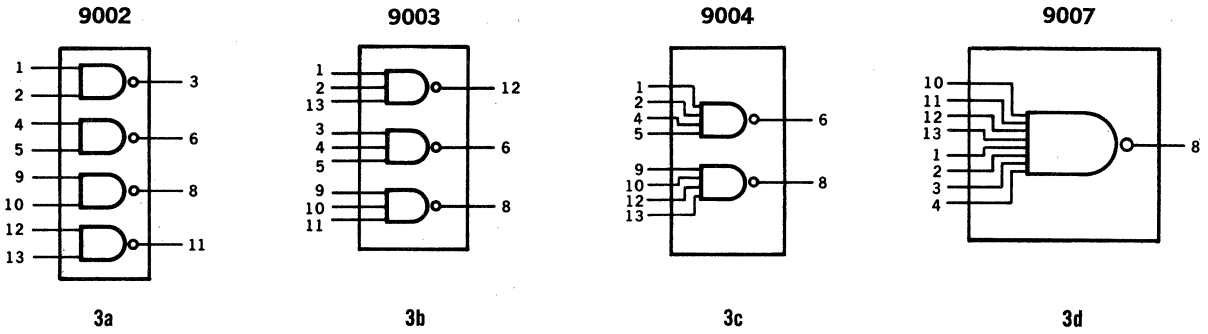
Figure 1

LOADING RULES

The outputs CANNOT be tied together for the "wired OR" function.

Figure 2

PIN CONFIGURATION



3a 3b 3c 3d

Figure 3

V_{CC} = PIN 14 GND = PIN 7

ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = 1.0\ mA$ V_{IL} = value indicated below on this table.
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 17.6\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 14.5\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs.
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs.
I_F	Input Load Current		−1.76		−1.10	−1.76		−1.76	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$, $V_R = 4.5\ V$ on other inputs
I_F	Input Load Current		−1.45		−0.97	−1.45		−1.45	mA	$V_{CC} = 4.5\ V$
I_R	Input Leakage Current				20	60		100	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$, Gnd. on other inputs
t_{pd+}	Turn Off Delay			4.0		12			ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ (see fig. 5b)
t_{pd-}	Turn On Delay			3.0		10			ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ (see fig. 5b)

GATE ELEMENTS — 9002, 9003, 9004, 9007 (continued)

WORST CASE LOGIC LEVELS VERSUS TEMPERATURE

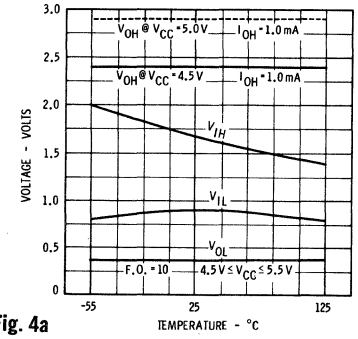


Fig. 4a

WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS TEMPERATURE

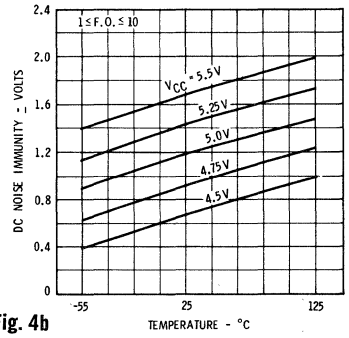


Fig. 4b

WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS TEMPERATURE

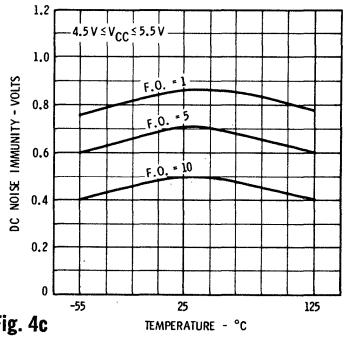


Fig. 4c

WORST CASE POWER DISSIPATION VERSUS SUPPLY VOLTAGE (PER GATE)

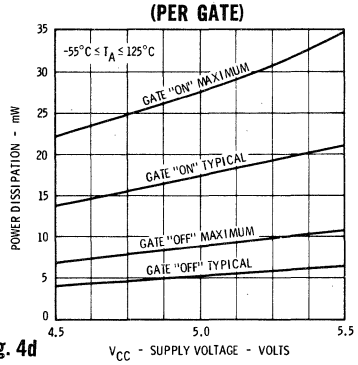


Fig. 4d

WORST CASE POWER DISSIPATION VERSUS FREQUENCY (PER GATE)

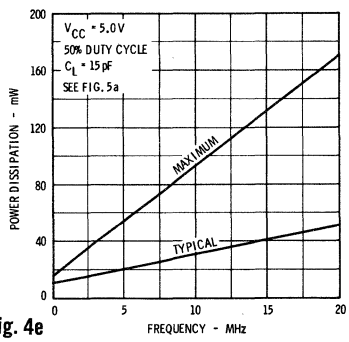


Fig. 4e

WORST CASE TURN OFF DELAY VERSUS TEMPERATURE

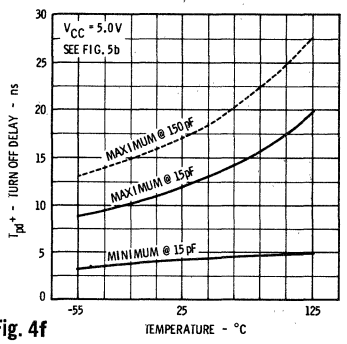


Fig. 4f

WORST CASE TURN ON DELAY VERSUS TEMPERATURE

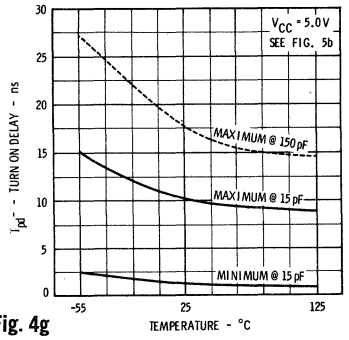
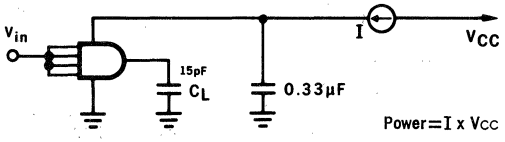


Fig. 4g

FIGURE 4

AC POWER TEST CIRCUIT

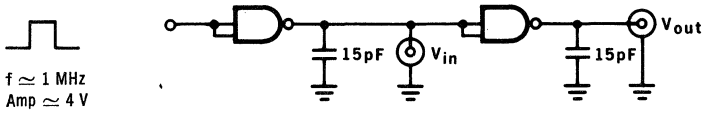


V_{in}
50% Duty Cycle
Amp ≃ 4 V
$t_r = t_f \leq 10$ ns

FIGURE 5a

NOTE: Capacitance includes probe and jig capacity. All inputs are to be tied together.

tpd TEST CIRCUIT



f ≃ 1 MHz
Amp ≃ 4 V
Width ≃ 200 ns
$t_r = t_f \leq 10$ ns

SWITCHING WAVEFORM

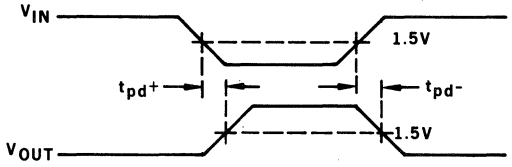


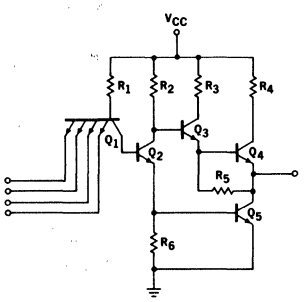
FIGURE 5b

NOTE: Capacitance includes probe and jig capacity. All inputs are to be tied together.

POWER GATE ELEMENT — 9009

The TTμL 9009 element is a NAND power gate capable of driving and sinking large currents for high fan-out applications.

For noise immunity and operating level curves, refer to the gate section.



TYPICAL RESISTOR VALUES

R_1 = 2.2kΩ R_4 = 50Ω

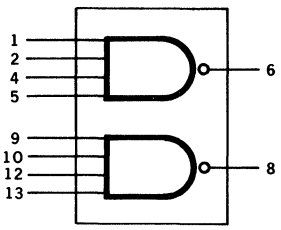
R_2 = 450Ω R_5 = 4kΩ

R_3 = 150Ω R_6 = 400Ω

LOADING RULES:

The outputs CANNOT be tied together for the "wired OR" function.

PIN CONFIGURATION



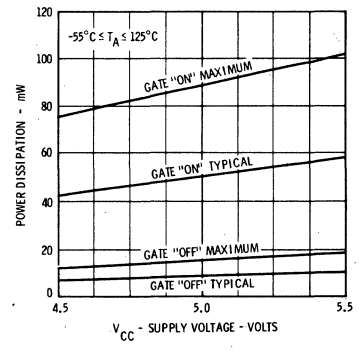
V_{CC} = PIN 14 GND = PIN 7

ELECTRICAL CHARACTERISTICS

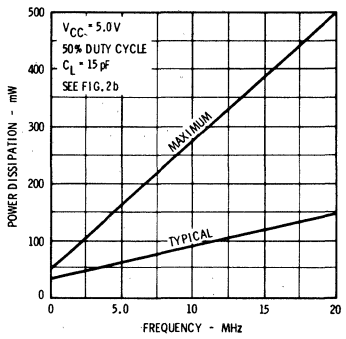
SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = 3.0 mA V_{IL} = value indicated below on this table.
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 52.8 mA V_{CC} = 4.5 V, I_{OL} = 42.9 mA
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs.
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs.
I_F	Input Load Current		− 3.52		− 1.95	− 3.52		− 3.52	mA	V_{CC} = 5.5 V; V_F = 0.4 V, V_R = 4.5 V on other inputs
I_F	Input Load Current		− 2.9		− 1.6	− 2.9		− 2.9	mA	V_{CC} = 4.5 V; V_F = 0.4 V, V_R = 4.5 V on other inputs
I_R	Input Leakage Current				35	120		200	μA	V_{CC} = 5.5 V, V_R = 4.5 V, Gnd. on other inputs.
t_{pd+}	Turn Off Delay				4.0	17			ns	V_{CC} = 5.0 V, C_L = 15 pF (see fig. 2a)
t_{pd-}	Turn On Delay				3.0	10			ns	V_{CC} = 5.0 V, C_L = 15 pF (see fig. 2a)

POWER GATE ELEMENT — 9009 (continued)

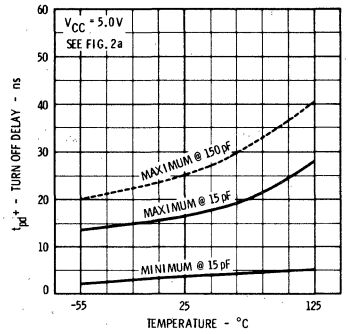
WORST CASE POWER DISSIPATION VERSUS COLLECTOR SUPPLY VOLTAGE (PER GATE)



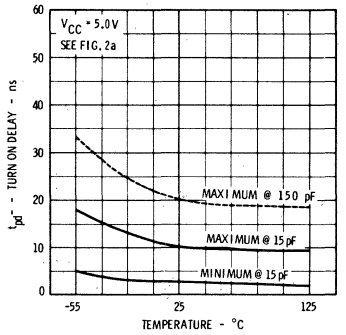
WORST CASE POWER DISSIPATION VERSUS FREQUENCY (PER GATE)



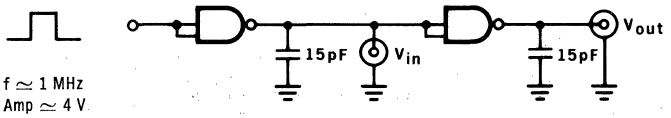
WORST CASE TURNOFF DELAY VERSUS TEMPERATURE



WORST CASE TURN ON DELAY VERSUS TEMPERATURE

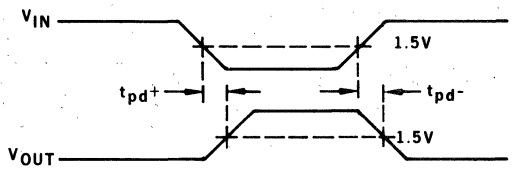


tpd TEST CIRCUIT



f ≃ 1 MHz
Amp ≃ 4 V
Width ≃ 200 ns
$t_r = t_f \leq 10$ ns

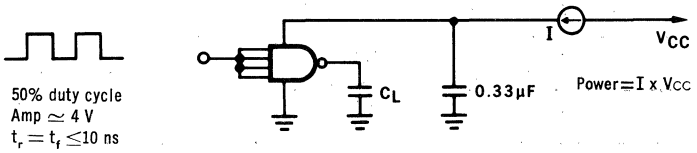
SWITCHING WAVEFORM



NOTE: Capacitance includes probe and jig capacity.
All inputs are to be tied together.

FIGURE 2a

AC POWER TEST CIRCUIT



50% duty cycle
Amp ≃ 4 V
$t_r = t_f \leq 10$ ns

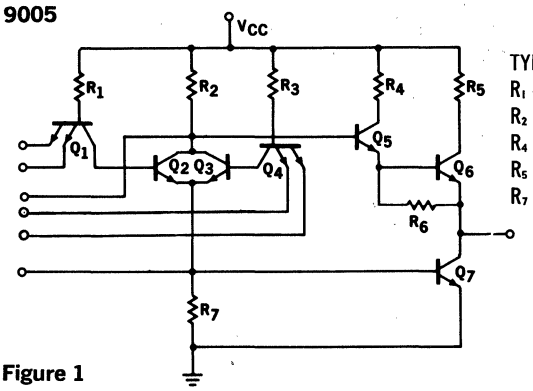
NOTE: Capacitance includes probe and jig capacity.
All inputs are to be tied together.

FIGURE 2b

EXPANDABLE GATES — 9005, 9006, 9008

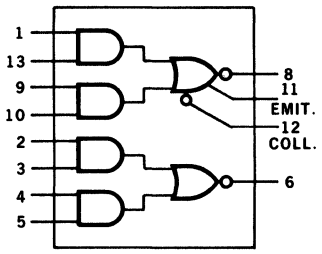
The TTμL 9005 and 9008 are AND-NOR gates which may be NOR expanded with the use of the 9006 element.
For noise immunity and operating level curves, refer to the gate section.

9005



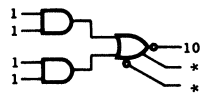
TYPICAL RESISTOR VALUES
$R_1 = R_3 = R_6 = 4\ k\Omega$
$R_2 = 1.5\ k\Omega$
$R_4 = 150\ \Omega$
$R_5 = 80\ \Omega$
$R_7 = 1.25\ k\Omega$

PIN CONFIGURATION



V_{CC} = PIN 14 GND = PIN 7

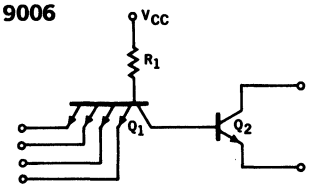
LOADING RULES:



*Four Expanders (9006) may be tied to these terminals.

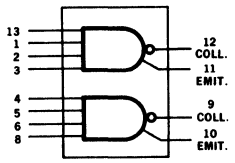
Figure 1

9006



TYPICAL RESISTOR VALUE
$R_1 = 4\ k\Omega$

PIN CONFIGURATION



V_{CC} = PIN 14 GND = PIN 7

LOADING RULES:

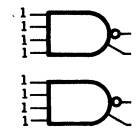
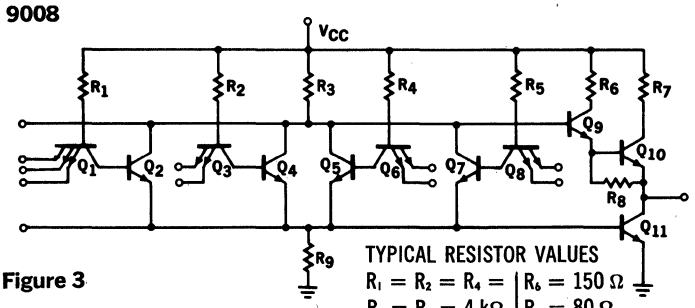


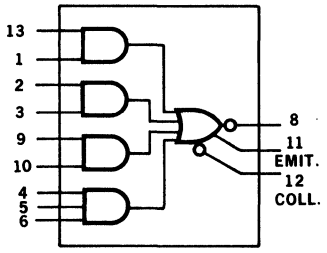
Figure 2

9008



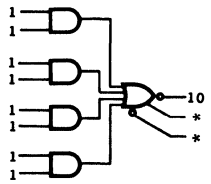
TYPICAL RESISTOR VALUES
$R_1 = R_2 = R_4 = R_5 = R_8 = 4\ k\Omega$
$R_3 = 1.5\ k\Omega$
$R_6 = 150\ \Omega$
$R_7 = 80\ \Omega$
$R_9 = 1.25\ k\Omega$

PIN CONFIGURATION



V_{CC} = PIN 14 GND = PIN 7

LOADING RULES:



*Four Expanders (9006) may be tied to these terminals.

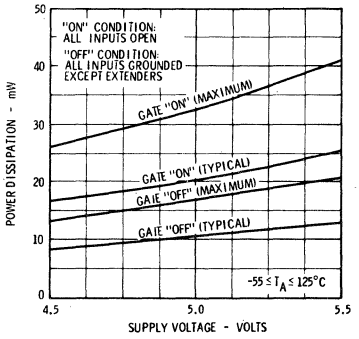
Figure 3

ELECTRICAL CHARACTERISTICS

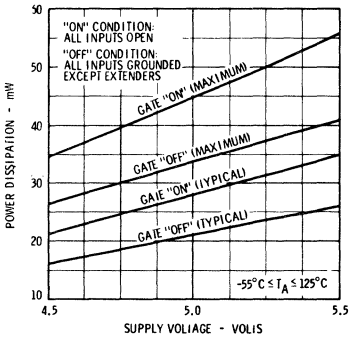
SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = 1.0\ mA$ V_{IL} = value indicated below on this table
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 17.6\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 14.5\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs.
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs.
I_F	Input Load Current		−1.76		−1.10	−1.76		−1.76	mA	$V_{CC} = 5.5\ V$; $V_F = 0.4\ V$, $V_R = 4.5\ V$ on other inputs
I_F	Input Load Current		−1.45		−0.97	−1.45		−1.45	mA	$V_{CC} = 4.5\ V$
I_R	Input Leakage Current				20	60		100	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$, Gnd. on other inputs
t_{pd+}	Defined in Test Circuit			4		12			ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ Applies to 9005 nonexpandable Gate only
t_{pd-}	Defined in Test Circuit			3		12			ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ Applies to 9005 nonexpandable Gate only
t_{pd+}	Defined in Test Circuit			4		15			ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$, $C_N = 5.0\ pF$ Applies to 9008 and 9005 Expandable Gate
t_{pd-}	Defined in Test Circuit			3		10			ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$, $C_N = 5.0\ pF$ Applies to 9008 and 9005 Expandable Gate
Δt_{pd+}	See Comment			0		4			ns	9006 only
Δt_{pd-}	See Comment			0		4			ns	The 9006 shall be tested by measuring its propagation time through the 9005.
										The t_{pd} reading shall not exceed the 9005 reading by the specified amount.

EXPANDABLE GATES — 9005, 9006, 9008 (continued)

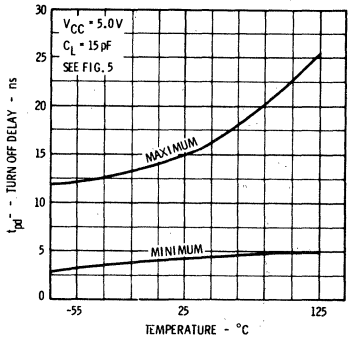
WORST CASE POWER DISSIPATION OF 9005 VERSUS SUPPLY VOLTAGE (PER GATE)



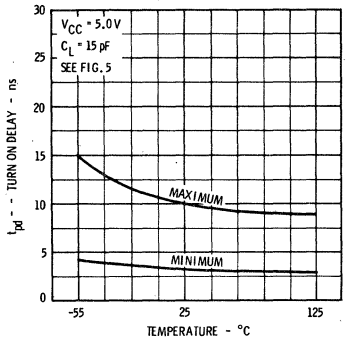
WORST CASE POWER DISSIPATION OF 9008 VERSUS SUPPLY VOLTAGE



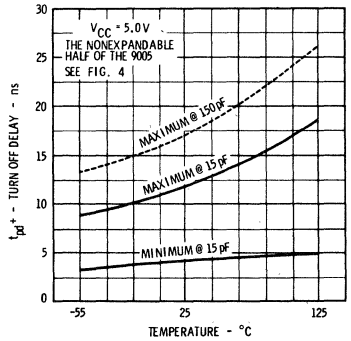
WORST CASE TURN OFF DELAY OF EXPANDABLE GATE VERSUS TEMPERATURE



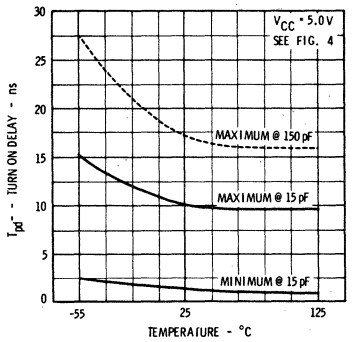
WORST CASE TURN ON DELAY OF EXPANDABLE GATE VERSUS TEMPERATURE



WORST CASE TURN OFF DELAY OF NONEXPANDABLE GATE VERSUS TEMPERATURE

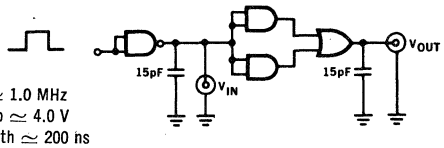


WORST CASE TURN ON DELAY OF NONEXPANDABLE GATE VERSUS TEMPERATURE



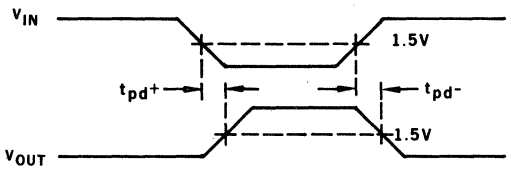
tpd TEST CIRCUIT

9005 NONEXPANDABLE GATE ONLY



f ≃ 1.0 MHz
Amp ≃ 4.0 V
Width ≃ 200 ns
$t_r = t_f \leq 10$ ns

SWITCHING WAVEFORM

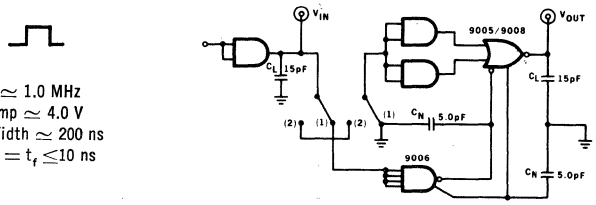


NOTE: Capacitance includes probe and jig capacity.
All inputs are to be tied together.

Figure 4

tpd TEST CIRCUIT

9005/9008 EXPANDABLE GATE AND 9006 EXPANDER



f ≃ 1.0 MHz
Amp ≃ 4.0 V
Width ≃ 200 ns
$t_r = t_f \leq 10$ ns

NOTE: Position (2) is used to test 9005/9008.
Position (1) is used to test 9006.
Capacitance includes probe and jig capacity.

Figure 5

J-K FLIP-FLOPS — 9000, 9001

GENERAL DESCRIPTION — The TTμL family includes the 9000 and 9001 flip-flops to satisfy the storage element needs of a logic system. Each is a master-slave JK flip-flop with the same multi-emitter inputs and low impedance active pull-up outputs common to the gate elements.

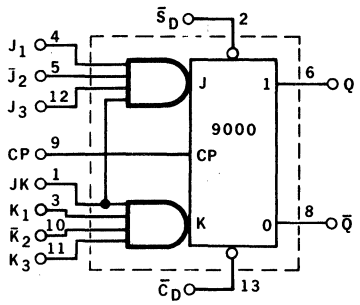
The internal JK connections assure the user of non-ambiguous operation for all input states. The master-slave design with buffered clock input offers high noise immunity, low clock loading and eliminates the need for careful control of clock pulse rise or fall times. Data is accepted by the master when the clock is in the low logic state. Transfer from master to slave occurs when the clock goes from the low to the high logic level. When the clock is in the high logic level both J and K inputs are inhibited. For this reason it is desirable to maintain the clock pulse in the high level most of the duty cycle. Direct set and reset inputs provide true asynchronous control of both master and slave flip-flops independent of logic and clock input levels.

A common J-K input is provided which is useful in the physical layout of most logic configurations.

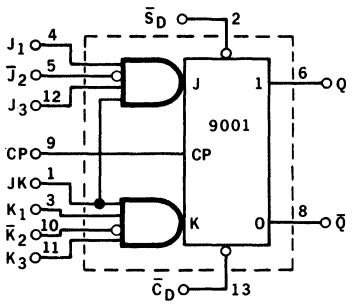
The two circuits are identical with a few exceptions. The 9000 has capacitors at the outputs of the J and K data input gates in the master flip-flop. The capacitors serve to lengthen the time requirements between J or K data and the low-to-high clock transition. This feature makes the 9000 particularly attractive for applications where clock skew is an important consideration.

The 9001 provides one $\overline{J}$ and one $\overline{K}$ input for additional logic flexibility. It has no master flip-flop capacitors to extend the set-up time and therefore has a higher toggling rate.

The important characteristics of the two flip-flops are illustrated in the following curves and specifications. Noise immunity and operating level curves shown in the gate section of the data sheet are applicable to the flip-flops as well.



VCC = PIN 14
GND = PIN 7



V_{CC} = PIN 14
GND = PIN 7

LOADING RULES

FLIP-FLOP INPUTS	LOADING*
CP, J_1, J_2, J_3, K_1, K_2, K_3, $\overline{J}_2$, $\overline{K}_2$,	1
JK	2
$\overline{S}_D$, $\overline{C}_D$	2.7

OUTPUTS	FAN-OUT
Q, $\overline{Q}$	10

*1 load=1 TTμL Gate Input Load

TRUTH TABLES

SYNCHRONOUS ENTRY
J-K MODE OPERATION

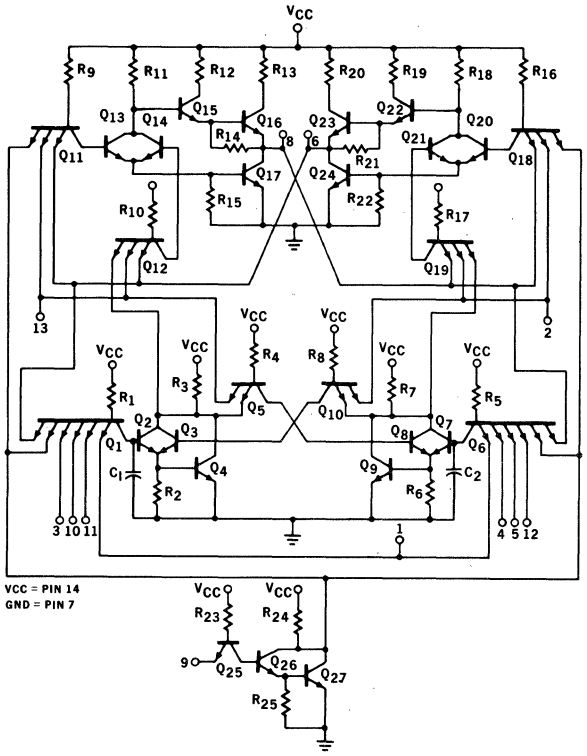
INPUTS @ t_n			OUTPUTS @ t_{n+1}	
JK	(5) $J_1 \cdot J_2 \cdot J_3$	(5) $K_1 \cdot K_2 \cdot K_3$	Q	$\overline{Q}$
1	4 5 12	3 10 11	6	8
L	X	X	No Change (4)	
H	L	L	No Change (4)	
H	L	H	L	H
H	H	L	H	L
H	H	H	Toggles	

ASYNCHRONOUS ENTRY
Independent of Clock and Synchronous Input

INPUTS		OUTPUTS	
S_D	C_D	Q	$\overline{Q}$
2	13	6	8
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

NOTES:
(1.) H = Most positive logic level.
(2.) L = Most negative voltage level.
(3.) X = Could be high or low.
(4.) For no change of outputs, the J and K inputs or the common JK input must remain low from the time the clock goes low to the time the clock goes high again.
(5.) The 9001 has inverted J_2 (Pin 5) and K_2 (Pin 10) inputs. When not in use, they must be grounded.

9000 SCHEMATIC DIAGRAM



TYPICAL COMPONENT VALUES

$R_1, R_4, R_5, R_8, R_{10}, R_{14}, R_{17}, R_{21}, R_{22}, R_{23}, R_{24} = 4\ k\Omega$

$R_2, R_3, R_6, R_7 = 2\ k\Omega$

$R_9, R_{16} = 6\ k\Omega$

$R_{11}, R_{18} = 1.5\ k\Omega$

$R_{12}, R_{19} = 150\ \Omega$

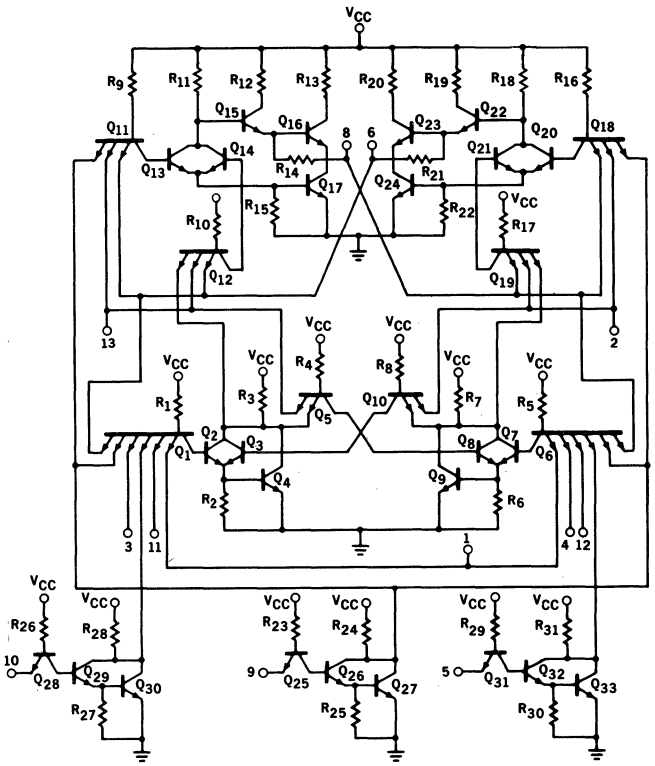
$R_{13}, R_{20} = 80\ \Omega$

$R_{15}, R_{22}, R_{25} = 1.25\ k\Omega$

$C_1, C_2 = 10\ pF$

Figure 6

9001 SCHEMATIC DIAGRAM



TYPICAL COMPONENT VALUES

$R_1, R_4, R_5, R_8, R_{10}, R_{14}, R_{17}, R_{21}, R_{22}, R_{23}, R_{24}, R_{26}, R_{29} = 4\ k\Omega$

$R_2, R_3, R_6, R_7 = 2\ k\Omega$

$R_9, R_{16}, R_{28}, R_{31} = 6\ k\Omega$

$R_{11}, R_{18} = 1.5\ k\Omega$

$R_{12}, R_{19} = 150\ \Omega$

$R_{13}, R_{20} = 80\ \Omega$

$R_{15}, R_{22}, R_{25}, R_{27}, R_{30} = 1.25\ k\Omega$

Figure 7

9000 AND 9001 FUNCTIONAL LOGIC DIAGRAM

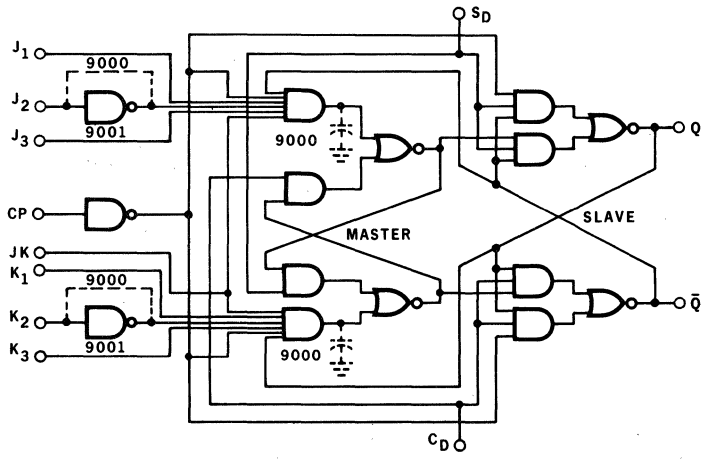


Figure 8

J-K FLIP-FLOPS — 9000, 9001 (continued)

ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = 1.0 mA, V_{IL} on asynchronous input	
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 14.5 mA V_{CC} = 5.5 V, I_{OL} = 17.7 mA	
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs	
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs	
	Input Leakage Current								μA	V_{CC} = 5.5 V, V_R = 4.5 V,	
I_R	J, K, J, K & Clock Inputs				20	60		100		Gnd. on other inputs	
$2\ I_R$	J-K Input				40	120		200			
I_{RS}	Asynchronous Inputs				55	162		270			
	Input Load Current								mA		
I_F	J, K, J, K & Clock Inputs		−1.76		−1.1	−1.76		−1.76		V_{CC} = 5.5 V	V_F = 0.4 V
$2\ I_F$	J-K Input		−3.52		−2.2	−3.52		−3.52		V_{CC} = 5.5 V	V_R = 4.5 V
I_{FSI}	Asynchronous Inputs		−4.75		−3.0	−4.75		−4.75		V_{CC} = 5.5 V	on other inputs
	Input Load Current								mA		
I_F	J, K, J, K & Clock Inputs		−1.45		−0.91	−1.45		−1.45		V_{CC} = 4.5 V	
$2\ I_F$	J-K Input		− 2.9		−1.82	− 2.9		−2.9		V_{CC} = 4.5 V	
I_{FSI}	Asynchronous Inputs		− 3.92		−2.48	−3.92		−3.92		V_{CC} = 4.5 V	
t_{pd+}				—	12	20			ns	9000 or 9001	
t_{pd-}				—	18	30			ns	9000 or 9001	V_{CC} = 5.0 V C_L = 15 pF See test circuits and curves.
$t_{release}$	See Fig. 8				5	1			ns	9001 only	
t_{set-up}	See Fig. 8			10	6				ns	9001 only	
	Negative Clock pulse width			15	10				ns	9001 only Toggle condition	

WORST CASE POWER DISSIPATION VERSUS CLOCK INPUT FREQUENCY

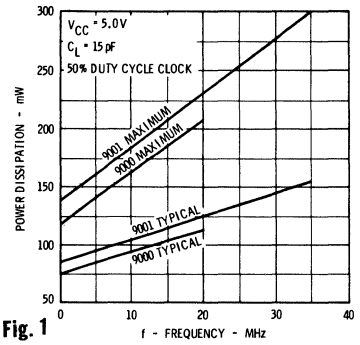


Fig. 1

9000 & 9001 WORST CASE MAX. & MIN. t_{pd+} & t_{pd-} PROPAGATION DELAYS — CP TO OUTPUTS

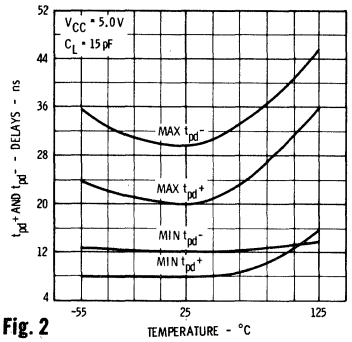


Fig. 2

9000 & 9001 WORST CASE MAX. & MIN. t_{pd+} & t_{pd-} PROPAGATION DELAYS — ASYNCHRONOUS INPUTS TO OUTPUTS

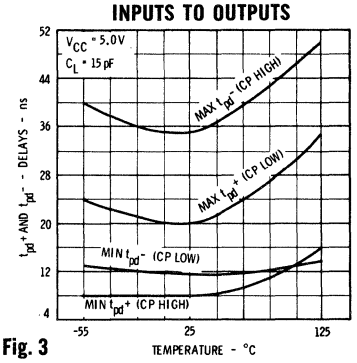


Fig. 3

INCREASE IN ASYNCHRONOUS OR CLOCK INPUT t_{pd+} AND t_{pd-} DUE TO OUTPUT CAPACITANCE

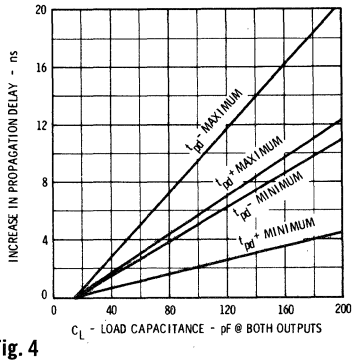


Fig. 4

9001 WORST CASE SET-UP/RELEASE TIME & NEG. CLOCK PULSE WIDTH

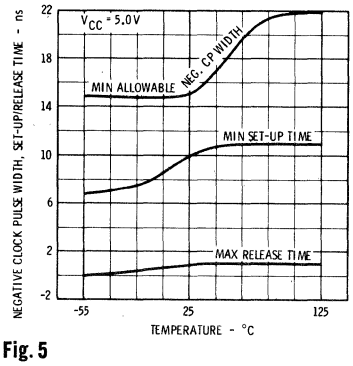


Fig. 5

J-K FLIP-FLOPS — 9000, 9001 (continued)

SWITCHING TIME TEST CIRCUITS

9000

t_{pd+} and t_{pd-}

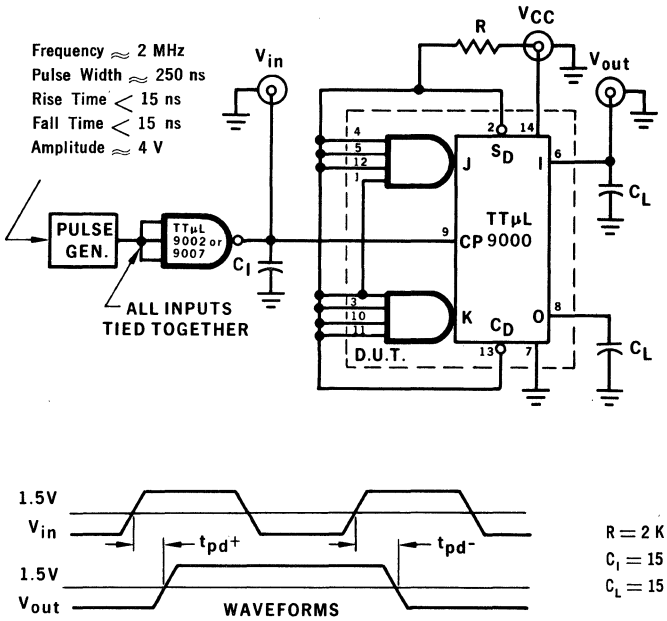


Figure 9

9001

t_{pd+} and t_{pd-}

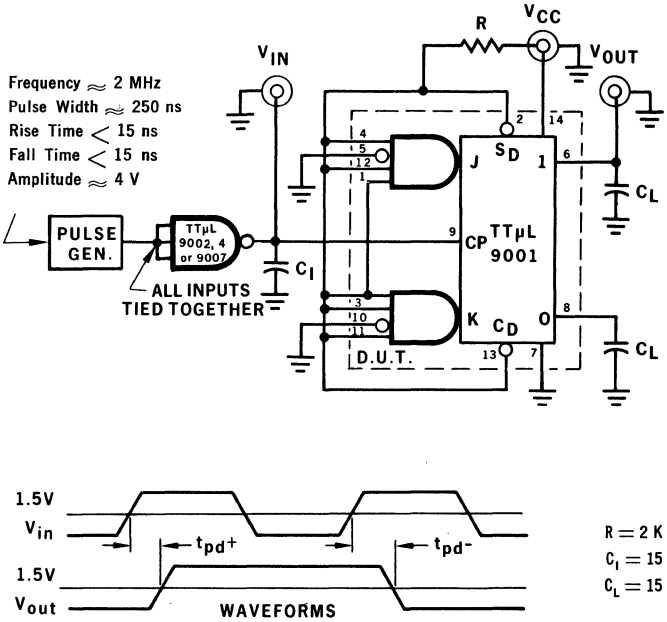


Figure 10

SWITCHING NOTES

(1) The load capacitance indicated in test circuits includes the capacitance of probe and jig.

(2) All curves represent worst case composites of the behavior of limit devices. A typical device will not necessarily follow the temperature trend indicated by the curve, but should always be better than the worst case curve at any temperature in the range.

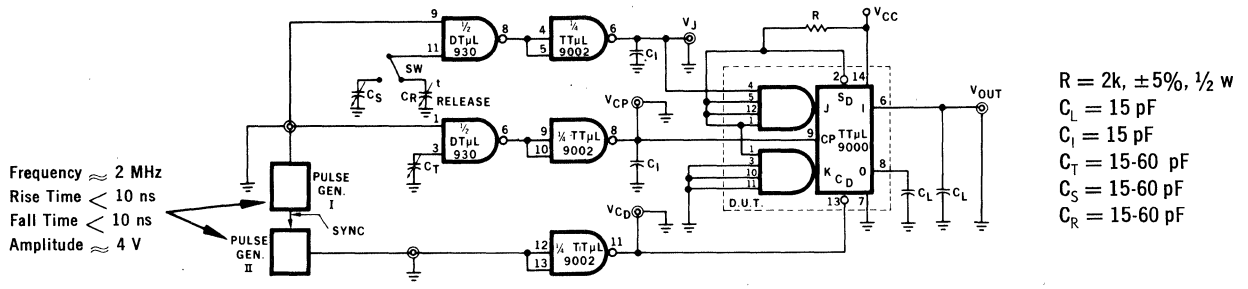
(3) Sensitivity of all switching parameters to supply voltage change (within range of 5 V ± 10%) and D.C. loading is very small.

(4) Figure 4 should be used with Figs. 2 and 3 to determine worst case delays with capacitive loading greater than 15 pF.

(5) Allowable clock skew $\leq t_{pd+}$ (min.) + $t_{release}$ (max.)

J-K FLIP-FLOPS — 9000, 9001 (continued)

9000 t_{set-up} and $t_{release}$ TEST CIRCUIT



R = 2k, ±5%, ½ w
C_L = 15 pF
C_I = 15 pF
C_T = 15-60 pF
C_S = 15-60 pF
C_R = 15-60 pF

INITIAL ADJUSTMENT

1. With switch in t release position adjust pulse generators, C_T & C_R for proper V_{CP}, V_J & V_D waveforms and t release limit value.
2. With switch in t set-up position adjust C_S for t set-up limit value

t set-up is defined as the minimum time required for a ONE to be present at the logic input prior to the clock transition from low to high in order for the flip flop to respond.

t release is defined as the maximum time allowed for a ONE to be present at the logic inputs prior to the clock transition from low to high in order for the flip flop **not** to respond.

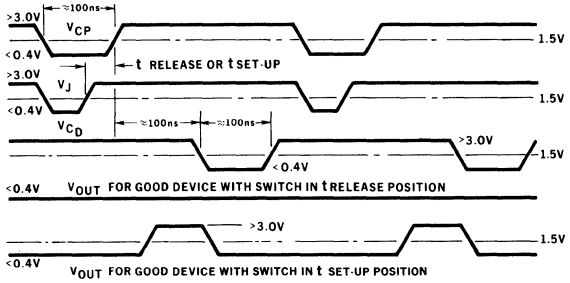
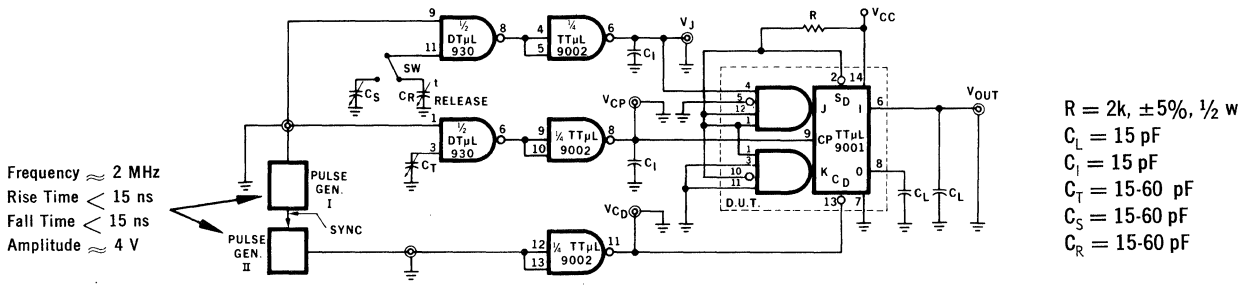


Figure 11

9001 t_{set-up} and $t_{release}$ TEST CIRCUIT



R = 2k, ±5%, ½ w
C_L = 15 pF
C_I = 15 pF
C_T = 15-60 pF
C_S = 15-60 pF
C_R = 15-60 pF

INITIAL ADJUSTMENT

1. With switch in t release position adjust pulse generators, C_T & C_R for proper V_{CP}, V_J & V_D waveforms and t release limit value.
2. With switch in t set-up position adjust C_S for t set-up limit value

t set-up is defined as the minimum time required for a ONE to be present at the logic input prior to the clock transition from low to high in order for the flip flop to respond.

t release is defined as the maximum time allowed for a ONE to be present at the logic inputs prior to the clock transition from low to high in order for the flip flop **not** to respond.

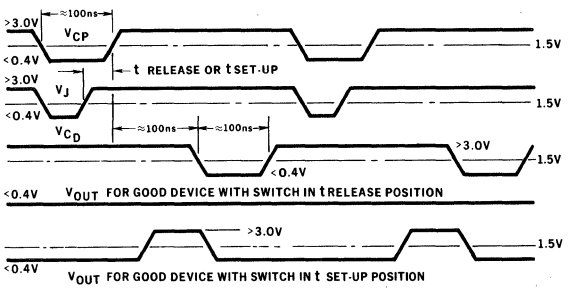


Figure 12

CCSL COMPOSITE DATA SHEET

COMPATIBLE CURRENT SINKING LOGIC

-55°C TO +125°C TEMPERATURE RANGE

CCSL LOADING RULES

The first step towards realization of a compatable logic family is to establish optimized input-output logic levels. These levels. determine the noise immunity for all the elements, as well as the basis for system interfacing.

Fairchild CCSL loading rules guarantee the optimum logic levels over the full military temperature range of -55°C to +125°C with V_{CC} supply within the range of 5V ± 0.5V. These same logic levels, as well as the input load and output drive factors are also guaranteed over the temperature range of -20°C to +100°C, for all CCSL elements. These guaranteed levels are:

Low level output voltage (V_{OL}) = 0.4V
High level output voltage (V_{OH}) = 2.5V
Low level input voltage (V_{IL}) = 0.7V
High level input voltage (V_{IH}) = 2.1V

Noise immunity is derived from the above numbers according to the following equations.

1. High level noise immunity = $V_{OH} - V_{IH}$
2. Low level noise immunity = $V_{IL} - V_{OL}$

Once the logic levels and DC noise margins are established, interfacing rules can be resolved. To simplify input loading and output drive capability, load factors and drive factors were assigned to each element.

These factors are written as a ratio, but are not defined as an arithmetic ratio. The numerator can be added or subtracted independent of the denominator and vice versa. This ratio form was chosen for convenient loading rule analysis.

$$\text{Load Factor} \equiv \frac{\text{High Level Load Factor}}{\text{Low Level Load Factor}} \text{ (Shown as ratio on inputs to circuits)}$$

$$\text{Drive Factor} \equiv \frac{\text{High Level Drive Factor}}{\text{Low Level Drive Factor}} \text{ (Shown as ratio on outputs of circuits)}$$

Where:

High Level Load Factor = Input current drawn into the inputs, during the High Input Level State.
Low Level Load Factor = Input current drawn out of the input during the Low Input Level State.
High Level Drive Factor = Ability of the output to supply current out of the output during the High Output Level State.
Low Level Drive Factor = Ability of the output to sink current into the output during the Low Output Level State.

A necessary condition is that the High Level Drive Factor must be equal to or greater than the sum of the Driven High Level Load Factors and the Low Level Drive Factor must be equal to or greater than the sum of the Driven Low Level Load Factors. Both High Level Drive and Load factors and Low Level Drive and Load factors must be considered if efficient interfacing is to be accomplished.

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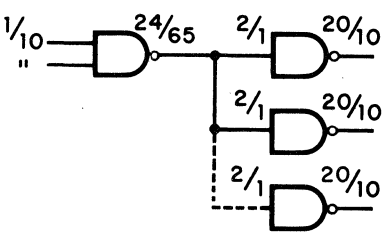
The load factors given are based on worst case conditions at both -55°C and +125°C. Input Low Level Load Factors are guaranteed with the Low Level Output Voltage (V_{OL}) applied to the inputs. Input High Level Load Factors are tested with arbitrarily selected voltages much higher than the V_{OH} value.

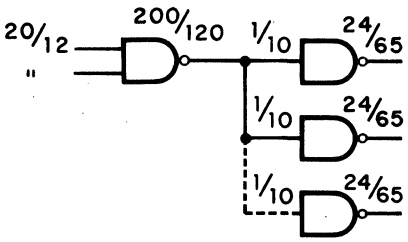
If the temperature range is restricted to -40°C to +110°C or the V_{CC} range to 4.75 to 5.25V, a 10% increase in drive factors may be used.

Examples: A.



(1) DTuL Gate (6K pullup) driving LPDTL Gates

B.



(2) TTL gate driving DTL Gates

Example A

Maximum load = 12 LPDTL gates. Limited by the high level drive capabilities. In this case the Low Level Load is only 12, and the drive capability is 65. Reference to the curves shown in Figure 1, will show this node to have a maximum V_{OL} = 100mV and therefore a worst case Low level noise immunity of 0.6 volts.

Example B

Maximum load - 12 DTL gates, limited by low level drive capabilities. Here the high level load = 12 and the drive capability is 200.

LIMITED LOADING APPLICATIONS

The curves shown in Figures 1, and 2 show improvements in the low level noise margin for TTL and DTμL. DTμL is shown with 6K or 2K pullup resistors.

Example: A TTL gate type output can drive a maximum of 120 low level loads and meet a guaranteed V_{OL} of 0.40 volts. If, however, this same output is only driving 50 low level loads, the worst case V_{OL} at that output would be 0.20 volts and the worst case low level noise immunity would be 0.50 volts.

Figure 2 shows similar low level curves for the TTL and DTμL Buffers.

Figure 3 shows the increase of V_{OH} of a DTμL output high level if the high level loads are less than the maximum specified in the CCSL loading rules. This drive is determined by using a -30% tolerence resistor and is guaranteed by D.C. testing.

Figure 4 shows changes in V_{OH} for DTμL devices which have 2K pullup resistor. The test point guarantees a V_{OH} 4.0 volts with 24 high level loads being driven. The increased number of loads which can be driven and still meet the CCSL V_{OH} of 2.5 volts is based on a worst case maximum tolerance pullup resistor as determined by D.C. testing. If less than 24 high level loads are driven, the increase in V_{OH} is determined by the worst case minimum tolerance pullup resistor.

TTL and LPDTμL devices having active pullups are relatively immune to changes in the high level loads. Their V_{OH} level is primarily set by being $2V_{BE}$'s below V_{CC}.

SPECIAL APPLICATIONS

When using the DTμL 9944 element, the following currents represent unit loads, and must be considered when choosing different external collector resistors.

		-55 C	+25 C	-125 C
V_{CC} = 4.5V	High Level	3μA	3μA	5μA
	Low Level	.121mA	Not worst case	Not worst case
V_{CC} = 5.5V	High Level	Not worst case	Not worst case	Not worst case
	Lower Level	.151mA	.154mA	.146mA

"WIRED OR" APPLICATIONS

For elements 9930, 9962, 9946 and 9936 add 24 to the High Level Drive Factor and subtract 9 from the Low Level Drive Factor for each added gate.

For elements 9041, 9043, 9046 and 9048 using one internal 15Ω pull-up resistor the High Level Drive Factor becomes 14 and the Low Level Drive Factor becomes 7. Subtract 2 from the High Level Drive Factor for each added gate.

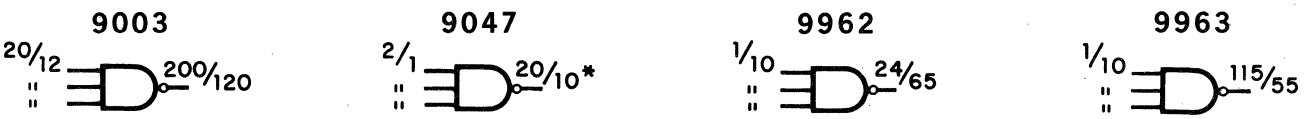
Note 1

If the minimum temperature is limited to -30°C, the Low Level Drive Factor is 12.

CCSL INPUT LOAD & DRIVE FACTORS

QUAD 2-INPUT NAND GATES

TRIPLE 3-INPUT NAND GATES



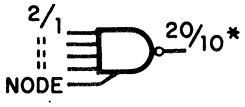
*See Note 1

CCSL INPUT LOAD & DRIVE FACTORS

DUAL 4-INPUT NAND GATES

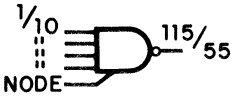
9004

9044



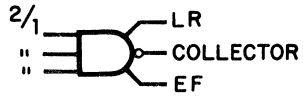
9930

9961

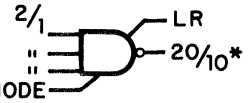


DUAL 3-INPUT NAND GATES

9041



9042



LR=LOAD RESISTOR OUTPUT, EF=EMITTER FOLLOWER OUTPUT

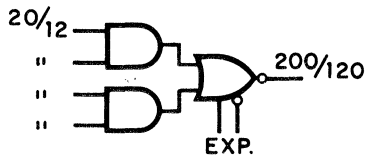
3 & 4-INPUT NAND GATES

9043

LR=LOAD RESISTOR OUTPUT

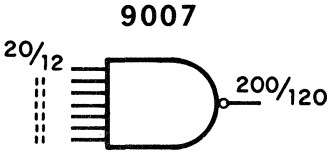
DUAL AND/NOR FUNCTION

9005



EIGHT-INPUT NAND GATE

9007



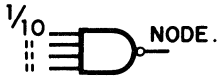
*See Note 1

CCSL INPUT LOAD & DRIVE FACTORS

DUAL 4-INPUT EXPANDERS

9006

9933



HEX INVERTERS

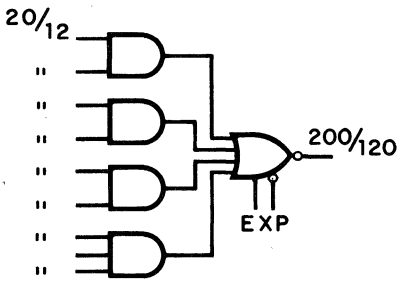
9935

9936

9937

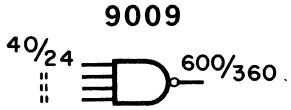
2-2-2-3-INPUT AND/NOR FUNCTION

9008

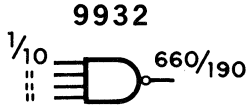


DUAL 4-INPUT BUFFERS

9009



9932



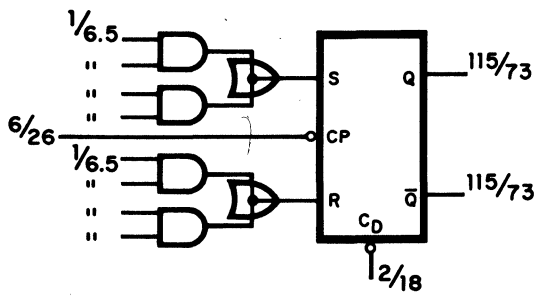
DUAL 4-INPUT DRIVER

9944

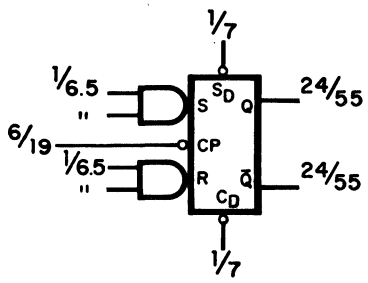
CCSL INPUT LOAD & DRIVE FACTORS

R-S FLIP-FLOPS

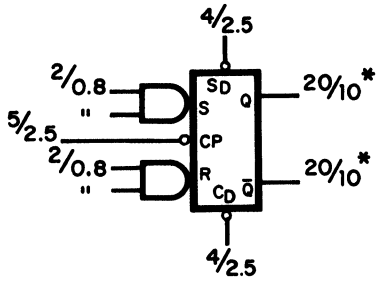
9111



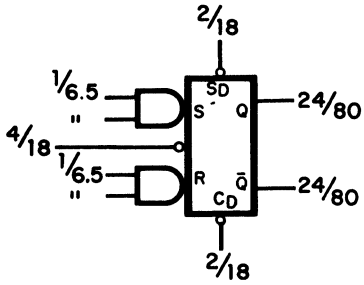
9931



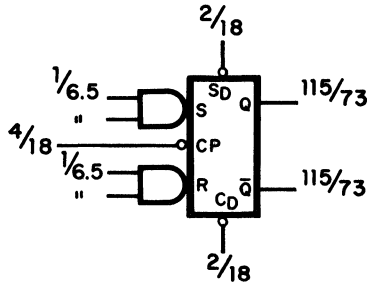
9040



9945

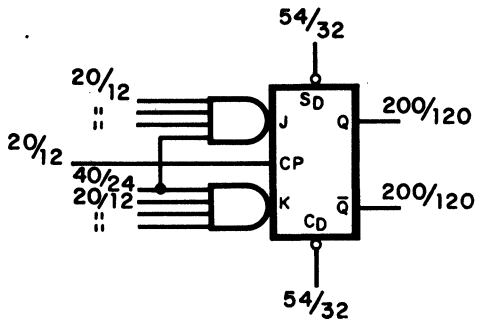


9948

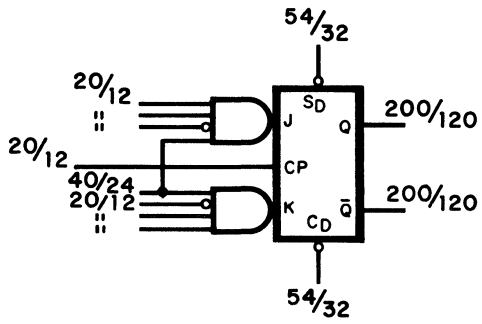


J-K FLIP-FLOPS

9000



9001

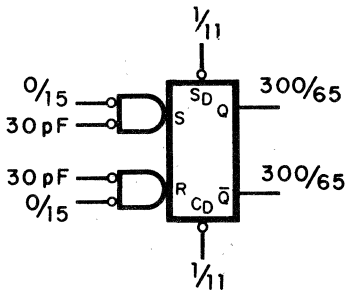


* See Note 1

CCSL INPUT LOAD & DRIVE FACTORS

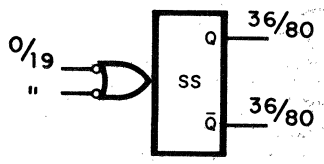
BINARY

9950

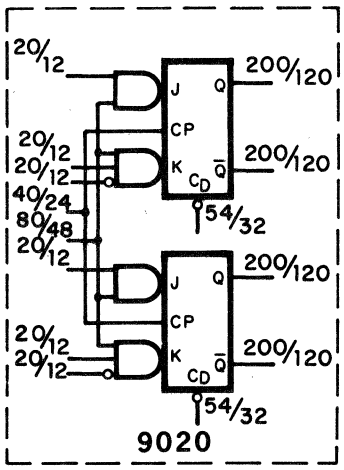


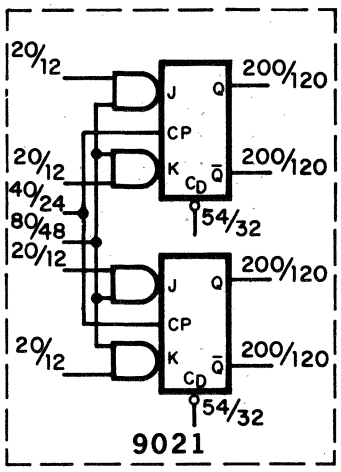
ONE-SHOTS (MONOSTABLE)

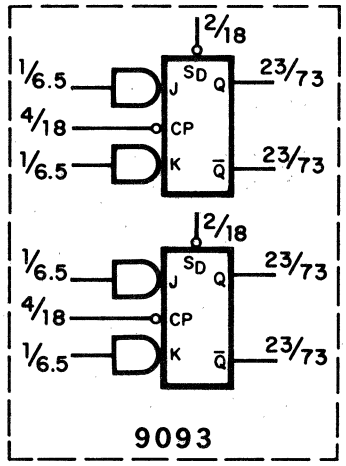
9941 & 9951

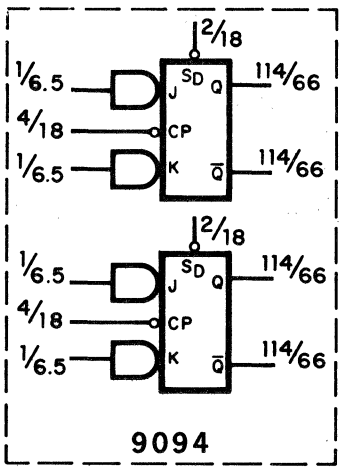


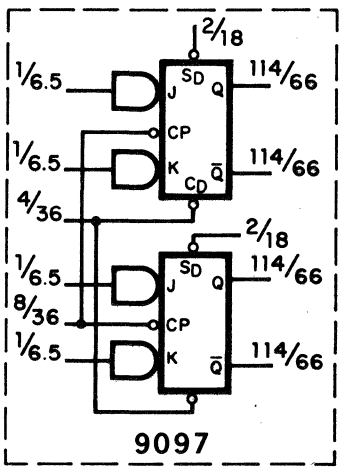
DUAL FLIP-FLOPS

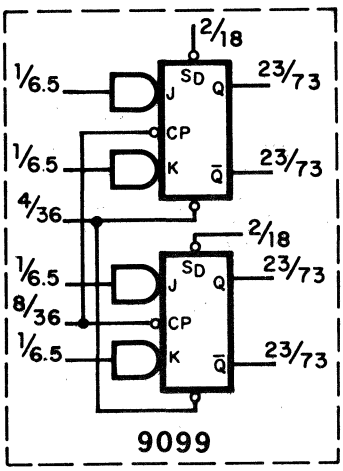






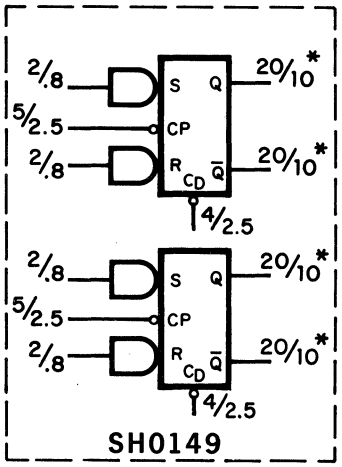




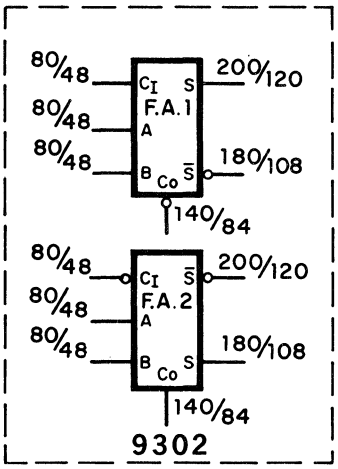


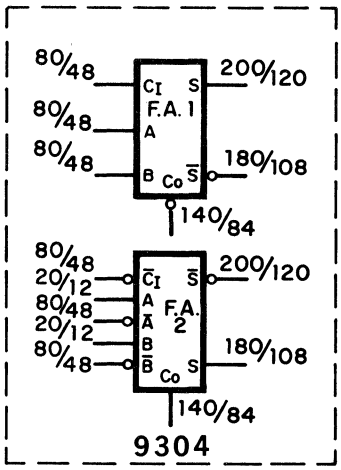
CCSL INPUT LOAD & DRIVE FACTORS

DUAL FLIP-FLOPS (continued)



DUAL FULL-ADDERS





OUTPUT LEVELS VERSUS LOADING

GATE TYPE ELEMENTS

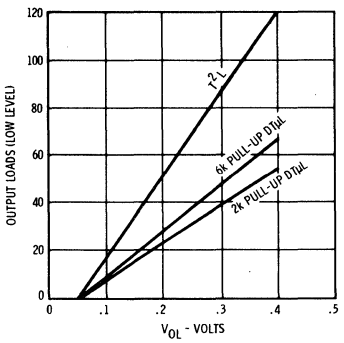


FIG. 1

BUFFER ELEMENTS

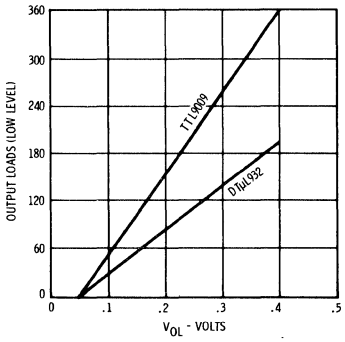


FIG. 2

6k PULL-UP

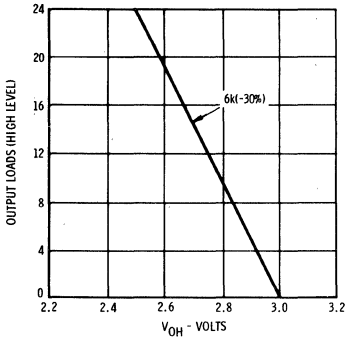


FIG. 3

2k PULL-UP

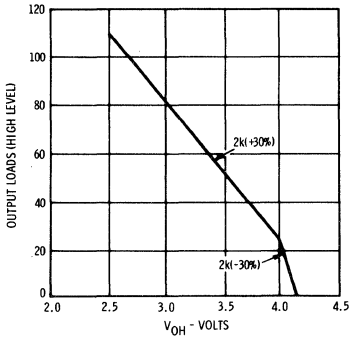


FIG. 4

* See Note 1

TTμL9016

HEX INVERTER

TRANSISTOR-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

A FAIRCHILD COMPATIBLE CUURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION

The 9016 consists of six TTμL gates where each gate performs a single inversion function. Designed for high speed operation, the 9016 is very useful where a number of complement signals are desired simultaneously.

FEATURES

- High Speed Operation
- Input Diode Clamping
- High Capacitive Drive Capability
- The input/output characteristics provide easy interfacing with Fairchild DTμL, LPDTμL, TTμL and MSI families (CCSL.)
- All ceramic "HERMETIC" packages

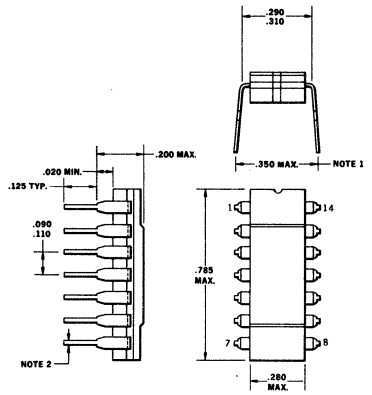
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5V to +8V
Input Voltage	-0.5V to +5.5V
Voltage Applied to Outputs	-0.5V to +V_{CC} value

ORDER INFORMATION

Specify U3I90165XX for flat package and U6A90165XX for Dual-In-Line package, where 5XX is 51X for -55°C to +125°C temperature range or 59X for the 0°C to +75°C temperature range.

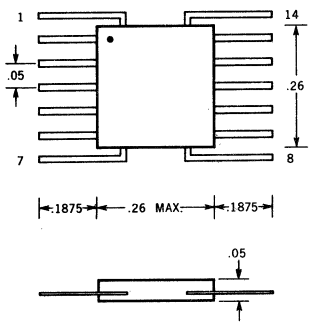
TYPICAL DUAL IN-LINE PACKAGE



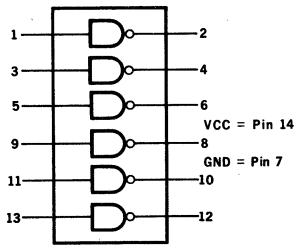
NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

TYPICAL FLAT PACKAGE

TOP VIEW



LOGIC DIAGRAM



FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS 0°C to +75°C, Vcc=5.0V ±5%

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	MAX.	+25°C MIN.	TYP.	MAX.	+75°C MIN.	MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75V, I_{OH} = -1.2 mA V_{IL} = VALUE INDICATED BELOW
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 4.75V, I_{OL} = 14.1 mA V_{CC} = 5.25V, I_{OL} = 16.0 mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs.
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	* Guaranteed input low threshold for all inputs.
I_F	Input Load Current		-1.6		-1.0	-1.6		-1.6	mA	V_{CC} = 5.25V, V_F = 0.45V
I_F	Input Load Current		-1.24		-0.97	-1.24		-1.24	mA	V_{CC} = 4.75V V_F = 0.45V
I_R	Input Leakage Current				15	60		60	μA	V_{CC} = 5.25V, V_R = 4.5V
t_{pd+}	Turn Off Delay			3	8	15			ns	V_{CC} = 5.0V C_L = 15pF
t_{pd-}	Turn On Delay			3	7	13			ns	

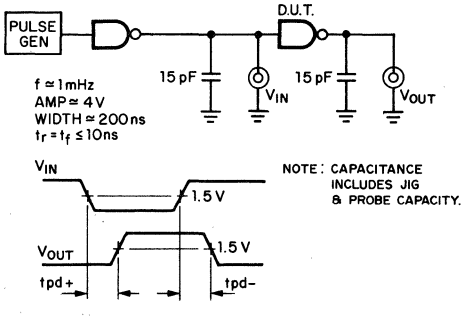
* Pulse Tested (pulse duration = 50 msec.)

ELECTRICAL CHARACTERISTICS −55°C to +125°C, Vcc=5.0V ±10%

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	MAX.	+25°C MIN.	TYP.	MAX.	+75°C MIN.	MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5V, I_{OH} = -1.32mA V_{IL} = VALUE INDICATED BELOW
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 4.5V, I_{OL} = 13.6mA V_{CC} = 5.5V, I_{OL} = 17.6mA
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs.
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	*Guaranteed input low threshold for all inputs.
I_F	Input Load Current		-1.6		-1.10	-1.6		-1.6	mA	V_{CC} = 5.5V V_F = 0.4V
I_F	Input Load Current		-1.24		-0.97	-1.24		-1.24	mA	V_{CC} = 4.5V V_F = 0.4V
I_R	Input Leakage Current				15	60		60	μA	V_{CC} = 5.5V, V_R = 4.5V
t_{pd+}	Turn Off Delay			3	8	12			ns	V_{CC} = 5.0V C_L = 15pF
t_{pd-}	Turn On Delay			3	7	10			ns	

* Pulse Tested (pulse duration = 50 msec.)

tpd TEST CIRCUIT



LOADING RULES

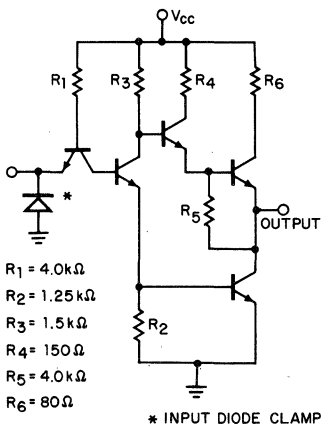
INPUT LEVEL	LOAD FACTOR
HIGH	1
LOW	1

OUTPUT STATE	FANOUT 51X	59X
HIGH	22	20
LOW	11	10

1 HIGH LEVEL LOAD = I_R

1 LOW LEVEL LOAD = I_F

SCHEMATIC DIAGRAM



TTμL 9020

DUAL JK$\overline{K}$ FLIP-FLOP

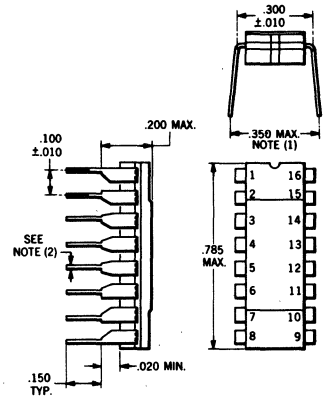
A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION

The 9020 consists of two JK flip-flops with a common clock, separate J, K, and $\overline{K}$ inputs and a common JK input. The JK$\overline{K}$ design allows the 9020 to be operated as a D type flip-flop or as a standard J-K flip-flop. Incorporated in the element is a single clock buffer which reduces clock loading.

The joint (JK) input to the flip-flops can be used to advantage for gating information into the flip-flops. This common input removes the necessity of gating clock waveforms and can result in an improved logic design requiring fewer circuits. It also minimizes clock skew problems if a single clock line is used and all the clock drivers are tied together.

PHYSICAL DIMENSIONS



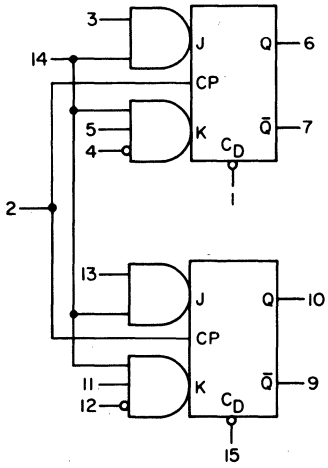
NOTES:

1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 linch diameter lead.

FEATURES

- **50 MHz operation**
- **Master-slave circuit**
- **Common buffered clock input**
- **Separate JK$\overline{K}$ inputs**
- **Common Input Enable logic**
- **Separate Direct Clear inputs**
- **The input/output characteristics provide easy interfacing with Fairchild DTμL, LPDTμL, and MSI families (CCSL).**
- **All ceramic "HERMETIC" 16-pin Dual In-Line package**
- **Input Diode Clamping**

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +8V
Input Voltage	−1.5V to +5.5V
Voltage Applied to Outputs	−0.5V to V_{CC} Value
Current Into Output When Output is Low	50 mA

ORDER INFORMATION

Specify U6B9020XXX for 16 pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

FAIRCHILD
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313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

TRUTH TABLE

SYNCHRONOUS ENTRY J-K MODE OPERATION

INPUTS @ t_n			OUTPUTS @ t_{n+1}	
JK 14	J 3(13)	K • $\overline{K}$ 5(11) • 4(12)	Q 6(10)	$\overline{Q}$ 7(9)
L	X	X	(1)	No Change
H	L	L	(1)	No Change
H	L	H	L	H
H	H	L	H	L
H	H	H	Toggles	

ASYNCHRONOUS ENTRY INDEPENDENT OF CLOCK & SYNCHRONOUS INPUTS

INPUTS	OUTPUTS	
C_D 1(15)	Q 6(10)	$\overline{Q}$ 7(9)
L	L	H
H	No Change	

H = Most positive logic level
L = Most negative logic level
X = Could be high or low

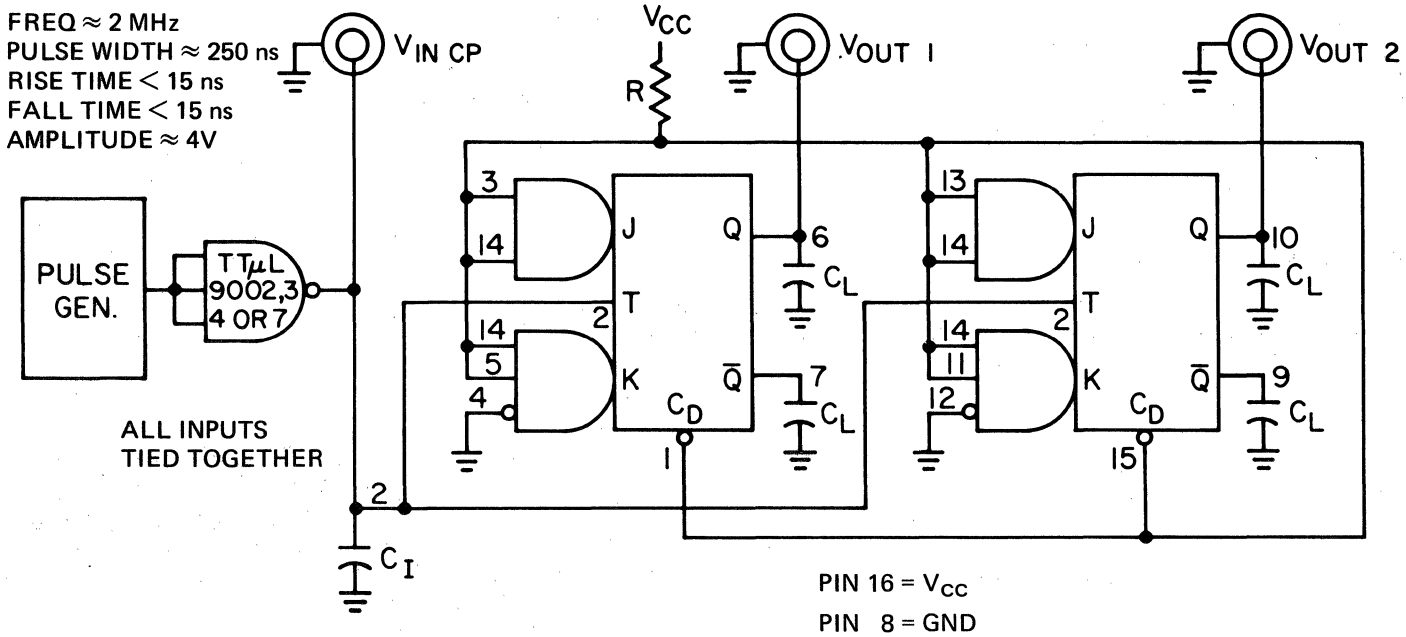
NOTES:

(1) For no change of outputs, the J and K inputs or the common JK input must remain low for the entire period in which the clock pulse is at low logic level.
(2) $\overline{K}$ inputs should be grounded when not in use.

LOADING RULES

INPUTS	LOADING
J, K, $\overline{K}$	1
CP	2
JK	4
CD	2.7
OUTPUTS	**FANOUT**
Q, $\overline{Q}$	10

SWITCHING TIME TEST CIRCUITS:



ELECTRICAL CHARACTERISTICS

INDUSTRIAL TEMPERATURE RANGE 0°C to 75°C, V_{CC} 5.0V ±5%

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	75°C MIN.	75°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75V, I_{OH} = 1.2 mA	
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 4.75V, I_{OL} = 14.1 mA V_{CC} = 5.25V, I_{OL} = 16 mA	
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs.	
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs.	
I_R $2\ I_R$ $4\ I_R$ I_{RS}	J, K, $\overline{K}$ Leakage Current Clock Input J-K Input Asynchronous Inputs				5 10 20 14	60 120 240 160		60 120 240 160	μA	V_{CC} = 5.25V, V_R = 4.5V Gnd. on other inputs.	
I_F $2\ I_F$ $4\ I_F$ I_{FSI}	J, K, $\overline{K}$ Input Current Clock Input J-K Input Asynchronous Inputs		−1.60 −3.20 −6.40 −4.32		−1.0 −2.0 −4.0 −2.7	−1.60 −3.20 −6.40 −4.32		−1.60 −3.20 −6.40 −4.32	mA	V_{CC} = 5.25V	V_F = 0.45V V_R = 4.5V on other inputs.
I_F $2\ I_F$ $4\ I_F$ I_{FSI}	J, K, $\overline{K}$ Input Current Clock Input J-K Input Asynchronous Inputs		−1.41 −2.82 −5.64 −3.78		−0.94 −1.88 −3.76 −2.54	−1.41 −2.82 −5.64 −3.78		−1.41 −2.82 −5.64 −3.78	mA	V_{CC} = 4.75V	
t_{pd+}					13	22			ns		V_{CC} = 5.0V
t_{pd-}					21	35			ns		C_L = 15 pF
$t_{release}$					6	1			ns		
$t_{set\text{-}up}$				12	7				ns		
	Negative Clock pulse width			16	11				ns	Toggle Condition	

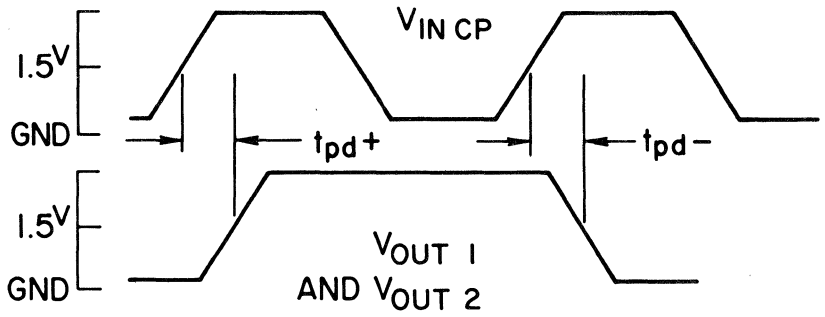
SWITCHING TIME TEST CIRCUITS (Continued)

NOTES:

R = 2K, ±5%, ½W
C_I = 15 pF ±5%
C_L = 15 pF ±5%

C_I & C_L include all probe and jig capacity.
Very short stranded or printed wire should be used for all interconnections.
Probes should be connected directly to the input & output pins.

WAVEFORMS



ELECTRICAL CHARACTERISTICS

MILITARY TEMPERATURE RANGE **–55°C to +125°C, V_{CC} 5.0V ±10%**

SYMBOL	CHARACTERISTIC	LIMITS							UNITS	CONDITIONS & COMMENTS	
		–55°C		25°C			125°C				
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5V, I_{OH} = 1.2 mA	
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 4.5V, I_{OL} = 12.4 mA V_{CC} = 5.5V, I_{OL} = 16 mA	
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs.	
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs.	
I_R $2\ I_R$ $4\ I_R$ I_{RS}	J, K, $\overline{K}$ Leakage Current Clock Input J-K Input Asynchronous Inputs				5 10 20 14	60 120 240 160		60 120 240 160	μA	V_{CC} = 5.5V, V_R = 4.5V Gnd. on other inputs.	
I_F $2\ I_F$ $4\ I_F$ I_{FSI}	J, K, $\overline{K}$ Input Current Clock Input J-K Input Asynchronous Inputs		–1.60 –3.20 –6.40 –4.32		–1.1 –2.2 –4.4 –3.0	–1.60 –3.2 –6.40 –4.32		–1.60 –3.2 –6.40 –4.32	mA	V_{CC} = 5.5V	V_F = 0.4V V_R = 4.5V
I_F $2\ I_F$ $4\ I_F$ I_{FSI}	J, K, $\overline{K}$ Input Current Clock Input J-K Input Asynchronous		–1.24 –2.48 –4.86 –3.29		–0.91 –1.82 –3.64 –2.48	–1.24 –2.48 –4.96 –3.29		–1.24 –2.48 –4.96 –3.29	mA	V_{CC} = 4.5V	on other inputs
t_{pd+}					13	22			ns	Each Flip-Flop	V_{CC} = 5.0V
t_{pd-}					21	35			ns		C_L = 15 pF
$t_{release}$					6	1			ns		
$t_{set\text{-}up}$				12	7				ns		
	Negative Clock pulse width			16	11				ns	Toggle Condition	

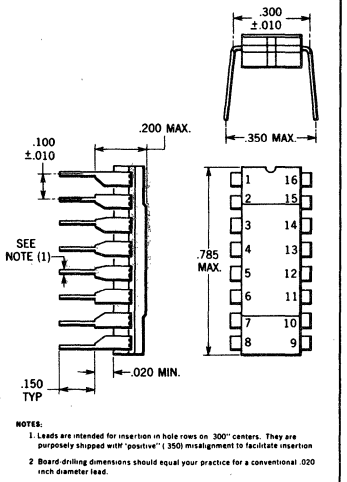
TTμL 9022
DUAL J$\overline{K}$ FLIP-FLOP
A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION

The 9022 consists of two J$\overline{K}$ flip-flops with a common clock, separate J and $\overline{K}$ inputs and a common JK input. The J$\overline{K}$ design allows the 9022 to be operated as a D type flip-flop or as a standard J-K flip-flop. Incorporated in the element is a single clock buffer which reduces clock loading.

The joint (JK) input to the flip-flops can be used to advantage for gating information into the flip-flops. It also minimizes clock skew by allowing separate enable control of flip-flops when they are connected to a common clock buss.

PHYSICAL DIMENSIONS

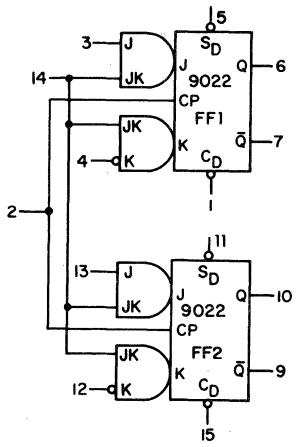


NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

FEATURES

- 35 MHz operation
- Master-slave circuit
- Common buffered clock input
- Separate J$\overline{K}$ inputs
- Common Input Enable logic
- Separate Direct Clear and Direct set inputs
- The input/output characteristics provide easy interfacing with Fairchild DTμL, LPDTμL, and MSI families (CCSL).
- All ceramic "HERMETIC" 16-pin Dual In-Line package
- Input Diode Clamping

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5V to +8V
Input Voltage	-0.5V to +5.5V
Voltage Applied to Outputs	-0.5V to V_{CC} Value
Current Into Output When Output is Low	50 mA

ORDER INFORMATION

Specify U6B9022XXX for 16 pin Dual In-Line package where XXX is 51X for the -55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

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TRUTH TABLE

SYNCHRONOUS ENTRY J-K MODE OPERATION

INPUTS @ t_n			OUTPUTS @ t_{n+1}	
JK 14	J 3(13)	$\overline{K}$ 4(12)	Q 6(10)	$\overline{Q}$ 7(9)
L	X	X	(1)	No Change
H	L	H	(1)	No Change
H	L	L	L	H
H	H	H	H	L
H	H	L	Toggles	

ASYNCHRONOUS ENTRY INDEPENDENT OF CLOCK & SYNCHRONOUS INPUTS

INPUTS		OUTPUTS	
S_D 5(11)	C_D 1(15)	Q 6(10)	$\overline{Q}$ 7(9)
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

H = Most positive logic level

L = Most negative logic level

X = Could be high or low

NOTES:

(1) For no change of outputs, the J and K inputs or the common JK input must remain low ($\overline{K}$ = High) for the entire period in which the clock pulse is at low logic level.

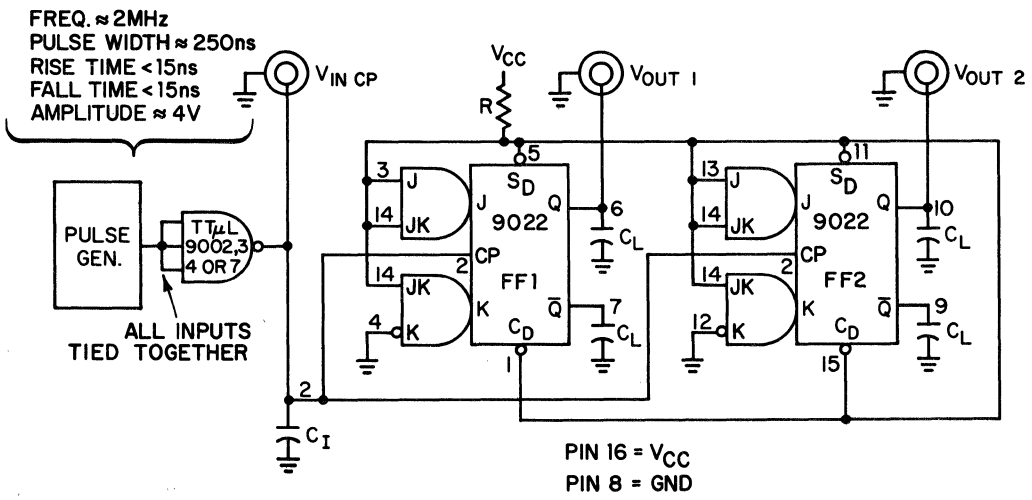
(2) $\overline{K}$ inputs should be grounded when not in use.

LOADING RULES

INPUTS	LOADING
J, $\overline{K}$	1
CP	2
JK	4
C_D & S_D	2.7

OUTPUTS	FANOUT
Q, $\overline{Q}$	10

SWITCHING TIME TEST CIRCUITS



ELECTRICAL CHARACTERISTICS

INDUSTRIAL TEMPERATURE RANGE 0°C to 75°C, V_{CC} 5.0V ±5%

SYMBOL	CHARACTERISTIC	LIMITS							UNITS	CONDITIONS & COMMENTS	
		0°C		25°C			75°C				
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V I_{OH} = -1.2 mA	
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 14.1 mA V_{CC} = 5.25 V, I_{OL} = 16 mA	
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs.	
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs.	
I_R	J,$\overline{K}$ Leakage Current				5	60		60	μA	V_{CC} = 5.25 V, V_R = 4.5 V	
$2I_R$	Clock Input				10	120		120		Gnd. on other inputs.	
$4I_R$	J-K Input				20	240		240			
I_{RS}	Asynchronous Inputs				14	160		160			
I_F	J,$\overline{K}$ Input Current		-1.60		-1.0	-1.60		-1.60	mA	V_{CC} = 5.25 V	V_F = 0.45 V
$2I_F$	Clock Input		-3.20		-2.0	-3.20		-3.20			V_R = 4.5 V
$4I_F$	J-K Input		-6.40		-4.0	-6.40		-6.40			on other inputs.
I_{FSI}	Asynchronous Inputs		-4.32		-2.7	-4.32		-4.32			
I_F	J,$\overline{K}$ Input Current		-1.41		-0.94	-1.41		-1.41	mA	V_{CC} = 4.75 V	
$2I_F$	Clock Input		-2.82		-1.88	-2.82		-2.82			
$4I_F$	J-K Input		-5.64		-3.76	-5.64		-5.64			
I_{FSI}	Asynchronous Inputs		-3.78		-2.54	-3.78		-3.78			
t_{pd+}					12	22			ns		V_{CC} = 5.0 V
t_{pd-}					21	35			ns		C_L = 15 pF
$t_{release}$					6	1			ns		
t_{set-up}				12	7				ns		
	Negative Clock pulse width			16	11				Toggle Condition		

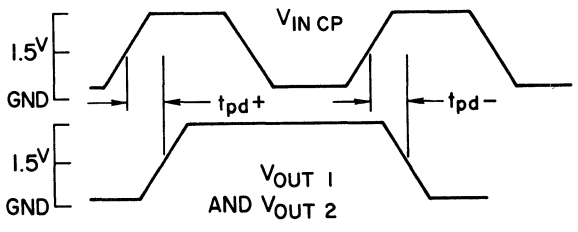
SWITCHING TIME TEST CIRCUITS (Continued)

NOTES:

R = 2K, ±5%, 1/2W
C_I = 15 pF ±5%
C_L = 15 pF ±5%

C_I & C_L include all probe and jig capacity.
Very short stranded or printed wire should be used for all interconnections.
Probes should be connected directly to the input & output pins.

WAVEFORMS



ELECTRICAL CHARACTERISTICS

MILITARY TEMPERATURE RANGE −55°C to +125°C, V_{CC} 5.0V ±10%

SYMBOL	CHARACTERISTICS	LIMITS							UNITS	CONDITIONS & COMMENTS	
		-55°C		25°C			125°C				
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = -1.2 mA	
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 12.4 mA V_{CC} = 5.5 V, I_{OL} = 16 mA	
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs.	
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs.	
I_R	J,$\overline{K}$ Leakage Current				5	60		60	μA	V_{CC} = 5.5 V, V_R = 4.5 V	
$2I_R$	Clock Input				10	120		120		Gnd. on other inputs.	
$4I_R$	J-K Input				20	240		240			
I_{RS}	Asynchronous Inputs				14	160		160			
I_F	J,$\overline{K}$ Input Current		-1.60		-1.1	-1.60		-1.60	mA	V_{CC} = 5.5 V	V_F = 0.4 V
$2I_F$	Clock input		-3.20		-2.2	-3.2		-3.2			
$4I_F$	J-K Input		-6.40		-4.4	-6.40		-6.40			
I_{FSI}	Asynchronous Inputs		-4.32		-3.0	-4.32		-4.32			V_R = 4.5 V
I_F	J,$\overline{K}$ Input Current		-1.24		-0.91	-1.24		-1.24	mA	V_{CC} = 4.5 V	on other inputs
$2I_F$	Clock Input		-2.48		-1.82	-2.48		-2.48			
$4I_F$	J-K Input		-4.86		-3.96	-4.96		-4.96			
I_{FSI}	Asynchronous		-3.29		-2.48	-3.29		-3.29			
t_{pd+}					12	22			ns	Each Flip-Flop	V_{CC} = 5.0 V
t_{pd}					21	35			ns		C_L = 15 pF
$t_{release}$					6	1			ns		
$t_{set\text{-}up}$				12	7				ns		
	Negative Clock pulse width			16	11				ns	Toggle Condition	

MμL9033

16-BIT MEMORY CELL

MEMORY MICROLOGIC® INTEGRATED CIRCUITS

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The MμL9033 is a Planar* epitaxial integrated 16-bit, bit-oriented, non-destructive readout memory cell, compatible with Fairchild Transistor-Transistor Micrologic® (TTμL) and other Compatible Current-Sinking Logic (CCSL) integrated circuits. This memory cell, organized as 16 words by one bit, is designed for high-speed scratch-pad memory applications.

OPERATION — The memory cell consists of 16 R-S flip-flops arranged in an addressable four-by-four matrix. The desired bit location is selected by raising the coincident X-Y address lines to a logic "H" level (>2.1 volts) and holding the non-selected address lines at logic "L" level (<0.7 volts). As many as four locations may be addressed simultaneously without destroying stored information. The stored data and its complement at the addressed bit location may be read at the output terminals. If the addressed bit location contains a "1", the S_1 output will be low and the S_0 output will be high. If the addressed bit location contains a "0", the S_1 output will be high and the S_0 output will be low.

Writing is accomplished by activating one of the write amplifiers. To write a "1", the desired bit location is addressed and the input of the "write one" (W_1) amplifier is raised to a High level. To write a "0", the input of the "write zero" (W_0) amplifier is raised to a High level.

The outputs are open-collector, which may be wire "OR"ed for word expansion. (The output transistors are off when none of the bits are selected.) An external resistor should be returned to V_{CC} to pull-up the wire "OR"ed outputs.

FEATURES

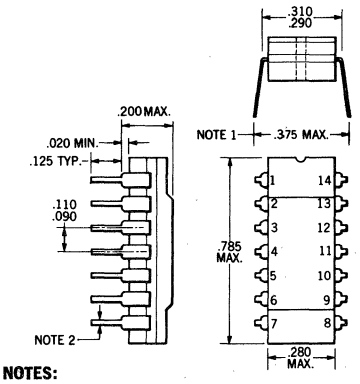
- **CCSL COMPATIBLE**
- **OUTPUT WIRED-OR CAPABILITY**
- **TRUE AND COMPLEMENTARY OUTPUTS ARE PROVIDED**
- **NON DESTRUCTIVE READ OUT**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground	−0.5 V to +8.0 V
Input Pin Voltage	−1.5 V to +5.5 V
Current Into Output Terminal	100 mA
Output Voltage	−0.5 V to +8.0 V

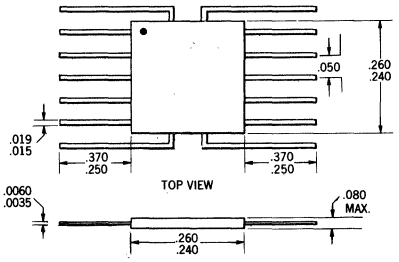
ORDER INFORMATION — Specify A3I9033XXX for Flat Package or A6A9033XXX for Dual In-Line (TO-116) package where XXX is 51X for −55°C to 125°C temperature range or 59X for the 0°C to 75°C range. The last digit in the order code is 1 for 40 mA Fanout and 2 for 20 mA Fanout.

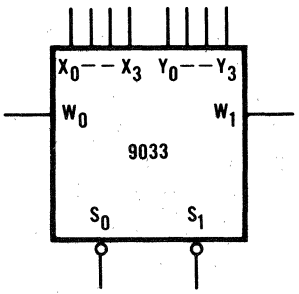
PHYSICAL DIMENSIONS
In Accordance With
JEDEC (TO-116) Outline
Dual In-Line Package



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

PHYSICAL DIMENSIONS
In Accordance With
JEDEC (TO-86) Outline
CERPAK I 14 lead





*Planar is a patented Fairchild process.

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ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	TEST	LIMITS MIN.	LIMITS MAX.	UNITS	TEST CONDITIONS
I_{FX}	X Address Input Load Current		11	mA	$V_{CC} = 5.5\ V$, $V_X = 0\ V$, $V_Y = 4.5\ V$, other X inputs grounded
I_{FY}	Y Address Input Load Current		11	mA	$V_{CC} = 5.5\ V$, $V_Y = 0\ V$, $V_X = 4.5\ V$, other Y inputs grounded
I_{RX}	X Address Input Leakage Current		400	μA	$V_{CC} = 5.5\ V$, $V_X = 4.5\ V$, other X and Y inputs grounded
I_{RY}	Y Address Input Leakage Current		400	μA	$V_{CC} = 5.5\ V$, $V_Y = 4.5\ V$, other X and Y inputs grounded
I_{FW}	Write Input Load Current		1.5	mA	$V_{CC} = 5.5\ V$, $V_W = 0\ V$
I_{RW}	Write Input Leakage Current		100	μA	$V_{CC} = 5.5\ V$, $V_W = 4.5\ V$,
I_{CC}	Power Supply Current		65	mA	$V_{CC} = 5.5\ V$, All Inputs Grounded
I_{BV}	Power Supply Current at $V_{CC} = 7\ V$		84	mA	$V_{CC} = 7.0\ V$, All Inputs Grounded
I_{CEX}	Output Leakage Current		250	μA	$V_{CC} = 5.5\ V$, $V_{CEX} = 5.5\ V$, all inputs grounded
V_{OL}	Output Low Voltage		0.45	V	$V_{CC} = 4.5\ V$, One Bit Selected $I_{OL} = 20\ mA$ (A6A9033512 - A3F9033512)
$V_{XY(W)}$	Address Input Threshold to Prevent Writing		0.75	V*	$V_{CC} = 5.0\ V$, other X and Y grounded. Alternately pulse W_0 and W_1, cell must not change state.
$V_{XY(W)}$	Address Input Threshold to insure Writing	2.1		V*	$V_{CC} = 5.0\ V$, other X and Y grounded. Alternately pulse W_0 and W_1, cell state must alternate.
$V_{XY(R)}$	Address Input Threshold to Prevent Reading		0.8	V	$V_{CC} = 5.0\ V$, other inputs grounded. Both outputs must be on "high" state.
$V_{XY(R)}$	Address Input Threshold to Insure Reading	2.1		V*	$V_{CC} = 5.0\ V$, other X and Y grounded. Alternately pulse W_0 and W_1, cell state must alternate.
$V_{W(W)}$	Write Input Threshold to Prevent Writing		0.8	V*	$V_{CC} = 5.0\ V$, one X and one Y to 4.5 V, other X and Y grounded. One write input to $V_{W(W)}$, pulse the other write input. If W_0 is pulsed, S_0 will assume low state. If W_1 is pulsed, S_1 will assume low state.
$V_{W(W)}$	Write Input Threshold to Insure Writing	2.1		V*	$V_{CC} = 5.0\ V$, one X and one Y to 4.5 V, other X and Y grounded. One write input to $V_{W(W)}$, pulse the other write input. If W_0 is pulsed, S_1 will assume low state. If W_1 is pulsed, S_0 will assume low state.

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	TEST	LIMITS MIN.	LIMITS MAX.	UNITS	TEST CONDITIONS
I_{FX}	X Address Input Load Current		11	mA	$V_{CC} = 5.25\ V$, $V_X = 0\ V$, $V_Y = 4.5\ V$, other X inputs grounded
I_{FY}	Y Address Input Load Current		11	mA	$V_{CC} = 5.25\ V$, $V_Y = 0\ V$, $V_X = 4.5\ V$, other X inputs grounded
I_{RX}	X Address Input Leakage Current		400	μA	$V_{CC} = 5.25\ V$, $V_X = 4.5\ V$, other X and Y inputs grounded
I_{RY}	Y Address Input Leakage Current		400	μA	$V_{CC} = 5.25\ V$, $V_Y = 4.5\ V$, other X and Y inputs grounded
I_{FW}	Write Input Load Current		1.5	mA	$V_{CC} = 5.25\ V$, $V_W = 0\ V$
I_{RW}	Write Input Leakage Current		100	μA	$V_{CC} = 5.25\ V$, $V_W = 4.5\ V$
I_{CC}	Power Supply Current		65	mA	$V_{CC} = 5.25\ V$, All Inputs Grounded
I_{BV}	Power Supply Current at $V_{CC} = 7\ V$		95	mA	$V_{CC} = 7.0\ V$, All Inputs Grounded
I_{CEX}	Output Leakage Current		250	μA	$V_{CC} = 5.25\ V$, $V_{CEX} = 5.5\ V$, all inputs grounded
V_{OL}	Output Low Voltage		0.45	V	$V_{CC} = 4.75\ V$, One bit selected $I_{OL} = 20\ mA$ (A6A9033592 - A3F9033592) $I_{OL} = 40\ mA$ (A6A9033591 - A3F9033591)
$V_{XY(W)}$	Address Input Threshold to Prevent Writing		0.8	V*	$V_{CC} = 5.0\ V$, other X and Y grounded. Alternately pulse W_0 and W_1, cell must not change state.
$V_{XY(W)}$	Address Input Threshold to insure Writing	2.0		V*	$V_{CC} = 5.0\ V$, other X and Y grounded. Alternately pulse W_0 and W_1, cell state must alternate.
$V_{XY(R)}$	Address Input Threshold to Prevent Reading		1.0	V	$V_{CC} = 5.0\ V$, other inputs grounded. Both outputs must be on "high" state.
$V_{XY(R)}$	Address Input Threshold to Insure Reading	2.0		V*	$V_{CC} = 5.0\ V$, other X and Y grounded. Alternately pulse W_0 and W_1, cell state must alternate.
$V_{W(W)}$	Write Input Threshold to Prevent Writing		1.0	V*	$V_{CC} = 5.0\ V$, one X and one Y to 4.5 V, other X and Y grounded. One write input to $V_{W(W)}$, pulse the other write input. If W_0 is pulsed, S_0 will assume low state. If W_1 is pulsed, S_1 will assume low state.
$V_{W(W)}$	Write Input Threshold to Insure Writing	2.0		V*	$V_{CC} = 5.0\ V$, one X and one Y to 4.5 V, other X and Y grounded. One write input to $V_{W(W)}$, pulse the other write input. If W_0 is pulsed, S_1 will assume low state. If W_1 is pulsed, S_0 will assume low state.

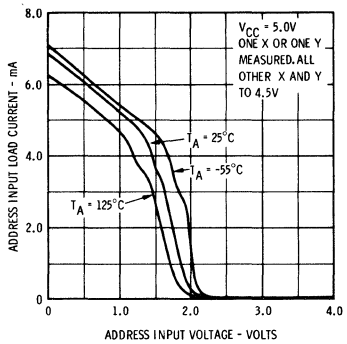
* Amplitude of the pulse ≥2.5 V, pulse width ≥100 ns. The cell state is determined 35 ns after pulse disappears.

SWITCHING CHARACTERISTICS

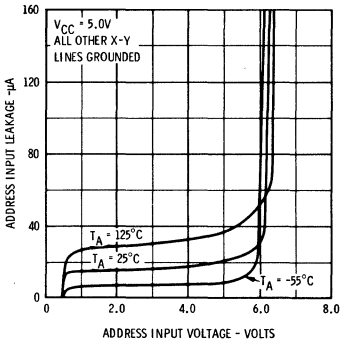
SYMBOL	CHARACTERISTICS	9033511 −55°C to 125°C MIN.	9033511 MAX.	9033591 0°C to 75°C MIN.	9033591 MAX.	9033592 0°C to 75°C MIN.	9033592 MAX.	UNITS	CONDITIONS LOAD (mA)	CONDITIONS C_L (pF)	CONDITIONS INPUT
t_{WP}	Write Pulse Width	25		25				ns	20		$V_{CC} = 5.0\ V$, One X-Y Location Selected
						25			40		
t_{WR}	Write Recovery Time		40		35			ns	20	30	
							35		40	30	
t_{on}	Turn On Delay		25		20			ns	20	30	$V_{CC} = 5.0\ V$, One X-Y Location Switched
			35		30				20	100	
						20			40	30	
						30			40	200	
t_{off}	Turn Off Read Delay		25		20			ns	20	30	
			35		30				20	100	
						20			40	30	
						30			40	200	

TYPICAL ELECTRICAL CHARACTERISTICS

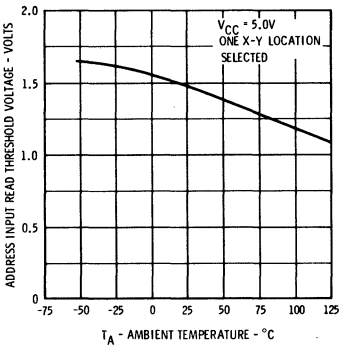
ADDRESS INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



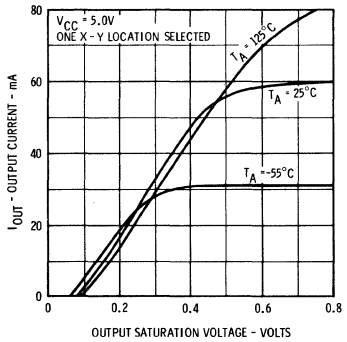
ADDRESS INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE



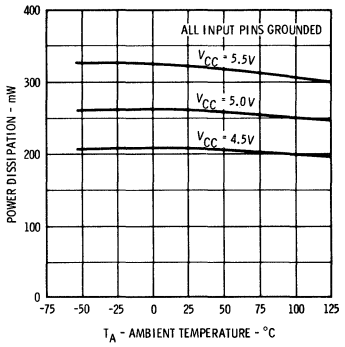
ADDRESS INPUT READ THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE



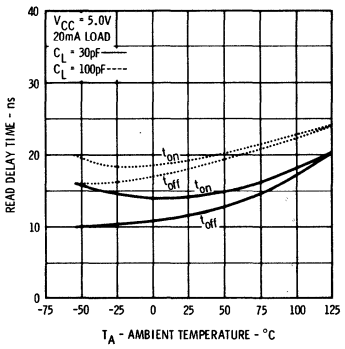
OUTPUT CURRENT VERSUS OUTPUT SATURATION VOLTAGE



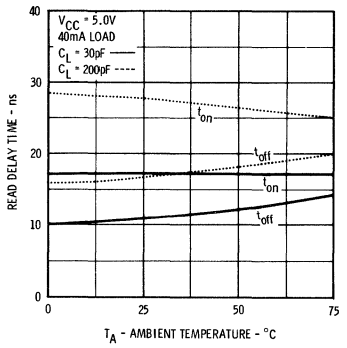
POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



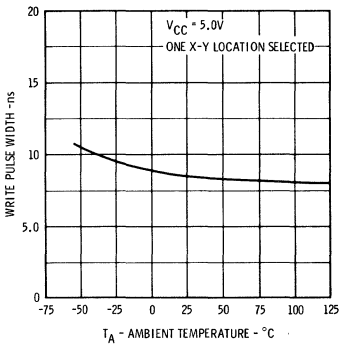
READ DELAY VERSUS AMBIENT TEMPERATURE 20 mA LOAD



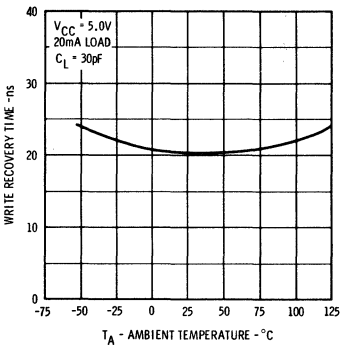
READ DELAY VERSUS AMBIENT TEMPERATURE 40 mA LOAD

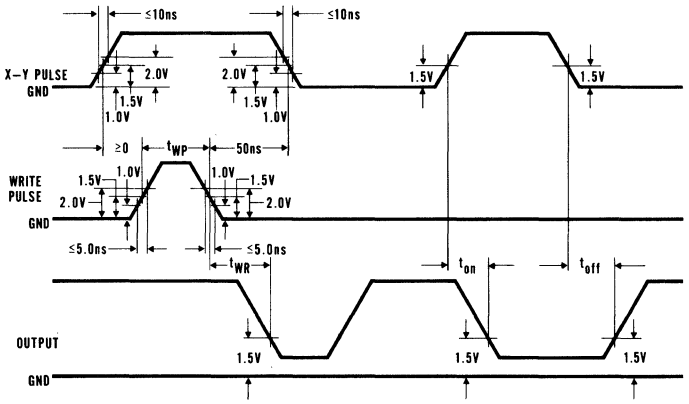


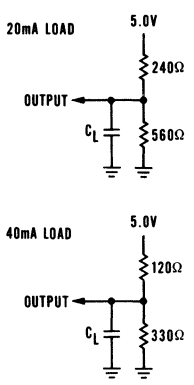
WRITE PULSE WIDTH VERSUS AMBIENT TEMPERATURE



WRITE RECOVERY TIME VERSUS AMBIENT TEMPERATURE







APPLICATION:

A memory utilizing 9033 memory cells may have any desired word length. The number of words in the memory is a multiple of four words. The following example of a 64 word memory illustrates how a number of 16 bit memory cells 9033 may be used to construct a typical memory.

The 64 word memory as shown in Figure A consists of groups of four 9033 memory cells. Each of the groups of four 9033 memory cells supplies one bit for each of the 64 words stored in the memory. All bits belonging to one word are stored in the same address location. Therefore, the address of a word in the memory is the address of each of the bits of the addressed word in the groups of four 9033 memory cells. The equal outputs of the four memory cells are tied together so that each group of four memory cells has one high and one low level output.

The six memory address lines from an external source are decoded at the first level with two 9301 decoders. The fourth input to each of the two decoders can be used as an enable control input to the 64 word memory. If the address enable is at a low logic level, one and only one of the eight outputs, 0 to 7, in the illustration assumes a low logic level. If the address enable is at a high logic level, the outputs 0 to 7 of the two decoders assume a high logic level, thus none of the 64 words stored in the memory is addressed. The outputs, 0 to 7, of the two decoders serve as X-and-Y address lines. The output signals of the decoders are connected to driving transistors which provide the necessary current to address the memory cells.

The example given above is only one of the many organizations and is presented as an illustration. Obviously many address decoding schemes may be utilized depending on memory size, driver fan-out, decoder fan-out, wiring, heat dissipation, etc.

Figures B through D show alternative schemes to enter data into the memory cell.

LOGIC DIAGRAM

Fig. A

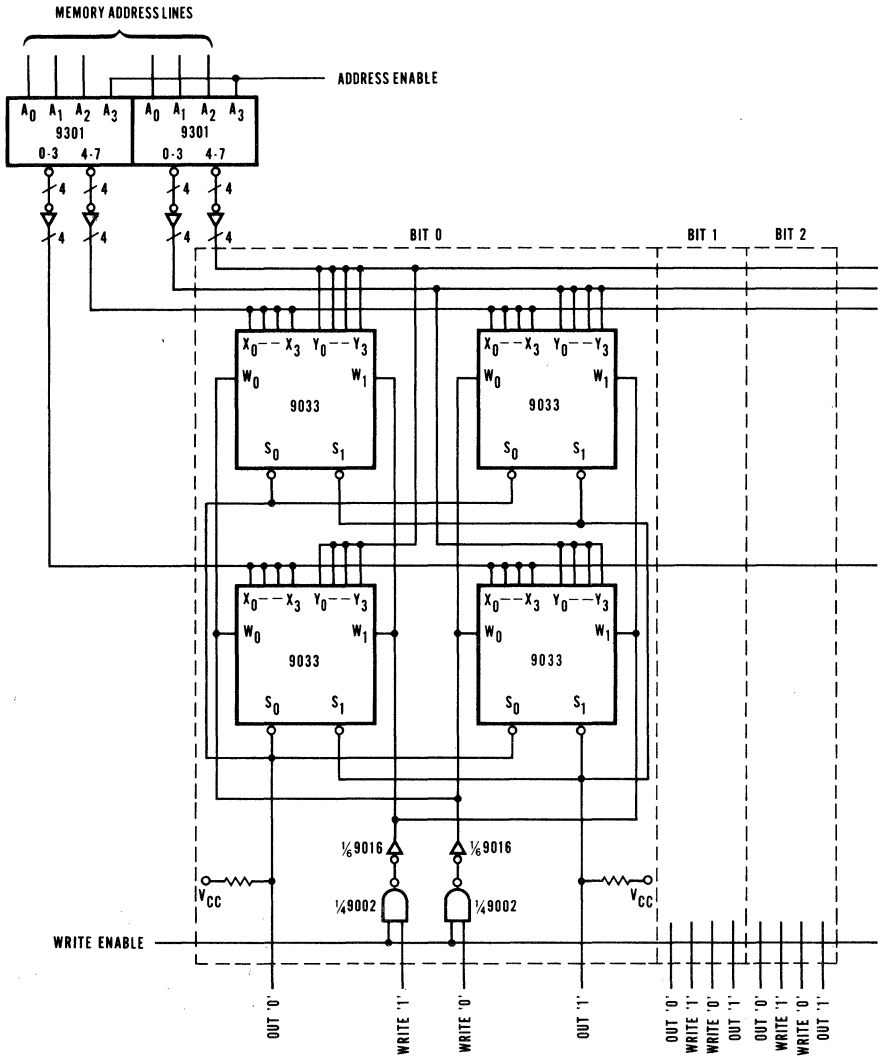


Fig. B
DOUBLE RAIL ACTIVE LOW INPUTS AND ENABLE

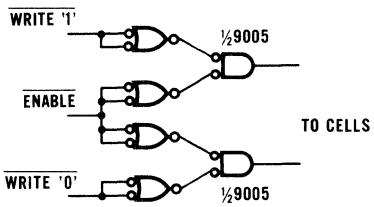


Fig. C
SINGLE RAIL ACTIVE HIGH INPUT AND ENABLE

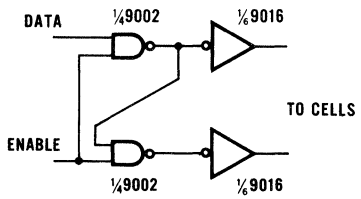
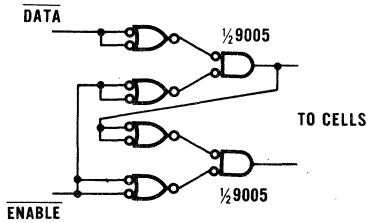


Fig. D
SINGLE RAIL ACTIVE LOW INPUT AND ENABLE



MμL9034

256-BIT READ ONLY MEMORY

MEMORY MICROLOGIC® INTEGRATED CIRCUITS

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

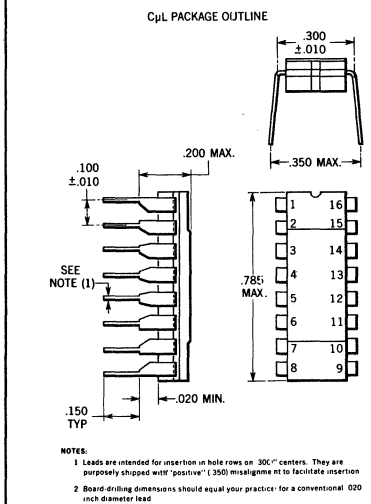
GENERAL DESCRIPTION — The Fairchild MμL9034 is a 256-bit bipolar transistor read only memory. The memory is organized as 32 words of 8-bits each. The words are selected through 5 address lines. The 8 outputs of the words are uncommitted collectors which may be wired-or'd with the outputs of other ROM's. An Enable input is provided for additional decoding flexibility. A low Enable forces all outputs to be high.

The contents of the memory are permanently programmed on customer request.

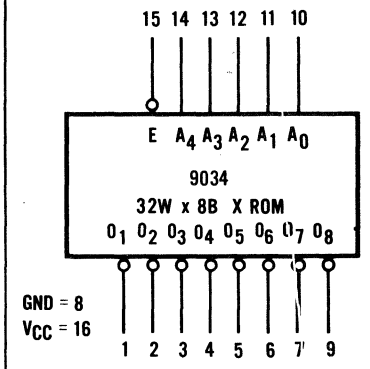
FEATURES:

- **CCSL COMPATIBLE**
- **OUTPUT WIRED-OR'D ABLE WITH OTHER OUTPUTS**
- **SINGLE TTL LOAD INPUTS**

PHYSICAL DIMENSIONS



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground	−0.5 V to +8.0 V
Input Pin Voltage	−1.5 V to 5.5 V
Current Into Output Terminal	100 mA
Output Voltages	−0.5 to V_{CC} Value

ORDER INFORMATION

Custom Code — Specify A6B9034XXX where X1X is for −55°C to +125°C temperature range or X9X is for 0°C to +75°C temperature range. Remaining X's are to be assigned alphabet letters to customer code.

Standard Code Available — Specify A6B9034A1A or A6B9034A9A for figures 1 thru 6 code. Specify A6B9034A1B or A6B9034A9B for figures 7 thru 0, comma and period code. For additional information on these two codes refer to individual data sheets.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	TEST	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	TEST CONDITIONS
I_{FA}	Address Input Load Current		1.6		1.6		1.6	mA	$V_{CC} = 5.5\ V$ $V_A = 0$
I_{FI}	Enable Input Load Current		1.6		1.6		1.6	mA	$V_{CC} = 5.5\ V$ $V_E = 0$
I_{RA}	Address Input Leakage Current		100		100		100	μA	$V_{CC} = 5.5\ V$ $V_A = 4.5\ V$
I_{RI}	Enable Input Leakage Current		100		100		100	μA	$V_{CC} = 5.5\ V$ $V_I = 4.5\ V$
I_{CEX}	Output Leakage Current		100		100		100	μA	$V_{CC} = 5.5\ V$ $V_{CEX} = 5.5\ V$ Enable Input to 2.0 V
V_{OL}	Output Low Voltage		0.45		0.45		0.45	V	$V_{CC} = 4.5\ V$ $I_{OUT} = 10\ mA$ The word containing a "1" bit is selected when performing this test.
V_{IL}	Input Low Voltage		0.8		0.9		0.8	V	$V_{CC} = 5.5\ V$ Enable input grounded. Monitor appropriate output to guarantee this test.
V_{IH}	Input High Voltage	2.1		2.0		2.0		V	$V_{CC} = 4.5\ V$ Enable input grounded. Monitor appropriate output to guarantee this test.

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	TEST	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	TEST CONDITIONS
I_{FA}	Address Input Load Current		1.6		1.6		1.6	mA	$V_{CC} = 5.25\ V$ $V_A = 0$
I_{FI}	Enable Input Load Current		1.6		1.6		1.6	mA	$V_{CC} = 5.25\ V$ $V_E = 0$
I_{RA}	Address Input Leakage Current		100		100		100	μA	$V_{CC} = 5.25\ V$ $V_A = 4.5\ V$
I_{RI}	Enable Input Leakage Current		100		100		100	μA	$V_{CC} = 5.25\ V$ $V_I = 4.5\ V$
I_{CEX}	Output Leakage Current		100		100		100	μA	$V_{CC} = 5.25\ V$ $V_{CEX} = 5.25\ V$ Enable Input to 2.0 V
V_{OL}	Output Low Voltage		0.45		0.45		0.45	V	$V_{CC} = 4.75\ V$ $I_{OUT} = 10\ mA$ The word containing a "1" bit is selected when performing this test.
V_{IL}	Input Low Voltage		0.85		0.9		0.85	V	$V_{CC} = 5.25\ V$ Enable input grounded. Monitor appropriate output to guarantee this test.
V_{IH}	Input High Voltage	2.0		2.0		2.0		V	$V_{CC} = 4.75\ V$ Enable input grounded. Monitor appropriate output to guarantee this test.

SWITCHING CHARACTERISTICS ($T_A = +25°C$, $V_{CC} = 5.0\ V$)

SYMBOL	LIMIT (Max.)	CONDITION NOTE	CONDITION LOAD	C_L
t_{++}	50 ns	1	10 mA	30 pF
t_{--}	50 ns	1	10 mA	30 pF
t_{+-}	50 ns	2	10 mA	30 pF
t_{-+}	50 ns	2	10 mA	30 pF

NOTES:

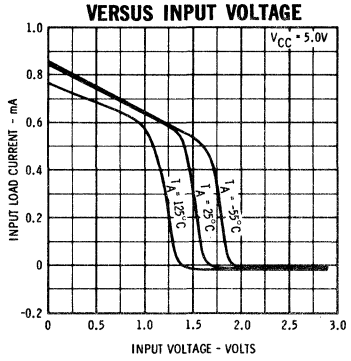
(1) To test enable delay, apply input pulse to enable input. The word selected must contain a "1" in the bit under test.

To test address delay, apply input pulse to the address input under test. The words selected must contain a "1" when input pulse is low and a "0" when input pulse is high in the bit under test.

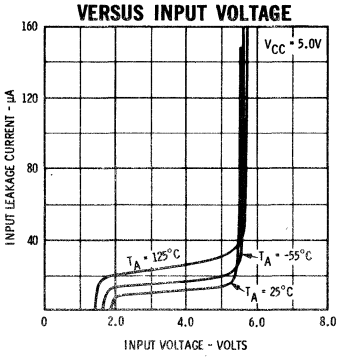
(2) To test address delay, apply input pulse to the address input under test. The words selected must contain a "0" when input pulse is low and a "1" when input pulse is high in the bit under test.

TYPICAL ELECTRICAL CHARACTERISTICS

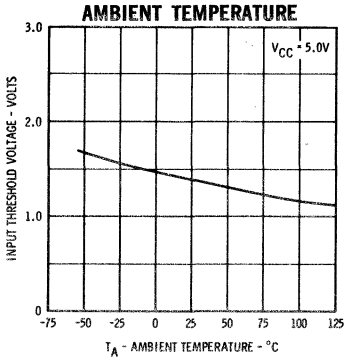
INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



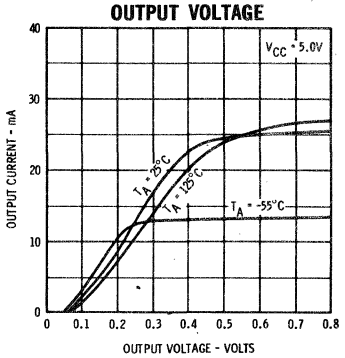
INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE



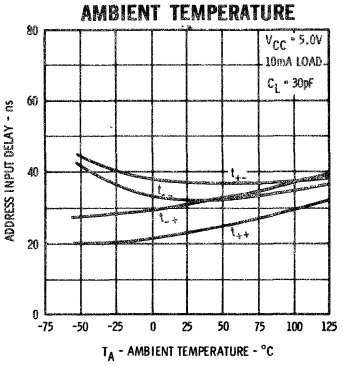
INPUT THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE



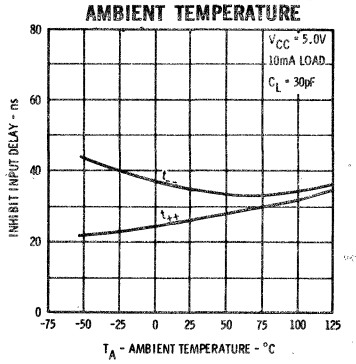
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE



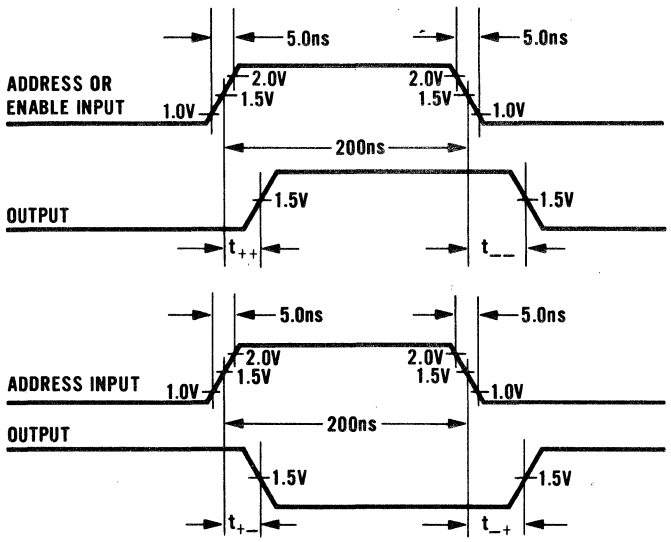
ADDRESS INPUT DELAY VERSUS AMBIENT TEMPERATURE

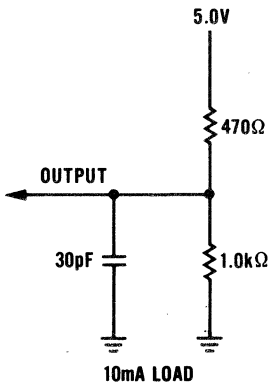


INHIBIT INPUT DELAY VERSUS AMBIENT TEMPERATURE



SWITCHING TIME TEST CONDITIONS AND WAVEFORMS





FAIRCHILD MEMORY MICROLOGIC® INTEGRATED CIRCUIT MμL9034

APPLICATIONS:

The Fairchild MμL9034 Read-Only Memory has many storage and display applications. Two main uses of the memory are for 1) microprogrammed subroutines (core replacements) and 2) character generator display systems.

APPLICATION OF THE 9034 READ-ONLY MEMORY IN DIFFERENT TYPES OF DISPLAY SYSTEMS.

In the application of this ROM as display storage, the enable input is the most important control, since every display system requires a number of ROM's organized in parallel to each other. The effectiveness of such a character storage system depends on the flexibility in addressing a desired character. Most of the character storage systems will be character code oriented.

16 SEGMENT DECODER

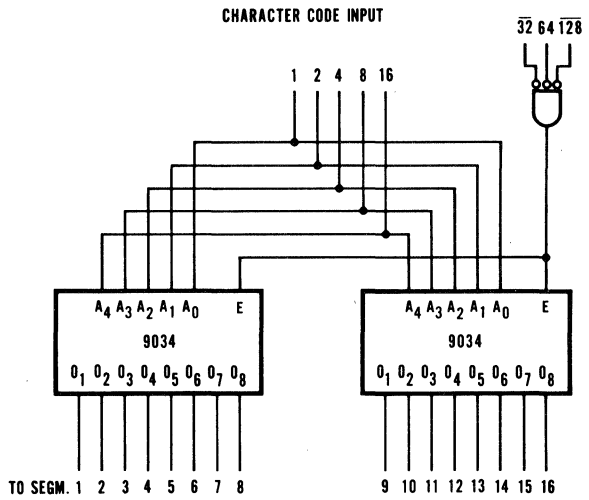
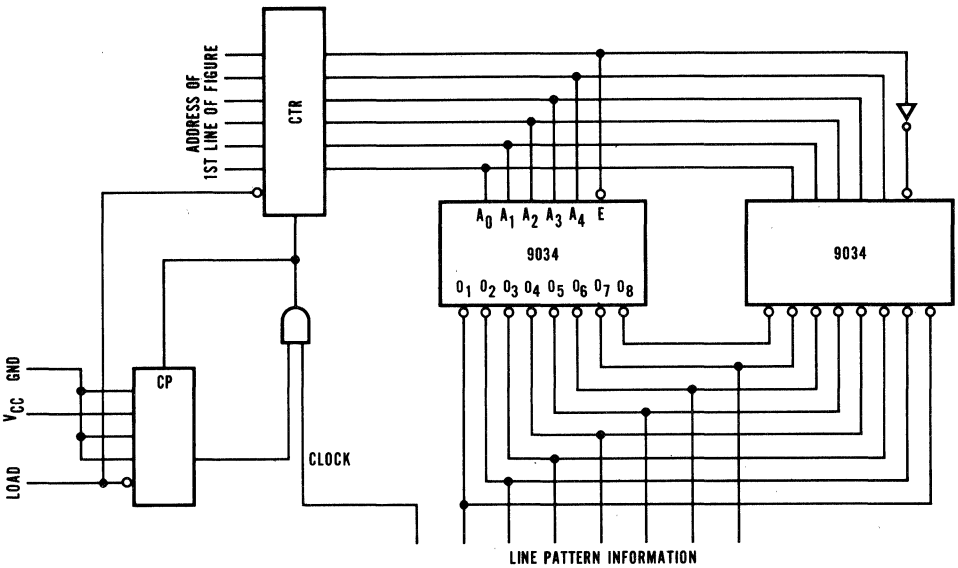


Figure 1a illustrates the use of two 9034 ROM's for driving a 16 segment decoder. The character code is used directly as a control for both ROM's. One additional 3-input gate controlling the enable inputs of the 2 ROM's is required for selecting the group of codes within the ASCII system which refer to the characters. For uninterrupted control, 2 ROM's are required for each of the 16 segment display units.

DISPLAY GENERATOR 5 x 8 DOT MATRIX



The four 8-bit words representing the 5 x 8 dot pattern of a figure are stored in sequence. The external source which calls for a figure has to supply the address of the first 8-bit word of this figure. The clock will increment this address by one each time the generated pattern has been displayed until all five 8-bit patterns have been used. The mod. 5 counter calls for the first line address of the next figure automatically.

If these data are used to control a CRT display the outputs of the 2 9034 ROM's may be connected to an 8-channel multiplexer (3705) which serves as an interface to the Z modulation input of the display unit. The 8 channels are selected in sequence by a mod. 8 counter of which the eight output generates the control pulses for the mod. 5 and the address counter.

MμL9034AXA

256-BIT READ-ONLY MEMORY

MEMORY MICROLOGIC® INTEGRATED CIRCUITS

GENERAL DESCRIPTION

The 9034 Read-Only Memory code AXA (9034AXA) is programmed to store information for generating Figures 1 thru 6 on a 5 by 8 dot pattern display. The memory stores the information by using 5 consecutive words of 8 bits for each figure or symbol.

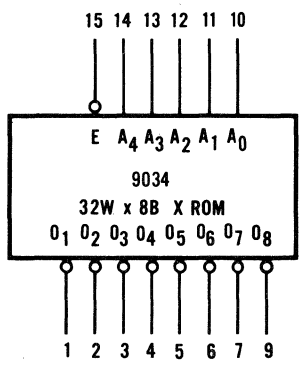
OPERATION AND ELECTRICAL CHARACTERISTICS

Refer to 9034 Data Sheet

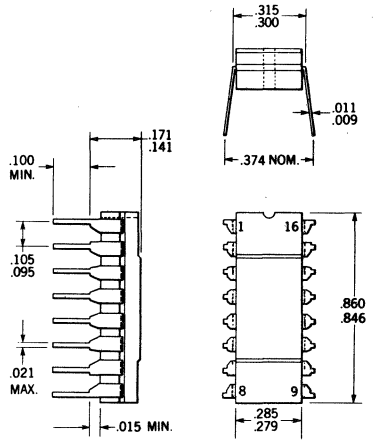
ORDER INFORMATION

Specify A6B9034AXA where A1A is for −55°C to +125°C temperature range or A9A for the 0°C to +75°C temperature range.

LOGIC SYMBOL



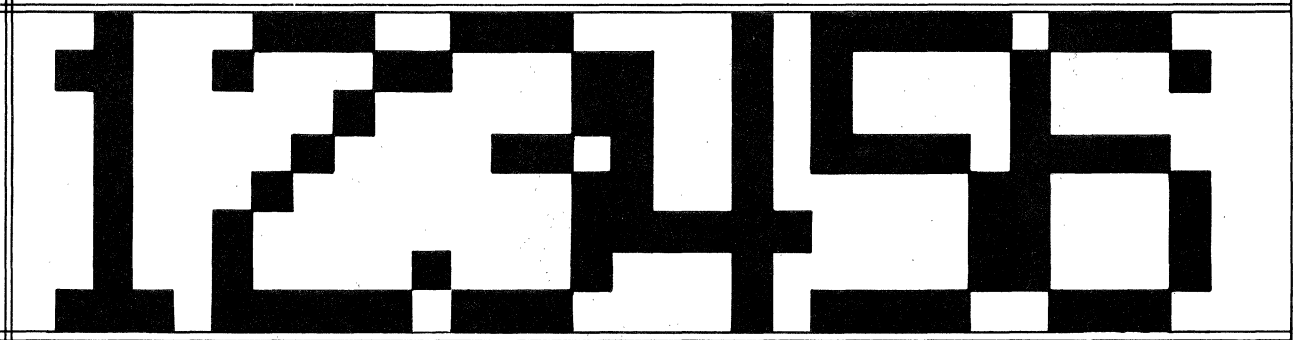
PHYSICAL DIMENSIONS



9034AXA TRUTH TABLE

OUTPUTS	O_1	H	H	L	H	H	H	L	L	L	H	H	L	L	L	H	H	H	H	L	H	L	L	L	L	L	H	L	L	L	H	H	H
	O_2	H	L	L	H	H	L	H	H	H	L	L	H	H	H	L	L	H	H	L	H	L	H	H	H	H	L	H	H	H	L	H	H
	O_3	H	H	L	H	H	H	H	H	L	H	H	H	H	H	L	L	H	H	L	H	L	H	H	H	H	L	H	H	H	H	H	H
	O_4	H	H	L	H	H	H	H	L	H	H	H	H	L	L	H	L	H	H	L	H	L	L	L	L	H	L	L	L	L	H	H	H
	O_5	H	H	L	H	H	H	L	H	H	H	H	H	H	H	L	L	H	H	L	H	H	H	H	H	L	L	H	H	H	L	H	H
	O_6	H	H	L	H	H	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L	H	H	H	H	L	L	H	H	H	L	H	H
	O_7	H	H	L	H	H	L	H	H	H	H	L	H	H	H	L	H	H	H	L	H	H	H	H	H	L	L	H	H	H	L	H	H
	O_8	H	L	L	L	H	L	L	L	L	L	H	L	L	L	H	H	H	H	L	H	L	L	L	L	H	H	L	L	L	H	H	H
INPUTS	A_0	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
	A_1	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
	A_2	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
	A_3	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
	A_4	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32

OUTPUTS O_1 O_2 O_3 O_4 O_5 O_6 O_7 O_8



L — Low Voltage H — High Voltage

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FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

MμL9034AXB

256-BIT READ-ONLY MEMORY

MEMORY MICROLOGIC® INTEGRATED CIRCUITS

GENERAL DESCRIPTION

The 9034 Read-Only Memory code AXB (9034AXB) is programmed to store information for generating Figures 7 thru 0, a comma and period on a 5 x 8 dot pattern display. The memory stores the information by using 5 consecutive words of 8 bits for each figure or symbol.

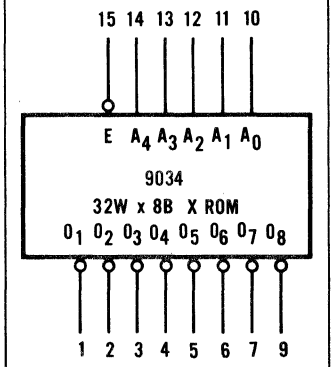
OPERATION AND ELECTRICAL CHARACTERISTICS

Refer to 9034 Data Sheet

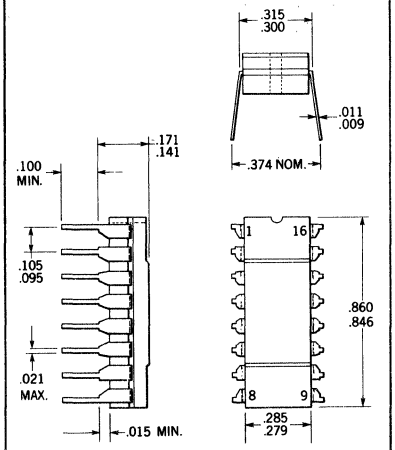
ORDER INFORMATION

Specify A6B9034AXB where A1B is for −55°C to +125°C temperature range or A9A for the 0°C to +75°C temperature range.

LOGIC SYMBOL

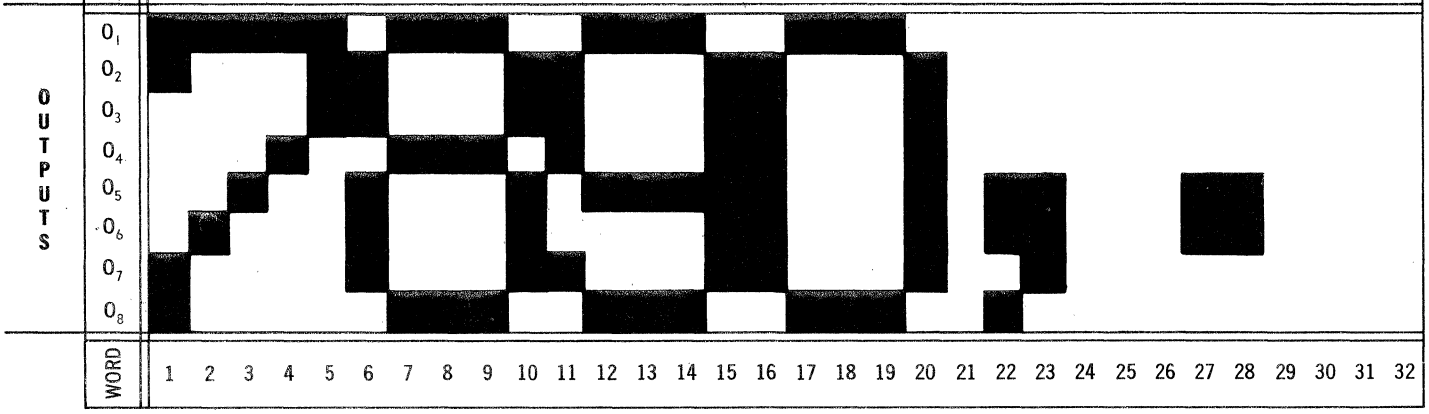


PHYSICAL DIMENSIONS



9034AXB TRUTH TABLE

OUTPUTS	O_1	L	L	L	L	L	H	L	L	L	H	H	L	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H
	O_2	L	H	H	H	L	L	H	H	H	L	L	H	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	O_3	H	H	H	H	L	L	H	H	H	L	L	H	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	O_4	H	H	H	L	H	H	L	L	L	H	L	H	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	O_5	H	H	L	H	H	L	H	H	H	L	H	L	L	L	L	L	H	H	H	L	H	L	L	H	H	H	L	L	H	H	H
	O_6	H	L	H	H	H	L	H	H	H	L	H	H	H	H	L	L	H	H	H	L	H	L	L	H	H	H	L	L	H	H	H
	O_7	L	H	H	H	H	L	H	H	H	L	L	H	H	H	L	L	H	H	H	L	H	H	L	H	H	H	H	H	H	H	H
	O_8	L	H	H	H	H	H	L	L	L	H	H	L	L	L	H	H	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H
INPUTS	A_0	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
	A_1	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
	A_2	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
	A_3	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
	A_4	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32



L — Low Voltage H — High Voltage

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MμL9035

64-BIT READ/WRITE MEMORY CELL

MEMORY MICROLOGIC® INTEGRATED CIRCUITS

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9035 is a high speed 64-bit read/write memory cell designed for use in high speed scratch pad memories. It is organized in a linear select 16 word by 4-bit array. The 9035 is made with TTμL circuitry making it CCSL compatible.

The 9035 is available in the hermetically sealed 36-pin ceramic dual in-line package and will operate over the temperature range from −55°C to +125°C.

OPERATION — In addition to 16 address lines, 4 data outputs, and 4 data inputs, the 9035 has a chip select and a write enable. When the chip select is high, a word may be addressed by a high on the address input. Data is written into the addressed word only when the write enable is held low. While the address is present, the outputs continuously show the contents of the word selected. Readout is non-destructive.

Up to four words may be addressed and read simultaneously with the OR function of the words appearing at the output. Data can be written into two locations simultaneously.

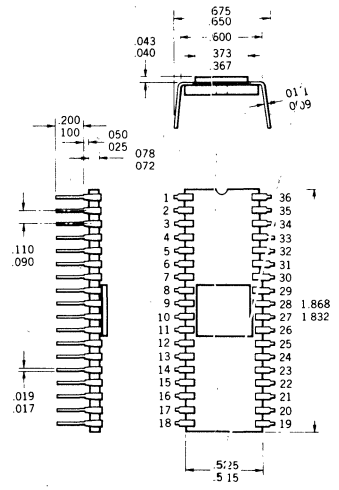
Uncommitted collector outputs are provided on the 9035 to allow maximum flexibility in output connection. In many applications such as word expansion, the outputs of many 9035's are wire-OR'd together. In other applications the wire-OR is not used. In either case an external pullup resistor of value R must be used to provide a high at the output when it is off. Any value of R within the range specified below may be used.

$$\frac{5.1}{10 - \text{F.O. } (1.6)} \leq R \leq \frac{2.1}{N(0.1) + \text{F.O. } (0.06)}$$

R is in KΩ
N = number of outputs wire-OR'd
F.O. = number of TTμL loads driven

The minimum value of R is limited by output current sinking ability. The maximum value of R is determined by the output and input leakage current (I_{CEX} and I_R) which must be supplied to hold the output at 2.4 V.

PHYSICAL DIMENSIONS



FEATURES:

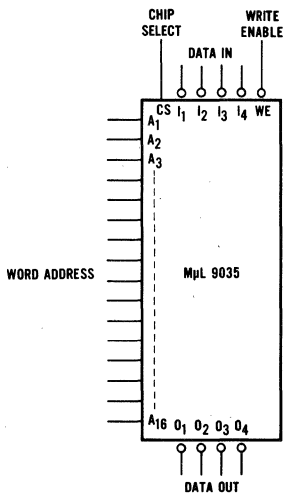
- **35 ns READ ACCESS TIME**
- **CHIP SELECT AND WRITE ENABLES**
- **UNCOMMITTED COLLECTOR OUTPUTS FOR WIRE OR CAPABILITY**
- **LINEAR SELECT**
- **ON CHIP ADDRESS LINE BUFFERING**
- **CCSL COMPATIBLE**

ABSOLUTE MAXIMUM RATINGS

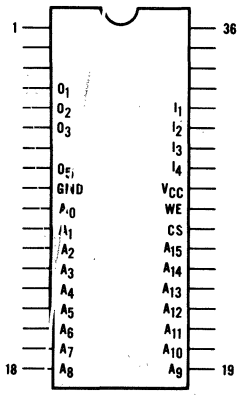
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground	−0.5 V to +8.0 V
Input Pin Voltage	−1.5 V to +5.5 V
Current into Output Terminal	100 mA
Output Voltage	−0.5 V to +8.0 V

ORDER INFORMATION — Specify A6H* 9035XXX where XXX is 51X for the −55°C to +125°C temperature range or 59X for the 0°C to 75°C temperature range.

LOGIC DIAGRAM



PIN CONFIGURATION



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LOADING RULES

	HIGH LEVEL (TTμL Unit Loads)	LOW LEVEL (TTμL Unit Loads)
Address	1.67	1
Chip Select	26.7	1 (see note 1)
Write Enable	1.67	1
Data Input	3.34	2
Data Output	Open Collector	6.2

1 Low Level TTμL Unit Load = 60 μA

1 High Level TTμL Unit Load = −1.6 mA

ELECTRICAL CHARACTERISTICS (T_A = −55°C to 125°C, V_{CC} = 5.0 V ±10%)

		LIMITS							
		−55°C		+25°C		+125°C			
SYMBOL	TEST	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNITS	CONDITIONS
I_{FA}	Address Input Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.5 V, V_A = 0.4 V
I_{FS}	Chip Select Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.5 V, V_{CS} = 0.4 V See Note 1
I_{FW}	Write Enable Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.5 V, V_W = 0.4 V
I_{FD}	Data Input Load Current		−3.2		−3.2		−3.2	mA	V_{CC} = 5.5 V, V_D = 0.4 V
I_{RA}	Address Input Leakage Current		100		100		100	μA	V_{CC} = 5.5 V, V_A = 4.5 V
I_{RS}	Chip Select Input Leakage Current		1.6		1.6		1.6	mA	V_{CC} = 5.5 V, V_{CS} = 4.5 V
I_{RW}	Write Enable Leakage Current		100		100		100	μA	V_{CC} = 5.5 V, V_W = 4.5 V
I_{RD}	Data Input Leakage Current		200		200		200	μA	V_{CC} = 5.5 V, V_D = 4.5 V
I_{CEX}	Output Leakage Current		200		200		200	μA	V_{CC} = 5.5 V, V_{CEX} = 5.5 V Enable Input Grounded
V_{OL}	Output "Low" Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 10 mA One Word Selected
V_{IL}	Input "Low" Voltage		0.8		0.8		0.8	V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
V_{IH}	Input "High" Voltage	2.1		2.0		2.0		V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
I_{PD}	Supply Current		118		118		118	mA	V_{CC} = 5.5 V, One Word Selected

NOTE 1: I_{FE} increases by 1.6 mA for each address enable held at a logical 1.

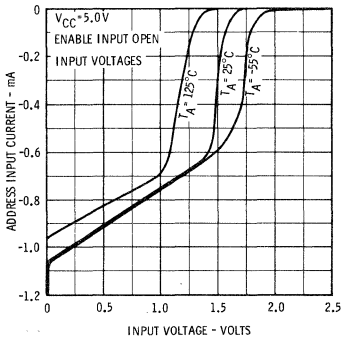
ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 5.0 V ±5%)

		LIMITS							
		0°C		+25°C		+75°C			
SYMBOL	TEST	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNITS	CONDITIONS
I_{FA}	Address Input Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.25 V, V_A = 0.45 V
I_{FS}	Chip Select Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.25 V, V_{CS} = 0.45 V See Note 1
I_{FW}	Write Enable Load Current		−1.6		−1.6		−1.6	mA	V_{CC} = 5.25 V, V_W = 0.45 V
I_{FD}	Data Input Load Current		−3.2		−3.2		−3.2	mA	V_{CC} = 5.25 V, V_D = 0.45 V
I_{RA}	Address Input Leakage Current		100		100		100	μA	V_{CC} = 5.25 V, V_A = 4.5 V
I_{RE}	Chip Select Leakage Current		1.6		1.6		1.6	mA	V_{CC} = 5.25 V, V_{CS} = 4.5 V
I_{RW}	Write Enable Leakage Current		100		100		100	μA	V_{CC} = 5.25 V, V_W = 4.5 V
I_{RD}	Data Input Leakage Current		200		200		200	μA	V_{CC} = 5.25 V, V_D = 4.5 V
I_{CEX}	Output Leakage Current		200		200		200	μA	V_{CC} = 5.25 V, V_{CEX} = 5.25 V Enable Input Grounded
V_{OL}	Output "Low" Voltage		0.45		0.45		0.45	V	V_{CC} = 4.75 V, I_{OL} = 10 mA One Word Selected
V_{IL}	Input "Low" Voltage		0.85		0.85		0.85	V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
V_{IH}	Input "High" Voltage	2.0		2.0		2.0		V	V_{CC} = 5.0 V, Monitor Appropriate Output To Guarantee This Test Limit
I_{PD}	Supply Current		124		124		124	mA	V_{CC} = 5.25 V, One Word Selected

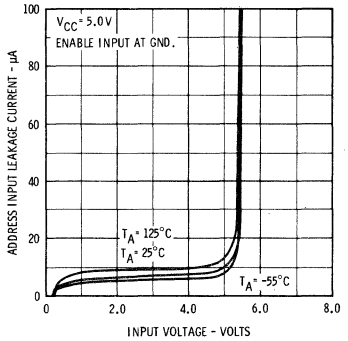
NOTE 1: I_{FE} increases by 1.6 mA for each address enable held at a logical 1.

TYPICAL ELECTRICAL CHARACTERISTICS

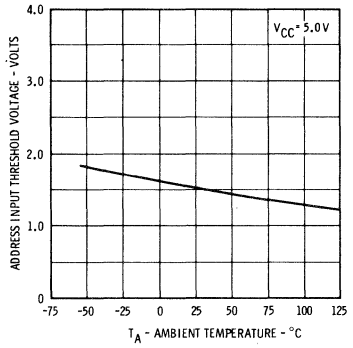
ADDRESS INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



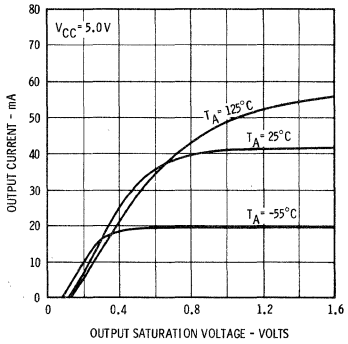
ADDRESS INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE



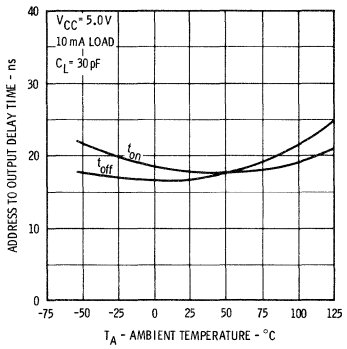
ADDRESS INPUT THRESHOLD VOLTAGE VERSUS TEMPERATURE



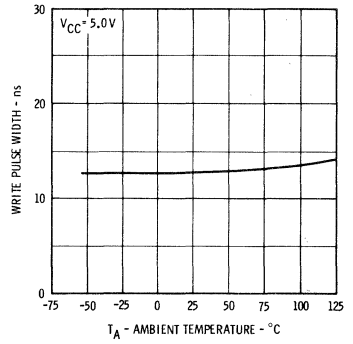
OUTPUT CURRENT VERSUS OUTPUT SATURATION VOLTAGE



ADDRESS TO OUTPUT DELAY TIME VERSUS TEMPERATURE



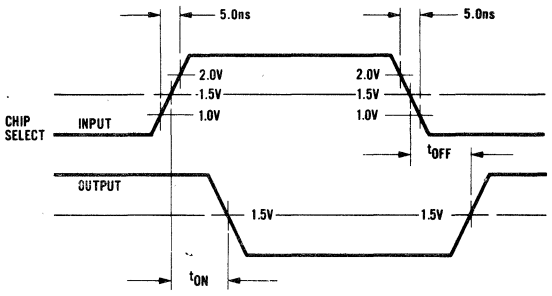
WRITE PULSE WIDTH VERSUS TEMPERATURE

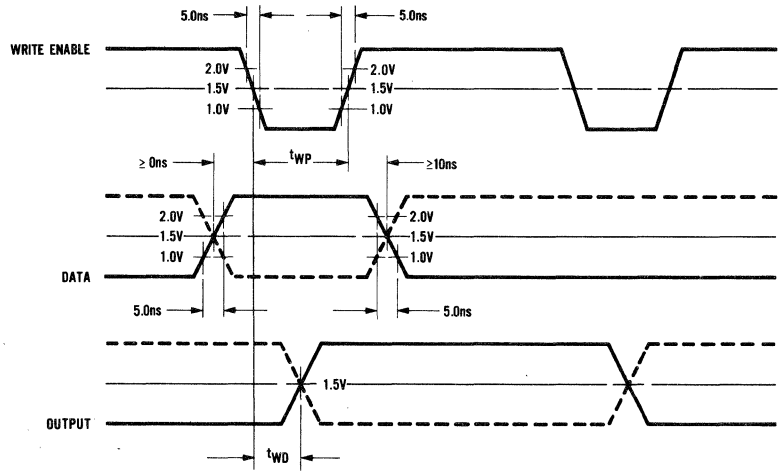


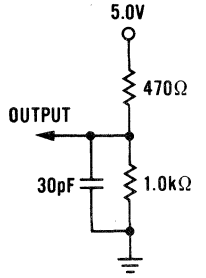
SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

SYMBOL	TEST	LIMIT (ns)			CONDITION		
		MIN.	TYP.	MAX.	LOAD	C	NOTE
t_{on}	Address to Output Turn-On Delay		16	35	10 mA	30 pF	1
t_{off}	Address to Output Turn-Off Delay		18	35	10 mA	30 pF	1
t_{WP}	Write Pulse Width Required to Write	25	15		10 mA	30 pF	2
t_{WD}	Write Delay		30	50	10 mA	30 pF	2

NOTE 1: To test t_{on} and t_{off}, a "Low" must be stored in the cell under test.
NOTE 2: One word is selected during the test.



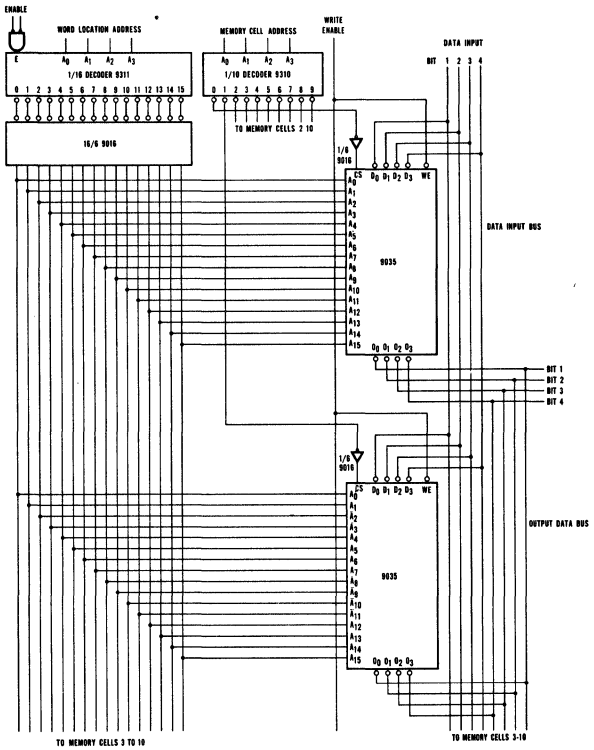




10 mA TEST LOAD

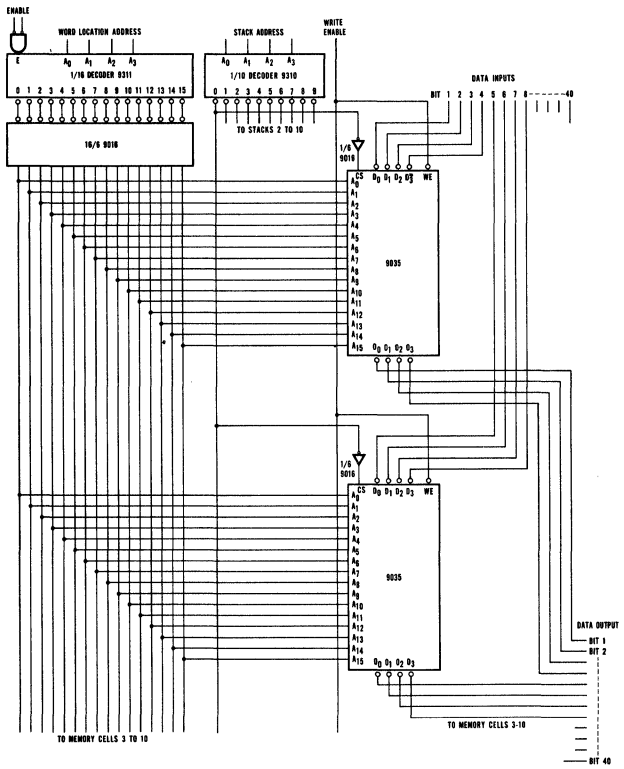
APPLICATIONS

MEMORY EXPANSIONS: N16 WORDS BY 4-BITS



In this application the 9035 memory cells are connected in parallel and two levels of decoding are performed. One of the cells is selected by the 9310 decoder and then a word is addressed by the 9316.

MEMORY STACK 160 WORDS OF 40-BITS



There are 16 words by 40 bits for each stack. The outputs and inputs of all stacks are tied together. Stack 1 contains words 1-16, stack 2, 17-32, and so on through 144-160 for the 10th stack. The stack address decoder tells which word group (1-16 or 17-32, etc.) is addressed while the word location decoder addresses one of the 16 words of the stack addressed. The entire memory has 40 data input lines, 40 data output lines, 8 address lines, and a write enable line.

LPDTμL 9040, 9041 AND 9042

LOW POWER DIODE TRANSISTOR MICROLOGIC®
INTEGRATED CIRCUITS

GENERAL DESCRIPTION

The Fairchild LPDTμL Micrologic® Integrated Circuit Family consists of a set of compatible, integrated logic circuits specifically designed for low power, medium speed applications.

The circuits are fabricated with a silicon monolithic substrate using standard Fairchild Planar* epitaxial processes.

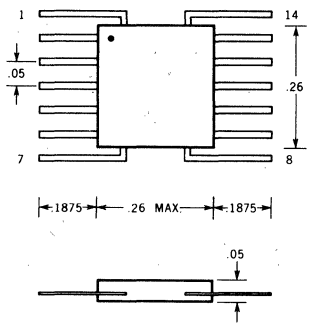
Packaging options include the Flat package and the Dual In-Line package.

Important features of the LPDTμL Micrologic® integrated circuits include the following:

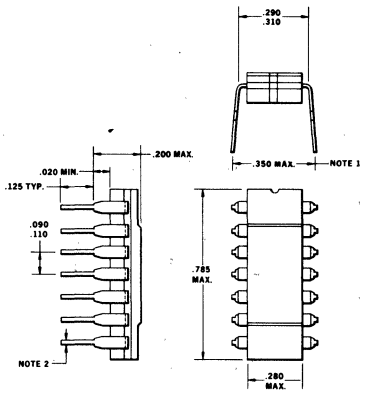
- Reliable operation over the full military temperature range of -55°C to +125°C
- Typical power drains of less than 1 mW per gate (50% duty cycle) for the logic gate elements and less than 4 mW for the clocked flip-flop.
- Single power supply requirement—5 volts optimum, 4.5 to 5.5 volts range.
- Guaranteed fan-out of 10 LPDTμL unit loads or 1 standard Fairchild DTμL unit load, over the full temperature and supply voltage range.
- Guaranteed minimum of 450 mV noise immunity at the temperature extremes.
- Typical logic gate propagation delays of 60 ns and binary clock rate of 2.5 MHz.
- Emitter follower outputs providing good capacitive drive capability.

TYPICAL FLAT PACKAGE

TOP VIEW



TYPICAL DUAL IN-LINE PACKAGE



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

*Planar is a patented Fairchild process.

ORDER INFORMATION

To order Low Power Diode Transistor Micrologic® integrated circuit elements specify U31XXXX51X for flat package and U6AXXXX51X for Dual In-Line package where XXXX is 9040, 9041 or 9042.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

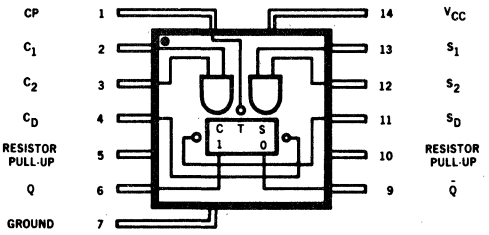
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

LPDTμL 9040 CLOCKED FLIP-FLOP

DESCRIPTION

The LPDTμL 9040 element is a directly coupled, dual-rank flip-flop suitable for use in counters, shift registers and other storage applications. Either R-S or J-K mode operation is possible. Direct set and clear inputs are provided which override all other data inputs.

LOGIC DIAGRAM SHOWING FLAT OR DUAL-IN LINE PACKAGE PIN ASSIGNMENT



SYNCHRONOUS ENTRY TRUTH TABLES

R-S MODE OPERATION

INPUTS @t_n				OUTPUTS @t_{n+1}	
S_1	S_2	C_1	C_2	Q	$\bar{Q}$
13	12	2	3	6	9
L	X	L	X	NC	NC
L	X	X	L	NC	NC
X	L	L	X	NC	NC
X	L	X	L	NC	NC
L	X	H	H	L	H
X	L	H	H	L	H
H	H	L	X	H	L
H	H	X	L	H	L
H	H	H	H	AMBIGUOUS	

J-K MODE OPERATION

INPUTS @t_n		OUTPUTS @t_{n+1}	
S_1	C_1	Q	$\bar{Q}$
13	2	6	9
L	L	NC	NC
L	H	L	H
H	L	H	L
H	H	TOGGLES	

ASYCHRONOUS ENTRY TRUTH TABLE

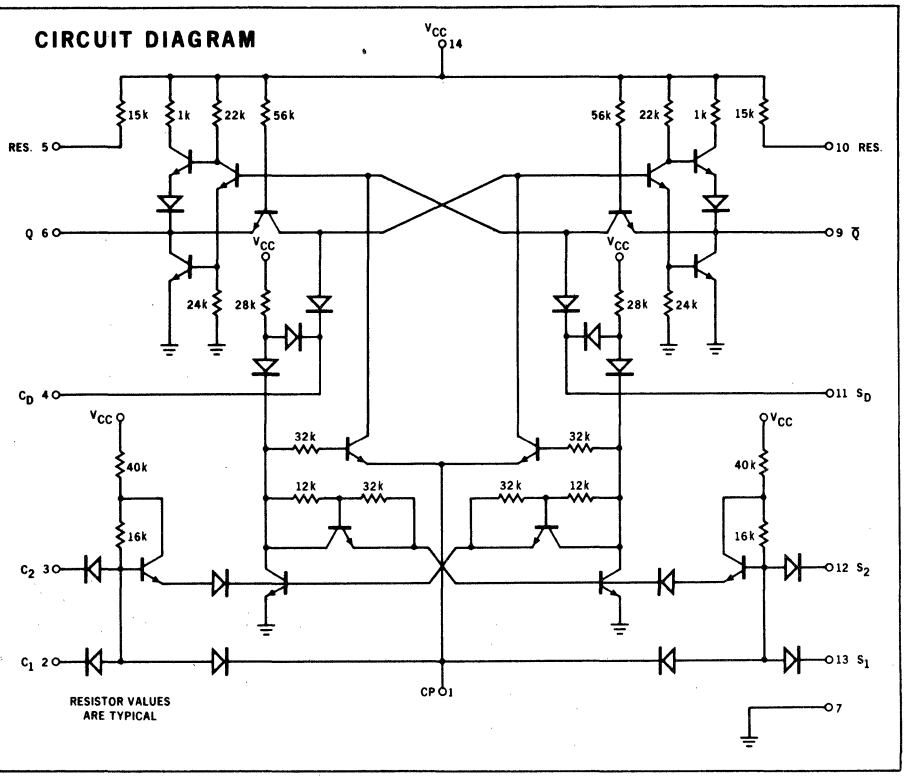
INPUTS		OUTPUTS	
S_D	C_D	Q	$\bar{Q}$
11	4	6	9
H	H	NC	NC
H	L	L	H
L	H	H	L
L	L	H	H

Symbols

H - Most positive logic level
L - Most negative logic level
X - Either H or L can be present
NC - No change in state

NOTES:
1. For J-K mode operation connect Pin 6 to Pin 3 and Pin 9 to Pin 12.
2. Asynchronous entries override all synchronous entries.

CIRCUIT DIAGRAM



LOADING RULES

INPUT	*NORMALIZED UNIT LOADS (U.L.)
S_1 S_2 / C_1 C_2	0.75 U.L.
S_D C_D	2.5 U.L.
CP	2.5 U.L.
OUTPUT	**FAN-OUT**
Q, $\bar{Q}$	10 U.L. 7 U.L. WITH RESISTOR PULL-UP CONNECTED

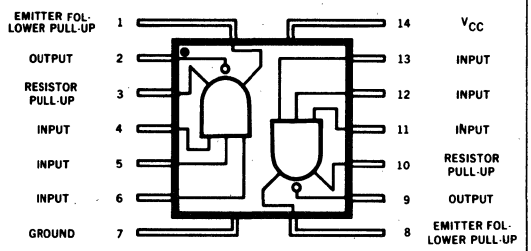
*1UNIT LOAD EQUALS 1-LPDTμL 9041 OR 9042 INPUT LOAD

LPDTμL 9041 — DUAL 3 INPUT NAND GATE

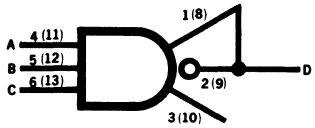
DESCRIPTION

The LPDTμL 9041 element consists of two, 3-input positive logic NAND gates suitable for general logic gate and inverter applications. The unique feature of this gate is that the output transistor collector and the emitter follower pull-up are not internally connected. This allows the user to tie collectors to a common node for the wired "OR" logic function.

LOGIC DIAGRAM SHOWING FLAT OR DUAL-IN-LINE PACKAGE PIN ASSIGNMENT



POSITIVE LOGIC NAND GATE

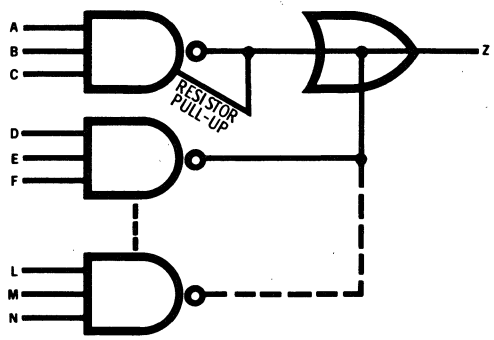


$\overline{ABC} = D$

EACH INPUT = 1 UNIT LOAD
OUTPUT FAN-OUT = 10 UNIT LOADS
= 7 U.L. WITH RESISTOR PULL-UP CONNECTED

EITHER THE EMITTER FOLLOWER OR RESISTOR PULL-UP MUST BE CONNECTED TO THE OUTPUT TO ESTABLISH THE HIGH LEVEL.

WIRED 'OR' APPLICATION

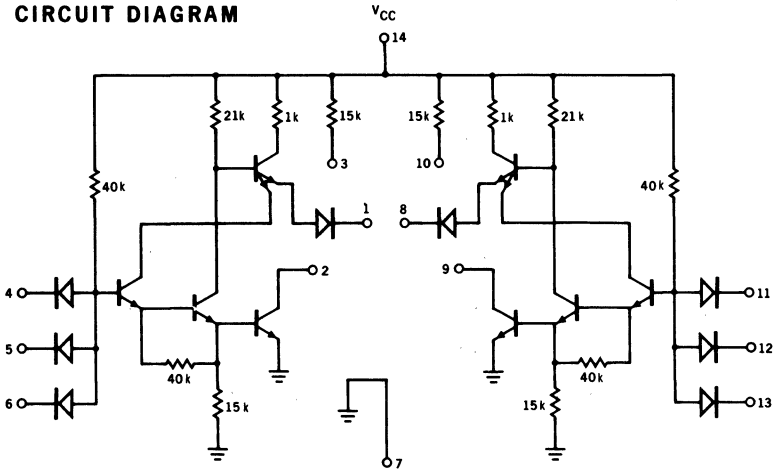


$\overline{ABC + DEF + \cdots + LMN} = Z$

OUTPUT FAN-OUT = 10 - 3 (NO. OF RESISTOR PULL-UPS)

ONE PULL-UP RESISTOR IS REQUIRED FOR EVERY 8 GATES CONNECTED TO THE COMMON "OR" NODE.

CIRCUIT DIAGRAM



RESISTOR VALUES ARE TYPICAL

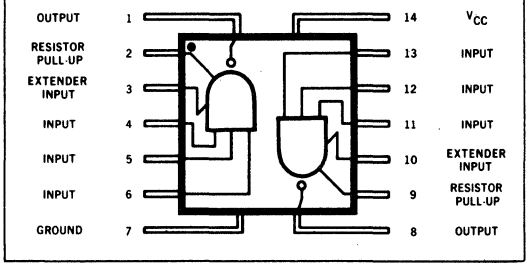
LPDTμL 9042 — DUAL 3 INPUT NAND GATE WITH EXTENDER INPUTS

DESCRIPTION

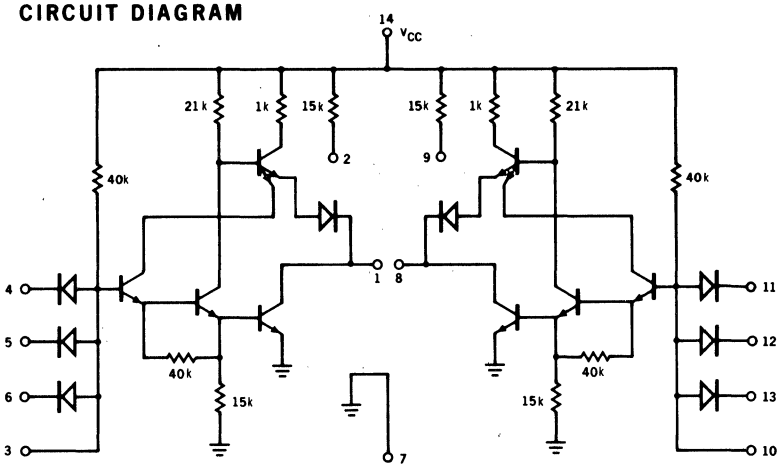
The LPDTμL 9042 element consists of two 3-input positive logic NAND gates with extender inputs. This element in the family allows the user to implement logic applications requiring a gate fan-in exceeding three.

The DTμL 9933 4-input extender element or equivalent—may be used to provide additional diode inputs. Any capacitance added to the extender input will increase the turn-on delay of the LPDTμL 9042 gate. Typically, the increase is 10 ns/pico-farad. Turn-off delay is not affected.

LOGIC DIAGRAM SHOWING FLAT OR DUAL-IN-LINE PACKAGE PIN ASSIGNMENT

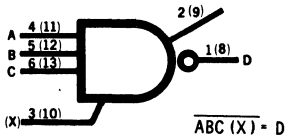


CIRCUIT DIAGRAM



RESISTOR VALUES ARE TYPICAL

POSITIVE LOGIC NAND GATE



$\overline{ABC}$ (X) = D

EACH INPUT = 1 UNIT LOAD

OUTPUT FAN-OUT = 10 UNIT LOADS

= 7 UNIT LOADS WITH RESISTOR PULL-UP CONNECTED

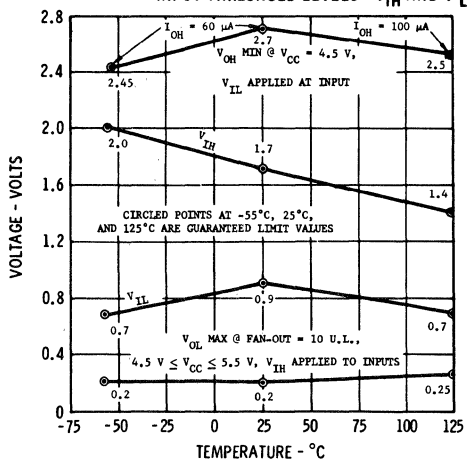
BUFFER ELEMENT

For applications requiring a fan-out exceeding ten, the Fairchild DTμL 9930 Dual 4-Input Gate may be used. The DTμL 9930 will drive 44 LPDTμL unit loads, while maintaining the same output logic levels as the low power circuits.

The input of a DTμL 9930 requires the equivalent of 10 LPDTμL unit loads. Therefore, a low power circuit can drive only one DTμL 9930 input.

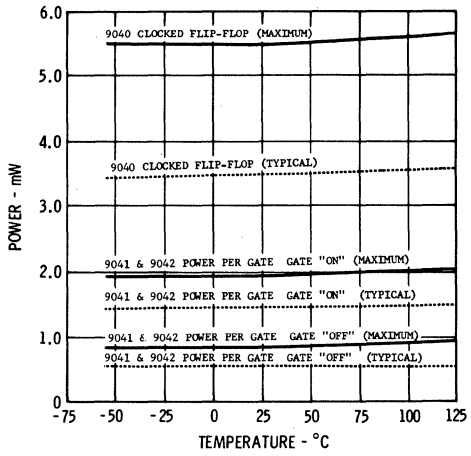
OPERATING VOLTAGE CHARACTERISTICS

WORST CASE OUTPUT LOGIC LEVELS - V_{OH} AND V_{OL}
INPUT THRESHOLD LEVELS - V_{IH} AND V_{IL}

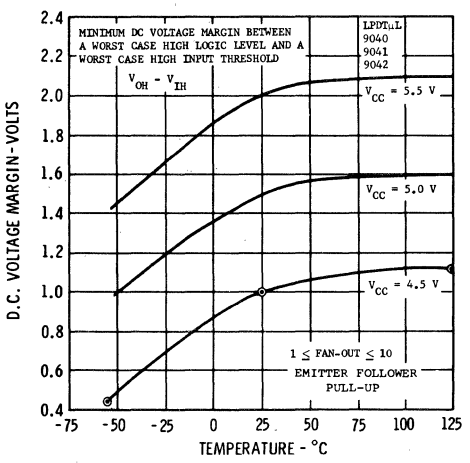


POWER CHARACTERISTICS

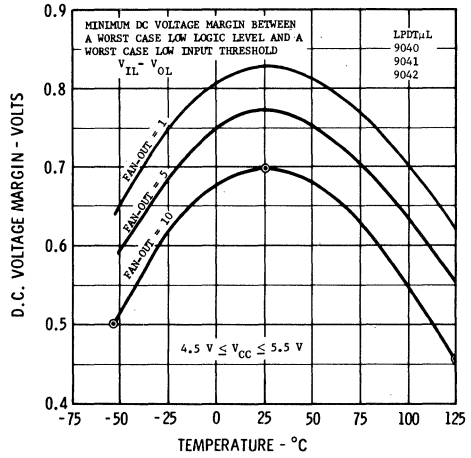
VCC = 5V
EMITTER FOLLOWER PULL-UP



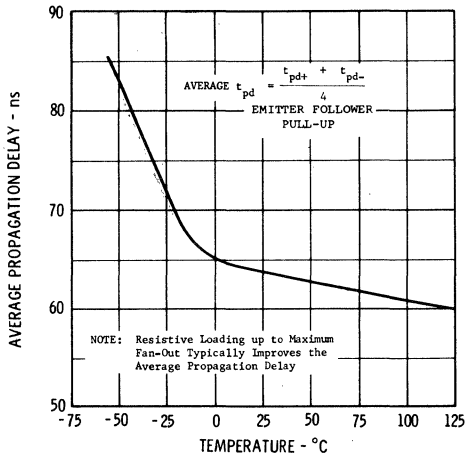
HIGH LEVEL NOISE IMMUNITY



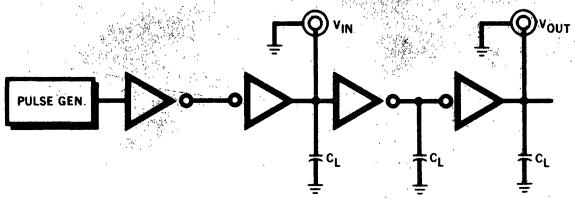
LOW LEVEL NOISE IMMUNITY



TYPICAL AVERAGE PROPAGATION DELAY LPDTμL 9041 • 9042



TEST CIRCUIT

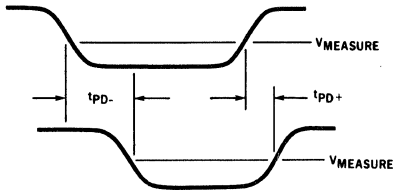


CONDITIONS

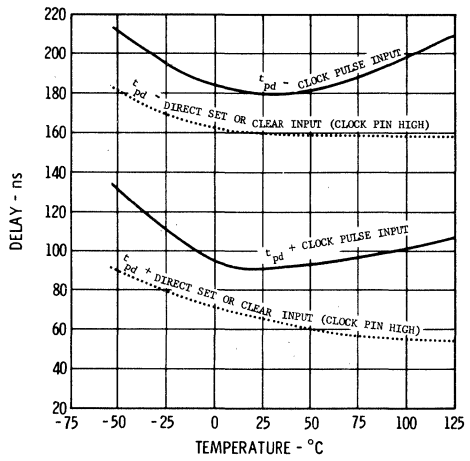
V_{CC} = 5.0V, C_L = 50pf (INCLUDING PROBE AND JIG CAPACITANCE)

$V_{MEASURE}$ = 1.6V @ -55°C
(GND. REF.) 1.3V @ 25°C
0.9V @ 125°C

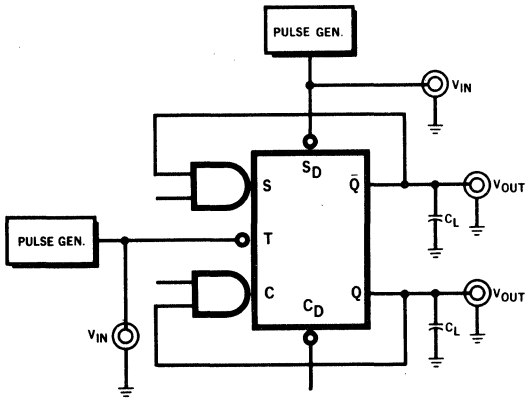
WAVE FORMS



TYPICAL DELAY CHARACTERISTICS LPDTμL 9040



TEST CIRCUIT

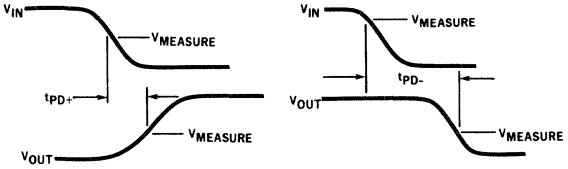


CONDITIONS

V_{CC} = 5.0V, C_L = 50pf (INCLUDING PROBE AND JIG CAPACITY)

$V_{MEASURE}$ = 1.6V @ -55°C
(GND. REF.) 1.3V @ 25°C
0.9V @ 125°C

WAVE FORMS



DTμL 9093 • 9094 • 9097 • 9099

DUAL MONOLITHIC, CLOCKED J-K FLIP-FLOPS DIODE TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

TEMPERATURE RANGE: −55°C to +125°C, −20°C to +100°C, 0°C to +75°C

General Description:

- The 9093 and 9094 devices are Dual Monolithic, internally connected J-K flip-flops of the 9945 and 9948 DTμL type respectively. These devices have separate clocks, separate J and K inputs, separate Direct Set inputs and no Direct Clear input (refer to logic diagram).
- The 9097 and 9099 devices are also Dual Monolithic, internally connected J-K flip-flops of the 9948 and 9945 DTμL type respectively. These devices have separate J and K inputs, separate Direct Set inputs, a common clock input pin and a common Direct Clear input pin (refer to logic diagram).

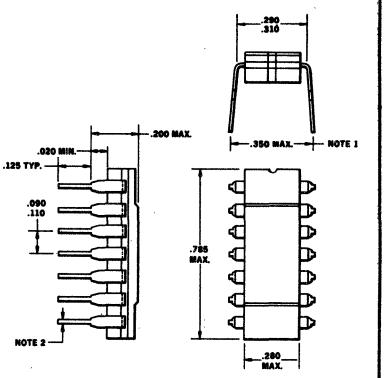
Typical Applications:

- Shift Registers
- Two individually operated flip-flops
- Counters

Features:

- Compatible with all DTμL 930 series
- Compatible with TTμL
- Reduced can count
- Greater logic flexibility

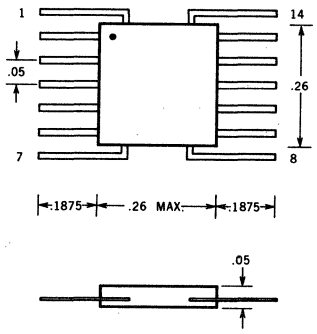
TYPICAL DUAL IN-LINE* PACKAGE



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

TYPICAL FLAT PACKAGE

TOP VIEW



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) Continuous	+8.0 Volts
Supply Voltage (V_{CC}) Pulsed <1.0 second	+12.0 Volts
Internal Power Dissipation 25°C Ambient	500 mW
Typical Power Dissipation 5 V (V_{CC})	100 mW
Operating Temperature Range	−55° to +125°C
Storage Temperature Range	+65°C to +150°C
Lead Temperature (Soldering 60 second)	300°C

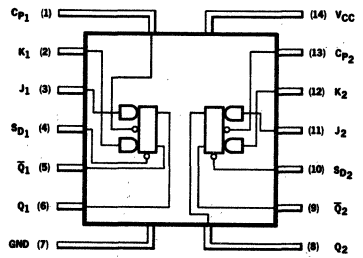
LOADING RULES

• INPUTS	9093/9094	9097/9099
	C_{P1} or C_{P2} = 2	C_P = 4
	K_1 or K_2 = ⅔	K_1 or K_2 = ⅔
	J_1 or J_2 = ⅔	J_1 or J_2 = ⅔
	S_{D1} or S_{D2} = 2	S_{D1} or S_{D2} = 2
		C_D = 4

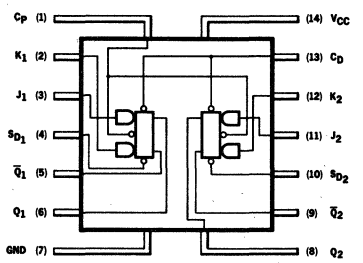
• FANOUT	−55°C to +125°C / −20°C to +100°C	0°C to 75°C
9093 — Q_1, = Q_2, = $\overline{Q_1}$, = $\overline{Q_2}$ =	12	10
9094 — Q_1 = Q_2 = $\overline{Q_1}$ = $\overline{Q_2}$ =	11	9
9097 — Q_1 = Q_2 = $\overline{Q_1}$ = $\overline{Q_2}$ =	11	9
9099 — Q_1 = Q_2 = $\overline{Q_1}$ = $\overline{Q_2}$ =	12	10

PIN CONFIGURATION: Identical for dual-in-line and flat packages.

9093/9094
(DUAL 9945/9948 SEPARATE S_D; SEPARATE Cp)



9097/9099
(DUAL 9948/9945 COMMON Cp; COMMON C_D)



PURCHASING INFORMATION:

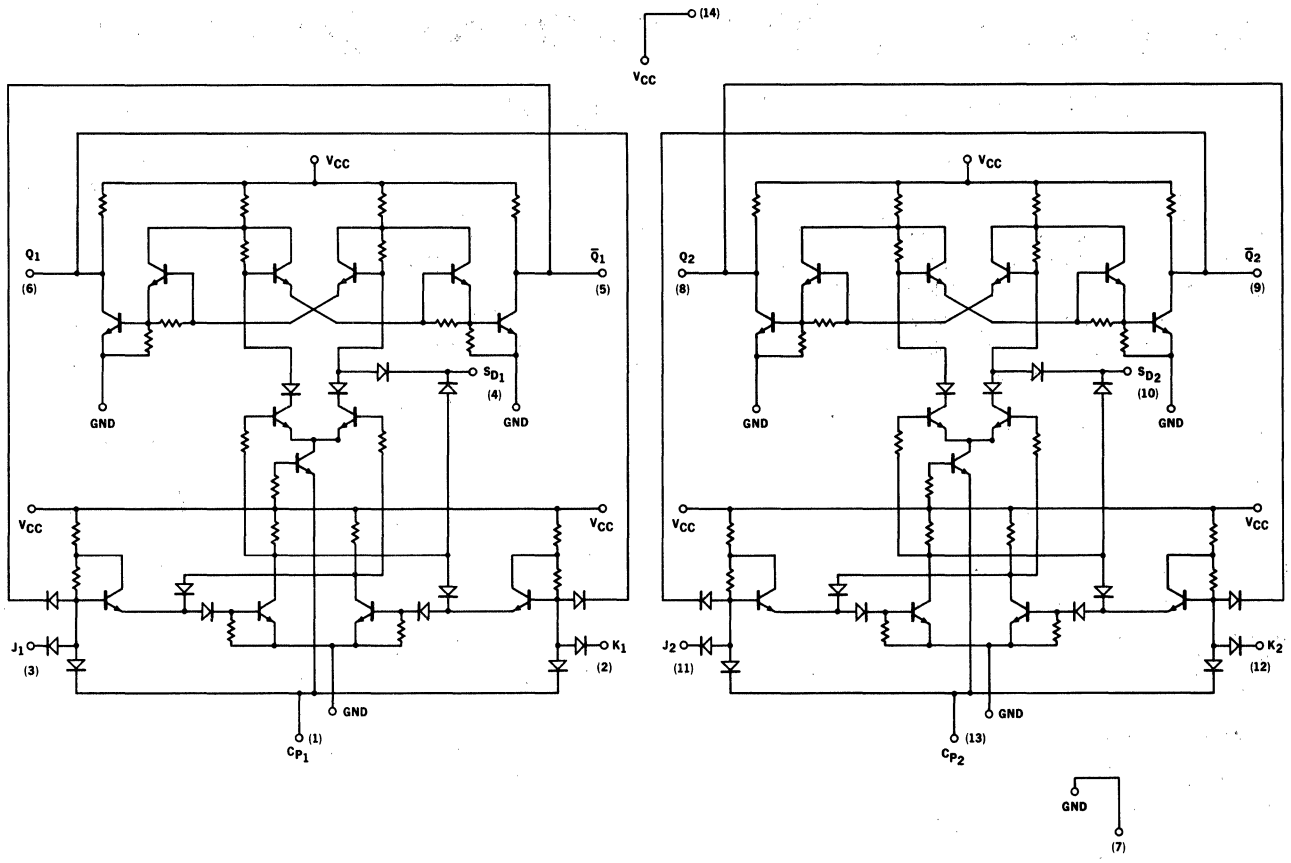
To order Diode Transistor Micrologic Integrated Circuit elements specify U31XXXX5XX for flat package and U6A-XXXX5XX for Dual In-line package, where XXXX is 9093, 9094, 9097, or 9099, and 5X is 51 for the −55°C to +125°C temperature range, 56 for the −20°C to +100°C temperature range or 59 for the 0°C to 75°C temperature range.

* Fairchild patent Pending

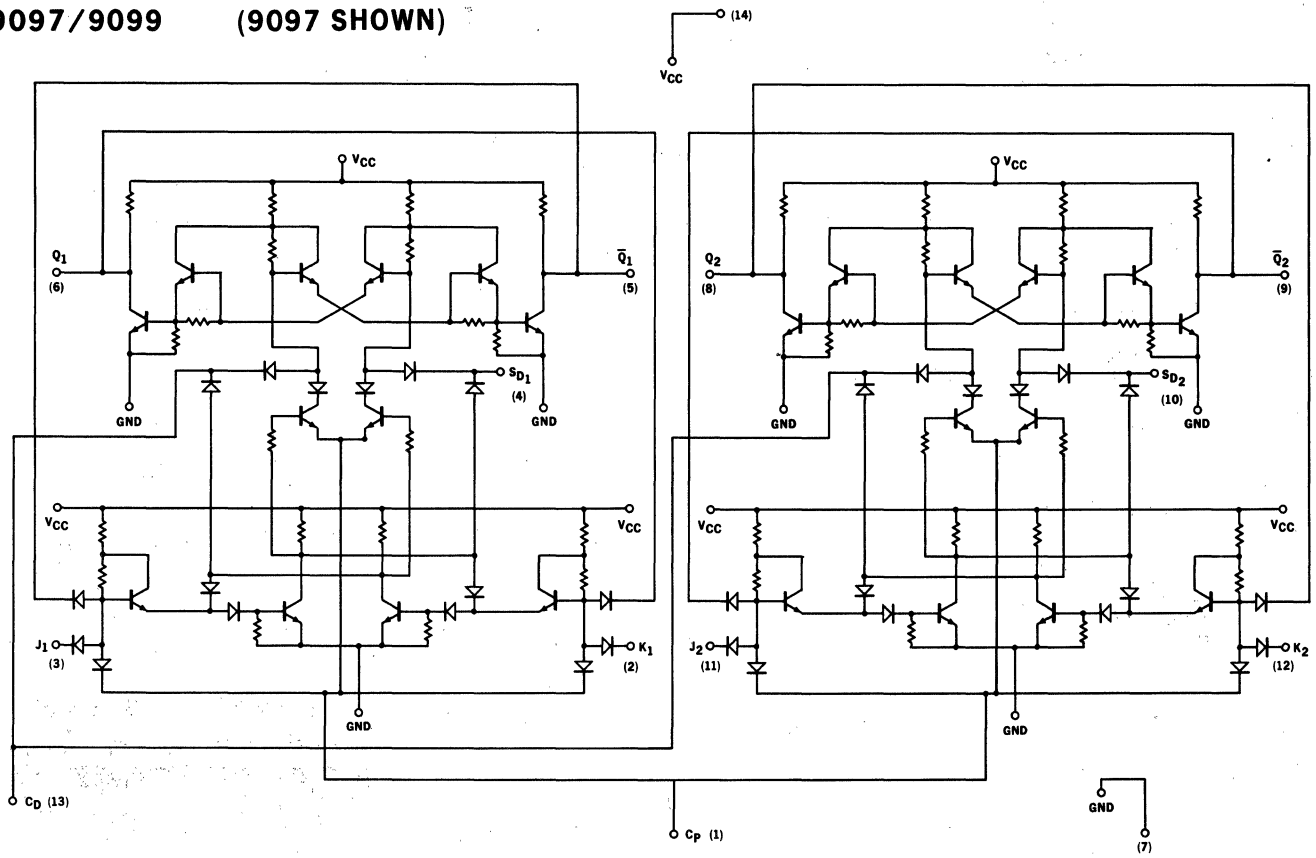
FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

9093/9094 (9093 SHOWN)



9097/9099 (9097 SHOWN)



HIGH LEVEL LOGIC DIODE-TRANSISTOR MICROLOGIC®

INTEGRATED CIRCUITS COMPOSITE DATA SHEET

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

0°C TO 75°C TEMPERATURE RANGE

GENERAL DESCRIPTION — The Fairchild High Level Logic Diode-Transistor Micrologic® Integrated Circuit family (HLLDTμL) consists of three high voltage, high threshold hex inverters which offer extremely good D.C. and A.C. Noise Immunity. These circuits are useful in applications involving a high noise environment or high voltage supply which prohibits the use of CCSL.

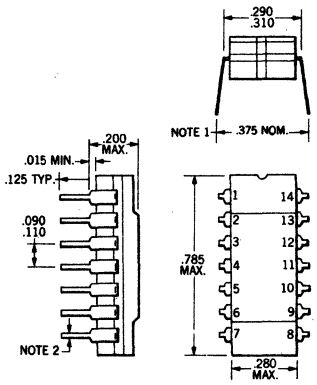
Interfacing from CCSL to HLLDTμL is accomplished with the 9112, shifting from HLLDTμL to CCSL is accomplished with the 9109. The 9112 can also be used to drive the μM3700 MOS Multiplexer.

The circuits are fabricated within a silicon monolithic substrate using standard Fairchild Planar* and Epitaxial processes.

HLLDTμL elements are available in the hermetically sealed ceramic Dual In-Line Package (DIP), designed for automated and low cost insertion techniques.

TYPICAL DUAL IN-LINE PACKAGE

similar to
JEDEC (TO-116) Outline



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 linch diameter lead.

FEATURES

- **High Voltage Operation . . . V_{CC} Range 12 to 20 V.**
- **Utilizes inexpensive external input diodes to facilitate a high density building block approach and very high Logic Fan-In where desired.**
- **High D.C. Noise Immunity . . . 6.5 V minimum**
- **High A.C. Noise Immunity . . . 10 V at 150 ns**
- **Interfaces with CCSL**

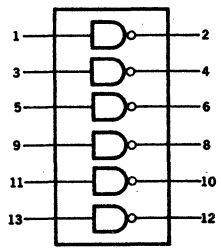
ABSOLUTE MAXIMUM RATINGS (above which the reliability of the device may be impaired)

Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +75°C
V_{CC} Pin Potential to Gnd Pin	−0.5 V to +25 V
Output Current when output is low	40 mA
Input Current (9109, 9110)	10 mA
Output Voltage	25 V
Input Voltage (9112)	5.5 V

ORDERING INFORMATION

To order HLLDTμL elements specify U6AXXXX59X, where XXXX is the four-digit number denoting the specific element desired.

LOGIC DIAGRAM



VCC = Pin 14
GND = Pin 7

*Planar is a patented Fairchild process.

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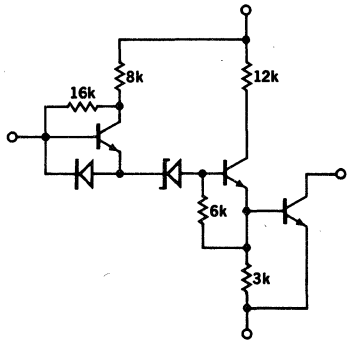
ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTIC	DEVICE	LIMITS 0°C MIN.	MAX.	+25°C MIN.	TYP.	MAX.	+75°C MIN.	MAX.	UNITS	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	9110 9112	Note 2		Note 2			Note 2		Volts	V_{CC} = 12 V to 20 V @ V_{IL} I_{OH} = −0.1 mA
I_{CEX}I	Output Leakage Current	9109		75		1.0	75		75	μA	V_{CC} = 20 V @ V_{IL} V_{OH} = 20 V
V_{OL1}	Output Low Voltage	9109 9110 9112		0.5		0.25	0.5		0.5	Volts	V_{CC} = 12 V @ V_{IH} I_{OL} = 10 mA
V_{OL2}	Output Low Voltage	9109 9110 9112		1.0		0.5	1.0		1.0	Volts	V_{CC} = 20 V @ V_{IH} I_{OL} = 20 mA
V_{IL}	Input Low Voltage	9109 9110		7.05			7.0		6.8	Volts	Input Low Threshold @ V_{OH}
		9112		1.05			1.0		0.8		
V_{IH}	Input High Voltage	9109 9110	8.6		8.5			8.4		Volts	Input High Threshold @ V_{OL}
		9112	2.1		2.0			1.9			
I_F	Input Load Current	9109 9110 9112		−1.20		−0.80	−1.12		−1.12	mA	V_{CC} = 20 V, V_F = 0.5 V
I_{SC}	Output Short Circuit Current	9110 9112		−17 −2.4		−9.0 −1.65	−16.3 −2.3		−15.6 −2.3	mA	V_{CC} = 20 V, V_{IN} = 0 V V_{OUT} = 0 V
I_{CEX}	Output Leakage Current	9110 9112		75		1.0	75		75	μA	V_{CC} = 20 V, V_{OUT} = 20 V V_{IN} = 0 V
I_{PDH}	Input High Supply Current	9109 9110				19	28			mA	V_{CC} = 20 V, Input Open
		9112				22	34				
I_R	Input Leakage Current	9112					5.0		10	μA	V_{CC} = 20 V, V_R = 4.0 V
I_{max}	Ground Current	9109 9110 9112					15			mA	V_{CC} = V_{OUT} = 25 V, Inputs @ GND
t_{pd+}	Turn Off Delay	9109 9110 9112				145	300			ns	See Fig. 4
t_{pd-}	Turn On Delay	9109 9110				95	200			ns	See Fig. 4
		9112				30	125				
V_{TN}	"0" Level A.C. Noise Immunity	9110				7.0				Volts	See Fig. 5
V_{TP}	"1" Level A.C. Noise Immunity	9110				8.5				Volts	See Fig. 5

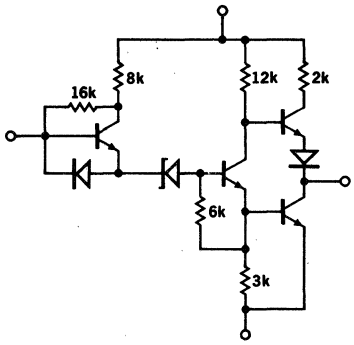
NOTES:
(1) Tests on 9109, 9110 are performed with FDH6 input diodes.
(2) MIN = V_{CC} −2.0 V for all temperature
TYP = V_{CC} −1.5 V for 25°C

Fig. 1a



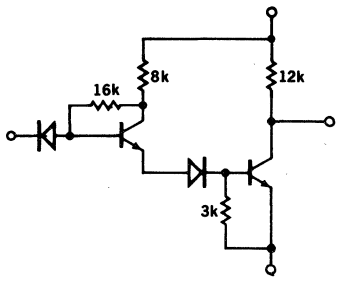
1/6 HLLDTL 9109
HLL → CCSL

Fig. 1b



1/6 HLLDTL 9110
HLL → HLL

Fig. 1c



1/6 HLLDTL 9112
CCSL → HLL

Fig. 2a

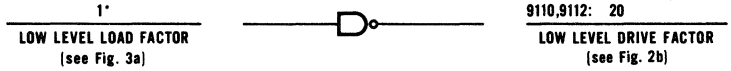


Fig. 2b
OUTPUT LOADS
(LOW LEVEL DRIVE FACTOR)
VERSUS SUPPLY VOLTAGE

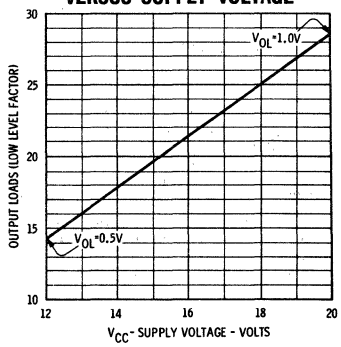


Fig. 3a
WORST CASE INPUT FORWARD
CURRENT AND INPUT LOADS
VERSUS SUPPLY VOLTAGE

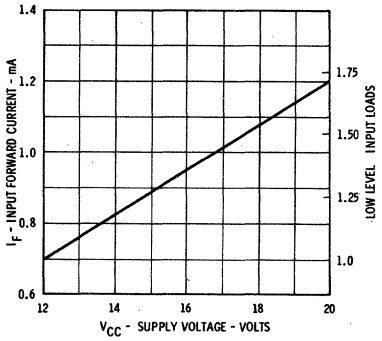


Fig. 3b
WORST CASE POWER DISSIPATION
VERSUS SUPPLY VOLTAGE
(PER GATE)

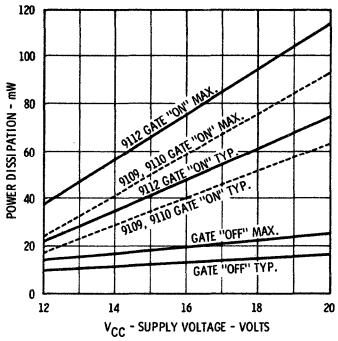


Fig. 3c
WORST CASE HIGH LEVEL
D.C. NOISE IMMUNITY
VERSUS TEMPERATURE

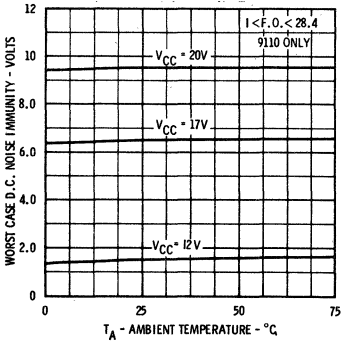


Fig. 3d
WORST CASE HIGH INPUT
THRESHOLD VOLTAGE VERSUS
FORWARD DIODE VOLTAGE

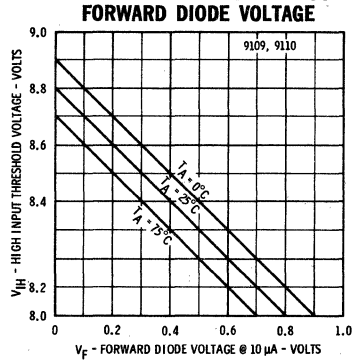


Fig. 3e
WORST CASE LOW THRESHOLD
VOLTAGE VERSUS
FORWARD DIODE VOLTAGE

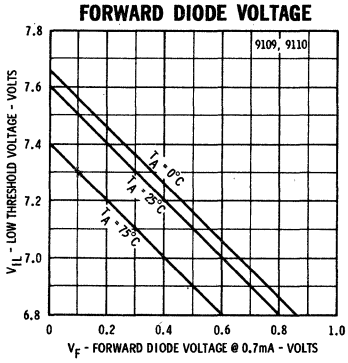


Fig. 3f
WORST CASE LOW LEVEL
D.C. NOISE IMMUNITY
VERSUS AMBIENT TEMPERATURE

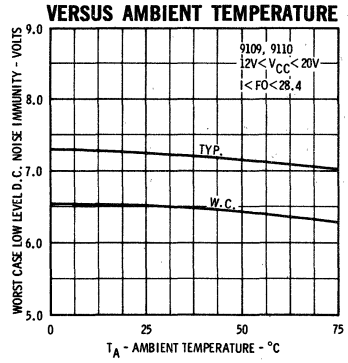


Fig. 3g
TURN OFF DELAY
VERSUS AMBIENT TEMPERATURE

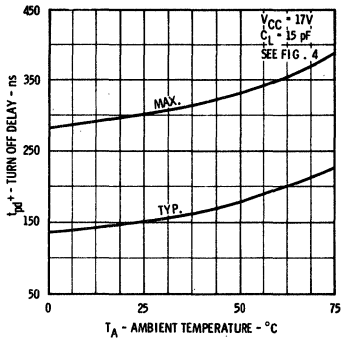


Fig. 3h
TURN ON DELAY
VERSUS AMBIENT TEMPERATURE

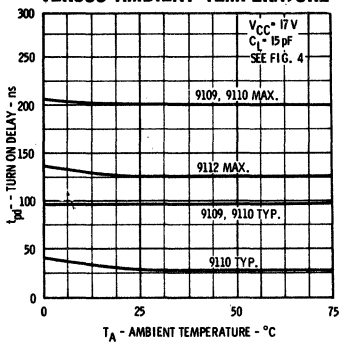


Fig. 3i
TYPICAL A.C. NOISE IMMUNITY
INPUT VOLTAGE VERSUS
PULSE WIDTH

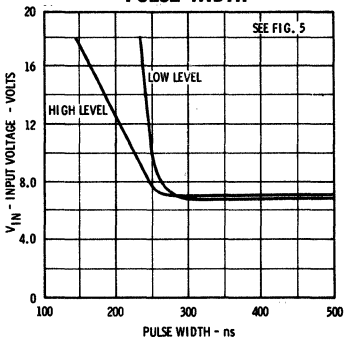
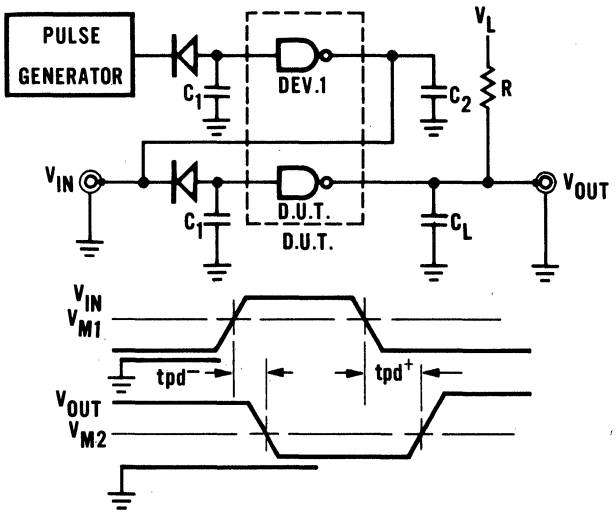


Fig. 4
SWITCHING TIME TEST CIRCUIT
AND WAVEFORMS



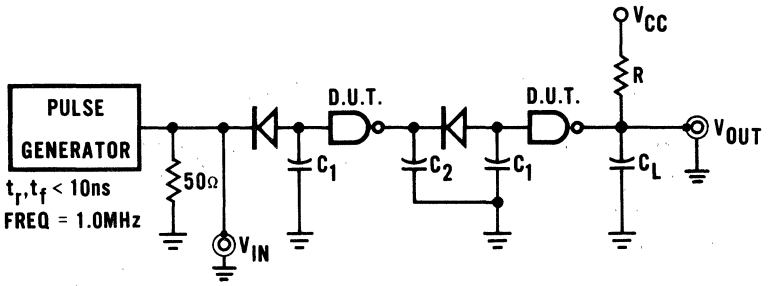
$C_1 = 5.0$ pF Includes all probe
$C_2 = 10$ pF and jig capacitance
$C_L = 15$ pF

FDH6 Input Diodes are
used on 9109, 9110

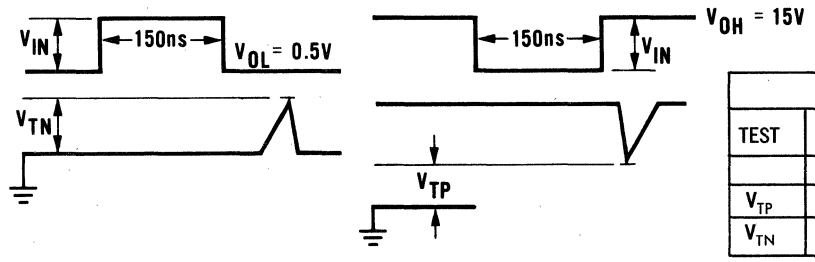
TEST CONDITIONS

D.U.T.	DEV. 1	V_{m1}(V)	V_{m2}(V)	V_L(V)	R_{tpd-}	R_{tpd+}
9109	9110	7.5	1.5	5.0	510 Ω	3.6 k
9110	9110	7.5	7.5	17.0	2.4 k	24 k
9112	932	1.5	7.5	17.0	2.4 k	24 k

Fig. 5
A.C. NOISE IMMUNITY TEST CIRCUIT



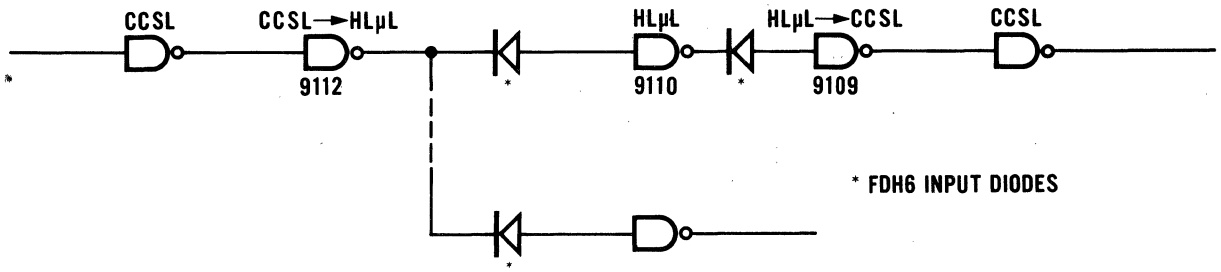
Unused inputs grounded
diodes are FDH6
$C_1 = 5.0$ pF Includes jig and
$C_2 = 10$ pF all probe capacitance
$C_L = 15$ pF



TEST CONDITIONS AND LIMITS						
TEST	LIMIT		V_{CC}	R	T_A	V_{IN}
	MIN.	MAX.	(Volts)	(kΩ)	(°C)	(Volts)
V_{TP}	8.5 V		17	24	25	10
V_{TN}		7.0 V	17	2.4	25	10

APPLICATIONS:

Fig. 6—CCSL INTERFACING



1 HLLDTL High Level Load Factor
= 1 CCSL High Level Load Factor
1 HLLDTL Low Level Load Factor
= 7.5 CCSL Low Level Load Factors

Fig. 7—LAMP DRIVER

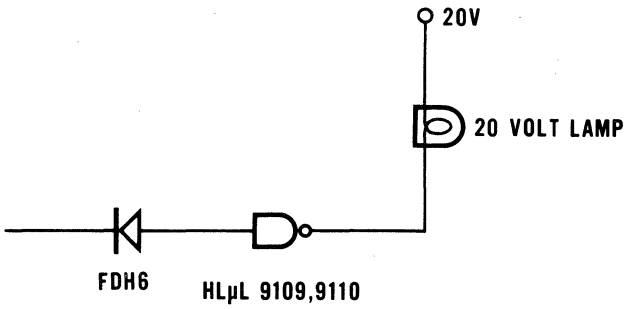
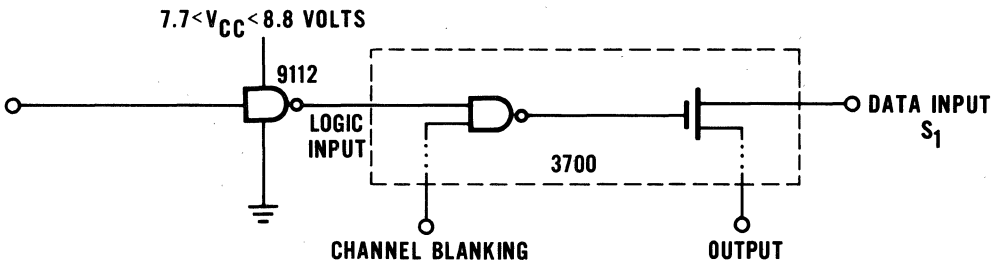
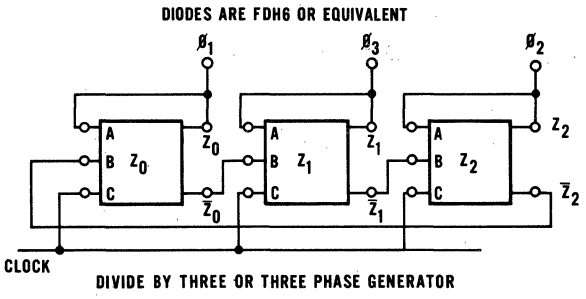


FIG. 8—DRIVING MOS3700 MULTIPLEXER OR EQUIVALENT



Output Levels : min "1" level = V_{CC} —1.5 V
: max "0" level = 0.2 V

Fig. 9—SEQUENTIAL COUNTER



ϕ_1	ϕ_3	ϕ_2	Clock
1	0	0	0
1	0	1	1
0	0	1	0
0	1	1	1
0	1	0	0
1	1	0	1

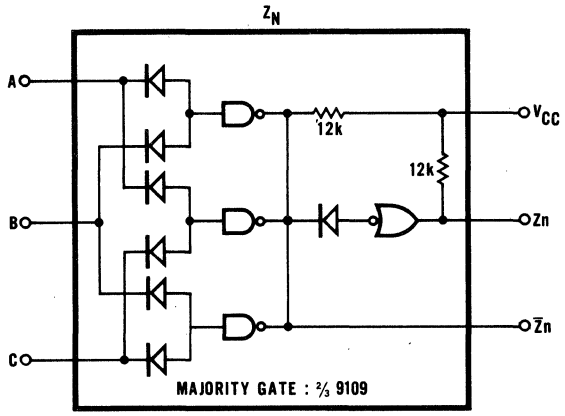
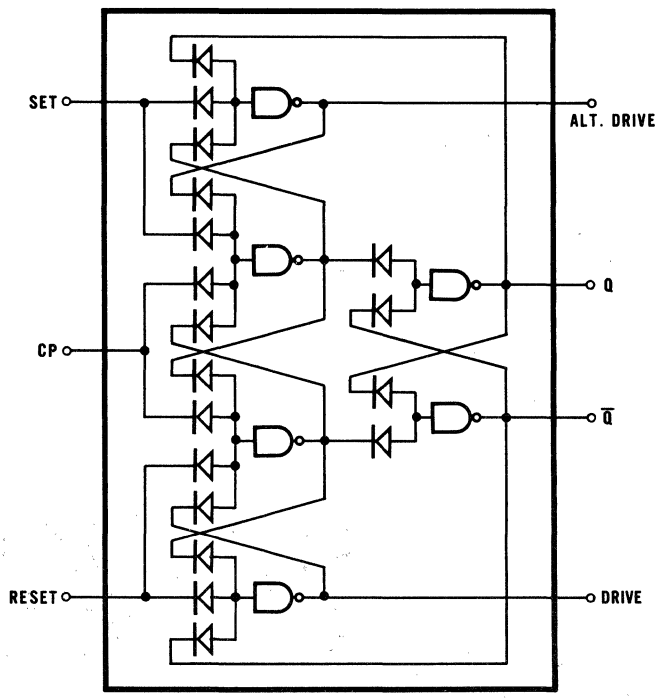
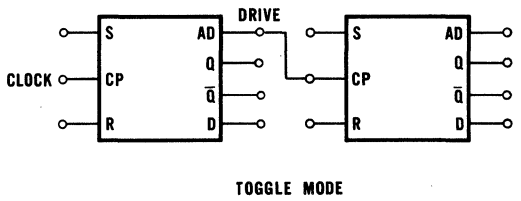
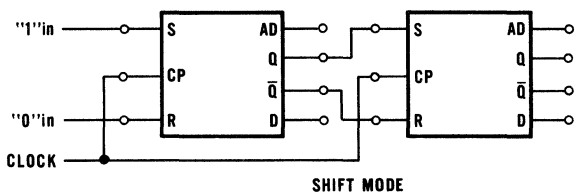


Fig. 10—JK FLIP FLOP







DIODES ARE FDH6 OR EQUIVALENT

J	K	Qn+1
L	H	L
L	L	Qn
H	H	$\overline{Q}$n
H	L	H

HLLDTμL 9109

HIGH VOLTAGE HEX INVERTER

HIGH LEVEL LOGIC DIODE-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION

The HLLDTμL9109 is a high voltage, high threshold hex inverter designed for the conversion of high level logic to any logic level from 4V to 20V. The unit is characterized by a 6.5V(min.) DC Noise Immunity and a 20V/100 nsec AC Noise Immunity. The input diode has been left off the circuit so that the input can be expanded to any number of inputs which allows maximum flexibility in use.

The 9109 is available in ceramic Dual In-Line* Package.

FEATURES

CCSL Compatibility

High Voltage Operation 12 to 20 V

Utilizes external input diodes to facilitate high density building block approach

F.O. = 7 CCSL

D.C. Noise Immunity of 6.5V

APPLICATIONS

Interfacing from HLL to CCSL levels.

Line receiver.

General purpose logic level converter

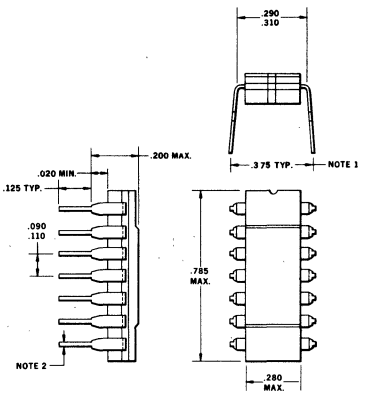
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to 150°C
Operating temperature	0°C to 75°C
V_{CC}	25 V
Output Voltage	25 V
Output low current	40 mA

*Fairchild patent pending

TYPICAL DUAL IN-LINE PACKAGE

(In accordance with JEDEC TO-116)



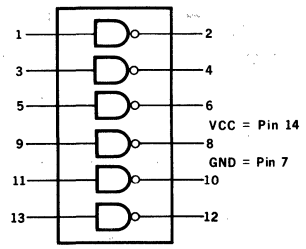
NOTES:

1 Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.

2 Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

ORDER PART NO. U6A910959X

LOGIC DIAGRAM



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FAIRCHILD SEMICONDUCTOR

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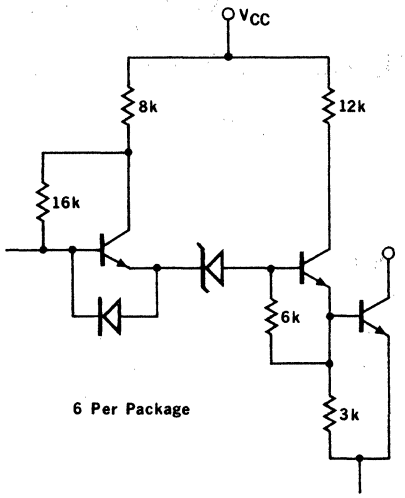
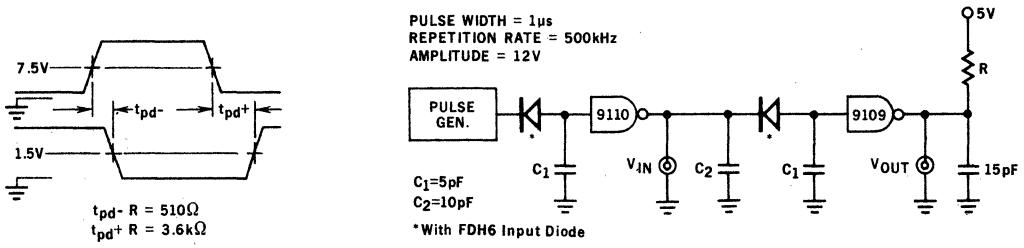


CIRCUIT DIAGRAM

ELECTRICAL CHARACTERISTICS

SYMBOL	LIMITS						UNITS	CONDITIONS AND COMMENTS
	0°C		25°C			75°C		
	MIN.	MAX.	MIN.	TYP.	MAX.	MIN. MAX.		
I_{OH}	75			0.2	75	75	μA	V_{CC} = 20 V, V_{OH} = 20 V
V_{IL}					7.0	6.8	Volts	
V_{OL1}		0.5		0.25	0.5	0.5	Volts	V_{CC} = 12 V, I_{OL} = 10 mA V_{IH} = Value indicated on this table.
V_{OL2}		1.0		0.5	1.0	1.0		V_{CC} = 20 V, I_{OL} = 20 mA
V_{IH}	8.6		8.5				Volts	
I_F		-1.24		-.81	-1.16		mA	V_{CC} = 20 V, V_F = 0.5 V
I_{PDH}	30			19	28		mA	V_{CC} = 20 V, Inputs open
I_{PDL}	9.5			6.0	9.0		mA	V_{CC} = 25 V, Inputs GnD V_{OUT} = 25 V
t_{pd}^+				145	400		ns	See switching time test circuit
t_{pd}^-				85	200		ns	

NOTE: Tests are performed with FDH6 input diode.



CIRCUIT AND WAVEFORMS FOR SWITCHING TESTS

HLLDTμL 9110

HIGH VOLTAGE HEX INVERTER

HIGH LEVEL LOGIC DIODE-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION

The HLLDTμL 9110 is a high voltage, high threshold hex inverter with extremely good D.C. and A.C. Noise Immunity. The circuit is useful in applications involving a high noise environment or high voltage supplies which prohibit the use of DTμL.

The 9110 contains six basic logic building blocks from which more complex functions (Flip-Flop, Shift Registers, etc.) can easily be built.
The 9110 is available in the hermetically sealed cermic Dual-In-Line Package (DIP), designed for automated and low cost insertion techniques.

FEATURES

- High Voltage Operation V_{CC} Range 12 to 20 V.
- Utilizes inexpensive external input diodes to facilitate a high density building block approach and a very high logic Fan-In where desired.
- High D.C. Noise Immunity 6.5 V minimum
- High A.C. Noise Immunity 10 V at 150 ns.

APPLICATIONS

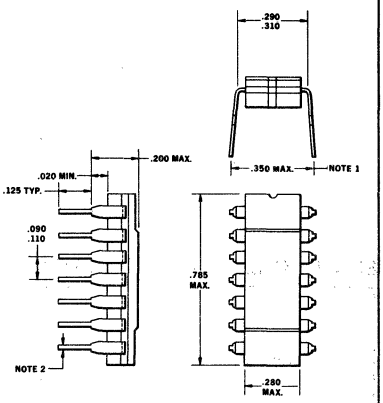
Industrial Control Logic, Automotive Logic, Lamp Driver, Relay Driver

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to 150°C
Operating Temperature	0°C to 75°C
V_{CC}	25 V
Output Voltage	25 V
Output low current	40 mA

TYPICAL DUAL IN-LINE PACKAGE

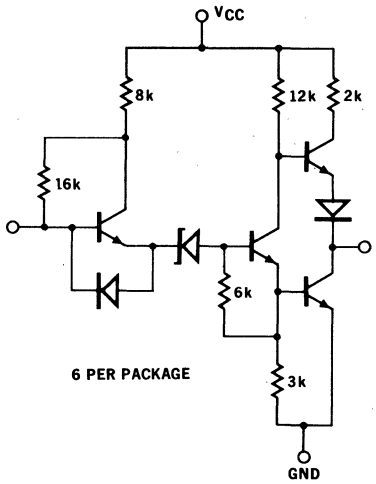
In Accordance With
JEDEC (TO-116) Outline



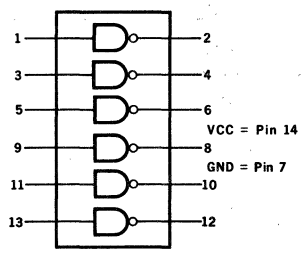
NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

ORDER PART NO. U6A911059X

CIRCUIT DIAGRAM



LOGIC DIAGRAM



* Fairchild patent pending

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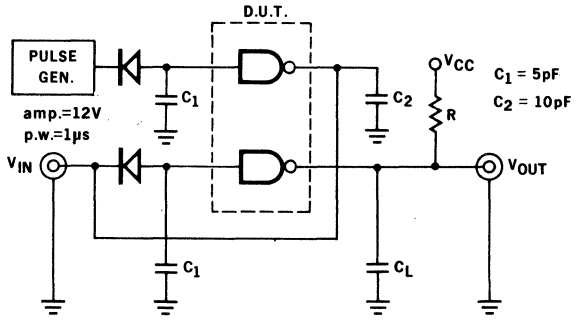
FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

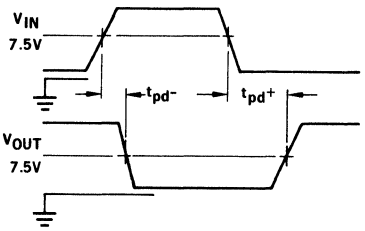
ELECTRICAL CHARACTERISTICS

SYMBOL	LIMITS 0°C MIN.	0°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	75°C MIN.	75°C MAX.	UNITS	CONDITIONS AND COMMENTS
V_{OH}			$V_{OH\ (min.)} = (V_{CC} - 2.0\,V)$ $V_{OH(typ.)} = (V_{CC} - 1.5\,V)$					Volts	V_{CC} = 12 to 20 V I_{OH} = -0.1 mA @ V_{IL}
V_{IL}					7.0		6.8	Volts	V_{CC} = 12 to 20 V
V_{OL1}		0.5		0.25	0.5		0.5	Volts	V_{CC} = 12 V I_{OL} = 10 mA @ V_{IH}
V_{OL2}		1.0		0.5	1.0		1.0	Volts	V_{CC} = 20 V I_{OL} = 20 mA @ V_{IH}
V_{IH}	8.6		8.5					Volts	V_{CC} = 12 to 20 V
I_F		-1.24		-0.81	-1.16		-1.16	mA	V_{CC} = 20 V V_F = 0.5 V
I_{SC}		17.0		9.0	16.3		15.6	mA	V_{CC} = 20 V V_{out} = 0 V
I_{PDH}		30		19	28		28	mA	V_{CC} = 20 V Inputs open.
I_{PDL}		9.5		6.0	9.0		9.0	mA	V_{CC} = 25 V Inputs GND Outputs = 25 V
t_{pd+}				145	400			ns	See switching
t_{pd-}				100	200			ns	test circuit.

SWITCHING TIME TEST CIRCUIT

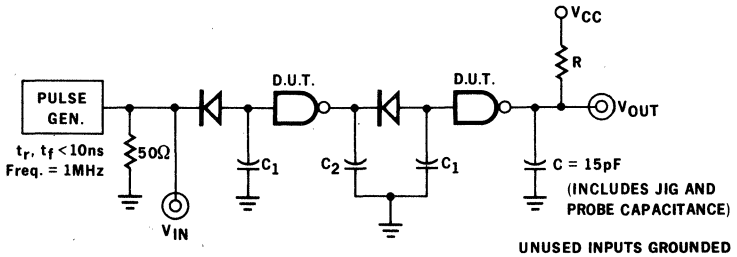


C_L = 15pF
t_{pd^-} : R = 2.4k
t_{pd^+} : R = 24k
*INCLUDES JIG CAPACITANCE
DIODES ARE FDH6
GND UNUSED INPUTS



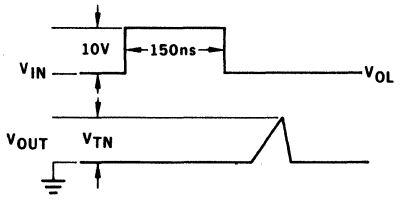
NOTE: TESTS ARE PERFORMED WITH FDH6 INPUT DIODE

A.C. NOISE IMMUNITY TEST CIRCUIT

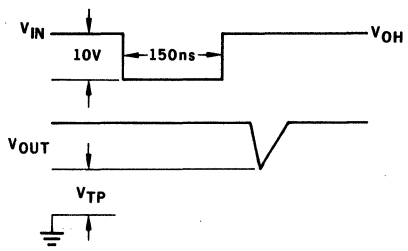


UNUSED INPUTS GROUNDED
DIODES ARE FDH6
C_1 = 5pF
C_2 = 10pF

LOW LEVEL AC NOISE IMMUNITY



HIGH LEVEL AC NOISE IMMUNITY



TEST CONDITIONS AND LIMITS					
TEST	LIMIT MIN.	LIMIT MAX.	V_{CC} (Volts)	R kΩ	T_A °C
V_{TP}	8.5 V		17	24k	25
V_{TN}		7.0 V	17	2.4	25

DTμL 9111

PARALLEL GATED-CLOCKED FLIP-FLOP

FAIRCHILD DIODE-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

INDUSTRIAL MICROCIRCUITS - 0°C TO +75°C TEMPERATURE RANGE

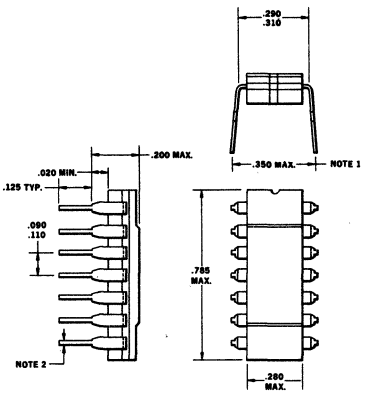
GENERAL DESCRIPTION - The DTμL9111 is a Parallel Gated, Clocked Flip-Flop. It features directly coupled units operating on the "master-slave" principle. Operation is logically and electrically identical to the DTμL9948 with the addition of another pair of two-input gates at the inputs of the flip-flop. This feature enhances the Logic design of some counters and shift-registers and can significantly reduce can count.

A direct clear input is provided which allows asynchronous entry irrespective of signals applied to any other inputs.

Output buffers provide isolation between the "slave" and the output load, thereby enhancing immunity to signal line noise.

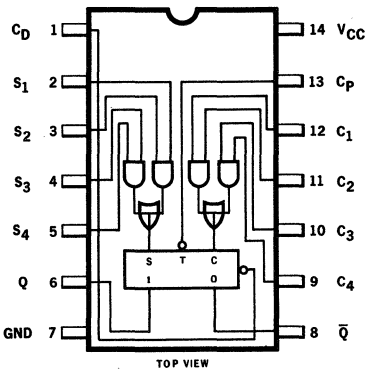
The DTμL9111 is completely compatible with all of the Fairchild 9930 Series Diode-Transistor Micrologic® integrated circuits.

TYPICAL DUAL IN-LINE PACKAGE



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

LOGIC DIAGRAM



TOP VIEW

$f_s = (S_1 \cdot S_2 + S_3 \cdot S_4)\, C_p$

$f_c = (C_1 \cdot C_2 + C_3 \cdot C_4) C_p + C_D$

INPUT-OUTPUT LOADING FACTORS

(V_{CC} = 5.0 V)

Output Drive

Pins 6 & 8 = 11

Input Loading

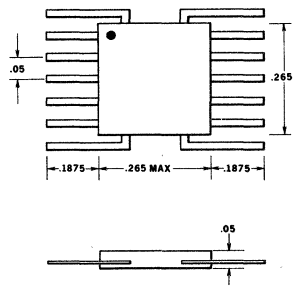
Pins 2, 3, 4, 5, 9, 10, 11, 12 = 2/3

Pin 1 = 2

Pin 13 = 3

TYPICAL FLAT PACKAGE

TOP VIEW



ORDER INFORMATION:

To order the DTμL9111 element, specify the following Part Number:

U31911159X for Flat Pkg.

U6A911159X for Dual In-Line Pkg.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

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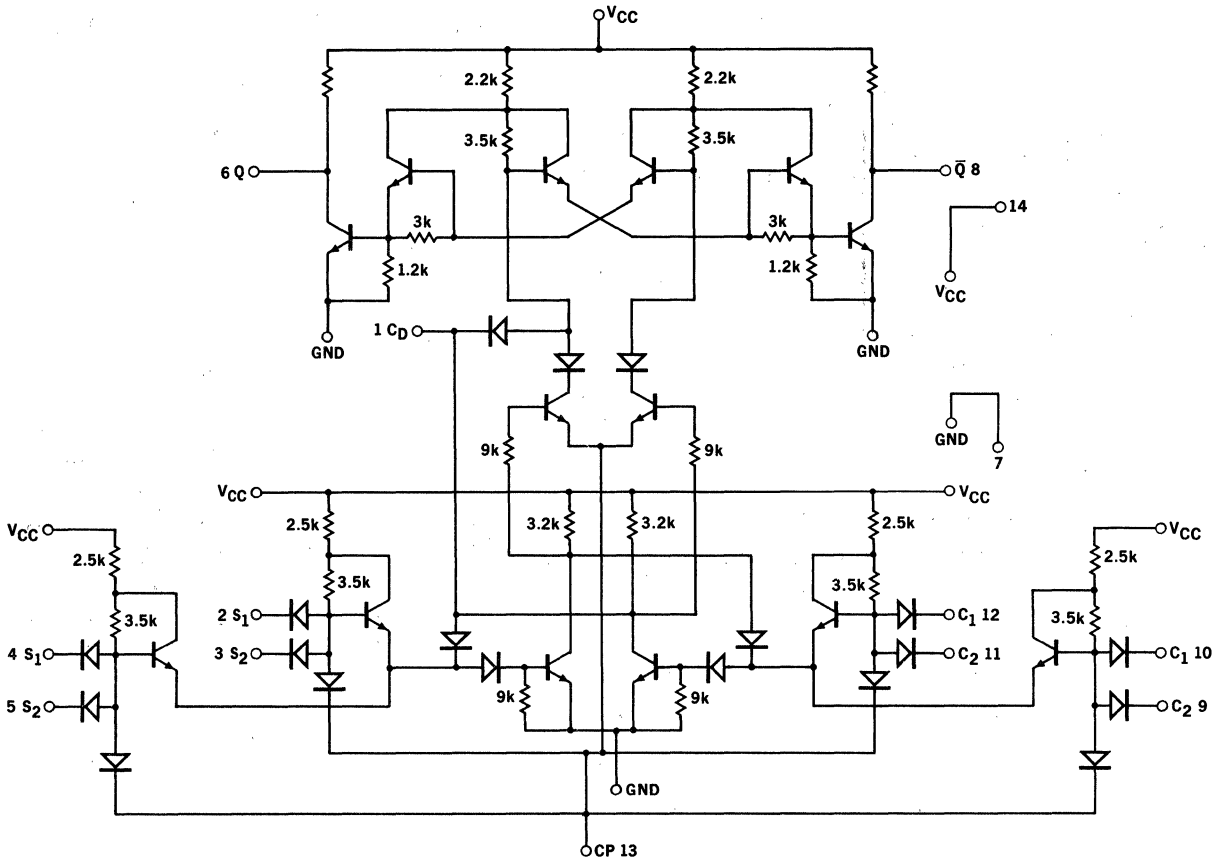
SCHEMATIC DIAGRAM



TRUTH TABLE

SYNCHRONOUS ENTRY

	INPUTS t_n								OUTPUTS t_{n+1}	
Pin	2	3	4	5	9	10	11	12	6	8
	L	X	L	X	L	X	L	X	NC	NC
	X	L	X	L	X	L	X	L	NC	NC
	H	H	X	X	L	X	X	L	H	L
	X	X	H	H	X	L	L	X	H	L
	L	X	X	X	H	H	X	X	L	H
	X	L	L	X	X	X	H	H	L	H
	H	H	X	X	H	H	X	X	Undetermined	
	X	X	H	H	X	X	H	H	Undetermined	

This is a partial table showing significant input-output conditions. Other conditions are similar combinations. Operation is best defined by the set and clear functions shown on Page 1.

For J-K Mode operation:

Connect 6 to 11 and 9; 8 to 3 and 5.

ASYNCHRONOUS ENTRY*

INPUT	OUTPUTS	
Pin 1	6	8
H	NC	NC
L	L	H

*Asynchronous entry is independent of all other inputs and overrides synchronous entry.

NOTES:

(1) Pin numbers refer to flat package or dual in-line package.

(2) Abbreviations used in the body of tables:

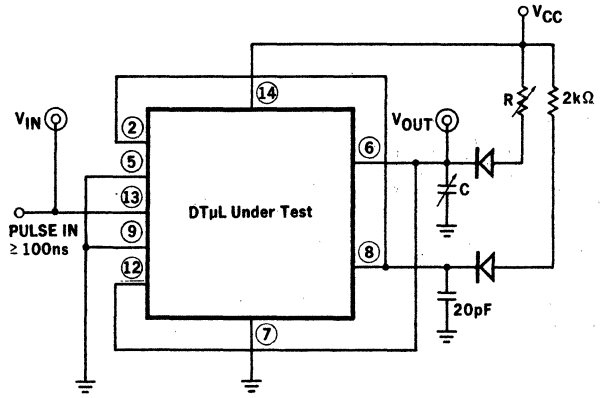
L = low, the more negative voltage level

H = high, the more positive voltage level
(In all cases, unused pins have the same effect as high.)

X = immaterial, either H or L has equal effect

NC = no change, the trigger-pulse has no effect on outputs

tpd TEST CIRCUIT

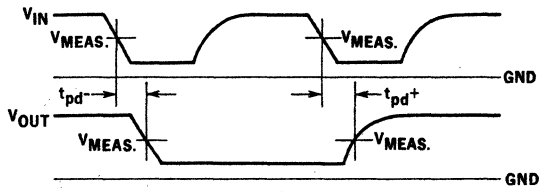


(V_{CC} = 5.0 V, T = 25°C)

	R	C	Min.	Max.
t_{pd+}	2.0 k	30 pF	30 ns	65 ns
t_{pd-}	330 Ω	50 pF	30 ns	75 ns

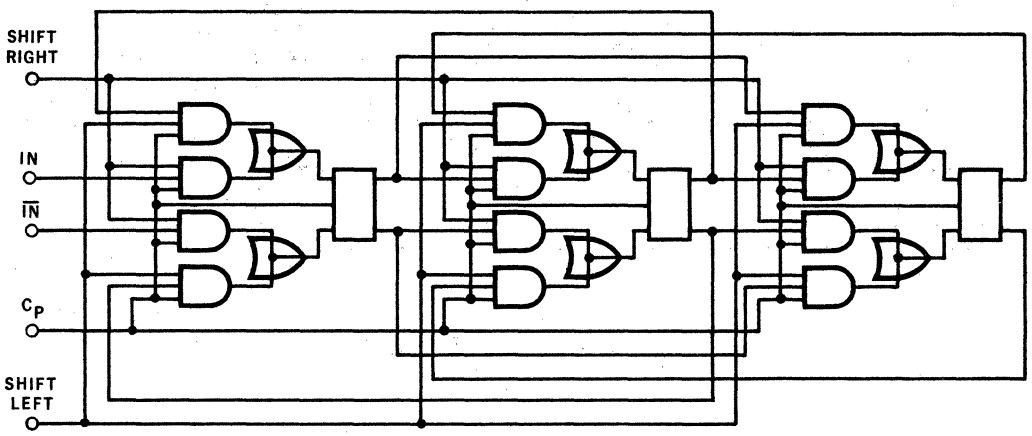
DIODES ARE FD600 OR EQUIVALENT.
ALL C's INCLUDE JIG & PROBE.

WAVE FORMS



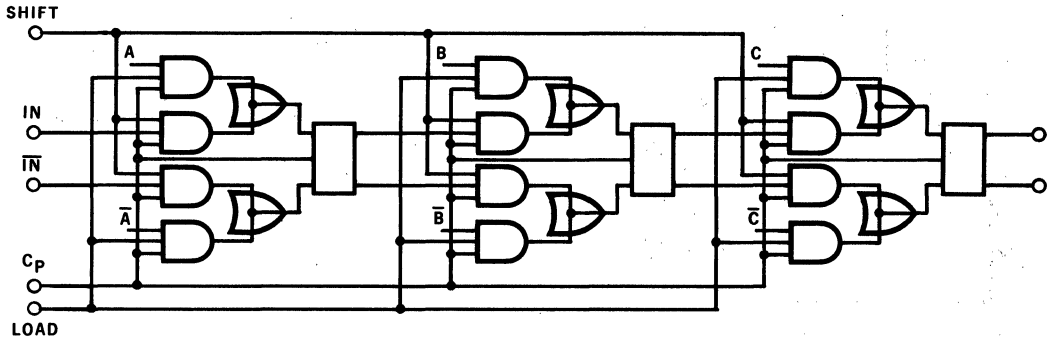
$V_{meas.}$ = 1.5 V at +25°C

TYPICAL APPLICATIONS

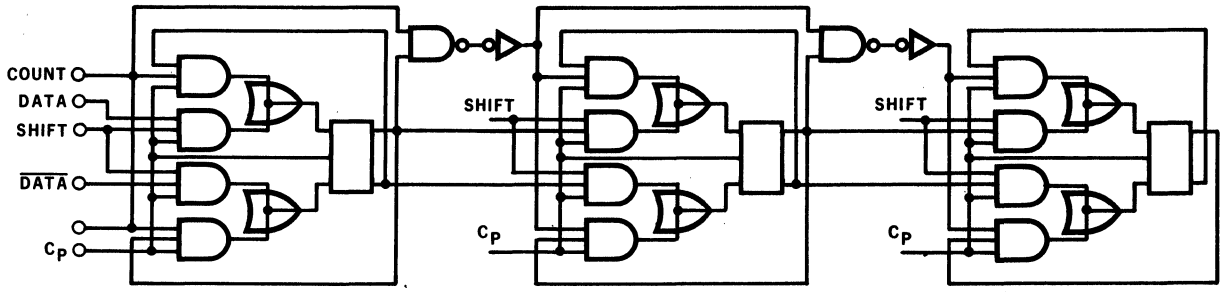


SHIFT RIGHT / SHIFT LEFT SHIFT REGISTER

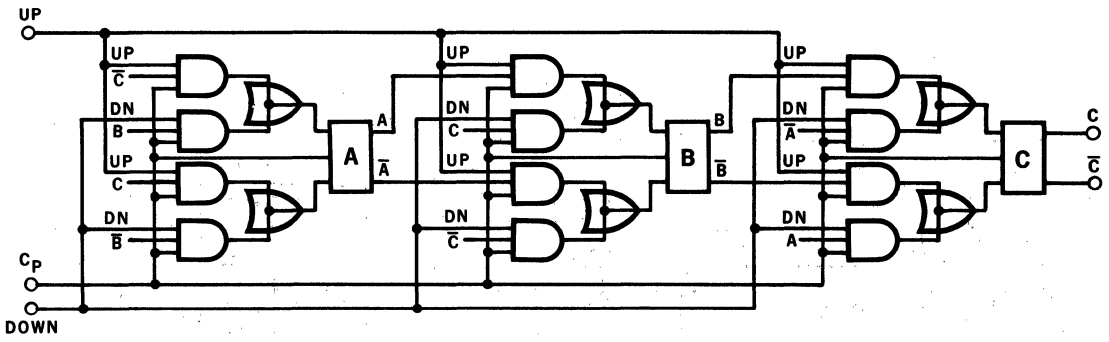
TYPICAL APPLICATIONS



SHIFT REGISTER WITH PARALLEL INPUT LOADING



SERIAL ENTRY - BINARY COUNTER



THREE STAGE MOIBUS COUNTER

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

HLLDTμL 9112

HIGH VOLTAGE HEX INVERTER

HIGH LEVEL LOGIC DIODE-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

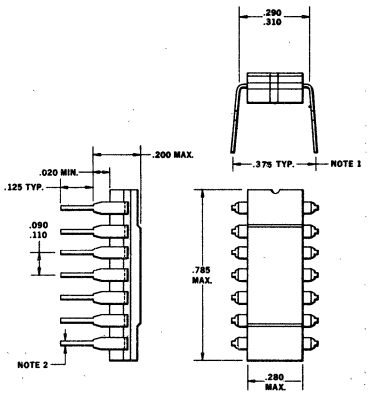
GENERAL DESCRIPTION

The HLLDTμL9112 is a CCSL to high level hex interface element, The 9112 consists of six gates suitable for converting from CCSL levels up to high logic levels (10V to 18V.) The 9112 is ideal for driving MOS devices such as the μM3700 element (6 Channel Multiplexer.)

The 9112 is available in ceramic Dual In-Line* Package.

TYPICAL DUAL IN-LINE PACKAGE

(In accordance with JEDEC TO-116)



NOTES:

1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead

ORDER PART NO. U6A911259X

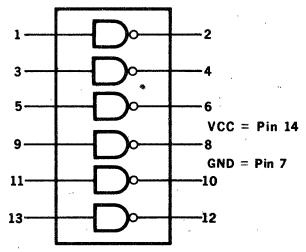
FEATURES

- CCSL Compatibility
- High Voltage Operation — V_{CC} Range 12 to 20 V
- F.O. = 10 HL
- Wired-OR Capability
- Good AC Noise Immunity

APPLICATIONS

- CCSL→HL interface element
- MOS driver

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Storage temperature	-65°C to 150°C
Operating temperature	0°C to 75°C
V_{CC}	25 V
Output Voltage	25 V
Output low current	40 mA

*Fairchild patent pending

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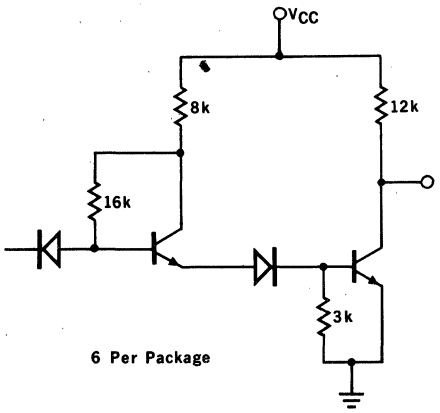
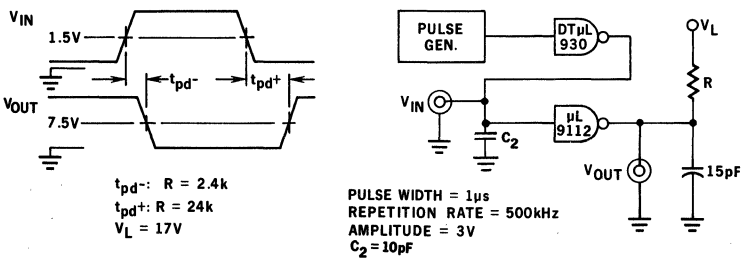


CIRCUIT DIAGRAM

ELECTRICAL CHARACTERISTICS

SYMBOL	LIMITS 0°C MIN.	MAX.	25°C MIN.	TYP.	MAX.	75°C MIN.	MAX.	UNITS	CONDITIONS AND COMMENTS
V_{OH} (Output High)			18	18.5				Volts	V_{CC} = 20 V, I_{OH} = 0.1 mA V_{IL} = Value indicated in this table.
V_{IL}					1.0		0.8	Volts	
I_{CEX} (Output Leakage)		75		0.2	75		75	μA	V_{CC} = 20 V, V_{OH} = 20. V V_{IN} = OV
V_{OL1} (Output Low)		0.5		0.25	0.5		0.5	Volts	V_{CC} = 12 V, I_{OL} = 10 mA V_{IH} = Value indicated in this table.
V_{IH}	2.1		2.0				0.8	Volts	
V_{OL2}		1.0		0.5	1.0		1.0	Volts	V_{CC} = 20 V, I_{OL} = 20 mA
I_F (Input Low)		-1.20		-0.8	-1.12		-1.12	mA	V_{CC} = 20 V, V_F = 0.45 V
I_{SC} (Output Shorted)		-2.4		-1.65	-2.3		-2.3	mA	V_{CC} = 20 V, V_{IN} = 0 V V_{OUT} = 0 V
I_{PDH} (Power Diss.)		36		22	34		34	mA	V_{CC} = 20 V, Input open
I_{PDL} (Power Diss.)		9.5		6.0	9.0		9.0	mA	V_{CC} = 25 V, Input GND V_{OUT} = 25 V
t_{pd}^+ (Turn Off)				145	400			ns	See switching time test circuit
t_{pd}^- (Turn On)				25	200			ns	



CIRCUIT AND WAVEFORMS FOR SWITCHING TESTS

9300

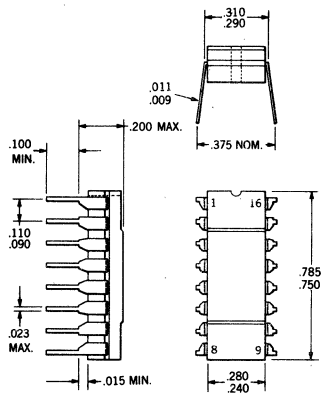
MSI 4-BIT SHIFT REGISTER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9300 Four Bit Shift Register is a high speed multi-functional sequential logic block which is useful in a wide variety of register and counter applications. As a register it may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data transfers. The circuit uses TTμL for high speed and high fanout capability, and is compatible with all devices in the CCSL group of digital integrated circuits.

- **15 MHz shift frequency**
- **Synchronous parallel entry**
- **J, $\overline{K}$ inputs to first stage**
- **Asynchronous common reset**
- **Typical power dissipation of 300 mW**
- **The input/output characteristics provide easy interfacing with Fairchild DTμL, LPDTμL, and TTμL families (CCSL).**
- **All ceramic "HERMETIC" 16 pin Dual In-Line package.**
- **Input diode clamping**

PHYSICAL DIMENSIONS



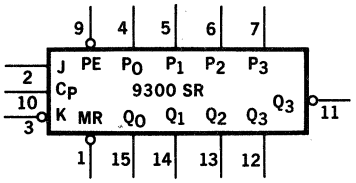
NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

Figure 1

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to +V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

Figure 2

ORDER INFORMATION

Specify U6B9300XXX for 16 pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

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FUNCTIONAL DESCRIPTION

The logic symbol of Figure 2 provides an indication of the functional characteristics of the 9300 four bit shift register. Several special logical features of the 9300 design which provide a high degree of general usefulness are described below:

1. A J$\overline{K}$ input is provided to the first flip flop in the register. This type of input is the same as the more common JK input except that the low voltage level activates the $\overline{K}$ input. This provides the greater power of the JK type input for more general applications and at the same time the simple D type input that is most appropriate for a shift register can be easily obtained by simply tying the two inputs together.
2. There is no restriction on the activity of the J or $\overline{K}$ inputs for logical operation — except for the set up and release time requirements.
3. Parallel inputs for all four stages are provided. These will determine the next condition of the shift register synchronous with the clock input, whenever the Parallel Enable input is low. With the Parallel Enable input low the element appears as four common clocked D flip flops. When the Parallel Enable is high, or not connected, the shift register performs a one bit shift for each clock input. In both cases the next state of the flip flops occurs after the low to high transition of the clock input.
4. An internal clock buffer provides both reduced clock input loading, and the ability to gate the clock with only a single NAND gate.
5. The active high output is provided for all four stages and an active low output is provided for the last stage.
6. A master asynchronous clear input allows the setting to zero of all stages, independent of the condition of any other inputs.

TABLE I — TRUTH TABLE FOR SERIAL ENTRY
(PE = HIGH, MR = HIGH, (n + 1) indicates state after next clock)

J	$\overline{K}$	Q_0 at t_{n+1}
L	L	L
L	H	Q_0 at t_n (no change)
H	L	$\overline{Q}_0$ at t_n (toggles)
H	H	H

TABLE II — LOADING RULES (1 U.L. = 1 TTμL Gate Input Load)

INPUTS	LOADING
J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3	1 U.L.
$\overline{PE}$	2.3 U.L.
C_P	4 U.L.
OUTPUTS	**FANOUT**
Q_0, Q_1, Q_2, Q_3 & $\overline{Q}_3$	6 U.L.

TABLE III
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part #U6B930051X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.2		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.36\ mA$
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 9.6\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 7.44\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current* J, K, MR, P_0, P_1, P_2 & P_3		−1.6 −1.24		−1.10 −0.97	−1.6 −1.24		−1.6 −1.24	mA mA	$V_{CC} = 5.5\ V$ $V_{CC} = 4.5\ V$ $V_F = 0.4\ V$
I_R	Input Leakage Current* J, K, MR, P_0, P_1, P_2 & P_3				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$

TABLE IV
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) (Part #U6B930059X)

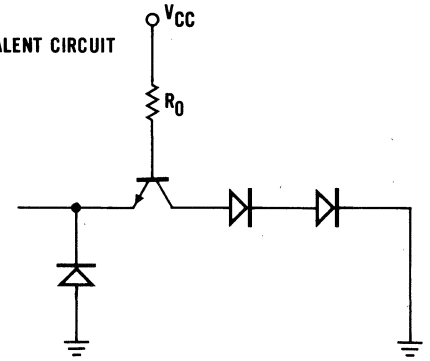
SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.36\ mA$
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 9.6\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 8.5\ mA$ Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current* J, $\overline{K}$, MR, P_0, P_1, P_2 & P_3		−1.6 −1.41		−1.0 −0.9	−1.6 −1.41		−1.6 −1.41	mA mA	$V_{CC} = 5.25\ V$ $V_{CC} = 4.75\ V$, $V_F = 0.45\ V$
I_R	Input Leakage Current* J, $\overline{K}$. MR, P_0, P_1, P_2 & P_3				15	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$

*For CP and PE input currents, use load factors in Table II

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

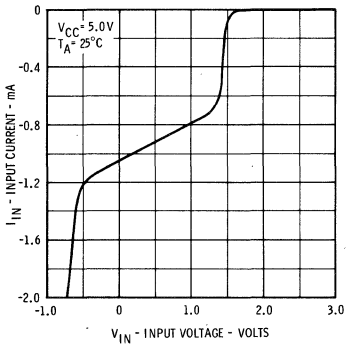
INPUTS

EQUIVALENT CIRCUIT

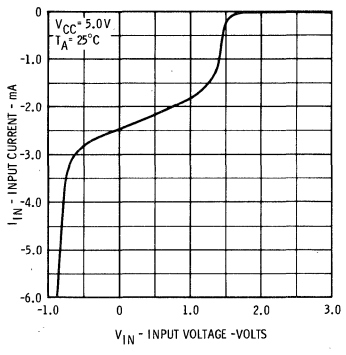


INPUT CURRENT VERSUS INPUT VOLTAGE

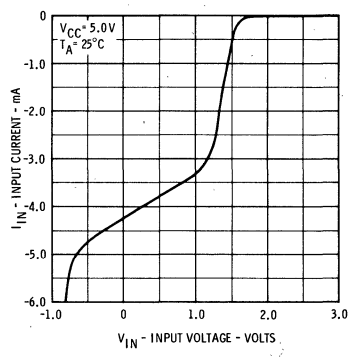
$\overline{MR}$, J, $\overline{K}$, P_0, P_1, P_2 & P_3



$\overline{PE}$

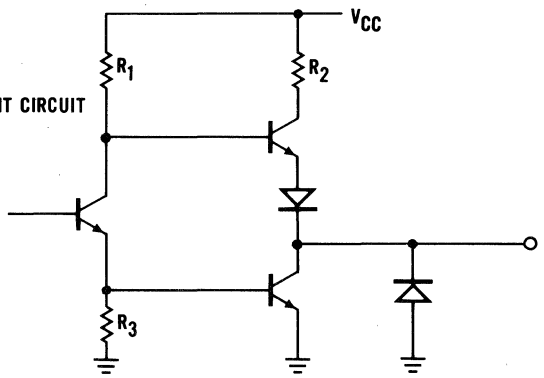


CP



OUTPUTS

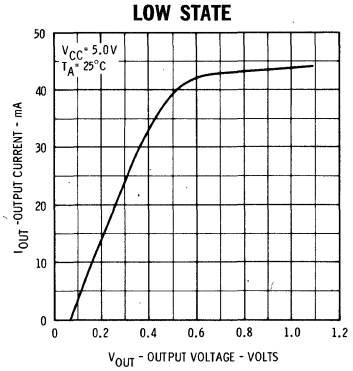
EQUIVALENT CIRCUIT



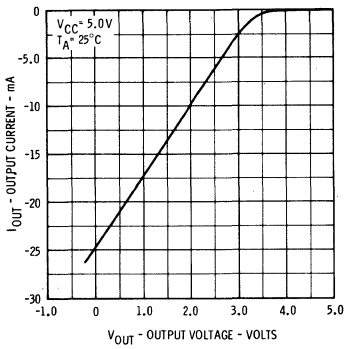
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

(Q_0, Q_1, Q_2, Q_3 AND $\overline{Q}_3$)

LOW STATE



HIGH STATE



SWITCHING CHARACTERISTICS ($T_A = 25°C$) (Parts #U6B930051X and U6B930059X)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+}	Turn Off Delay		20	35	ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{pd-}	Turn On Delay		25	45	ns	(See Fig. 5 & 6a)
f_{sr}	Shift Right Frequency	15	25		MHz	$V_{CC} = 5.0$ V, $C_L = 15$ pF (See Fig. 5 & 6c)
CP_{pw}	Clock Pulse Width	35	15		ns	
t_s	Set-up Time	35	17		ns	$V_{CC} = 5.0$ V
t_r	Release Time		16	0	ns	$C_L = 15$ pF
$t_s(\overline{PE})$	Set-up Time for $\overline{PE}$	45	26		ns	(See Figs. 6a & 6b)
$t_r(\overline{PE})$	Release Time for $\overline{PE}$		25	10	ns	
$t_{pd-}(\overline{MR})$	Reset Time for $\overline{MR}$		35		ns	
$t_{rec}(\overline{MR})$	Recovery Time for $\overline{MR}$		20		ns	
$\overline{MR}_{pw}$	Min Reset Pulse Width		15		ns	

SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) to respond.

RELEASE TIME: t_r is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) not to respond.

RECOVERY TIME FOR $\overline{MR}$: $t_{rec}(\overline{MR})$ is defined as the minimum time required between the end of the reset pulse and the clock transition from low to high in order for the flip-flop(s) to respond to the clock.

Figure 3
PROPAGATION DELAY — CLOCK TO Q_3 OR $\overline{Q}_3$ OUTPUT VS TEMPERATURE

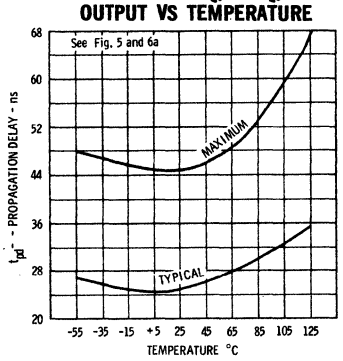
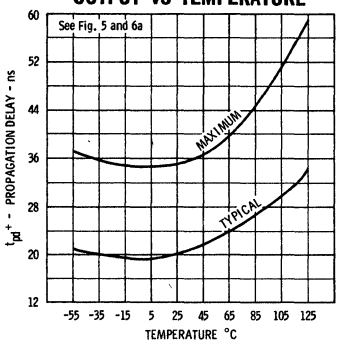
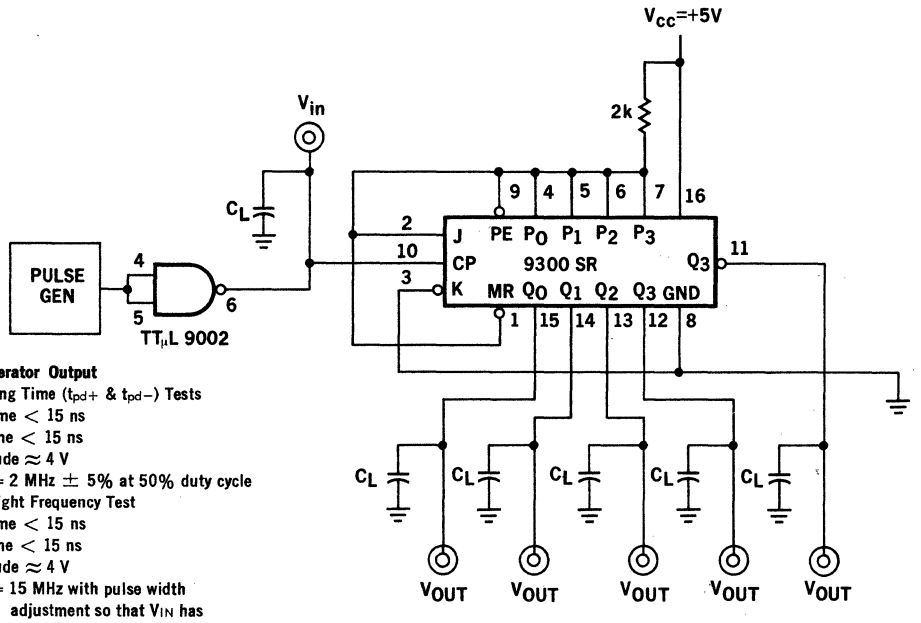


Figure 4
PROPAGATION DELAY — CLOCK TO Q_3 OR $\overline{Q}_3$ OUTPUT VS TEMPERATURE





Pulse Generator Output
1. Switching Time (t_{pd+} & t_{pd-}) Tests
   Rise Time < 15 ns
   Fall Time < 15 ns
   Amplitude ≈ 4 V
   Freq. = 2 MHz ± 5% at 50% duty cycle
2. Shift Right Frequency Test
   Rise Time < 15 ns
   Fall Time < 15 ns
   Amplitude ≈ 4 V
   Freq. = 15 MHz with pulse width adjustment so that V_{IN} has duty cycle of approx. 50%.

C_L includes probe and jig capacitance

Figure 5 — SWITCHING TIME & SHIFT RIGHT FREQUENCY TEST CIRCUIT

Fig. 6a

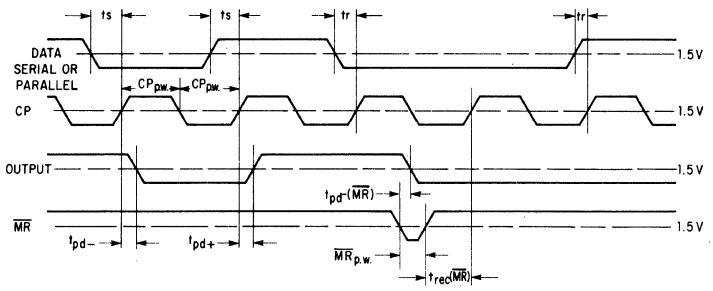


Fig. 6b

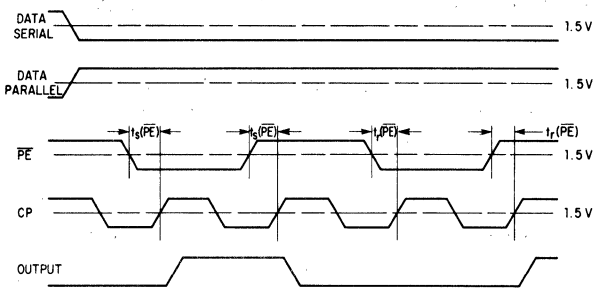
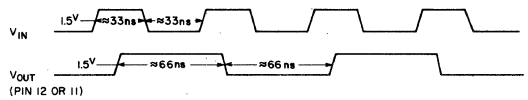


Fig. 6c



VOUT Frequency = ½ X VIN Frequency

Figure 6 — SWITCHING TIME & SHIFT RIGHT FREQUENCY WAVEFORMS

APPLICATIONS — The 9300 has been designed to be useful in a wide variety of applications. The multifunctional capability of the Fairchild 9300 is illustrated by the applications shown below.

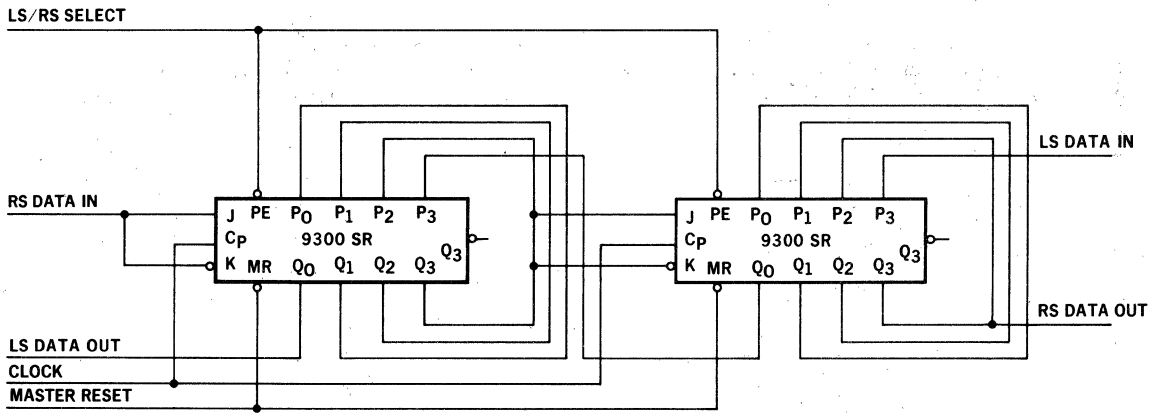


Figure 7 — EIGHT BIT LEFT/RIGHT SHIFT REGISTER

This register shifts Left or Right on each shift clock, depending upon the condition of the LS/RS SELECT input. If this input is high, Right Shift occurs and if low, Left Shift occurs.

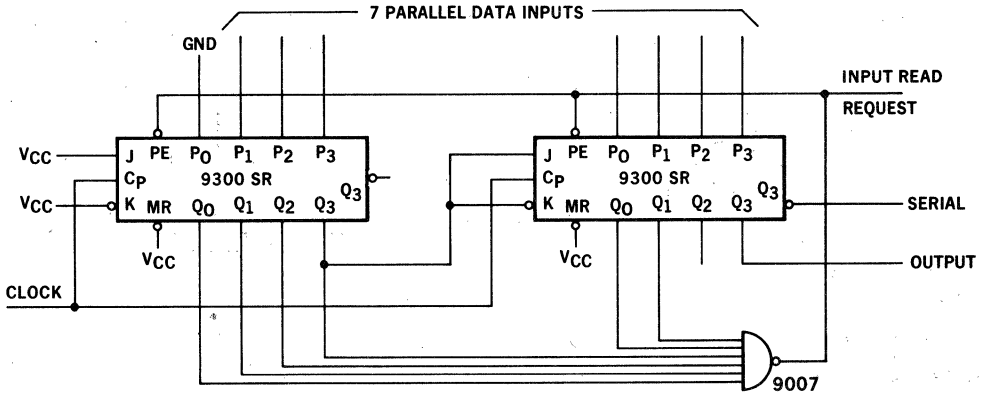


Figure 8 — SEVEN BIT PARALLEL TO SERIAL CONVERTER

This parallel to serial converter uses a marker bit, to count the data bits shifted out, so that a parallel load enable is generated to load the next parallel word for conversion at the correct time.

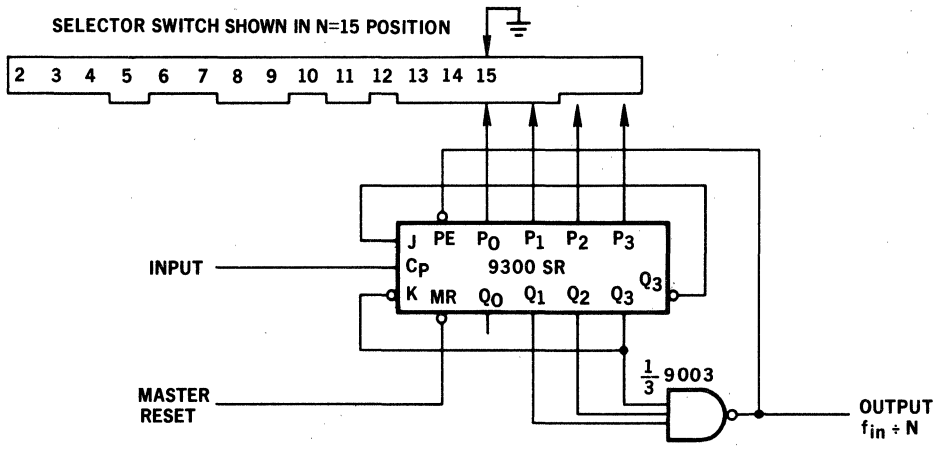
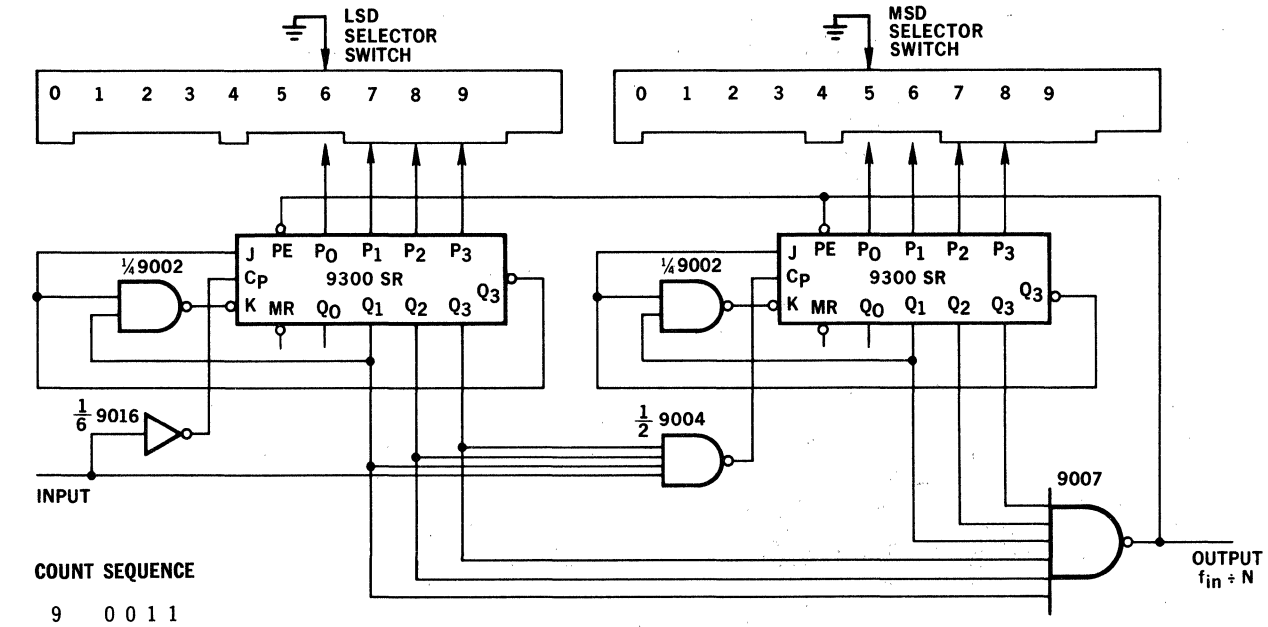


Figure 9 — DIVIDE BY N COUNTER FOR N = 2 to 15

This counter produces an output pulse for every N input pulses, where the number N is determined by the setting of the slide selector switch as shown or by logic inputs to the parallel data lines from an external source.



COUNT SEQUENCE

9	0 0 1 1
8	0 0 0 1
7	0 0 0 0
6	1 0 0 0
5	1 1 0 0
4	0 1 1 0
3	1 0 1 1
2	1 1 0 1
1	1 1 1 0
0	0 1 1 1

Figure 10 — TWO DECADE PROGRAMMABLE DIVIDER

This circuit divides by any number "N" from 1 to 100. The selected N is one greater than is shown on the slide switches. As an example the switches are showing 56, therefore the circuit will divide by 57 with this setting.

9301

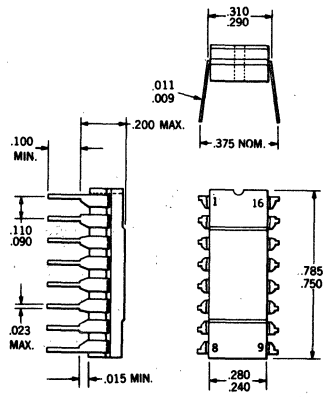
MSI ONE-OF-TEN DECODER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9301 is a multipurpose decoder designed to accept four inputs and provide 10 mutually exclusive outputs. The circuit uses TTμL for high speed and high fan out capability, and is compatible with all members of the CCSL group of digital integrated circuits.

- **Multi-function capability**
- **Mutually exclusive outputs**
- **Guaranteed fanout of 10 TTμL loads over the full temperature range and supply voltage ranges**
- **High capacitive drive capability**
- **Demultiplexing capability**
- **Typical power dissipation of 145 mW**
- **The input/output characteristics provide easy interfacing with Fairchild DTμL, LPDTμL and TTμL families (CCSL).**
- **All ceramic "HERMETIC" 16-pin Dual In-Line* package**
- **Input clamp diodes limit high speed line termination effects**

PHYSICAL DIMENSIONS



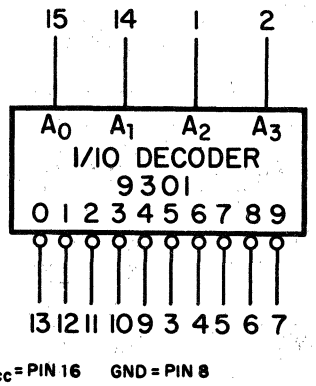
NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 linch diameter lead.

Fig. 1

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to +V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

LOGIC SYMBOL



V_{CC} = PIN 16 GND = PIN 8

Fig. 2

ORDER INFORMATION

Specify U6B9301XXX for 16 pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

*Fairchild patent pending.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FUNCTIONAL DESCRIPTION

The 9301 Decoder accepts four active high BCD inputs and provides ten mutually exclusive active low outputs, as shown by Figure 2. The active low outputs facilitate memory addressing when inverting drivers are used between decoder and memory elements such as the 9033.

The logic design of the 9301 ensures that all outputs are high when binary codes greater than nine are applied to the inputs.

The most significant A_3 input produces a useful inhibit function when the 9301 is used as a 1 out of 8 decoder. This is illustrated in the 1 out of 32 decoder shown in Figure 9.

The Truth Table and Loading Rules for the 9301 are shown in Table I and Table II.

TABLE I — TRUTH TABLE

A_0	A_1	A_2	A_3	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Voltage Level
L = Low Voltage Level

TABLE II —

LOADING RULES (1 U.L. = TTμL Gate Input Load)

INPUTS	LOADING
A_0, A_1, A_2 & A_3	1 U.L.

OUTPUTS	FANOUT
0, 1, 2, 3, 4, 5, 6, 7, 8, & 9	10 U.L.

TABLE III —

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part #U6B930151X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.6\ mA$
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 12.4\ mA$ $V_{CC} = 5.5\ V$, $I_{OL} = 16.0\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.10	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
			−1.24		−0.97	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$, $V_F = 0.4\ V$
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
t_{pd+}	Turn Off Delay Input to Output				23	35			ns	$V_{CC} = 5.0\ V$
t_{pd-}	Turn On Delay Input to Output				20	30			ns	$C_L = 15\ pF$ See Fig. 8

TABLE IV —

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%) (Part #U6B930159X)

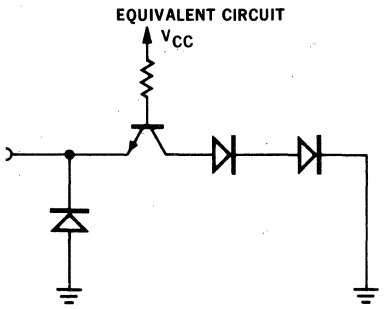
SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −0.6 mA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 14.1 mA V_{CC} = 5.25 V, I_{OL} = 16.0 mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V, V_F = 0.45 V
			−1.41		−0.9	−1.41		−1.41	mA	V_{CC} = 4.75 V, V_F = 0.45 V
I_R	Input Leakage Current				15	60		60	μA	V_{CC} = 5.25 V, V_R = 4.5 V
t_{pd+}	Turn Off Delay Input to Output				23	35			ns	V_{CC} = 5.0 V
t_{pd-}	Turn On Delay				20	30			ns	C_L = 15 pF See Fig. 8

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

Fig. 3

INPUTS

EQUIVALENT CIRCUIT



INPUT CURRENT VERSUS INPUT VOLTAGE

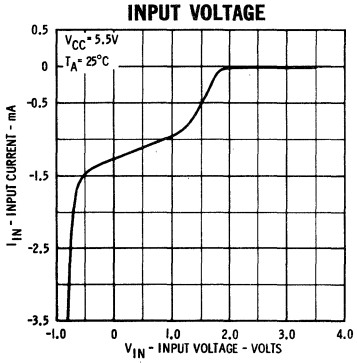
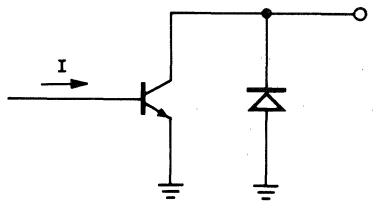


Fig. 4

OUTPUTS

EQUIVALENT CIRCUIT

OUTPUT LOW



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT LOW

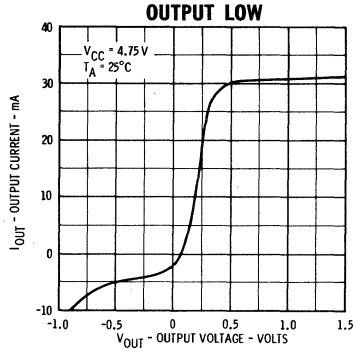
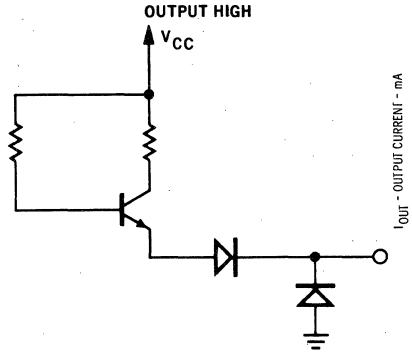
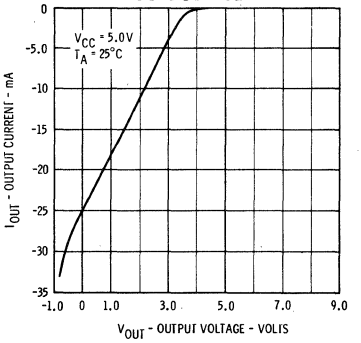


Fig. 5

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT HIGH

OUTPUT HIGH





SWITCHING PERFORMANCE

Fig. 6

TYPICAL TURN ON DELAY VERSUS TEMPERATURE

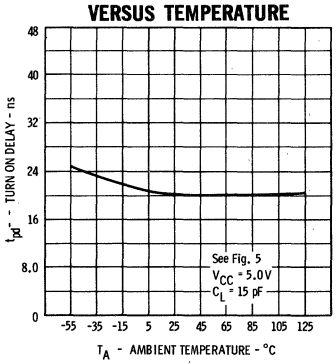
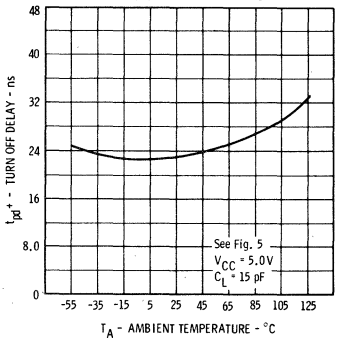
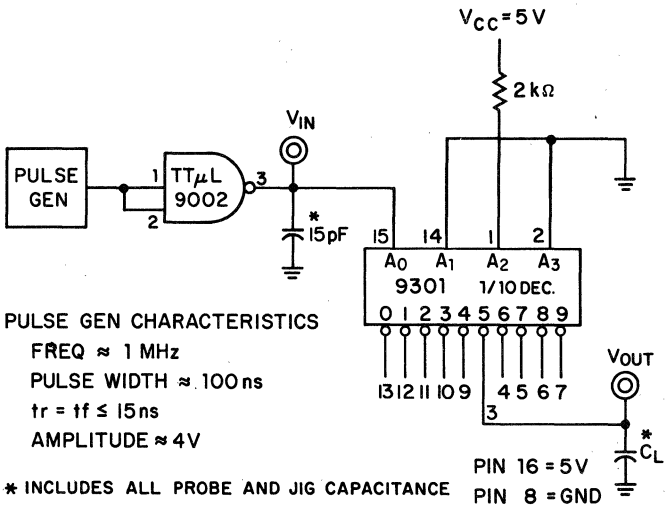


Fig. 7

TYPICAL TURN OFF DELAY VERSUS TEMPERATURE





PULSE GEN CHARACTERISTICS
- FREQ ≈ 1 MHz
- PULSE WIDTH ≈ 100 ns
- tr = tf ≤ 15 ns
- AMPLITUDE ≈ 4V

* INCLUDES ALL PROBE AND JIG CAPACITANCE

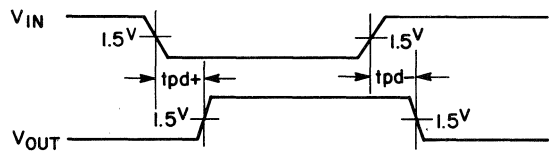


Fig. 8 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

APPLICATIONS — The 9301 decoder may be used for BCD to Decimal or 3 bit binary to octal conversion as well as many other applications. The general purpose nature of the 9301 is indicated by its use in the following applications.

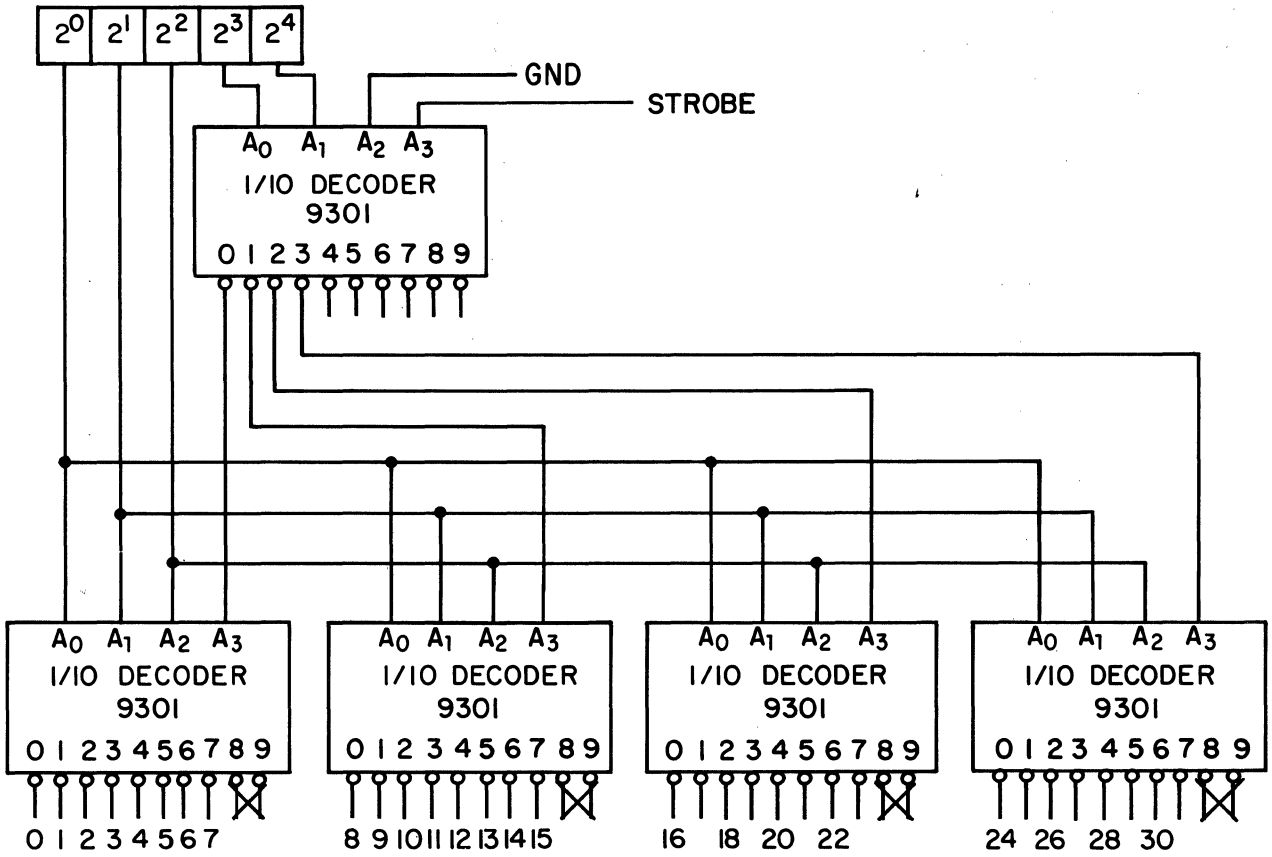
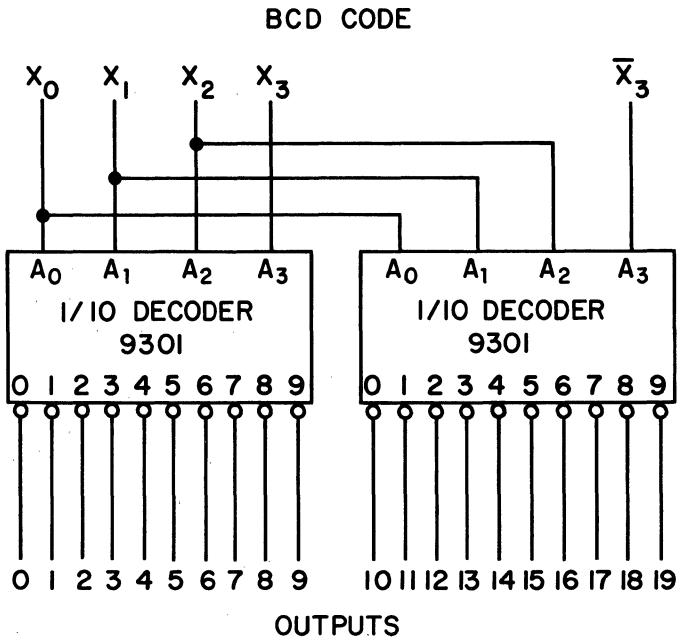


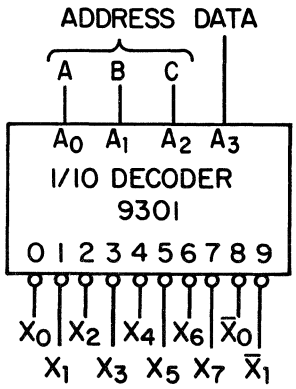
Fig. 9 — ONE-OUT-OF-THIRTY-TWO DECODING



DECIMAL DIGIT	OUTPUT SELECTION BCD CODE 8421	5421	EXCESS 3	4221
0	0, 18	0, 18	3	0, 18
1	1, 19	1, 19	4	1, 19
2	2	2	5	2
3	3	3	6	3
4	4	4	7	6
5	5	8, 10	8, 10	9, 11
6	6	9, 11	9, 11	14
7	7	12	12	15
8	8, 10	13	13	16
9	9, 11	14	14	17

Decode any BCD code using two 9301 elements. Any 4 bit BCD code may be decoded by selecting outputs as shown in the table.

Fig.10 — DECODE ANY BCD CODE

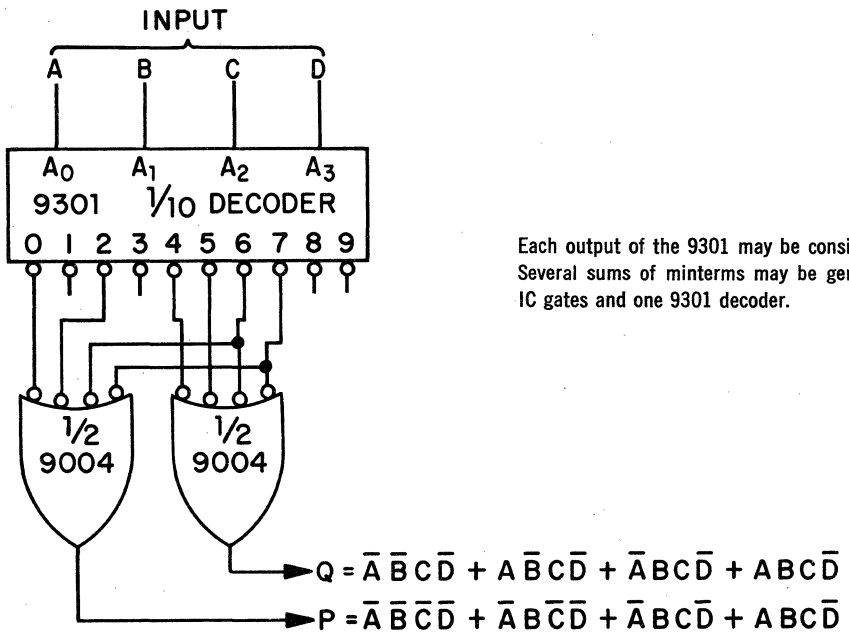


ADDRESS			OUTPUT
A	B	C	LINE
0	0	0	0
1	0	0	1
0	1	0	2
1	1	0	3
0	0	1	4
1	0	1	5
0	1	1	6
1	1	1	7

Data may be routed from a source to any of 8 outputs by addressing that output.
All non-addressed outputs remain high.

Complements of outputs 0 and 1 are available at outputs 8 and 9 respectively.

Fig. 11— DIGITAL DEMULTIPLEXER



Each output of the 9301 may be considered a minterm of the input code. Several sums of minterms may be generated economically using discrete IC gates and one 9301 decoder.

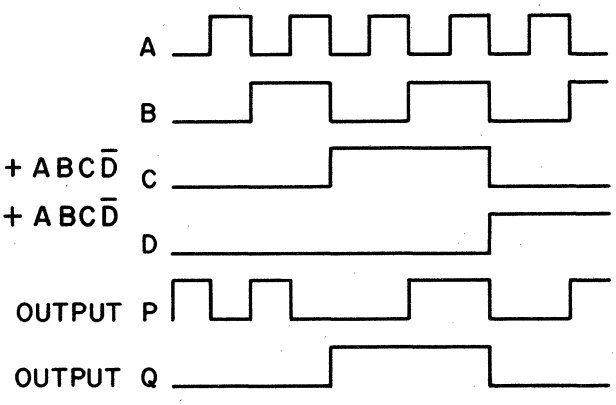


Fig. 12— MINTERM GENERATOR

9304

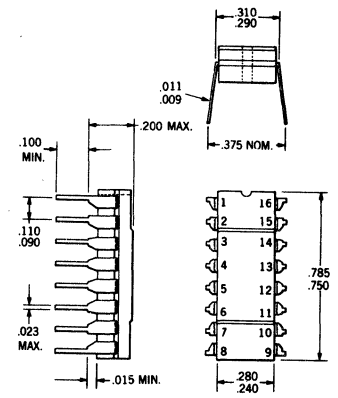
MSI DUAL FULL ADDER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9304 consists of two independent, high speed, binary full adders. The adders are useful in a wide variety of applications including multiple bit parallel add/serial carry addition, parity generation and checking, code conversion, and majority gating. The circuit uses TTμL for high speed, high fanout operation and is compatible with all members of the CCSL group of digital integrated circuits.

- **Multi-function capability**
- **8ns carry propagation delay**
- **Complementary inputs and outputs available**
- **Typical power dissipation of 150 mW**
- **The input/output characteristics provide easy interfacing with Fairchild DTμL, LPDTμL and TTμL families (CCSL).**
- **All ceramic "HERMETIC" 16-pin Dual In-Line* package**
- **Input clamp diodes limit high speed termination effects**

PHYSICAL DIMENSIONS



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

Fig. 1

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to +V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

LOGIC SYMBOL

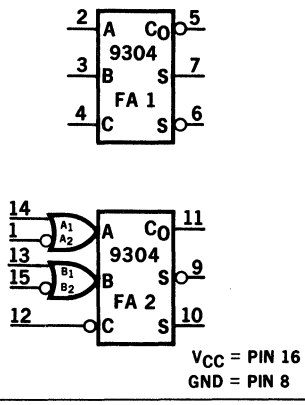


Fig. 2

ORDER INFORMATION

Specify U6B9304XXX for 16 pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

*Fairchild patent pending

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FUNCTIONAL DESCRIPTION

The Fairchild 9304 logic block consists of two separate high speed carry dependent sum full adders. This design allows a minimum carry propagation time when the adders are used in ripple carry applications. The adders are identical except that adder 2 has provision for either active high or active low inputs at the A and B terminals. The adders produce a low carry and both low and high sum with active high inputs, a high carry and both high and low sum when active low inputs are used. This principle of duality is shown in Figure 12, where the adders are drawn as functional blocks.

The Truth Table and Loading Rules for the 9304 are shown in Table I and Table II.

TABLE I — TRUTH TABLES

ADDER 1					
INPUTS			OUTPUTS		
C	B	A	$\overline{C}_O$	$\overline{S}$	S
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

ADDER 2							
INPUTS					OUTPUTS		
$\overline{C}$	B_1	A_1	$\overline{B}_2$	$\overline{A}_2$	C_O	S	$\overline{S}$
L	L	L	L	L	H	H	L
L	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H
L	L	L	H	H	L	H	L
L	L	H	L	L	H	H	L
L	L	H	L	H	H	H	L
L	L	H	H	L	H	L	H
L	L	H	H	H	H	L	H
L	H	L	L	L	H	H	L
L	H	L	L	H	H	L	H
L	H	L	H	L	H	H	L
L	H	L	H	H	H	L	H
L	H	H	L	L	H	H	L
L	H	H	L	H	H	H	L
L	H	H	H	L	H	H	L
L	H	H	H	H	H	H	L
H	L	L	L	L	H	L	H
H	L	L	L	H	L	H	L
H	L	L	H	L	L	H	L
H	L	L	H	H	L	L	H
H	L	H	L	L	H	L	H
H	L	H	L	H	H	L	H
H	L	H	H	L	L	H	L
H	L	H	H	H	L	H	L
H	H	L	L	L	H	L	H
H	H	L	L	H	L	H	L
H	H	L	H	L	H	L	H
H	H	L	H	H	L	H	L
H	H	H	L	L	H	L	H
H	H	H	L	H	H	L	H
H	H	H	H	L	H	L	H
H	H	H	H	H	H	L	H

H = High Voltage Level
L = Low Voltage Level

TABLE II —

LOADING RULES (1 U.L. = TTμL Gate Input Unit Load)

INPUTS		LOADING
FA 1	A, B & C	4 U.L.
FA 2	$\overline{A}_2$, $\overline{B}_2$ & $\overline{C}$	4 U.L.
	A_1 & B_1	1 U.L.

OUTPUTS		FANOUT
FA 1	$\overline{C}_O$	7 U.L.
	$\overline{S}$	9 U.L.
	S	10 U.L.
FA 2	C_O	7 U.L.
	S	9 U.L.
	$\overline{S}$	10 U.L.

TABLE III —
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part #U6B930451X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.2		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -1.2$ mA (Pins 7 & 9) $V_{CC} = 4.5\ V$, $I_{OH} = -1.08$ mA (Pins 6 & 10) $V_{CC} = 4.5\ V$, $I_{OH} = -0.84$ mA (Pins 5 & 11)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 16$ mA (Pins 7 & 9) $I_{OL} = 14.4$ mA (Pins 6 & 10) $I_{OL} = 11.2$ mA (Pins 5 & 11) $V_{CC} = 4.5\ V$, $I_{OL} = 12.4$ mA (Pins 7 & 9) $I_{OL} = 11.2$ mA (Pins 6 & 10) $I_{OL} = 8.7$ mA (Pins 5 & 11)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$; $V_F = 0.4\ V$, $V_R = 5.5\ V$ on other inputs
$4\ I_F$	Input Load Current		−6.4		−4.4	−6.4		−6.4		
I_F	Input Load Current		−1.24		−0.97	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$; $V_F = 0.4\ V$, $V_R = 5.5\ V$ on other inputs
$4\ I_F$	Input Load Current		−4.96		−3.88	−4.96		−4.96		
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
$4\ I_R$	Input Leakage Current				60	240		240		Ground on other inputs
t_{pd+}	C to C_O				8	13			ns	$V_{CC} = 5.0\ V$, $C_L = 15$ pF, See Fig. 11
t_{pd-}	C to C_O				8	13			ns	
t_{pd+}	A_I to $\overline{S}$				28	40			ns	
t_{pd-}	A_I to $\overline{S}$				25	35			ns	

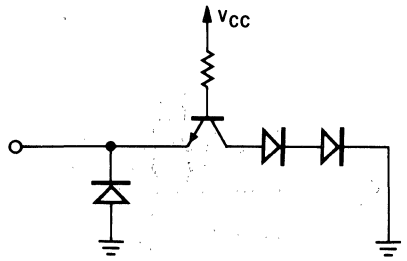
TABLE IV —
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) (Part #U6B930459X)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -1.2$ mA (Pins 7 & 9) $V_{CC} = 4.75\ V$, $I_{OH} = -1.08$ mA (Pins 6 & 10) $V_{CC} = 4.75\ V$, $I_{OH} = -0.84$ mA (Pins 5 & 11)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 16$ mA (Pins 7 & 9) $I_{OL} = 14.4$ mA (Pins 6 & 10) $I_{OL} = 11.2$ mA (Pins 5 & 11) $V_{CC} = 4.75\ V$, $I_{OL} = 14.1$ mA (Pins 7 & 9) $I_{OL} = 12.7$ mA (Pins 6 & 10) $I_{OL} = 9.85$ mA (Pins 5 & 11)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$ $V_R = 5.25\ V$ on other inputs
$4\ I_F$	Input Load Current		−6.4		−4.0	−6.4		−6.4		
I_F	Input Load Current		−1.41		−0.9	−1.41		−1.41	mA	$V_{CC} = 4.75\ V$, $V_F = 0.45\ V$ $V_R = 5.25\ V$ on other inputs
$4\ I_F$	Input Load Current		−5.64		−3.6	−5.64		−5.64		
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
$4\ I_R$	Input Leakage Current				60	240		240		Ground on other inputs
t_{pd+}	C to C_O				8.0	15			ns	$V_{CC} = 5.0\ V$, $C_L = 15$ pF, See Fig. 11
t_{pd-}	C to C_O				8.0	15			ns	
t_{pd+}	A_I to $\overline{S}$				28	45			ns	
t_{pd-}	A_I to $\overline{S}$				25	40			ns	

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUTS

EQUIVALENT CIRCUIT



INPUT CURRENT VS INPUT VOLTAGE

FIG. 3 PINS 1, 2, 3, 4, 12, 15

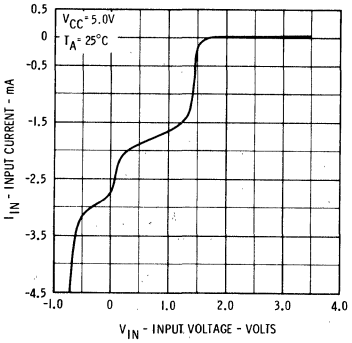
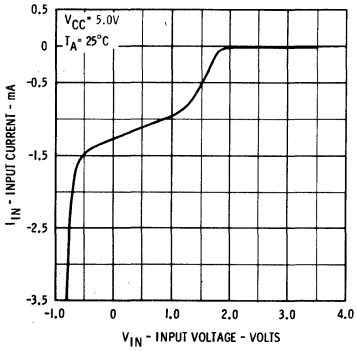
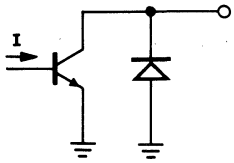


FIG. 4 PINS 13, 14

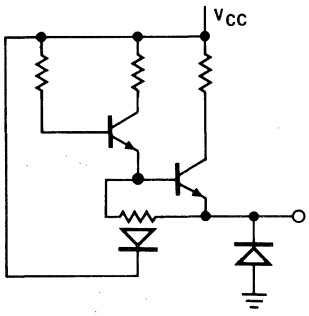


OUTPUTS

LOW STATE



HIGH STATE



OUTPUT CURRENT VS OUTPUT VOLTAGE

FIG. 5 LOW STATE

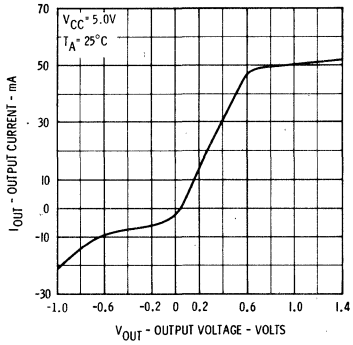


FIG. 6 HIGH STATE

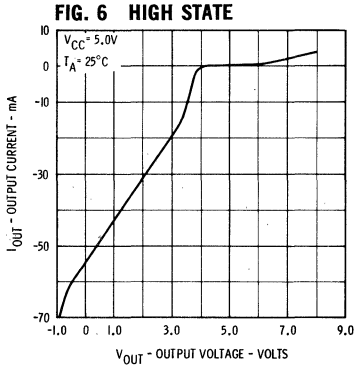


Fig. 7
TYPICAL CARRY TURN ON DELAY TIME VERSUS TEMPERATURE

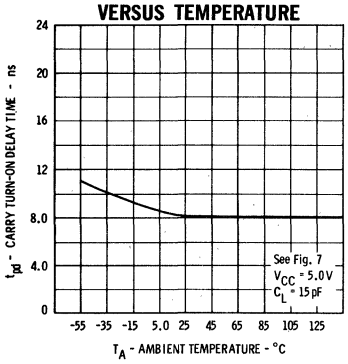


Fig. 8
TYPICAL CARRY TURN OFF DELAY TIME VERSUS TEMPERATURE

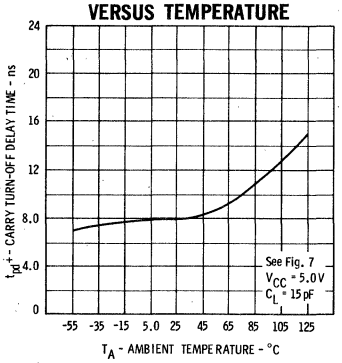


Fig. 9
TYPICAL ADD TURN ON DELAY TIME VERSUS TEMPERATURE

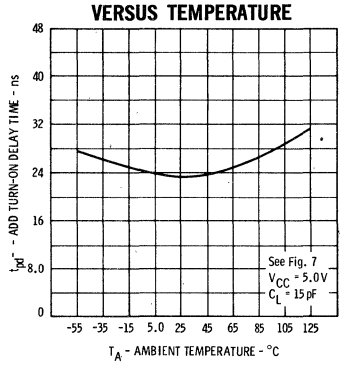
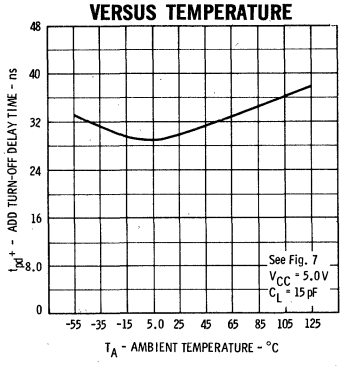
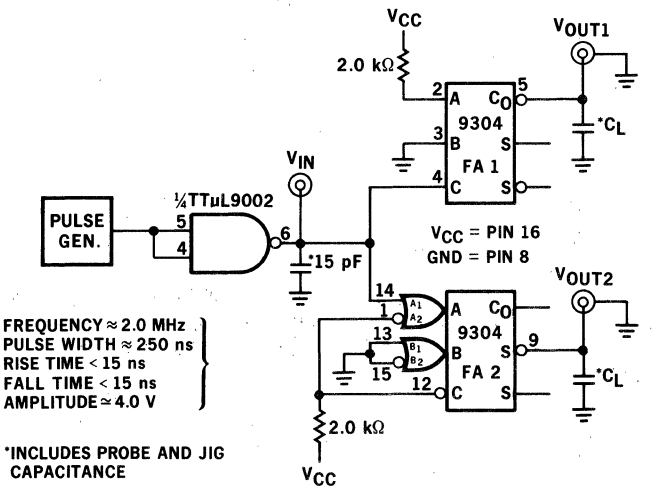
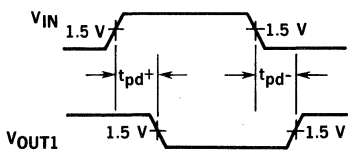


Fig. 10
TYPICAL ADD TURN OFF DELAY TIME VERSUS TEMPERATURE







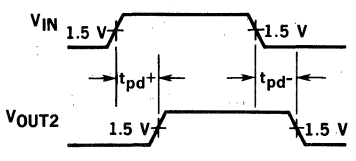


Fig.11— SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

APPLICATIONS — The 9304 dual adder has been designed to be useful in a wide variety of applications such as addition, parity generation and checking, code conversion, majority gating and other applications for which this combination of logic gates may be useful. The multifunctional capabilities of the Fairchild dual adder can be seen from reference to the applications shown.

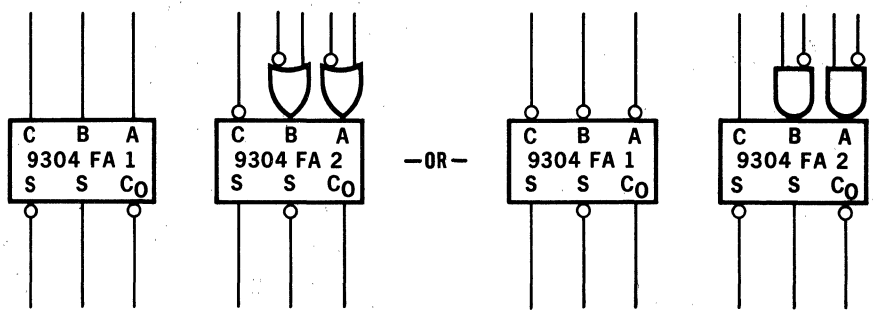


Fig.12— FUNCTIONAL BLOCK REPRESENTATION

The principle of duality allows 2 ways of representing each adder. The circuit is the same in both cases but the logic diagrams differ. The dual diagrams facilitate logic design and allow a greater understanding of the capabilities of the device.

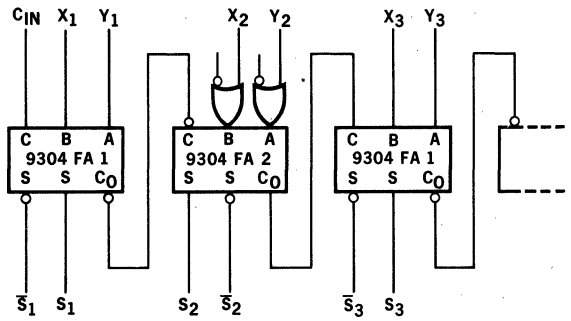


Fig.13— RIPPLE CARRY PARALLEL ADDITION

Shown above is a high speed ripple carry parallel addition scheme. Only one and-or-not gate relay is incurred at each stage allowing a typical addition speed of (N+1) x 8 ns, where N is the number of bits in the word. A similar scheme will work if the negation inputs are used, and the design acts as a subtractor when the complement of one variable is provided.

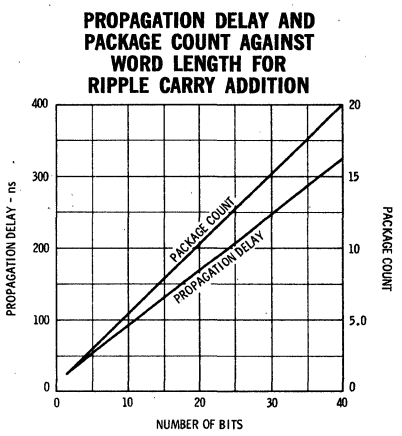


Fig. 14

The curve shows propagation delay of the ripple Carry Adder drawn in Figure 5. Plotted on the same diagram is a curve showing the low package count resulting from this Ripple Scheme.

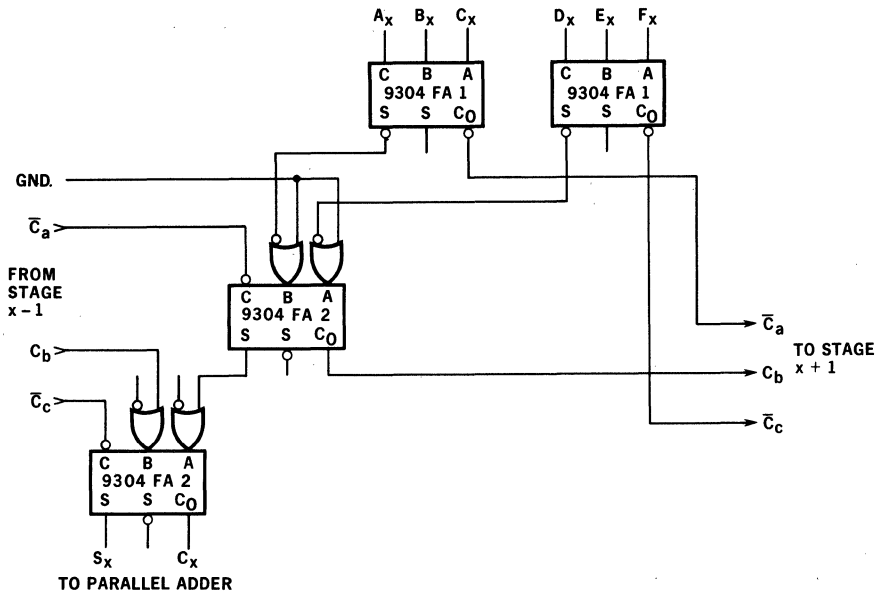


Fig. 15 — ADDITION OF SIX VARIABLES

The above design shows how the 9304 can be used in carry save arithmetic. Six input variable are reduced to two where they can be added in a parallel adder. Delay between inputs and outputs is typically 50 ns, allowing extremely high speed computation. Additional variables may be added or the concept can be extended to multiplication, division, and various other arithmetic operations.

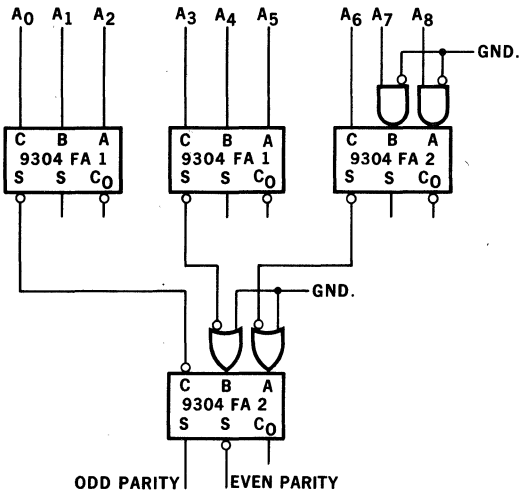


Fig. 16 — BYTE PARITY GENERATION OR CHECKING

The 9304 can be used for parity checking or generating. The above design uses 2 9304's to generate parity for an 8 bit byte or check parity over 9 bits. The delay from input to odd parity is typically 35 ns. Additional adder blocks can be used to generate or check parity over larger word lengths. The concept can also be used for hamming and cyclic code generation and checking.

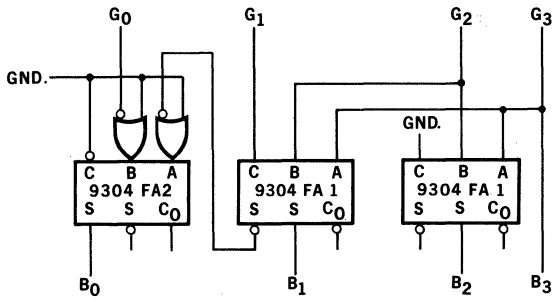


Fig. 17 — 4 BIT PARALLEL GRAY TO BINARY CONVERSION

A 4 bit parallel binary to gray conversion is shown. The adders can also be used for other cyclic code manipulations.

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9306

MSI UP/DOWN BCD COUNTER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9306 is a high speed synchronous 8421 BCD up/down decade counter. It is a synchronously presetable, multifunctional MSI building block useful in a large number of counting, digital integration, and conversion applications. Seven decades of synchronous operation are obtainable with no external gating packages required through an internal carry look-ahead counting technique.

FEATURES:

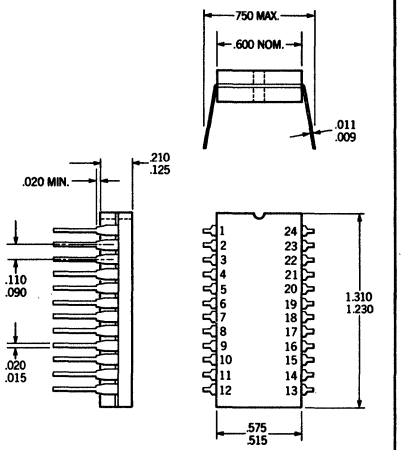
- **SYNCHRONOUS COUNTING AND PARALLEL ENTRY**
- **DECODED TERMINAL COUNT**
- **BUILT-IN CARRY/BORROW CIRCUITRY**
- **TYPICAL POWER DISSIPATION OF 350 mW**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTμL, LPDTμL, AND TTμL FAMILIES (CCSL).**
- **ALL CERAMIC HERMETIC 24 PIN DUAL IN-LINE PACKAGE**
- **INPUT DIODE CLAMPING**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

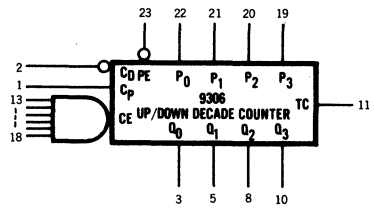
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

ORDER INFORMATION — Specify U6N9306XXX for 24-pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to 75°C temperature range.

PHYSICAL DIMENSIONS



LOGIC DIAGRAM



V_{CC} — Pin 24
Gnd — Pin 12

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

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FUNCTIONAL DESCRIPTION — A clock buffer and inverter drives the four clocked RS master-slave flip flops in parallel, so that synchronous operation is obtained. When the clock input (CP) is low, the slave is steady, but data can enter the master via the R and the S inputs. During the low to high transition of CP, first the data inputs (R and S) are inhibited, so that a later change in the input data will not affect the master; secondly, the now trapped information in the master is transferred to the slave and is reflected at the outputs. When the transfer is completed both the master and the slave are steady as long as the clock input remains high, and regardless of the logic state at any other input to the device. During the high to low transition of the clock input, first the transfer path from master to slave are inhibited, leaving the slave steady in its present state, secondly, the data inputs (R and S) are enabled so that new data can enter the master. As a result of this synchronous operation higher clock frequency is possible and much less external logic is required in most applications. Mode selection is accomplished as shown in the table below. However, several restrictions are placed on the manner of selection. First, the transition of CE from high to low or of PE from low to high may only be done when CP is high. Second, any change of CD must be done only when CP is high. The remaining transitions may be made by following the setup and release times specified under "Switching Characteristics."

MODE SELECTION SCHEME

PE	CD	CE	Mode
0	0	0	presetting
0	0	1	presetting
0	1	0	presetting
0	1	1	presetting
1	1	1	count up
1	0	1	count down
1	1	0	no change
1	0	0	no change

Note: $CE = CE_0 \cdot CE_1 \cdot CE_2 \cdot CE_3 \cdot CE_4 \cdot CE_5$

LOADING RULES
(1 U.L. = 1 TTμL input gate load)

INPUT	FAN IN
CD, CE_0, CE_1, CE_2,	1 Unit Load
CE_3, CE_4, CE_5	1 Unit Load
CP, PE	2 Unit Loads
P_0, P_1, P_2, P_3	⅔ Unit Load
OUTPUT	**FAN OUT**
Q_0, Q_1, Q_2, Q_3, TC	6 Unit Loads

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.36\ mA$
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 9.6\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 7.44\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current E_0, E_1, E_2, E_3, E_4, E_5, CD		−1.6		−1.0	−1.6		−1.6	mA	
$2\ I_F$	Input Load Current CP, PE		−3.2		−2.0	−3.2		−3.2	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$
$⅔ I_F$	Input Load Current P_0, P_1, P_2, P_3		−1.07		−.7	−1.07		−1.07	mA	
I_R	Input Leakage Current E_0, E_1, E_2, E_3, E_4, E_5, CD		60		10	60		60	μA	
$2\ I_R$	Input Leakage Current CP, PE		120		20	120		120	μA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$
$⅔ I_R$	Input Leakage Current P_0, P_1, P_2, P_3		40		7	40		40	μA	

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.36\ mA$
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 9.6\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 8.5\ mA$ Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current $E_0, E_1, E_2, E_3, E_4, E_5, CD$		−1.6		−1.0	−1.6		−1.6	mA	
$2\ I_F$	Input Load Current CP, PE		−3.2		−2.0	−3.2		−3.2	mA	$V_{CC} = 5.25\ V$ $V_F = 0.4\ V$
$⅔ I_F$	Input Load Current P_0, P_1, P_2, P_3		−1.07		−.7	−1.07		−1.07	mA	
I_R	Input Leakage Current $E_0, E_1, E_2, E_3, E_4, E_5, CD$		60		10	60		60	μA	
$2\ I_R$	Input Leakage Current CP, PE		120		20	120		120	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$
$⅔ I_R$	Input Leakage Current P_0, P_1, P_2, P_3		40		7	40		40	μA	

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+} (Q)	Turn-Off Delay		20		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig. 1)
t_{pd-} (Q)	Turn-On Delay		20		ns	
t_{pd+} (TC)	Turn-Off Delay for TC		40		ns	
t_{pd-} (TC)	Turn-On Delay for TC		30		ns	
t_s (CE)	Set-Up Time for CE		25		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig. 2)
t_r (CE)	Release Time for CE		25		ns	
t_s	Set-Up Time for Data		15		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig. 3)
t_r	Release Time for Data		15		ns	
t_s (PE)	Set-Up Time for PE		20		ns	
t_r (PE)	Release Time for PE		20		ns	

SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) to respond.

RELEASE TIME: t_r is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) not to respond.

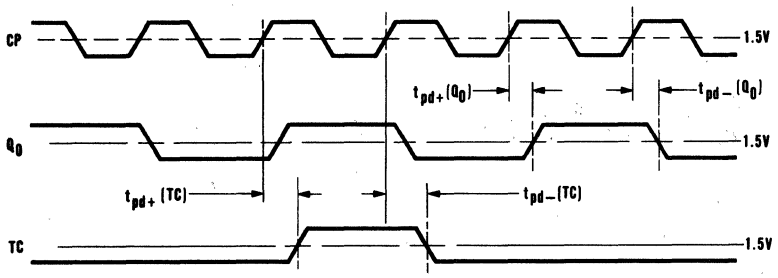


Fig. 1

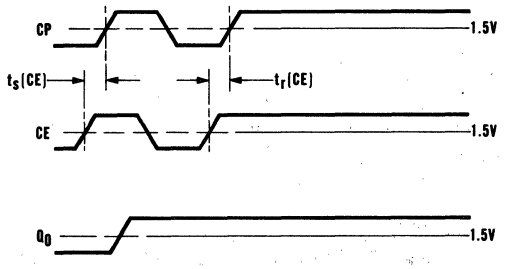


Fig. 2

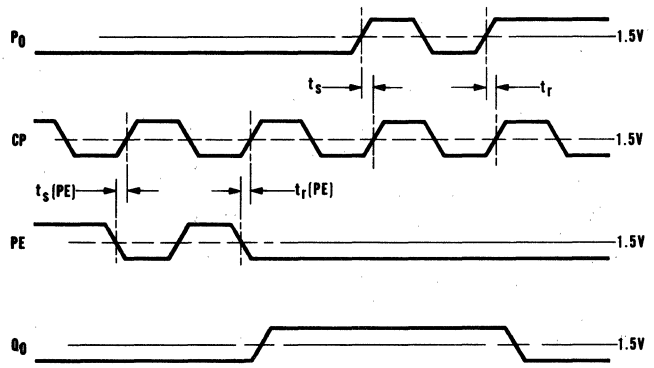


Fig. 3

APPLICATIONS

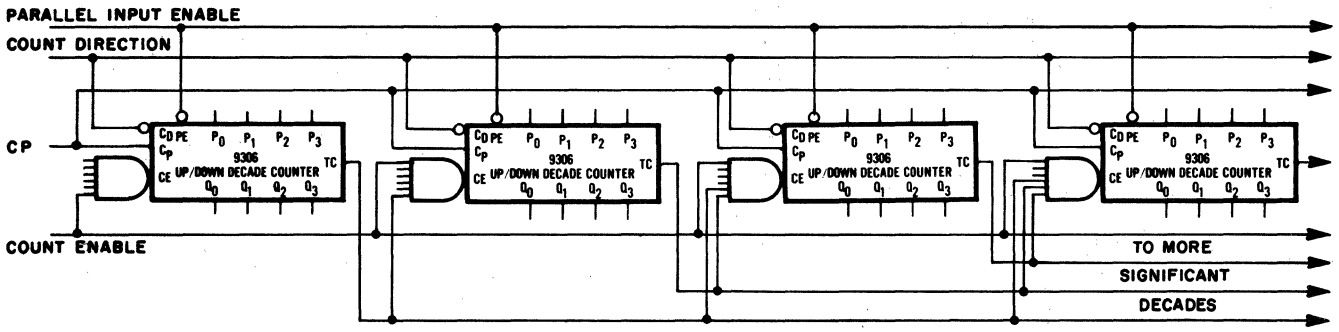


Fig. 4

9307

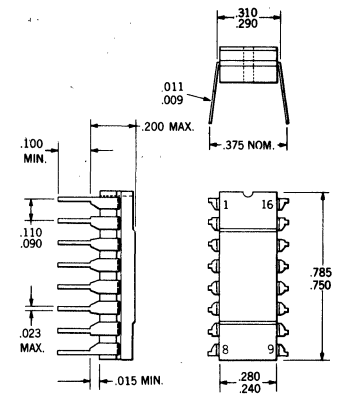
MSI SEVEN SEGMENT DECODER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9307 is a Seven Segment Decoder designed to accept four inputs in 8421 BCD code and provide the appropriate outputs to drive a seven segment numerical display. The decoder can be used with seven segment incandescent lamp, neon, electro-luminescent, or CRT numeric displays. The 9307 is compatible with all other Fairchild CCSL devices.

- **CCSL COMPATIBLE**
- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZEROES**
- **LAMP INTENSITY MODULATION CAPABILITY**
- **LAMP TEST FACILITY**
- **BLANKING INPUT**
- **ACTIVE HIGH OUTPUTS**
- **ALL CERAMIC "HERMETIC" 16 PIN DUAL IN-LINE* PACKAGE**

PHYSICAL DIMENSIONS



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

Fig. 1

LOGIC SYMBOL

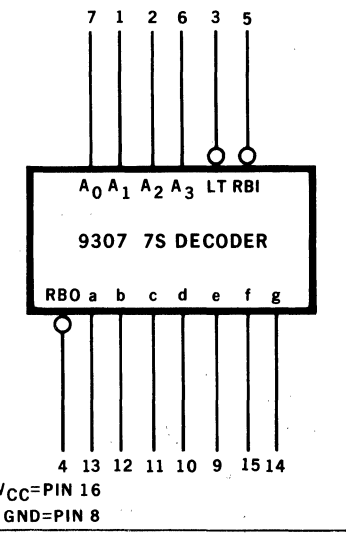


Fig. 2

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to +V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

ORDER INFORMATION

Specify U6B9307XXX for 16 pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

*Fairchild patent pending.

FAIRCHILD SEMICONDUCTOR
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313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

The 9307 seven segment decoder accepts a 4 Bit BCD 8421 code input and produces the appropriate outputs for selection of segments in a seven segment matrix display used for representing the decimal numbers 0 - 9. The seven outputs (a, b, c, d, e, f, g) of the decoder select the corresponding segments in the matrix shown in Figure 3. The numeric designations chosen to represent the decimal numbers are shown in Figure 5, together with the resulting displays for input code configurations in excess of binary nine.

The decoder has active high outputs so that a buffer transistor may be used directly to provide the high currents required for incandescent displays. If additional base drive current is required external resistors may be added from the supply voltage to the seven segment outputs of the decoders. The value of this resistor is constrained by the 10 mA current sinking capability of the output transistors of the circuit.

The device has provision for automatic blanking of the leading and/or trailing edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display, conforming to normal writing practice. In an eight digit mixed integer fraction decimal representation, using the automatic blanking capability, (0060.0300) would be displayed as (60.03). Leading edge zero suppression is obtained by connecting the Ripple Blanking Output (RBO) of a decoder to the Ripple Blanking Input (RBI) of the next lower stage device. The most significant decoder stage should have the RBI input grounded; and, since suppression of the least significant integer zero in a number is not usually desired, the RBI input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing edge zeroes.

The decoder has an active low input Lamp Test which overrides all other input combinations and enables a check to be made on possible display malfunctions. The RBO terminal of the decoder can be OR - tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of DTμL gates.

Fig. 3
SEGMENT DESIGNATION

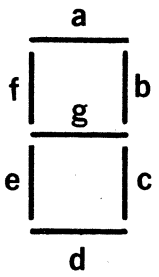


Fig. 4
TRUTH TABLE

LT	RB IN	A_0	A_1	A_2	A_3	a	b	c	d	e	f	g	RB OUT	
L	X	X	X	X	X	H	H	H	H	H	H	H	H	
H	L	L	L	L	L	L	L	L	L	L	L	L	L	0
H	H	L	L	L	L	H	H	H	H	H	H	L	H	0
|	X	H	L	L	L	L	H	H	L	L	L	L	H	1
|	|	L	H	L	L	H	H	L	H	H	L	H	H	2
|	|	H	H	L	L	H	H	H	H	L	L	H	H	3
|	|	L	L	H	L	L	H	H	L	L	H	H	H	4
|	|	H	L	H	L	H	L	H	H	L	H	H	H	5
|	|	L	H	H	L	H	L	H	H	H	H	H	H	6
|	|	H	H	H	L	H	H	H	L	L	L	L	H	7
|	|	L	L	L	H	H	H	H	H	H	H	H	H	8
|	|	H	L	L	H	H	H	H	H	L	H	H	H	9
|	|	L	H	L	H	L	L	L	H	H	L	H	H	10
|	|	H	H	L	H	L	L	L	H	L	L	H	H	11
|	|	L	L	H	H	L	H	H	L	L	H	H	H	12
|	|	H	L	H	H	H	L	H	H	L	H	H	H	13
|	|	L	H	H	H	L	L	L	H	H	H	H	H	14
H	X	H	H	H	H	L	L	L	L	L	L	L	H	15

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = EITHER HIGH OR LOW VOLTAGE LEVEL

Fig. 5
NUMERICAL DESIGNATIONS

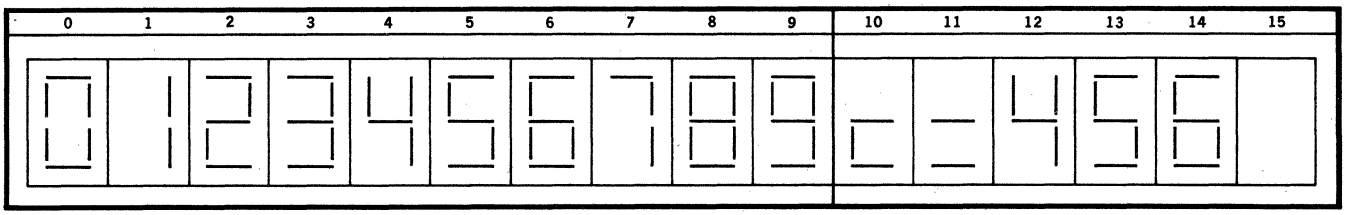


Table 1—Loading Rules (1 U.L. = 1 DTμL Gate Input Load)

Inputs	Loading (51X & 59X)	
	High State	Low State
A_0, A_1, A_2, A_3	1	1
$R_{B(IN)}$	1	½
LT	5	4.3

Outputs	Fan Out	
	51X	59X
a, b, c, d, e, f, g	8	7
$R_{B(OUT)}$	2.0	1.5

TABLE II —
ELECTRICAL CHARACTERISTICS (T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%) (Part #U6B930751X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	4.3 3.0		4.3 3.0	4.4 4.0		4.4 3.0		Volts	V_{CC} = 4.5 V I_{OH} = 0.0 mA (Pins 9-15) V_{CC} = 4.5 V I_{OH} = −70 μA (Pin 4) Inputs at threshold voltages (V_{IL} or V_{IH})
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 5.5 V I_{OL} = 12.5 mA (Pins 9-15) I_{OL} = 3.1 mA (Pin 4) V_{CC} = 4.5 V I_{OL} = 10 mA (Pins 9-15) I_{OL} = 2.4 mA (Pin 4) Inputs at threshold voltages (V_{IL} or V_{IH})
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed input low threshold for all inputs
I_F (Pin 3) I_F (Pins 1, 2, 6, 7) I_F (Pin 5)	Input Load Current Input Load Current Input Load Current		−6.4 −1.5 −0.75			−6.4 −1.5 −0.75		−6.4 −1.5 −0.75	mA	V_{CC} = 5.5 V V_F = 0.4 V V_R = 5.5 V on other inputs
I_R (Pin 3) I_R (Pins 1, 2, 5, 6, 7)	Input Leakage Current Input Leakage Current					10 2.0		25 5.0	μA	V_{CC} = 5.5 V V_R = 4.5 V Ground on other inputs
I_A (Pins 9-15)	Available Output Current	−1.4		−1.4			−1.0		mA	V_{OUT} = 0.85 V V_{CC} = 4.5 V Inputs at threshold voltages (V_{IL} or V_{IH})
I_{SC} (Pins 9-15)	Short Circuit Current					−3.7			mA	V_{OUT} = 0.0 V V_{CC} = 5.5 V
t_{pd+}	Switching Speed					500			ns	V_{CC} = 5.0 V, See Figure 6
t_{pd-}	Switching Speed					500			ns	

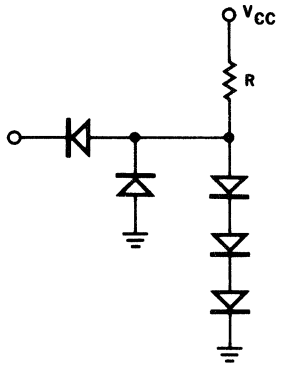
TABLE III —
ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%) (Part #U6B930759X)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	4.3 2.7		4.3 2.7	4.6 4.0		4.3 2.7		Volts	V_{CC} = 4.75 V I_{OH} = 0.0 mA (Pins 9-15) V_{CC} = 4.75 V I_{OH} = −70 μA (Pin 4) Inputs at threshold voltages (V_{IL} or V_{IH})
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 5.25 V I_{OL} = 11.5 mA (Pins 9-15) I_{OL} = 2.75 mA (Pin 4) V_{CC} = 4.75 V I_{OL} = 10 mA (Pins 9-15) I_{OL} = 2.4 mA (Pin 4) Inputs at threshold voltages (V_{IL} or V_{IH})
V_{IH}	Input High Voltage	2.0		2.0			2.0		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (Pin 3) I_F (Pins 1, 2, 6, 7) I_F (Pin 5)	Input Load Current Input Load Current Input Load Current		−6.4 −1.5 −0.75			−6.4 −1.5 −0.75		−6.4 −1.5 −0.75	mA	V_{CC} = 5.25 V V_F = 0.45 V V_R = 5.25 on other inputs
I_R (Pin 3) I_R (Pins 1, 2, 5, 6, 7)	Input Leakage Current Input Leakage Current					25 5.0		50 10	μA	V_{CC} = 5.25 V V_R = 4.5 V Ground on other inputs
I_A (Pins 9-15)	Available Output Current	−1.4		−1.4			−1.0		mA	V_{OUT} = 0.75 V V_{CC} = 4.75 V Inputs at threshold voltages (V_{IL} or V_{IH})
I_{SC} (Pins 9-15)	Short Circuit Current					−4.0			mA	V_{OUT} = 0.0 V V_{CC} = 5.5 V
t_{pd+}	Switching Speed					500			ns	V_{CC} = 5.0 V, See Figure 6
t_{pd-}	Switching Speed					500			ns	

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

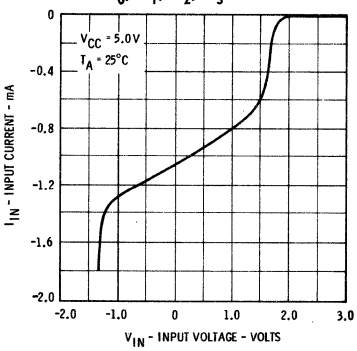
INPUTS

Equivalent Circuit

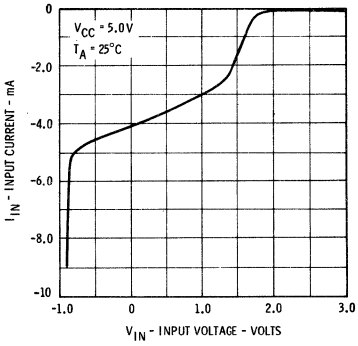


INPUT CURRENT VERSUS INPUT VOLTAGE

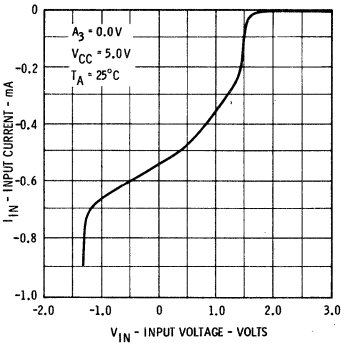
A_0, A_1, A_2, A_3 INPUTS



LT INPUT



$RB_{(IN)}$ INPUT

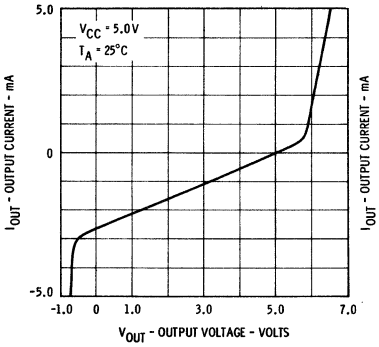


OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

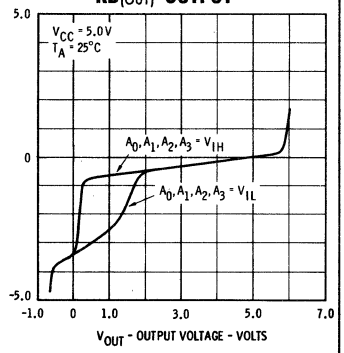
U6B930751X (−55°C to +125°C)

OUTPUT IN HIGH STATE

a, b, c, d, e, f, g OUTPUTS

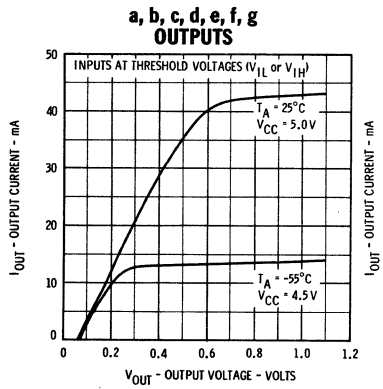


$RB_{(OUT)}$ OUTPUT

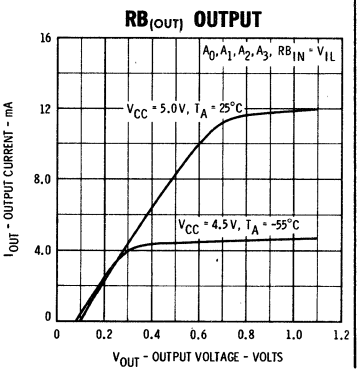


OUTPUT IN LOW STATE

a, b, c, d, e, f, g OUTPUTS



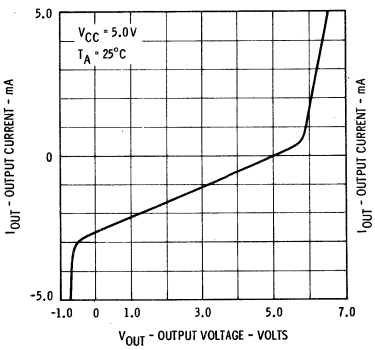
$RB_{(OUT)}$ OUTPUT



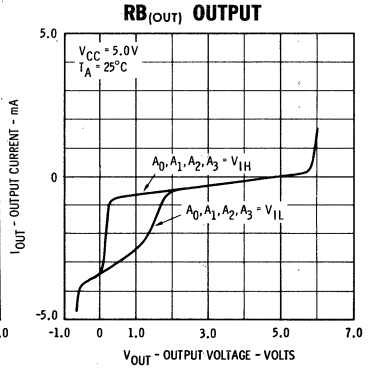
U6B930759X (0°C to +75°C)

OUTPUT IN HIGH STATE

a, b, c, d, e, f, g OUTPUTS

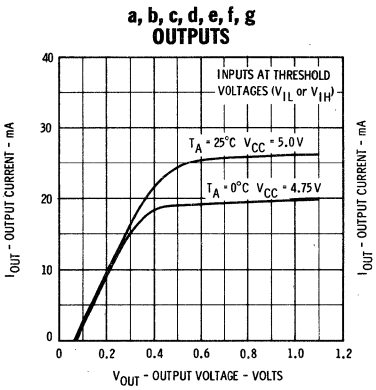


$RB_{(OUT)}$ OUTPUT

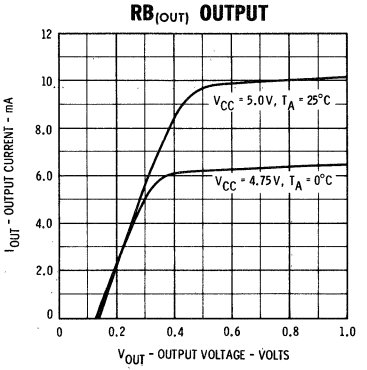


OUTPUT IN LOW STATE

a, b, c, d, e, f, g OUTPUTS



$RB_{(OUT)}$ OUTPUT



OUTPUTS

Equivalent Circuit

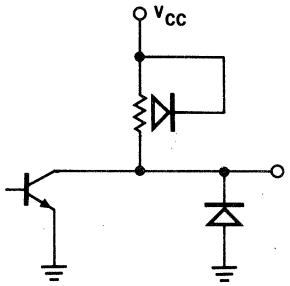
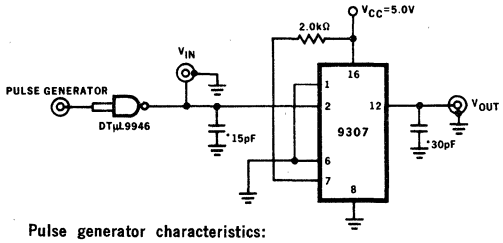
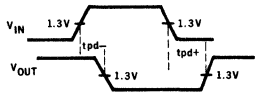


Fig. 6—SWITCHING CIRCUIT AND WAVEFORMS



Pulse generator characteristics:
Amptitude = 3.0 V
Freq. = 500 kHz
Pulse width = 1000 ns
$t_r = t_f \leq 15$ ns
*Includes probe and jig capacitance



APPLICATIONS

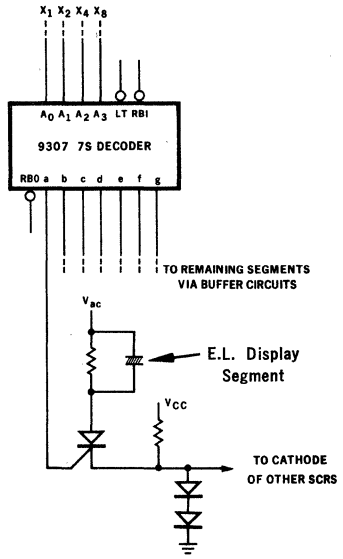


Fig. 7
9307 Seven Segment Decoder driving Electro-Luminescent Display.

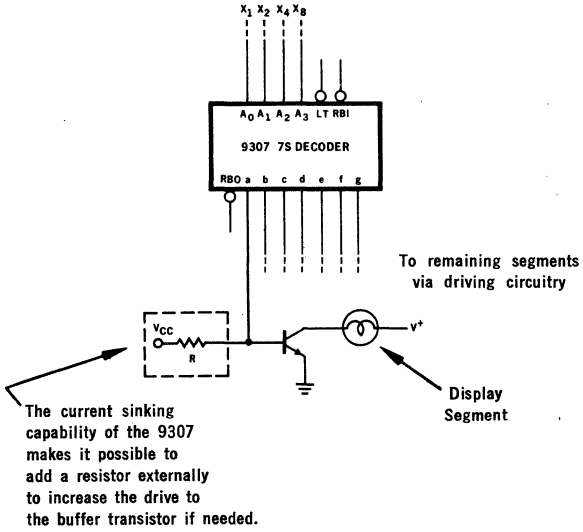


Fig. 8
9307 Seven Segment Decoder driving Incandescent lamp Display.

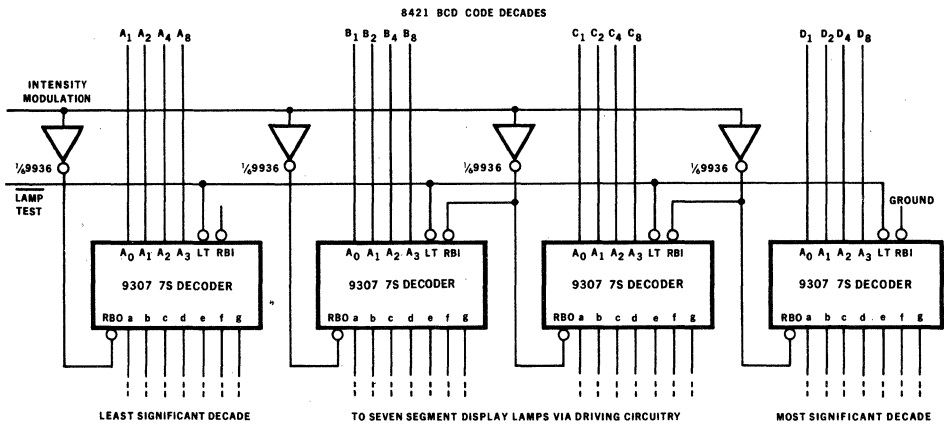


Fig. 9—FOUR DECADE SEVEN SEGMENT INTEGER DISPLAY SCHEME

This scheme incorporates automatic blanking of leading edge zeroes and intensity modulation using an external variable duty cycle signal.

9308

MSI DUAL FOUR-BIT LATCH

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The MSI 9308 is a Dual 4-Bit Latch designed for general purpose storage applications in high speed digital systems. The 9308 uses TTμL technology and is CCSL compatible. All inputs incorporate diode clamps to ground to reduce negative line transients. All outputs have active pull-up circuitry to provide high capacitive drive and low impedance outputs in both logic states to provide good A.C. noise immunity.

FEATURES

- **ACTIVE LEVEL LOW ENABLE GATE INPUTS**
- **OVERRIDING MASTER RESET**
- **25 ns THROUGH DELAY**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE DIRECT INTERFACING WITH FAIRCHILD DTμL, LPDTμL, TTμL, AND MSI FAMILIES (CCSL).**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS.**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Input Voltage (D.C.) (See Note 1)	−0.5 V to +5.5 V
Input Current (D.C.) (See Note 1)	−30 mA to +5 mA
Voltage Applied to Outputs (Output High)	−0.5 V to +V_{CC} value
Output Current (D.C.) (Output Low)	+30 mA

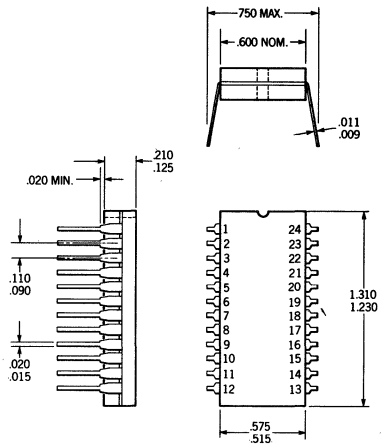
NOTE 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

DESCRIPTION OF LATCH OPERATION — Data can be entered into the latch when both of the enable inputs are low. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs goes high, the data present in the latch at that time is held in the latch and is no longer affected by the data input.

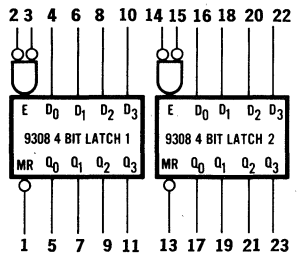
The master reset overrides all other input conditions and forces the outputs of all the latches low when a low signal is applied to the master reset input.

ORDER INFORMATION — Specify U6N9308XXX for 24-pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

PHYSICAL DIMENSIONS



LOGIC DIAGRAM



V_{CC} = Pin 24
Gnd = Pin 12

Electrical Characteristics on Page 2.

FAIRCHILD SEMICONDUCTOR
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TABLE I —
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$, See Note 1) (Part #U6N930851X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.8		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.6\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 14.4\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 11.2\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current E_0, E_I and MR Inputs		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
$1.5\ I_F$	Input Load Current D Inputs		−2.7		−1.9	−2.7		−2.7		$V_F = 0.0\ V$ (See Note 3)
I_R	Input Leakage Current E_0, E_I and MR Inputs				10	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
$1.5\ I_R$	Input Leakage Current D Inputs				15	90		90		
I_{PD}	Power Supply Current		90		65	90		90	mA	$V_{CC} = 5.0\ V$ all outputs low inputs disabled

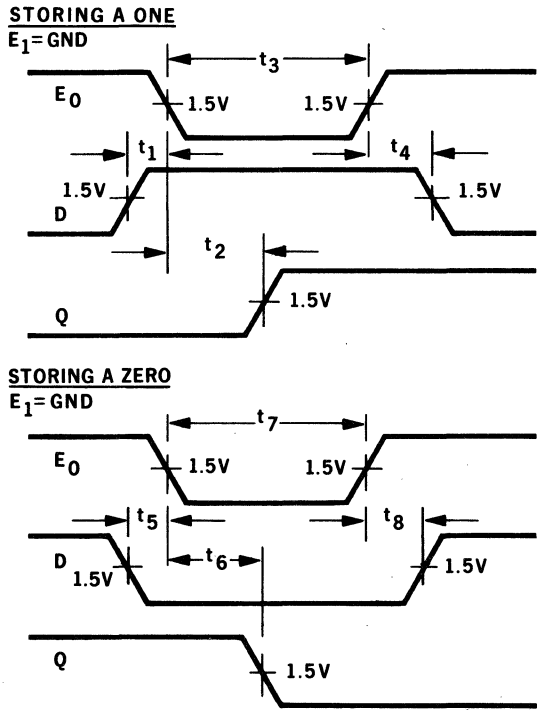
TABLE II —
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$, See Note 1) (Part #U6N930859X)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.1		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OUT} = -0.6\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OUT} = 14.4\ mA$ $V_{CC} = 4.75\ V$, $I_{OUT} = 12.7\ mA$ Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current E_0, E_I and MR Inputs		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$
$1.5\ I_F$	Input Load Current D Inputs		−2.7		−1.8	−2.6		−2.7		$V_F = 0.0\ V$ (See Note 3)
I_R	Input Leakage Current E_0, E_I and MR Inputs				10	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
$1.5\ I_R$	Input Leakage Current D Inputs				15	90		90		
I_{PD}	Power Supply Current		117		65	117		117	mA	$V_{CC} = 5.0\ V$ all outputs low inputs disabled

NOTE 1: Units are pulse tested.
NOTE 2: Output Voltages are guaranteed for either the input enabled or input disabled case.
NOTE 3: This current is measured at $V_{IN} = 0.0\ V$ to insure that no current is being absorbed by the device internally. The maximum value given guarantees that the maximum instantaneous current that can flow out of the input at $V_{IN} = 0.4\ V$ is 2.4 mA.

A.C. CHARACTERISTICS

9308 SWITCHING WAVEFORMS



TIME	DEFINITION	LIMIT (See Note 4) MIN.	TYP.	MAX.	UNITS
t_1	Min. time that data must be present before enable to not increase t_2	X	minus 4	—	ns
t_2	Delay from enable to output turning off	—	22	X	ns
t_3	Min. enable pulse width to store a ONE	X	15	—	ns
t_4	Min. time that data must remain constant after removal of enable	X	5	—	ns
t_5	Min. time that data must be present before the enable to not increase t_6	X	0	—	ns
t_6	Delay from enable to output turning on	—	15	X	ns
t_7	Min. enable pulse width to store a ZERO	X	15	—	ns
t_8	Min. time that data must remain constant after removal of enable	X	2	—	ns

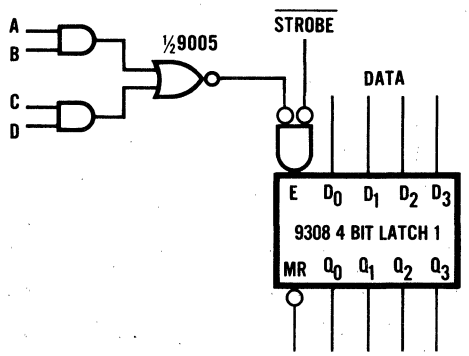
NOTE 4: Limits indicated by X will be shown on final data sheets.

All delays are measured with $V_{CC} = 5.0$ V applied to Pin 24 and Pin 12 grounded. The active input is driven by a 9002 TTμL gate with the output loaded with 15 pF. All outputs are loaded with 15 pF.

LOADING RULES

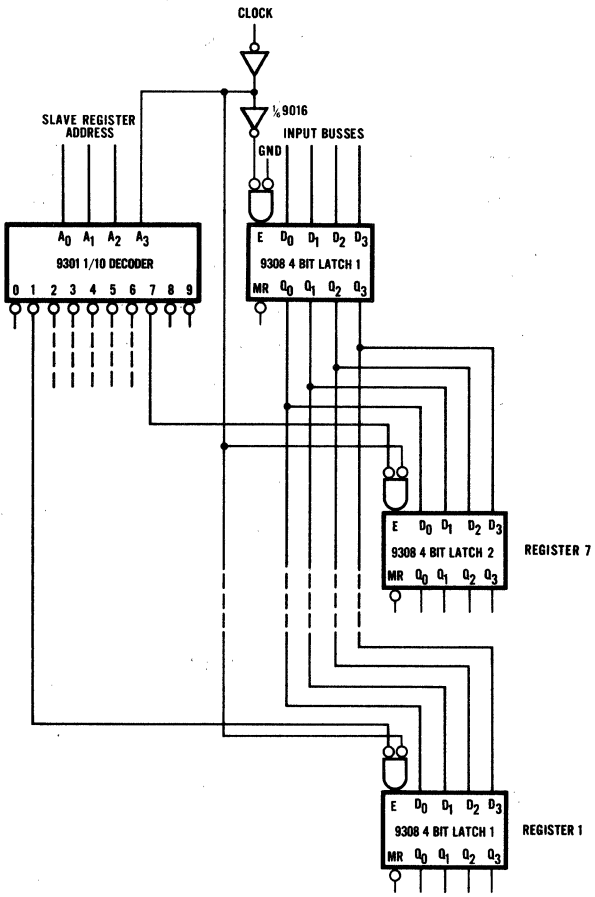
	PIN	LOADING
INPUTS	D_0, D_1, D_2, D_3	1.5
	MR, E_0, E_1	1.0
OUTPUTS	Q_0, Q_1, Q_2, Q_3	9.0

APPLICATIONS

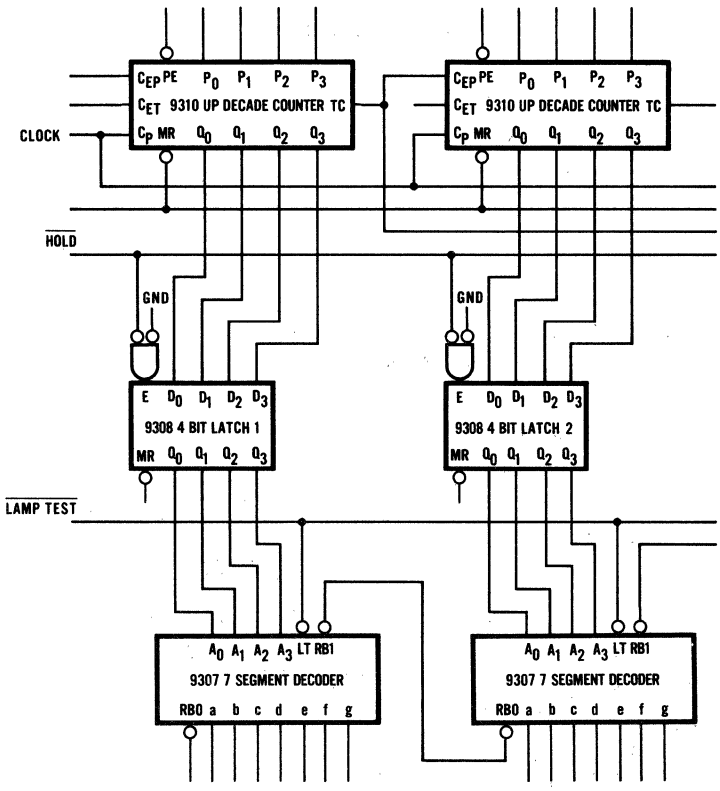


AND-OR ENABLE SHOWING ACTIVE LEVEL
LOW ENABLE GATE UTILITY

SINGLE MASTER/MULTIPLE SLAVE FLIP-FLOP



9308 AS A HOLDING REGISTER IN COUNTING AND DISPLAY APPLICATIONS



9309

MSI DUAL FOUR-INPUT MULTIPLEXER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9309 is a monolithic, high speed, dual four-input digital multiplexer circuit, constructed with the Fairchild Planar* epitaxial process. It consists of two multiplexing circuits with common input select logic, each circuit contains four inputs and fully buffered complementary outputs. In addition to operating as a multiplexer, the 9309 can generate any two function of three variables. Active pullups in the outputs ensure high drive and high speed performance. Because of its high speed performance and on-chip select decoding, the 9309 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output buss. The circuit uses TTμL for high speed, high fanout operation and is compatible with all other members of the CCSL family of digital integrated circuits.

FEATURES

- **MULTIFUNCTION CAPABILITY**
- **25 ns THROUGH DELAY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED COMPLEMENTARY OUTPUTS**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTμL, LPDTμL, TTμL, AND MSI FAMILIES (CCSL).**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS.**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Output when output is high	0 V to +V_{CC} value
Input Voltage (DC) (See Note 1)	−0.5 V to +5.5 V
Input Current (DC) (See Note 1)	−30 mA to +5 mA
Current into Output when output is low	+30 mA

Note 1—either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

ORDER INFORMATION — Specify U6B9309XXX for 16-pin Dual In-Line package or U3L9309XXX for 16-pin Flatpak, where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

LOGIC DIAGRAM

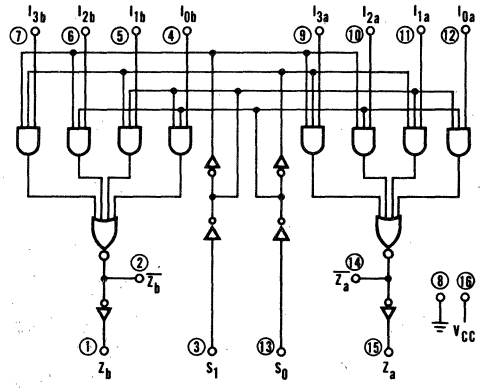
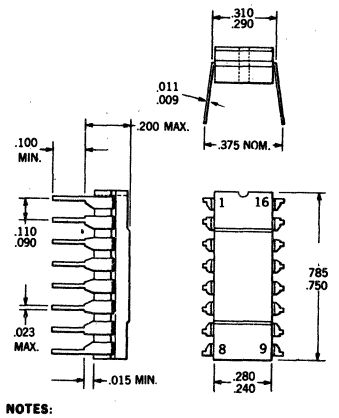


Fig. 4

9309
Dual four input multiplexer
Logic diagram

DUAL IN-LINE PACKAGE



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.

Fig. 1

FLAT PACKAGE

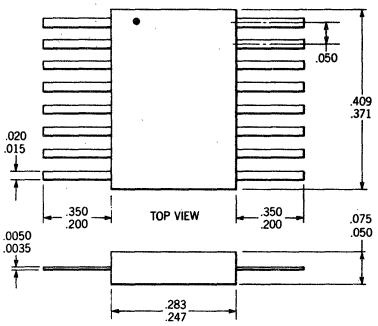
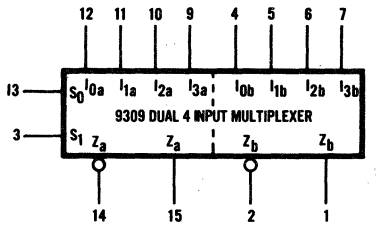


Fig. 2

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

Fig. 3

*Planar is a patented Fairchild process.

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FUNCTIONAL DESCRIPTION

The 9309 dual four input multiplexer is a member of the Fairchild family of compatible Medium Scale Integrated (MSI) digital building blocks. It provides this family with the ability to select two bits of either data or control from up to four sources, in one package.

The 9309 dual four input multiplexer is the logical implementation of a two-pole four-position switch, with the position of the switch being set by the logic levels supplied to the two select inputs. Both assertion and negation outputs are provided for both multiplexers. The logic equations for the outputs are shown below:

$$Z_a = I_{0a} \cdot S_1 \cdot S_0 + I_{1a} \cdot S_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot S_0 + I_{3a} \cdot S_1 \cdot S_0$$

$$Z_b = I_{0b} \cdot S_1 \cdot S_0 + I_{1b} \cdot S_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot S_0 + I_{3b} \cdot S_1 \cdot S_0$$

A common use of the 9309 would be the moving of data from a group of registers to a common output buss. The particular register from which the data came would be determined by the state of the select inputs.

TRUTH TABLE

SELECT INPUTS		INPUTS				OUTPUTS	
S_0	S_1	I_{0a}	I_{1a}	I_{2a}	I_{3a}	Z_a	Z_a
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L
S_0	S_1	I_{0b}	I_{1b}	I_{2b}	I_{3b}	Z_b	Z_b
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

L = low voltage level
H = high voltage level
X = either high or low logic level

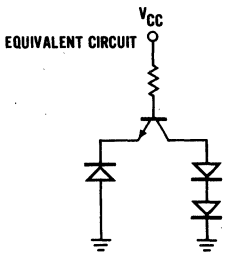
LOADING RULES

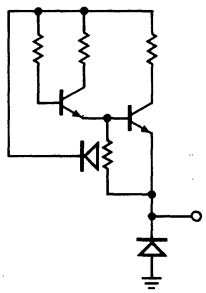
(1 U.L. = 1 TTμL gate input load)

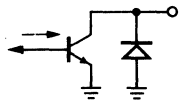
INPUTS	LOADING
I_{0a}, I_{1a}, I_{2a}, I_{3a}, I_{0b}, I_{1b}, I_{2b}, I_{3b}, S_0, S_1	1 U.L.

	FANOUT AT LOGIC LEVEL	
OUTPUTS	HIGH	LOW
Z_a, Z_b	20 U.L.	10 U.L.
Z_a, Z_b	18 U.L.	9 U.L.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS







INPUT CURRENT VERSUS INPUT VOLTAGE

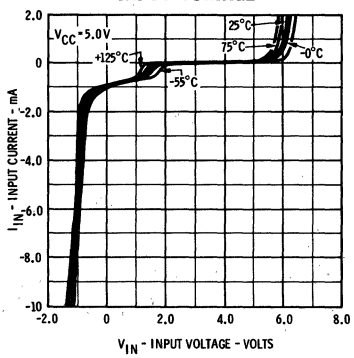


Fig. 5

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

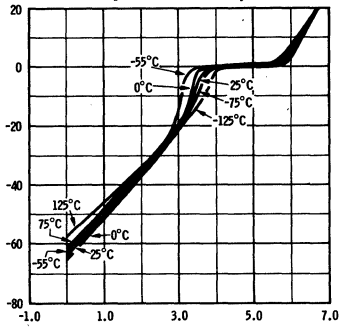


Fig. 6

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

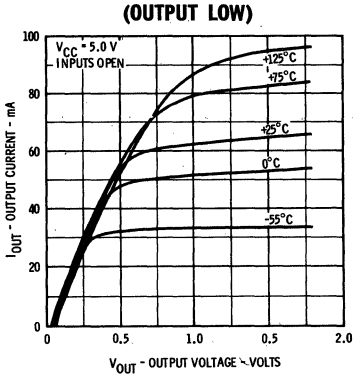


Fig. 7

ELECTRICAL CHARACTERISTICS* ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part No. UXX930951X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$ $I_{OH} = -1.2$ mA (Pins 1 & 15) $V_{CC} = 4.5\ V$ $I_{OH} = -1.08$ mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 16.0$ mA (Pins 1 & 15) $I_{OL} = 14.4$ mA (Pins 2 & 14) $V_{CC} = 4.5\ V$ $I_{OL} = 12.4$ mA (Pins 1 & 15) $I_{OL} = 11.2$ mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ Input selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current		40		30	40		40	mA	$V_{CC} = 5.0\ V$ All inputs high
t_{pd+} (S_0 to Z_a)	Switching Speed				24	32			ns	$V_{CC} = 5.0\ V$, $C_L = 15$ pF, See Figure 5
t_{pd-} (S_0 to Z_a)	Switching Speed				24	32			ns	

*Pulse tested

ELECTRICAL CHARACTERISTICS* ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) (Part No. UXX930959X)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$ $I_{OH} = -1.2$ mA (Pins 1 & 15) $V_{CC} = 4.75\ V$ $I_{OH} = -1.08$ mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$ $I_{OL} = 16.0$ mA (Pins 1 & 15) $I_{OL} = 14.4$ mA (Pins 2 & 14) $V_{CC} = 4.75\ V$ $I_{OL} = 14.1$ mA (Pins 1 & 15) $I_{OL} = 12.7$ mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$ $V_F = 0.45\ V$ Input selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current		43		30	43		43	mA	$V_{CC} = 5.0\ V$ All inputs high
t_{pd+} (S_0 to Z_a)	Switching Speed				24	32			ns	$V_{CC} = 5.0\ V$, $C_L = 15$ pF, See Figure 5
t_{pd-} (S_0 to Z_a)	Switching Speed				24	32			ns	

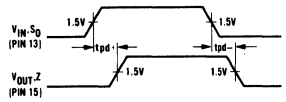
*Pulse tested

SWITCHING WAVEFORMS

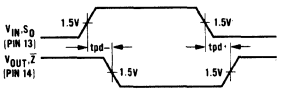
All input waveforms are output of TTμL 9000 series gates loaded with 15 pF. All outputs are loaded with the same capacitance (referred to as C_L) and only with capacitance.

Fig. 8 — WAVEFORMS

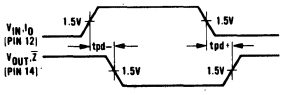
t_{pd}; S_0 to Z_a
CONDITIONS
Pins 3, 12 = GND.
Pin 11 = V_{CC}



t_{pd}; S_0 to Z_a
CONDITIONS
Pins 3, 12 = GND.
Pin 11 = V_{CC}



t_{pd}; I_{a0} to Z_a
CONDITIONS
Pins 3, 13 = GND.



SWITCHING CHARACTERISTICS

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to Z_a)

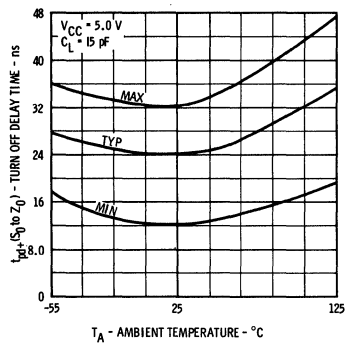


Fig. 9

TURN ON DELAY TIME VERSUS TEMPERATURE (S_0 to Z_a)

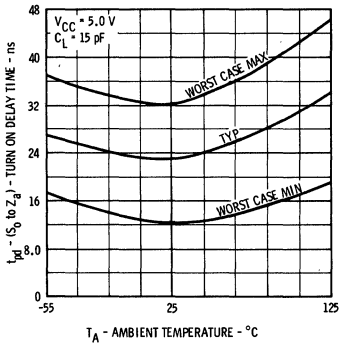


Fig. 10

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{0a} to Z_a)

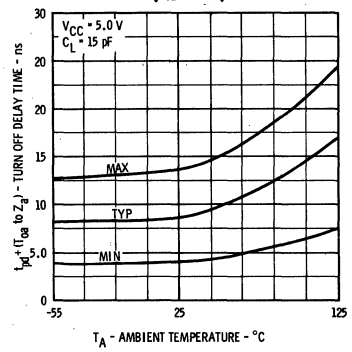


Fig. 11

TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{0a} to Z_a)

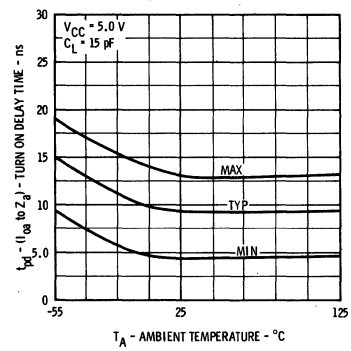


Fig. 12

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to Z_a)

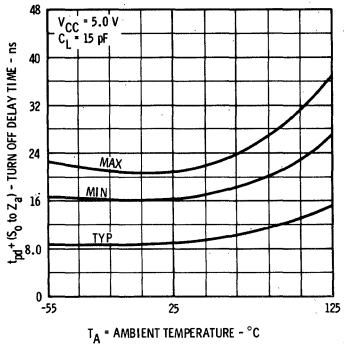


Fig. 13

TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to Z_a)

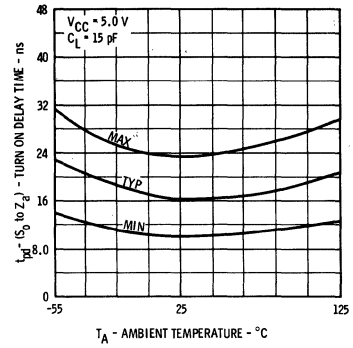


Fig. 14

APPLICATIONS

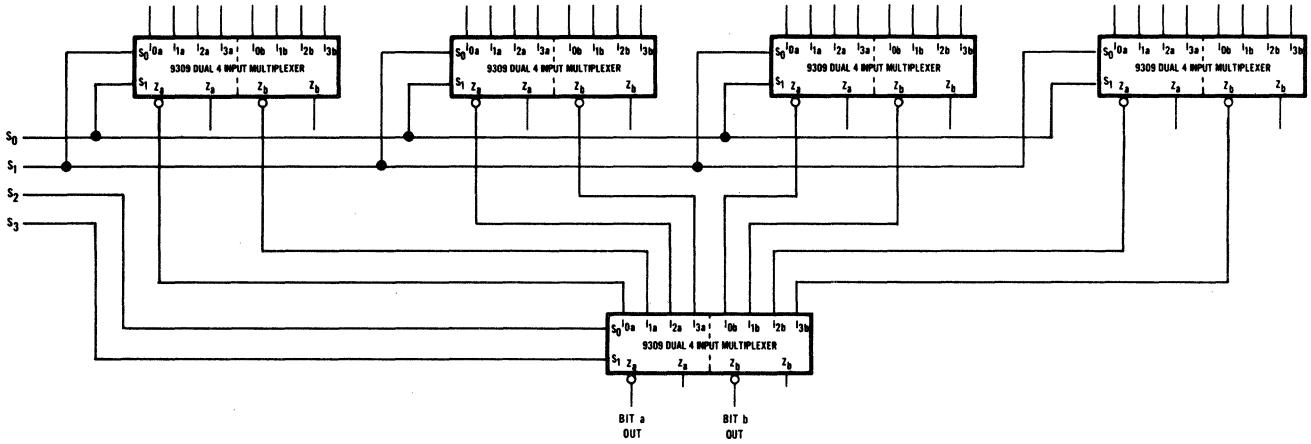


Fig. 12 — MULTIPLEXING TWO BITS FROM SIXTEEN SOURCES

This diagram shows the interconnection of five 9309 dual four bit multiplexers to provide switching of two bits of data from one of sixteen words onto a two bit data buss. The selection of which word will be transferred to the buss is made by the address supplied to the S_0, S_1, S_2 and S_3 inputs. As an example: if twelve bit words are to be transferred to a twelve bit buss, the above diagram would be repeated six times. Notice that the negative outputs are used at both levels resulting in the assertion output (negation of the negation) at a higher speed due to the fact that the through delay is less on the negation output.

If the word selecting address is held in four TTμL flip flops (two dual packages) enough load capability is available to select between sixteen, sixteen bit words.

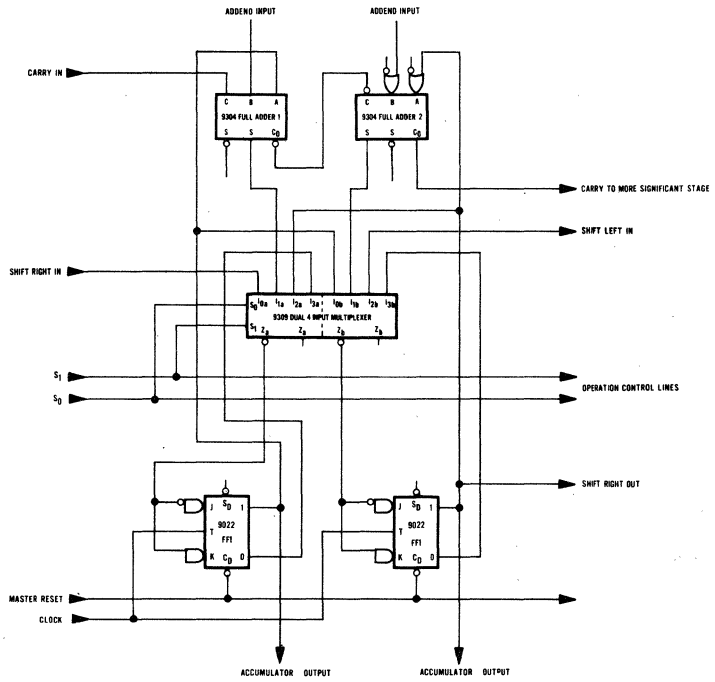


Fig. 13 — GENERAL PURPOSE ACCUMULATOR

A fast, general purpose accumulator for computer applications is capable of: 1) shift left; 2) add; 3) shift right and 4) complement operations. Only three packages are required to construct two stages of the general purpose accumulator (Figure 1).

The D input capability of the 9022 is utilized here to allow each flip flop of the accumulator to accept the data as presented by the 9309 multiplexer. Under the operation code instructions the multiplexer provides an input to the 9022 from: 1) adjacent stage to the right for a shift left operation; 2) adjacent stage to the left for a shift right operation; 3) output of adders for add operation and 4) Q outputs of 9022 for the complement operation. The operation code at the right of Figure 1 shows the instruction codes to perform the various operations.

The accumulator should be capable of 20 to 25 MHz operation.

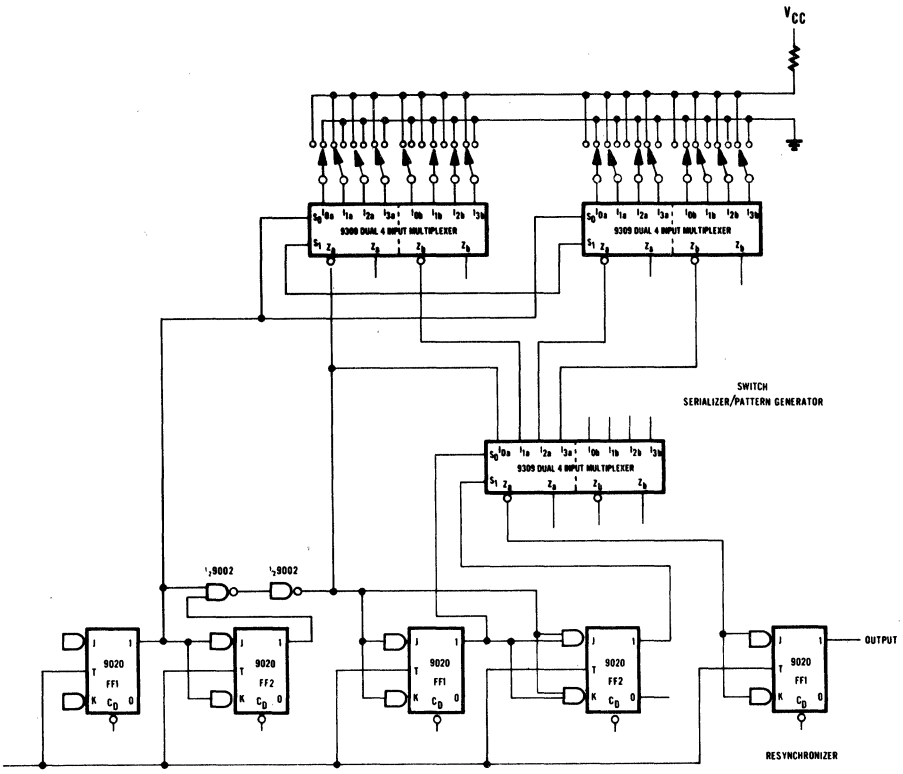
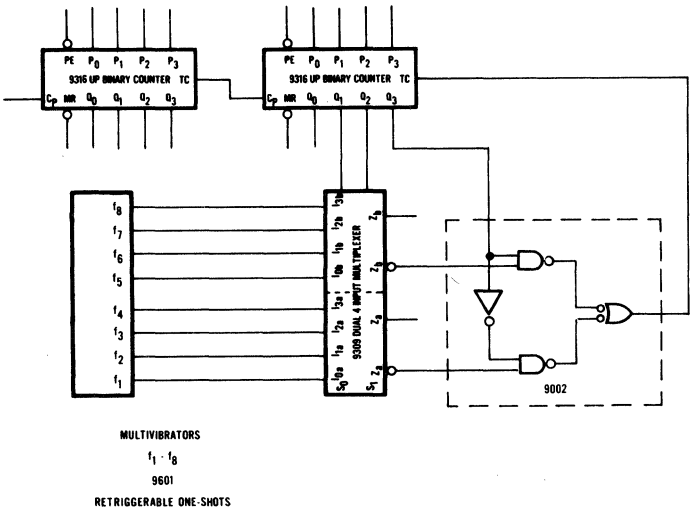


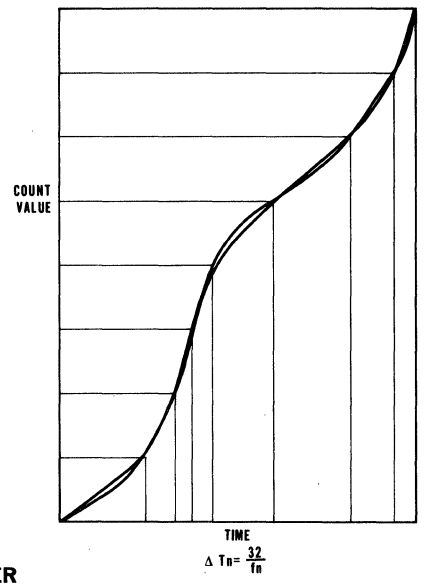
Fig. 14 — 16-BIT PATTERN GENERATOR

This application illustrates the use of 9309 and 9020 in the design of one channel of a 16 bit pattern generator. Each channel requires ½ 9020, ½ 9002 and 2½ 9309. Each channel consists of a switch serializer/pattern generator and resynchronizer sections with a modulo 16 binary counter common to all channels.

The two least significant bits and two most significant bits of the counter control the first and second stages of multiplexing respectively. In this manner four bits are multiplexed on each of the four lines from the first stage to the second stage. Every four clock times a new input line containing four multiplexed bits is selected by the second stage of the serializer thus serializing the 16 input bits from the switches.

The resynchronizer flip flop is used to eliminate decoding spikes.





OPERATION CODE LIST

S_0	S_1	INSTRUCTION
0	0	SHIFT LEFT
1	0	ADD
0	1	SHIFT RIGHT
1	1	COMPLEMENT

H = "1", L = "0"

Fig. 15 — NON-LINEAR COUNTER

The rate of the non-linear counter depends on the multivibrator clock frequency selected under control of the three most significant bits of the counter. This makes the count rate a function of both the count value of counter and frequency of clock multivibrator selected.

Clock multiplexing is accomplished by a 9309 dual 4-input multiplexer and one 9002 quad gate. Eight line segments representing clock rates of the multivibrators may be adjusted in slope to approximate a non-linear function.

9312

MSI EIGHT-INPUT MULTIPLEXER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9312 is a monolithic, high speed, eight input digital multiplexer circuit. It provides in one package the ability to select one bit of data from up to eight sources. The 9312 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided. TTμL circuitry with active pullups on the outputs provides high speed, high fanout operation and is compatible with all other members of the CCSL family of digital integrated circuits.

FEATURES

- **MULTIFUNCTION CAPABILITY**
- **25 ns THROUGH DELAY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED COMPLEMENTARY OUTPUTS**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTμL, LPDTμL, TTμL, AND MSI FAMILIES (CCSL).**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS.**

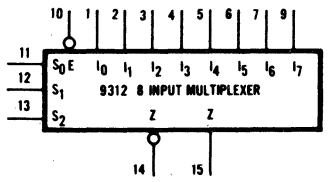
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage applied to output when output is high	0 V to +V_{CC} value
Input Voltage (DC) (See Note 1)	−0.5 V to +5.5 V
Input Current (DC) (See Note 1)	−30 mA to +5 mA
Current into output when output is low	+30 mA

Note 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

ORDER INFORMATION — Specify U6B9312XXX for 16-pin Dual In-Line package or U3L9312XXX for 16-pin Flatpak, where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

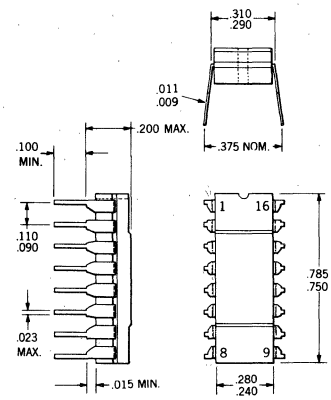
LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

Fig. 1

DUAL IN-LINE PACKAGE



NOTE :
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.

Fig. 2

FLAT PACKAGE

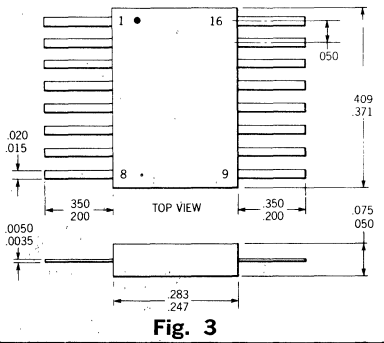


Fig. 3

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FUNCTIONAL DESCRIPTION — The 9312 is a logical implementation of a single pole - 8 position switch with the switch position controlled by the state of three select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The enable input (E) is active low. When it is not activated the negation output is high and the assertion output is low regardless of all other inputs. The logic function provided at the output is:

$$Z = E \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

The 9312 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the 9312 can provide any logic function of four variables and its negation. Thus any number of random topic elements used to generate unusual truth tables can be replaced by one 9312.

TRUTH TABLE

E	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = High voltage level
L = Low voltage level
X = Level does not affect output

Fig. 5

LOADING RULES

INPUTS	LOADING
All Inputs	1 U.L.

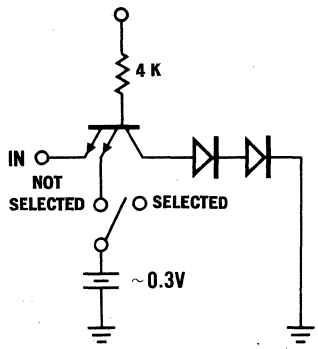
OUTPUTS	FAN-OUT	
	High State	Low State
$\overline{Z}$	18	9
Z	20	10

Fig. 4

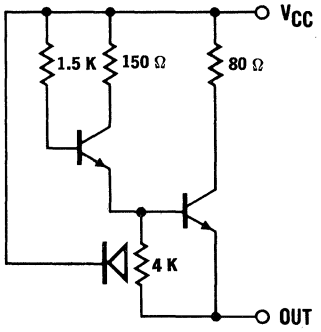
1 U.L. = 1 TTμL Unit Load
1 U.L. is defined by the entries I_R and I_F in the table on page 3.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

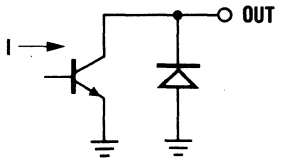
EQUIVALENT INPUT CIRCUIT



OUTPUT HIGH EQUIVALENT CIRCUIT



OUTPUT LOW EQUIVALENT CIRCUIT



INPUT CURRENT VERSUS INPUT VOLTAGE

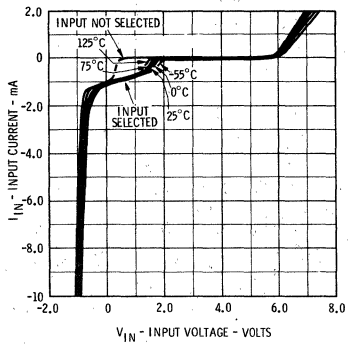


Fig. 6

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

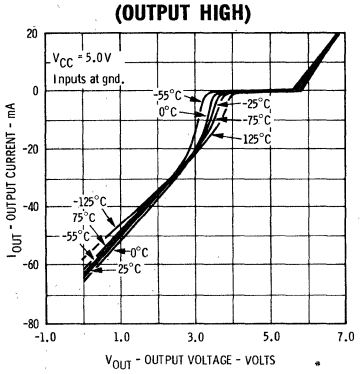


Fig. 7

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

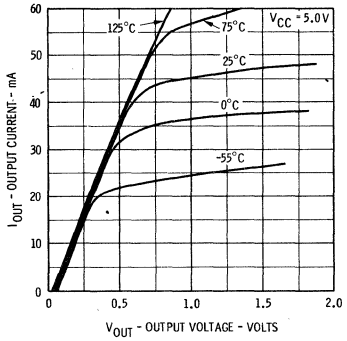


Fig. 8

ELECTRICAL CHARACTERISTICS* ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part No. UXX931251X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$ $I_{OH} = -1.2\ mA$ (Pin 15) $V_{CC} = 4.5\ V$ $I_{OH} = -1.08\ mA$ (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 16.0\ mA$ (Pin 15) $I_{OL} = 14.4\ mA$ (Pin 14) $V_{CC} = 4.5\ V$ $I_{OL} = 12.4\ mA$ (Pin 15) $I_{OL} = 11.2\ mA$ (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$
			−1.24		−0.85	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$ Input Selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current		40		27	40		40	mA	$V_{CC} = 5.0\ V$
t_{pd+} (S_0 to Z)	Switching Speed				23	34			ns	$V_{CC} = 5.0\ V$, See Page 4
t_{pd-} (S_0 to Z)	Switching Speed				25	36			ns	$C_L = 15\ pF$

***Pulse tested**

ELECTRICAL CHARACTERISTICS* ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) (Part No. UXX931259X)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$ $I_{OH} = -1.2\ mA$ (Pin 15) $V_{CC} = 4.75\ V$ $I_{OH} = -1.08\ mA$ (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$ $I_{OL} = 16.0\ mA$ (Pin 15) $I_{OL} = 14.4\ mA$ (Pin 14) $V_{CC} = 4.75\ V$ $I_{OL} = 14.1\ mA$ (Pin 15) $I_{OL} = 12.7\ mA$ (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$ $V_F = 0.45\ V$
			−1.41		−0.91	−1.41		−1.41	mA	$V_{CC} = 4.75\ V$ Input Selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current		43		27	43		43	mA	$V_{CC} = 5.0\ V$
t_{pd+} (S_0 to Z)	Switching Speed				23	34			ns	$V_{CC} = 5.0\ V$, See Page 4
t_{pd-} (S_0 to Z)	Switching Speed				25	36			ns	$C_L = 15\ pF$

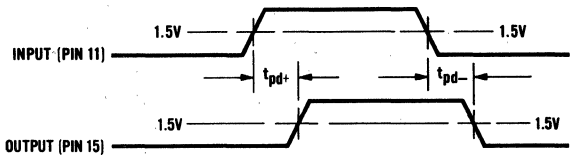
***Pulse tested**

A. C. CHARACTERISTICS

A.C. CHARACTERISTICS

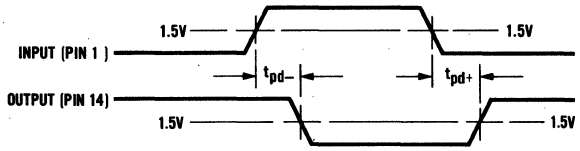
All measurements are made with $V_{CC} = 5.0$ V applied to pin 16 and with pin 8 grounded. The active input is driven by a 9002 TTμL gate with the output loaded with 15 pF. Both outputs of the 9312 are loaded with 15 pF.

t_{pd}: S_0 to Z



Other Conditions: Pins 1, 8, 10, 12, 13 = Gnd
Pin 2 = Vcc through 1.0 kΩ
Pin 16 = Vcc

t_{pd}: I_0 to $\overline{Z}$



Other Conditions: Pins 8, 10, 11, 12, 13 = Gnd
Pin 16 = Vcc

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; S_0 to Z

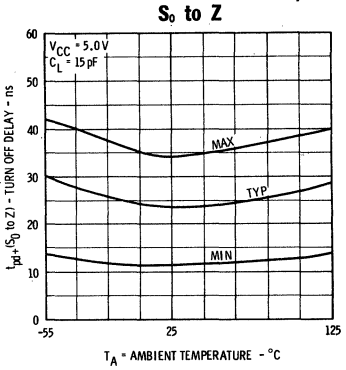


Fig. 9

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; S_0 to Z

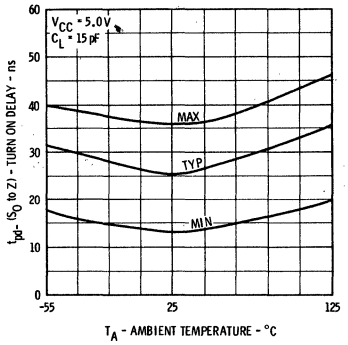


Fig. 10

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; I_0 to Z

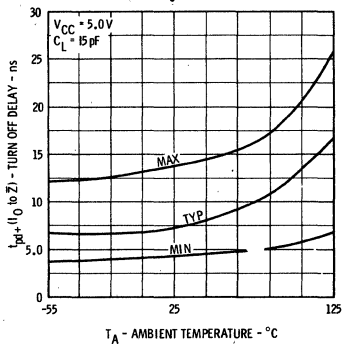


Fig. 11

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; I_0 to Z

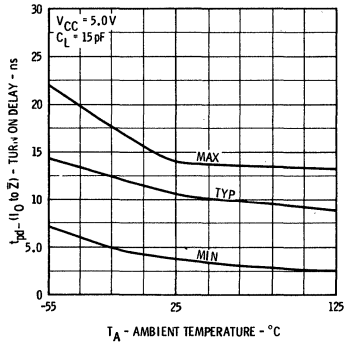
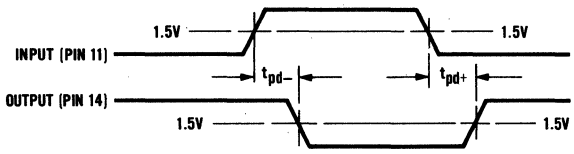


Fig. 12

t_{pd}: S_0 to $\overline{Z}$



Other Conditions: Pins 1, 8, 10, 12, 13 = Gnd
Pin 2 = Vcc through 1.0 kΩ
Pin 16 = Vcc

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; S_0 to $\overline{Z}$

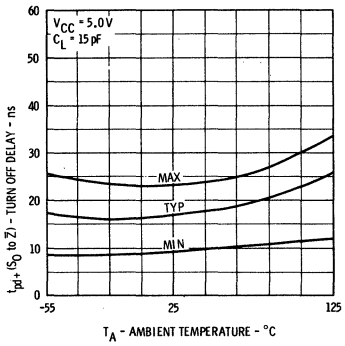


Fig. 13

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; S_0 to $\overline{Z}$

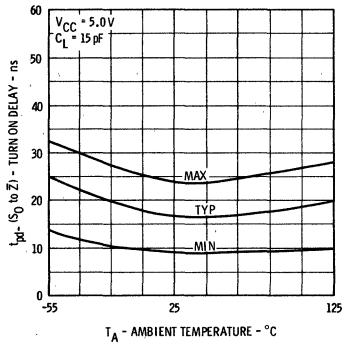
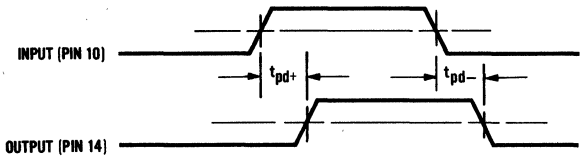


Fig. 14

t_{pd}: E to $\overline{Z}$



Other Conditions: Pins 8, 11, 12, 13 = Gnd
Pin 1 = Vcc through 2.0 kΩ
Pin 16 = Vcc

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; E to $\overline{Z}$

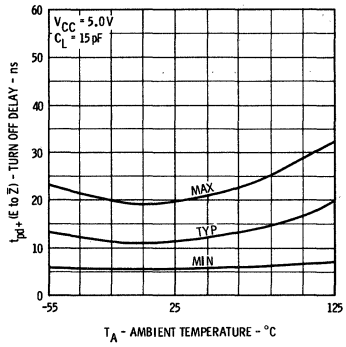


Fig. 15

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; E to $\overline{Z}$

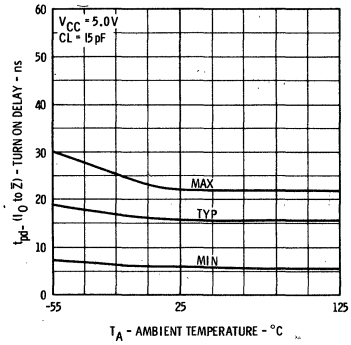


Fig. 16

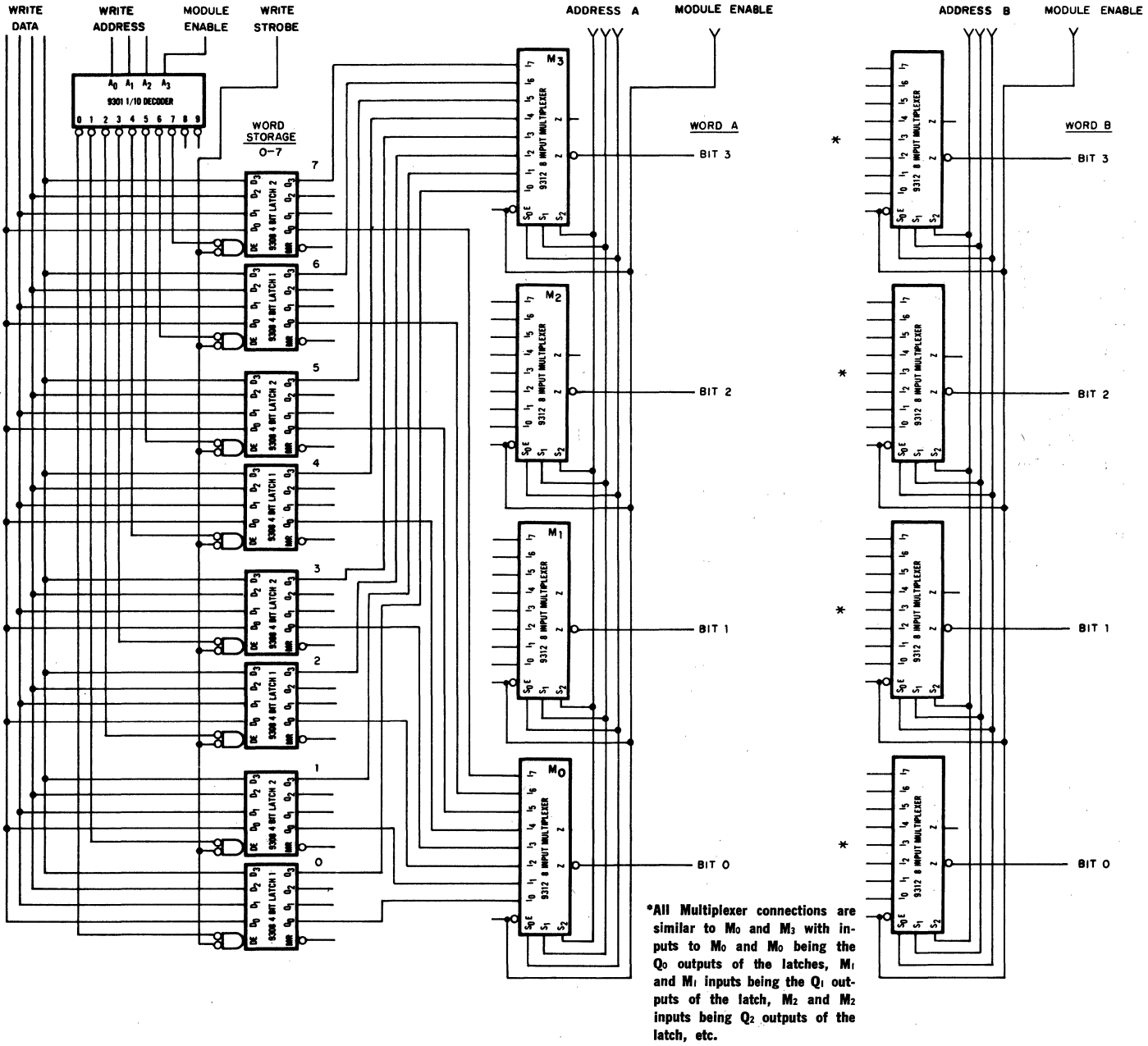
APPLICATIONS

A MULTI-PORT MEMORY MODULE

The four bit by eight word multi-port memory module shown in the below diagram uses only thirteen MSI packages; four 9308 24 pin dual four bit latches, eight 9312 eight input multiplexers, and one 9301 one-out-of-ten decoder.

The module as shown is capable of simultaneously reading from two independently specified locations and writing into a third independently selected location. The necessary enables are provided so that a number of these modules may be connected together to produce a larger memory. As an example a sixteen bit by sixty-four word memory would require thirty-two of the modules shown below.

By connecting this type of memory to a function generator unit, a processor could be constructed that would execute three address instructions at a very high speed on the data contained in this type of memory. In order to utilize the speed of the memory the instructions would also have to be contained in fast semiconductor memory.



*All Multiplexer connections are similar to M_0 and M_3 with inputs to M_0 and M_0 being the Q_0 outputs of the latches, M_1 and M_1 inputs being the Q_1 outputs of the latch, M_2 and M_2 inputs being Q_2 outputs of the latch, etc.

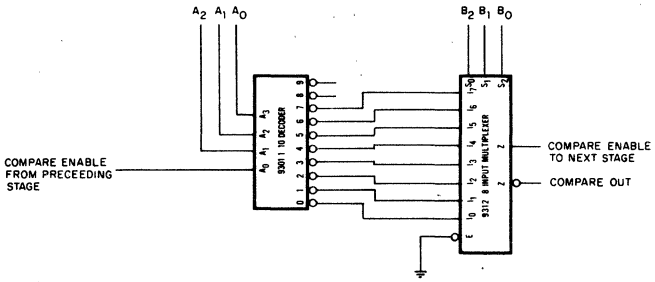
Fig. 17

APPLICATIONS

3 BIT COMPARATOR

Three bits of data to be compared are supplied to the address and select inputs of the 9301 and 9312 respectively. If A_0, A_1, A_2, and B_0, B_1, B_2 compare, the mutually exclusive active low output of the 9301 1/10 decoder and the selected input of the 9312 multiplexer will be coincidental and COMPARE OUT will be high. The COMPARE ENABLE must be low to permit compare operation.

3 BIT COMPARATOR



INTERCONNECTION DIAGRAM FOR 9 BITS

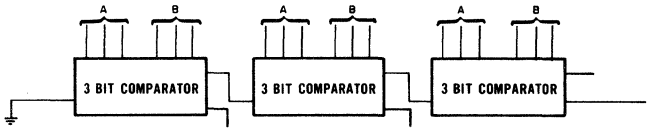


Fig. 18

IMPLEMENTING ANY FOUR-VARIABLE BOOLEAN FUNCTION

The 9312 eight input multiplexer can (in addition to performing its nominal function) produce any Boolean function of four variables without any additional elements if both the assertion and negation of one of the variables are present. If an assertion and negation are not present, one inverter may be required.

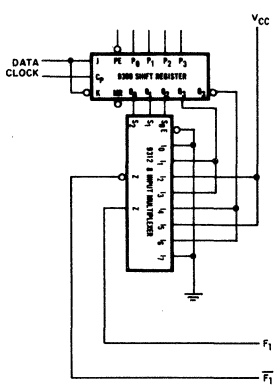
The procedure for implementing a four-variable function, along with an example, is shown in the attached diagram. First, consider the function in terms of a Karnaugh map. If the Q_0, Q_1 and Q_2 variable are connected to the S_0, S_1 and S_2 inputs of the 9312 then the Karnaugh map will be split, as shown, into eight sections, with each section corresponding to an input to the 9312. In order to implement the function each input of the 9312 is connected to one of the following four signals: ground, V_{CC}, the assertion, or negation of the fourth variable.

The contents of the two squares associated with an input, on the Karnaugh map, determine which connection is made to that input. If both squares contain a zero, ground should be connected to the input; if both squares contain a one, the input should be connected to V_{CC}. If the two squares contain a one and a zero then either the assertion or negation of the fourth variable will be required to implement the function. If the single one is located in the square associated with the assertion of the fourth variable then the assertion of the assertion of the fourth variable is connected to that input, and vice versa.

Shown in the illustration below is a 9312 decoding the condition of a 9300, producing a one output whenever the register contains two or more transitions. The truth table, Karnaugh map and the connection to the 9312 for this function are also shown in the illustration.

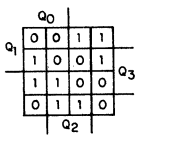
In many applications, using the 9312 to implement general logic functions of four variables will result in a sizeable reduction in package count. In many cases use of the 9312 with additional gates to produce functions of more than four variables will also reduce the package count.

The concept of using the 9312 eight input-multiplexer as a general logic function generator is described by S. S. Yau and C. K. Tang of Northwestern University in a paper presented at the 1968 Spring Joint Computer Conference in Atlantic City, New Jersey.

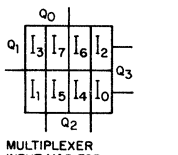


Q_0	Q_1	Q_2	Q_3	F_1
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

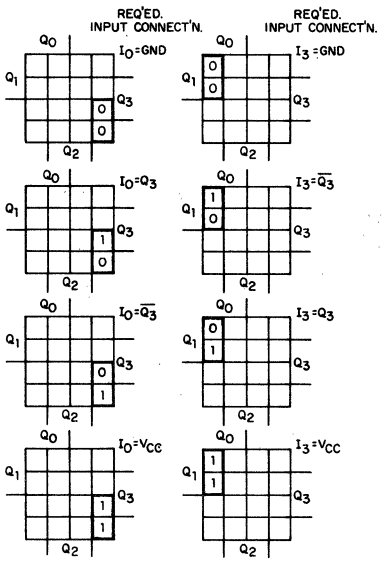
TRUTH TABLE



KARNAUGH MAP OF FOUR VARIABLE FUNCTION.



MULTIPLEXER INPUT MAP FOR $S_0=Q_0$, $S_1=Q_1$, $S_2=Q_2$



FROM THE KARNAUGH MAP OF THE DESIRED FUNCTION I_0–I_7 CONNECTIONS CAN BE DETERMINED.

Fig. 19

TTμL9601

RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

TRANSISTOR-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

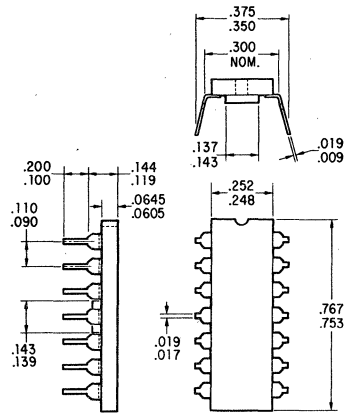
A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The retriggerable monostable multivibrator or one-shot provides an output pulse with high accuracy and a very wide duration range (50 nsec to ∞). It has four DC level-sensitive inputs, two are active-level High and two are active-level Low. Designed for high speed operation, the 9601 will respond to trigger inputs even when already in its active timing state, and will time itself out from the last input pulse received.

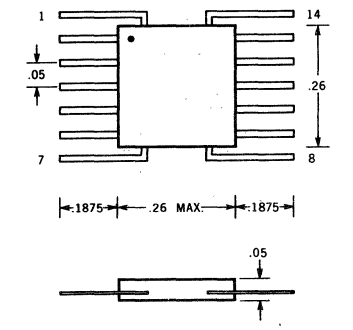
The unique design of the 9601 makes it very useful in applications such as in square-wave and variable delay pulse generators, long delay timers, pulse absence detectors, digital low-pass filters, and even FM demodulators.

- **HIGH SPEED OPERATION — MAXIMUM INPUT REP/RATE GREATER THAN 10 MHz**
- **COMPLEMENTARY DC LEVEL SENSITIVE INPUTS**
- **50 nsec TO ∞ OUTPUT PULSE WIDTH RANGE**
- **OPTIONAL RETRIGGERING/LOCK-OUT CAPABILITY**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH DTμL, LPDTμL, TTμL, MSI, AND OTHER CCSL PRODUCTS.**

FAIRPAK OUTLINE



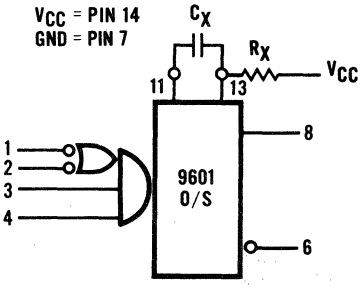
TYPICAL FLAT PACKAGE
TOP VIEW



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +8 V
Input Voltage	−0.5 V to +5.5 V
Voltage Applied to Outputs	−0.5 V to +V_{CC} value

LOGIC DIAGRAM



ORDER INFORMATION

Specify U3I96015XX for flat package and U1A96015XX for FAIRPAK package, where 5XX is 51X for −55°C to +125°C temperature range or 59X for the 0°C to +75°C temperature range.

PULSE WIDTH CALCULATION

$TPW = 0.36\ R_X C_X$

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD RETRIGGERABLE MONOSTABLE MULTIVIBRATOR TTμL9601

ELECTRICAL CHARACTERISTICS 0°C to +75°C, $V_{CC} = 5.0\ V \pm 5\%$

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS (Note 1)
V_{OH}	Output High Voltage	2.4		2.4	3.4		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.72\ mA$ (Note 2)
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 10.0\ mA$ (Note 2)
V_{IH}	Input High Voltage	2.0		2.0	1.7				Volts	$V_{CC} = 4.75\ V$ (Note 3)
V_{IL}	Input Low Voltage				1.4	0.8		0.8	Volts	$V_{CC} = 5.25\ V$ (Note 3)
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$
I_F	Input Load Current		−1.24		−0.97	−1.24		−1.24	mA	$V_{CC} = 4.75\ V$, $V_F = 0.45\ V$
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
I_{pd}	Quiescent Power Supply Drain		25			25		25	mA	$V_{CC} = 5.25\ V$
T_{pd+}	Negative Trigger Input to True Output				25	50			ns	$V_{CC} = 5.0\ V$, $R_X = 5\ K\Omega$, $C_X = 0$, $C_L = 15\ pF$
T_{pd-}	Negative Trigger Input to Complement Output				25	50			ns	$V_{CC} = 5.0\ V$, $R_X = 5\ K\Omega$, $C_X = 0$, $C_L = 15\ pF$
$T_{pw\ min}$	Min True Output Pulse Width				45	65			ns	$V_{CC} = 5.0\ V$, $R_X = 5\ K\Omega$, $C_X = 0$, $C_L = 15\ pF$
C_{stray}	Max allowable Wiring Cap Pin 13 (Note 4)		50			50		50	pF	Pin 13 to Ground
R_X	Timing Resistor	5	40	5		40	5	40	KΩ	

NOTES:

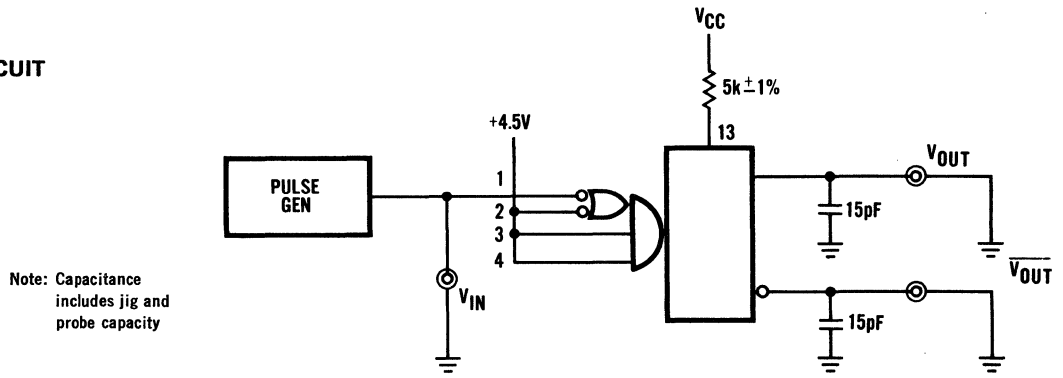
(1) Unless otherwise noted, 10 KΩ resistor is placed between Pin 13 and V_{CC} for all tests. (R_X)

(2) Ground Pin 11 for V_{OL} Pin 6 or V_{OH} Pin 8
Open Pin 11 for V_{OL} Pin 8 or V_{OH} Pin 6

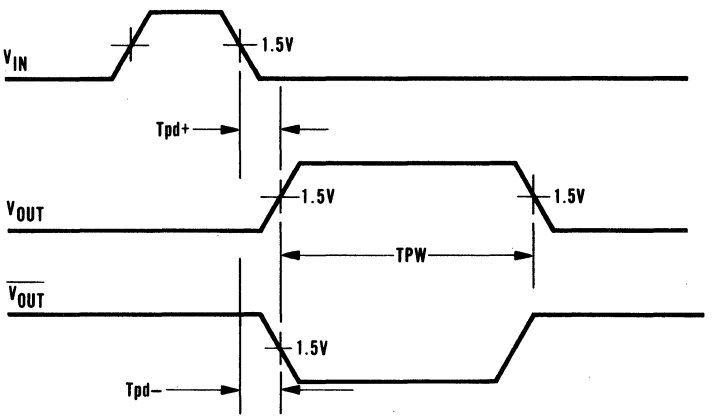
(3) Pulse test to determine V_{IH} and V_{IL} (min. pw 40 nsec)

(4) This capacitance, if present, will add to C_X in determining output pulse width.

tpd TEST CIRCUIT



Note: Capacitance includes jig and probe capacity



f ≃ 1 MHz
Amp ≃ 3 V
Width ≃ 40 ns
$t_r = t_f \leq 10$ ns

ELECTRICAL CHARACTERISTICS −55°C to +125°C, V_{CC} = 5.0 V ±10%

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	CONDITIONS (Note 1)
V_{OH}	Output High Voltage	2.4		2.4	3.3		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −0.72 mA (Note 2)
V_{OL}	Output Low Voltage		0.40	0.2	0.40			0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 10.0 mA (Note 2)
V_{IH}	Input High Voltage	2.0		2.0	1.7				Volts	V_{CC} = 4.5 V (Note 3)
V_{IL}	Input Low Voltage				1.4	0.85		0.85	Volts	V_{CC} = 5.5 V (Note 3)
I_F	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	V_{CC} = 5.5 V, V_F = 0.4 V
I_F	Input Load Current		−1.24		−0.97	−1.24		−1.24	mA	V_{CC} = 4.5 V, V_F = 0.4 V
I_R	Input Leakage Current				15	60		60	μA	V_{CC} = 5.5 V, V_R = 4.5 V
I_{pd}	Quiescent Power Supply Drain		25			25		25	mA	V_{CC} = 5.5 V
T_{pd+}	Negative Trigger Input to True Output				25	50			ns	V_{CC} = 5.0 V, R_X = 5 KΩ C_X = 0, C_L = 15 pF
T_{pd-}	Negative Trigger Input to Complement Output				25	50			ns	V_{CC} = 5.0 V, R_X = 5 KΩ C_X = 0, C_L = 15 pF
$T_{pw\ min}$	Min True Output Pulse Width				45	65			ns	V_{CC} = 5.0 V, R_X = 5 KΩ C_X = 0, C_L = 15 pF
C_{stray}	Max allowable Wiring Cap Pin 13 (Note 4)		50			50		50	pF	Pin 13 to Ground
R_X	Timing Resistor	5	20	5		20	5	20	KΩ	

NOTES:

(1) Unless otherwise noted, 10 KΩ resistor is placed between Pin 13 and V_{CC} for all tests. (R_X)

(2) Ground Pin 11 for V_{OL} Pin 6 or V_{OH} Pin 8
Open Pin 11 for V_{OL} Pin 8 or V_{OH} Pin 6

(3) Pulse test to determine V_{IH} and V_{IL} (min. pw 40 nsec)

(4) This capacitance, if present, will add to C_X in determining output pulse width.

LOADING RULES

INPUT LEVEL	LOAD FACTOR
High	1
Low	1

OUTPUT STATE	FANOUT
High	12
Low	8

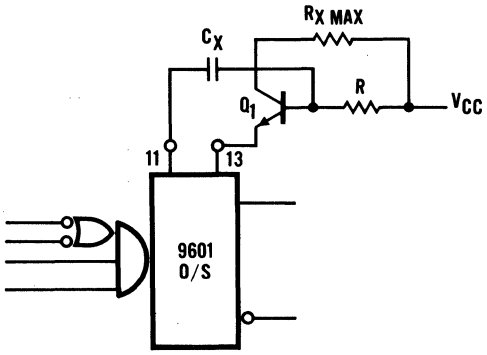
1 High Level Load = I_R
1 Low Level Load = I_F

APPLICATION HINTS

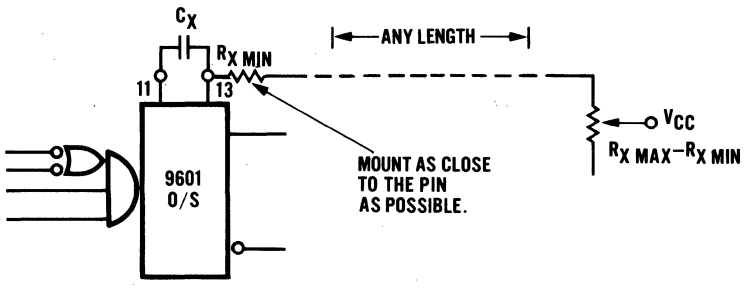
A. Extending the Range of the External Timing Resistor R_X.

Pulse Width stability over Supply Voltage and Temperature Range will depreciate slightly using this circuit.

$R = H_{FE}Q_1\ (0.7)\ (R_{X\ max})$
Q_1 may be any NPN transistor with suitable H_{FE} at currents of < 1 mA.



B. Recommended Method for using Remotely Located Timing Resistors.



9622

DUAL LINE RECEIVER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9622 is a dual line receiver designed to discriminate a worst case logic swing of 2 volts from a ± 10 volt common mode noise signal or ground shift. A 1.5 volt threshold is built into the differential amplifier to offer a CCSL compatible threshold voltage and maximum noise immunity. The offset is obtained by use of current sources and matched resistors and varies only ± 5% (75 mV) over the military and industrial temperature ranges.

The 9622 allows the choice of output states with the inputs open without affecting circuit performance by use of S3. A 130 Ω terminating resistor is provided at the input of the each line receiver. An enable is also provided for each line receiver. The output is CCSL compatible. The output high level can be increased to +12 V by tieing it to a positive supply through a resistor. The outputs can be wire-OR'ed.

FEATURES:

- **CCSL COMPATIBLE THRESHOLD VOLTAGE**
- **INPUT TERMINATING RESISTORS**
- **CHOICE OF OUTPUT STATE WITH INPUTS OPEN**
- **CCSL COMPATIBLE OUTPUT**
- **HIGH COMMON MODE**
- **WIRE-OR CAPABILITY**
- **ENABLE INPUTS**
- **FULL MILITARY TEMPERATURE RANGE**
- **LOGIC COMPATIBLE SUPPLY VOLTAGES**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

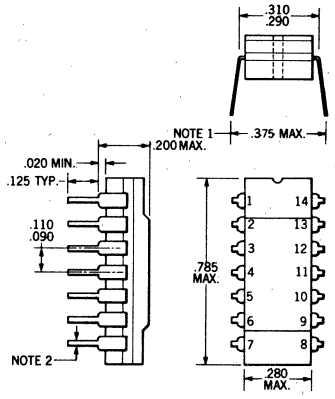
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Input Voltage	±15 V
Voltage Applied to Outputs for High Output State	−0.5 V to +13.2 V
V_{EE} Pin Potential to Ground Pin	−0.5 V to −12 V
Enable Pin Potential to Ground Pin	−0.5 V to +15 V

ORDER INFORMATION

Specify U6A9622XXX for 14 pin Dual In-Line package, U3I9622XXX for 14 pin Flat package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

TYPICAL DUAL IN-LINE PACKAGE

In Accordance With
JEDEC (TO-116) Outline

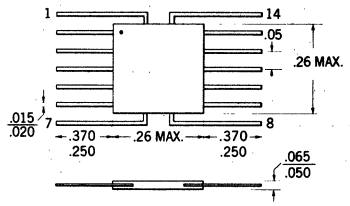


NOTES:

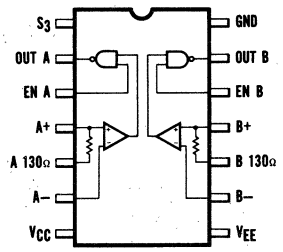
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

FLAT PACKAGE

TOP VIEW



LOGIC DIAGRAM



313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

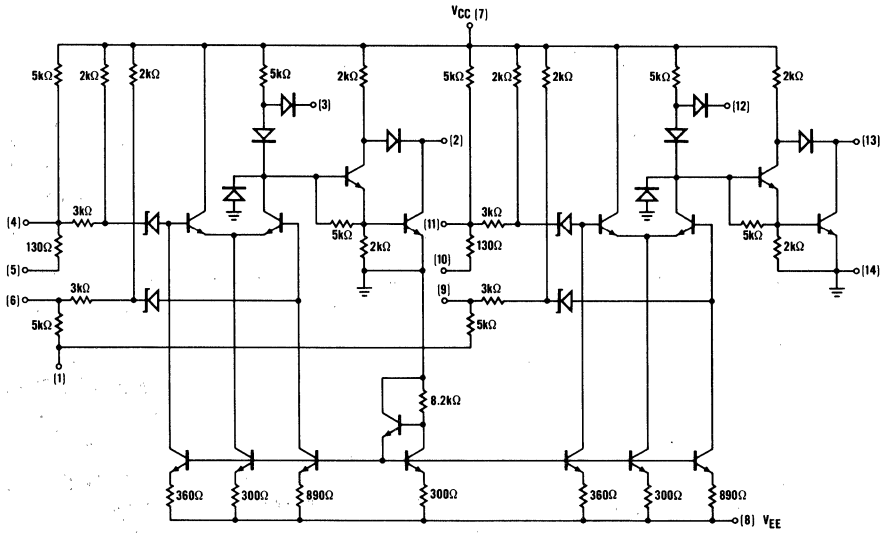
FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ELECTRICAL CHARACTERISTICS (Temperature Range −55°C to +125°C, V_{CC} = 5.0 V ±10%, V_{EE} = −10 V ±10%) (Part No. UXX962251X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OL}	Output Low Voltage		0.40		0.25	0.40		0.40	V	V_{CC} = 4.5 V *V_{DIFF} = 2.0 V	V_{EE} = −11 V I_{OL} = 12.4 mA
V_{OH}	Output High Voltage	2.8		3.0	3.3		2.9		V	V_{CC} = 4.5 V *V_{DIFF} = 1.0 V	V_{EE} = −9.0 V I_{OH} = −0.2 mA
I_{CEX}	Output Leakage Current		50			100		200	μA	V_{CC} = 4.5 V *V_{DIFF} = 1.0 V	V_{EE} = −11 V V_{CEX} = 12 V
I_{SC}	Output Shorted Current	−1.3	−3.1	−1.4	−2.15	−3.1	−1.3	−3.1	mA	V_{CC} = 5.0 V *V_{DIFF} = 1.0 V	V_{EE} = −10 V V_{SC} = 0 V
$I_{R(ENABLE)}$	Enable Input Leakage Current					2.0		5.0	μA	V_{CC} = 4.5 V S_3 = 4.5 V	V_{EE} = −11 V V_R = 4.0 V
$I_{F(ENABLE)}$	Enable Input Forward Current		−1.5		−0.96	−1.5		−1.5	mA	V_{CC} = 5.5 V S_3 = 0 V	V_{EE} = −9.0 V V_F = 0 V
$I_{F(+Input)}$	+ Input Forward Current		−2.3		−1.67	−2.1		−2.0	mA	V_{CC} = 5.0 V − Input = Gnd	V_{EE} = −10 V V_F = 0 V
$I_{F(-Input)}$	− Input Forward Current		−2.6		−1.87	−2.4		−2.3	mA	V_{CC}, S_3 = 5.0 V + Input = Gnd	V_{EE} = −10 V V_F = 0 V
$V_{IL(ENABLE)}$	Input Low Voltage		1.3		1.4	1.0		0.7	V	V_{CC} = 5.0 V ±10% V_{EE} = −10 V ±10%	
V_{th}	Differential Input Threshold Voltage	1.0	2.0	1.0	1.5	2.0	1.0	2.0	V	V_{CC} = 5.0 V ±10% V_{EE} = −10 V ±10%	
V_{CM}	Common Mode Voltage			−10	±12	+10			V	V_{CC} = 5.0 V *V_{DIFF} = 1.0 V or 2.0 V	V_{EE} = −10 V
$R_{130\Omega}$	Terminating Resistance			100	130	175			Ω		
I_{CC}	5 V Supply Current				13.7	22.9			mA	V_{CC} = 5.5 V S_3, + Inputs = 5.5 V, − Inputs = 0 V	V_{EE} = −11 V
I_{EE}	−10 V Supply Current				−6.5	−11.1			mA	V_{CC} = 5.5 V S_3, + Inputs = 5.5 V, − Inputs = 0 V	V_{EE} = −11 V
t_{pd+}	Turn-off Time				38	50			ns	V_{CC} = 5.0 V V_{IN} 0→3 V, R_L = 3.9 kΩ, C_L = 30 pF	V_{EE} = −10 V
t_{pd-}	Turn-on Time				35	50			ns	V_{CC} = 5.0 V V_{IN} 0→3.0 V, R_L = 0.39 kΩ, C_L = 30 pF	V_{EE} = −10 V

*V_{DIFF} is a differential input voltage referred from A+ to A− and from B+ to B−.

SCHEMATIC DIAGRAM
(LINE RECEIVER)

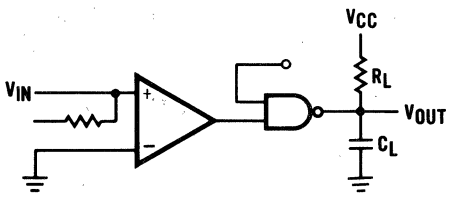


ELECTRICAL CHARACTERISTICS (Temperature Range 0°C to +75°C, V_{CC} = 5.0 V ±5%, V_{EE} = −10 V ±5%) (Part No. UXX962259X)

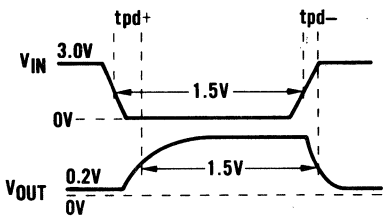
SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	V	V_{CC} = 4.75 V *V_{DIFF} = 2.0 V	V_{EE} = −10.5 V I_{OL} = 14.1 mA
V_{OH}	Output High Voltage	2.9		3.0	3.3		2.9		V	V_{CC} = 4.75 V *V_{DIFF} = 1.0 V	V_{EE} = −9.5 V I_{OH} = −0.2 mA
I_{CEX}	Output Leakage Current		80			100		200	μA	V_{CC} = 4.75 V *V_{DIFF} = 1.0 V	V_{EE} = −10.5 V V_{CEX} = 5.25 V
I_{SC}	Output Shorted Current	−1.3	−3.1	−1.4	−2.15	−3.2	−1.3	−3.1	mA	V_{CC} = 5.0 V *V_{DIFF} = 1.0 V	V_{EE} = −10 V V_{SC} = 0 V
$I_{R(ENABLE)}$	Enable Input Leakage Current					5		10	μA	V_{CC} = 4.75 V S_3 = 4.75 V	V_{EE} = −10.5 V V_R = 4.0 V
$I_{F(ENABLE)}$	Enable Input Forward Current		−1.5		−.96	−1.5		−1.5	mA	V_{CC} = 5.25 V S_3 = 0 V	V_{EE} = −9.5 V V_F = 0 V
$I_{F(+Input)}$	+ Input Forward Current		−2.6		−1.67	−2.4		−2.3	mA	V_{CC} = 5.0 V − Input = Gnd	V_{EE} = −10 V V_F = 0 V
$I_{F(-Input)}$	− Input Forward Current		−2.9		−1.87	−2.7		−2.6	mA	V_{CC}, S_3 = 5.0 V + Input = Gnd	V_{EE} = −10 V V_F = 0 V
$V_{IL(ENABLE)}$	Input Low Voltage		1.2		1.4	1.0		0.85	V	V_{CC} = 5.0 V ±5% V_{EE} = −10 V ±5%	
V_{th}	Differential Input Threshold Voltage	1.0	2.0	1.0	1.5	2.0	1.0	2.0	V	V_{CC} = 5.0 V ±5% V_{EE} = −10 V ±5%	
V_{CM}	Common Mode Voltage			−7.5	±12	+7.5			V	V_{CC} = 5.0 V *V_{DIFF} = 1.0 V or 2.0 V	V_{EE} = −10 V
$R_{130}\Omega$	Terminating Resistance			91	130	185			Ω		
I_{CC}	5 V Supply Current				13.7	22.9			mA	V_{CC} = 5.25 V S_3, +Inputs = 5.25 V, −Inputs = 0 V	V_{EE} = −10.5 V
I_{EE}	−10 V Supply Current				−6.5	−11.1			mA	V_{CC} = 5.25 V S_3, +Inputs = 5.25 V, −Inputs = 0 V	V_{EE} = −10.5 V
t_{pd+}	Turn-off Time				38	100			ns	V_{CC} = 5.0 V V_{IN} 0→3.0 V, R_L = 3.9 kΩ, C_L = 30 pF	V_{EE} = −10 V
t_{pd-}	Turn-on Time				35	100			ns	V_{CC} = 5.0 V V_{IN} 0→3.0 V, R_L = 0.39 kΩ, C_L = 30 pF	V_{EE} = −10 V

*V_{DIFF} is a differential input voltage referred from A+ to A− and from B+ to B−.

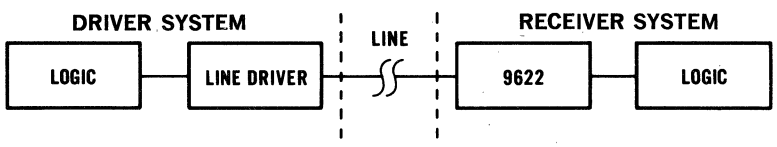
SWITCHING TIME TEST CIRCUIT



WAVEFORMS

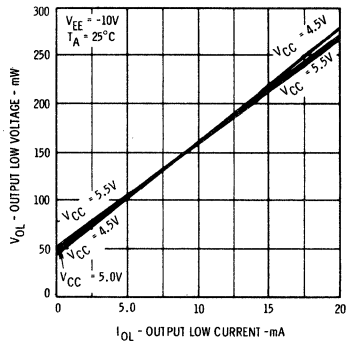


STANDARD USAGE

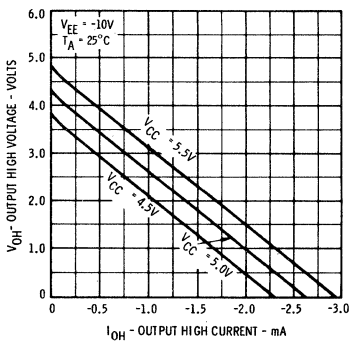


TYPICAL ELECTRICAL CHARACTERISTICS

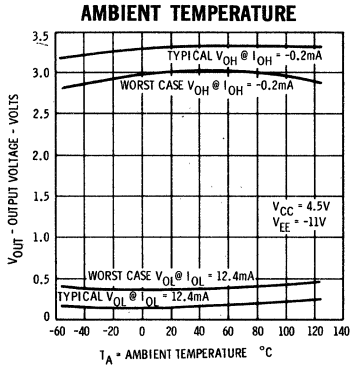
TYPICAL OUTPUT LOW VOLTAGE VERSUS OUTPUT LOW CURRENT



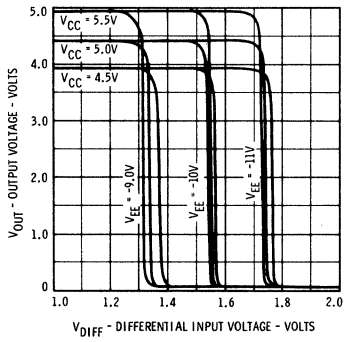
TYPICAL OUTPUT HIGH VOLTAGE VERSUS OUTPUT HIGH CURRENT



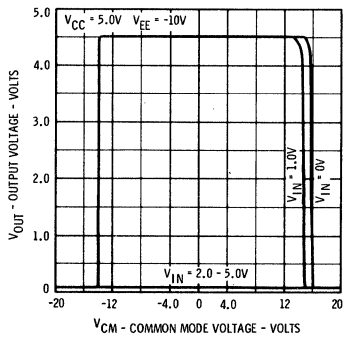
LOGIC LEVELS VERSUS AMBIENT TEMPERATURE



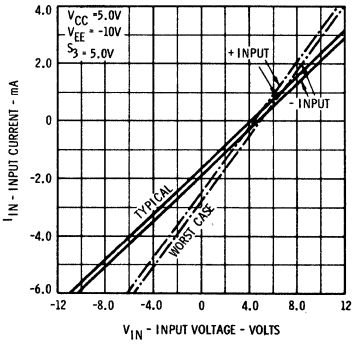
TYPICAL V_{out} - V_{DIFF} TRANSFER CHARACTERISTICS



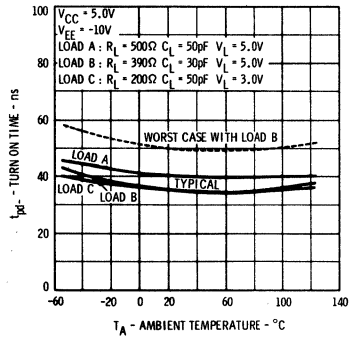
TYPICAL OUTPUT VOLTAGE VERSUS COMMON MODE VOLTAGE



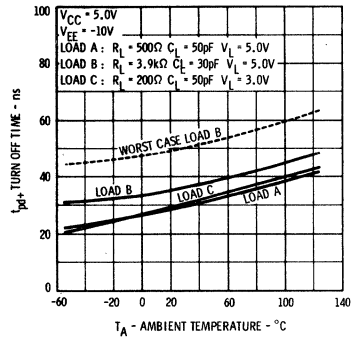
INPUT CURRENT VERSUS INPUT VOLTAGE



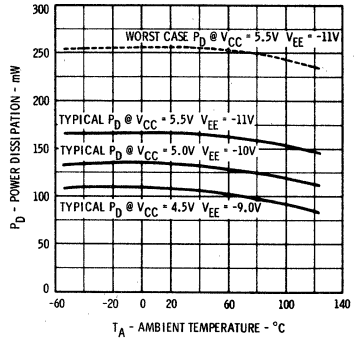
TURN ON TIME VERSUS AMBIENT TEMPERATURE



TURN OFF TIME VERSUS AMBIENT TEMPERATURE



POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



FAIRCHILD DIODE-TRANSISTOR MICROLOGIC®

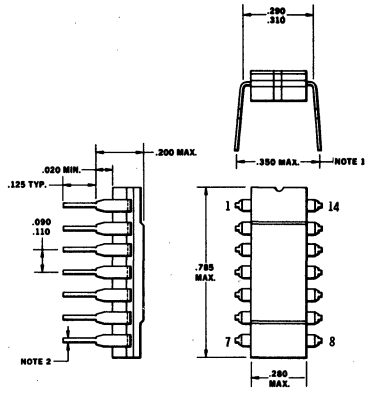
INTEGRATED CIRCUITS COMPOSITE DATA SHEET

A FAIRCHILD *COMPATIBLE CURRENT SINKING LOGIC* PRODUCT
0°C TO 75°C TEMPERATURE RANGE

GENERAL DESCRIPTION — Fairchild Diode Transistor Micrologic® (DTμL) Integrated Circuits family uses diode-transistor logic and is designed specfically for integrated circuit technology. The design of these circuits offers distinctly superior performance. Some of the advantages follow:

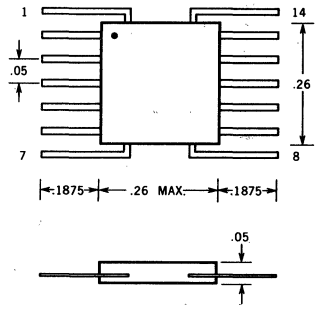
- **HIGH PERFORMANCE WITH A SINGLE POWER SUPPLY - - 5.0 V**
- **HIGH NOISE IMMUNITY - - 1.0 V**
- **HIGH FAN-OUT CAPABILITY - - 8-25**
- **GATES WITH 6 k OR 2 k PULL-UP RESISTORS FOR OPTIMUM SPEED**
- **FAN-OUT AND NOISE IMMUNITY TRADE-OFF**
- **LOW POWER DISSIPATION - - 8.5 mW/GATE**
- **GATE OUTPUTS CAN BE TIED TOGETHER FOR THE "WIRED OR" FUNCTION**

TYPICAL DUAL IN-LINE PACKAGE
(In accordance with JEDEC TO—116)



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

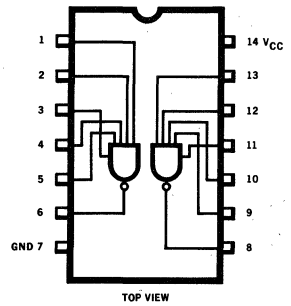
TYPICAL FLAT PACKAGE
TOP VIEW



ORDER INFORMATION — To order Diode Transistor Micrologic® Integrated Circuits elements specify U31XXXX59X for Flat package and U6AXXXX59X for Dual In-Line* package where XXXX is 9930, 9932 etc.

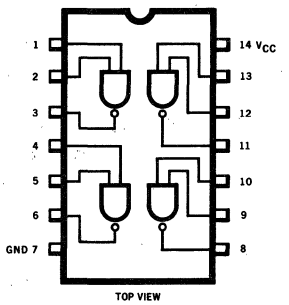
PIN CONFIGURATION: IDENTICAL FOR DUAL-IN-LINE AND FLAT PACKAGES

DTμL 9930 • DTμL 9961
DTμL 9932 • DTμL 9944



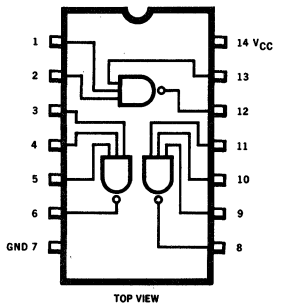
TOP VIEW

DTμL 9946 • DTμL 9949



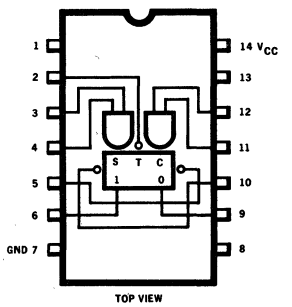
TOP VIEW

DTμL 9962 • DTμL 9963



TOP VIEW

DTμL 9945 • DTμL 9948



TOP VIEW

*Fairchild Patent Pending

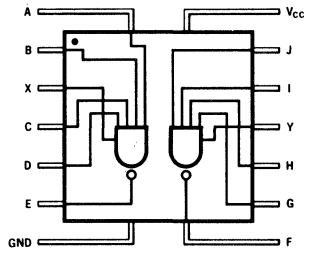
FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

DTμL GATES

All DTμL gates are positive logic NAND gates or negative logic NOR gates. A variety of gate combinations is available which provides the system designer the utmost in logic flexibility and reduces package requirements to a minimum. Gate outputs may be paralleled to perform OR (collector) logic. In addition, gates may be cross-connected to form flip-flops, exclusive OR, etc. Gates with 2 kΩ pull-up resistors offer improved propagation delay times.

LOGIC DIAGRAM



POSITIVE (NAND) LOGIC

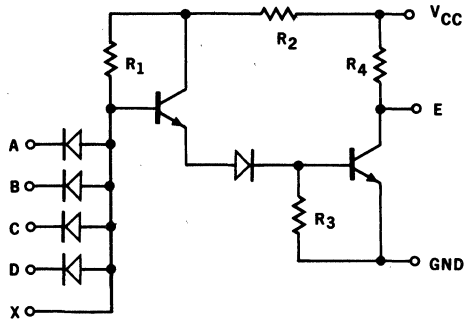
$E = \overline{A \cdot B \cdot C \cdot D \cdot (X)}$

$F = \overline{G \cdot H \cdot I \cdot J \cdot (Y)}$

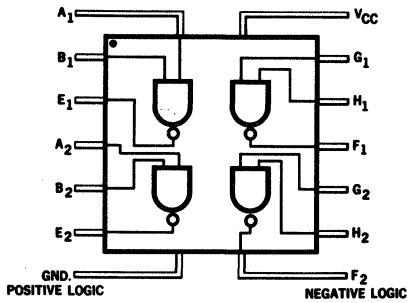
SCHEMATIC DIAGRAM — ONE GATE ONLY
DTμL 9930 • DTμL 9961

TYPICAL RESISTOR VALUES

$R_1 = 2.00k\ \Omega$
$R_2 = 1.75k\ \Omega$
$R_3 = 5.00k\ \Omega$
$R_4 = 6.00k\ \Omega$ (9930)
$R_4 = 2.00k\ \Omega$ (9961)



LOGIC DIAGRAM



POSITIVE (NAND) LOGIC

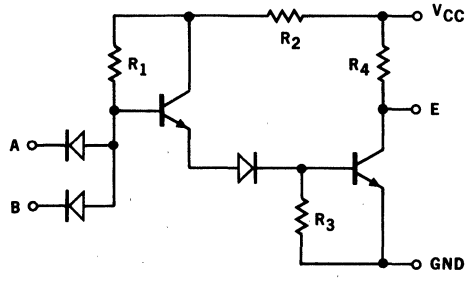
$E = \overline{A \cdot B}$

$F = \overline{G \cdot H}$

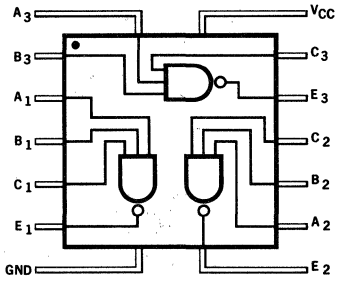
SCHEMATIC DIAGRAM — ONE GATE ONLY
DTμL 9946 • DTμL 9949

TYPICAL RESISTOR VALUES

$R_1 = 2.00k\ \Omega$
$R_2 = 1.75k\ \Omega$
$R_3 = 5.00k\ \Omega$
$R_4 = 6.00k\ \Omega$ (9946)
$R_4 = 2.00k\ \Omega$ (9949)



LOGIC DIAGRAM



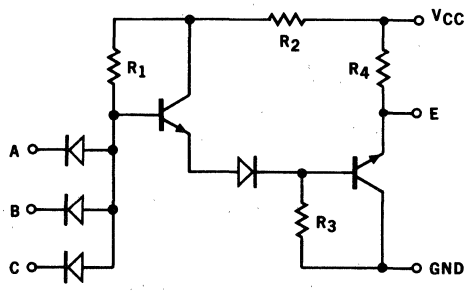
POSITIVE (NAND) LOGIC

$E = \overline{A \cdot B \cdot C}$

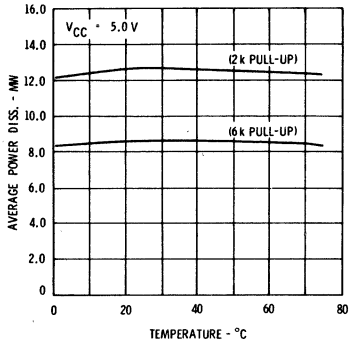
SCHEMATIC DIAGRAM — ONE GATE ONLY
DTμL 9962 • DTμL 9963

TYPICAL RESISTOR VALUES

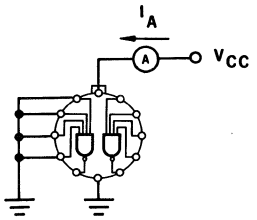
$R_1 = 2.00k\ \Omega$
$R_2 = 1.75k\ \Omega$
$R_3 = 5.00k\ \Omega$
$R_4 = 6.00k\ \Omega$ (9962)
$R_4 = 2.00k\ \Omega$ (9963)



AVERAGE POWER DISSIPATION VERSUS TEMPERATURE (TYPICAL EACH GATE)

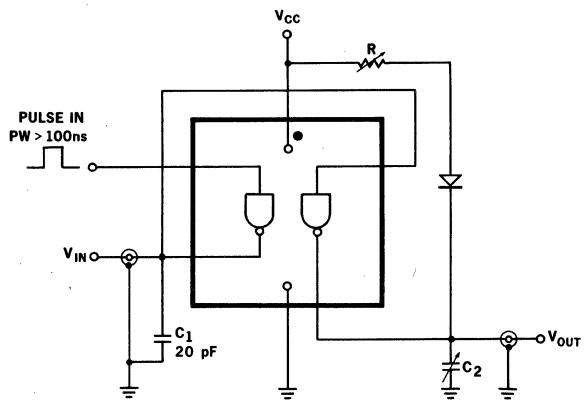


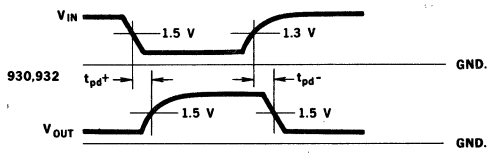
TEST CONDITIONS



AV. POWER DRAIN = $\frac{V_{CC}\ I_A}{2}$

TYPICAL Tpd TEST CIRCUIT DTμL GATES





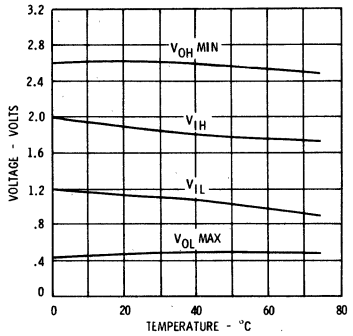
T_{pd} — will be read from input at 1.3 V

(V_{CC} = 5 V, T = 25°C)

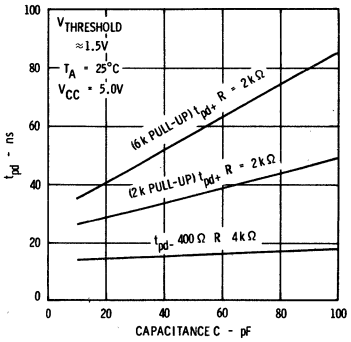
		R	C_2	Min.	Max.
(6 k Pull-up)	t_{pd+}	3.9kΩ	30 pF	25 ns	80 ns
(6 k & 2 k Pull-up)	t_{pd-}	400 Ω	50 pF	10 ns	30 ns
(2 k Pull-up)	t_{pd+}	3.9kΩ	30 pF	15 ns	50 ns

OPERATING VOLTAGE CHARACTERISTICS

WORST CASE (OUTPUT LOGIC LEVEL — V_{OH} AND V_{OL} / INPUT THRESHOLD LEVELS — V_{IH} AND V_{IL})



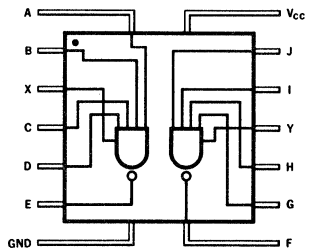
TIME DELAY VERSUS CAPACITIVE LOADS



DTμL 9932 BUFFER ELEMENT
DTμL 9944 POWER GATE

The DTμL 9932 is a dual 4-input inverting driver. It features an emitter-follower pull-up which provides a high fan-out device with superior capacitance-driving capability. The DTμL 9944 has an output with no internal pull-up. This provides a high fan-out device whose outputs may be tied together to perform the "wired OR" function. The 9944 is useful as an interface driver or as a low-power lamp driver. The fan-in of either element may be extended with the use of the DTμL 9933.

LOGIC DIAGRAM

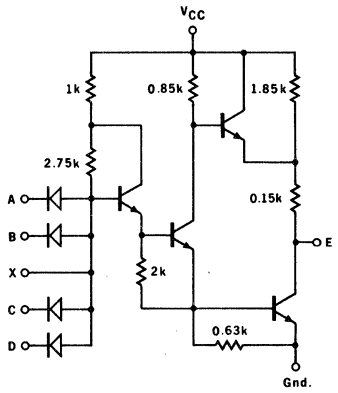


POSITIVE (NAND) LOGIC

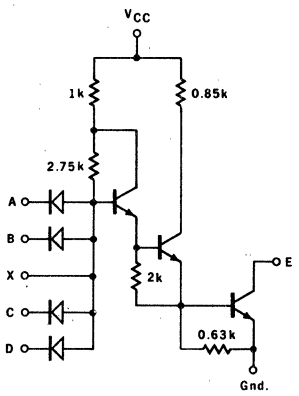
$E = \overline{A \cdot B \cdot C \cdot D \cdot (X)}$

$F = \overline{G \cdot H \cdot I \cdot J \cdot (Y)}$

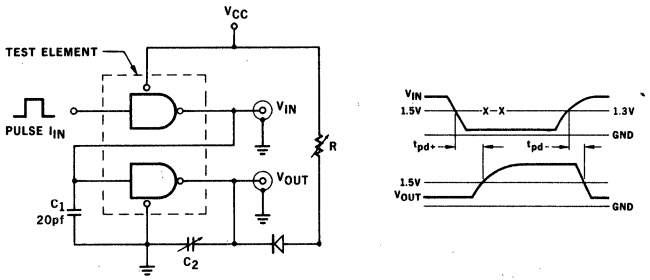
SCHEMATIC DIAGRAM OF THE DTμL 9932 ELEMENT (ONE SIDE ONLY)



SCHEMATIC DIAGRAM OF THE DTμL 9944 ELEMENT (ONE SIDE ONLY)



tpd TEST CIRCUIT FOR DTμL 9932 ELEMENT

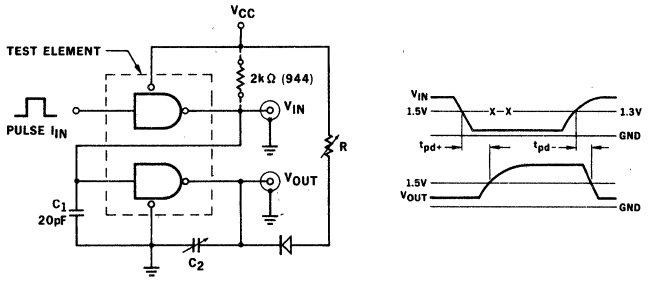


All Diodes are FD600 or Equivalent at 25°C
C_1 and C_2 includes Probe and Jig Capacitance

($V_{CC} = 5.0$ V, $T_A = 25°C$)

		R	C	Min.	Max.
t_{pd+}	9932	510 Ω	500 pF	25 ns	80 ns
t_{pd-}	9932	150 Ω	500 pF	15 ns	40 ns

tpd TEST CIRCUIT FOR DTμL 9944 ELEMENT

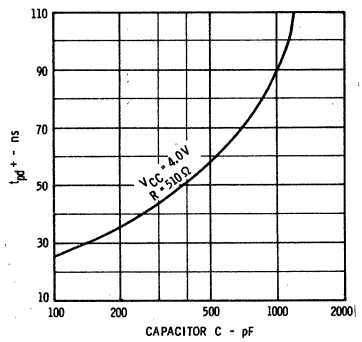


C_1 and C_2 includes Probe and Jig Capacitance

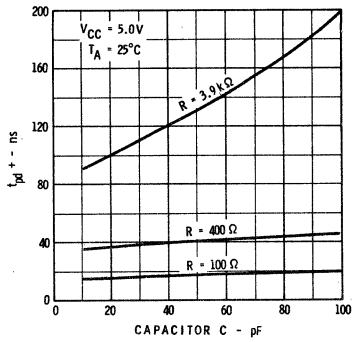
($V_{CC} = 5.0$ V, $T_A = 25°C$)

		R	C	Min.	Max.
t_{pd+}	9944	510 Ω	20 pF	15 ns	50 ns
t_{pd-}	9944	150 Ω	100 pF	10 ns	35 ns

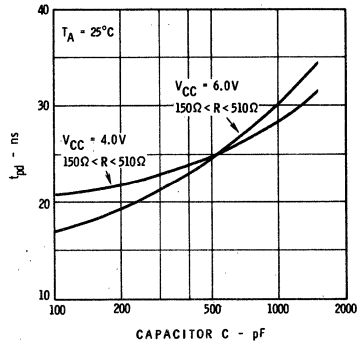
TYPICAL tpd + VERSUS CAPACITY (9932)



TYPICAL tpd + VERSUS CAPACITY (9944)



TYPICAL tpd – VERSUS CAPACITY (9932, 9944)



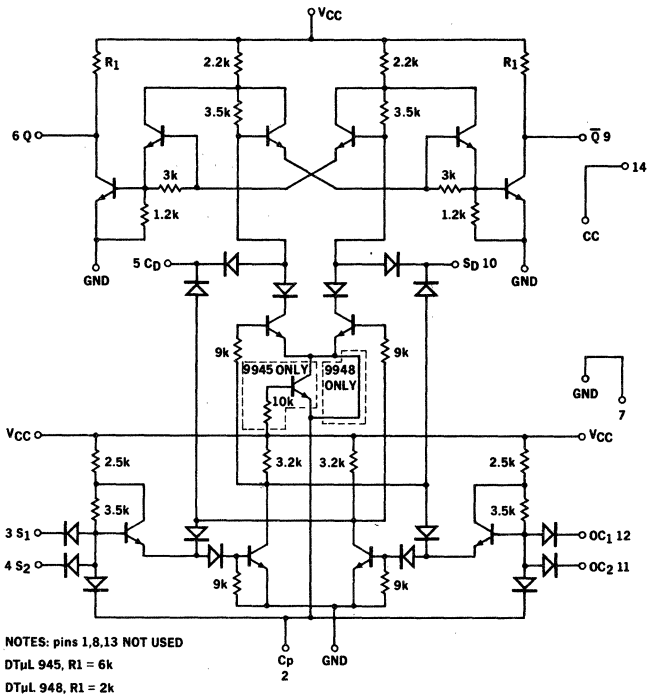
DTμL 9945 • DTμL 9948 - CLOCKED FLIP FLOP

The DTμL 9945 and DTμL 9948 Clocked Flip-Flops are directly-coupled units operating on the "master-slave" principle. Information enters the "master" while the Trigger input voltage is high and transfers to the "slave" when the Trigger input voltage goes low. Since operation depends only on voltage levels, any sort of waveshape having the proper voltage levels may be used as a trigger signal. Rise and fall times are irrelevant.

The DTμL 9945 and DTμL 9948 have an improved direct Set and Clear design which allows unhampered asynchronous entry irrespective of signals applied to any other inputs. The direct inputs always take precedence, thus simplifying the design of arbitrarily preset ripple-counters and other minimum hardware applications.

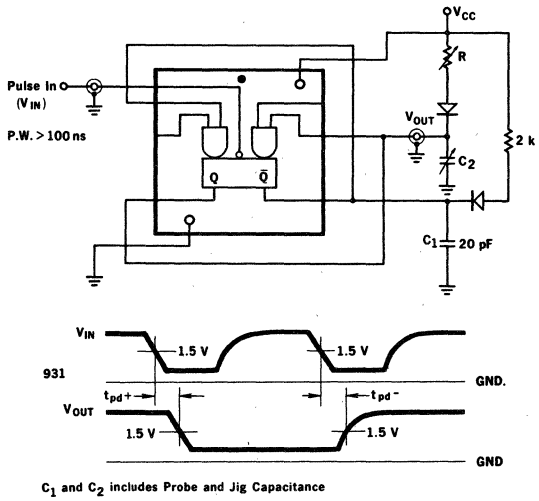
Output buffers provide isolation between the "slave" and the output load, thereby enhancing immunity to signal line noise. The DTμL 9945 incorporates the standard 6 k Ω output pull-up resistor, while the DTμL 9948 features a 2 k Ω output pull-up resistor for improved rise times, and matched delay between rising and falling outputs for capacitive loading up to 100 pF.

SCHEMATIC DIAGRAM



NOTES: pins 1,8,13 NOT USED
DTμL 945, R1 = 6k
DTμL 948, R1 = 2k

tpd TEST CIRCUIT

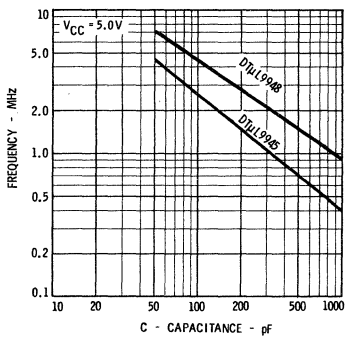


C_1 and C_2 includes Probe and Jig Capacitance

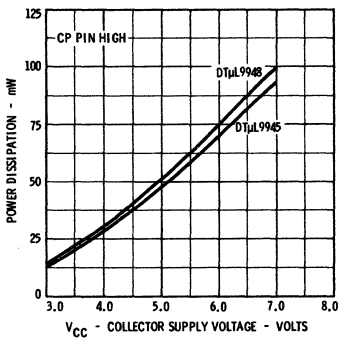
(V_{CC} = 5 V, T = 25°C)

		R	C_2	Min.	Max.
t_{pd+}	9945	2.00 k	30 pF	35 ns	75 ns
t_{pd-}	9945	330 Ω	30 pF	35 ns	75 ns
t_{pd+}	9948	2.00 k	30 pF	20 ns	65 ns
t_{pd-}	9948	330 Ω	30 pF	30 ns	75 ns

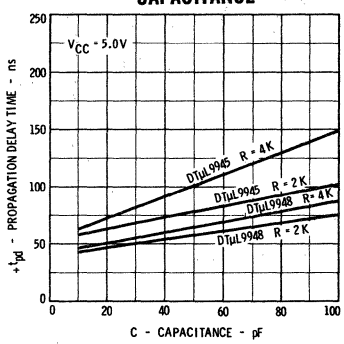
TYPICAL MAXIMUM BINARY COUNTING RATE VERSUS CAPACITY



TYPICAL POWER DISSIPATION VERSUS V_{CC}



TYPICAL tpd VERSUS CAPACITANCE

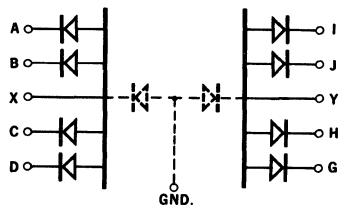


DTμL 9933 EXTENDER

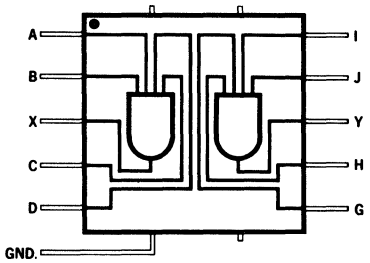
The DTμL 9933 is a Dual Input-Extender consisting of two independent diode arrays identical in every respect to the input diodes of the DTμL Gate and Buffer elements. Good practice dictates that extension interconnection paths be as short as possible to minimize the effects of distributed capacitance on circuit performance.

Typical input capacitance of DTμL 9933 is 2 pF, output capacitance is 5 pF.

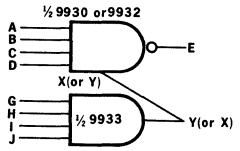
SCHEMATIC DIAGRAM



FLAT PACKAGE LAYOUT



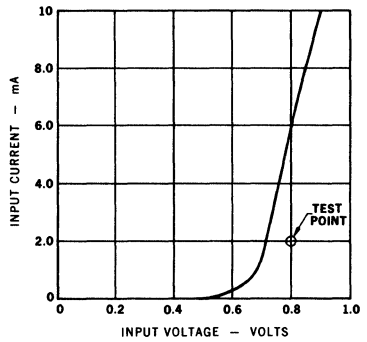
LOGIC EXAMPLE



POSITIVE LOGIC $E = \overline{A\,B\,C\,D\,G\,H\,I\,J}$

NEGATIVE LOGIC $E = A + B + C + D + G + H + I + J$

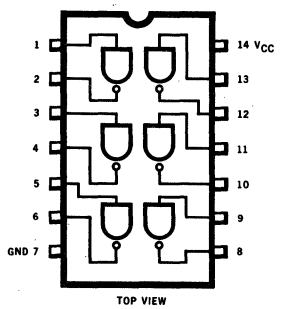
FORWARD VOLTAGE VERSUS FORWARD CURRENT +25°C



DTμL 9936 • DTμL 9937 - HEX INVERTER

The DTμL 9936 hex inverter has input-output characteristics identical to the other DTμL gates. Inverters can be cross-connected to form flip-flops or the outputs can be paralleled to perform the "wired OR" function.

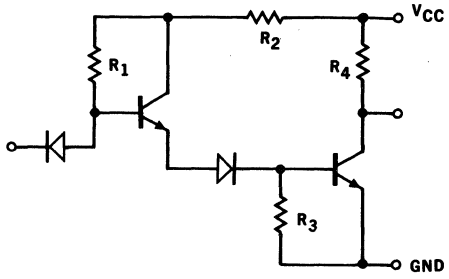
DTμL 9936 • DTμL 9937



SCHEMATIC DIAGRAM — ONE INVERTER ONLY
DTμL 9936 • DTμL 9937

TYPICAL RESISTOR VALUES

$R_1 = 2.00k\ \Omega$
$R_2 = 1.75k\ \Omega$
$R_3 = 5.00k\ \Omega$
$R_4 = 6.00k\ \Omega$ (9936)
$R_4 = 2.00k\ \Omega$ (9937)



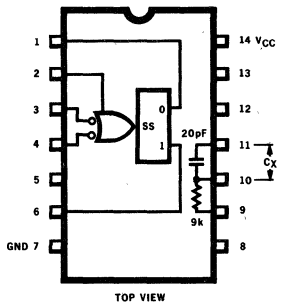
DTμL 9951 - MONOSTABLE MULTIVIBRATOR

The DTμL 9951 is an integrated monostable multivibrator designed for use with other members of the DTμL family. It provides complementary output pulses which are typically 100 ns wide. This pulse width is adjustable by the addition of external components.

ABSOLUTE MAXIMUM RATINGS
(above which useful life may be impaired)

Supply Voltage (V_{CC}), −55°C to +125°C, continuous:	+8.0 Volts
Supply Voltage (V_{CC}), pulsed, <1 second:	+12 Volts
Output Current, into outputs:	50 mA
Current into Pin 10	5.0 mA
Input Forward Current	−10 mA
Input Reverse Current	1.0 mA

DTμL 9951

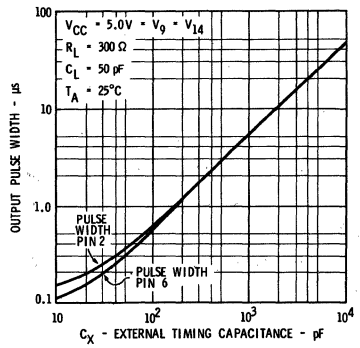


TOP VIEW

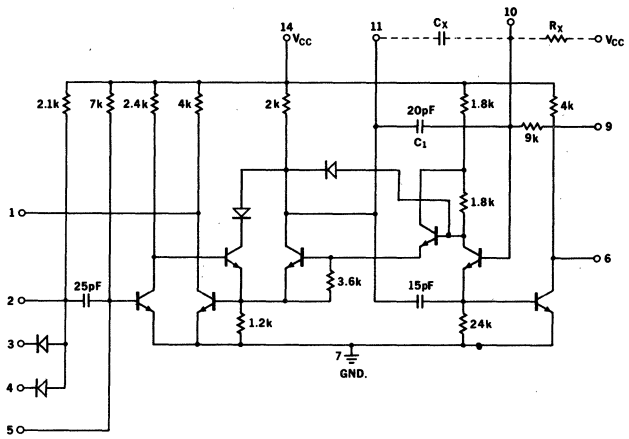
INPUT-OUTPUT LOAD FACTORS TO DTμL FAMILY

Each DTμL 9951 input should be rated at 2 loads.
Each DTμL 9951 output may drive 10 DTμL loads.

OUTPUT PULSE WIDTH VERSUS EXTERNAL TIMING CAPACITANCE C_X



SCHEMATIC DIAGRAM



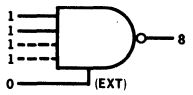
RULES FOR USE OF DTμL 9951

1. With Pin 9 connected to V_{CC} and no external capacitor (C_x), the output pulse width is approximately 100 ns.
2. With Pin 9 connected to V_{CC} and an external capacitor (C_x) connected between Pins 10 and 11, the output pulse width (T) is: $T \approx 4.5\ (C_x + 20)$ with C_x in pF and T in ns.
3. For improved pulse width control, Pin 9 is left open and a stable external resistor (R_x) of 9 kΩ minimum to 15 kΩ maximum is connected from Pin 10 to V_{CC}. The output pulse width is given by the expression: $T \approx 0.5\ R_x\ (C_x + 20)$ with R_x in kΩ, C_x in pF and T in ns.
4. The output duty cycle (pulse width/period) should not exceed 40%. It may be increased to 50% by adding a 2 kΩ resistor between Pin 11 and V_{CC}. Higher duty cycles are obtainable but the output pulse width and performance are less predictable.
5. The maximum input fall time to trigger: 25 ns for a 1.0-volt swing; 50 ns for a 2.0 volt swing; 100 ns for a 4.0-volt swing.
6. The AC sensitivity of the inputs may be decreased by connecting a capacitor between Pin 5 and ground.
7. The minimum pulse width at output Pin 1 is approximately 100 ns. This pulse width may be decreased to 50 ns by connecting a 10 kΩ resistor between Pin 5 and V_{CC}.

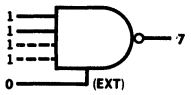
ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Supply Voltage (V_{CC}), −55°C to 125°C, continuous	+8.0 Volts
Supply Voltage (V_{CC}), pulsed, <1 second	+12 Volts
Output Current, into outputs	
DTμL 9932 & 9944	100 mA
DTμL, except 9932 & 9944	30 mA
Input Forward Current	−10 mA
Input Reverse Current	1.0 mA
Operating Temperature	0°C to +75°C
Storage Temperature	−65°C to +150°C

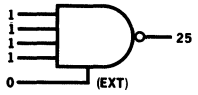
INPUT-OUTPUT LOADING FACTORS



1/2 DTμL 9930,
1/4 9946,
1/3 9962,
1/6 9936

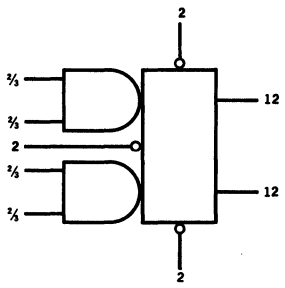


1/2 DTμL 9961,
1/4 9949,
1/3 9963,
1/6 9937

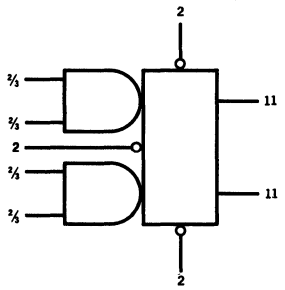


1/2 DTμL 9932
1/2 DTμL 9944

1/2 DTμL 9933



DTμL 9945

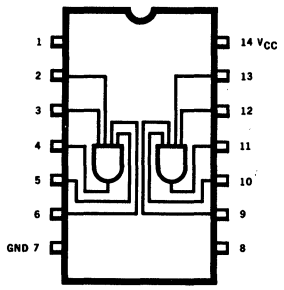


DTμL 9948

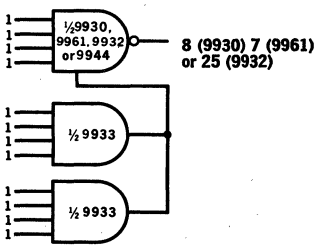
The number of elements that may be driven by an output terminal may consist of any combination of elements whose summation of input loading does not exceed the output terminal driving capability.

RULES FOR INPUT EXPANSION AND "WIRED OR" CONNECTION

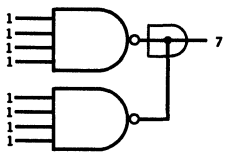
DTμL 9933
EXPANDER



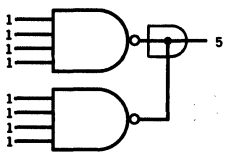
TOP VIEW



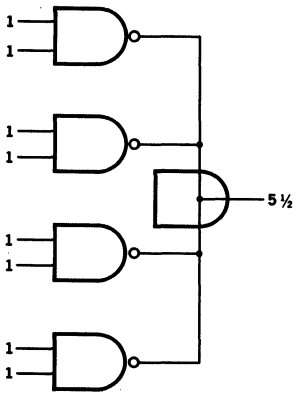
EXTENSION OF INPUTS



DTμL 9930 "wired OR"
ALSO 9946, 9962



DTμL 9961 "wired OR"
ALSO 9949, 9963



4 x 1/4 DTμL 9946

RULES

1. Outputs of DTμL gates with 6 kΩ pull-up resistors, 9930, 9946, and 9962 may be tied together for the "wired OR" function. Subtract 1 unit fan-out for each added gate. Subtract 5 fan-outs for 6 added gates.
2. Outputs of DTμL gates with 2 kΩ pull-up resistors, 9949, 9961, and 9963 may be tied together for the "wired OR" function. Subtract 2 units of fan-out for each added gate.
3. Outputs of DTμL 9932 may not be tied together for the "wired OR" function.

DTμL9935
HEX INVERTER
DIODE-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION

The 9935 is an expandable CCSL Hex Inverter. It consists of six DTμL gates without input diodes which are expandable by using external diodes or by using the DTμL 9933 Dual 4-Input Extender element. It is ideal for a wide variety of applications, including one-shot multivibrators, latching circuits, flip-flops, adders, registers, counters, decoders and many more.

FEATURES

- Expandable Inputs
- Wired-OR Capability
- The input/output characteristics provide easy interfacing with Fairchild LPDTμL, TTμL and MSI families (CCSL).
- All ceramic "HERMETIC" 14-pin Dual In-Line and CERPAK packages

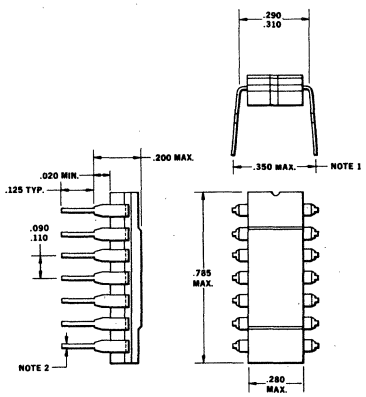
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambrient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +8 V
Input Voltage	-1.5 V to Input Diode Breakdown
Voltage Applied to Outputs (Inputs Low)	-0.5 V to V_{CC} Value
Current Into Output When Output is Low	30 mA

ORDER INFORMATION

Specify U3I99355XX for flat package and U6A99355XX for Dual-In-Line package, where 5XX is 51X for -55°C to +125°C temperature range or 59X for the 0°C to +75°C temperature range.

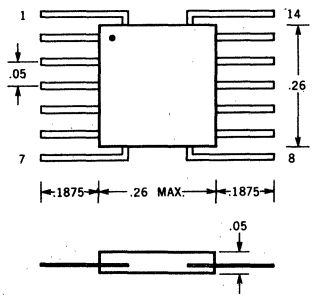
TYPICAL DUAL IN-LINE PACKAGE



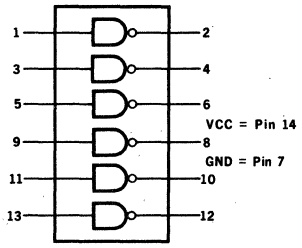
NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

TYPICAL FLAT PACKAGE

TOP VIEW



LOGIC DIAGRAM



FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

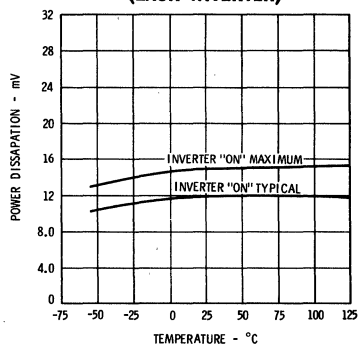
ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTIC	-55°C MIN	-55°C TYP	-55°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+125°C MIN	+125°C TYP	+125°C MAX	UNITS	CONDITIONS & COMMENTS V_{CC} = 5.0 V ±10%
V_{OH}	Output High Voltage	2.6			2.6	3.3		2.5			Volts	V_{CC} = 4.5V, I_{OH} = -180μA V_{IL} = Value indicated on this Table
V_{OL}	Output Low Voltage			0.4		0.3	0.4			0.4	Volts	V_{CC} = 5.5V, I_{OL} = 15 mA V_{CC} = 4.5V, I_{OL} = 12 mA
V_{IH}	Input High Voltage	2.3			2.0			1.8			Volts	Input High Threshold with FD600 on Input
V_{IL}	Input Low Voltage			1.4			1.1			0.8	Volts	Input Low Threshold with FD600 on Input
I_F	Input Load Current			-1.5			-1.5			-1.5	mA	V_{CC} = 5.5V, V_F = 0.4
I_F	Input Load Current			-1.2			-1.2			-1.2	mA	V_{CC} = 4.5V, V_F = 0.4
t_{pd+}	Turn-Off Delay				25	65	80				ns	SEE Figure. 4
t_{pd-}	Turn-On Delay				10	30	40				ns	SEE Figure 4

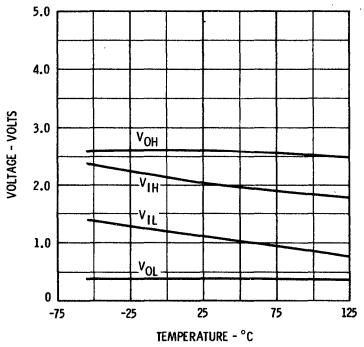
SYMBOL	CHARACTERISTIC	0°C MIN	0°C TYP	0°C MAX	25°C MIN	25°C TYP	25°C MAX	75°C MIN	75°C TYP	75°C MAX	UNITS	CONDITIONS & COMMENTS V_{CC} = 5.0 V ±5%
V_{OH}	Output High Voltage	2.6			2.6			2.5			Volts	V_{CC} = 4.75, I_{OH} = -180μA V_{IL} = Value indicated on this Table
V_{OL}	Output Low Voltage			0.45			0.45			0.45	Volts	V_{CC} = 5.25V, I_{OL} = 15.2 mA V_{CC} = 4.75V, I_{OL} = 13.3 mA
V_{IH}	Input High Voltage	2.1			2.0			1.85			Volts	Input High Threshold with FD600 on Input
V_{IL}	Input Low Voltage			1.2			1.1			0.95	Volts	Input Low Threshold with FD600 on Input
I_F	Input Load Current			-1.52			-1.52			-1.52	mA	V_{CC} = 5.25V, V_F = 0.45
I_F	Input Load Current			-1.33			-1.33			-1.33	mA	V_{CC} = 4.75V, V_F = 0.45
t_{pd+}	Turn-Off Delay				25	65	80				ns	SEE FIGURE 4
t_{pd-}	Turn-On Delay				10	30	40				ns	SEE FIGURE 4

CURVES FOR −55°C TO +125°C TEMPERATURE RANGE

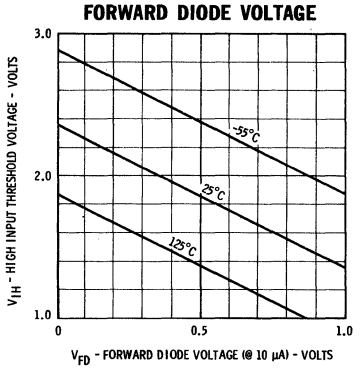
WORST CASE POWER DISSIPATION VERSUS TEMPERATURE (EACH INVERTER)



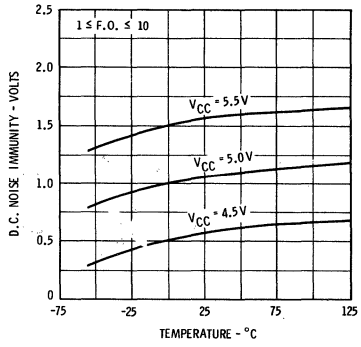
WORST CASE OPERATING VOLTAGE CHARACTERISTICS



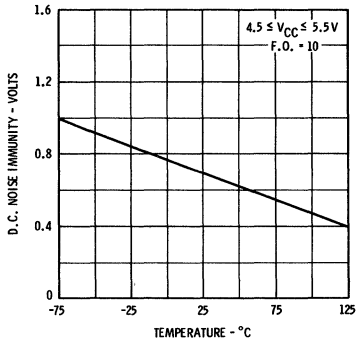
V_{IH} THRESHOLD VERSUS FORWARD DIODE VOLTAGE



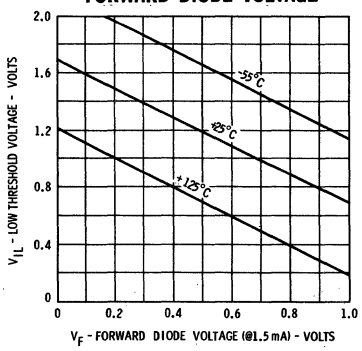
WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS TEMPERATURE



WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS TEMPERATURE

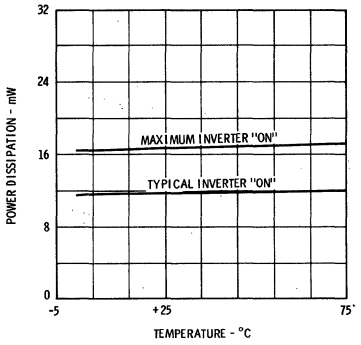


V_{IL} THRESHOLD VERSUS FORWARD DIODE VOLTAGE

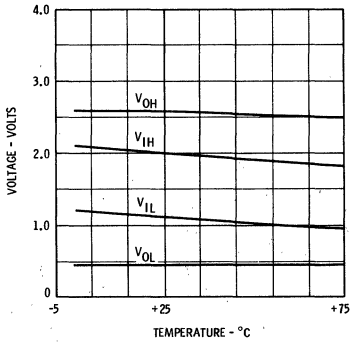


CURVES FOR 0°C TO +75°C TEMPERATURE RANGE

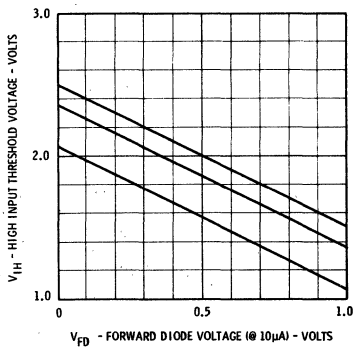
WORST CASE POWER DISSIPATION VERSUS TEMPERATURE (PER INVERTER)



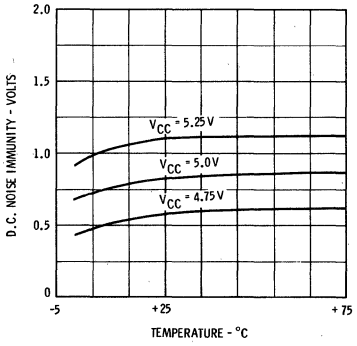
WORST CASE OPERATING VOLTAGE CHARACTERISTICS



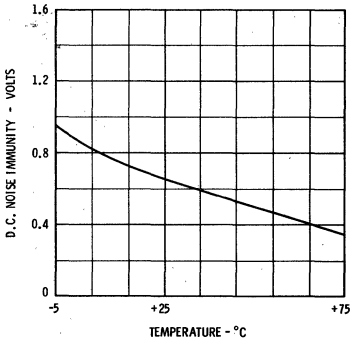
V_{IH} THRESHOLD VERSUS FORWARD DIODE VOLTAGE



WORST CASE HIGH LEVEL NOISE IMMUNITY



WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS TEMPERATURE



V_{IL} THRESHOLD VERSUS FORWARD DIODE VOLTAGE

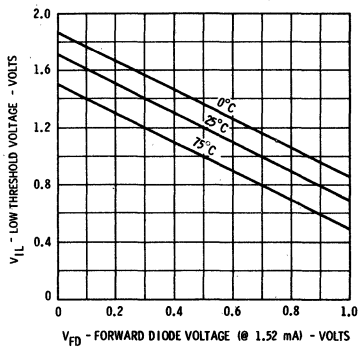


FIG. 1

SCHEMATIC DIAGRAM (ONE INVERTER ONLY)

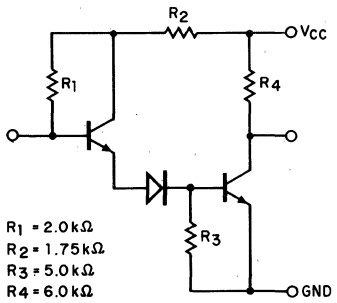


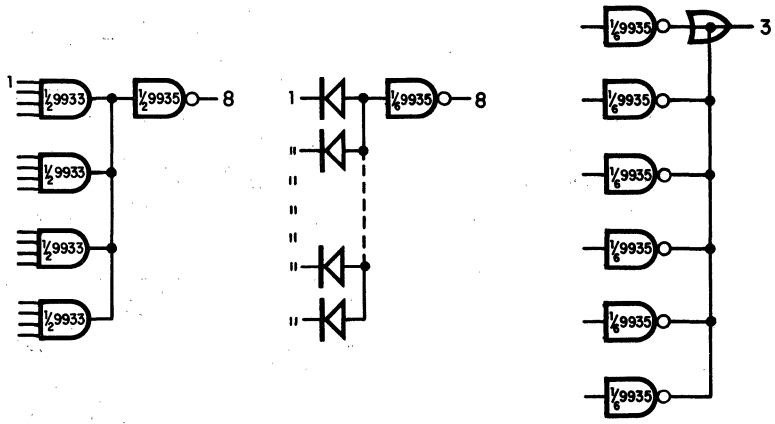
FIG. 2

LOADING RULES

OUTPUT STATE	FANOUT 51X	59X
HIGH	10	10
LOW	10	10

FIG. 3

RULES FOR INPUT EXPANSION AND "WIRED OR" CONNECTION



6 x 1/6 9935 "WIRED OR" For the "WIRED OR" function - Subtract 1 unit fan-out for each added gate. Subtract 5 fan-outs for 6 added gates.

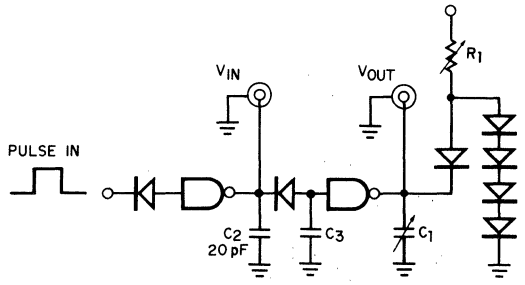
EXPANSION OF INPUTS

Typical input capacitance of the 9933 is 2.0 pF and output capacitance is 5.0 pF. All wiring should be kept as possible to minimize effects of distributed capacitance on circuit performance.

Use FD600 or equivalent expansion.

FIG. 4

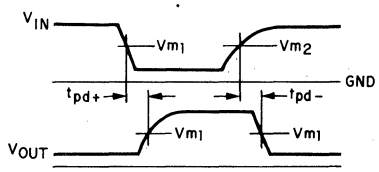
SWITCHING TIME TEST CIRCUIT



Diodes are FD600

	tpd+	tpd-
R1	3.9k	400Ω
C1	30pF	50pF
C2	20pF	20pF
C3	5 pF	5 pF

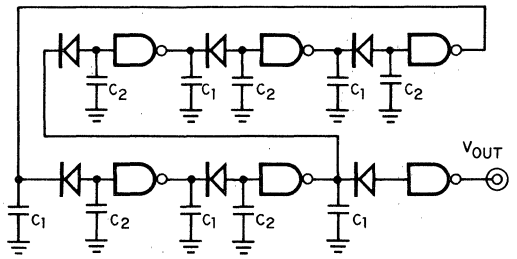
(INCLUDES JIG & PROBE CAPACITANCE)



TEMP.	Vm1 (VOLTS)	Vm2 (VOLTS)
-55°C	1.7	1.5
+25°C	1.5	1.3
+125°C	1.3	1.1

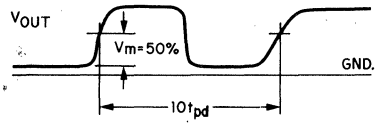
FIG. 5

RING CIRCUIT FOR MEASURING AVERAGE PROPOGATION DELAY

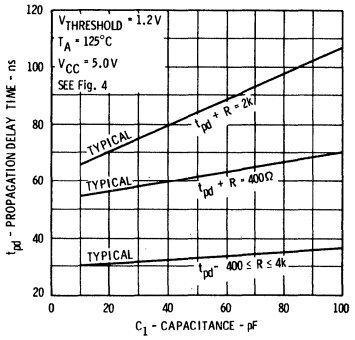


C1 = 30 pF
C2 = 5pF
(INCLUDES JIG & PROBE CAPACITANCE)

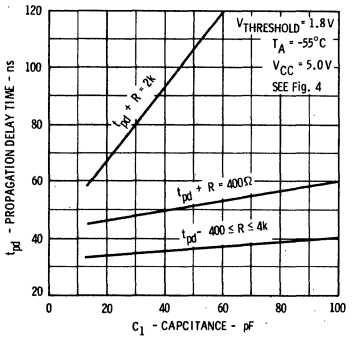
Diodes are FD600



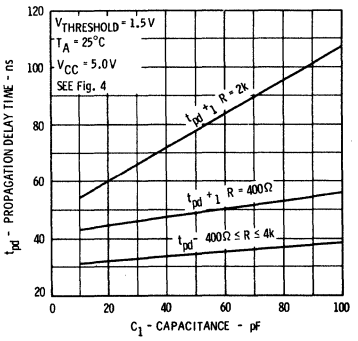
PROPAGATION DELAY VERSUS CAPACITANCE AT +125°C



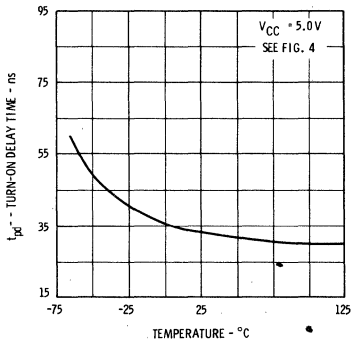
PROPAGATION DELAY VERSUS CAPACITANCE AT +25°C



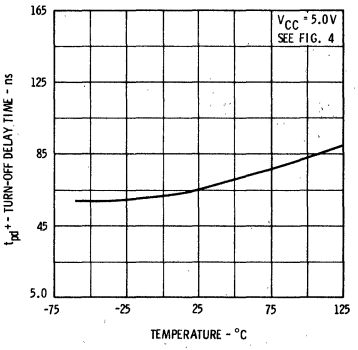
PROPAGATION DELAY VERSUS CAPACITANCE AT —55°C



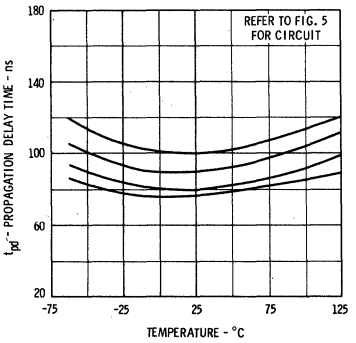
TYPICAL TURN-ON DELAY (t_{pd-}) VERSUS TEMPERATURE



TYPICAL TURN-OFF DELAY (t_{pd+}) VERSUS TEMPERATURE



MAXIMUM PROPAGATION DELAY VERSUS TEMPERATURE



FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

DTμL 9941 • DTμL 9951
MONOSTABLE MULTIVIBRATORS

DIODE-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS (TEMPERATURE RANGE: −55°C to 125°C)

A FAIRCHILD *COMPATIBLE CURRENT SINKING LOGIC* PRODUCT

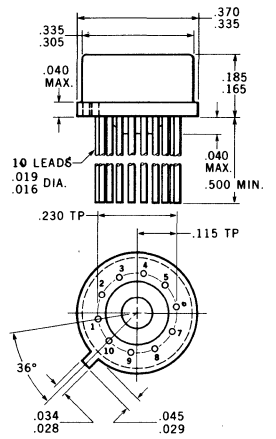
GENERAL DESCRIPTION — The DTμL 9941 and DTμL 9951 Monostable Multivibrators are monolithic silicon epitaxial integrated circuits for use with Fairchild Diode-Transistor Micrologic® Integrated Circuits or any other similar DTL logic elements. They provide complementary output pulses which are typically 150 ns wide. This pulse width is adjustable by the addition of external discrete passive components.

Both elements are compatible with the Fairchild DTμL Family over the full military temperature range of −55°C to +125°C and with a V_{CC} supply of 4.0 volts to 6.0 volts. They can also drive and be driven by Fairchild μL® Integrated Circuit .

The output pulse width is very stable as either V_{CC} or temperature (or both) is varied when an external timing resistor is used instead of the internal diffused resistor.

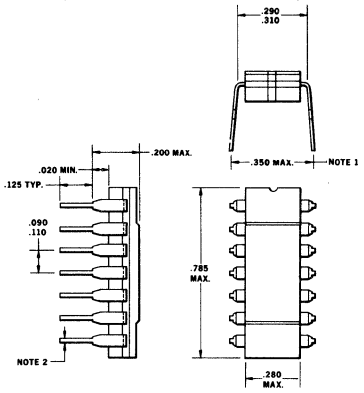
The DTμL 9941 has the same circuit as the DTμL 9951 with the addition of three series diodes from the extender pin (Pin 2) to ground. These diodes give the DTμL 9941 a DC threshold of about 1.5V which gives the circuit a greater than 2.0V noise immunity.

PHYSICAL DIMENSIONS
(In accordance with JEDEC TO−100)



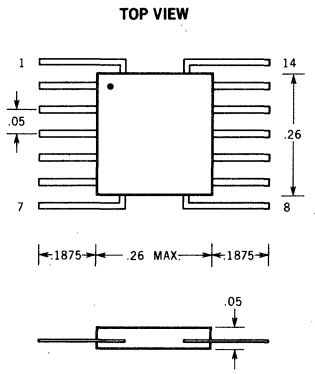
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

TYPICAL DUAL IN-LINE* PACKAGE
(In accordance with JEDEC TO−116)

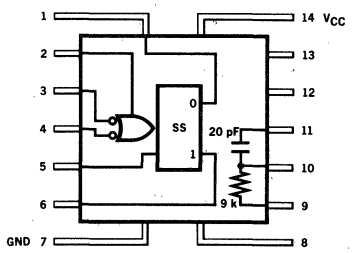


NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

TYPICAL FLAT PACKAGE



CONNECTION DIAGRAM

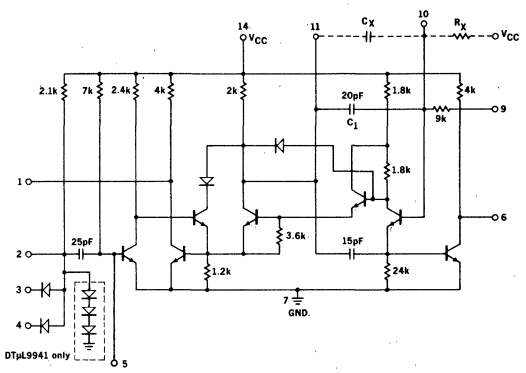


(Top View)

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Supply Voltage (V_{CC}) −55°C to +125°C, continuous:	+8.0 Volts
Supply Voltage (V_{CC}), pulsed, <1 second:	+12 Volts
Output Current, into outputs	50 mA
Current into Pin 10	5.0 mA
Input Forward Current	−10 mA
Input Reverse Current	1.0 mA
Operating Temperature	−55°C to +125°C
Storage Temperature	−65°C to +150°C

SCHEMATIC DIAGRAM



*Fairchild Patent Pending

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

TEST SEQUENCE

FORCING FUNCTIONS

Test No.	CERPAK Pin no.: / TO-100 Pin no.:	5	1 / 7	2 / 8	3 / 9	4 / -	6 / 10	7 / 1	9 / 2	10 / 3	11 / 4	14 / 6	Note 1 Sense	Limits Min.	Limits Max.
1				V_F				GND				V_{CCH}	I_2	$.5\ I_F$	
2					V_F	V_R		GND				V_{CCH}	I_3	$.5\ I_F$	$2\ I_F$
3	Note 2				V_R	V_F		GND				V_{CCH}	I_4	$.5\ I_F$	$2\ I_F$
4								GND			V_F	V_{CCH}	I_{11}	$.5\ I_F$	
5				GND	V_R			GND				V_{CCH}	I_3		I_R
6	Note 2			GND		V_R		GND				V_{CCH}	I_4		I_R
7			I_{OL}					GND		GND		V_{CCL}	V_1		V_{OL}
8		GND						GND	V_{CCL}			V_{CCL}	V_1		V_{OL}
9							I_{OL}	GND	V_{CCL}			V_{CCL}	V_6		V_{OL}
10			I_{OH}	GND				GND	V_{CCL}			V_{CCL}	V_1	V_{OH}	
11							I_{OH}	GND		GND		V_{CCL}	V_6	V_{OH}	
12								GND	V_{CCH}	GND		V_{CCH}	I_9	I_{9K}	I_{9K}
13	*				GND	GND		GND	V_{PD}			V_{PD}	$I_9 + I_{14}$		I_{PDL}
14					GND	GND		GND				V_{MAX}	I_{14}		I_{MAX}
15								GND	V_{CCH}			V_{CCH}	V_2	V_{2L}	V_{2H}
16	$t_{pd}-$ Pin 1	See Test Circuit, page 3													50 ns
17	$t_{pd}+$ Pin 6	See Test Circuit, page 3													50 ns
18	Pulse width Pin 1 (DTμL9951)	See Test Circuit, page 3												90	220 ns
19	Pulse width Pin 6 (DTμL9951)	See Test Circuit, page 3												70	160 ns
20	Pulse width Pin 1 (DTμL9941)													90	330 ns
21	Pulse width Pin 6 (DTμL9941)													70	270 ns

TABLE OF FORCING CONDITIONS

		−55°C	25°C	+125°C
V_{CCH}	Volts	5.5	5.5	5.5
V_{CCL}	Volts	4.5	4.5	4.5
V_{PD}	Volts		5.0	
V_{MAX}	Volts		8.0	
V_R	Volts		4.0	
V_F	Volts	0.0	0.0	0.0
I_{OL}	mA	15.0	15.0	14.0
I_{OH}	mA	−.18	−.18	−.18

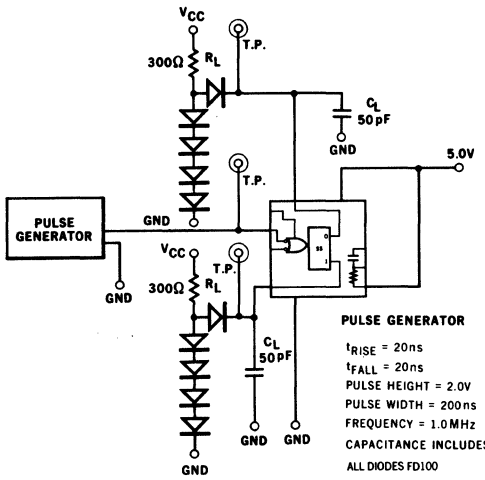
TABLE OF TEST LIMITS

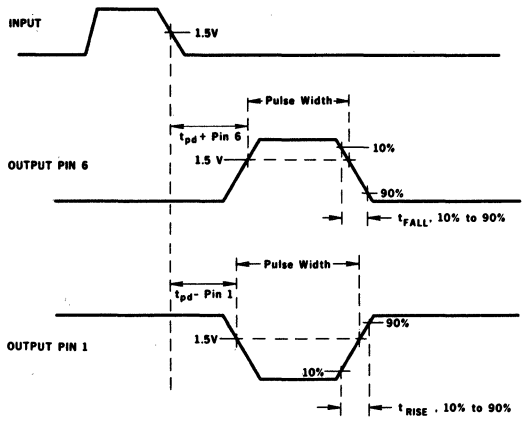
		−55°C Min.	−55°C Max.	25°C Min.	25°C Max.	+125°C Min.	+125°C Max.
$.51_F$	mA	−.80		−.80		−.75	
21_F	mA		−3.20		−3.20		−3.0
I_R	μA				5.0		10.0
V_{OL}	Volts		.40		.40		.45
V_{OH}	Volts	2.5		2.5		2.5	
I_{9K}	mA			.50	.75		
I_{PDL}	mA				9.0		
I_{MAX}	mA				22.0		
V_{2H}(9951)	Volts			5.0			
V_{2L}(9941)	Volts				2.5		

PURCHASING INFORMATION

To order the elements specify U3IXXX51X for Flat Package, U5FXXXX51X for TO-100 and U6AXXXX51X for Dual-In-Line* package (TO-116) where XXXX is the four-digit number denoting the specific element desired.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

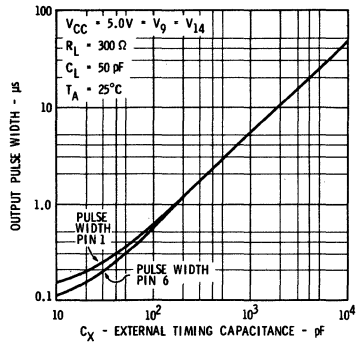




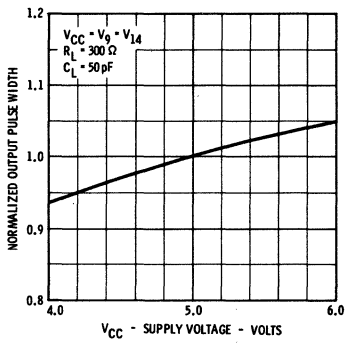
TIMING CHARACTERISTICS

(Test circuit above is used with appropriate modifications where necessary)

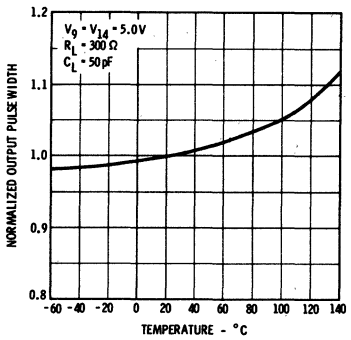
OUTPUT PULSE WIDTH VERSUS EXTERNAL TIMING CAPACITANCE C_X



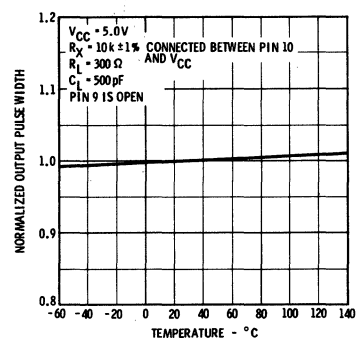
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



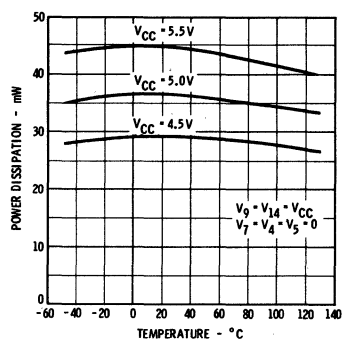
NORMALIZED OUTPUT PULSE WIDTH VERSUS TEMPERATURE



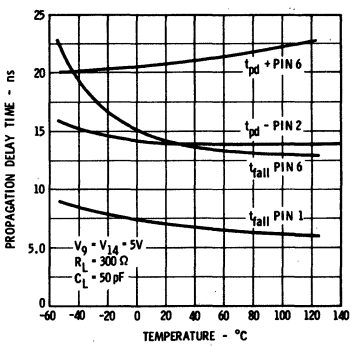
NORMALIZED OUTPUT PULSE WIDTH VERSUS TEMPERATURE USING EXTERNAL TIMING RESISTOR R_X



TYPICAL POWER DISSIPATION VERSUS TEMPERATURE



SWITCHING TIMES VERSUS TEMPERATURE



RULES FOR USE OF DTμL 9941 AND DTμL 9951

1. With Pin 9 connected to V_{CC} and no external capacitor (C_x), the output pulse width is approximately 150 ns.

2. With Pin 9 connected to V_{CC} and an external capacitor (C_x) connected between Pins 10 and 11, the output pulse width (T) is: $T \approx 4.5\ (C_x + 20)$ with C_x in pF and T in ns.

3. For improved pulse width control, Pin 9 is left open and a stable external resistor (R_x) of 9 kΩ minimum to 15 kΩ maximum is connected from Pin 10 to V_{CC}. The output pulse width is given by the expression: $T \approx 0.5R_x\ (C_x + 20)$ with R_x in kΩ, C_x in pF and T in ns.

4. The output duty cycle (pulse width/period) should not exceed 40%. It may be increased to 50% by adding a 2 kΩ resistor between Pin 11 and V_{CC}. Higher duty cycles are obtainable but the output pulse width and performance are less predictable.

5. The maximum input fall time to trigger: 25 ns for a 1.0 volt swing; 50 ns for a 2.0 volt swing; 100 ns for a 4.0 volt swing.

6. The minimum pulse width at output Pin 1 is approximately 100 ns. This pulse width may be decreased to 50 ns by connecting a 10 kΩ resistor between Pin 5 and V_{CC}.

USE OF DTμL 9941 AND DTμL 9951 WITH MICROLOGIC® INTEGRATED CIRCUITS

The DTμL 9951 may be operated from a V_{CC} supply of 4.0 to 6.6 volts. Operation is essentially independent of output resistive and capacitive loading. The input triggering action is initiated by a negative-going input with an amplitude change of 1.0 volt or more. The DTμL 9941 requires the input to go at least one volt below its 1.5 V threshold.

RTμL and Low Power RTμL outputs can drive the DTμL 9941 and DTμL 9951 inputs, provided the output swing is greater than 1.0 volt. Either of the outputs of the DTμL 9941 and DTμL 9951 can drive RTμL and Low Power RTμL inputs. Fan-out from the DTμL 9941 and DTμL 9951 is 4 RTμL unit loads and 1 Low Power RTμL unit load, for the DTμL 9941 and DTμL 9951 $V_{CC} \geq 4.0$ volts. Use of a resistor of 500Ω to 1kΩ from the DTμL 9941 and DTμL 9951 output to V_{CC} will increase fan-out into Low Power RTμL, or RTμL.

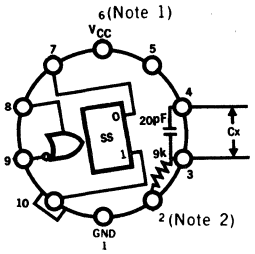
INPUT-OUTPUT LOAD FACTORS TO DTμL FAMILY

Each DTμL 9941 and DTμL 9951 input should be rated at 2 loads.

Each DTμL 9941 and DTμL 9951 output may drive 10 DTμL loads.

For input-output load factors of other DTμL elements, please refer to the DTμL Composite Data Sheet and to the individual DTμL element specifications.

TO-100 TYPE CONNECTION DIAGRAM (Top View)



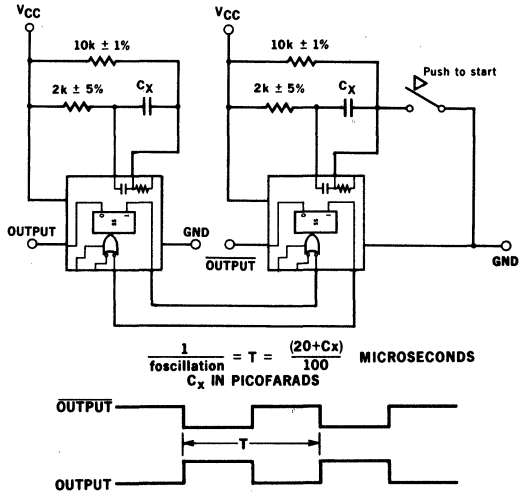
NOTES:

(1) The V_{CC} supply pin is not the tabbed pin on the DTμL 9951.

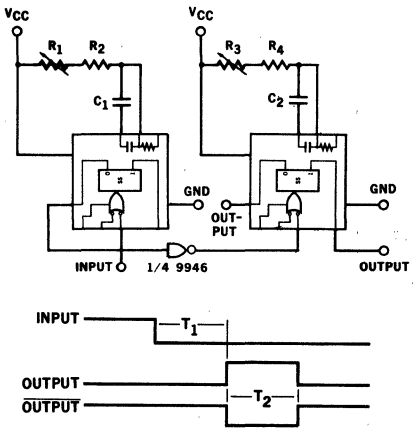
(2) Connect to V_{CC} when R external is not used.

All data in this specification refers to 14-pin Cerpak pin numbers except this outline and the 10-pin reference numbers in the test sequence on Page 2.

STABLE MULTIVIBRATOR



VARIABLE DELAY PULSE GENERATION



Explanation

The input 9951 determines T_1, the time before the initiation of the output pulse. The second or output 9951 determines T_2, the output pulse width.

With $R_2 = 10$ kΩ and R_1 a 5 kΩ potentiometer, T_1 is variable over a range of 2 to 3 and is given by $T_1 \approx 0.5\ (R_1 + R_2)\ (C_1 + 20$ pF).

Similarly, with $R_4 = 10$ kΩ and R_3 a 5 kΩ potentiometer, T_2 is $\approx 0.5\ (R_3 + R_4)\ (C_2 + 20$ pF) and T_2 can be controlled by the potentiometer over a range of 2 to 3 since $10\ k\Omega \leq (R_3 + R_4) \leq 15\ k\Omega$.

A much greater range in T_1 and T_2 is available by varying C_1 and C_2.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

COMPATIBLE CURRENT SINKING LOGIC COMING SOON

Type	Function
4600/4700	TTμL Micromatrix™ Array
4610	Dual Two-Variable Function Generator
TTμL9014	Quad Exclusive OR Gate
MSI9306	BCD Up/Down Counter
MSI9308	Dual 4-Bit Latch
MSI9310	Decade Counter
MSI9311	1-of-16 Decoder
MSI9315	One of Ten Decoder/Driver
MSI9316	Hexidecimal Counter
MSI9317	7-Segment Decoder/Driver
MSI9326	Up/Down Binary Counter
CCSL9644	High Current/High Voltage Driver

Type	Function
Radiation Resistant Devices	
9702	TTL Gate, Quad 2-Input
9703	TTL Gate, Triple 3-Input
9704	TTL Gate, Dual 4-Input
9705	TTL Gate, Dual Exclusive OR
9706	TTL Extender, Dual 4-Input
9707	TTL Gate, Single 8-Input
9709	TTL Buffer, Dual 4-Input
9724	TTL Flip Flop, Single J-K
9745	DTL Flip Flop, R-S Clocked
9969	DTL Gate, Triple 3-Input

4600/4700 — TTμL MICROMATRIX™ ARRAY

The 4600 is a TTμL Micromatrix array consisting of six cells arranged in a 3 x 2 matrix. The cell is made up of two internal and two external gates. Each gate has two 4-way AND's OR'd together and inverted (AOI). The array equivalence is 48 gates.

The 4600 (chip size — 105 x 115) is a monolithic CCSL device. The entire 4600 array (device) is capable of custom interconnection between cells and portions of cells to produce any logic function in any digital logic system. The interconnection, achieved with computer-aided design, is accomplished by using two layers of metallization separated by a dielectric film — the key to LSI.

The 4700 is Fairchild's largest, most complex Micromatrix array. It has twice the gate count of the 4600.

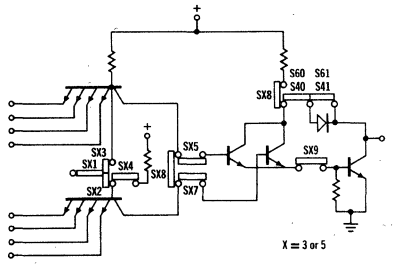
The 4700, a TTμL Micromatrix array, consists of 12 cells arranged in a 3 x 4 matrix. The cell is made up of two internal and two external gates. Each gate has two 4-way AND's OR'd together and inverted (AOI). The array equivalence is 96 gates.

The 4700 (chip size — 145 x 145) is a monolithic CCSL device. The entire 4700 array (device) is capable of custom interconnection between cells and portions of cells to produce any logic function in any digital logic system. The interconnection, achieved with computer-aided design, is accomplished by using two layers of metallization separated by a dielectric film — the key to LSI.

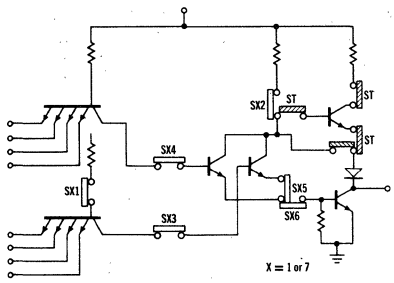
The primary application for the 4600/4700 is in circuits used to interconnect basic system building blocks. These arrays are also used as fundamental building blocks; i.e., standard products. The arrays can be packaged in 16, 24, 36, or 50 pin DIP or Flatpak.

To assist evaluation and full exploitation of the interconnection possibilities of the 4600/4700 array, a special design kit is available from all Fairchild distributors.

4600/4700 - ½ Cell



INTERNAL GATE



EXTERNAL GATE

4610 — DUAL TWO-VARIABLE FUNCTION GENERATOR

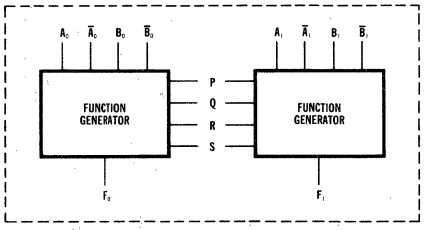
The 4610 consists of two 2-variable function generators, implemented with the 4600 TTμL Micromatrix™ array. Each circuit, controlled by a four-bit control word, is capable of performing any possible Boolean function of two variables.

The output function is defined by the four control inputs and two variables. Outputs are available in active high or low states. The unit is useful for performing logic operations in digital machines, and for self-adapting digital systems.

The 4610 will be available in a 16-pin Dual In-Line package.

FEATURING:

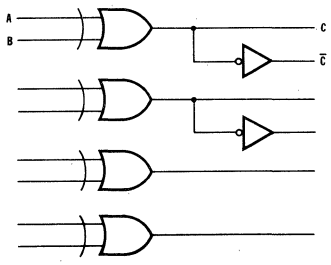
- Active Level Low or High Outputs
- 2-Bit Expansion
- Member 4600 Micromatrix Array Family
- CCSL - Compatible
- Two-Level Metallization



TTμL 9014 QUAD EXCLUSIVE OR GATE

9014 quad exclusive OR gate is a new member of the TTμL family. It produces a high output level when the inputs are complementary. Two of the four exclusive OR gates have complementary outputs for greater system design flexibility.

The 9014 will be available in hermetically sealed 16-pin Dual In-Line and Cerpak packages.



MSI 9306 BCD UP/DOWN COUNTER

The 9306 is a presettable synchronous BCD Up/Down Decade Counter which can be expanded to seven decades without external logic and with no degradation in speed over a single decade.

Presetting is accomplished by synchronously entering, in parallel, the desired data. Counting direction is controlled by a single input. Count-down is enabled by a low input on the C_D terminal and count-up by a high input.

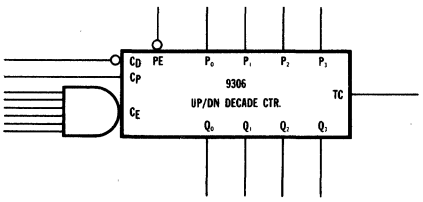
Six enable inputs are provided for terminal carry from all stages in the counter. These inputs may also be used to inhibit the count.

The 9306 will be available in 24-pin Dual In-Line and flat packages.

FEATURING:

- 15 MHz Seven Decade Operation without External Circuitry
- Synchronous Preset
- Single Line Up/Down Control
- Multifunction Capability

COMPATIBLE CURRENT SINKING LOGIC COMING SOON



MSI 9308 DUAL 4-BIT LATCH

The 9308 consists of two 4-bit latch circuits which provide high speed 4-bit parallel gated data storage.

Each 4-bit latch circuit has an active low two-input AND gate which enables the four data inputs. An overriding master reset is also provided on each 4-bit latch circuit.

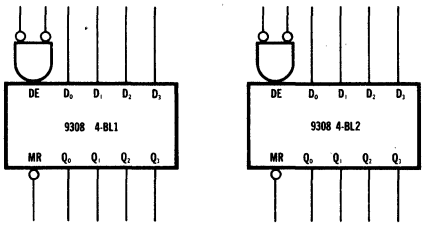
The output circuit incorporates active pull-ups for greater drive capability.

By the use of the enable input, data can be entered into any number of latches from a single bus.

The 9308 will be available in 24-pin Dual In-Line and flat packages.

FEATURING:

- 25 nsec Latch Time
- Data Input Enable
- Master Reset
- Multifunctional Usage



MSI 9310 DECADE COUNTER

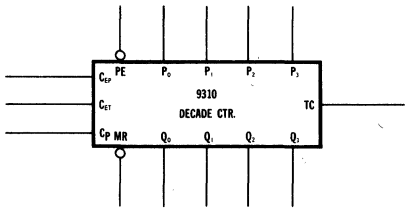
The 9310 is a presettable synchronous BCD Decade Counter which can be expanded to six decades without external logic and with very little degradation in speed over a single decade.

Presetting is accomplished by synchronously entering, in parallel, the desired data. Counting is enabled by HIGHS on the C_{EP} and C_{ET} terminals, which can accept terminal count information from previous decades, thus permitting multiple decades without external logic.

The 9310 will be available in 16-pin Dual In-Line and flat packages.

FEATURING:

- 15 MHz Operation for n Decades
- Synchronous Preset
- Asynchronous Master Reset
- Terminal Count Output
- Count Enable Input



MSI 9311 1-OF-16 DECODER/DEMULTIPLEXER

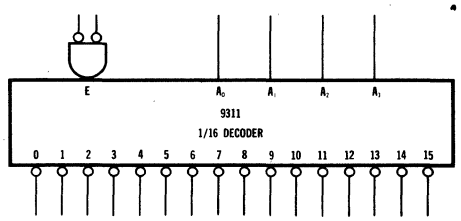
The 9311 is a multi-function decoder, designed to convert four digital inputs into one-of-16 mutually exclusive digital outputs.

The active low outputs are enabled by LOWS on both inputs of the enable AND gate. This enabling feature makes the 9311 suitable for demultiplexing, memory, and control decoding applications.

The 9311 will be available in 24-pin Dual In-Line and flat packages.

FEATURING:

- 20 nsec. Through Delay
- Active Level High
- Input Enable
- Multifunction Capability

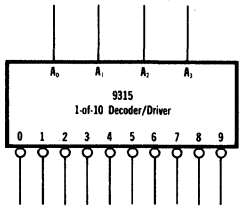


MSI 9315 ONE-OF-TEN DECODER/DRIVER

The 9315 is a CCSL-compatible one-of-ten decoder/driver. The 9315 accepts 8421 BCD code and produces ten mutually exclusive outputs which can directly drive nixie tubes.

The 9315 is similar in operation to the 9960, but the 9315 can be driven from any MSI, TTμL, DTμL, LPDμL circuit.

The 9315 will be available in hermetically sealed 16-pin Dual In-Line and Cerpak packages.



MSI 9316 HEXIDECIMAL COUNTER

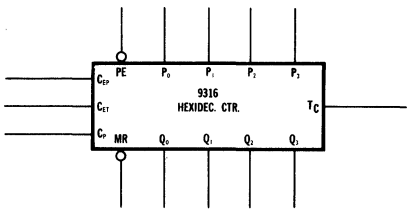
The 9316 is a presettable synchronous binary hexidecimal counter which can be expanded to six stages without external logic and with very little degradation in speed over a single stage.

Presetting is accomplished by synchronously entering, in parallel, the desired data. Counting is enabled by HIGHS on the C_{EP} and C_{ET} terminals, which can accept terminal count information from previous decades, thus permitting multiple stages without external logic.

The 9316 will be available in 16-pin Dual In-Line and flat packages.

FEATURING:

- 15 MHz Operation for N Decades
- Synchronous Preset
- Asynchronous Master Reset
- Terminal Count Output
- Count Enable Input

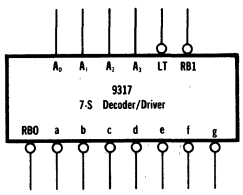


MSI 9317 7-SEGMENT DECODER/DRIVER

The 9317 is a 7-segment decoder/driver designed to convert four inputs of 8421 BCD code into the appropriate output, which will directly drive a seven-segment numerical display. The outputs are active level low and can drive 25-volt incandescent lamps directly.

The 9317 has all the features of the 9307, including automatic ripple blanking for suppression of leading edge zeros, blanking input, lamp intensity, modulation, lamp test facility, and CCSL compatibility.

The 9317 will be available in hermetically sealed 16-pin Dual In-Line and Cerpak packages.



COMPATIBLE CURRENT SINKING LOGIC COMING SOON

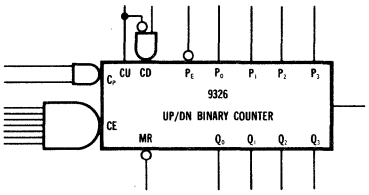
MSI 9326 UP/DOWN BINARY COUNTER

The 9326 is a presettable synchronous hexidecimal up/down counter which can be expanded to eight decades without external logic and with no significant degradation in speed over one decade.

Presetting is accomplished by synchronously entering, in parallel, the desired data. Counting direction is controlled by a single input. Count-down is enabled by a low input on the C_D terminal and count-up by a high input.

Six enable inputs are provided for terminal carry from all stages in the counter. These inputs may also be used to inhibit the count.

The 9326 will be available in 24-pin Dual In-Line and flat packages.

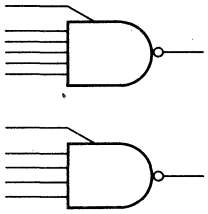


CCSL 9644 — HIGH-CURRENT/HIGH-VOLTAGE DRIVER

The 9644 is a high current driver with CCSL-compatible inputs. The driver operates from CCSL power supply and has an uncommitted collector that will sink 500 mA and hold off 30 volts.

The 9644 is ideal for driving high current peripheral equipment such as lamps, relays, line printers, etc.

The 9644 will be available in the hermetically sealed 16-lead Dual In-Line package.



RADIATION-RESISTANT CCSL COMING SOON

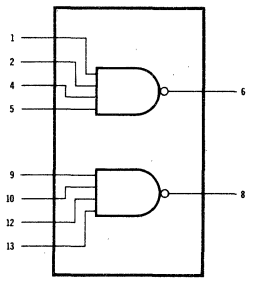
RR CCSL

1. Fairchild will release a radiation resistant CCSL product series during 1968. The devices will incorporate state of the out dielectric isolation construction in conjunction with thin film resistor technologies. The particular RR CCSL products selected will have identical electrical specifications and flatpak pin assignments as their junction isolated counterparts.
2. Those devices to be available are as follows:

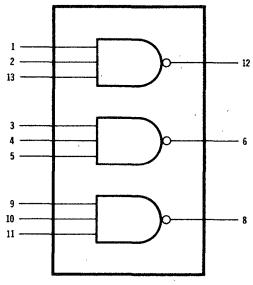
RR CCSL	FUNCTION	CCSL EQUIVALENT
9969	DTL gate, Triple 3 input	9962
9745	DTL flip flop, R-S clocked	9945
9702	TTL gate, Quad 2 input	9002
9724*	TTL flip flop, Single J-K	9024
9704	TTL gate, Dual 4 input	9004
9703	TTL gate, Triple 3 input	9003
9709	TTL buffer, Dual 4 input	9009
9707	TTL gate, Single 8 input	9007
9705	TTL gate, Dual Exclusive OR	9005
9706	TTL extender, Dual 4 input	9006

* Note that the 9724 incorporates 9001 pin assignments.

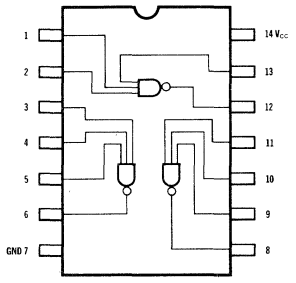
3. For ready review, the logic diagrams are as follows:



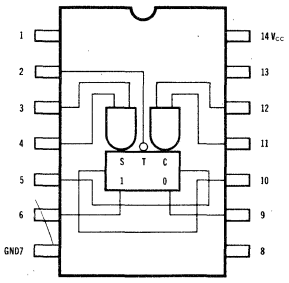
9704



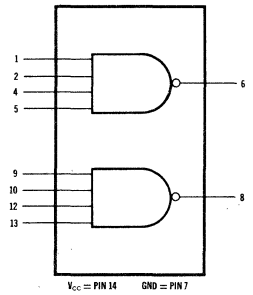
9703



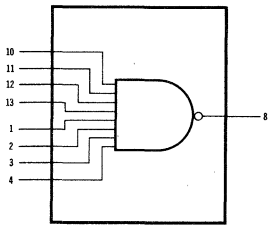
9969



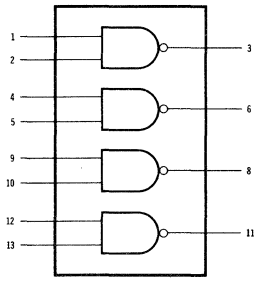
9745



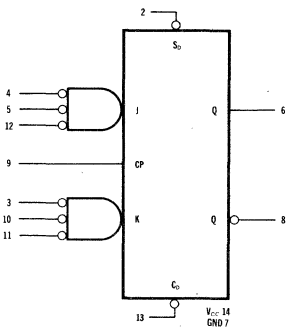
9709



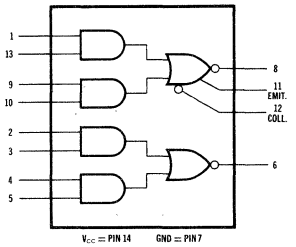
9707



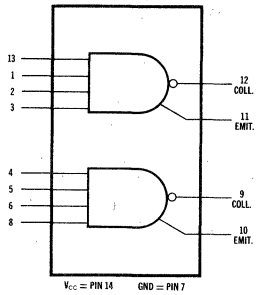
9702



9724



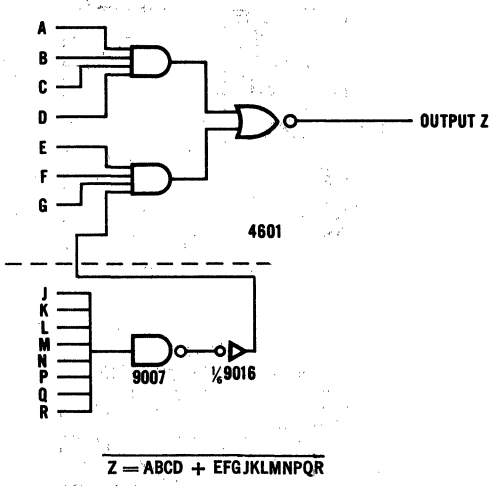
9705



9706

APPLICATIONS (continued)

INPUT "AND" EXPANSION

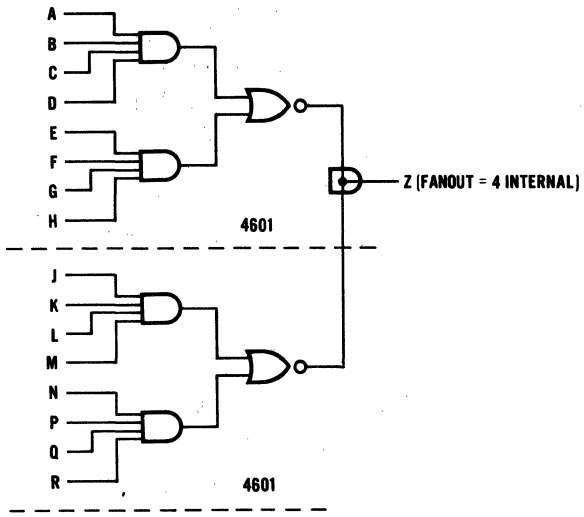


$\overline{Z = ABCD + EFGJKLMNPQR}$

Standard TTμL gates may be used for expansion of "AND" inputs.

*Provision for "AND" expansion is made on the micromatrix array thru "selective bar" options.

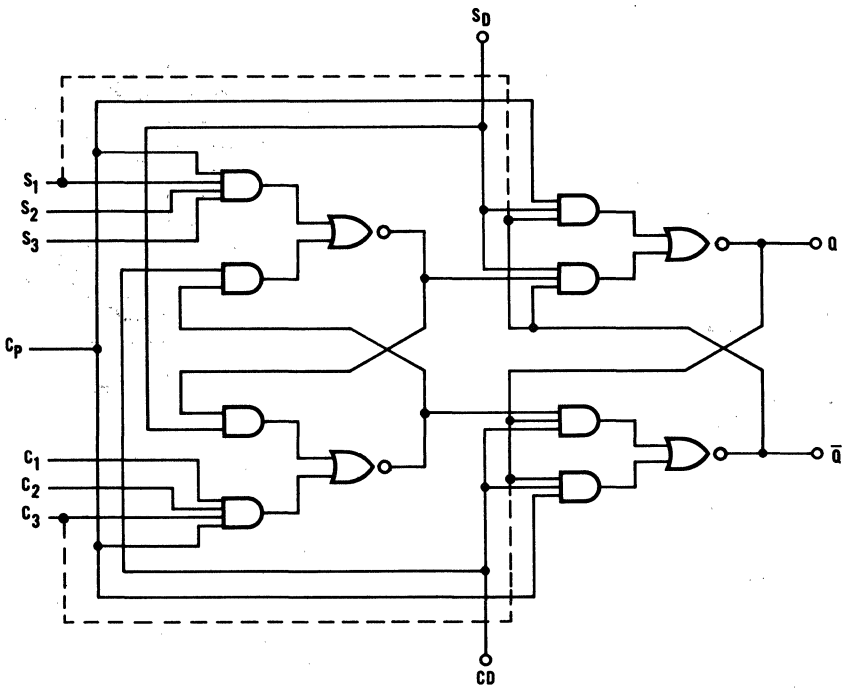
WIRED "AND"



$Z = \overline{[ABCD+EFGH]} \cdot \overline{[JKLM+NPQR]}$

Fig. 4

GENERAL PURPOSE MASTER-SLAVE FLIP-FLOP USING FOUR 4601



For J-K operation, connect as shown in dotted lines. The outputs change on the high to low clock transition.

Fig. 5