In preparing material for this Microcomputer Systems Reference Issue, EDN has spotted seven significant trends in the semiconductor industry. Since many if not all of these developments could have a significant impact on the way you can successfully perform your design functions, let’s examine each in detail.

- **Suppliers of midrange µP’s are compressing whole multichip systems into 1- or 2-chip systems for minimum cost low-end applications.** Examples illustrating this trend include the 3870 version of the F8, the 6801 variant of the 6800, the 6600 outgrowth of the 6500, the 9940 version of the 9900, the Z8 version of the Z80, etc. To this list we might also add the 8048, because although it isn’t a software-compatible version of the B0B0/85 family, it shares much of the same hardware support.

- **Widespread activity is evident from many sources in developing support chips for use with the established µC families.** This trend is particularly true for such midrange families as the 8080 and 6800. EDN predicts the CRT controllers, A/D converters and other peripheral chips will be the most numerous new IC’s introduced in 1978.

- **Growing interest exists in serial I/O buses.** The leader in this innovative effort is Texas Instruments. For many years the firm has used its CRU serial bus for its 990 minicomputer family. Finding the serial bus ideally suited to LSI devices with their limited package pinouts, TI has designed a whole series of serial-bus support chips. National Semiconductor has also favored serial buses (notice that the company brings out flags and jump conditions on Pace and provides a serial shift-register port for SC/MP).

EDN notes that most of the one-chip µC’s scheduled for introduction in ’78 will have similar serial ports. The list includes the 6801, 6600 and...
NAKED MINI products are sold only under volume purchase agreements.

The 4/10 has 64K-word addressing and a MAXI-BUS that allows interfacing with the wide variety of interchangeable memories and I/O controllers in the NAKED MINI 4 family.

What about software? It's one of the 4/10's real strengths. Not only a wide range of software, but also software optimized individually for both development and execution needs.

Available software ranges from the simplest—a memory-based system that runs in as few as 4K words—through the most sophisticated, a full-blown, disk operating system that supports FORTRAN IV, BASIC, PASCAL, and MACRO 4 assembler.

In terms of hardware and software, the 4/10 is fully compatible with its higher performance brothers, the 4/30 and 4/90.

Okay, we've served up our new 4/10 mini with lots of standard and optional hors d'oeuvres. Still hungry for information? Contact Department 1161, NAKED MINI Division, 18651 Von Karman, Irvine, CA 92713, (714) 833-8830, for our new brochure. It's quite a bit of food for thought.
Low-cost systems for all—that's one key effect of the continuing development of tried-and-true μP families and the explosion of support chips for them. Typifying these trends is Intel's 8748 μC. (Photo courtesy Intel Corp.)

Z8. Even some of the support "combo" chips for 2-chip systems will have serial ports. For emphasis, we observe that higher end μC's such as the microNova also use high-performance versions of these serial buses.

- There seems to be a general industry reluctance to risk bringing out a new μC family. Most of the innovations found in this year's μC directories are actually embellishments on such established μC families as the 8080, 6800 or F8, or on such established minicomputer families as the PDP-11 or Nova 1200. Perhaps just too many good μC's are available for any semiconductor supplier to hope at this late date to launch any totally new μC family. And it would cost perhaps $50 million to generate a barrage of product and support sufficient to convince designers that they should learn a totally new machine. (This financial fact of life was one of the reasons that Electronic Arrays abandoned its fine 9002 μP, despite having produced working chips.)

- Several ambitious high-end projects are underway, but they will mostly use existing software. Fairchild's impressive 9940 μP uses IL technology to squeeze a full bipolar-speed Nova 1200 CPU on a 182x189-mil chip. The company is also working on an ECL microprogrammable chip set that will feature such extreme performance features as 20 MHz clock and 20-nsec instruction cycle time. This "super-speed" chip set will be made up of slices of eight bits plus parity and memory. Our sources confirm that the 3859 has been withdrawn.

8000—Developed in Europe, this μP has been quite successful there. However, it's essentially the predecessor of the F8, and, as such, it couldn't be competitive in the USA market once the more advanced Fairchild machine was introduced. Therefore, General Instrument is no longer actively pushing the 8000, although it's listed in the firm's catalog.

SBA—Termed the "Sequential Boolean Analyzer," this 1-bit device from General Instrument is no more a μP than is a PLA. Rather, it's a device designed to implement Boolean equations. Marketing management at GI agreed with EDN's assessment.

825100—This family of bipolar field-programmable gate arrays and logic arrays actually is more related to μP's than the SBA because it performs many μP-like functions and often is used with μP's. However, although the devices handle part of the μP function, they are not classical digital computers, as are all true μP's.

Coming soon: a low-end 8048
As EDN went to press with this issue, we received word that Intel plans to introduce a low-end addition to its 8048 single-chip μC family. Designated the 8021, the new chip will serve automotive, appliance and instrumentation applications.

Slated for sampling by the end of the year and volume production by April of 1978, the 8021 will come in a 28-pin DIP and incorporate 21 I/O lines. Software compatible with the 8048, it will house 1k bytes of ROM and 64 bytes of RAM just like that chip.

The 8021 will have a 10-μsec instruction time. For noncritical applications, a single resistor can replace the crystal for frequency generation. Power requirements can span the 4.5-6.5V range.

Additional features will include zero crossing detection for ac control and time generation, plus two high-current output pins capable of driving 7 mA in audio alarm applications.

Intel sees the device competing with such 4-bit controllers as the Texas Instruments TMS1000 Series and plans to sell it for about $3 in large OEM quantities.
**1-BIT CMOS**

**MC 14500**

One-bit serial controller is suitable for scanning input lines, making decisions and generating control signals. Unit needs external program counter.

**HARDWARE**

Device specs matched to JEDEC B series CMOS, with full 3-18V power supply range. 16-pin DIP. Quiescent current is 5 μA at 5V. Outputs will drive low-power TTL.

**SOFTWARE**

Primitive set of 16 instructions, most execute in one clock cycle (1 μsec).

---

**Legend diagram for EDN's μP files** with the various "information spaces" called out and explained. The information is purposely equally divided into a hardware half and a software half to emphasize the "two-sided" nature of these SP/CP/DC-type products. (SP/CP/DC stands for stored program, general-purpose digital computer.)

**1-BIT CMOS**

**AVAILABILITY:** Now.

**COST:** $7.58 in 100 qty.

**SECOND SOURCE:** None.

**MC 14500**

Motorola Semiconductor Products
3501 Ed Bluestein Blvd.
Austin, TX 78721
Phone (512) 928-2600.

**HARDWARE SUPPORT:** Only sales demonstration units being contemplated.

**SOFTWARE SUPPORT:** None claimed to be needed, since simple instructions permit hand assembly of programs.

---

**NOTES:** Program is counted out by external counter and will repeat endlessly as PC wraps around. PC addresses program ROM (or RAM) which contains both op code for 14500 and addresses for I/O bit selection. Notice "Harvard" architecture with program separate from data and absence of data memory.
housed in a new JEDEC standard, 68-pin leadless package (a requirement because the packages dissipate 5W). Needless to say, Fairchild is not developing this super µC on its own; rather, it's working jointly with a sponsor identified only as a major computer manufacturer. Because the set will be microprogrammable, it will be able to emulate existing software.

EDN observes that Intel and Zilog have been widely rumored to be developing advanced machines that will execute higher level languages like PL/M and PASCAL directly. The word is that they will do so by using stack architectures like that of the Hewlett-Packard HP 3000. Again, the goal is not to launch a new instruction set.

*Most of the innovation in µP's these days is found at the very, very low end. Only down at the extreme low end does EDN's directory reveal any significant willingness on the part of IC makers to innovate with new architectures. Motorola's little CMOS 14500 "controller," Rockwell's MPC (listed in our Support Chip Directory) and GI's continued development of its PIC 1650 are examples of such innovation. Other very low-end innovative µP's include TI's TMS1000, National's MM 5799 Cop family and WD's 1872.

EDN sees three reasons why the semiconductor houses are willing to risk innovation in these devices. First, the software for such µP's is simpler (for example, the Motorola 14500 has only

### For more information

Our "file card" format dictates that the information on each µP be considerably condensed. To obtain additional details on specific processors (or on support chips covered in our µC Support Directory), or to obtain data on µP's manufactured overseas, contact these manufacturers directly. We thank them for providing information vital to the preparation of our µP Directory and µC Support Chip Directory.

<table>
<thead>
<tr>
<th>Company</th>
<th>Address</th>
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<th>Notes</th>
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<tbody>
<tr>
<td>Advanced Micro Devices</td>
<td>901 Thompson Pl. Sunnyvale, CA 94086 (408) 732-2400</td>
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<tr>
<td>Analog Devices</td>
<td>Box 280 Norwood, MA 02062 (617) 329-4700</td>
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<tr>
<td>American Microsystems, Inc.</td>
<td>3800 Homestead Rd. Santa Clara, CA 95051 (408) 246-0300</td>
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<tr>
<td>Burr-Brown</td>
<td>Box 11400 Tucson, AZ 85734 (602) 294-1431</td>
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<td>Data General Corp.</td>
<td>Microcomputer Div. Westboro, MA 01581 (617) 366-8911</td>
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<tr>
<td>EMM Semi</td>
<td>3823 N. 28th Ave. Phoenix, AZ 85017 (408) 263-0202</td>
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<tr>
<td>Fairchild Semiconductor</td>
<td>464 Ellis St. Mt. View, CA 94040 (415) 962-3541</td>
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<tr>
<td>Fairchild Micro Systems</td>
<td>1725 Technology Dr. San Jose, CA 95110 (408) 998-0123</td>
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<td>Ferranti Electric</td>
<td>E. Bethpage Rd. Plainview, NY 11803 (516) 283-8363</td>
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<td>Fujitsu Ltd</td>
<td>6-1 Marunouchi 2 Chome Chiyoda-ku Tokyo, Japan</td>
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<tr>
<td>General Instrument Corp.</td>
<td>Microelectronics Div. 600 W. John St. Hicksville, NY 11802 (516) 733-3000</td>
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<tr>
<td>Harris Semiconductor</td>
<td>Box 883 Melbourne, FL 32901 (305) 727-5407</td>
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<td>Hitachi, Ltd</td>
<td>6-2, 2-Chome Otemachi, Chiyoda-ku Tokyo 100, Japan</td>
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<tr>
<td>Hughes Microelectronics</td>
<td>500 Superior Ave. Newport Beach, CA 92663 (714) 548-0671</td>
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<tr>
<td>Intel Corp.</td>
<td>3005 Bowers Ave. Santa Clara, CA 95051 (408) 987-8080</td>
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<tr>
<td>Intersil, Inc.</td>
<td>10000 N. Tantau Ave. Cupertino, CA 95014 (408) 996-5000</td>
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<tr>
<td>ITT Semiconductors</td>
<td>74 Commerce Way Woburn, MA 01801 (617) 935-7910</td>
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<tr>
<td>Micro Networks Corp.</td>
<td>324 Clark St. Worcester, MA 01606 (617) 852-5400</td>
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<td>Monolithic Memories, Inc.</td>
<td>1165 E. Arques Ave. Sunnyvale, CA 90406 (408) 739-3535</td>
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<tr>
<td>Mostek</td>
<td>1215 W. Crosby Rd. Carrollton, TX 75006 (214) 242-0444</td>
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<td>Motorola Semiconductor</td>
<td>7005 E. McDowell Rd. Phoenix, AZ 85008 (602) 244-6900</td>
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<tr>
<td>Motorola Integrated Ckts. Div.</td>
<td>3510 Ed Bluestein Blvd. Austin, TX 78721 (512) 928-2600</td>
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**Listing continues on pg. 49**
4-BIT MOS

**AVAILABILITY:** Now

**COST:** $5.50 for 4040, $5.00 for 4004 (100 qty in plastic)

**SECOND SOURCE:** National Semiconductor for 4001, 4002, 4004, 4008 and 4009

**HARDWARE**

PMOS LSI family of custom parts powered from single – 15V supply with CPU in 24-pin pkg.

**SOFTWARE**

59 instructions* include all the older 4004 set and are executed in 8 µsec vs. 10.8 µsec cycle time.

**I—DATA MANIPULATION INSTRUCTIONS**

Arithmetic and shift.

BCD arithmetic via BCD correction.

Logicals.*

Compare.*

**II—DATA MOVEMENT INSTRUCTIONS**

Uses GP registers on CPU as pointers to reach memory, taking several steps.

Can reach GP registers directly.

Also has immediate and indirect mode.

I/O on memory chips & shares addresses.

**III—PROGRAM MANIPULATION INSTRUCTIONS**

Two decision instructions, conditional branch and skip-on-zero.

Seven levels of subroutine nesting.*

Software interrupt disable.*

Interrupt with automatic saving and vectoring.*

**IV—PROGRAM STATUS MANIPULATION INSTRUCTIONS**

Can test status via the conditional branch instruction.

**SOFTWARE SUPPORT:** "MAC40" cross-assembler and "Interp/40" 4040/4044 cross-simulator are available on timeshare and for minis. Program library has over 50 programs. No higher-level language planned.

**HARDWARE SUPPORT:** Designer's kit and Intellect 4Mod 4 development system that has resident monitor and peripheral interfaces.

4-BIT MOS

**AVAILABILITY:** Now

**COST:** Under $5 in 25k qty, under $3 at 100k.

**SECOND SOURCE:** Under negotiation.

**HARDWARE**

NMOS, 40-pin DIP, 9V, 234 mW. Has on-chip 7-segment decoder, LED or vacuum-fluorescent drivers, timer that accepts 50/60 Hz for sync to line-frequency controls, and power-on reset circuit. Miltemp version being developed.

**SOFTWARE**

51 single-byte instructions; 4 µsec cycle time. On-chip 1k x 8 mask-programmable ROM, with external expansion capability to 8k. Escapes and dual-use options give designer feel of using more general architecture than calculator.

**SOFTWARE SUPPORT:** Assembler, text editor, real-time debugger, software simulator; floppy disc operating system; self-diagnostics; macroprogram library; applications programs; logic analyzer.

**HARDWARE SUPPORT:** MDC (disk-based CFT terminal with editing, macro and trace capability); software simulator; hardware emulator with PROM sockets; logic analyzer; tester.

4040/4004

4040 is upwards compatible version of widely used 4004, which will still be available. 4040 includes features lacking in 4004 (marked with asterisk).

**SOFTWARE**

59 instructions* include all the older 4004 set and are executed in 8 µsec vs. 10.8 µsec cycle time.

**I—DATA MANIPULATION INSTRUCTIONS**

Arithmetic and shift.

BCD arithmetic via BCD correction.

Logicals.*

Compare.*

**II—DATA MOVEMENT INSTRUCTIONS**

Uses GP registers on CPU as pointers to reach memory, taking several steps.

Can reach GP registers directly.

Also has immediate and indirect mode.

I/O on memory chips & shares addresses.

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Seven levels of subroutine nesting.*

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**SOFTWARE SUPPORT:** "MAC40" cross-assembler and "Interp/40" 4040/4044 cross-simulator are available on timeshare and for minis. Program library has over 50 programs. No higher-level language planned.

**HARDWARE SUPPORT:** Designer's kit and Intellect 4Mod 4 development system that has resident monitor and peripheral interfaces.

S2000

Aimed primarily at appliance, game and timing/control applications, this 1-chip µC interfaces directly to standard or capacitive keyboards, drives displays directly and provides motor control (phase control or trac drive).

**SOFTWARE**

51 single-byte instructions; 4 µsec cycle time. On-chip 1k x 8 mask-programmable ROM, with external expansion capability to 8k. Escapes and dual-use options give designer feel of using more general architecture than calculator.

**SOFTWARE SUPPORT:** Assembler, text editor, real-time debugger, software simulator; floppy disc operating system; self-diagnostics; macroprogram library; applications programs; logic analyzer.

**HARDWARE SUPPORT:** MDC (disk-based CFT terminal with editing, macro and trace capability); software simulator; hardware emulator with PROM sockets; logic analyzer; tester.
16 instructions), and therefore an innovative new part doesn't demand that the user be willing to invest in many months of self-education.

Second, low-end µP's typically need only short (1k bytes or less) application programs. Designers can hand code such short programs if necessary, further cutting down on the support needed.

### Which µC's are the safest bets?

You can obtain criteria (or assessing the "safeness" of a µC family as follows:

- From our µP Directory, determine the number of second sources for a given µP.
- From our µC Systems Directory, gauge the relative popularity of different µP's with board-level systems suppliers.
- From our µC Support Chip Directory, determine the scope of support chips for the various µC families.

Each of these criteria has its strong and weak points and must be used with common sense.

---

**Third, low-end µP's** are typically used in high-volume end applications (because they can sell for just a few dollars in volume). Therefore designers can afford to spend extra time on their hardware and software application. (Actually, in many instances the IC maker's own team performs the application design for the customer, under contract.)

- **Steady progress in CMOS technology could see CMOS µC's finally coming into their own in 1978.** Both Intersil and RCA and their respective second sources say that CMOS EROM's will become available in 1978, not to mention a wider selection of RAM's. EDN's Support Chip Directory points out the growing selection of CMOS auxiliary chips, including A/D converters. Fairchild should share in this CMOS growth with its Macrologic, as should Texas Instruments with its CMOS version of the TMS1000, Motorola with its "nano-P" 14500 and Hewlett-Packard with its advanced MC² (many inside H-P would like to offer MC² as a general product.)

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**EDN NOVEMBER 20, 1977**

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**4-BIT MOS**

**MM5799**

MM5799 is middle of line of calculator-oriented processor system (COPS) family of dedicated controllers. Others are 5782 and 57140.

**SOFTWARE**


**I - DATA MANIPULATION INSTRUCTIONS**

Basic binary BCD-coded instructions.

Individual memory bit manipulation.

Performs right and left shifts and floating point via software.

Includes general-purpose I/O instructions in addition to specialized calculator instructions.

**II - DATA MOVEMENT INSTRUCTIONS**

Versatile output with printer and display interface, including LED and fluorescent. Compatible with 8-bit μP bus for number crunching.

**III - PROGRAM MANIPULATION INSTR'S**

Two-level nesting.

No hardware interrupt.

**IV. PROGRAM STATUS MANIP. INSTR.**

Status flag flip-flops set and reset by switch.

**NOTE:** The 1-chip 5799 is not expandable. However, a 2-chip version (5781 and 5782) provides double the ROM and more RAM and also allows for further memory expansion. Available support chips interface to printers and displays, etc.

**SOFTWARE SUPPORT:** Simulation and assembly programming available on time-sharing networks. Cross-assembler runs on IMP-16P.

**HARDWARE SUPPORT:** Chips without ROM available for hardware emulation of systems with PROM's or RAM's. IMP-16 development system has ROM-simulation capability.

**SOFTWARE SUPPORT:** Cross-assembler on time-sharing network. Text editor, assembler and debug utility on universal assemulator. Tutorial manuals. Regular seminars.

---

**PPS-4/1 FAMILY**

One-chip microprocessor family offers wide range of I/O and several sizes of ROM/RAM. Seven standard models aim at low speed, high volume applications.

**SOFTWARE**

50 unique instructions, most of which execute in one 12.5-μsec cycle.

**I - DATA MANIPULATION INSTRUCTIONS**

Arithmetic and logicals.

BCD with decimal correction instr.

**COMPLEMENT**

**II - DATA MOVEMENT INSTRUCTIONS**

Instructions for moving strings of 4-bit words, so can handle as multiple precision.

Can achieve function of indexing if memory carefully allocated, as several instructions incorporate automatic address modification and tests for loop termination.

**III - PROGRAM MANIPULATION INSTR'S**

Two-level subroutine nesting.

Table look-up function.

Two conditional interrupt test instructions.

**IV. PROGRAM STATUS MANIP. INSTR.**

Bit setting and testing directly in RAM memory.

**NOTE:**

Most packages are 42-pin QIL, but MM75 available in 28-pin DIP and MM76C/D in 52-Pin QIL. (76C has counters; 76D incorporates 12-bit A/D.)

**SOFTWARE SUPPORT:** Cross-assembler on time-sharing network. Text editor, assembler and debug utility on universal assemulator. Tutorial manuals. Regular seminars.

---

**HARDWARE SUPPORT:** Stand-alone development system, XPO-1, costs $495, contains PPS-4/1's with either utility/debug monitors or assembler/line editors. Socket brings out ROM address lines. Personality board for universal development system.
**4-BIT MOS**

**AVAILABLE:** Now.

**COST:** $18.15 for PPS-4 in 100 qty; $5-$10 for PPS-4/2 set in 100 qty.

**SECOND SOURCE:** None. (National Semiconductor not active.)

**PPS-4, PPS-4/2**

Self-sufficient system with expansion capability intended to implement full SPI/GP/DC at lowest cost in high volume. Substantial use history. (See PPS-4/1 for single-chip version.)

**SOFTWARE:**

50 unique instructions, most of which execute in one 5-μsec cycle.

**I—DATA MANIPULATION INSTRUCTIONS**

Arithmetic and logicals.

BCD with decimal correction instr.

**II—DATA MOVEMENT INSTRUCTIONS**

Instructions for moving strings of 4-bit words, so can handle as “calculator-length” BCD-coded decimal numbers.

**III—PROGRAM MANIPULATION INSTR’S**

Can achieve function of indexing if memory carefully allocated, as several instructions incorporate automatic address modification and tests for loop termination.

Can implement subroutine return address stack in RAM for unlimited nesting. PPS-4 has interrupt.

**IV—PROGRAM STATUS MANIP. INSTR.**

Carry and two FF’s that are software accessible for setting and testing.

**HARDWARE**

PMOS LSI powered from 17V supply; 42-pin pkg. PPS-4/2 has clock on CPU. PPS-4 has interrupt.

**SOFTWARE SUPPORT:** Cross-assembler on time-sharing network. Text editor, assembler, and debug utility on universal assemulator. Tutorial manuals. Regular seminars.

**HARDWARE SUPPORT:** Prototype board. Personality boards for universal assemulator with System Analysis Module (SAM).

**TMS—1000/1200 (1100/1300)**

Texas Instruments, Inc.

Houston, TX 77001

Phone (713) 494-5115

**AVAILABLE:** Now.

**COST:** As low as $2 in 100k volume.

**SECOND SOURCE:** None for PMOS chip; Motorola possible for CMOS version.

**HARDWARE**

PMOS, 15V, 28- and 40-pin DIPs. Both T.I. and Motorola are developing CMOS versions.

**SOFTWARE**

43 fixed instruction set can be augmented by microcoding the decode PLA. This allows compacting oversized programs into limited on-chip ROM. 24-μsec instruction cycle.

**I—DATA MANIPULATION INSTRUCTIONS**

Binary two's-complement arithmetic with decimal operations done by test and correction instructions.

Logical and comparison and bit tests.

**II—DATA MOVEMENT INSTRUCTIONS**

Has implied, immediate and direct addressing modes, with separate for program ROM, data RAM and I/O input and I/O output. Can switch output format by status bit (therefore could have both 7-segment and BCD output formats).

**III—PROGRAM MANIPULATION INSTR’S**

One-level subroutine calls. Branches on test of status bit. Status bit serves both for carry and for indicating result of comparisons.

**IV—PROGRAM STATUS MANIP. INSTR.**

None.

**HARDWARE SUPPORT:** SE-1/TMS-1099 ($26.20) and SE-2/TMS-1098 ($35.63) provides access to ROM connections for development. Prototype boards. “AMPL” development system permits assembly, simulation and (soon) in-circuit emulation.

**SOFTWARE SUPPORT:** Assembler and simulator on 3 timeshare networks. High-level-language compiler (TML) and variety of utility programs. Four-day training course at Houston costs $500.
Single, dual, and triple output supplies having output ratings from 1 to 28 volts; from 30 ma to 60 amps. A choice of performance levels, with regulation ranging from ±0.005% to ±0.5%. Many provide dual and triple isolated outputs, matched or dissimilar, in both standard and user-selectable combinations. Others have balanced, tracking outputs.

The variety of shape factors and the mounting versatility of these supplies provide easy answers to mechanical layout problems. Miniaturized models are available for either PCB mounting or, with screw terminals, for chassis mounting. Narrow profile units fit into thin spaces. Metered benchtop supplies are handy sources of power for experimental circuitry. Plug-in modules mount in seconds.

Ask for a copy of our full color, 28-page brochure. It contains complete specifications, outline drawings, prices, and — just as important — it also details our guarantee to ship within 3 days after receiving your order.
4-BIT MOS

**AVAILABILITY:** Now (mask in 6 weeks).
**COST:** $8.55 in 1000 qty with $1500 mask charge. (Total cost will be well under $5 in 100k qty in 1978).

**SECOND SOURCE:** Under negotiation.

**HARDWARE**
PMOS LSI powered from single 12V supply. 40-pin package, on-chip clock. TTL compatible, mask programmable.

**SOFTWARE**
37 instructions, with most executed in 6.25 μsec. Instructions are designed for control applications and do not require computer-programming techniques to use.

I—DATA MANIPULATION INSTRUCTIONS
Binary or BCD arithmetic under program control.
Multi-digit arithmetic operations are programmed in two words instead of a subroutine.

II—DATA MOVEMENT INSTRUCTIONS
Data movement, AND & OR instructions provide for easy movement of data to register files and direct setting and resetting of bits in output registers.

III—PROGRAM MANIPULATION INSTR'S
One-level subroutine call. 16-way conditional jumps and unconditional jump. Special unconditional jump provides vectored addressing.

IV—PROGRAM STATUS MANIP. INSTR.
Binary-BCD set/reset, reset latched inputs.

**SOFTWARE SUPPORT:** Cross-assembler and simulator available for PDP-11 disc-based systems. Alternatively, W.D. will contract to do in-house programming and deliver board-level solution.

8-BIT MOS

**AVAILABILITY:** Now.
**COST:** $9.95 for CPU in 100 qty.
**SECOND SOURCE:** Mostek, Motorola and SGS/ATES, licensed.

**HARDWARE**
NMOS, isoplanar, 40-pin DIP. 5V at 80 mA plus 12V at 25 mA. Minimum system contains 3850 CPU plus one or more program storage units (3851/56,757 PSU's) that can hold up to 2k bytes.

**SOFTWARE**
Unique instruction set to go with unusual architecture. Most of 76 basic instructions execute in 2 μsec.

I—DATA MANIPULATION INSTRUCTIONS
Arithmetic and logicals. Decrement any scratch pad register. BCD arithmetic. Built-in timer functions distributed in all chips and tied to interrupt.

II—DATA MOVEMENT INSTRUCTIONS
Most instructions operate on GP registers in CPU scratchpad with 1-byte codes. But 1-byte code can reach only first 12 of 64 CPU GP registers, and indirect addressing via "ISAR" register needed to reach the rest.

III—PROGRAM MANIPULATION INSTR'S
"Data Counter" registers can perform pseudo indexing. Subroutines save by hardware for first level and by software-directed movements for deeper levels. Novel interrupt scheme whereby each of system chips is in daisy chain.

IV—PROGRAM STATUS MANIP. INSTR.
5-bit status registers (sign, carry, overflow, zero and interrupt enable) have instructions to store.

**SOFTWARE SUPPORT:** Fortran-IV cross assembler runs on 16-bit minis. Assembler, editor and debugger in resident development system. ROM-based FAIRBUG has load, dump, display and store features.
PRESENTING VMOS FROM A BIG TIME PRODUCER.

With a major producer like Fairchild behind it, you know VMOS is going to be a big star someday. So remember the name: Enhancement Mode Power Vertical Mosfet. Stagename: Fairchild VMOS.

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For more information, Circle No. 31
8-BIT MOS

**AVAILABILITY:** Now.

**COST:** Masked-ROM versions (8048/8041) will sell at $5 in high volumes. EPROM versions are $245 for the 8748, $250 for the 8741.

**SECOND SOURCE:** AMD, Signetics and NEC, licensed, mask exchange.

**HARDWARE**

NMOS, silicon gate, +5V operation, 40-pin pkg. Compatible with all 8080-type peripherals.

**SOFTWARE**

Over 90 instructions. Most single cycle. Cycle time ~ 2.5 μsec.

Takes best instructions of 4004 and 8080, but not 8080 compatible.

**I—DATA MANIPULATION INSTRUCTIONS**

Arithmetic and logic.

Bit set and reset.

Two working banks of 8-bit registers.

**II—DATA MOVEMENT INSTRUCTIONS**

Both internal and external RAM are fully accessible by instruction set. Direct and indirect data fetches.

**III—PROGRAM MANIPULATION INSTR'S**

Decrement and skip if zero.

Over 20 conditional branches.

An 8-level stack with expansion capability.

Two vectored interrupts.

Two programmable flag bits under software control.

**IV—PROGRAM STATUS MANIP. INSTR.**

Status word is fully accessible and is stored in the stack.

**SOFTWARE SUPPORT:** Macroassembler on floppy disc or paper tape. Resident text editor in MDS development system. Debug software in ICE-48 in-circuit emulator. "Insite" program library contains over 350 programs.

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EDN NOVEMBER 20, 1977

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We've lead the way in MOS/LSI data communications circuits with proprietary products like our COM 5025 Multi-Protocol Synchronous Receiver/Transmitter and our COM 2017 and COM 2502 Universal Asynchronous Receiver/Transmitter plus others. Now we're second sourcing Western Digital's UC 1671 ASTRO with our new GOM 1671.

It's a software responsive device capable of handling complex communications formats in a variety of systems applications.

Like our COM 5025, and our recently announced CRT 5027, the new COM 1671 ASTRO has high speed, and high density n-channel Coplamos® technology in a 40 lead ceramic DIP.

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We make custom LSIs too.

SMC's custom circuit department has helped many medium-volume users with the design and production of custom devices. Applications personnel are available to discuss the tradeoffs involved in custom MOS/LSI design. The solution may include either standard or custom circuits or a combination of both.

For standard or custom LSI come to Standard Microsystems Corp. No one knows more about building data communications circuits than us.
8-BIT MOS

**850X, 851X**

Somewhat similar to 6800, but not software compatible. 850X µPs have on-chip oscillator & clock driver, while 851X machines (aimed primarily at multi-processor systems) require 2-phase, high-level clock.

**HARDWARE**

NMOS, silicon gate. +5V, 250mW. Versions are available that can run at up to 4 MHz clock rates (250 nsec cycle time).

**SOFTWARE**

Fifty-seven instructions execute in 2.5 μsec, typ, 13 powerful addressing modes.

**I-DATA MANIPULATION INSTRUCTIONS**

Arithmetic and logical. Decimal mode via control bit in status register. Can operate on locations in memory space (which can be either RAM or I/O ports).

**II-DATA MOVEMENT INSTRUCTIONS**

True indexed addressing, though index offset limited to 8 bits in two CPU registers, X and Y. Short-form addressing to zero page. Has two sophisticated indirect indexed and indexed indirect instructions for handling tables.

**III-PROGRAM MANIPULATION INSTR’S**

Conditional branches with signed relative addresses. Non-maskable and/or maskable interrupt, depending on model. Stack pointer for implementing 256-byte LIFO in external RAM.

**IV-PROGRAM STATUS MANIP. INSTR.**

Push and pull status register from memory stack. Set and clear carry, decimal mode and interrupt bits. (8502 & 8512 have external input to one status bit, useful for handshaking with peripherals.)

**SOFTWARE SUPPORT:** All software packages for 650X family.

**8-BIT MOS**

**MCS-660X (6500/1)**

Single-chip 6500X-type µC’s. Rockwell’s 6600/1 will be essentially same as 650X, while MOS Technology’s 6600X will be more powerful machine.

**HARDWARE SUPPORT:** Special 64-pin device for prototyping. 660X’s ROM can carry “KIM” or “TIM” monitors, so users can develop stand-alone prototyping stations. Besides 650X parallel-bus support chips, 660X will have serial-bus peripheral devices.

**SOFTWARE SUPPORT:** All software packages for 650X family.
Our new 5100/5101A calibrators can calibrate VTVMs, VOMs, 3½-, 4½- and most 5½-digit DMMs around, in a fraction of the time it takes you now! (It's a cal lab in a box! All at an average price under $9,000.)

For $10,000 to $15,000, you could invest in an intricate maze of instruments that takes a wizard to operate. Or, you could fill a room with computer-based hardware and expensive talent. About $100,000 worth.

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We've designed the new 5100A and 5101A for production test, QA and cal lab applications that need large system flexibility at a fraction of large system cost.

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Both models have a friendly calculator-type keyboard. And, both have the RS232 or IEEE 488 system options you want for remote operation or hard-copy printouts of results.

Call (800) 426-0361, toll free. Ask for complete technical specs or the location of your local Fluke office or representative. Or, write: John Fluke Mfg. Co., Inc., P.O. Box 43210, Mountlake Terrace, WA 98043.

*U.S. price only.
8 BIT MOS

**3870**

A complete F8 μC on one chip, the 3870 features 2k×8 program ROM, 64×8 RAM, 32 bits of bidirectional I/O ports and a timer/event counter. Device has gained wide popularity in short time.

**SOFTWARE**

Executes F8’s complete set of 70 instructions, except STORE. Most execute in 2 μsec. Software compatible with F8 systems.

1—DATA MANIPULATION INSTRUCTIONS

Arithmetic and logicals. Decrement any scratch-pad register. BCD arithmetic. Built-in binary timer (with start/stop and pulse-width interval capabilities, plus 2/5/20 programmable prescaler). Timer is tied to interrupt.

2—DATA MOVEMENT INSTRUCTIONS

Most instructions operate on GP registers in CPU scratch pad with 1-byte code. Because 1-byte code can reach only first 12 registers of 64, you need indirect addressing via “ISAR” register to reach the rest.

3—PROGRAM MANIPULATION INSTR’S

Full vectored-interrupt capability. DC registers can perform pseudo-indexing. Subroutines save by hardware for first level; by software for deeper levels.

4—PROGRAM STATUS MANIP. INSTR.

5-bit status registers (sign, carry, overflow, zero and interrupt) have instructions to store.

**SOFTWARE SUPPORT:** Fortran IV cross assembler for 2-16-bit minis; resident edit, assembly and debug programs; and many ROM-based software packages. 3870 uses all F8 application programs.

**HARDWARE**

NMOS, silicon gate, 40-pin DIP, +5V, 500 mW. Versions with −55 to +125°C operation available.

**AVAILABILITY: Now.**

**COST:** In 25-99 qty: $17.95 for 1-MHz 6800, $25 for 1.5-MHz 6800A, $40 for 2-MHz 6800B, $22 for 6802.

**SECOND SOURCE:** AMI, Fairchild, Hitachi and Seacorn, licensed. Fujitsu MB8661 is a slightly enhanced 6800 with 5 more instructions.

**HARDWARE SUPPORT:** Various levels of pc-board and console aids, including the EXORciser and Evaluation MOD/2. Tektronix 8001/8002 supports the 6800. Many new peripheral chips being added to family.

**SOFTWARE SUPPORT:** Cross-assembler, interactive simulator, editor, macroassembler, disc-based operating system, debug, PL/M, BASIC and FORTRAN. Over 65 programs in user library.

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**8 BIT MOS**

**6800**

Popular μP family is being expanded to include faster 6800 CPUs, a 6802/6846 2 chip μC, a 6801 1-chip μC (see separate listing) and a 6809 16-bit “super” CPU.

**SOFTWARE:**

Copied from the PDP-11 set as closely as is possible with a shorter word-length machine. Execution times from 2-5 μsec.

1—DATA MANIPULATION INSTRUCTIONS

Arithmetic and logic. Instructions to take advantage of two accumulators.

2—DATA MOVEMENT INSTRUCTIONS

Can reach the first 256 locations of memory with short instructions. Can list-process efficiently with the Index Register. Relative addressing allows data relocation.

3—PROGRAM MANIPULATION INSTR’S

Has the PDP-11 Branches and Conditional Branches. Unlimited subroutine nesting via stack pointer addressing LIFO stacks in RAM. Does not have vectored interrupt, but can achieve function with software.

4—PROGRAM STATUS MANIP. INSTR.

Instructions for storing status register.

**SOFTWARE SUPPORT:** Cross-assembler, interactive simulator, editor, macroassembler, disc-based operating system, debug, PL/M, BASIC and FORTRAN. Over 65 programs in user library.

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**AVAILABILITY:** Now.

**COST:** $9.95 in 1000 qty, with much lower prices in large volumes.

**SECOND SOURCE:** Fairchild and Motorola, licensed.

**HARDWARE**

NMOS, silicon gate, +5V (± 10%), 40-pin DIP, 300 mW. F8 hardware compatibility for system expansion. Planned are +5V EROM and 4k ROM versions.

**SOFTWARE**

Executes F8’s complete set of 70 instructions, except STORE. Most execute in 2 μsec. Software compatible with F8 systems.

1—DATA MANIPULATION INSTRUCTIONS

Arithmetic and logicals. Decrement any scratch-pad register. BCD arithmetic. Built-in binary timer (with start/stop and pulse-width interval capabilities, plus 2/5/20 programmable prescaler). Timer is tied to interrupt.

2—DATA MOVEMENT INSTRUCTIONS

Most instructions operate on GP registers in CPU scratch pad with 1-byte code. Because 1-byte code can reach only first 12 registers of 64, you need indirect addressing via “ISAR” register to reach the rest.

3—PROGRAM MANIPULATION INSTR’S

Full vectored-interrupt capability. DC registers can perform pseudo-indexing. Subroutines save by hardware for first level; by software for deeper levels.

4—PROGRAM STATUS MANIP. INSTR.

5-bit status registers (sign, carry, overflow, zero and interrupt) have instructions to store.

**SOFTWARE SUPPORT:** Various levels of pc-board and console aids, including the EXORciser and Evaluation MOD/2. Tektronix 8001/8002 supports the 6800. Many new peripheral chips being added to family.

**SOFTWARE SUPPORT:** Cross-assembler, interactive simulator, editor, macroassembler, disc-based operating system, debug, PL/M, BASIC and FORTRAN. Over 65 programs in user library.
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For more information, Circle No. 35
**8-BIT MOS**

**PIC1650/1655/1670**

Containing ROM, RAM I/O and CPU, the PIC1650 is a complete, single chip, 8-bit µC. It's the only low-end machine to have mini-type access to its register stack.

**AVAILABILITY:** Now. **COST:** $20 in 2500 (min) qty; $10 at 10k; $3-$4 at 100k. **SECOND SOURCE:** Will be EM&M SEMI.

**HARDWARE**

NMOS device uses +5V. On-chip oscillator needs external R & C to provide 2-phase clock. 40-pin package.

**SOFTWARE**

User defines ROM program. Most of the 31 instructions execute in 1 µsec. Set is strong in bit manipulations and logical instructions. Word width of 12 bits shortens programs.

**I DATA MANIPULATION INSTRUCTIONS**

Add & subtract.

Logicals.

Rotate right and left.

Swap halves.

Bit set and clear.

Skip if zero.

**II DATA MOVEMENT INSTRUCTIONS**

Page addressing.

Move file.

**III PROGRAM MANIPULATION INSTR'S**

Move literal to W.

Call Subroutine.

Go to, return.

**IV PROGRAM STATUS MANIP. INSTR.**

Can bit test on status-register carry, decimal carry and zero.

**6801**

Single-chip, but expandable, µC version of 6800. Features “PIA-type” parallel ports, a serial port and sophisticated timer. Machine will be suited to multiprocessing and master/slave modes.

**SOFTWARE**

Upward compatible with 6800, but 12 new instructions.

**I — DATA MANIPULATION INSTRUCTIONS**

New: Hardware multiply and divide; 16-bit add, subtract shift and rotate; add 8 register to index register. From 6800: Arithmetic and logic; instructions to take advantage of dual accumulators.

**II — DATA MOVEMENT INSTRUCTIONS**

New: Instructions to push and pull index register on and off stack (in RAM). From 6800: Can reach the first 256 memory locations with short instructions; can list-process efficiently with index register; relative addressing allows data relocation.

**III — PROGRAM MANIPULATION INSTRUCTIONS**

From 6800: Has POP-11 branches and conditional branches; unlimited subroutine nesting via stack-pointer addressing. LIFO stacks in RAM; achieves vectored interrupt via software.

**IV — PROGRAM STATUS MANIPULATION INSTR.**

From 6800: Instructions for storing status register.
When you want more than a handshake but don’t need a "Phi Bete."

Our 8030B is at the head of its class if you’re looking for a smart CRT information terminal. Of course, we can provide a Phi Beta Kappa at the top end of the intelligent spectrum too—the 8035—but you can always upgrade to that when you’re ready.

In the meantime, here’s a sampling of the “smarts” 8030B can bring to your system. It’s a semi-programmable keyboard and display combination. It can be equipped with a memory option that will store and retrieve up to six pages of characters (1920 characters per page) for immediate access. It can cut “on-line” time as much as 50% and is, of course, available for the usual handshaking.

It’s smart features also include full editing capability, eight levels of video intensity and the ability to provide 128 unique function codes.

It’s 8080 based and delivers up to 9600 BAUD. It has a 15 inch screen, is kind to its operators because of its 14 x 9 dot matrix and its simplicity of operation. It has an 8000 hour MTBF. And can be made to emulate the protocol of most host computer systems.

Write or call Michael L. Squires for details and specifications, Information Products Division, Omron Electronics, Inc., 432 Toyama Drive, Sunnyvale, CA. 94086. (408) 734-8400.
8-BIT MOS

**8060 (SC/MP-II)**

SC/MP-II is NMOS version of PMOS SC/MP. Though described as simple μP by National, this machine has sophisticated features that demand close study by user.

**HARDWARE**

NMOS SC/MP-II uses 5V, dissipates 250mW. 40-pin DIP. Incorporates controls that permit 3 SC/MP’s to operate in master/slave fashion on same bus for multiprocessing use.

**SOFTWARE**

Pointer-type addressing, auto indexing, plus special instructions to utilize unique I/O features. Executions take 5-25 μsec.

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**CDP1802**

Second-generation CMOS machine makes extensive use of pointer-based addressing. Family device specs match standard 4000B CMOS, except for 11-15V voltage limits. Two- and one-chip μC’s are planned.

**SOFTWARE**

91-command instruction set uses pointer-based architecture. Most instructions require 2.5 μsec for fetch and execute.

---

**AVAILABILITY:** Now for both versions.

**COST:** SC/MP-II is $9 in 100 qty in plastic. Price expected to drop under $5 in volume in 1978.

**SECOND SOURCE:** Signetics, licensed.

**HARDWARE**

NMOS SC/MP-II uses 5V, dissipates 250mW. 40-pin DIP. Incorporates controls that permit 3 SC/MP’s to operate in master/slave fashion on same bus for multiprocessing use.

**SOFTWARE**

Pointer-type addressing, auto indexing, plus special instructions to utilize unique I/O features. Executions take 5-25 μsec.

---

**AVAILABILITY:** Now.

**COST:** $15.90 in 100 qty.

**SECOND SOURCE:** Hughes and Solid State Scientific, licensed.

**HARDWARE**

Static CMOS chip consumes 10 mW at 3.2 MHz/5V; 40 mW at 6.4 MHz/10V. 40-pin pkg. 3-15V, −5 to +125°C operation. Noise immunity 30% of VCC. Family being converted to CMOS/SOS for improved performance. Support will include CMOS EPROM in 75.

**SOFTWARE**

91-command instruction set uses pointer-based architecture. Most instructions require 2.5 μsec for fetch and execute.
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Body: 0.15 square to 0.5 square
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Space 0.1 to 0.4 standard (others available)

Capacitance: 4.7pf to 4.7mfd
Voltagess: 50, 100VDC
Three temperature characteristics

For more information, Circle No. 37
PPS-8, PPS-8/2

Aimed at low-cost controller and processor applications requiring high throughput.

SOFTWARE
Over 90 instructions, many unique, designed to take advantage of sophisticated architecture. Most executed in 1 cycle or 4 μsec.

DATA MANIPULATION INSTRUCTIONS
Binary arithmetic and logicals. Shifting and compare. Decimal arithmetic (packed).

DATA MOVEMENT INSTRUCTIONS
Many custom instructions designed to ease task of simultaneously processing multiple lists. Indirect and auto-incrementing addressing.

PROGRAM MANIPULATION INSTR.
Custom instructions for generating efficient loops. Subroutine starting-address pool allows code sharing to save ROM bytes. 16-level subroutine nesting. Three levels of priority interrupt.

PROGRAM STATUS MANIP. INSTR.
Bit setting and testing directly in RAM memory.

Note: Rockwell is now concentrating its development work on the MOS 6500. However, the firm will continue to support the PPS-8.

8 BIT MOS

2650/A/A-1

When designed in 1973, this µP was ahead of its time. However, hardware implementation delays crippled sales. To gain market share Signetics is now investing heavily in the development of new support chips.

SOFTWARE
The 75 instructions are patterned after those found in minicomputers. Most take 2 or 3 machine cycles and are executed in 4.8 to 7.2 μsec for the 2650A (3 to 9 μsec for the 2650A-1).

DATA MANIPULATION INSTRUCTIONS
Add, Subtract and Logical with choice of 8 addressing modes: 1- Register, 2- Immediate, 3- Relative direct, 4- Relative indirect, 5- Absolute direct nonindexed, 6- Absolute indirect nonindexed, 7- Absolute direct indexed, 8- Absolute indirect indexed.

DATA MOVEMENT INSTRUCTIONS
Load and Store, with option of all 8 addressing modes. Any of the 7 GP registers can be assigned as index register by bits in the op code. Buses can be 3-stated for DMA.

PROGRAM MANIPULATION INSTR.
Branch on condition; branch to subroutine on conditions (with all relative and absolute addressing modes). All-in-one conditional branch instructions provide efficient loop housekeeping control. Single-level interrupts vectored by interrupt source to service routines.

PROGRAM STATUS MANIP. INSTR.
Sixteen-bit wide program status register has its own commands.

SOFTWARE SUPPORT: "PIPBUG" ROM-based editor and loader, 16- and 32-bit Fortran IV assembler and simulator, plus 16- and 32-bit "PL0, S" compiler.
You can now have the industry's finest microcomputer with that all-important disk drive

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You can rely on this: Cromemco is committed to supplying quality software support.

For example, here's what's now available for our Z-2D users:

CROMEMCO FORTRAN IV COMPILER: a well-developed and powerful FORTRAN that's ideal for scientific use. Produces optimized, relocatable Z-80 object code.

CROMEMCO 16K DISK BASIC: a powerful pre-compiling interpreter with 14-digit precision and powerful I/O handling capabilities. Particularly suited to business applications.

CROMEMCO Z-80 ASSEMBLER: a macro-assembler that produces relocatable object code. Uses standard Z-80 mnemonics.

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For more information, Circle No. 38
**8-BIT MOS**

**MCP-1600**

Microprogrammable chip set builds 8- and 16-bit µP's with custom instructions (see NOTE, below).

**SOFTWARE**

Microinstructions operate in 500-nsec cycles. Four- and 8-bit op-codes allow machines of PDP-11/40 class to be attempted.

**1. DATA MANIPULATION INSTRUCTIONS**

The micro-instruction set includes decimal as well as binary arithmetic. It will operate with single bytes as well as double bytes so 8-bit machines can also be emulated.

**II. DATA MOVEMENT INSTRUCTIONS**

Developed by user, by selecting sequences of micro-instructions and encoding these in the µROM.

**III. PROGRAM MANIPULATION INSTR'S**

Developed by user.

**IV. PROGRAM STATUS MANIP. INSTR.**

Developed by user.

Note: MCP-1600 available from Western Digital in two macro versions: the MP-1600, which is similar to the Data General Eclipse; and the WD-1600, which has a unique instruction set aimed at the hobby market.

**SOFTWARE SUPPORT:** Assembler, simulator, editor and debugger run on disc-based DEC PDP-11/05 system. Single-user floppy-disc based software offered in source form without higher-level languages.

**HARDWARE SUPPORT:** Development pc boards. 2-board CPU set is compatible with S-100 bus; microprogramming development system contains CPU, memory and writable control store. (Support effort has been cut back due to W.D.'s financial difficulties.)

**8-BIT MOS**

**Z80/Z8/Z8000**

Superset of 8080; adds hardware and software features. Not pin-for-pin compatible with 8080, but can use 8080 software and peripherals (though to do so would not take full advantage of Z80's capabilities).

**SOFTWARE**

Totally Z80A software compatible. Features 50 additional instructions plus many more registers. Two banks of GP registers allow fast response via bank switching.

**I. DATA MANIPULATION INSTRUCTIONS**

8-bit arithmetic and logicals.

16-bit arithmetic BCD add and subtract.

Nine types of rotate and shift directly on any register or memory location. Can set, reset or test bit in any register or memory location.

**II. DATA MOVEMENT INSTRUCTIONS**

8- or 16-bit register or memory loads.

Two index registers allow indexed addressing.

Extensive memory-block move search commands.

**III. PROGRAM MANIPULATION INSTR'S**

Uses 16-bit stack pointer with LIFO stack with RAM memory. Relative jump capability. Interrupt capability with 3 types of selectable response.

**IV. PROGRAM STATUS MANIP. INSTR.**

Seven flag bits, including arithmetic and overflow, can be stored and tested.

* Support chips include peripheral interface (PIO), timer (CTC) and DMA which provide daisy chained vectored priority interrupt for CPU.

**SOFTWARE SUPPORT:** Macro-assembler with relocatable assembler, linking loader, file maintenance programs, and resident BASIC, COBOL, FORTRAN and PL/1. (Latter can mix assembly and higher-level "system" language statements.)

**HARDWARE SUPPORT:** Wide range, from evaluation pc boards to disc-based development system with real-time in-circuit emulation capability. Disk operating software includes the ability to edit files of any size.
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12-BIT CMOS

**AVAILABILITY:** Now.  
**COST:** $15 in 100 qty for commercial CPU; $16.50 for industrial version; $52.80 for military-grade chip.  
**SECOND SOURCE:** Harris licensed.

**HARDWARE:** Single-chip CPU in low-voltage CMOS (no guard rings). 4-11V PS. Operates dc to 8 MHz with upper limit proportional to supply voltage (speed increases 2½ times as voltage is doubled). Dissipation is less than 10 mW at 5V, 4 MHz.

**SOFTWARE:**  
Executes PDP-8/E instructions with 5 μsec memory-to-accumulator add at 5V supply; 2.5 μsec add at 10V supply. PDP-8 family has been around so long, so many routines exist to circumvent its shortcomings.

**I—DATA MANIPULATION INSTRUCTIONS**  
Basic, rather primitive selection of just a two's-complement binary add and a complementation for subtraction. Decimal arithmetic through software correction.

**II—DATA MOVEMENT INSTRUCTIONS**  
Addresses 4k locations via paging method where pages are 128 locations long (instead of the 256 common now in l1Ps). No literal mode of addressing, as that was not common when PDP-8 originally was developed some 15 years ago. Magnetic core memories rather than ROM's were used then for nonvolatility.

**III—PROGRAM MANIPULATION INSTR's**  
Subroutine returns accomplished via more primitive approach of using software step to save return address at top of subroutine, rather than modern use of hardware LIFO's or stack-pointer registers. Skip-type instructions used for conditional branching.

**IV—PROGRAM STATUS MANIP. INSTR.**  
No status register, but link or carry flip-flop can be set, cleared or tested by software.

**HARDWARE SUPPORT:** Both Intersil and Harris offer board-and-box-level prototyping system. Intersil uses the name "Intercept." Harris, the name "SIMON."

**SOFTWARE SUPPORT:** Extended package contains loaders, assemblers, editors, debuggers and floating point arithmetic. Also: FOPAL cross assembler and FOCAL interpreter. Can use DECUS library and DEC service programs.

----

**16-BIT MOS**

**AVAILABILITY:** Now.  
**COST:** mN601 CPU is $75 in 100 qty.  
**SECOND SOURCE:** None announced.

**HARDWARE**  
NMOS, silicon-gate, dynamic CPU needs ±5 and ±15V. On-chip 2-phase clock uses external 8.33 MHz xtal. Refresh control for dynamic RAM's.

**SOFTWARE**  
Full compatibility with NOVA software. Accumulator load takes 2.9 μsec add, 2.4 μsec.

**I—DATA MANIPULATION INSTRUCTIONS**  
Hardware multiplication and division. Single-word instructions can execute arithmetic or logical operations from any pair of registers, and can also shift, test and store the result.

**II—DATA MOVEMENT INSTRUCTIONS**  
Single-word instructions move data between BAVI locations and any register. Multiple addressing modes include absolute, relative, indexed, deferred and auto-increment/decrement. Two of the multiple accumulators can be used as index registers.

**III—PROGRAM MANIPULATION INSTR's**  
Programmed priority interrupts to 16 levels. Hardware stack facilitates programming of reentrant and recursive subroutines. SAVE instruction allocates new stack frame, while simultaneously storing all CPU registers.

**IV—PROGRAM STATUS MANIP. INSTR.**  
Carry bit, interrupt enable bit, real-time clock enable and request bits, stack-overflow request bit.

**HARDWARE SUPPORT:** Wide range, from single-board μC with up to 4k words RAM, to stand-alone mini, to development system with diskette-based Disc Operating System (DOS).

**SOFTWARE SUPPORT:** Wide range, including DOS with text editor, FORTRAN IV compiler, assembler, symbolic debugger and relocatable loader; real-time operating system and extensive application library.
Put our new UART and BIT RATE GENERATOR together and what have you got?

The first programmable CMOS Communications System.

With the Harris HD-6402/6402A CMOS/LSI, and HD-4702/6405 CMOS Bit Rate Generator, you can convert parallel data to serial and back again asynchronously, substantially reducing the amount of interconnect in your data acquisition systems.

Now, all it takes is two lines to connect terminals to computers, for example, instead of the spaghetti of wire used in older systems.

And, only with Harris do you enjoy the benefits of all-CMOS technology. Like less power consumption, permitting remote, hand-held battery-operated systems. Faster speed. Fewer and smaller components for added economy in equipment costs. Plus full temperature ranges, including military.

The Harris HD-6402/6402A, designed to replace the older and slower P-channel types, is the industry’s first CMOS UART. It features an industry standard pinout. Single power supply—operates on 4 to 11 volts. And it’s fast…125K Baud…the fastest UART in operation today.

The Harris all-CMOS Bit Rate Generator provides the necessary clock signals for the UART. The HD-4702 generates 13 commonly used bit rates, while the HD-6405 provides two additional bits and consumes significantly less power, with no pull-up resistors.

If you’ve been waiting for CMOS for your modems, printers, peripherals, and remote data acquisition systems designs, your wait is over! Now Harris technology has something you can really work with. And you can start today!

For full details, call the Harris Hot Line, or write:
Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901.

HARRIS HOT LINE!
1-800-528-6050, Ext. 455
Call toll-free for phone number of your nearby Harris sales office, authorized distributor or expedited literature service.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION

For more information, Circle No. 40

EDN NOVEMBER 20, 1977
MACROLOGIC

Four-bit-slice building blocks for microprogrammable computers. Available in both Schottky-TTL and CMOS, with some parts using FL technology.

SOFTWARE:
User defines his own instruction set by microprogramming the μROM. Parts will respond to the following type commands.

I—DATA MANIPULATION INSTRUCTIONS
Arithmetic and logic, increment and decrement, logic shift, left and right, bit and byte masking, sign extension.

II—DATA MOVEMENT INSTRUCTIONS
Uses register transfer module concept. Any device can be designated as source or destination of data. User can implement variety of addressing modes, including indexing.

III—PROGRAM MANIPULATION INSTR’S
Jump
Call Subroutine
Conditional and subroutine branch
4-deep stack for micro-subroutine nesting.
User can have stack with PC, or (via stack pointer register) he can put stack in main memory, depending on which of two PC parts he uses (9406 or 9407).

IV—PROGRAM STATUS MANIP. INSTR.
Carry, overflow, negative, zero and PC stack full and empty (on 9406).

SOFTWARE SUPPORT:
Microprogram assembler available through purchase or timeshare.

16-BIT MOS

CP-1600/1610

Aimed at real-time control automation. Yield problems lowered 1600’s clock spec from 5 MHz to 4 MHz. (The 1610 operates at 3.3 MHz.)

SOFTWARE
68 instructions execute in 2-6 μsec (2.4-7.2 μsec for 1610). 16-bit add from memory takes 4 μsec (4.8 for 1610). Instructions patterned after PDP-11, but no indexing mode.

SOFTWARE SUPPORT:
Cross-assembler, debugger, simulator, diagnostics and subroutine library. Also, relocatable linking loader, text editor and SUPER ASSEMBLY high-level language.

EDN NOVEMBER 20, 1977
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PROBLEM:
Go directly from relay requirement "A" to optimum relay specification "B" for any application.

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Because we're the only relay company that makes all its own switches, we know relays from the inside out—and make more than anyone else. More types...more versions of each type.

And, we accept single responsibility for maintaining high standards of quality for every one. So, when matching the optimum relay to an application, we help keep tradeoffs down. We offer a broad perspective unmatched by suppliers with fewer alternatives...a greater product base from which to select special-purpose relay solutions others just don't have...plus the technological expertise to avoid high custom-design costs often by simply modifying a standard solid-state, axial-travel, or reed relay design.

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For more information, Circle No. 41
16-BIT MOS

**8900 (PACE)**

National Semiconductor Corp.
2900 Semiconductor Dr., M/S 470
Santa Clara, CA 95051
Phone (408) 737-5000

Similar to NOVA-1200 in architecture, but with instruction set suited to Microcomputer applications. Has many unassigned op codes, so much potential growth left.

**SOFTWARE**

All 45 instructions are single word length; most execute in 10 µsec. Rich option fields in each instruction provide over 300 combinations.

**DATA MANIPULATION INSTRUCTIONS**

Add, subtract and logicals (hardware multiply and divide are planned for future version). N-bit shifts and rotates. Efficient decimal-adjust instruction allows much better performance on decimal number than IMP-16.

**DATA MOVEMENT INSTRUCTIONS**

Indexing using any of four accumulators. Can do serial I/O through jump condition inputs and flag outputs up to 4800 baud.

**PROGRAM MANIPULATION INSTR'S**

Skip and branch. Increment and skip if zero. Push and pull 16-level stack. Five levels of interrupts, with on-chip prioritized vectoring.

**PROGRAM STATUS MANIP. INSTR.**

Full 16-bit status register has not only the usual indications of ALU results but space left over for user-definable flags.

**SOFTWARE SUPPORT:** FORTRAN-IV cross-assembler that runs on >16-bit computers ($495); BASIC interpreter that needs 8k memory system ($100); and resident 4k and 8k packages that include assemblers, loaders, debug and utilities ($200).

**HARDWARE SUPPORT:** Board assemblies for prototyping and short-run production. Development systems range from $585 LCDS to $5000 unit with 8k of memory.

**HARDWARE:**

PMOS slices for CPU and CROM, with rest of P programming CROM. It will become obsolete when NMOS single-chip PACE is introduced.

**SOFTWARE:**

43 instructions for basic 16-bit full-sized version executed in 5-10 µsec. Similar to Data General Nova 1200 mini.

**DATA MANIPULATION INSTRUCTIONS**

Basic CROM provides conventional Add, Subtract and Logicals.

Additional CROM provides powerful instructions: multiply and divide and double-precision operations.

**DATA MOVEMENT INSTRUCTIONS**

Direct addressing in three modes: base page, PC relative and indexed. Indirect addressing to full 65k of memory. Additional CROM will allow block transfer, I/O and memory search.

**PROGRAM MANIPULATION INSTR'S**


**PROGRAM STATUS MANIP. INSTR.**

Can manipulate status flag bits and move 16-bit flag register as a whole.

**SOFTWARE SUPPORT:** Cross-assemblers and high-level language (SM/PL). Also, self-assembler, debug, timeshare, diagnostic, etc.

16-BIT MOS

**IMP-16**

National Semiconductor Corp.
2900 Semiconductor Dr., M/S 470
Santa Clara, CA 95051
Phone (408) 737-5000

Machine is based on 4-bit “RALU" slices plus microprogramming CROM. It will become obsolete when NMOS single-chip PACE is introduced.

**SOFTWARE:**

43 instructions for basic 16-bit full-sized version executed in 5-10 µsec. Similar to Data General Nova 1200 mini.

**DATA MANIPULATION INSTRUCTIONS**

Basic CROM provides conventional Add, Subtract and Logicals.

Additional CROM provides powerful instructions: multiply and divide and double-precision operations.

**DATA MOVEMENT INSTRUCTIONS**

Direct addressing in three modes: base page, PC relative and indexed. Indirect addressing to full 65k of memory. Additional CROM will allow block transfer, I/O and memory search.

**PROGRAM MANIPULATION INSTR'S**


**PROGRAM STATUS MANIP. INSTR.**

Can manipulate status flag bits and move 16-bit flag register as a whole.

**SOFTWARE SUPPORT:** Cross-assemblers and high-level language (SM/PL). Also, self-assembler, debug, timeshare, diagnostic, etc.

**HARDWARE SUPPORT:** Functional computer on a pcb board. Console-level "microcomputers."
The new design standard.
Low Power Schottky. From the leader.
Texas Instruments.

Now there are 165 Low Power Schottky functions available from the leader, Texas Instruments. The broadest line in the industry...SSI, MSI and LSI circuits for every low-power, high-performance application...military systems, data processing, telecommunications, process control, with or without microprocessors. You'll find TI Low Power Schottky circuits provide greater reliability at a lower cost in less space with less power.

All of TI's innovative 74LS/74LS circuits feature typical speeds to 6 ns/gate with power dissipation of less than 2 mW. In fact, power requirements are 80% less than for standard TTL logic. Less heat is generated. Less heat sinking is required. Low Power Schottky MSI and LSI circuits increase package density reducing package count and the number of interconnections required. Costly pc board real estate is thus minimized.

And, TI's Low Power Schottky circuits cost less, as low as $1.40 for a 74LS245N Octal Bus Transceiver and $0.69 for a 74LS669N 4-Bit Binary Counter (100 pieces). Add it all together and the result is high performance and reliability at lower manufacturing costs.

Design with more confidence with the LS line that serves more of your needs for less. To learn more about system benefits, contact Texas Instruments Incorporated, P. O. Box 5012, M/S 308, Dallas, Texas 75222.

MORE NEW PRODUCTS
23 new Low Power Schottky circuits have been introduced in 1977 for a total of 165 since 1971...with more on the way.
SN54LS/74LS673 16-Bit POSI Shift Register with Storage
SN54LS/74LS674 16-Bit PISO Shift Register
SN54LS/74LS322 8-Bit Shift Register w/Sign Extend
SN54LS/74LS173 4-Bit D-type Register, 3-State

For more information, Circle No. 42
BIPOLAR

AVAILABILITY: Now.
COST: $385 in 100 qty including software.
SECOND SOURCE: To be announced.

HARDWARE
PL technology keeps CPU chip size to 182 x 189 mils. 930
mW (180 mA at 1 V for PL, 150 mA at 5 V for TTL): 40-pin DIP.

SOFTWARE
Executes all NOVA-1200 instructions at full “bipolar” speed. Takes
only 1.5 µsec for memory reads and writes.

I — DATA MANIPULATION INSTRUCTIONS
ALU instructions particularly powerful because code’s multiple
fields allows shifts, tests, etc. to also be performed in the same
instruction that does arithmetic or logic. Hardware multiply/divide
by external 9443 support chip (not shown).

II — DATA MOVEMENT INSTRUCTIONS
Eight addressing modes: zero page direct and indirect, PC-relative
direct and indirect, index (via AC 2 and AC 3) direct and indirect.
Many I/O instructions perform manipulations on I/O as well as basic
data movement.

III — PROGRAM MANIPULATION INSTRUCTIONS
Decisions via conditional SKIP instructions. Subroutines must be
software implemented using AC 3; stacks must be formed in mem-
ory using software and AC 2 and AC 3.

IV — PROGRAM STATUS MANIPULATION
INSTRUCTIONS
No status register, per se, but equivalent functions built into ALU
instruction fields.

SOFTWARE SUPPORT: Five items initially: system diagnostics,
bootstrap loader, “FIREBUG” interactive program entry and debug
monitor, stand-alone text editor and stand-alone business BASIC.
In 1978 expect disc-based FORTRAN compiler with string operators
and macro assembler.

BIPOLAR

AVAILABILITY: Now.
COST: $8.80 for 2-bit slice in 100 qty. (A 16-
bit kit with 26 parts costs $210 in 100 qty.
SECOND SOURCE: Signetics.

HARDWARE
Schottky-TTL 2-bit wide slices and 9-bit microprogram sequencer.
Use ±5V power supply. Standard bipolar PROM’s available.

SOFTWARE
CPU slices respond to 40 micro-instructions, taking 150 nsec/cycle
on systems level. Hardware’s 3 input and 2 output CPU buses allow
fast 1-cycle processing of memory and I/O data. Good at bit testing
for controller use.

I — DATA MANIPULATION INSTRUCTIONS
Arithmetic and logic.
Increment/decrement.
Shift left and right.
Swap bytes.
Bit testing.

II — DATA MOVEMENT INSTRUCTIONS
Developed by user using the micro-instructions to assemble
desired macro-instructions.

III — PROGRAM MANIPULATION INSTR’S
Developed by user.

IV — PROGRAM STATUS MANIP. INSTR.
Developed by user.

NOTE: User codes µROM to define the regular or “macro” instruc-
tion set for each application. For example, Signetics emulates 8000
with 3000-Series parts.

SOFTWARE SUPPORT: CROMIS, cross-microassembler avail-
able in FORTRAN-IV tape form ($1250) or on several timeshar-
ing networks.
Our family gives you a flat answer.

Our new flat cable connector family has both standard and stackable sockets, PCB connectors and headers, all designed for lowest total applied cost.

In socket connectors our BA Series gives you a low profile package with the option of either open or closed cover design for both end-cable and through-cable applications.

Our BD Series stackable socket line concept permits stacking two connectors on a wire-wrappable post.

For direct solder applications our BC Series handles PCB connector needs.

Featured with the product family is a simple universal termination system designed for minimum tooling cost.

For your header applications our low profile BB Series line is available for both vertical and right-angle mounting in solder or wire-wrappable designs.

Contact GTE Sylvania, Connector Products Operation, Box 29, Titusville, PA 16354. Phone: 814-589-7071.

Remember, good connections run in our family.
**8-BIT MOS**

**TMS9900/9980/9940, SBP9900**

Memory-to-memory architecture (no accumulator or working registers in CPU) allows multiprocessing and rapid context switching upon interrupt or subrouting. All machines are 16 bits in CPU. One-chip 9940 µC makes extensive use of 1-bit serial port, includes ROM and RAM.

**SOFTWARE**

Minicomputer set of 69 instructions (58 for 9940).

**I—DATA MANIPULATION INSTRUCTIONS**

Binary arithmetic including multiply and divide. Logicals and shifts. Can operate on words, bytes, or bits.

**II—DATA MOVEMENT INSTRUCTIONS**

Addressing first chooses the "workspace" in memory that will contain the 16 GP registers used by instructions. This takes extra step, but allows rapid, easy context switching between a large number of alternate register groups. Information in workspaces can be left intact when computer switches tasks, allowing different tasks to be processed concurrently.

**III—PROGRAM MANIPULATION INSTR'S**

Some unique instructions due to memory-to-memory architecture. However, not difficult to understand. Can do indexing. Signed, relative type of precision jumps (branches). Sixteen levels of priority vectored interrupt, speeded by the context switching. (Upon interrupt, machine switches to the service workspace.)

**IV—PROGRAM STATUS MANIP. INSTR.**

The 16-bit long status word contains usual ALU results indicator bits, plus extended mode set bit and four status code bits that set priority level allowed for interrupt.

**SOFTWARE SUPPORT**

Assemblers and simulators in batch form or through timesharing network; portable ANSI Fortran assembler and simulator; PL/9900, Fortran and BASIC languages. Program library offered.

**BIPOLAR**

**AM 2900**

Advanced Micro Devices
901 Thompson Pl.
Sunnyvale, CA 94086
Phone (408) 732-2410

Popular family of low-power Schottky-TTL LSI devices aims at microprogrammable computers. New 2903 RALU slice is an enhanced 2901A, with features suited to arithmetic processing.

**SOFTWARE**

User defines microinstruction set by programming µ-ROM. Parts respond to following instructions within 1 clock cycle (50-125 nsec); 16-bit RR and add takes 145 nsec.

**I—PROGRAM STATUS MANIPULATION INSTRUCTIONS**

ALU performs three arithmetic operations on two operands and five logical functions. Shifting networks can be used with add instruction for efficient multiplication and division.

**II—DATA MOVEMENT INSTRUCTIONS**

The 16 working registers in RALU RAM can be addressed two at a time for simultaneously supplying the two operands to the ALU.

**III—PROGRAM MANIPULATION INSTR'S**

Defined by user via microcode. All modern modes of addressing should be possible.

**IV—PROGRAM STATUS MANIP. INSTR.**

Carry, overflow, zero and negative status outputs.

**NOTE:** In addition to the 2901A and 2903 RALU slices, the 2900 family includes the 2913 interrupt expander, 2919 1 × 2 port register; 2970/40/50 64-bit, 2-port RAM's; 29720/21 256-bit RAM's; 29750/51 256-bit PROM's; 29803 16-way branch controller for 2939; 2911 instruction controller for 2911; and N8X02 (Signetics) controlled-store sequencer.

**SOFTWARE SUPPORT**

AMD/ASM microprogram assembler is available in 3 forms: timesharing, floppy disc for Intel MD5-80 and resident in AMD System-29.
What price boredom?

ACDC will bore you for less. Much less. Because we've reduced prices on our open frame power supplies to an all-time low. Thanks to new manufacturing facilities. The latest engineering advances. And an insane desire to increase our sales.

But what's all this talk about boredom? Aren't low prices exciting? Certainly. It's our open frame power supplies that are boring. Boring because they're so dependable. (In fact, our entire open frame line just received UL recognition.)

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acdc electronics
401 Jones Road, Oceanside, California 92054

We made a science out of boredom.

For more information, Circle No. 44
### Bipolar

**Availability:** Now for the 10800-10808.
**Cost:** $30 per slice in 100 qty. for 10800.
**Second Source:** Possibly Fairchild.

**Hardware**
Bipolar ECL using −5.2 and −2.0V supplies. The package has 48 pitched pins that take up same area as 24-pin pkg. Can be pipelined for maximum speed.

**Software**
Microprogramming is used to meet requirements of any processor's instruction set. Cycle time is approx 100 nsec.

### 10800

**Hardware**
Four-bit-slice building blocks for high-performance computers, controllers and communications processors. Compatible with ECL 10k family.

**Software**
Arithmetic including high-speed hardware BCD in ALU. The 10803 includes an additional binary ALU. Shifts, both left and right; both logical and arithmetic.

### System Bus, 16-Bits

![Diagram of system bus](image)

1. **Clock:** 3.3 MHz
2. **Std 501 TTL:** Starts
3. **Std Mem:** (50 – 85°C)
4. **Std Mem:** (50 – 85°C)

**Software Support:** On-line demonstrator system in conjunction with 6800 EXORciser.

## 5701/6701

**Availability:** Now.
**Cost:** 6701 is $26.15/slice in 100 qty; 5701, $53.30/slice.
**Second Source:** ITT licensed.

**Hardware**
Schottky TTL. 5701 MIL version operates from −55 to +125°C at +5V ±10% power supply. 40-pin package.

**Software**
Slices will respond to 32 microinstructions within 200 nsec (6701), doing complete on-chip register operations (longer with multiple slices).

---

**Data Manipulation Instructions**

**Arithmetic, Logic and Shifting**

**Data Movement Instructions**

**Program Manipulation Instrs**

**Program Status Manip. Instr.**

### Monolithic Memories Inc.

1165 E. Arques Ave., Sunnyvale, CA 94086.
Phone (408) 739-3535

### Motorola Semiconductor Products Div.

5005 E. McDowell Rd., Phoenix, AZ 85008.
Phone (602) 244-6900

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**Address, Instructions and Data**

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Software Support: MACE 29800 system for developing microprogrammable μC's will handle both ECL and TTL slices. This system will be available in 1978.
S-D's Dual Channel Power Supply: the first supply designed for IEEE-488 bus applications.

- Two independent, bipolar power sources
- All analog functions bus controlled
- Programmable overvoltage and current limits
- Memory register displays

The industry's best dual channel power supply now includes the IEEE bus interface as standard equipment! With a single address, you can program two 50 volt, 1 amp bipolar supplies; set the voltages; limit the currents; assign trip points, and reverse polarities. (For faster systems, a BCD parallel bus version is available.)

Behind the hinged front panel of Model DP5D-50 sits a complete local control center. These local-mode switches provide a fast and easy way to set the address, step through a program sequence, or verify calibration.

Key specifications: resolution, 1 mV; basic accuracy, 1 mV; stability, 300 µV.

Instead of buying two expensive power supplies, you can now do the job with one DP5D-50 ($3,000 in U.S., slightly higher outside U.S.). For more details, contact Scientific Devices or Systron-Donner at 10 Systron Drive, Concord, CA 94518. Phone (415) 676-5000.

For more information, Circle No. 45
### BIPOLAR

**BIPOLAR AVAILABILITY:** Now.

**COST:** CPU is $32 (100 qty). The $175 starter kit includes CPU, 4 IV bytes and 1.5k words of PROM.

**SECOND SOURCE:** To be announced (a major U.S. company).

**HARDWARE**

Schotky-TTL LSI chips. CPU consumes 1.57 W, has 50-pin pkg.

**SOFTWARE**

Only 8 instruction types; all execute in 250 nsec, max. Each specifies source for data, operation to be performed, and destination for data. Data can be internal register or any group of 1 to 8 bits on interface.

**SOFTWARE SUPPORT:** $775 MicroController cross-assembler will run on any 16-bit machine that uses FORTRAN. Also available on NCSS timesharing.

---

**SBP0400A**

**AVAILABILITY:** Now.

**COST:** $14.60 per 4-bit slice in 100 qty.

**SECOND SOURCE:** None announced.

**HARDWARE**

Circuits operate with very low voltage supplies over a 1000:1 range of injector current. Power consumption can be very low, but dropping resistors needed with 5V TTL raise total consumption, 40-pin DIP.

**SOFTWARE**

Slices respond to 512 microinstructions (9-bit control word) within one 200-nsec clock cycle, and operate at true micro or gate control level. User builds up his macroinstruction set from these.

**SOFTWARE SUPPORT:** Application-note examples detail micro- and macroinstruction codes for selection of instructions from variety of machine types.

---

**8X300 MicroController**

Originally a custom chip processed for SMS by Signetics. 8X300 is now offered at device level. The first single-chip 8-bit processor, it is being applied to CRT and floppy disc control, real-time digital communications, etc.

**SOFTWARE**

Only 8 instruction types; all execute in 250 nsec, max. Each specifies source for data, operation to be performed, and destination for data. Data can be internal register or any group of 1 to 8 bits on interface.

**SOFTWARE SUPPORT:** $775 MicroController cross-assembler will run on any 16-bit machine that uses FORTRAN. Also available on NCSS timesharing.

---

**ADDRESS BUS (3X4 = 12)**

Note: 12-bit µC diagrammed. Other multiples of 4 possible.

**HARDWARE SUPPORT:** LCM-1000 series of microprogrammable prototyping modules (approximately $75 to $150).
Custom Hybrid Microcircuits from Exacting Craftsmen

Building highly reliable custom hybrid microcircuits is a subtle craft, requiring the mastery of artisans. For years, our engineers have teamed with designers of circuits for high-reliability military and aerospace projects, such as F15, Hawk, Viking, Mars, and Intelsat. There, they have carefully honed the techniques necessary to guide you through a smooth transition from your basic electronics to a highly reliable and economical hybrid. They will also consolidate a preferred circuit for you, so that you can take advantage of the assembly, space, handling, stock and inventory savings of the hybrid package.

With custom hybrids, your only limitation is your imagination. You'll be amazed by the variety and number of parts that we can put in a package. In our unique facility, our craftsmen produce thin film and thick film hybrid microcircuits ranging from simple multiple-chip circuits to complex multi-layered assemblies.

No matter what circuit we produce for you, it will meet whatever level of reliability you require. We manufacture to all provisions of MIL-M-38510 and screen to any level of MIL-STD-883. Our quality systems meet or exceed MIL-Q-9858A and NASA NPC-200-3, with many processing options. Whatever your hybrid microcircuit requirement, you'll find Crystalonics unbeatable on size, reliability, and turn around time. For the full story, send for our custom hybrids brochure. For immediate action, call our applications engineering team at (617) 491-1670.

TELEDYNE CRYSTALONICS
147 Sherman Street
Cambridge, MA 02140
Tel: (617) 491-1670 • TWX 710-320-1196
BIPOLAR

AVAILABILITY: Now.
COST: $29.25 in 100 qty.
SECOND SOURCE: None announced.

74S481, etc. Chip Set
Fast, microprogrammable Schottky TTL chip set suitable for constructing minicomputers with LSI parts.

SOFTWARE:
Microprogrammable, so user defines instruction set. However, TI will offer version that emulates TI's own 990 mini.

Both hardwired algorithms (macro) and micro operations are available, totalling 24,780 unique instructions. The 14 classes of instructions include the following:

I—DATA MANIPULATION INSTRUCTIONS
Built-in multiplies and divides.

II—DATA MOVEMENT INSTRUCTIONS

III—PROGRAM MANIPULATION INSTR'S

IV—PROGRAM STATUS MANIP. INSTR.

HARDWARE:
Schottky TTL will operate at 10-MHz clock, with usual 5V supply and over Mil. temp. range.

SOFTWARE SUPPORT: Minicomputer level.
HARDWARE SUPPORT: Minicomputer level.

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