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CL-SH351

Data Sheet

FEATURES

Microcontroller Interface

- Supports high-speed microcontroller interfaces (e.g., 16 MHz 8051, 12 MHz 68HC11, 30 MHz HPC460X3)

SCSI Interface

- Supports SCSI-2 Initiation and Target Modes
- Supports asynchronous DMA/PIO transfers up to 3 Mbytes/second
- Supports synchronous DMA/PIO transfers up to 10 Mbytes/second
- Supports up to 15-byte synchronous transfer offsets and 13 programmable transfer periods
- Controls synchronous transfer overrun/underrun
- Controls arbitration, selection, and reselection in hardware
- Detects selected and reselected conditions automatically
- Integrates 48 mA SCSI bus drivers in the interface
- Provides control for the external differential driver option

Sector Formatter

- Programmable Format Sequencer Writable Control Store (WCS – 31 x 4 bytes)
- Supports up to 32 MHz NRZ data rates

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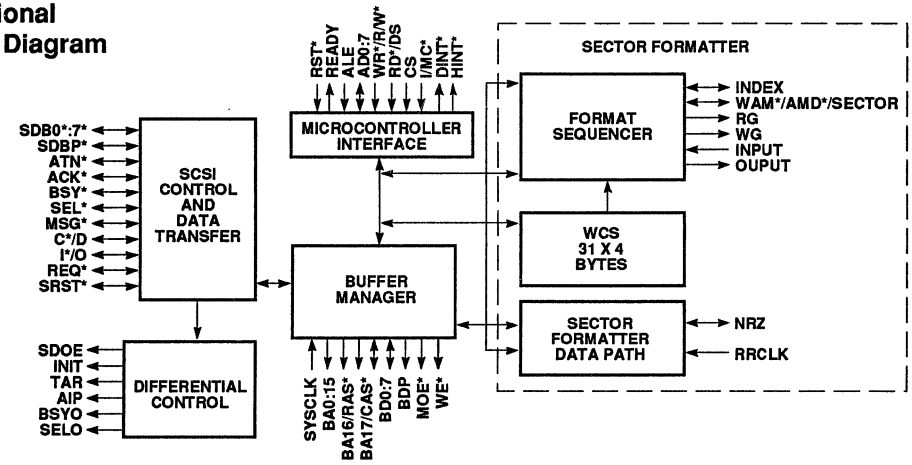
High-Performance Synchronous/Asynchronous Integrated SCSI Disk Controller

OVERVIEW

The CL-SH351 is a VLSI component that provides the majority of the hardware necessary to build a Small Computer System Interface (SCSI) Winchester disk controller. The CL-SH351 design combines a high-speed local microcontroller port, extensive hardware support for the SCSI interface, a two-channel Buffer Manager, and an advanced Sector Formatter. With the addition of only a few discrete components for the device-level interface, the CL-SH351, along with a local microcontroller, system ROM and RAM, and an optional data separator, completes a disk controller subsystem with high performance at a low-overall cost.

A local microcontroller provides the CL-SH351 with initial operating parameters that include disk sector format, the type and size of buffer memory, and SCSI Host control. *(cont. next page)*

Functional Block Diagram



FEATURES (cont.)

- **Allows split data field processing for embedded servo and zoned designs**
- **Provides selectable 16-bit CRC or 32/56-bit ECC with proprietary error correction hardware †**

Buffer Manager

- **Dual-channel, circular buffer control with priority resolution**
- **Direct buffer addressing up to 256K bytes of SRAM and 1 Mbyte of DRAM**
- **Permits concurrent buffer memory throughput up to 14 Mbytes/second in DRAM Page Mode and 15 Mbytes/second for SRAM**
- **Odd-parity data verification between the SCSI bus and the Sector Formatter**

Technology

- **100-pin Quad Flat Pack (QFP) package**
- **Advanced, low-power, double-metal CMOS technology**

OVERVIEW (cont.)

During data transfer operations, the CL-SH351 requires only minimal intervention from the local microcontroller. The microcontroller- to-CL-SH351 communication path is a multiplexed address and data bus similar to that provided by the Intel® 8051- and the Motorola® 68HC11-class of controllers. (There is a configuration signal available to allow for either family of data control signal methods). The CL-SH351 has centralized status registers with interrupt capability. These features allow firmware designers flexibility in writing polled loops or interrupt handlers that provide real-time process control critical in embedded controller drive applications.

The SCSI Host interface is designed for compliance with the proposed SCSI-2 specification and supports synchronous transfer capability of up to 10 Mbytes/second. This ensures long-term compatibility for both the hardware and the firmware developed around the CL-SH351. The SCSI interface logic includes integrated high-current (48 mA) drivers for the single-ended option, as well as signals for control of the external logic necessary to implement the differential transceiver option. Both the asynchronous and synchronous transfer protocols are supported in either Initiator or Target Mode. Routine bus control operations, such as arbitration, selection and reselection, are automatically sequenced in hardware. This method of implementing the SCSI interface makes the SCSI protocol firmware extremely flexible and very efficient.

The Sector Formatter provides the disk data and control functions. The Sector Formatter is capable of handling NRZ data rates up to 32 Mbits/second. The Sector Formatter is subdivided into a Format Sequencer and the Sector Formatter Data path. The Format Sequencer uses a 31-word-by-4-byte Writable Control Store (WCS) to hold a user-written program. This program contains the control information for the disk track and sector format. The Sector Formatter Data path consists of the NRZ data handling circuitry that includes the serializer/deserializer (SERDES), the ECC and CRC error control logic, the SERDES parity logic, and the data signals to the Buffer Manager interface.

The Buffer Manager controls the flow of data between the host and disk interfaces. These interfaces store and retrieve data from the buffer memory using interleaved access cycles. The actual buffer memory may be implemented with static or dynamic RAM devices. The CL-SH351 Buffer Manager is programmable to provide all of the necessary address and control signals for RAM devices of varying access times. Up to 256K bytes of SRAM can be directly addressed by the CL-SH351. As much as 1 Mbyte of DRAM is directly supported by the CL-SH351, with specific control for 64K, 256K, and 1 Mbit devices. In DRAM Mode, refresh is generated automatically through a third channel to the buffer memory, in addition to the concurrent disk and host accesses.

† A U.S. patent has been issued on Cirrus Logic proprietary 56-bit ECC.

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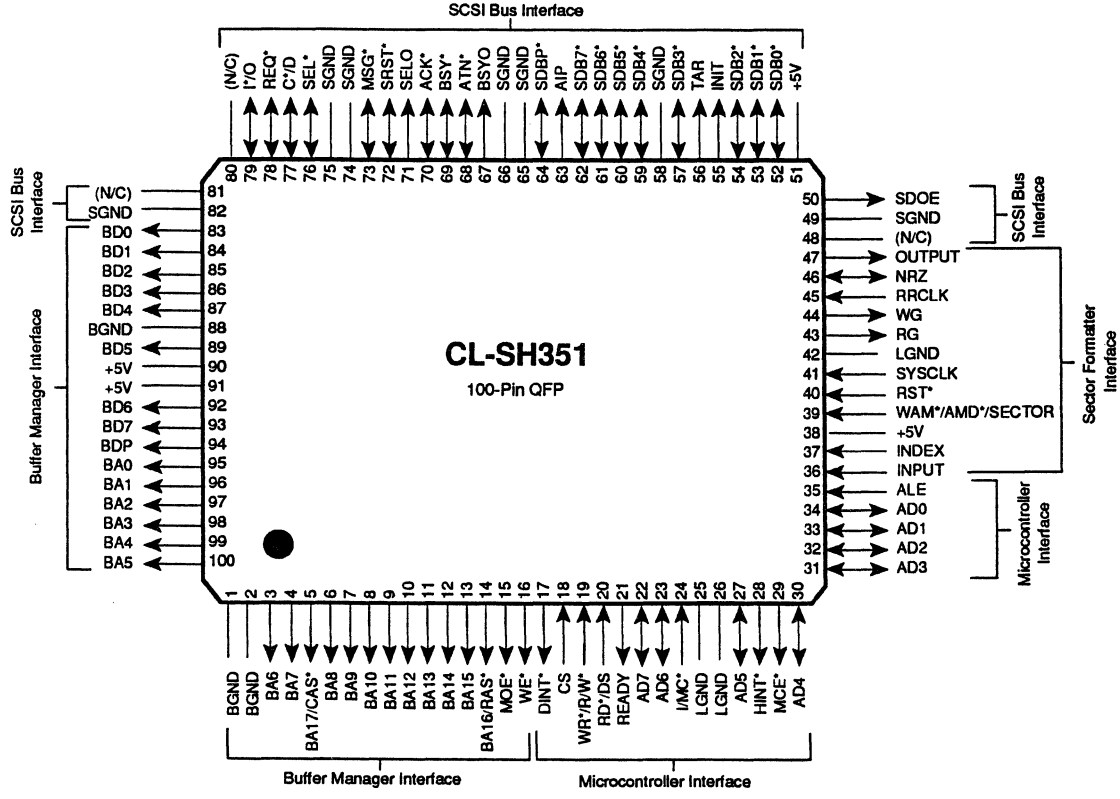
1. PIN INFORMATION

The CL-SH351 is available in a 100-pin Quad Flat Pack (QFP) package. The diagram below shows the pinout of this package. All unused inputs must be tied to the inactive state to VCC or GND respectively.

1.1 Pin Diagram for the 100-Pin Quad Flat Pack (QFP) Package



*Denotes negative true signal.

2. PIN ASSIGNMENTS

The following conventions are used in the pin assignment tables. An asterisk (*) denotes a negative true signal. An (I) indicates an input pin. An (O) indicates an output pin. An input/output pin is indicated by (I/O). A (Z) indicates a tri-state output. Open drain output pins are indicated by (OD). All unused inputs must be tied to the inactive state to VCC or GND respectively.

2.1 Microcontroller Interface Pins

Symbol	QFP Pin No.	Type	Description
DINT*	17	O,OD, Z	**DISK INTERRUPT:** This signal is a disk interrupt line to the microcontroller. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-impedance state.
CS	18	I	**CHIP SELECT:** This signal must be asserted high for all microcontroller accesses to the CL-SH351 registers and to the Writable Control Store (WCS).
WR*/R/W*	19	I	**WRITE STROBE/READ/WRITE:** When the Intel bus control interface is selected (the I/MC* signal (pin 24) is asserted high), this signal acts as the WR* signal. When the WRITE STROBE signal is asserted low and the CS signal (pin 18) is asserted high, the data on the A/D lines will be written to the specified register. When the Motorola bus control interface is selected (the I/MC* signal (pin 24) is deasserted low), this signal acts as the R/W* signal. A high on this input along with the RD*/DS signal (pin 20) asserted and the CS signal (pin 18) asserted high indicates a read operation. A low on this input along with the RD*/DS signal (pin 20) asserted and the CS signal (pin 18) asserted high indicates a write operation.
RD*/DS	20	I	**READ STROBE/DATA STROBE:** When the Intel bus control interface is selected (the I/MC* signal (pin 24) is asserted high), this signal acts as the RD* signal. When the READ STROBE signal is asserted low and the CS signal (pin 18) is asserted high, the data from the specified register will be driven onto the A/D lines. When the Motorola bus control interface is selected (the I/MC* signal (pin 24) is deasserted low), this signal acts as the DS signal. A high on the R/W* signal along with this signal asserted and the CS signal (pin 18) asserted high indicates a read operation. A low on the R/W* signal along with this signal asserted and the CS signal (pin 18) asserted high indicates a write operation.

2.1 Microcontroller Interface Pins *(cont.)*

Symbol	QFP Pin No.	Type	Description
READY	21	O	**READY:** This is the microcontroller ready line. When this is deasserted low, the microcontroller shall insert wait states to allow time for the CL-SH351 to respond to the access.
I/MC*	24	I	**INTEL/MOTOROLA:** This signal selects the microcontroller interface to be used. When this signal is asserted high, it selects the Intel bus control interface. When this signal is deasserted low, it selects the Motorola bus control interface. This input signal may be legally 'floated' with the default selection of the Intel bus control interface. This pin is pulled up internally and will source current when pulled low.
HINT*	28	O, OD, Z	**HOST INTERRUPT:** This signal is a host interrupt line to the microcontroller. It is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-impedance state.
AD0:7	34-30 27 23-22	I/O	**LOCAL MICROCONTROLLER ADDRESS/DATA BUS:** These are tri-state Address/Data lines that interface with a multiplexed microcontroller Address/Data bus.
ALE	35	I	**ADDRESS LATCH ENABLE:** The trailing edge of this control signal latches the address on the A/D lines.
RST*	40	I	**RESET:** An asserted low input generates a component reset that stops all operations within the chip and deasserts all output signals. All input/output signals, the SCSI interface output signals and the HINT* signal (pin 28) and the DINT* signal (pin 17) are set to the high-impedance state. Refer to the section on register initialization (Section 5.3).

2.2 SCSI Bus Interface Pins

Symbol	QFP Pin No.	Type	Description
SDB0*:7*	52-54, 57 59-62	I/O, OD	**SCSI DATA BUS:** These eight signals comprise the SCSI data bus for information transfer.
SDBP*	64	I/O, OD	**SCSI DATA BUS PARITY:** This signal transfers odd parity of the SCSI data bus.
ATN*	68	I/O, OD	**SCSI ATTENTION:** This signal indicates the ATTENTION condition on the SCSI bus.
BSY*	69	I/O, OD	**SCSI BUSY:** This signal when asserted low indicates that the SCSI bus is being used.
ACK*	70	I/O	**SCSI ACKNOWLEDGE:** When this signal is asserted low, it indicates that the SCSI Initiator has acknowledged the data transfer.
SRST*	72	I/O, OD	**SCSI RESET:** This signal when asserted low indicates that the reset condition is on the SCSI bus.
MSG*	73	I/O, OD	**SCSI MESSAGE:** When this signal is asserted low, it indicates that the SCSI Message Phase is active on the SCSI bus.
SEL*	76	I/O, OD	**SCSI SELECT:** This signal is used by a SCSI Initiator to select a SCSI Target or by a SCSI Target to reselect a SCSI Initiator.
C*/D	77	I/O, OD	**SCSI COMMAND/DATA:** This signal indicates whether CONTROL (when asserted low) or DATA (when deasserted high) information is on the SCSI data bus signals.
REQ*	78	I/O	**SCSI REQUEST:** This signal when asserted low indicates that a request for a data transfer is active on the SCSI bus.
I*/O	79	I/O, OD	**SCSI INPUT/OUTPUT:** This signal controls the direction of data transfer on the SCSI data bus signals with respect to a SCSI Initiator. When this signal is asserted low, it indicates information input to the SCSI Initiator. When this signal is deasserted high, it indicates output from the SCSI Initiator. This signal is also used to distinguish between the SCSI Selection and the SCSI Reselection Phases.

2.3 SCSI Bus Control Pins

Symbol	QFP Pin No.	Type	Description
SDOE	50	O	**SCSI DATA BUS OUTPUT ENABLE:** This signal is asserted high when the SCSI data bus is to be driven by the CL-SH351.
INIT	55	O	**INITIATOR:** When this signal is asserted, it indicates that the CL-SH351 is an Initiator device active on the SCSI bus.
TAR	56	O	**TARGET:** When this signal is asserted, it indicates that the CL-SH351 is a Target device active on the SCSI bus.
AIP	63	O	**ARBITRATION IN PROGRESS:** When this signal is asserted, it indicates that the CL-SH351 is in the SCSI Arbitration Phase.
BSYO	67	O	**BUSY OUT:** This is the SCSI BUSY output signal. When this signal is asserted, it indicates that the CL-SH351 is driving the SCSI BUSY signal (pin 69).
SELO	71	O	**SELECT OUT:** This is the SCSI SELECT output signal. When it is asserted, it indicates that the CL-SH351 is driving the SCSI SELECT signal (pin 76).

2.4 Buffer Manager Interface Pins

Symbol	QFP Pin No.	Type	Description
BA17/CAS*	5	O	**BUFFER MEMORY ADDRESS 17/COLUMN ADDRESS STROBE:** This signal is used for addressing the buffer memory in SRAM Mode or as the column address strobe in DRAM Mode.
BA16/RAS*	14	O	**BUFFER MEMORY ADDRESS 16/ROW ADDRESS STROBE:** This signal is used for addressing the buffer memory in SRAM Mode or as the row address strobe in DRAM Mode.
MOE*	15	O	**MEMORY OUTPUT ENABLE:** This signal is asserted low when a buffer memory read operation is active in both SRAM and DRAM Modes.
WE*	16	O	**WRITE ENABLE:** This signal is asserted low when a buffer memory write operation is active in both SRAM and DRAM Modes.
MCE*	29	O	**MEMORY CHIP ENABLE:** In SRAM Mode, this signal is asserted low whenever buffer memory is active. It is recommended that this signal be connected to the SRAM chip enable for low-power operation.
SYSCLK	41	I	**SYSTEM CLOCK:** This is the clock input that is used to generate buffer memory access cycles. It is also used to control automatic SCSI timing operations.
BD0:7	83-87, 89, 92-93	I/O	**BUFFER MEMORY DATA BUS:** These eight signals are bits 0-7 of the 8-bit parallel data lines to/from the buffer memory.
BDP	94	I/O	**BUFFER MEMORY DATA PARITY:** This signal transfers odd parity of the buffer memory data bus to/from the buffer memory.
BA0:15	95-100 3, 4, 6-13	O	**BUFFER MEMORY ADDRESS LINES:** These are signals 0-15 for addressing the buffer memory.

2.5 Sector Formatter Interface Pins

Symbol	QFP Pin No.	Type	Description
INPUT	36	I	**FORMAT SEQUENCER INPUT:** This input signal is available to synchronize the Format Sequencer to an external event.
INDEX	37	I	**INDEX:** This is the input for the Index pulse received from the disk drive.
WAM*/ AMD*/ SECTOR	39	I/O	**WRITE ADDRESS MARK/ADDRESS MARK DETECT/SECTOR:** In Soft Sector Mode, a pulse is output when the WRITE GATE signal (pin 44) is asserted and an Address Mark is to be written. Also in Soft Sector Mode, when the READ GATE signal (pin 43) is asserted, a low-level input indicates an Address Mark was detected. In Hard Sector Mode, this is the input for the Sector pulse from the disk drive.
RG	43	O	**READ GATE:** This signal is asserted when a disk read operation is in progress and the NRZ data is input to the CL-SH351.
WG	44	O	**WRITE GATE:** This signal is used to enable the writing of NRZ data out to the storage device during a write operation.
RRCLK	45	I	**READ REFERENCE CLOCK:** This signal input clocks the NRZ data.
NRZ	46	I/O	**NON-RETURN TO ZERO:** This signal is the read data input from the disk drive when the READ GATE signal (pin 43) is asserted; it is the write data output to the disk drive when the WRITE GATE signal (pin 44) is asserted.
OUTPUT	47	O	**FORMAT SEQUENCER OUTPUT:** This output signal is available to synchronize the external hardware to the Format Sequencer. This signal is controlled by Bit 2 of the CONTROL FIELD of the Writable Control Store (WCS).

2.6 Power and Ground Pins

Symbol	QFP Pin No.	Type	Description
BGND†	1, 2, 88	N/A	Buffer Ground Pins
LGND†	25, 26, 42	N/A	Logic Ground Pins
N/C	48, 80, 81	N/A	No Connection; Reserved for Future Use
+5V	38, 51, 90, 91	N/A	Power Supply (+5).
SGND†	49, 58, 65-66, 74 75, 82	N/A	High-Current SCSI Ground Pins

NOTE: The superscript † indicates that SGND, BGND, and LGND are connected to three separate ground rings internally.

3. REGISTER TABLES

3.1 SCSI Interface Registers

Address	Type	Description/Function
40H/60H	R/W	DIRECT SCSI ACCESS PORT
41H/61H	R	SELECTION/RESELECTION ID INPUT
41H/61H	W	SELECTION/RESELECTION ID OUTPUT
42H/62H	R/W	SCSI PHASE CONTROL
43H/63H	R/W	SCSI SYNCHRONOUS CONTROL
44H/64H	R/W	SCSI MODE CONTROL
45H/65H	R/W	SCSI OPERATION CONTROL
46H/66H	R/W	SCSI STATUS REGISTER 1
47H/67H	R/W	SCSI INTERRUPT ENABLE REGISTER 1
48H	R/W	SCSI STATUS REGISTER 2
49H	R/W	SCSI INTERRUPT ENABLE REGISTER 2
4AH	R/W	MICROCONTROLLER SCSI FIFO ACCESS PORT
4BH	R/W	MISCELLANEOUS CONTROL/STATUS REGISTER

3.2 Buffer Manager Registers

Address	Type	Description/Function
50H	R/W	SCHEDULED BUFFER DATA
51H	R/W	BUFFER STATUS/CONTROL REGISTER
52H	R/W	BUFFER TRANSFER CONTROL
53H	R/W	BUFFER MODE CONTROL
54H	R/W	BUFFER MANAGER TIMING CONTROL
55H	R/W	DRAM REFRESH PERIOD
56H	R/W	SEGMENT SIZE
57H-59H	R/W	DISK ADDRESS POINTER
5AH-5CH	R/W	HOST ADDRESS POINTER
5DH-5FH	R/W	STOP ADDRESS POINTER

3.3 Sector Formatter Registers

Address	Type	Description/Function
4EH	R/W	SECTOR SIZE
4FH	R/W	SECTOR FORMATTER MODE CONTROL
70H	R/W	SYNCHRONIZATION BYTE-COUNT LIMIT
71H	R/W	ECC CONTROL
72H	R/W	ECC CORRECTION SHIFT-REGISTER/COUNTER
73H-76H	R	ECC STATUS
77H	R/W	SECTOR FORMATTER OPERATION CONTROL
78H	R	NEXT FORMAT SEQUENCER ADDRESS
78H	W	BRANCH ADDRESS
79H	R	FORMAT SEQUENCER STATUS REGISTER 1
79H	W	FORMAT SEQUENCER START ADDRESS
7AH	R	FORMAT SEQUENCER STATUS REGISTER 2
7BH	R/W	WAM CONTROL
7CH	R/W	SYNCHRONIZATION BYTE PATTERN
7DH	R/W	SECTOR FORMATTER INTERRUPT
7EH	R/W	SECTOR FORMATTER INTERRUPT ENABLE
7FH	R	SECTOR FORMATTER STACK
7FH	W	SYNCHRONIZATION COMPARE MASK

3.4 Writable Control Store (WCS) Fields

Address	Type	Description/Function
80H-9EH	R/W	NEXT ADDRESS FIELD
A0H-BEH	R/W	CONTROL FIELD
C0H-DEH	R/W	COUNT FIELD
E0H-FEH	R/W	DATA/BRANCH FIELD

3.5 Sequencer Registers

Address	Type	Description/Function
9FH	R/W	CURRENT SEQUENCER WORD — NEXT ADDRESS FIELD
BFH	R/W	CURRENT SEQUENCER WORD — CONTROL FIELD
DFH	R/W	CURRENT SEQUENCER WORD — COUNT FIELD
FFH	R/W	CURRENT SEQUENCER WORD — DATA/BRANCH FIELD

3.6 Register and Bit Table

Address	Type	Description/Function
40H/60H	R/W	**DIRECT SCSI ACCESS PORT**
41H/61H	R	**SELECTION/RESELECTION ID INPUT**
41H/61H	W	**SELECTION/RESELECTION ID OUTPUT**
42H/62H	R/W	**SCSI PHASE CONTROL**
		Bit 7 SCSI Acknowledge
		Bit 6 SCSI Attention
		Bit 5 SCSI Select
		Bit 4 SCSI Busy
		Bit 3 SCSI Request
		Bit 2 SCSI Message
		Bit 1 SCSI Input/Output*
		Bit 0 SCSI Control/Data*
43H/63H	R/W	**SCSI SYNCHRONOUS CONTROL**
		Bits 7-4 Synchronous Transfer Rate
		Bits 3-0 Offset Count
44H/64H	R/W	**SCSI MODE CONTROL**
		Bits 7-5 SCSI Logic Clock Prescalar
		Bit 4 SCSI Logic Clock Disable
		Bit 3 SCSI Parity Enable
		Bits 2-0 SCSI ID Bits
45H/65H	R/W	**SCSI OPERATION CONTROL**
		Bit 7 SCSI Reset Out
		Bit 6 Test Mode
		Bit 5 Enable Initiator
		Bit 4 Enable Target
		Bit 3 Microcontroller Direct SCSI Output Enable
		Bit 2 SCSI Automatic Selection/Reselection Mode
		Bit 1 SCSI Automatic Selection/Reselection Enable
		Bit 0 Arbitration/Selection Start
46H/66H	R/W	**SCSI STATUS REGISTER 1**
		Bit 7 SCSI RST In
		Bit 6 SCSI Parity Error
		Bit 5 SCSI Bus Parity Error Detected
		Bit 4 SCSI/Buffer Parity Error Detected
		Bit 3 SCSI Bus Free Detected
		Bit 2 SCSI Offset Overrun/Underrun Detected
		Bit 1 SCSI Attention Detected
		Bit 0 SCSI Reset Detected
47H/67H	R/W	**SCSI INTERRUPT ENABLE REGISTER 1**
		Bits 7-6 Reserved
		Bit 5 SCSI Bus Parity Error Enable
		Bit 4 SCSI/Buffer Parity Error Enable
		Bit 3 SCSI Bus Free Detected Enable
		Bit 2 Offset Overrun/Underrun Enable
		Bit 1 Attention Detected Enable
		Bit 0 SCSI Reset Detected Enable

3.6 Register and Bit Table *(cont.)*

Address	Type	Description/Function
48H	R/W	**SCSI STATUS REGISTER 2**
		Bit 7 Req-On
		Bit 6 SCSI Phase Mismatch
		Bit 5 Transfer Halted
		Bit 4 Transfer Done
		Bit 3 Automatic Selecting/Reselecting Done
		Bit 2 Arbitration Won
		Bit 1 Device Reselected
		Bit 0 Device Selected
49H	R/W	**SCSI INTERRUPT ENABLE REGISTER 2**
		Bit 7 Req-On Enable
		Bit 6 SCSI Phase Mismatch Enable
		Bit 5 Transfer Halted
		Bit 4 Transfer Done Enable
		Bit 3 Automatic Selecting/Reselecting Enable
		Bit 2 Arbitration Won Enable
		Bit 1 Device Reselected Enable
		Bit 0 Device Selected Enable
4AH	R/W	**MICROCONTROLLER SCSI FIFO ACCESS PORT**
4BH	R/W	**MISCELLANEOUS STATUS/CONTROL REGISTER**
4CH	R/W	**Reserved**
4DH	R/W	**Reserved**
4EH	R/W	**SECTOR SIZE**
4FH	R/W	**SECTOR FORMATTER MODE CONTROL**
		Bit 7 Split Field Mode Disable
		Bit 6 Local INT* Mode Enable
		Bit 5 Hard/Soft* Sector Mode Control
		Bit 4 SCSI Interface Register Decode Select
		Bit 3 Local INT* Pin Pull-up Disable
		Bit 2 Local DINT* Enable
		Bit 1 Local HINT* Enable
		Bit 0 Sector Formatter Reset
50H	R/W	**SCHEDULED BUFFER DATA**
51H	R/W	**BUFFER STATUS/CONTROL REGISTER**
		Bit 7 SCSI Active Pull Up Select
		Bit 6 SYNC SCSI Data Set Up Select
		Bit 5 SCSI Data Set Up Select
		Bit 4 Clear FIFO
		Bits 3-0 Synchronous Data Transfer Offset
52H	R/W	**BUFFER TRANSFER CONTROL**
		Bits 7-4 PIO Transfer Count
		Bit 3 SCSI R/W* Transfer Direction
		Bit 2 PIO Start
		Bit 1 DMA Start
		Bit 0 Reserved

3.6 Register and Bit Table *(cont.)*

Address	Type	Description/Function
53H	R/W	**BUFFER MODE CONTROL**
		Bits 7-6 Wait States
		Bit 5 Host/Buffer Reset
		Bit 4 MOE Disable
		Bit 3 Buffer Memory Parity Enable
		Bits 2-1 DRAM Type
		Bit 0 DRAM/SRAM*
54H	R/W	**BUFFER MANAGER TIMING CONTROL**
		Bits 7-6 CAS* High Time
		Bits 5-4 CAS* Low Time
		Bits 3-2 RAS* High Time
		Bits 1-0 RAS* Low Time/SRAM Cycle Time
55H	R/W	**DRAM REFRESH PERIOD**
56H	R/W	**SEGMENT SIZE**
57H-59H	R/W	**DISK ADDRESS POINTER**
5AH-5CH	R/W	**HOST ADDRESS POINTER**
5DH-5FH	R/W	**STOP ADDRESS POINTER**
70H	R/W	**SYNCHRONIZATION BYTE-COUNT LIMIT**
71H	R/W	**ECC CONTROL**
		Bit 7 Reserved
		Bit 6 32/56 Bit ECC Select
		Bit 5 Reserved
		Bit 4 Correctable Error Found
		Bit 3 Initialize ECC
		Bit 2 Disable ECC Feedback
		Bit 1 ECC Shift Control
		Bit 0 ECC Syndrome Reversal/Correction Control
72H	R/W	**ECC CORRECTION SHIFT-REGISTER/COUNTER**
73H-76H	R	**ECC STATUS**
77H	R/W	**SECTOR FORMATTER OPERATION CONTROL**
		Bit 7 Reserved
		Bit 6 Two Index Detection Mode Enable
		Bit 5 Edge Detect Sensitivity Selection
		Bit 4 Inhibit Data Field Carry
		Bit 3 Buffer/Disk R/W* Transfer Direction
		Bit 2 Suppress Transfer
		Bit 1 Data/Branch Field Mode Enable
		Bit 0 Enable Sector Branch
78H	R	**NEXT FORMAT SEQUENCER ADDRESS**
		Bits 7-5 Reserved
		Bits 4-0 Next Active Format Sequencer Address
78H	W	**BRANCH ADDRESS**
		Bits 7-5 Reserved
		Bits 4-0 Branch Address

3.6 Register and Bit Table *(cont.)*

Address	Type	Description/Function
79H	R	**FORMAT SEQUENCER STATUS REGISTER 1**
		Bit 7 Byte Ready
		Bit 6 Format Sequencer Output
		Bit 5 Format Sequencer Input
		Bit 4 Synchronization Detect Status
		Bit 3 Branch Active
		Bit 2 Data Transfer
		Bit 1 AM Active
		Bit 0 Format Sequencer Active
79H	W	**FORMAT SEQUENCER START ADDRESS**
		Bits 7-5 Reserved
		Bits 4-0 Start Address
7AH	R	**FORMAT SEQUENCER STATUS REGISTER 2**
		Bit 7 Reserved
		Bit 6 Disk/Buffer Parity Error
		Bit 5 Two Index Detected
		Bit 4 Synchronization Time-Out Error
		Bit 3 Data Field ECC Error
		Bit 2 ECC Error
		Bit 1 Secondary Compare Not Equal
		Bit 0 Primary Compare Not Equal
7BH	R/W	**WAM CONTROL**
7CH	R/W	**SYNCHRONIZATION BYTE PATTERN**
7DH	R/W	**SECTOR FORMATTER INTERRUPT**
		Bit 7 Secondary Miscompare Detected
		Bit 6 Sequencer Output Detected
		Bit 5 Data Transfer Detected
		Bit 4 Branch Active Detected
		Bit 3 Sequencer Stopped Detected
		Bit 2 Input Detected
		Bit 1 Sector Detected
		Bit 0 Index Detected
7EH	R/W	**SECTOR FORMATTER INTERRUPT ENABLE**
		Bit 7 Secondary Miscompare Detected Enable
		Bit 6 Sequencer Output Detected Enable
		Bit 5 Data Transfer Detected Enable
		Bit 4 Branch Active Detected Enable
		Bit 3 Sequencer Stopped Detected Enable
		Bit 2 Input Detected Enable
		Bit 1 Sector Detected Enable
		Bit 0 Index Detected Enable
7FH	R	**SECTOR FORMATTER STACK**
7FH	W	**SYNCHRONIZATION COMPARE MASK**

3.6 Register and Bit Table *(cont.)*

Address	Type	Description/Function
80H-9EH	R/W	**WCS NEXT ADDRESS FIELD** Bits 7-5 Branch Command Bits 4-0 Next Address
9FH	R/W	**CURRENT SEQUENCER WORD — NEXT ADDRESS FIELD**
A0H-BEH	R/W	**WCS CONTROL FIELD** Bit 7 Alternate Branch Command Select Bits 6-5 Control Field Bit 4 Stack Enable Bit 3 Process Split/Invalid NRZ Control Bit 2 Output Bit 1 Compare Enable Bit 0 Data Transfer
BFH	R/W	**CURRENT SEQUENCER WORD — CONTROL FIELD**
C0H-DEH	R/W	**WCS COUNT FIELD** Bit 7 Count/Process AM Bit 6 Count/Process ECC Bit 5 Count/Start Synchronization Timer/Secondary Compare Enable/Two Index Timer Bit 4 Count/CRC Select Bits 3-0 Count
DFH	R/W	**CURRENT SEQUENCER WORD — COUNT FIELD**
E0H-FEH	R/W	**WCS DATA/BRANCH FIELD**
FFH	R/W	**CURRENT SEQUENCER WORD — DATA/BRANCH FIELD**

4. FUNCTIONAL DESCRIPTION

Within high-performance, intelligent, disk drive controller subsystems, the CL-SH351 is the VLSI component that enables the local microcontroller to offload all of the disk controller real-time tasks. Consequently, the microcontroller can execute commands at a higher level by parsing the command into lower level, high-speed tasks. These lower level, high-speed tasks are, in turn, completely managed by the CL-SH351.

As the block diagram on the cover page indicates, the component can be divided into the following four functional blocks:

- **Microcontroller**
- **SCSI Host**
- **Buffer Manager**
- **Sector Formatter**

Each of these functional logic blocks has an associated interface that is specifically designed to manage the operation of the external devices and buses. In order to provide this support, each interface uses information that is programmed by the local microcontroller in advance of the required operations.

4.1 Microcontroller Interface

A number of features have been included in the microcontroller interface to enable the CL-SH351 to operate with a variety of high-speed microcontrollers. For example, the CL-SH351 has a configuration signal called the I/MC* signal (pin 24) that allows for either the Intel or the Motorola method of data control to be used. Through the CL-SH351 microcontroller interface, all of its registers are read or written, and the Writable Control Store (WCS) is programmed for the required operations of any sector and track format.

Microcontroller Interface to the CL-SH351

The microcontroller-to-CL-SH351 communication path is a multiplexed, 8-bit address and data bus similar to that provided by the Intel 8051- and the Motorola 68HC11-class of controllers. The CL-SH351 can use either the Intel or the Motorola method of data control. If the I/MC* configuration signal (pin 24) is connected to power or is left unconnected, then the component uses the Intel method of data control. When the Intel interface is selected, the WR*/R/W* signal (pin 19) acts as a write strobe. In the case of a write operation, this write strobe provides the timing and control for the data transfers. Similarly, in the case of a read operation, the RD*/DS signal (pin 20) acts as a read strobe to provide the timing and the control for the data transfers.

If the I/MC* signal (pin 24) is connected to ground, then the Motorola interface is assumed. This configuration converts the WR*/R/W* signal (pin 19) into a control signal that is used *only* to determine the direction of the data transfer. When the input to this signal is high, a read operation is in progress; when it is low, a write operation is in progress. Data timing is derived with respect to the RD*/DS signal (pin 20). In the case of a read operation, the rising (leading) edge of the RD*/DS signal (pin 20) indicates when the CL-SH351 can start driving the data bus. In the case of a write operation, the falling (trailing) edge is used by the CL-SH351 to latch the data from the microcontroller address/data bus.

The CL-SH351 can also generate wait states to the local microcontroller through its READY signal (pin 21). This permits microcontrollers with a wait state input to operate the disk controller system bus without any loss of performance, if the microcontroller can normally perform read or write accesses faster than the CL-SH351 permits. The component powers up with the maximum number of wait states inserted into every microcontroller access. The microcontroller can

then program either no wait states or the actual number of wait states required by the system microcontroller.

Microcontroller-to-Buffer Manager Interface

In order to write a byte to the buffer memory, the microcontroller loads the CL-SH351 Port 50H (the SCHEDULED BUFFER DATA Register) with the data to be written to the buffer memory. This generates a transfer request to the Buffer Manager which will grant a prioritized buffer memory access cycle. When the byte has been successfully written, the BYTE READY bit (Register 79H, bit 7) will be set. Reading a byte from the buffer memory is initiated by having the microcontroller read Port 50H (the SCHEDULED BUFFER DATA Register). This first byte is discarded because it is a dummy read. When the status for byte ready becomes valid (the BYTE READY bit (Register 79H, bit 7) is set), then the first valid byte which is the byte pointed to by the Disk Address Pointer (Registers 57H-59H) has been read into Port 50H (the SCHEDULED BUFFER DATA Register). When that byte is read, the read strobe causes an automatic request for another buffer memory access cycle. This request causes the byte located at the next address pointed to by the Disk Address Pointer (Registers 57H-59H) to be fetched. Note that the Disk Address Pointer (Registers 57H-59H) is automatically incremented after each access.

Switches or jumpers for user-configurable options can be implemented on the buffer memory data bus. The logical value of these switches is read in much the same way that a byte of data is read from the buffer memory. However, the MEMORY OUTPUT ENABLE signal (MOE* — pin 15) should be disabled for both SRAM and DRAM Modes, and the BA16/RAS* (pin 14) and the BA17/CAS* (pin 5) signals should be disabled in DRAM Mode to prevent the buffer memory from driving the bus. (The MOE* signal (pin 15), the BA16/RAS* signal (pin 14), and the BA17/CAS* signal (pin 5) can be disabled by setting the MOE DISABLE bit (Register 53H, bit 4).

Microcontroller-to-SCSI Interface

There are two methods that the local microcontroller can use to access the SCSI data bus: (1) transfers that are controlled completely by the firmware, or (2) Programmed I/O (PIO) transfers that use the CL-SH351 FIFO.

In the first method, a single byte at a time is transferred, and the transfer is handled completely by the firmware. Using firmware control to handshake and read or write each byte to the SCSI data bus is appropriate for particular SCSI Bus Phases such as the Message In Phase or the Message Out Phase. This transfer method allows the microcontroller to monitor the SCSI ATTENTION signal (ATN* — pin 68) on a byte-by-byte basis (monitoring of the SCSI ATTENTION signal is a requirement of the SCSI-2 protocol during message transfers when a device is operating in Target Mode).

For firmware-controlled accesses, the information bytes are either read or written through the DIRECT SCSI ACCESS PORT (Register 40H/60H). The SCSI REQUEST signal (REQ* — pin 78) and the SCSI ACKNOWLEDGE signal (ACK* — pin 70) are controlled and monitored in the SCSI PHASE CONTROL Register (42H/62H). The SCSI Phase is set in advance of the transfer in the SCSI PHASE CONTROL Register (42H/62H).

In the second method, the CL-SH351 16-byte FIFO is used for automatic Programmed I/O (PIO) transfers. This permits automatic handshaking of the SCSI REQUEST signal (REQ* — pin 78) and the SCSI ACKNOWLEDGE signal (ACK* — pin 70) which allows up to 15 bytes of information to be transferred without any microcontroller intervention. This method of transfer is useful, for example, in the SCSI Command Phase in order

to bring in the first six bytes of a command. In fact, because most SCSI commands are six bytes long, this transfer method will bring in all of the command. Programmed I/O (PIO) transfers can be asynchronous or synchronous. For example, asynchronous transfers would be used to transfer a command; whereas, synchronous transfers (if the negotiation is still valid) would be used to transfer the data requested by an Initiator.

The microcontroller always accesses the CL-SH351 FIFO for reads or writes through the MICROCONTROLLER SCSI FIFO ACCESS PORT (Register 4AH). The Programmed I/O (PIO) transfer count, control, and direction are all managed in the BUFFER TRANSFER CONTROL Register (52H).

The CL-SH351 Local Microcontroller Interface

Interrupts and status to the local microcontroller are consistently implemented from all four of the CL-SH351 functional blocks. The SCSI Host and the Buffer Manager interrupts are located in the SCSI Status Registers (46H/66H and 48H). The Sector Formatter interrupts are located in the SECTOR FORMATTER INTERRUPT Register (7DH).

The SCSI Host and the Buffer Manager interrupts have their own dedicated interrupt signal output to the microcontroller via the CL-SH351 HINT* signal (pin 28). The Sector Formatter interrupts also have their own dedicated interrupt signal output to the microcontroller via the CL-SH351 DINT* signal (pin 17). This permits the microcontroller to localize the source of the interrupt or the pending status much quicker than if all of the interrupts were connected to the same interrupt output. If the local microcontroller permits only one interrupt signal, then these interrupt sources collectively can be configured to drive only one interrupt output signal by setting the LOCAL INT* MODE ENABLE bit (Register 4FH, bit 6).

In addition, each SCSI Host and Buffer Manager status bit can be masked individually via the SCSI Interrupt Enable Registers (47H/67H and 49H). Each Sector Formatter status bit can also be masked individually via the SECTOR FORMATTER INTERRUPT ENABLE Register (7EH). Because of this masking capability, the bit can be prevented from generating an interrupt, yet it still can provide status information to the microcontroller that is operating in Polled Mode. The interrupt output signals can be configured for open-drain operation in a multiplexed interrupt system by setting the LOCAL INT* PIN PULL-UP DISABLE bit (Register 4FH, bit 3). Interrupts can be disabled completely by resetting the interrupt enables. Interrupts are enabled by setting the LOCAL HINT* ENABLE bit and the LOCAL DINT* ENABLE bit (bits 1 and 2, respectively, of the SECTOR FORMATTER MODE CONTROL Register (4FH)). Interrupts are disabled by resetting bits 1 and 2 of Register 4FH.

4.2 SCSI Functional Description

The second functional logic block of the CL-SH351 is the CL-SH351 Small Computer System Interface (SCSI). The control, timing, interface and data transfer sections of this interface adhere to the requirements of the SCSI-2 proposed specification as well as to the ANSI X3.131-1986 SCSI specification. It is assumed that the reader is familiar with these requirements; otherwise, it is assumed that the ANSI document will be used in conjunction with Section 4.2.

The SCSI interface is the means of communication between a host computer system and one or more peripheral devices. A SCSI device assumes one of two roles in any SCSI bus communication. The Initiator is defined as the SCSI device that generates a process, or, more

specifically, the nexus. The Target is the recipient of the Initiator request and must execute some operation in response to an Initiator request.

The SCSI bus is an intermediate physical construct between the host system and the attached peripheral device(s). The host system uses an interface circuit to gain access to the SCSI bus. Previously, the peripheral device usually required external interface circuitry to connect to the SCSI bus. In the case of the CL-SH351, however, all of the required interface, timing, control and data paths are included in one integrated circuit.

The majority of the activity on the SCSI bus is with the host system computer acting as an Initiator that issues commands to a Target device such as a disk controller. It is through a well-defined protocol that the Initiator can request data reads or writes and other more sophisticated operations of the Target. It is permissible for a Target to assume the role of an Initiator and vice versa.

Overview of the CL-SH351 SCSI Capabilities

Implementation of the SCSI Bus Phases can be cumbersome. Consequently, many of these often-repeated processes are designed into the CL-SH351 control logic. Such routine SCSI bus control operations as arbitration, selection and reselection are automatically sequenced in the CL-SH351 hardware; this results in more automated handling and ease of use.

The firmware engineer, however, still must program a SCSI ID for the device into bits 2-0 of the SCSI MODE CONTROL Register (44H/64H). The CL-SH351 can be programmed to assume either the role of an Initiator or a Target. For firmware-controlled operations, the selection of a Target or Initiator is controlled by setting either the ENABLE TARGET bit or the ENABLE INITIATOR bit (bits 4 and 5, respectively, in Register 45H/65H). Otherwise, the Target or Initiator role is derived from the programmed automatic operation (e.g., the selection, reselection, selection detected, or reselection detected process).

Microcontroller-to-SCSI-Bus Connection

The local microcontroller is allowed access to the SCSI data bus through two distinct CL-SH351 address ports — (1) Port 40H/60H (the DIRECT SCSI ACCESS PORT Register), and (2) Port 4AH (the MICROCONTROLLER SCSI FIFO ACCESS PORT Register). The accesses can be handled singly under direct firmware control or by an automatic Programmed I/O (PIO) circuit in the event of multiple bytes. In the latter case, the data is stored or received in the CL-SH351 16-byte FIFO.

The local microcontroller is provided access to the SCSI bus through addressing Port 40H/60H (the DIRECT SCSI ACCESS PORT Register). The microcontroller can either read or write data directly to the SCSI bus through this port. The 16-byte FIFO is given a separate port address so that the hardware can automatically distinguish the type of microcontroller to SCSI bus access. The FIFO must be addressed by writing or reading Port 4AH (the MICROCONTROLLER SCSI FIFO ACCESS PORT Register). The FIFO can be used for stacking messages, sense data, or any other concurrent information transfer that would not constitute a DMA data transfer. The direction of the information transfer is controlled by the SCSI R/W* TRANSFER DIRECTION bit (Register 52H, bit 3). This applies to both DMA transfers (refer to the section *SCSI Data Transfers*), as well as automatic Programmed I/O (PIO) transfers through the FIFO.

For the Programmed I/O (PIO) mode of operation the REQ*/ACK* handshake is handled automatically by an internal CL-SH351 state machine. In the case of reading information from the bus, the expected or minimum number of bytes to be read should be loaded into the PIO TRANSFER COUNT field (Register 52H, bits 7-4). In the case of writing bytes to the SCSI bus, the exact

number of bytes to be written is always known, so that the number of bytes for the Programmed I/O (PIO) transfer should be loaded into the PIO TRANSFER COUNT field (Register 52H, bits 7-4).

Before commencing with any new operation that will use the FIFO, the FIFO must be cleared by setting the CLEAR FIFO bit (bit 4) and then resetting this bit of the BUFFER STATUS/CONTROL Register (51H). The sequence is then started by setting the PIO START bit (bit 2) of the BUFFER TRANSFER CONTROL Register (52H). The byte count in the FIFO can be obtained by reading the count in bits 7-4 of Register 52H. The PIO START bit (Register 52H, bit 2) is automatically reset when the FIFO count has reached zero.

Programmed I/O (PIO) transfers can be either asynchronous or synchronous. If the information being transferred is data, and a previous synchronous negotiation is still in effect, then the Programmed I/O (PIO) transfer should be configured for synchronous transfers (refer to the section *SCSI Data Transfers*).

SCSI Phase Control

The majority of the SCSI Phase control and detection can be handled under the hardware control of the CL-SH351 if the CL-SH351 is programmed accordingly. The SCSI Arbitration Phase is automatically started by setting the ARBITRATION/SELECTION START bit (Register 45H/ 65H, bit 0). After waiting the appropriate Bus Free delay, the CL-SH351 ID bit driven onto the SCSI bus during the SCSI Arbitration Phase is derived from the encoded bits 2-0 of the SCSI MODE CONTROL Register (44H/64H). Arbitration has been won when the ARBITRATION/ SELECTION START bit (Register 45H/65H, bit 0) resets itself or the ARBITRATION WON bit (Register 48H, bit 2) is set. If arbitration was lost, the CL-SH351 continues to arbitrate for control of the SCSI bus until arbitration has been won, or until the ARBITRATION/SELECTION START bit (Register 45H/65H, bit 0) is reset by the local microcontroller.

Whether the SCSI Selection Phase or the SCSI Reselection Phase is the pending phase (one or the other is the only possible phase after the SCSI Arbitration Phase), both the CL-SH351 ID and the desired Target or Initiator ID bit must be set by writing to the SELECTION/RESELECTION ID OUTPUT Register (41H/61H).

The SCSI Selection or Reselection Phases are allowed to start automatically after a successful SCSI Arbitration Phase by setting the SCSI AUTOMATIC SELECTION/RESELECTION ENABLE bit (Register 45H/65H, bit 1). For the SCSI Selection Phase, the SCSI AUTOMATIC SELECTION/RESELECTION MODE bit (Register 45H/65H, bit 2) must be set. To go to the SCSI Reselection Phase, the SCSI AUTOMATIC SELECTION/RESELECTION MODE bit (Register 45H/65H, bit 2) must be reset.

If the device is an Initiator, then the SCSI Selection Phase is the appropriate SCSI Bus Phase to follow arbitration. The SCSI ATTENTION bit (bit 6) of the SCSI PHASE CONTROL Register (42H/62H) should be set such that the SCSI ATTENTION signal (pin 68) is automatically asserted low during the SCSI Selection Phase. This should be done before setting the SCSI AUTOMATIC SELECTION/RESELECTION ENABLE bit (Register 45H/65H, bit 1). Having set the SCSI AUTOMATIC SELECTION/RESELECTION ENABLE bit (bit 1) of the SCSI OPERATION CONTROL Register (45H/65H), the CL-SH351 will then proceed to the SCSI Selection Phase.

If the device is a Target, then the SCSI Reselection Phase is the next phase to follow arbitration. Having set the SCSI AUTOMATIC SELECTION/RESELECTION ENABLE bit (bit 1) of the SCSI OPERATION CONTROL Register (45H/65H), the CL-SH351 will then proceed to the SCSI Reselection Phase.

The CL-SH351 will also perform the converse of these functions automatically if the SCSI AUTOMATIC SELECTION/RESELECTION ENABLE bit (Register 45H/65H, bit 1) is set. That is, if the CL-SH351 is being selected by an Initiator, it will detect that it is being selected and will set the DEVICE SELECTED bit (bit 0) in the SCSI STATUS REGISTER 2 (48H). In addition, the CL-SH351 will respond to the selection by: (1) setting the ENABLE TARGET bit (bit 4) of the SCSI OPERATION CONTROL Register (45H/65H), (2) asserting low the SCSI BUSY signal (pin 69), (3) setting the SCSI BUSY bit (bit 4) of the SCSI PHASE CONTROL Register (42H/62H), and (4) latching the contents of the SCSI data bus into the SELECTION/ RESELECTION ID INPUT Register (41H/61H).

If a valid reselection by a Target is observed on the bus, the CL-SH351 will set the DEVICE RESELECTED bit (bit 1) of the SCSI STATUS REGISTER 2 (48H). The CL-SH351 will also do the following: (1) set the ENABLE INITIATOR bit (Register 45H/65H, bit 5), (2) assert the SCSI BUSY signal (pin 69) low and set the SCSI BUSY bit (bit 4) of the SCSI PHASE CONTROL Register (42H/62H) until the SCSI SELECT signal (pin 76) is asserted low, and (3) latch the contents of the SCSI data bus into the SELECTION/RESELECTION ID INPUT Register (41H/61H).

If the control of the SCSI Selection or Reselection Phase is performed through firmware operations, then the SCSI control signals are qualified with one of two bits — the ENABLE TARGET bit or the ENABLE INITIATOR bit (bits 4 and 5, respectively, of Register 45H/65H).

The ENABLE TARGET bit (Register 45H/65H, bit 4) is set to allow the CL-SH351 to drive the following Target signals: the SCSI MESSAGE signal (pin 73), the SCSI COMMAND/DATA signal (pin 77), the SCSI INPUT/OUTPUT signal (pin 79), and the SCSI REQUEST signal (pin 78). These signals can be individually controlled or monitored in the SCSI PHASE CONTROL Register (42H/62H).

The ENABLE INITIATOR bit (Register 45H/65H, bit 5) is set to allow the CL-SH351 to drive the following Initiator signals: the SCSI ATTENTION signal (pin 68) and the SCSI ACKNOWLEDGE signal (pin 70). These two signals can be controlled or monitored through the SCSI PHASE CONTROL Register (42H/62H).

The SCSI BUSY signal (pin 69) and the SCSI SELECT signal (pin 76) that are controlled by bits 4 and 5 of Register 42H/62H are not gated by either the ENABLE TARGET bit or the ENABLE INITIATOR bit (bits 4 and 5, respectively, of Register 45H/65H). The SCSI SELECT signal (pin 76) can be driven to allow for a firmware-controlled SCSI Selection Phase in Initiator Mode or a SCSI Reselection Phase in Target Mode. This also permits the SCSI BUSY signal (pin 69) to be asserted low by the firmware in response to being selected or reselected, yet still allows the CL-SH351 to assert this signal for automatic arbitration.

Because the SCSI data bus must be driven with the Initiator and Target ID values during the SCSI Selection and Reselection Phases, the MICROCONTROLLER DIRECT SCSI OUTPUT ENABLE bit (Register 45H/65H, bit 3) must be set before setting the ENABLE TARGET bit or the ENABLE INITIATOR bit (bits 4 and 5, respectively, of Register 45H/65H). This allows the SCSI data bus to be driven, provided that the ENABLE INITIATOR bit or the ENABLE TARGET bit is set during the selection or reselection process.

The RST* signal (pin 40) has a more global effect on the function of the SCSI bus, and can be asserted low at anytime by setting the SCSI RESET OUT bit (bit 7) of the SCSI OPERATION CONTROL Register (45H/65H).

SCSI Information Transfer Phases

All SCSI Bus Phases, other than the Arbitration, Selection, and Reselection Phases, are collectively defined as Information Transfer Phases.

The Information Transfer Phase is always set by the Target device during communication with an Initiator. The phase is defined by the encoded values of the following SCSI signals: the SCSI COMMAND/DATA signal (pin 77), the SCSI INPUT/OUTPUT signal (pin 79), and the SCSI MESSAGE signal (pin 73). The Information Transfer Phase is set through firmware by the local microcontroller for the particular Target. The ENABLE TARGET bit (Register 45H/65H, bit 4) must be set, either in firmware, or through an automatic selection or selection detected process before these signals are actively driven by the CL-SH351. Note that the corresponding bits in the SCSI PHASE CONTROL Register (42H/62H) for the SCSI COMMAND/DATA signal (pin 77), the SCSI INPUT/OUTPUT signal (pin 79), and the SCSI MESSAGE signal (pin 73) are the logical complement of the levels on the bus, because the SCSI bus is an active low bus.

Bit 0 of the SCSI PHASE CONTROL Register (42H/62H) is the SCSI CONTROL/DATA* bit. When this bit is set, it indicates that the information being transferred on the SCSI data bus signals is either command, status, or message byte(s). Resetting this bit to a logical zero indicates that the information being transferred is data byte(s).

Bit 1 of the SCSI PHASE CONTROL Register (42H/62H) is the SCSI INPUT/OUTPUT* bit. This bit indicates the direction of information transfer with respect to the Initiator. When this bit is set to a logical one, the information will be transferred in to the Initiator. Resetting this bit to a logical zero indicates that the information will be transferred out from the Initiator to the Target.

Bit 2 of the SCSI PHASE CONTROL Register (42H/62H) is the SCSI MESSAGE bit. When this bit is set, it indicates that the information transfer is specifically a SCSI message. When this bit is reset, then the information could be data, a command, or status. A SCSI message could be either a Message In to the Initiator or a Message Out to the Target.

The following table lists the permissible Information Transfer Phases for the encoded states of bits 2-0 of the SCSI PHASE CONTROL Register (42H/62H).

Information Transfer Phase Control Bits

Register 42H/62H			
Bit 2	**Bit 0**	**Bit 1**	
MSG	C/D*	I/O*	Information Transfer Phase
0	0	0	Data Out Phase
0	0	1	Data In Phase
0	1	0	Command Out Phase
0	1	1	Status In Phase
1	0	0	Undefined
1	0	1	Undefined
1	1	0	Message Out Phase
1	1	1	Message In Phase

As a Target, the CL-SH351 can go to a SCSI Message In Phase at any time by setting the three bit values, as shown in the table above. As an Initiator, however, the CL-SH351 has no control over these three bits. As an Initiator to request a SCSI Message Out Phase, the local microcontroller should set the SCSI ATTENTION bit (bit 6) of the SCSI PHASE CONTROL Register (42H/62H). The Target device should respond by setting the phase to a SCSI Message Out Phase at the earliest possible time.

These three Information Transfer Phase control bits can also be used by the Initiator to read their value, if required. They will provide status to the Initiator if the Target changes one or more of their values to an Information Transfer Phase that the Initiator is not expecting.

In the execution of most SCSI nexus, the Initiator can predict the next phase of operation. For example, from the SCSI Command Phase, depending on the command, the Target will typically enter a SCSI Status Phase or Data Phase. The Initiator can predict this from the command sent. When in Initiator Mode, the CL-SH351 provides a status signal or an interrupt, if

the Target device drives to a SCSI Bus Phase that the Initiator does not expect (e.g., the Message In Phase). A transfer will not occur to prevent erroneous information transfer.

Bits 2-0 of Register 42H/62H should be set by the Initiator microcontroller to the predicted state. That is, the expected Information Transfer Phase should be encoded using the SCSI MESSAGE bit, the SCSI INPUT/OUTPUT* bit, and the SCSI CONTROL/DATA* bit (bits 2-0, respectively, of Register 42H/62H). On each falling (leading) edge of the SCSI REQUEST signal (pin 78), the CL-SH351 compares the Target-driven Phase against the predicted state programmed in the CL-SH351. If any one of the three signals differ from the bits preprogrammed by the Initiator, then the SCSI PHASE MISMATCH bit (bit 6) of the SCSI STATUS REGISTER 2 (48H) will be set.

These bits can be read at anytime by either an Initiator or a Target. The values read always reflect the logical complement of the value on the CL-SH351 SCSI bus pin.

SCSI Data Transfers

SCSI data is transferred either during a SCSI Data In or Data Out Phase. This is done either by an Initiator or a Target, with the Target device controlling the data transfer. The major features in the CL-SH351 to improve data integrity, ease of implementation, and performance include the following: odd parity generation and detection, a 16-byte FIFO, an automatic DMA Transfer Mode, and both asynchronous and synchronous data transfers with the option of either a single-ended or differential bus connection.

SCSI parity checking is enabled by setting the SCSI PARITY ENABLE bit (Register 44H/64H, bit 3). Parity generation is not affected by the value of the SCSI PARITY ENABLE bit (Register 44H/64H, bit 3). If a parity error is detected during a data transfer, then the SCSI BUS PARITY ERROR DETECTED bit (bit 5) of the SCSI STATUS REGISTER 1 (46H/66H) is set. A parity error can only be detected on the SCSI bus when data is being read from the other device whether it is a Target or Initiator.

In addition to SCSI bus parity, there is a parity circuit between the internal CL-SH351 SCSI bus and the RAM data buffer port. This parity detection circuitry is enabled if the BUFFER MEMORY PARITY ENABLE bit (bit 3) of the BUFFER MODE CONTROL Register (53H) is set. This ensures the integrity of the data being read from the RAM data buffer to the CL-SH351 SCSI interface logic. If a parity error is detected, it is latched in the SCSI/BUFFER PARITY ERROR DETECTED bit (bit 4) of the SCSI STATUS REGISTER 1 (46H/66H).

Internal to the CL-SH351 and transparent to the user is a 16-byte, bidirectional FIFO used in data reads or writes with the RAM data buffer. This FIFO acts as a buffer between the host (SCSI) transfer rate and the rate at which data is written to or read from the buffer memory. The FIFO is useful for preventing overruns or underruns, as its status is used to control the assertion low of the SCSI REQUEST signal (pin 78) as a Target or the assertion low of the SCSI ACKNOWLEDGE signal (pin 70) as an Initiator.

The transfer of data is under the control of an automatic state sequencer which allows for the ability of a high-speed, DMA transfer to or from the RAM data buffer. DMA data transfers are enabled by setting the DMA START bit (bit 1) in the BUFFER TRANSFER CONTROL Register (52H). This bit is reset at the completion of a DMA transfer. A DMA transfer that is in progress can be cleanly terminated by resetting the DMA START bit (Register 52H, bit 1).

The CL-SH351 is capable of asynchronous data transfers up to 3 Mbytes/second, and synchronous data transfers up to 10 Mbytes/second. Synchronous transfers are established through a defined message protocol. The two parameters that must be agreed upon between the Initiator and Target are an offset

count and a synchronous transfer period. It is incumbent on the local microcontroller to arrive at compatible parameters with the other SCSI device. The parameters can then be programmed into the SCSI SYNCHRONOUS CONTROL Register (43H/63H). The offset count can be loaded with values from 1 to 15 bytes by setting the appropriate values into bits 3-0 of Register 43H/63H. An offset of zero sets data transfers to the asynchronous mode of operation. The synchronous transfer period is a function of the input SYSCLK frequency and can assume 13 different periods depending on the values programmed in bits 7 - 4 of Register 43H/63H.

Differential SCSI

Six additional pins are provided with the CL-SH351 for the control of the external logic that is necessary to implement the Differential Mode of bus operation. The Differential Mode is always enabled such that the six control pins always drive the correct control and timing. If Differential Mode is designed, then the pins are connected controlling the external logic; otherwise, the outputs are left unconnected. There are no internal control bits in the CL-SH351 to differentiate between the Single-ended and the Differential Mode of operation.

4.3 Buffer Manager Interface

The third functional logic block of the CL-SH351 is the Buffer Manager interface. This block controls the flow of data between the external RAM data buffer and the CL-SH351 SCSI interface, the Sector Formatter Data path, and the microcontroller buffer memory access ports. The Buffer Manager interface provides the external RAM addressing, timing, and control signals necessary for the CL-SH351 to interface with the RAM data buffer. The Buffer Manager interface also provides an additional data bit signal called the BUFFER MEMORY DATA PARITY signal (BDP — pin 94) for odd parity generation and checking.

The Buffer Manager logic can control either a Static RAM (SRAM) buffer or Dynamic RAM (DRAM) buffer. The CL-SH351 powers up in the SRAM Mode. If DRAM operation is desired then the DRAM/SRAM* bit (Register 53H, bit 0) should be set. The topics that are common to these two modes of operation are discussed in the section *RAM Data Buffer Segmentation* and the section *RAM Data Buffer Parity.* The two modes of operation, however, are sufficiently different that most of the logic is described in two different sections depending on the configuration. For details on the SRAM buffer interface operation, refer to *SRAM Buffer Interface Operation.* For details on the DRAM buffer interface operation, refer to *SRAM Addressing Operation.*

RAM Data Buffer Segmentation

For optimum data flow control, it is often desirable to divide the buffer memory into smaller 'protected' segments. The Buffer Manager provides the option to configure the RAM data buffer into programmable data segments on segment address boundaries. The segment size is programmable in Register 56H. The data segment is designated by the upper RAM address bits.

This buffer segmentation is always enabled. In this mode, after a buffer memory transfer is completed, only the lower bits of the address pointer corresponding to segment size are incremented. Consequently, the lower address bits of the address pointer would roll over to 0, without any change to the address pointer upper bits that designate the segment.

RAM Data Buffer Parity

The CL-SH351 supports data parity on the external RAM data buffer. The Buffer Manager interface can be configured to generate the odd parity of the 8-bit data being written to the RAM buffer. This parity check bit is written along with the 8-bit data to a 9-bit wide RAM data buffer. The BUFFER MEMORY DATA PARITY signal

(pin 94) is connected to the additional RAM device(s).

If the data is sourced from the Sector Formatter Data path, then the odd parity is generated at the serializer/deserializer (SERDES) and is passed through to the BUFFER MEMORY DATA PARITY signal (pin 94). If the data is sourced from the SCSI Host interface, then the parity generation is dependent on the value of the SCSI PARITY ENABLE bit (bit 3) of the SCSI MODE CONTROL Register (44H/64H). If this bit is set, then the value of the parity received from the SCSI data bus is passed through to the BUFFER MEMORY DATA PARITY signal (pin 94). If this bit is reset, then the odd parity value of the data received from the SCSI data bus is generated inside the CL-SH351 and then is written out on the BUFFER MEMORY DATA PARITY signal (pin 94).

When data is being read from the RAM data buffer, the odd parity value can be tested or ignored. If the BUFFER MEMORY PARITY ENABLE bit (bit 3) of the BUFFER MODE CONTROL Register (53H) is set, then the bit value received from the BUFFER MEMORY DATA PARITY signal (pin 94) is tested. It is tested to see if it is the odd parity value of the eight bits on the BUFFER MEMORY DATA BUS signals (BD0-7). The data being read from the RAM data buffer is either for the SCSI Host interface or the SERDES of the Sector Formatter Data path. In both cases, there is a bit available to report a parity error, if one is detected by the CL-SH351 parity checking circuitry.

If the Sector Formatter is reading the RAM data buffer and a parity error is detected on the BUFFER MEMORY DATA PARITY signal (pin 94), then the DISK/BUFFER PARITY ERROR bit (bit 6) of the FORMAT SEQUENCER STATUS REGISTER 2 (7AH) is set. If the SCSI Host interface is reading from the RAM data buffer and a parity error is detected, then the SCSI/BUFFER PARITY ERROR DETECTED bit (bit 4) of the SCSI STATUS REGISTER 1 (46H/66H) is set. The subsequent actions are firmware dependent; this enables different responses to the RAM data buffer parity errors to be constructed in the program.

If the BUFFER MEMORY PARITY ENABLE bit (bit 3) of the BUFFER MODE CONTROL Register (53H) is reset, then the two status bits — the DISK/BUFFER PARITY ERROR bit (Register 7AH, bit 6), and the SCSI/BUFFER PARITY ERROR DETECTED bit (Register 46H/66H, bit 4) — are always reset.

SRAM Buffer Interface Operation

In order to ensure the proper operation of the Buffer Manager in SRAM Mode, the DRAM/SRAM* bit (bit 0) of the BUFFER MODE CONTROL Register (53H) must be reset.

SRAM Addressing Operation

When in the SRAM Mode of operation, the Buffer Manager interface can address up to 256 K bytes of memory. This requires 18 address lines that correspond to the Buffer Manager address signals BA0-17 (pins 95-100, 3-4, 6-14, and 5). The buffer memory address is never placed in a high-impedance state; it is always driven by one of two sources — the Disk Address Pointer (Registers 57H-59H) or the Host Address Pointer (Registers 5AH-5CH). These pointers have various initialization conditions, and their starting values can be changed via direct firmware control.

The Disk Address Pointer (Registers 57H-59H) is dedicated for disk and microcontroller transfers. The two high-order bits of the Disk Address Pointer (Registers 57H-59H) are in bits 1-0 of Register 59H. The middle-order eight bits are in Register 58H, and the low-order eight bits are in Register 57H. Any access to the RAM data buffer by the Sector Formatter selects the value in Registers 57H-59H, the Disk Address Pointer, to be driven out on the buffer memory address bus.

When the local microcontroller accesses the buffer memory, the Disk Address Pointer

(Registers 57H-59H) is also used. Consequently, in order to prepare for a local microcontroller access to the buffer memory, all disk transfers to or from the CL-SH351 must be terminated before the Disk Address Pointer (Registers 57H-59H) is loaded.

The Host Address Pointer (Registers 5AH-5CH) is reserved for transfers between the SCSI bus and the RAM data buffer. The Host Address Pointer two high-order bits are in bits 1-0 of Register 5CH. The middle-order eight bits are in Register 5BH, and the low-order eight bits are in Register 5AH. Any access to the RAM data buffer by the SCSI interface logic selects the value in Registers 5AH-5CH, the Host Address Pointer, and has the CL-SH351 drive this value onto the buffer memory address bus.

The Host Address Pointer (Registers 5AH-5CH) is compared with the Stop Address Pointer (Registers 5DH-5FH) in order to contain the data transfers to a particular block boundary value. To translate the value of the Host Address Pointer (Registers 5AH-5CH) into a repeatable block size, the BUFFER SIZE Register (56H) is used to mask the upper address bits of the Host Address Pointer (Registers 5AH-5CH) and the Stop Address Pointer (Registers 5DH-5FH). Consequently, only the lower significant bits that are modulo a block size are used for the comparison. When the comparison of the Host Address Pointer (Registers 5AH-5CH) and the Stop Address Pointer (Register 5DH-5FH), masked by the BUFFER SIZE Register (56H), is equal, then the host transfer is terminated.

Both the Disk Address Pointer (Registers 57H-59H) and the Host Address Pointer (Registers 5AH-5CH) are automatically incremented by a count of one, after the completion of each access to the RAM data buffer.

If buffer memory segment size is 256K (refer to the section *Buffer Manager Segmentation*), then all 18 buffer memory address lines (BA0-17) are subject to being incremented after each RAM data buffer access. If the system's static buffer memory is less than 256K bytes, then the hardware engineer should not use the remaining most significant buffer memory address lines as memory chip selects. This limitation is imposed because the incrementing of the high-order address lines will deselect the memory chip(s). The firmware may avoid this problem by managing the address pointers (the Disk Address Pointer (Registers 57H-59H) and the Host Address Pointer (Registers 5AH-5CH)) on the proper address block boundaries.

SRAM Read/Write Access Control

The Buffer Manager accesses the buffer memory data bus to read or to write the contents of the RAM data buffer, or to read the static state of the data bus (see the section *Microcontroller-to-Buffer Manager Interface* for more details). The direction of the access must be specified in order to generate the correct control signals. The SCSI Host, the Sector Formatter, and the local microcontroller all use unique methods to specify the direction of the access.

In the case of SCSI Host transfers, the read/write control is set by the SCSI R/W* TRANSFER DIRECTION bit (bit 3) of the BUFFER TRANSFER CONTROL Register (52H). When this bit is set, the data read from the RAM data buffer is transferred through the CL-SH351 chip to the SCSI Host interface. If this bit is reset, then the data is transferred from the SCSI Host interface through the CL-SH351 chip and written to the RAM data buffer.

In the case of Sector Formatter transfers, the transfer direction is controlled by the BUFFER/DISK R/W* TRANSFER DIRECTION bit (bit 3) of the SECTOR FORMATTER OPERATION CONTROL Register (77H). When this bit is set, the data read from the RAM data buffer is transferred to the Sector Formatter. In order to write to the RAM data buffer from the Sector Formatter, this bit must be reset.

In the case of microcontroller transfers, the microcontroller control strobe is used in order to determine the transfer direction. A read of the CL-SH351 Port 50H (the SCHEDULED BUFFER DATA Register) results in a read of the RAM data buffer. A write to Port 50H (the SCHEDULED BUFFER DATA Register) causes a write to the RAM data buffer.

Given the direction of data transfer from the above controls, all read operations are the same, regardless of the requesting source; similarly, all write operations are the same. Both the read and write operation commence when the correct address pointer (the Disk Address Pointer (Registers 57H-59H), or the Host Address Pointer (Registers 5AH-5CH)) is driven onto the buffer memory address bus.

In the case of a read to the RAM data buffer, MEMORY CHIP ENABLE (MCE* — pin 29), and the MEMORY OUPUT ENABLE signal (MOE* — pin 15) are asserted low after the address is driven onto the address bus. The MEMORY OUTPUT ENABLE signal should be connected to the SRAM output enable(s) to ensure the highest throughput. Data must be provided from the SRAM shortly before the rising (trailing) edge of the MEMORY OUTPUT ENABLE signal (MOE* — pin 15). The duration of the MEMORY OUTPUT ENABLE signal (MOE* — pin 15) is a programmable parameter (refer to the section *SRAM Signal Timing*). The WRITE ENABLE signal (WE* — pin 16) remains deasserted high throughout the entire SRAM access.

In the case of a write to the RAM data buffer, the MEMORY CHIP ENABLE signal (MCE* — pin 29) and the WRITE ENABLE signal (WE* — pin 16) are concurrently asserted low after the address is driven onto the address bus. Data is driven from the CL-SH351 to the RAM data buffer shortly after the address is driven. The MEMORY CHIP ENABLE signal (MCE* — pin 29) and the WRITE ENABLE signal (WE* — pin 16) are deasserted high at the same time near the end of the cycle. The duration of the MEMORY CHIP ENABLE signal (MCE* — pin 29) and the WRITE ENABLE signal (WE* — pin 16) are a programmable parameter (refer to the following section *SRAM Signal Timing*).

SRAM Signal Timing

For both a read and a write access to the RAM data buffer, the correct address pointer (the Disk Address Pointer (Registers 57H-59H) and the Host Address Pointer (Registers 5AH-5CH)) is driven with respect to the rising edge of the SYSCLK signal input (pin 41). For both read and write access the MEMORY CHIP ENABLE signal (MCE* — pin 29) is driven with respect to the rising edge of SYSCLK signal input (pin 41) along with the address lines. The MEMORY CHIP ENABLE (MCE* — pin 29) is deasserted at the end of access, if there is no further memory access pending. For consecutive accesses, the signal will remain low.

In the case of a read access, the MEMORY OUTPUT ENABLE (MOE* — pin 15) is asserted low along with the address. If the next access is not a read access, it is deasserted at the end of an access. For consecutive read accesses, the signal will remain low.

In the case of a write access, the WRITE ENABLE signal (WE* — pin 16) is driven off the falling edge of SYSCLK signal (pin 41) one-half clock after the address is driven, and deasserted high one-half SYSCLK before the end of the SRAM address. This implies that the total SRAM access time controls the pulse width of these signals. The complete SRAM access time is programmed in terms of SYSCLK input signal (pin 41) periods. By programming a value into bits 1-0, RAS* LOW TIME/SRAM CYCLE TIME, of the BUFFER MANAGER TIMING CONTROL Register (54H) an access time of 2T to 5T (where T is the SYSCLK signal (pin 41) period) can be obtained.

In the case of a read access to the RAM data buffer, data is clocked into the CL-SH351 on the same edge of SYSCLK that causes the release

of the MEMORY OUTPUT ENABLE signal (MOE* — pin 15). In the case of a write, data is held by the CL-SH351 until the same rising edge of SYSCLK which removes the address. The WRITE ENABLE signal (WE* — pin 16) is released one-half clock earlier to write the data to the RAM data buffer.

The BUFFER MEMORY DATA PARITY signal (pin 94) has the same timing output and input requirements as all of the BUFFER MEMORY DATA BUS signals (BD0-7).

In SRAM Mode, the theoretical maximum Buffer Manager throughput is 15 Mbytes/second. The actual throughput is a function of the NRZ clock frequency from the disk drive, the SRAM speed used or required, the desired host throughput, and the input SYSCLK signal (pin 41) frequency. In general, the actual SRAM throughput available can be derived from the SRAM access time programmed in bits 1-0 of Register 54H. The total Buffer Manager throughput that is available can be obtained by multiplying the SYSCLK period times the number of cycles programmed; the throughput is the inverse of this value.

DRAM Buffer Interface Operation

When the CL-SH351 is operating in DRAM Mode, the Buffer Manager interface can address up to 1 Mbyte of memory. Before programming the CL-SH351 for DRAM operation, the refresh period, the DRAM device organization, and the DRAM timing parameters must be programmed. The CL-SH351 is configured for DRAM operation by setting the DRAM/SRAM* bit (bit 0) of the BUFFER MODE CONTROL Register (53H).

DRAM Parameter Programming

The refresh period is programmed in the DRAM REFRESH PERIOD Register (55H). This is an eight-bit value that is appended to a ninth (least significant value) bit which is always preset to one. This refresh period multiplied by the SYSCLK input period sets the time interval between automatic Refresh operations.

The CL-SH351 supports a Read Address Strobe (RAS) — only refresh scheme. This scheme is supported with an on-board, nine-bit refresh counter. This counter is referred to as the Refresh Address Counter and holds the buffer memory row address that is to be refreshed. It is incremented after a memory refresh cycle. This counter is initialized to zero when the RST* signal (pin 40) is asserted low.

The BUFFER MANAGER TIMING CONTROL Register (54H) contains the following four fields — CAS* HIGH TIME (bits 7-6), CAS* LOW TIME (bits 5-4), RAS* HIGH TIME (bits 3-2), and RAS* LOW TIME (bits 1-0). These four fields must be programmed with the specific timing characteristics of the DRAM devices used. Each of these four fields is allocated two bits. This enables each of the four DRAM timing characteristics to be programmed with one of four values. The values are integral multiples of the SYSCLK input signal (pin 41) period.

The parameters that need to be programmed into these four fields are as follows: (1) the BA17/CAS* signal (pin 5) high time for a DRAM Page Mode access, (2) the BA17/CAS* signal (pin 5) low time for a Page Mode DRAM access, (3) the BA16/RAS* signal (pin 14) high or precharge time, and (4) the BA16/RAS* signal (pin 14) low time during a normal DRAM access. Refer to the section *BA16/RAS* and BA17/CAS* Signal Timing* for more details on these parameters.

To ensure that the Buffer Manager drives the row and column address bits on the correct signal lines without any multiplexing or other external logic being required, the device organization should be programmed into the DRAM TYPE field (Register 53H, bits 2-1). The following three DRAM types are supported: 64K bits, 256K bits by 1 bit or 4 bits, and 1 Mbit devices.

DRAM Addressing Operation

The CL-SH351 supports 64K, 256K and 1M DRAMs, and provides up to 1 Mbytes of address space. The following table shows how the bits from the address pointer (either the Disk Address Pointer — Registers 57H-59H, or the Host Address Pointer — Registers 5AH-5CH) map into the buffer memory address lines BA0-11 (pins 95-100, 3-4, 6-9) for each DRAM size during row and column address time:

DRAM SIZE		BUFFER ADDRESS LINES											
		11	10	9	8	7	6	5	4	3	2	1	0
64K	Row Addr	19	18	17	16	15	14	13	12	11	10	9	8
	Col Addr	19	18	17	16	7	6	5	4	3	2	1	0
256K	Row Addr	--	19	18	17	16	15	14	13	12	11	10	9
	Col Addr	--	19	18	8	7	6	5	4	3	2	1	0
1M	Row Addr	--	--	19	18	17	16	15	14	13	12	11	10
	Col Addr	--	--	9	8	7	6	5	4	3	2	1	0

During a Refresh operation, the 10-bit Refresh Address Counter is driven on the buffer memory address lines BA0-9 (pins 95-100, 3-4, 6-7). Unlike SRAM Mode, for DRAM operation, the most significant bits of the buffer memory address are constant for 64 Kbit and 256 Kbit devices. These upper bits are managed by the firmware and force an inherent buffer segmentation equal to the RAM device size. In the case of a 1 Mbit device, all of the buffer memory address bits (bits 19-0) can be incremented.

The concept of the BUFFER SIZE Register (56H) masking the comparison of the high-order bits between the Host Address Pointer (Registers 5AH-5CH) and the Stop Address Pointer (Registers 5DH-5FH) is the same as described for the SRAM Mode of operation (refer to the section *SRAM Addressing Operation*). The value in the BUFFER SIZE Register (56H) determines the number of high-order address bits to mask in the comparison between the Host Address Pointer (Registers 5AH-5CH) and the Stop Address Pointer (Registers 5DH-5FH). The result of this comparison is used by the Buffer Manager to decide when to terminate the current buffer memory transfer. Bits are masked, starting from the most significant row address bits, until the request segment size is reached.

DRAM Page And Burst Mode Operation

The Buffer Manager always accesses the DRAM in Page Mode. This mode allows multiple byte accesses for each assertion of the BA16/RAS* signal (pin 14). To operate DRAMs in Page Mode, the Buffer Manager first asserts the BA16/RAS* signal (pin 14), followed by multiple CAS* cycles to strobe each new byte. This is the reason the CAS* timing programmed into Register 54H is the Page Mode CAS* timing, rather than the single-access timing. As mentioned previously, Refresh operations are Read Address Strobe (RAS), only, and are not considered Page Mode accesses.

When in DRAM Mode, the SCSI Host requests and the Sector Formatter requests for a buffer memory access are all Page Mode accesses. This mode of operation assures the most efficient use of the DRAM devices because it uses them in their fastest access mode.

If the host interface has a byte ready for transfer to the RAM data buffer, the Buffer Manager will not grant memory access cycles for the data in the host FIFO until there are at least four bytes ready for transfer. The same applies to the Sector Formatter interface to the Buffer Manager. The Sector Formatter has an internal FIFO used

to stack data that is to be read from, or written to, the RAM data buffer. The length of the data burst may be less than four bytes when the Buffer Manager is transferring the last or remaining data bytes of the requested transfer. Because DRAMs require a new RAS* cycle at each page break of the column address, the Buffer Manager must stop a burst transfer on a page boundary; this could also result in a data burst of less than four bytes.

The microcontroller interface into the RAM data buffer has no FIFO available; consequently, only single-byte requests can be transferred.

BA16/RAS* and BA17/CAS* Signal Timing

The Buffer Manager DRAM controller timing is specified in the BUFFER MANAGER TIMING CONTROL Register (54H), as discussed in the section *DRAM Parameter Programming.* Register 54H four timing parameters yield the following BA16/RAS* signal (pin 14) and BA17/CAS* signal (pin 5) timing:

CAS HIGH TIME* — (Register 54H, bits 7-6). This field specifies the CAS* precharge time in DRAM Page Mode access.

CAS LOW TIME* — (Register 54H, bits 5-4). This field specifies the BA17/CAS* signal (pin 5) low time in a Page Mode access. In a DRAM Page Mode access, the BA17/CAS* signal (pin 5) low time for the very first access of the burst access is the BA16/RAS* signal (pin 14) low time minus one SYSCLK cycle, as in the normal access. For the subsequent accesses, however, it is specified by the BA17/CAS* signal (pin 5) low time — bits 5-4 of Register 54H.

RAS HIGH TIME* — (Register 54H, bits 3-2). This field specifies the minimum number of SYSCLK cycles that the BA16/RAS* signal (pin 14) is deasserted for RAS precharge.

RAS LOW TIME* — (Register 54H, bits 1-0). This field specifies the number of SYSCLK cycles that the BA16/RAS* signal (pin 14) is asserted in a normal DRAM access cycle. The BA16/RAS* signal (pin 14) is asserted in phase 2 (the second half) of the first SYSCLK cycle starting the access; the BA17/CAS* signal (pin 5) is asserted one SYSCLK cycle later. The BA16/RAS* signal (pin 14) and the BA17/CAS* signal (pin 5) are deasserted simultaneously in a normal cycle.

For read accesses of the DRAM data buffer, the MEMORY OUTPUT ENABLE signal (MOE* — pin 15) is asserted low with the first assertion of the BA17/CAS* signal (pin 5), regardless of whether it is a single or multiple byte access. The MEMORY OUTPUT ENABLE signal (MOE* — pin 15) is deasserted high, along with the last BA17/CAS* signal (pin 5). For DRAM write accesses to the RAM data buffer, the WRITE ENABLE signal (WE* — pin 16) is asserted low with the assertion of the BA16/RAS* signal (pin 14), and is deasserted high with the deassertion of the BA16/RAS* signal (pin 14). During a Refresh operation, neither the MEMORY OUTPUT ENABLE signal (MOE* — pin 15) nor the WRITE ENABLE signal (WE* — pin 16) is asserted low.

4.4 Sector Formatter and Format Sequencer Operation

The fourth functional logic block of the CL-SH351 is the Sector Formatter. The Sector Formatter provides the disk data and control functions. As the block diagram on the cover page indicates, the Sector Formatter is subdivided into the Format Sequencer and the Sector Formatter Data path. The Sector Formatter operation is managed by the Format Sequencer, which in turn is controlled by a user-written program. This user-written program is referred to as the Format Sequencer program and contains the control information for the disk track and sector format. This program must be loaded into the Writable Control Store (WCS) before the Format Sequencer can function properly. The Writable

Control Store (WCS) consists of 124 bytes that are organized as 31 words, each four-bytes wide. The Format Sequencer program is then executed from the CL-SH351 Current Sequencer Word Register. Consequently, the Sector Formatter Current Sequencer Word Register actually controls the current disk operation and the disk interface output signals. Refer to *The Format Sequencer Operation* section for details on the operation of the Format Sequencer.

The other main component of the Sector Formatter is the Sector Formatter Data path. The Sector Formatter Data path consists of the NRZ data handling circuitry that includes the serializer/deserializer (SERDES), the ECC and CRC error control logic, the SERDES parity logic, and the data signals to the Buffer Manager interface. Refer to the section *Components of the Sector Formatter Data Path* for details on the operation.

The Sector Formatter is capable of handling NRZ data rates up to 32 Mbits/second. All disk data operations such as format, sector reads and writes, sector verifies and read ID fields are executed by one or more of these elements of the Sector Formatter.

Components of the Sector Formatter Data Path

The Sector Formatter Data path consists of the following seven components:

- **A serializer/deserializer (SERDES)**
- **Two eight-bit comparators**
- **A serial synchronization detector**
- **Primary and secondary comparison circuitry**
- **Error Detection and Correction (EDAC) Logic**
- **A ten-byte stack *and***
- **Buffer memory parity logic**

Serializer/Deserializer

Disk data is read or written from the CL-SH351 chip in a serial format. The NRZ signal (pin 46) provides the serial interface between the Sector Formatter Data path and the disk drive. This signal enables the CL-SH351 chip to read and write NRZ data to and from the disk drive. The NRZ signal (pin 46) is the Read Data input signal from the disk drive when the Format Sequencer READ GATE signal (pin 43) is asserted; it is the Write Data output signal when the Format Sequencer WRITE GATE signal (pin 44) is asserted.

After the serial data enters the CL-SH351, it is processed through the Sector Formatter Data path Error Detection and Correction (EDAC) logic and is deserialized simultaneously by the serializer/deserializer (SERDES). The SERDES appends a parity bit to each deserialized byte as it passes the byte on to the Buffer Manager.

Data to be written out to the disk drive is either generated by the Format Sequencer (e.g., sync bytes, ID field bytes), or it is received from the Buffer Manager interface in a byte-wide format with optional odd parity. The SERDES checks the parity of the deserialized byte (if parity has been enabled) and then serializes the data. Next the serialized data is simultaneously passed through to the CL-SH351 EDAC logic and the NRZ signal (pin 46).

Eight-Bit Comparators

The Sector Formatter Data path has two eight-bit comparators that are used by the serial synchronization detector circuit, and the primary and secondary compare circuits. The primary and secondary compare circuits share the same eight-bit comparator; however, it is not the same comparator that is used by the serial synchronization detector circuit.

The serial synchronization detector circuit uses one of the Sector Formatter comparators to

search for a match between the incoming NRZ data and the preprogrammed synchronization character. This circuit compares each deserialized byte received with the SYNCHRONIZATION BYTE PATTERN Register (7CH) that contains the synchronization character. For more details on this topic, refer to the section *Serial Synchronization Detector.*

The primary and secondary compare circuits can use the second comparator to compare each deserialized byte received with one of the following: (1) the DATA/BRANCH FIELD of the Current Sequencer Word Register, or (2) the byte received from the buffer memory. For more details on the primary and secondary comparisons, refer to the *Primary and Secondary Compare Circuits* section.

Both of these Sector Formatter comparators work in parallel with the Sector Formatter Data path handling of NRZ data. Based on the results from these two eight-bit comparators, the CL-SH351 makes real-time decisions.

Serial Synchronization Detector

One of the components of the Sector Formatter Data path is the serial synchronization detector circuit. The serial synchronization detector is used to synchronize the Sector Formatter with the incoming NRZ data stream. This circuit searches for a match between the preprogrammed, eight-bit synchronization character (defined in Register 7CH) and the incoming NRZ data stream. Any bit or combination of bits in this eight-bit pattern can be masked by setting the corresponding bits in the SYNCHRONIZATION COMPARE MASK Register (7FH).

When a match is detected, then the Format Sequencer logic is issued a synchronization signal. This synchronization signal enables the Format Sequencer to align itself with the incoming NRZ data. This synchronization signal is critical because the Format Sequencer operation is suspended until the synchronization character is found in the incoming NRZ data stream. This synchronization signal also supplies the SERDES with the timing information that it needs to convert the incoming serial data stream to bytes. The firmware can abort the search for the synchronization character by writing a 1FH to the FORMAT SEQUENCER START ADDRESS Register (79H). (Refer to the section *Format Sequencer Address Flow* for more details.)

The serial synchronization detector circuit is automatically engaged when the Format Sequencer READ GATE signal (pin 43) is first asserted.

Primary and Secondary Compare Circuits

Two additional components of the Sector Formatter Data path are the primary and secondary compare circuits. The primary compare circuit is typically used for the Format Sequencer branch commands, and for verification of the Sector ID field and the Sector Data field. The secondary compare circuit can be used as a means of implementing higher-level functions not within the scope of normal Sector ID field verification. For example, the secondary compare circuit is typically used for detecting bad block flags or the end of track marks. This ability to flag specific sector or track fields for the microcontroller and then pass this information, either directly or indirectly to the Format Sequencer, supports special data handling and automated retry mechanisms.

The primary and secondary compare circuits share the same eight-bit comparator. This comparator is not the same comparator used by the serial synchronization detector circuit. (Both comparators, however, do work in parallel with the Sector Formatter Data path handling of NRZ data.)

At the beginning of a disk read or write operation, the status bit for each of these compare circuits is set to the equal state. When a compare operation is performed, the status bit is updated

to indicate an equal or not equal state. If the compare circuit is not used by the Format Sequencer program, then the compare circuit will remain in the equal state.

In the case of a primary compare operation, the NRZ read Data is compared with one of the following: (1) the buffer memory data if a Sector Data Field Verify operation has been programmed, or (2) the Current Sequencer Word Register DATA/BRANCH FIELD on all bytes where the comparison was enabled, by setting the COMPARE ENABLE bit (Writable Control Store (WCS) CONTROL FIELD, bit 1). The status of the primary compare operation is available by testing the PRIMARY COMPARE NOT EQUAL bit (Register 7AH, bit 0) which is set when the result of the primary compare operation is not equal. The not equal status is cleared by toggling the INITIALIZE ECC bit (Register 71H, bit 3).

In the case of a secondary compare operation, the NRZ read Data is compared with the Current Sequencer Word Register DATA/BRANCH FIELD on all bytes where the comparison was enabled (by setting the SECONDARY COMPARE ENABLE bit (Writable Control Store (WCS) COUNT FIELD, bit 5) and the COMPARE ENABLE bit (Writable Control Store (WCS) CONTROL FIELD, bit 1)). The status of the secondary compare operation is available by testing the SECONDARY COMPARE NOT EQUAL bit (Register 7AH, bit 1) which is set when the result of the secondary compare operation is not equal. The not equal status is cleared by toggling the INITIALIZE ECC bit (Register 71H, bit 3). The status of the secondary compare circuit can generate a local microcontroller interrupt, as well as alter or stop the Format Sequencer program flow.

Error Detection and Correction Logic

As part of the Sector Formatter Data path Error Detection and Correction (EDAC) Logic, it provides three fixed polynomials. The three fixed polynomials are a 16-bit CRC, a 32-bit ECC, and a 56-bit ECC. The 16-bit CRC can only be used for error detection; however, the 32-bit and 56-bit ECC codes can be used for error detection, as well as error correction. All three polynomials have synchronization framing error protection.

The microcontroller must select which ECC polynomial is to be used. The Format Sequencer can select between the 16-bit CRC or the microcontroller-selected ECC polynomial, while it is executing the Format Sequencer program from the Writable Control Store (WCS).

If an ECC error is detected after a read Data operation, the syndrome is saved in the CL-SH351 ECC status registers (Registers 73H-76H). The syndrome is retained in these registers until a new disk operation is started. If an ECC error is detected, then the ECC ERROR bit (Register 7AH, bit 2) will be set. This bit is set if there is an error from the EDAC logic after reading either the Sector ID field or the Sector Data field. In order to simplify the processing of data errors, the DATA FIELD ECC ERROR bit (Register 7AH, bit 3) is set if the Data Field is read, and an error is detected.

The CL-SH351 has advanced correction logic (Registers 71H-76H) that the microcontroller can use to determine if the ECC error is correctable and to calculate the error pattern and its displacement from the beginning of the Data Field. After the microcontroller completes this process, it can correct the identified error in the RAM data buffer.

The following is the 16-bit CRC polynomial:

$(x^{16} + x^{12} + x^5 + 1)$.

The following is the 32-bit ECC polynomial:

$(x^{32} + x^{28} + x^{26} + x^{19} + x^{17} + x^{10} + x^6 + x^2 + 1)$.

The 32-bit ECC polynomial is a computer-generated code capable of correcting up to an 11-bit single burst error. When this code is used

strictly for error detection, then it will detect any 32-bit single error burst. This 32-bit ECC code does not, however, have any reasonable double burst error detection capability.

The following is the 56-bit ECC polynomial:

$(x^{56} + x^{52} + x^{50} + x^{43} + x^{41} + x^{34} + x^{30} + x^{26} + x^{24} + x^{8} + 1)$.

The 56-bit ECC polynomial is a computer-generated code that can detect up to 56-bit single burst errors. For a 1041-byte field, it can detect 41-bit double burst errors in which the sum of two bursts is less than 41 bits. This polynomial can correct up to 22-bit burst errors.

Ten-Byte Stack

Another component of the Sector Formatter Data path is its ten-byte, recirculating stack. If this stack is enabled during a read operation, then deserialized bytes from any desired sector field can be pushed onto this stack. This storing of information enables the local microcontroller to read the information in a non-real time manner. This capability can be used for defect management or to pass the Sector Identification field to the microcontroller.

Because it is a ten-byte stack, if more than ten bytes are written to the stack, only the last ten bytes are saved. The microcontroller reads this stack by reading the CL-SH351 SECTOR FORMATTER STACK Register (7FH). The microcontroller reads the data from the stack in LIFO (Last In, First Out) order. Consequently, the first microcontroller read of the SECTOR FORMATTER STACK Register (7FH) would entail the microcontroller reading the last byte that was written onto the stack. Each read of this register rotates the data in a ring fashion in the stack so that the entire stack can be read. If more than ten bytes are read from the stack, then the ten bytes of data are read continuously in a circular manner. For example, if the stack is read 11 times, then the stack pointer will have wrapped around to the top of the stack.

Buffer Memory Parity Logic

Buffer memory parity is an optional error detection feature supported by the Sector Formatter Data path. This buffer memory parity function is enabled by setting the BUFFER MEMORY PARITY ENABLE bit (Register 53H, bit 3). For more details, refer to RAM Data Buffer Parity.

The Format Sequencer Operation

The second major component of the Sector Formatter is the Format Sequencer. The Format Sequencer controls the processing of serial data across the disk interface. The Format Sequencer operation is controlled by a user-written program called the Format Sequencer program. This program controls the timing relationships between the disk interface output signals. It also monitors the disk interface input lines, and based on their value, it makes decisions to branch to different locations within the Format Sequencer program. The Format Sequencer program can be programmed to sequence through such types of operations as sector read, sector write, and sector verify. The Format Sequencer can also be programmed for various types of automatic retry algorithms and defect management schemes.

As the block diagram on the cover page indicates, one of the main components of the Format Sequencer is the Writable Control Store (WCS). The Writable Control Store (WCS), used to hold this Format Sequencer program, consists of 124 bytes that are organized as 31 words, each four bytes wide. Each Writable Control Store (WCS) word can be broken down into the following four eight-bit fields: (1) the NEXT ADDRESS FIELD, (2) the CONTROL FIELD, (3) the COUNT FIELD, and (4) the DATA/BRANCH FIELD. Refer to the description of the Writable Control Store (WCS) fields in Section 9 for details on each of these four fields. For details on the other major

components of the Format Sequencer, refer to the section *Format Sequencer Components*.

The track layout such as gap lengths, sector size, and sector data fill character can be flexibly defined in the Format Sequencer Writable Control Store (WCS). The Format Sequencer also offers other registers that can be used to control the definition of the track format. For example, the user can load the CL-SH351 SYNCHRONIZATION BYTE PATTERN Register (7CH) to define the synchronization character.

The Format Sequencer is started by writing a starting address (where the Format Sequencer should start executing at) to the FORMAT SEQUENCER START ADDRESS Register (79H). The user can stop the Format Sequencer by writing the address 1FH to Register 79H. Refer to the section *Format Sequencer Address Flow* for more details.

Format Sequencer Address Flow

The starting address (where the Format Sequencer is to begin execution) must be loaded into the FORMAT SEQUENCER START ADDRESS Register (79H). A write to Register 79H causes the four bytes at that Writable Control Store (WCS) word to be fetched from the WCS and then written into the Format Sequencer Current Sequencer Word Register. The Current Sequencer Word Register is a 32-bit register that consists of the following four eight-bit fields — the NEXT ADDRESS FIELD (9FH), the CONTROL FIELD (BFH), the COUNT FIELD (DFH), and the DATA/BRANCH FIELD (FFH). After the Writable Control Store (WCS) word is loaded into the Current Sequencer Word Register, it is executed. Consequently, this 32-bit Current Sequencer Word Register controls the current disk operation and the disk interface output signals.

Each time the Sector Formatter Data path reads or writes an eight-bit byte, the count in the Current Sequencer Word Register COUNT FIELD is decremented by one. When this COUNT FIELD decrements past zero (to minus one or underflows), another instruction word is fetched from the Writable Control Store (WCS) and then loaded into the Current Sequencer Word Register.

After the current instruction is executed, the source of the next address to be executed is dependent on the programmed branch command. The branch command is programmed in the NEXT ADDRESS FIELD (bits 7-5) of the Writable Control Store (WCS), and the ALTERNATE BRANCH COMMAND SELECT bit (bit 7 of the Writable Control Store (WCS) CONTROL FIELD).

The next address that the Format Sequencer should go to can be obtained from any one of the following sources: (1) the NEXT ADDRESS FIELD, or (2) the DATA/BRANCH FIELD, or (3) the BRANCH ADDRESS Register (78H), or (4) an implied address of 1FH. Any fetch of the Writable Control Store (WCS) address 1FH stops the Format Sequencer. Therefore, the user can stop the Format Sequencer by writing the address 1FH to the FORMAT SEQUENCER START ADDRESS Register (79H).

Variable Sector Data Field Size

The CL-SH351 supports variable Sector Data field sizes. The CL-SH351 uses an eight-bit Sector Data field length counter to support this feature. When the DATA TRANSFER bit (bit 0 of the CONTROL FIELD of the Writable Control Store (WCS)) is set, the COUNT FIELD of the Current Sequencer Word Register is an eight-bit programmable counter. By setting the COUNT FIELD to any value from 00H to FFH, a sector length of up to 256 bytes can be transferred (read from or written to the disk drive). The value of this counter should be programmed to be one less than the required sector length.

For sector sizes greater than 256 bytes, there are several different methods that can be used to define the Sector Data field size. The most direct approach is to use additional Writable Control

Store (WCS) words with each word processing up to 256 bytes of the Data Field.

Another approach uses the INHIBIT DATA FIELD CARRY bit (bit 4) in the SECTOR FORMATTER OPERATION CONTROL Register (77H) and the Sector Size Counter (initialized by the value in the SECTOR SIZE Register (4EH)). In this approach, the INHIBIT DATA FIELD CARRY bit (Register 77H, bit 4) is set before the count of the Sequencer instruction word (that has the DATA TRANSFER bit (CONTROL FIELD, bit 0) set) has expired. The Format Sequencer is inhibited from going on to the next Sequencer word, even though the Sector Size Counter has decremented to the last byte or has generated an underflow. Consequently, another 256 bytes of data are transferred. The initial value of the Sector Size Counter should be one less than the actual number of COUNT FIELD underflows that are to be suppressed. Each inhibited COUNT FIELD underflow decrements the Sector Size Counter. The INHIBIT DATA FIELD CARRY bit (Register 77H, bit 4) is automatically reset when the Sector Size Counter underflows.

The Sector Size Counter is automatically initialized to the sector size value programmed in Register 4EH before any Sector Data field is processed. Therefore, the sector size needs to be written only once in an initialization routine and only the INHIBIT DATA FIELD CARRY bit (Register 77H, bit 4) must be set for each Sector Data field transfer.

Split Data Field Processing

The CL-SH351 Format Sequencer also supports the processing of multiple Data Fields for a given Sector ID field. This function supports the synchronization of ECC computation or generation across non-contiguous Data Fields.

To implement this Split Data Field Processing function, the SPLIT FIELD MODE DISABLE bit (bit 7) of the SECTOR FORMATTER MODE CONTROL Register (4FH) should be reset. When this bit is reset, bit 3 of the CONTROL FIELD functions as the PROCESS SPLIT control bit. This enables the PROCESS SPLIT control bit to start and to stop the ECC calculation for Split Data Field Processing.

The setting of this control bit is either a soft stop operation or a soft start operation. The read or write operation is programmed to start in the usual manner without using the PROCESS SPLIT control bit (bit 3 of the CONTROL FIELD of the Writable Control Store (WCS)). A soft stop is invoked when the first 'split' Data Field ends. The PROCESS SPLIT control bit (Bit 3 of the CONTROL FIELD of the Writable Control Store (WCS)) should be set in the last Writable Control Store (WCS) word that has the DATA TRANSFER bit (bit 0 of the CONTROL FIELD of the Writable Control Store (WCS)) set. Then as many Writable Control Store (WCS) words as required can be used to skip fields or to assert the READ GATE signal (pin 43) or the WRITE GATE signal (pin 44) for the next Phase Locked Oscillator (PLO) synchronization field. Next, a soft start is required for the second Data Field of the sector. The PROCESS SPLIT control bit (bit 3 of the CONTROL FIELD of the Writable Control Store (WCS)) is set twice for the soft start. It should be set in the Writable Control Store (WCS) word that asserts the READ GATE signal (pin 43) or the WRITE GATE signal (pin 44); it needs to be set in the Writable Control Store (WCS) word, preceding the word with the DATA TRANSFER bit (bit 0 of the CONTROL FIELD of the Writable Control Store (WCS)) set for the second Data Field transfer. The PROCESS ECC bit (bit 6 of the CONTROL FIELD of the Writable Control Store (WCS)) should not be set when implementing a soft stop operation. The termination of the last Data Field is programmed as usual with the PROCESS ECC bit (bit 6 of the CONTROL FIELD of the Writable Control Store (WCS)) set.

By programming the sequence in the Writable Control Store (WCS) with the proper combination of soft start and soft stop operations, sector formats with servo bursts embedded in the Data Field can be handled easily while maximizing data capacity. Embedded servo and zoned techniques are easily employed as any

track or band of tracks can optimize the track format with varying Data Field sizes within the band. A constant number of sectors-per-track can be maintained, as bit densities are kept constant and the Data Field sizes are increased or decreased.

Format Sequencer Components

The following are the main components of the Format Sequencer:

- **The Writable Control Store (WCS)**
- **The Current Sequencer Word Register**
- **A Synchronization Timer**
- **A Two Index Counter *and***
- **A Disk/Buffer Parity Circuit**

For more information on the Writable Control Store (WCS) and the Current Sequencer Register, refer to *The Format Sequencer Operation* section.

Synchronization Timer

The Synchronization Timer is a circuit used to set a limit on the amount of time that the Format Sequencer is allowed to synchronize itself (find and match the synchronization byte pattern defined in Register 7CH) with the incoming NRZ data stream. This limit is programmed in the CL-SH351 SYNCHRONIZATION BYTE-COUNT LIMIT Register (70H). The limit is specified in terms of a byte-count limit that can be from 0 to 255. Only one value can be programmed into Register 70H. When the Synchronization Timer is activated by the Format Sequencer program, the value in Register 70H is decremented for each byte time that passes. If the value within Register 70H reaches zero a time-out occurs. When a time-out error occurs, the Synchronization Timer stops the Format Sequencer and sets the SYNCHRONIZATION TIME-OUT ERROR bit (Register 7AH, bit 4).

The Format Sequencer program can activate the Synchronization Timer by setting the COUNT/START SYNCHRONIZATION TIMER/SECONDARY COMPARE ENABLE/TWO INDEX TIMER bit (bit 5 of the Writable Control Store (WCS) COUNT FIELD). The Synchronization Timer is reset under the following conditions: (1) when the Format Sequencer is reset, or (2) when the serial synchronization detector finds the synchronization character (as defined in Register 7CH) in the incoming NRZ data stream.

This feature would typically be used to limit the amount of time that the Format Sequencer is allowed to search for the Sector Data field, after it successfully completes a Sector ID field comparison. The Synchronization Timer can also be used to limit the amount of time that the Format Sequencer searches for a Sector ID field, after a sector mark is detected in a hard-sectored disk drive.

Two Index Counter

Another component of the Format Sequencer is the Two Index Counter (TIC). This circuit is used to limit the execution of a Format Sequencer program to one complete revolution of the disk drive. This feature would typically be used to limit the number of times that the Format Sequencer would attempt to search for the Sector ID field of a target sector

The Two Index Counter (TIC) is activated by a Format Sequencer program if the TWO INDEX DETECT MODE ENABLE bit (Register 77H, bit 6) is set. A Format Sequencer program can turn on the Two Index Timer (TIC) by setting the COUNT/START SYNCHRONIZATION TIMER/SECONDARY COMPARE ENABLE/TWO INDEX TIMER bit (bit 5 of the Count Field of the Writable

Control Store (WCS)). Once the circuitry is armed, it will disarm upon one of the following three events:

1. Two Index Detect Mode Enable is reset;
2. Two index pulses are detected;
3. Disk data transfer between the Formatter and the buffer memory.

When the circuitry is rearmed, and two index edges are detected, the Two Index Detected (Register 7AH, bit 5) status bit is set. The status bit remains set until the circuitry is rearmed, or the Two Index Detection Mode enable is reset.

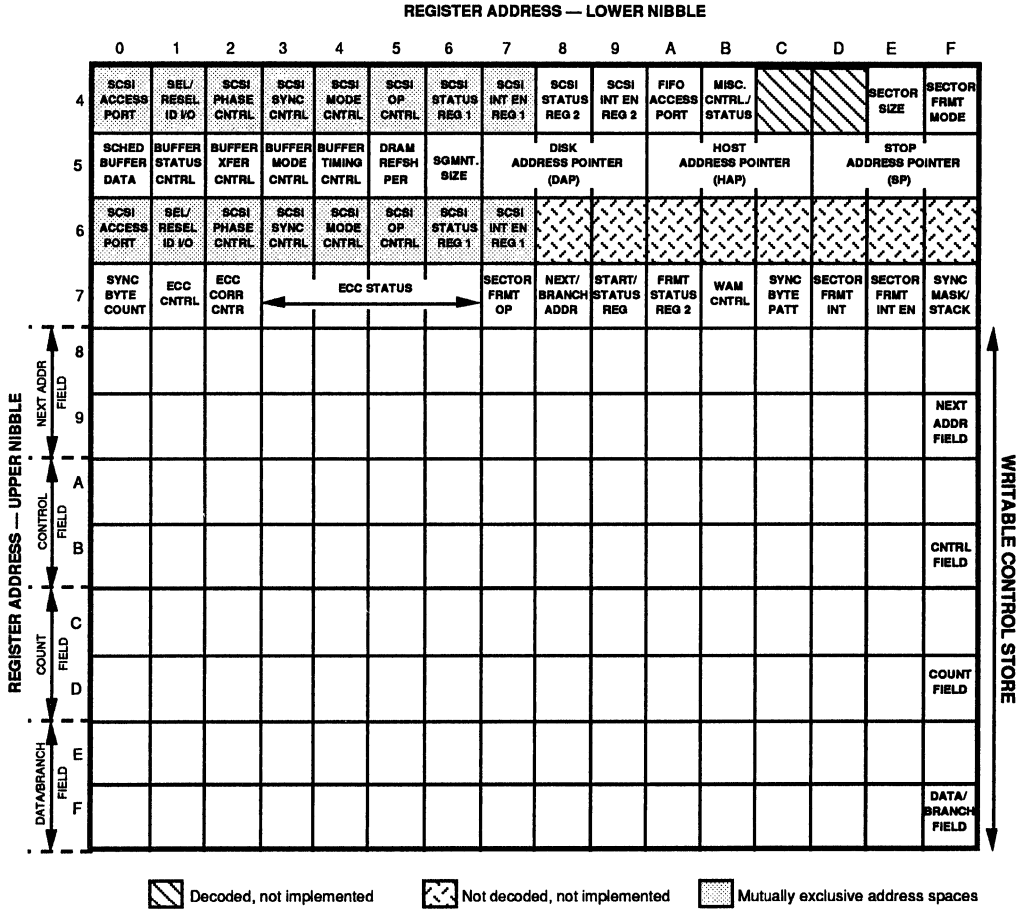
Disk/Buffer Parity Circuit

The disk/buffer parity circuit is another component of the Format Sequencer. This circuit enables the CL-SH351 to support data parity on the external RAM data buffer. This circuit can detect a parity error at the Sector Formatter Data path serializer/deserializer (SERDES) during either of the following operations: (1) an NRZ write operation, or (2) a Sector Data Verify operation (a read of the RAM data buffer).

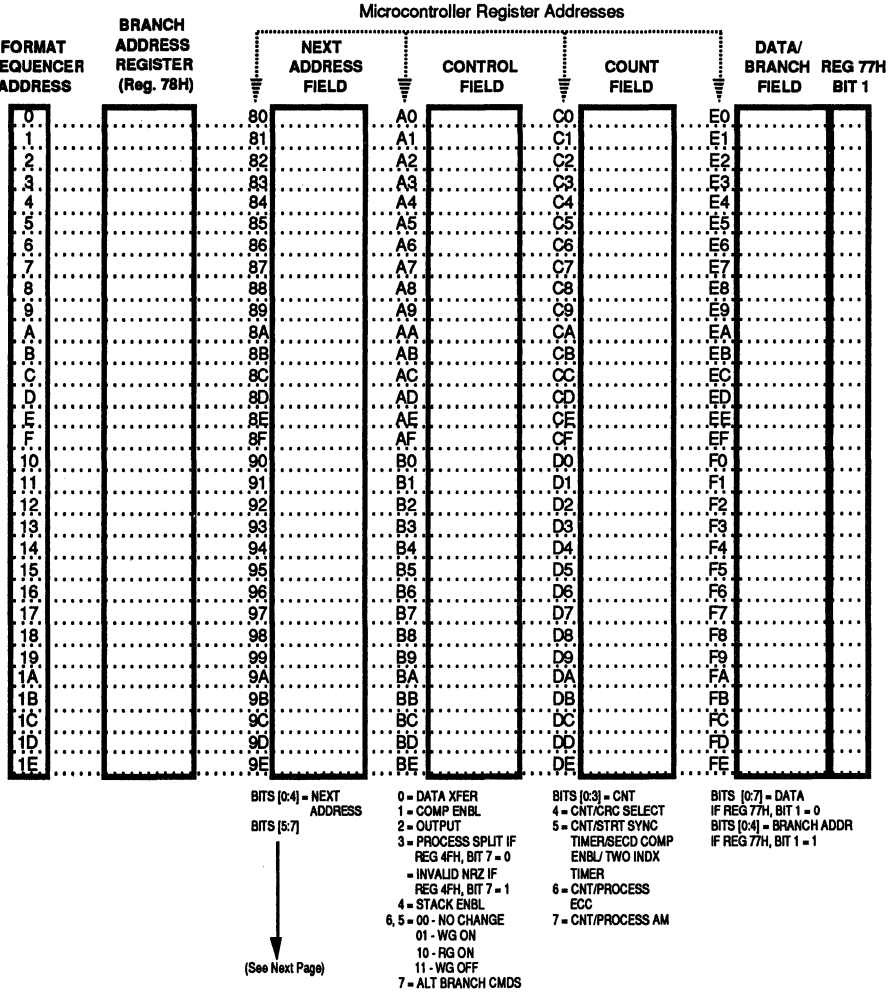
If the BUFFER MEMORY PARITY ENABLE bit (Register 53H, bit 3) is set, and a parity error is detected at the serializer/deserializer (SERDES), then the DISK/BUFFER PARITY ERROR bit (Register 7AH, bit 6) is set. Additionally, the CL-SH351 has a branch command that can be used to stop the Format Sequencer when a disk/buffer parity error is detected. Refer to the section *RAM Data Buffer Parity* for more details.

5. REGISTER ADDRESSES AND INITIALIZATION CONDITIONS

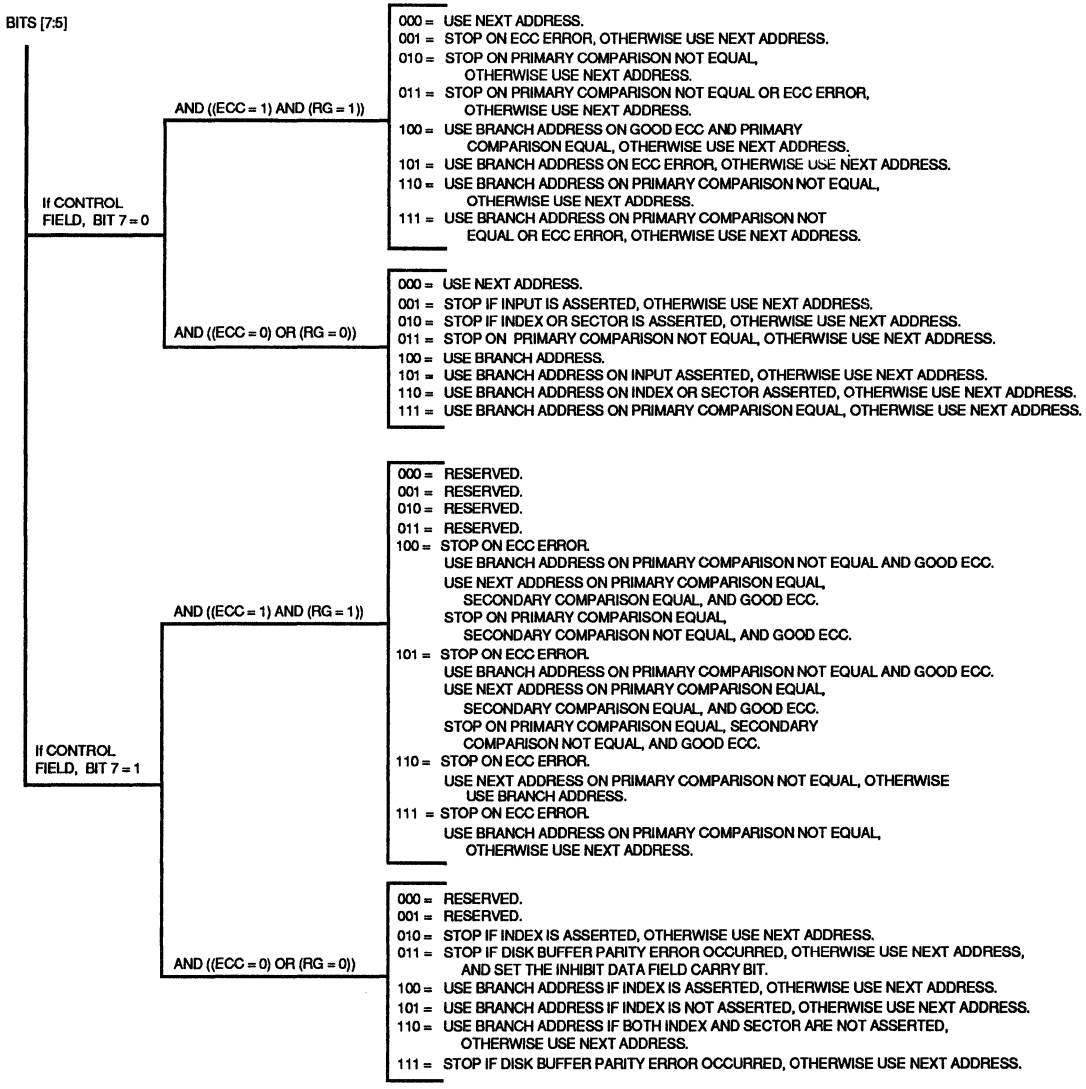
5.1 Memory Map



5.2 Writable Control Store (WCS) Worksheet



5.2 Writable Control Store (WCS) Worksheet *(cont.)*



5.3 Register Initialization

REGISTER ADDRESS	RST* (Pin 40)	SRST* (Pin 72)	REG53H (Bit 5=1)	REG 4FH (Bit 0=1)	REG 71H (Bit 3=1)	REGISTER BIT VALUE 7	6	5	4	3	2	1	0
40H/60H W						X	X	X	X	X	X	X	X
41H/61H	✓	✓	✓			0	0	0	0	0	0	0	0
42H/62H	✓	✓	✓			0	0	0	0	0	0	0	0
43H/63H	✓	✓	✓			0	0	0	0	0	0	0	0
44H/64H	✓		✓			0	0	0	0	0	0	0	0
45H/65H	✓	✓	✓			0	0	0	0	0	0	0	0
46H/66H	✓		✓			X	X	0	0	0	0	0	0
46H/66H		✓				X	X	0	0	0	0	0	1
47H/67H	✓		✓			X	X	0	0	0	0	0	0
48H	✓	✓	✓			0	0	0	0	0	0	0	0
49H	✓		✓			0	0	0	0	0	0	0	0
4AH	✓					X	X	X	X	X	X	X	X
4BH	✓					0	0	0	0	0	0	1	0
4EH	✓					0	0	0	0	0	0	0	0
4FH	✓					0	0	0	0	0	0	0	1
50H	✓		✓			0	0	0	0	0	0	0	0
51H	✓		✓			0	0	0	0	0	0	0	0
52H	✓	✓	✓			0	0	0	0	0	0	0	0
53H	✓					1	1	1	0	0	0	0	0
54H	✓					0	0	0	0	0	0	0	0
55H	✓					0	0	0	0	0	0	0	0
56H	✓					0	0	0	0	0	0	0	0
57H	✓		✓			0	0	0	0	0	0	0	0
58H	✓		✓			0	0	0	0	0	0	0	0
59H	✓		✓			0	0	0	0	0	0	0	0
5AH	✓	✓	✓			0	0	0	0	0	0	0	0
5BH	✓	✓	✓			0	0	0	0	0	0	0	0
5CH	✓	✓	✓			0	0	0	0	0	0	0	0
5DH	✓	✓	✓			0	0	0	0	0	0	0	0
5EH	✓	✓	✓			0	0	0	0	0	0	0	0
5FH	✓	✓	✓			0	0	0	0	0	0	0	0
70H	✓					0	0	0	0	0	0	0	0
71H	✓			✓		X	0	X	0	0	0	0	0
72H	✓			✓		0	0	0	0	0	0	0	0
73H	✓			✓	✓	1	1	1	1	1	1	1	1
74H	✓			✓	✓	1	1	1	1	1	1	1	1
75H	✓			✓	✓	1	1	1	1	1	1	1	1
76H	✓			✓	✓	1	1	1	1	1	1	1	1
77H	✓			✓		X	X	0	0	0	0	0	0
78H R	✓			✓		X	X	X	1	1	1	1	1
W	✓			✓		X	X	X	0	0	0	0	0
79H R	✓			✓		0	0	0	0	0	0	0	0
W	✓			✓		X	X	X	0	0	0	0	0
7AH †	✓				Bits 3-0	X	0	0	0	0	0	0	0
7BH	✓					0	0	0	0	0	0	0	0
7CH	✓					0	0	0	0	0	0	0	0
7DH	✓			✓		0	0	0	0	0	0	0	0
7EH	✓			✓		0	0	0	0	0	0	0	0
7FH R						X	X	X	X	X	X	X	X
W	✓			✓		0	0	0	0	0	0	0	0
9FH	✓			✓		0	0	0	1	1	1	1	1
BFH	✓			✓		0	0	0	0	0	0	0	0
DFH	✓			✓		0	0	0	0	0	0	0	0
FFH	✓			✓		0	0	0	0	0	0	0	0
80H-9EH						X	X	X	X	X	X	X	X
A0-BEH						X	X	X	X	X	X	X	X
C0-DEH						X	X	X	X	X	X	X	X
E0-FEH						X	X	X	X	X	X	X	X

NOTE: † Also reset by a write to Register 79H. X means indeterminate.

6. SCSI INTERFACE REGISTER DESCRIPTIONS

6.1 40H/60H — DIRECT SCSI ACCESS PORT (Read/Write)

This register has no initialization conditions.

Bits 0-7	Address 40H/60H decode allows the microcontroller direct access to the SCSI data bus. Data written to this address is stored and driven onto the SCSI data bus when the MICROCONTROLLER DIRECT SCSI OUTPUT ENABLE bit (Register 45H/65H, bit 3) is set. A microcontroller read of address 40H/60H reads the information directly from the SCSI data bus (the MICROCONTROLLER DIRECT SCSI OUTPUT ENABLE bit (Register 45H/65H, bit 3) must be reset for the SCSI data bus read).

6.2 41H/61H — SELECTION/RESELECTION ID INPUT (Read Only)

This register is reset when the SCSI RESET signal (pin 72) or the RST* signal (pin 40) is asserted low, or by a Host/Buffer Reset (Register 53H, bit 5).

Bits 0-7	When the SCSI AUTOMATIC SELECTION/RESELECTION ENABLE bit (Register 45H/65H, bit 1) is set, after the CL-SH351 has been selected or reselected, this register contains the combined source and destination IDs. The microcontroller should read this register after a selection/reselection of the device in order to determine the source ID.

6.3 41H/61H — SELECTION/RESELECTION ID OUTPUT (Write Only)

This register is reset when the SCSI RESET signal (pin 72) or the RST* signal (pin 40) is asserted low, or by a Host/Buffer Reset (Register 53H, bit 5).

Bits 0-7	When the SCSI AUTOMATIC SELECTION/RESELECTION ENABLE bit (Register 45H/65H, bit 1) is set, then the contents of this register are automatically driven onto the SCSI data bus during a SCSI Selection/Reselection Phase after winning the SCSI Arbitration Phase. The microcontroller should write the logical OR of the source and destination SCSI IDs to Register 41H/ 61H before the SCSI Selection/Reselection Phase can occur.

6.4 42H/62H — SCSI PHASE CONTROL (Read/Write)

This register is reset when the SCSI RESET signal (pin 72) or the RST* signal (pin 40) is asserted low, or by a Host/Buffer Reset (Register 53H, bit 5).

Bit 0	**SCSI CONTROL/DATA*:** Writing to this bit stores a value which is driven onto the SCSI COMMAND/DATA signal (pin 77) when the ENABLE TARGET bit (Register 45H/65H, bit 4) is set, or stores the value of the expected state compared with the SCSI COMMAND/DATA signal (pin 77) when the ENABLE INITIATOR bit (Register 45H/65H, bit 5) is set. The value written is logically inverted before being driven onto the SCSI COMMAND/DATA signal (pin 77) in Target Mode or compared with the value on the SCSI COMMAND/DATA (pin 77) signal in Initiator Mode. Reading this bit provides the logically inverted value of the SCSI COMMAND/DATA signal (pin 77).
Bit 1	**SCSI INPUT/OUTPUT*:** Writing to this bit stores a value which is driven onto the SCSI INPUT/OUTPUT signal (pin 79) when the ENABLE TARGET bit (Register 45H/65H, bit 4) is set, or stores the value of the expected state compared with the SCSI INPUT/OUTPUT signal (pin 79) when the ENABLE INITIATOR bit (Register 45H/65H, bit 5) is set. The value written is logically inverted before being driven onto the SCSI INPUT/OUTPUT signal (pin 79) or compared with the value on the SCSI INPUT/OUTPUT (pin 79) signal. Reading this bit provides the logically inverted value of the SCSI INPUT/OUTPUT signal (pin 79).
Bit 2	**SCSI MESSAGE:** Writing to this bit stores a value which is driven onto the SCSI MESSAGE signal (pin 73) when the ENABLE TARGET bit (Register 45H/65H, bit 4) is set, or stores the value of the expected state compared with the SCSI MESSAGE signal (pin 73) when the ENABLE INITIATOR bit (Register 45H/65H, bit 5) is set. The value written is logically inverted before being driven onto the SCSI MESSAGE signal (pin 73) or compared with the value on the SCSI MESSAGE (pin 73) signal. Reading this bit provides the logically inverted value of the SCSI MESSAGE signal (pin 73).
Bit 3	**SCSI REQUEST:** The value written to this bit is logically inverted and driven onto the SCSI REQUEST signal (pin 78) when the ENABLE TARGET bit (Register 45H/65H, bit 4) is set. Reading this bit provides the logically inverted value of the SCSI REQUEST signal (pin 78).
Bit 4	**SCSI BUSY:** The value written to this bit is logically inverted and driven onto the SCSI BUSY signal (pin 69). This bit controls the SCSI BUSY signal (pin 69) ungated by any other signals. Reading this bit provides the logically inverted value of the SCSI BUSY signal (pin 69).
Bit 5	**SCSI SELECT:** The value written to this bit is logically inverted and driven onto the SCSI SELECT signal (pin 76). This bit controls the SCSI SELECT signal (pin 76) ungated by any other signals. Reading this bit provides the logically inverted value of the SCSI SELECT signal (pin 76).
Bit 6	**SCSI ATTENTION:** The value written to this bit is logically inverted and driven onto the SCSI ATTENTION signal (pin 68) when the ENABLE INITIATOR bit (Register 45H/65H, bit 5) is set. Reading this bit provides the logically inverted value of the SCSI ATTENTION signal (pin 68). This bit is set and the SCSI ATTENTION signal is asserted automatically when the following conditions are met: • The ENABLE INITIATOR bit (Register 45H/65H, bit 5) is set; • The SCSI PARITY ENABLE bit (Register 44H/64H, bit 3) is set; • The current SCSI Phase is DATA IN; • A SCSI Parity Error occurs.

6.4 42H/62H — SCSI PHASE CONTROL (Read/Write) *(cont.)*

Bit 7 **SCSI ACKNOWLEDGE:** The value written to this bit is logically inverted and driven onto the SCSI ACKNOWLEDGE signal (pin 70) when the ENABLE INITIATOR bit (Register 45H/65H, bit 5) is set. Reading this bit provides the logically inverted value of the SCSI ACKNOWLEDGE signal (pin 70).

6.5 43H/63H — SCSI SYNCHRONOUS CONTROL (Read/Write)

This register is reset when the SCSI RESET signal (pin 72) or the RST* signal (pin 40) is asserted low, or by a Host/Buffer Reset (Register 53H, bit 5).

Bits 0-3 **OFFSET COUNT:** These four binary encoded bits set the synchronous transfer offset count. An offset count of one to fifteen can be programmed for SCSI bus synchronous transfers. An offset count of zero specifies an asynchronous transfer. Unlimited REQ/ACK offsets are not supported.

Synchronous Transfer Offset Count Table

Register 43H/63H Bits 3 2 1 0	Offset	*Register 43H/63H Bits* 3 2 1 0	Offset
0 0 0 0	= 0	1 0 0 0	= 8
0 0 0 1	= 1	1 0 0 1	= 9
0 0 1 0	= 2	1 0 1 0	= 10
0 0 1 1	= 3	1 0 1 1	= 11
0 1 0 0	= 4	1 1 0 0	= 12
0 1 0 1	= 5	1 1 0 1	= 13
0 1 1 0	= 6	1 1 1 0	= 14
0 1 1 1	= 7	1 1 1 1	= 15

Bits 4-7 **SYNCHRONOUS TRANSFER RATE:** These bits, in combination with the SYSCLK clock frequency, set the SCSI bus synchronous transfer rate. The equation for determining the synchronous transfer period is shown below.

T = SYSCLK Period
Synchronous Transfer Period = (P * T)

Synchronous Transfer Multiplier Table

Register 43H/63H Bits 7 6 5 4	P	*Register 43H/63H Bits* 7 6 5 4	P
0 0 0 0	= Reset State-RESERVED	1 0 0 0	= 9
0 0 0 1	= RESERVED	1 0 0 1	= 10
0 0 1 0	= 3	1 0 1 0	= 11
0 0 1 1	= 4	1 0 1 1	= 12
0 1 0 0	= 5	1 1 0 0	= 13
0 1 0 1	= 6	1 1 0 1	= 14
0 1 1 0	= 7	1 1 1 0	= 15
0 1 1 1	= 8	1 1 1 1	= RESERVED

6.6 44H/64H — SCSI MODE CONTROL (Read/Write)

This register is reset when the RST* signal (pin 40) is asserted low, or by a Host/Buffer Reset (Register 53H, bit 5).

Bits 0-2 **SCSI ID BITS:** These bits are the CL-SH351 encoded SCSI ID. An ID of 7 has the highest priority and an ID of 0 has the lowest.

Register 44H/64H Bits

2	1	0	SCSI ID
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Bit 3 **SCSI PARITY ENABLE:** Setting this bit enables the SCSI parity checking circuitry. The CL-SH351 always generates odd parity onto the SCSI bus.

Bit 4 **SCSI LOGIC CLOCK DISABLE:** The user must program this bit to be reset. When this bit is set, the internal SCSI logic clock is disabled. It is used for test purposes.

Bits 5-7 **SCSI LOGIC CLOCK PRESCALAR:** These bits specify the clock used for the SCSI Phase logic. The specified clock period should be within the range of 200 - 400 ns.

Register 44H/64H Bits

7	6	5	
0	0	0	= SYSCLK/2
0	0	1	= SYSCLK/4
0	1	0	= SYSCLK/6
0	1	1	= SYSCLK/8

Register 44H/64H Bits

7	6	5	
1	0	0	= SYSCLK/10
1	0	1	= SYSCLK/12
1	1	0	= SYSCLK/14
1	1	1	= SYSCLK/16

6.7 45H/65H — SCSI OPERATION CONTROL (Read/Write)

This register is reset when the SCSI RESET signal (pin 72) or the RST* signal (pin 40) is asserted low, or by a Host/Buffer Reset (Register 53H, bit 5).

Bit 0	**ARBITRATION/SELECTION START:** When this bit is set, the CL-SH351 will proceed to gain control of the SCSI bus through automatic implementation of a successful SCSI Arbitration Phase. As long as arbitration is impossible due to SCSI bus activity or a SCSI Arbitration Phase has been lost, the CL-SH351 will continue to monitor the SCSI bus to attempt arbitration until a SCSI Arbitration Phase is won or until this bit is reset.
Bit 1	**SCSI AUTOMATIC SELECTION/RESELECTION ENABLE:** When set, this bit enables the CL-SH351 to respond automatically to being selected or reselected. Also when this bit is set, the CL-SH351 is able to proceed automatically to either a SCSI Selection or Reselection Phase after winning the SCSI Arbitration Phase. A microcontroller reset of this bit will abort the selection/reselection process.
Bit 2	**SCSI AUTOMATIC SELECTION/RESELECTION MODE:** If the SCSI AUTOMATIC SELECTION /RESELECTION ENABLE bit (bit 1) is set and this bit is set, the CL-SH351 will automatically proceed to a SCSI Selection Phase after arbitration is won; and if this bit is reset, the CL-SH351 will proceed to a SCSI Reselection Phase.
Bit 3	**MICROCONTROLLER DIRECT SCSI OUTPUT ENABLE:** When this bit is set and the ENABLE TARGET or the ENABLE INITIATOR bit (bits 4 and 5, respectively) is set, the CL-SH351 will drive the contents of the DIRECT SCSI ACCESS PORT (Register 40H/60H) onto the SCSI DATA BUS (pins 52-54, 57, 59-62). Parity will be gated onto the SCSI DATA BUS PARITY signal (pin 64).
Bit 4	**ENABLE TARGET:** SCSI Outputs On Phase and handshake signals controlled by a Target are enabled when this bit is set. This bit need only be set by the local microcontroller for firmware controlled operations, as this will be set and reset throughout real-time automatic operations under the control of the CL-SH351 logic. A SCSI Bus Free Phase will inhibit setting this bit, either the SCSI BUSY signal (pin 69) or the SCSI SELECT signal (pin 76) must be asserted low on the SCSI bus to allow this bit to be set.
Bit 5	**ENABLE INITIATOR:** SCSI outputs on control and handshake signals controlled by an Initiator are enabled when this bit is set. This bit need only be set by the local microcontroller for firmware controlled operations, as this will be set and reset throughout real-time automatic operations under the control of the CL-SH351 logic. A SCSI Bus Free Phase will inhibit setting this bit, either the SCSI BUSY signal (pin 69) or the SCSI SELECT signal (pin 76) must be asserted low on the SCSI bus to allow this bit to be set.
Bit 6	**TEST MODE.**
Bit 7	**SCSI RESET OUT:** When this bit is set, the SCSI RESET signal (pin 72) will be asserted low.

6.8 46H/66H — SCSI STATUS REGISTER 1 (Read/Write)

When the SCSI RESET signal (pin 72) is asserted low, it sets bit 0 and resets bits 1-5 of this register. Bits 0-5 are reset when the RST* signal (pin 40) is asserted low, or by a Host/Buffer Reset (Register 53H, bit 5). Bits 0-5 must be reset by the microcontroller by writing a one to that bit, thus clearing interrupts (if enabled in Register 47H/67H and Register 4FH, bits 1 and 6) and receiving further updated status.

Bit 0	**SCSI RESET DETECTED:** This bit reflects the SCSI RESET signal (pin 72) history. When this bit is set, a SCSI reset has occurred and can still be in effect since this bit was last reset.
Bit 1	**SCSI ATTENTION DETECTED:** This bit reflects the SCSI ATTENTION signal (pin 68) history. When this bit is set, a SCSI ATTENTION assertion has been detected and can still be in effect since this bit was last reset.
Bit 2	**SCSI OFFSET OVERRUN/UNDERRUN DETECTED:** When this bit is set, it indicates that in SCSI Synchronous Transfer Mode an offset overrun/ underrun was detected.
Bit 3	**SCSI BUS FREE DETECTED:** When this bit is set, it indicates that a SCSI Bus Free Phase has been detected since this bit was last reset.
Bit 4	**SCSI/BUFFER PARITY ERROR DETECTED:** This bit reflects the error history for transfers from the buffer memory to the SCSI interface. When this bit is set, a parity error was detected transferring data from the buffer memory to the internal SCSI interface.
Bit 5	**SCSI BUS PARITY ERROR DETECTED:** This bit reflects the SCSI bus parity error history. When this bit is set, a SCSI bus parity error was detected.
Bit 6	**SCSI PARITY ERROR:** This bit reflects odd parity of the internal SCSI bus. The user is responsible to ensure that data is stable on the internal SCSI bus for this signal to have a valid state.
Bit 7	**SCSI RST IN:** This bit reflects the logically inverted state of the SCSI RESET signal (pin 72).

6.9 47H/67H — SCSI INTERRUPT ENABLE REGISTER 1 (Read/Write)

This register is reset when the RST* signal (pin 40) is asserted low or by a Host/Buffer Reset (Register 53H, bit 5).

Bit 0	**SCSI RESET DETECTED ENABLE:** When this bit set, it causes the HINT* signal (pin 28) to be asserted low when the SCSI RESET DETECTED bit (Register 46H/66H, bit 0) is set.
Bit 1	**ATTENTION DETECTED ENABLE:** When this bit is set, it causes the HINT* signal (pin 28) to be asserted low when the SCSI ATTENTION DETECTED bit (Register 46H/66H, bit 1) is set.
Bit 2	**OFFSET OVERRUN/UNDERRUN ENABLE:** When this bit is set, it causes the HINT* signal (pin 28) to be asserted low when the SCSI OFFSET OVERRUN/UNDERRUN DETECTED bit (Register 46H/66H, bit 2) is set.
Bit 3	**SCSI BUS FREE DETECTED ENABLE:** When this bit is set, it causes the HINT* signal (pin 28) to be asserted low when the SCSI BUS FREE DETECTED bit (Register 46H/66H, bit 3) is set.
Bit 4	**SCSI/BUFFER PARITY ERROR ENABLE:** When this bit is set, it causes the HINT* signal (pin 28) to be asserted low when the SCSI/BUFFER PARITY ERROR DETECTED bit (Register 46H/66H, bit 4) is set.
Bit 5	**SCSI BUS PARITY ERROR ENABLE:** When this bit is set, it causes the HINT* signal (pin 28) to be asserted low when the SCSI BUS PARITY ERROR DETECTED bit (Register 46H/ 66H, bit 5) is set.
Bits 6-7	**RESERVED.**

6.10 48H — SCSI STATUS REGISTER 2 (Read/Write)

This register is reset when the SCSI RESET signal (pin 72) or the RST* signal (pin 40) is asserted low, or by a Host/Buffer Reset (Register 53H, bit 5). Each bit must be reset by the microcontroller by writing a one to that bit, thus clearing interrupts (if enabled in Register 49H and Register 4FH, bits 1 and 6) and receiving further updated status.

Bit 0 **DEVICE SELECTED:** When this bit is set, the CL-SH351 has answered a SCSI selection attempt since this bit was last reset. When the SCSI AUTOMATIC SELECTION/RESELECTION ENABLE bit (Register 45H/65H, bit 1) is set, the CL-SH351 will detect the combination of:

- the SCSI SELECT signal (pin 76) asserted low,
- the SCSI BUSY signal (pin 69) deasserted high,
- the SCSI INPUT/OUTPUT signal (pin 79) deasserted high,
- the CL-SH351 SCSI ID (Register 44H/64H, bits 0-2) is asserted on the SCSI DATA BUS (pins 52-54, 57, 59-62),
- no more than two ID bits are asserted on the SCSI DATA BUS (pins 52-54, 57, 59-62),
- SCSI parity is correct (if the SCSI PARITY ENABLE bit (Register 44H/64H, bit 3) is set) and
- the SCSI RESET signal (pin 72) is deasserted high.

The detection of the above combination will:

- set this bit (DEVICE SELECTED),
- set the ENABLE TARGET bit (Register 45H/65H, bit 4)
- assert low the SCSI BUSY signal (pin 69 and Register 42H/62H, bit 4) and
- latch the SCSI DATA BUS (pins 52-54, 57, 59-62) (accessible in the SELECTION/RESELECTION ID INPUT Register (41H/61H)).

Bit 1 **DEVICE RESELECTED:** When this bit is set, the CL-SH351 has answered a SCSI reselection attempt since this bit was last reset. When the SCSI AUTOMATIC SELECTION/RESELECTION ENABLE bit (Register 45H/65H, bit 1) is set, the CL-SH351 will detect the combination of:

- the SCSI SELECT signal (pin 76) asserted low,
- the SCSI BUSY signal (pin 69) deasserted high,
- the SCSI INPUT/OUTPUT signal (pin 79) asserted low,
- the CL-SH351 SCSI ID (Register 44H/64H, bits 0-2) is asserted on the SCSI DATA BUS (pins 52-54, 57, 59-62),
- exactly two ID bits are asserted on the SCSI DATA BUS (pins 52-54, 57, 59-62),
- SCSI parity is correct (if the SCSI PARITY ENABLE bit (Register 44H/64H, bit 3) is set) and
- the SCSI RESET signal (pin 72) is deasserted high.

The detection of the above combination will:

- set this bit (DEVICE RESELECTED),
- assert low the SCSI BUSY signal (pin 69 and Register 42H/62H, bit 4) until the SCSI SELECT signal (pin 76) is deasserted high
- set the ENABLE INITIATOR bit (Register 45H/65H, bit 5) and
- latch the SCSI DATA BUS (pins 52-54, 57, 59-62) (accessible in the SELECTION/RESELECTION ID INPUT Register (41H/61H)).

6.10 48H — SCSI STATUS REGISTER 2 (Read/Write) *(cont.)*

Bit 2	**ARBITRATION WON:** When this bit is set, it indicates that a requested SCSI Arbitration Phase has been won by the CL-SH351 since this bit was last reset. If the SCSI AUTOMATIC SELECTION/ RESELECTION ENABLE bit (Register 45H/65H, bit 1) is set then the CL-SH351 will proceed to the SCSI Selection or Reselection Phase depending on the value programmed in the SCSI AUTOMATIC SELECTION/RESELECTION MODE bit (Register 45H/65H, bit 2).
Bit 3	**AUTOMATIC SELECTING/RESELECTING DONE:** When this bit is set, it indicates that the automatic SCSI Selection/Reselection Phase is completed.
Bit 4	**TRANSFER DONE:** When this bit is set, it indicates the completion of a SCSI transfer. Note that when this bit is set, it also means that the last SCSI handshake has been completed, and/or the last buffer memory cycle is completed. This is valid for DMA or Programmed I/O (PIO) transfers.
Bit 5	**TRANSFER HALTED:** When this bit is set, it indicates that a SCSI transfer was halted due to either a microcontroller halt request done by resetting the DMA START bit (Register 52H, bit 1) or a phase mismatch in Initiator Mode.
Bit 6	**SCSI PHASE MISMATCH:** When this bit is set, it indicates that SCSI COMMAND/ DATA signal (pin 77), the SCSI INPUT/OUTPUT signal (pin 79), and the SCSI MESSAGE signal (pin 73) do not match the expected phase (Register 42H/62H, bits 0-2) as programmed by the Initiator (the ENABLE INITIATOR bit (Register 45H/65H, bit 5) is set).
Bit 7	**REQ-ON:** When this bit is set, it indicates that assertion low of the SCSI REQUEST signal (pin 78) has been detected since this bit was last reset. This function is enabled only when the ENABLE INITIATOR bit (Register 45H/65H, bit 5) is set.

6.11 49H — SCSI INTERRUPT ENABLE REGISTER 2 (Read/Write)

This register is reset when the RST* signal (pin 40) is asserted low or by a Host/Buffer Reset (Register 53H, bit 5).

Bit 0	**DEVICE SELECTED ENABLE**: When this bit is set, it causes the HINT* signal (pin 28) to be asserted low when the DEVICE SELECTED bit (Register 48H, bit 0) is set.
Bit 1	**DEVICE RESELECTED ENABLE:** When this bit is set, it causes the HINT* signal (pin 28) to be asserted low when the DEVICE RESELECTED bit (Register 48H, bit 1) is set.
Bit 2	**ARBITRATION WON ENABLE**: When this bit is set, it causes the HINT* signal (pin 28) to be asserted low when the ARBITRATION WON bit (Register 48H, bit 2) is set.
Bit 3	**AUTOMATIC SELECTING/RESELECTING ENABLE:** When this bit is set, it causes the HINT* signal (pin 28) to be asserted low when the AUTOMATIC SELECTING/RESELECTING DONE bit (Register 48H, bit 3) is set.
Bit 4	**TRANSFER DONE ENABLE**: When this bit is set, it causes the HINT* signal (pin 28) to be asserted low when the TRANSFER DONE bit (Register 48H, bit 4) is set.
Bit 5	**TRANSFER HALTED**: When this bit is set, it causes the HINT* signal (pin 28) to be asserted low when the TRANSFER HALTED bit (Register 48H, bit 5) is set.
Bit 6	**SCSI PHASE MISMATCH ENABLE:** When this bit is set, it causes the HINT* signal (pin 28) to be asserted low when the SCSI PHASE MISMATCH bit (Register 48H, bit 6) is set.
Bit 7	**REQ-ON ENABLE**: When this bit is set, it causes the HINT* signal (pin 28) to be asserted low when the REQ-ON bit (Register 48H, bit 7) is set.

6.12 4AH — MICROCONTROLLER SCSI FIFO ACCESS PORT (Read/Write)

This register has no initialization conditions.

Bits 0-7	The register is the microcontroller SCSI FIFO access port. Writing to this address writes the microcontroller data to the FIFO.

6.13 4BH — MISCELLANEOUS CONTROL/STATUS REGISTER (Read/Write)

Bits 0-3	This register contains the chip revision number.
Bit 4	**DRAM BURST LENGTH SELECT**: When reset, it selects a DRAM burst length of 4. When set, selects a DRAM burst length of 8. This bit is reset when RST* signal (pin 40) is asserted low.

7. BUFFER MANAGER REGISTER DESCRIPTIONS

7.1 50H — SCHEDULED BUFFER DATA (Read/Write)

This register is reset when the RST* signal (pin 40) is asserted low, or by a Host/Buffer Reset (Register 53H, bit 5).

Bits 0-7 The local microcontroller uses this register to access the buffer memory (using the Disk Address Pointer). Data can be either read or written through this register. Additionally, the configuration switches on the buffer memory data bus are also read through this register (using the MOE DISABLE bit (Register 53H, bit 4)).

7.2 51H — BUFFER STATUS/CONTROL REGISTER (Read/Write)

This register is reset when the RST* signal (pin 40) is asserted low, or by a Host/Buffer Reset (Register 53H, bit 5).

Bits 0-3 **SYNCHRONOUS DATA TRANSFER OFFSET:** A microcontroller read of bits 0-3 give the running synchronous offset count.

Register 51H Bits 3 2 1 0	*Current* Offset	*Register 51H* Bits 3 2 1 0	*Current* Offset
0 0 0 0	= 0	1 0 0 0	= 8
0 0 0 1	= 1	1 0 0 1	= 9
0 0 1 0	= 2	1 0 1 0	= 10
0 0 1 1	= 3	1 0 1 1	= 11
0 1 0 0	= 4	1 1 0 0	= 12
0 1 0 1	= 5	1 1 0 1	= 13
0 1 1 0	= 6	1 1 1 0	= 14
0 1 1 1	= 7	1 1 1 1	= 15

Bit 4 **CLEAR FIFO:** When this bit is set, it causes the FIFO to be cleared. This bit must be reset before any access to the FIFO is attempted.

Bit 5 **SCSI DATA SET UP SELECT:** This bit selects the SCSI data set-up time in Asynchronous Mode, referenced to the SYSCLK period, T.

Bit 5	SCSI Data Set-Up Time
0	T
1	2T

NOTE: This is a logical value rather than an absolute value. See the AC parameters (Section 11.3) for specific data set-up times.

7.2 51H — BUFFER STATUS/CONTROL REGISTER (Read/Write) *(cont.)*

Bit 6 **SYNC SCSI DATA SET UP SELECT:** This bit selects the SCSI data set-up time in Synchronous Mode, referenced to SYSCLK period T, and synchronous Transfer Rate P, (Register 43/63 bits 7-4).

Bit 6	SYNC SCSI Data Set-Up for Odd P	SYNC SCSI Data Set-Up for Even P
0	$\frac{(P-1)}{2} * T$	$\frac{P}{2} * T$
1	$\frac{P}{2} * T$	$\frac{P}{2} * T$

Bit 7 **SCSI ACTIVE PULL UP SELECT:** Setting this bit enables active pull-ups on SCSI data bus, ATN* (pin 68), C*/D (pin 77), I*/O (pin 79), MSG* (pin 73), REQ* (pin 78), ACK* (pin 70) when reset selects open drain on all SCSI signals except REQ* (pin 78) and ACK* (pin 70).

7.3 52H — BUFFER TRANSFER CONTROL (Read/Write)

This register is reset when the SCSI RESET signal (pin 72) or the RST* signal (pin 40) is asserted low, or by a Host/Buffer Reset (Register 53H, bit 5).

Bit 0	**RESERVED.**
Bit 1	**DMA START:** When this bit is set, the CL-SH351 starts a DMA transfer. The direction is programmed in the SCSI R/W* TRANSFER DIRECTION bit (bit 3). This bit is reset when (a) the transfer is completed, or (b) the CL-SH351 is in the Initiator Mode, the SCSI Phase does not match the expected phase, and the SCSI REQUEST signal (pin 78) is asserted low on the SCSI bus. A reset of this bit by the microcontroller causes a DMA halt in Target Mode only.
Bit 2	**PIO START:** When this bit is set, the CL-SH351 starts transfers through the FIFO. The transfer byte count is specified by the PIO TRANSFER COUNT, bits 4-7. This bit is reset when (a) the transfer is completed, or (b) the CL-SH351 is in the Initiator Mode, the SCSI Phase does not match the expected phase, and the SCSI REQUEST signal (pin 78) is asserted low on the SCSI bus.
Bit 3	**SCSI R/W* TRANSFER DIRECTION:** This bit indicates the direction of information transfer on the SCSI bus in both the Programmed I/O (PIO) and DMA Transfer Modes. When this bit is set, information is transferred from the CL-SH351. When this bit is reset, information is transferred to the CL-SH351.
Bits 4-7	**PIO TRANSFER COUNT:** The value written to these bits is the number of bytes to be transferred under Programmed I/O (PIO). A microcontroller read of these bits gives the running count of bytes to be transferred under Programmed I/O (PIO).

Register 52H Bits 7 6 5 4		*PIO Transfer Count*	*Register 52H Bits* 7 6 5 4		*PIO Transfer Count*
0 0 0 0	=	0	1 0 0 0	=	8
0 0 0 1	=	1	1 0 0 1	=	9
0 0 1 0	=	2	1 0 1 0	=	10
0 0 1 1	=	3	1 0 1 1	=	11
0 1 0 0	=	4	1 1 0 0	=	12
0 1 0 1	=	5	1 1 0 1	=	13
0 1 1 0	=	6	1 1 1 0	=	14
0 1 1 1	=	7	1 1 1 1	=	15

7.4 53H — BUFFER MODE CONTROL (Read/Write)

When the RST* signal (pin 40) is asserted low, bits 5-7 of this register are set and bits 0-4 are reset.

Bit 0 **DRAM/SRAM*:** This bit selects the Buffer Manager Mode of operation. When this bit is set, the DRAM Mode is selected. When this bit is reset, the SRAM Mode is selected.

Bits 1-2 **DRAM TYPE:** These bits select the size of DRAM for buffer memory. The sizes supported are 64K, 256K, and 1M DRAMS as shown below:

Register 53H Bits 2 1	Description
0 0	64K DRAM
0 1	256K DRAM
1 0	1M DRAM
1 1	RESERVED

Bit 3 **BUFFER MEMORY PARITY ENABLE:** Setting this bit enables the buffer memory parity checking circuit on every read access of the buffer memory. The checking is enabled for buffer memory reads whether the destination is the host SCSI port or the disk SERDES logic. The CL-SH351 generates odd parity on every buffer memory write access regardless of the state of this bit. The SCSI bus parity value is passed through the CL-SH351 to the BUFFER DATA PARITY signal if the SCSI PARITY ENABLE bit (Register 44H/64H, bit 3) is set; otherwise, the odd parity value from the SCSI bus data is generated. Odd parity is always generated from the 8-bit deserialized data from the disk.

Bit 4 **MOE DISABLE:** When this bit is set, the MOE* signal (pin 15) in SRAM Mode and the MOE* signal (pin 15), the BA16/RAS* signal (pin 14), and the BA17/CAS* signal (pin 5) in DRAM Mode are disabled. This is intended to support switch reads (via the SCHEDULED BUFFER DATA Register (50H)) of the buffer memory data bus.

Bit 5 **HOST/BUFFER RESET:** Assertion of the RST* signal (pin 40) sets this bit and generates a hardware reset condition. When this bit is set by the microcontroller, a software reset condition is generated. Either reset stops all operations in the Buffer Manager and SCSI host logic. The software reset initializes Registers 40H/60H-47H/67H, 48H, 49H, 50H, 52H, and 57H-5FH. All SCSI signals are switched to a high-impedance state. The Buffer Manager signals are unaffected by a software reset.

Bits 6-7 **WAIT STATES:** These bits select the number of wait states the READY signal (pin 21) is deasserted for accessing the CL-SH351 internal registers. One wait state is defined to be T, the period of the SYSCLK signal (pin 41). The READY signal (pin 21) is asserted with respect to the ALE signal (pin 35). The number of wait states as listed below is measured from the assertion of the READ STROBE signal (pin 20), the WRITE STROBE signal (pin 19), or the DATA STROBE signal (pin 20).

Register 53H Bits 7 6	Description
0 0	No Wait States
0 1	1-2 Wait States
1 0	2-3 Wait States
1 1	3-4 Wait States

7.5 54H — BUFFER MANAGER TIMING CONTROL (Read/Write)

This register is reset when the RST* signal (pin 40) is asserted low.

Bits 0-1 **RAS* LOW TIME/SRAM CYCLE TIME:** When DRAM is used, this field specifies the number of SYSCLK cycles the BA16/RAS* signal (pin 14) is asserted in a Non-Page Mode DRAM access cycle. When SRAM is used, this field specifies the SRAM cycle time.

T = SYSCLK Period
RAS* LOW TIME, Twrl =

Bits 1 0	Bits 1 0	Bits 1 0	Bits 1 0
0 0 = 2T	0 1 = 3T	1 0 = 4T	1 1 = 5T

SRAM BUFFER ACCESS TIME, Twba =

Bits 1 0	Bits 1 0	Bits 1 0	Bits 1 0
0 0 = 2T	0 1 = 3T	1 0 = 4T	1 1 = 5T

Bits 2-3 **RAS* HIGH TIME:** When DRAM is used, this field specifies the minimum number of SYSCLK cycles the BA16/RAS* signal (pin 14) is deasserted (RAS precharge time).

T = SYSCLK Period
RAS* HIGH TIME, Twrh =

Bits 3 2	Bits 3 2	Bits 3 2	Bits 3 2
0 0 = T	0 1 = 2T	1 0 = 3T	1 1 = 4T

Bits 4-5 **CAS* LOW TIME:** When DRAM is used, this field specifies the number of SYSCLK cycles the BA17/CAS* signal (pin 5) is asserted in a DRAM Page Mode access.

T = SYSCLK Period
CAS* LOW TIME, Twcl =

Bits 5 4	Bits 5 4	Bits 5 4	Bits 5 4
0 0 = T	0 1 = 2T	1 0 = 3T	1 1 = 4T

Bits 6-7 **CAS* HIGH TIME:** When DRAM is used, this field specifies the minimum number of SYSCLK cycles the BA17/CAS* signal (pin 5) is deasserted in a DRAM Page Mode access.

T = SYSCLK Period
CAS* HIGH TIME, Twch =

Bits 7 6	Bits 7 6	Bits 7 6	Bits 7 6
0 0 = T	0 1 = 2T	1 0 = 3T	1 1 = 4T

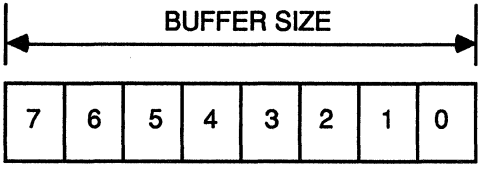
7.6 55H — DRAM REFRESH PERIOD (Read/Write)

This register is reset when the RST* signal (pin 40) is asserted low.

Bits 0-7	This register holds the most significant 8 bits of the 9-bit refresh period, the least significant bit (inaccessible) is always set. The refresh period is specified in the number of SYSCLK cycles.

7.7 56H — SEGMENT SIZE (Read/Write)

This register is reset when the RST* signal (pin 40) is asserted low.



00H =	4K bytes
01H =	8K bytes
03H =	16K bytes
07H =	32K bytes
0FH =	64K bytes
1FH =	128K bytes
3FH =	256K bytes
7FH =	512K bytes
FFH =	1 Mbytes

Bits 0-7	This register specifies the segment size (in bytes) where the codes for a given segment size are in the above table. The value programmed in this register controls the incrementing of address pointer bits. For example, when a 2K segment size is programmed, only the lower 12 bits are incremented.

7.8 57H — DISK ADDRESS POINTER LOW (DAPL) (Read/Write)

This register is reset when the RST* signal (pin 40) is asserted low, or by a Host/Buffer Reset (Register 53H, bit 5).

Bits 0-7	This register is the low-order byte of the buffer memory address for disk and microcontroller accesses.

7.9 58H — DISK ADDRESS POINTER MIDDLE (DAPM) (Read/Write)

This register is reset when the RST* signal (pin 40) is asserted low, or by a Host/Buffer Reset (Register 53H, bit 5).

Bits 0-7	This register is the middle-order byte of the buffer memory address for disk and microcontroller accesses.

7.10 59H — DISK ADDRESS POINTER HIGH (DAPH) (Read/Write)

This register is reset when the RST* signal (pin 40) is asserted low, or by a Host/Buffer Reset (Register 53H, bit 5).

Bits 0-3	These bits are the high-order byte of the buffer memory address for disk and microcontroller accesses.
Bits 4-7	**RESERVED.**

7.11 5AH — HOST ADDRESS POINTER LOW (HAPL) (Read/Write)

This register is reset when the SCSI RESET signal (pin 72) or the RST* signal (pin 40) is asserted low, or by a Host/Buffer Reset (Register 53H, bit 5).

Bits 0-7	This register is the low-order byte of the buffer memory address for host accesses.

7.12 5BH — HOST ADDRESS POINTER MIDDLE (HAPM) (Read/Write)

This register is reset when the SCSI RESET signal (pin 72) or the RST* signal (pin 40) is asserted low, or by a Host/Buffer Reset (Register 53H, bit 5).

Bits 0-7	This register is the middle-order byte of the buffer memory address for host accesses.

7.13 5CH — HOST ADDRESS POINTER HIGH (HAPH) (Read/Write)

This register is reset when the SCSI RESET signal (pin 72) or the RST* signal (pin 40) is asserted low, or by a Host/Buffer Reset (Register 53H, bit 5).

Bits 0-3	These bits are the high-order byte of the buffer memory address for host accesses.
Bits 4-7	**RESERVED.**

7.14 5DH — STOP ADDRESS POINTER LOW (SAPL) (Read/Write)

This register is reset when the SCSI RESET signal (pin 72) or the RST* signal (pin 40) is asserted low, or by a Host/Buffer Reset (Register 53H, bit 5).

Bits 0-7	This register is the low-order byte of the Stop Address Pointer (SAP) for host accesses.

7.15 5EH — STOP ADDRESS POINTER MIDDLE (SAPM) (Read/Write)

This register is reset when the SCSI RESET signal (pin 72) or the RST* signal (pin 40) is asserted low, or by a Host/Buffer Reset (Register 53H, bit 5).

Bits 0-7	This register is the middle-order byte of the Stop Address Pointer (SAP) for host accesses.

7.16 5FH — STOP ADDRESS POINTER HIGH (SAPH) (Read/Write)

This register is reset when the SCSI RESET signal (pin 72) or the RST* signal (pin 40) is asserted low, or by a Host/Buffer Reset (Register 53H, bit 5).

Bits 0-3	These bits are the high-order byte of the Stop Address Pointer (SAP) for host accesses.
Bits 4-7	**RESERVED.**

8. SECTOR FORMATTER REGISTER DESCRIPTIONS

8.1 4EH — SECTOR SIZE (Read/Write)

This register is reset when the RST* signal (pin 40) is asserted low.

Bits 0-7	Writing to this register sets the number of 256-byte data blocks to be transferred by the Format Sequencer when the INHIBIT DATA FIELD CARRY bit (Register 77H, bit 4) is used. The value programmed should be one less than the number of underflows of the Current Sequencer Word COUNT FIELD that will be inhibited. With this register set to 00H, and the INHIBIT DATA FIELD CARRY bit (Register 77H, bit 4) set, only one underflow of the Current Sequencer Word COUNT FIELD will be inhibited. For a 532-byte Data Field, set the COUNT FIELD of the Format Sequencer word to 13H, set this register to 01H, and set the INHIBIT DATA FIELD CARRY bit (Register 77H, bit 4). For a 4096-byte Data Field, set the COUNT FIELD of the Format Sequencer word to FFH, set this register to 0EH, and set the INHIBIT DATA FIELD CARRY bit (Register 77H, bit 4).

8.2 4FH — SECTOR FORMATTER MODE CONTROL (Read/Write)

This register is reset (except for bit 0 which will be set) when the RST* signal (pin 40) is asserted low.

Bit 0	**SECTOR FORMATTER RESET:** When the RST* signal (pin 40) is asserted low, this bit is set and generates a hardware reset condition. When this bit is set by the microcontroller, a software reset condition is generated. Either reset stops all operations in the Sector Formatter. The software reset initializes Registers 71H-76H, 78H-7EH, 9FH, BFH, DFH, FFH, deasserts the READ GATE signal (pin 43), the WRITE GATE signal (pin 44), and switches the NRZ signal (pin 46) to a high-impedance state. The Sector Formatter will remain in the reset condition as long as this bit is set. The reset condition can be removed by resetting this bit. Refer to the section on register reset conditions (Section 5.3).
Bit 1	**LOCAL HINT* ENABLE:** When this bit is set, it enables local interrupt capability on the HINT* signal (pin 28). The individual sources of interrupts can still be disabled by the Interrupt Enable Registers (Registers 47H/67H and 49H).
Bit 2	**LOCAL DINT* ENABLE:** When this bit is set, it enables local interrupt capability on the DINT* signal (pin 17). The individual sources of interrupts can still be disabled by the SECTOR FORMATTER INTERRUPT ENABLE Register (7EH).
Bit 3	**LOCAL INT* PIN PULL-UP DISABLE:** When this bit is set, it disables the pull-up on both the HINT* signal (pin 28) and the DINT* signal (pin 17), leaving an open drain output. This is intended to support system-level, multiple interrupt sources.
Bit 4	**SCSI INTERFACE REGISTER DECODE SELECT:** When this bit is set, the address space 40H-47H is decoded. When this bit is reset, the address space 60H-67H is decoded. After a Sector Formatter reset, decode of both address spaces is disabled until this register is written.
Bit 5	**HARD/SOFT* SECTOR MODE CONTROL:** When this bit is set, it selects the Hard Sector Mode. In this mode, the WAM*/AMD*/SECTOR signal (pin 39) functions as a SECTOR input signal. The SECTOR DETECTED bit (Register 7DH, bit 1) and Branch-on-Sector circuit will be triggered by the edge programmed by the EDGE DETECT SENSITIVITY SELECTION bit (Register 77H, bit 5) of the SECTOR signal. When this bit is reset, it selects the Soft Sector Mode. In this mode, only the WAM*/AMD* functions are enabled. The WAM*/AMD*/SECTOR signal (pin 39) is an input during NRZ Data Read operations and an external ENDEC must assert the input in order to synchronize the incoming NRZ data stream.
Bit 6	**LOCAL INT* MODE ENABLE:** When this bit is set, it routes both the HINT* and DINT* internal signals to the DINT* signal (pin 17) and disables any output to the HINT* signal (pin 28).
Bit 7	**SPLIT FIELD MODE DISABLE:** When this bit is reset, bit 3 of the CONTROL FIELD of the Current Sequencer Word functions as the PROCESS SPLIT control bit. When this bit is set, bit 3 of the CONTROL FIELD of the Current Sequencer Word functions as the INVALID NRZ CONTROL bit.

8.3 70H — SYNCHRONIZATION BYTE-COUNT LIMIT (Read/Write)

This register is reset when the RST* signal (pin 40) is asserted low.

Bits 0-7	This register holds the byte-count limit for NRZ Read Data synchronization attempts. This value is programmable from 0 to 255. Refer to the description of the COUNT/START SYNCHRONIZATION TIMER/SECONDARY COMPARE ENABLE/TWO INDEX TIMER bit (bit 5 of the Writable Control Store (WCS) COUNT FIELD) (Section 9.3). When the timer has been activated, the value is decremented for each byte time that passes. If the value reaches zero, the SYNCHRONIZATION TIME-OUT ERROR bit (Register 7AH, bit 4) is set. Reading this register provides the running count (if the timer is active), or the programmed limit if the timer is inactive.

8.4 71H — ECC CONTROL (Read/Write)

This register is reset when the RST* signal (pin 40) is asserted low, or by a Sector Formatter Reset (Register 4FH, bit 0).

Bit 0	**ECC SYNDROME REVERSAL/CORRECTION CONTROL:** Setting this bit selects the Correction function. Resetting this bit selects the ECC Syndrome Reversal function. To start either of these functions the ECC SHIFT CONTROL bit (bit 1) must be set.
Bit 1	**ECC SHIFT CONTROL:** Setting this bit starts the function selected in the ECC SYNDROME REVERSAL/CORRECTION CONTROL bit (bit 0). If the ECC SYNDROME REVERSAL/CORRECTION CONTROL bit (bit 0) is reset, setting this bit starts shifting data from the ECC CORRECTION SHIFT-REGISTER/COUNTER (Register 72H) into the ECC circuit. This bit is cleared automatically after the shift is completed. If the ECC SYNDROME REVERSAL/CORRECTION CONTROL bit (bit 0) is set, setting this bit starts the correction process. In this case, this bit is cleared if a correctable error is found, or the ECC circuit was shifted 256 bytes. The ECC CORRECTION SHIFT-REGISTER/COUNTER (Register 72H) is a byte counter and, in the case of a correctable error, will provide the means of determining the error offset. Note that all shifts are performed on byte boundaries. During normal read, write and format operations this bit should be set to zero.
Bit 2	**DISABLE ECC FEEDBACK:** Setting this bit causes the ECC circuit to function as a 32/56-bit shift register.
Bit 3	**INITIALIZE ECC:** ECC status will be held preset while this bit is set and read or write operations are not in progress. If this bit is set during a read or write operation, the ECC status bits will be re-initialized at the end of that operation.
Bit 4	**CORRECTABLE ERROR FOUND:** This bit indicates that the hardware ECC correction circuit has decoded a correctable error and has shifted the error burst to a byte boundary. This bit is valid after the ECC SHIFT CONTROL bit (bit 1) has gone from set to reset.
Bit 5	**RESERVED.**
Bit 6	**32/56 BIT ECC SELECT:** When this bit is set, the 56-bit ECC polynomial is selected. When this bit is reset, the 32-bit ECC polynomial is selected.
Bit 7	**RESERVED.**

8.5 72H — ECC CORRECTION SHIFT-REGISTER/COUNTER (Read/Write)

This register is reset when the RST* signal (pin 40) is asserted low, or by a Sector Formatter Reset (Register 4FH, bit 0).

Bits 0-7	When the ECC SYNDROME REVERSAL/CORRECTION CONTROL bit (Register 71H, bit 0) is set, this is an eight-bit counter used in the ECC correction algorithm to determine error placement. When the ECC SYNDROME REVERSAL/CORRECTION CONTROL bit (Register 71H, bit 0) is reset, this is a shift register used in the ECC correction algorithm for syndrome reversal.

8.6 73H — ECC Status 0 (31-24)/(7-0) (Read Only)

This register is set when the RST* signal (pin 40) is asserted low, or by a Sector Formatter Reset (Register 4FH, bit 0), or when the INITIALIZE ECC bit (Register 71H, bit 3) is set.

Bits 0-7	**STATUS ECC BITS (31-24)/(7-0):** When the 56-bit ECC is selected, these are ECC bits 31-24 (bit 0 = ECC bit 31). When the 32-bit ECC is selected, these are ECC bits 7-0 (bit 0 = ECC bit 7). The status of the bits in this register is only valid when the ECC is not cycling.

8.7 74H — ECC Status 1 (39-32)/(15-8) (Read Only)

This register is set when the RST* signal (pin 40) is asserted low, or by a Sector Formatter Reset (Register 4FH, bit 0), or when the INITIALIZE ECC bit (Register 71H, bit 3) is set.

Bits 0-7	**STATUS ECC BITS (39-32)/(15-8):** When the 56-bit ECC is selected, these are ECC BITs 39-32 (bit 0 = ECC BIT 39). When the 32-bit ECC is selected, these are ECC bits 15-8 (bit 0 = ECC BIT 15). The status of the bits in this register is only valid when the ECC is not cycling.

8.8 75H — ECC Status 2 (47-40)/(23-16) (Read Only)

This register is set when the RST* signal (pin 40) is asserted low, or by a Sector Formatter Reset (Register 4FH, bit 0), or when the INITIALIZE ECC bit (Register 71H, bit 3) is set.

Bits 0-7	**STATUS ECC BITS (47-40)/(23-16):** When the 56-bit ECC is selected, these are ECC bits 47-40 (bit 0 = ECC bit 47). When the 32-bit ECC is selected, these are ECC bits 23-16 (bit 0 = ECC bit 16). The status of the bits in this register is only valid when the ECC is not cycling.

8.9 76H — ECC Status 3 (55-48)/(31-24) (Read Only)

This register is set when the RST* signal (pin 40) is asserted low, or by a Sector Formatter Reset (Register 4FH, bit 0), or when the INITIALIZE ECC bit (Register 71H, bit 3) is set.

Bits 0-7	**STATUS ECC BITS (55-48)/(31-24):** When the 56-bit ECC is selected, these are ECC bits 55-48 (bit 0 = ECC bit 55). When the 32-bit ECC is selected, these are ECC bits 31-24 (bit 0 = ECC bit 31). The status of the bits in this register is only valid when the ECC is not cycling.

8.10 77H — SECTOR FORMATTER OPERATION CONTROL (Read/Write)

This register is reset when the RST* signal (pin 40) is asserted low, or by a Sector Formatter Reset (Register 4FH, bit 0).

Bit 0	**ENABLE SECTOR BRANCH:** When this bit is set, the WAM*/AMD*/ SECTOR signal (pin 39) is 'ORed' with the INDEX signal (pin 37) in the Format Sequencer branch logic. This allows the microcontroller to control certain Format Sequencer branch commands that can be triggered by the INDEX signal (pin 37) alone, or triggered by the INDEX signal (pin 37) and the SECTOR signal. Note that index and sector-dependent branch commands only test the index condition in Soft Sector Mode (Register 4FH, bit 5).
Bit 1	**DATA/BRANCH FIELD MODE ENABLE:** When this bit is set, the Format Sequencer uses the DATA/BRANCH FIELD (Register FFH) as a source for branch addresses instead of bits 0-4 of the BRANCH ADDRESS (Register 78H). When this bit is reset, the Format Sequencer uses bits 0-4 of the BRANCH ADDRESS Register (78H) as a source for branch addresses. This bit does not alter the address source for branch commands that use both the BRANCH ADDRESS (Register 78H) and the DATA/BRANCH FIELD (Register FFH) for potential address sources.
Bit 2	**SUPPRESS TRANSFER:** When this bit is set, the buffer access mechanism of Data Transfer (Current Sequencer Word CONTROL FIELD, bit 0) is disabled. During a write operation, the NRZ data field will be written with the pattern of the Current Sequencer Word DATA/BRANCH FIELD (Register FFH). During a read operation, the incoming NRZ data will have ECC verified, but no data will be transferred to the buffer memory.
Bit 3	**BUFFER/DISK R/W* TRANSFER DIRECTION:** This bit indicates the direction of information transfer to/from the Sector Formatter when disk data transfer is initiated by the Sector Formatter. When this bit is reset, the data transfer direction is from the Sector Formatter to the buffer memory. When this bit is set, the data transfer direction is from the buffer memory to the Sector Formatter.
Bit 4	**INHIBIT DATA FIELD CARRY:** When this bit is set, the Format Sequencer Byte Counter carry normally used to trigger the next fetch of a Writable Control Store (WCS) Word will be inhibited. This bit will be automatically reset whenever a carry has occurred and the SECTOR SIZE (Register 4EH) has previously been decremented to zero. This bit can be both set and reset by the Format Sequencer branch commands. When the Format Sequencer is running, writes to this register must be synchronized with the Format Sequencer activities.
Bit 5	**EDGE DETECT SENSITIVITY SELECTION:** This bit specifies which edge (rising or falling) triggers the Sector and Index edge detect circuits. This bit modifies the Format Sequencer branch logic, the Sector Detected (Register 7DH, bit 1) logic, and the Index Detected (Register 7DH, bit 0) logic. When this bit is reset, only rising edges will trigger the edge detect circuitry. When this bit is set, only falling edges will trigger the edge detect circuitry.

8.10 77H — SECTOR FORMATTER OPERATION CONTROL (Read/Write) *(cont.)*

Bit 6	**TWO INDEX DETECTION MODE ENABLE:** When this bit is set, the Two Index Detect circuitry is enabled. When enabled the circuitry is armed if the read gate-on code, and Data Transfer of WCS Control Field are off and bit 5 of the WCS Count Field is set. Once the circuitry is armed, it will disarm upon one of the following three events: 1) Two Index Detect Mode Enable is reset; 2) two index pulses are detected; 3) disk data transfer between the Formatter and the buffer memory. When the circuitry is armed, and two index edges are detected, the Two Index Detected (Register 7AH, bit 5) status bit is set. The status bit remains set until the circuitry is re-armed, or the Two Index Detection Mode enable is reset.
Bit 7	**RESERVED.**

8.11 78H — NEXT FORMAT SEQUENCER ADDRESS (Read)

This register is reset when the RST* signal (pin 40) is asserted low, or by a Sector Formatter Reset (Register 4FH, bit 0).

Bits 0-4	**NEXT ACTIVE FORMAT SEQUENCER ADDRESS:** Bits 0-4 provide the next Writable Control Store (WCS) address to be executed by the Format Sequencer. This address could read the contents of the FORMAT SEQUENCER START ADDRESS Register (79H), or the BRANCH ADDRESS Register (78H), or the Current Sequencer Word NEXT ADDRESS FIELD (Register 9FH) or the DATA/BRANCH FIELD (Register FFH).
Bits 5-7	**RESERVED.**

8.12 78H — BRANCH ADDRESS (Write)

This register is reset when the RST* signal (pin 40) is asserted low, or by a Sector Formatter Reset (Register 4FH, bit 0).

Bits 0-4	**BRANCH ADDRESS:** The Format Sequencer jumps to the address specified in these bits when a branch condition is programmed and met.
Bits 5-7	**RESERVED.**

8.13 79H — FORMAT SEQUENCER STATUS REGISTER 1 (Read)

This register is reset when the RST* signal (pin 40) is asserted low, or by a Sector Formatter Reset (Register 4FH, bit 0).

Bit 0	**FORMAT SEQUENCER ACTIVE:** This bit is set while the Format Sequencer is in an active processing state.
Bit 1	**AM ACTIVE:** This bit is set when the DATA TRANSFER bit (Writable Control Store (WCS) CONTROL FIELD, bit 0) is reset and the COUNT/PROCESS AM bit (Writable Control Store (WCS) COUNT FIELD, bit 7) is set. It is reset after reading or writing of the ECC bytes. It is also reset when the Format Sequencer stops.
Bit 2	**DATA TRANSFER:** This bit is set during data transfers between the buffer memory and the disk, that is any time the DATA TRANSFER bit (Writable Control Store (WCS) CONTROL FIELD, bit 0) is set even if the SUPPRESS TRANSFER bit (Register 77H, bit 2) is set.
Bit 3	**BRANCH ACTIVE:** This bit is set when a branch condition is met. Reading this register resets this bit.
Bit 4	**SYNCHRONIZATION DETECT STATUS:** This bit is set during a disk read operation when the internal serializer/deserializer has been synchronized with the NRZ Read Data (a match has been found between the NRZ Read Data and the preprogrammed sync character in the SYNCHRONIZATION BYTE PATTERN (Register 7CH)). This bit is reset on the falling (trailing) edge of the READ GATE signal (pin 43).
Bit 5	**FORMAT SEQUENCER INPUT:** This bit indicates the status of the INPUT signal (pin 36).
Bit 6	**FORMAT SEQUENCER OUTPUT:** This bit indicates the status of the OUTPUT bit (Writable Control Store (WCS) CONTROL FIELD, bit 2).
Bit 7	**BYTE READY:** When this bit is set, it indicates that the scheduled buffer memory access is completed, and that another scheduled buffer memory access may be started.

8.14 79H — FORMAT SEQUENCER START ADDRESS (Write)

This register is reset when the RST* signal (pin 40) is asserted low, or by a Sector Formatter Reset (Register 4FH, bit 0).

Bits 0-4	**START ADDRESS:** A write to this register starts the Format Sequencer at the address written to this register.
Bits 5-7	**RESERVED.**

8.15 7AH — FORMAT SEQUENCER STATUS REGISTER 2 (Read Only)

This register is reset when the RST* signal (pin 40) is asserted low, or by a Sector Formatter Reset (Register 4FH, BIT 0), or by a Format Sequencer start (a write to the FORMAT SEQUENCER START ADDRESS Register (79H)). Setting the INITIALIZE ECC bit (Register 71H, bit 3) resets bits 3-0.

Bit 0	**PRIMARY COMPARE NOT EQUAL:** This bit is set when the result of the compare operation is not equal. The comparison is performed between the NRZ Read Data and either the buffer memory data or the DATA/BRANCH FIELD in the Current Sequencer Word on all bytes where comparison was enabled in the COMPARE ENABLE bit (Writable Control Store (WCS) CONTROL FIELD, bit 1). PRIMARY COMPARE NOT EQUAL is only valid after the Format Sequencer has completed processing the ECC field. The INITIALIZE ECC bit (Register 71H, bit 3) will also reset this bit.
Bit 1	**SECONDARY COMPARE NOT EQUAL:** This bit is set when the result of the secondary compare operation is not equal. The comparison is performed between the NRZ Read Data and the DATA/BRANCH FIELD in the Current Sequencer Word on all bytes where comparison was enabled in both the SECONDARY COMPARE ENABLE bit (Writable Control Store (WCS) COUNT FIELD, bit 5) and the COMPARE ENABLE bit (Writable Control Store (WCS) CONTROL FIELD, bit 1). SECONDARY COMPARE NOT EQUAL is only valid after the Format Sequencer has completed processing the ECC field. The INITIALIZE ECC bit (Register 71H, bit 3) will also reset this bit.
Bit 2	**ECC ERROR:** This bit is set after the last ECC bit is read if there is a non-zero ECC syndrome indicating a read error. This status is reset upon the start of a Format Sequencer read or write operation. The INITIALIZE ECC bit (Register 71H, bit 3) will also reset this bit.
Bit 3	**DATA FIELD ECC ERROR:** This bit is set after the last ECC bit is read if there is a non-zero ECC syndrome indicating a read error in a data field. This status is reset upon the start of a Format Sequencer read or write operation. The INITIALIZE ECC bit (Register 71H, bit 3) will also reset this bit.
Bit 4	**SYNCHRONIZATION TIME-OUT ERROR:** This bit is set after a time-out occurs and read synchronization has not occurred. The timer limit is held in the SYNCHRONIZATION BYTE-COUNT LIMIT (Register 70H). The timer is enabled in the Current Sequencer Word.
Bit 5	**TWO INDEX DETECTED:** This bit is set when the Two Index Counter has detected the second Index pulse on the INDEX signal (pin 37).
Bit 6	**DISK/BUFFER PARITY ERROR:** This bit is set by a buffer parity error during a buffer read (disk data read by the Format Sequencer or the microcontroller) with the BUFFER MEMORY PARITY ENABLE bit (Register 53H, bit 3) set.
Bit 7	**RESERVED.**

8.16 7BH — WAM CONTROL (Read/Write)

This register is reset when the RST* signal (pin 40) is asserted low.

Bits 0-7	In Soft Sector Mode, the WAM*/AMD*/SECTOR signal (pin 39) will be asserted low for each bit cell time corresponding to the bits set in this register during a Write Address Mark operation. Output at the WAM*/AMD*/SECTOR signal (pin 39) is shifted three bits toward the LSB at the output. In Hard Sector Mode, the signal will not be driven by the CL-SH351.

8.17 7CH — SYNCHRONIZATION BYTE PATTERN (Read/Write)

This register is reset when the RST* signal (pin 40) is asserted low.

Bits 0-7	This register value is to be compared with the NRZ Read Data on the rising (leading) edge of the READ GATE signal (pin 43). A match (masked by the contents of the SYNCHRONIZATION COMPARE MASK (Register 7FH)) between the contents of this register and the NRZ Read Data will set the SYNCHRONIZATION DETECT STATUS bit (Register 79H, bit 4), will re-initialize to the original value and stop the Synchronization Timer and will allow the NRZ Read Data to be gated into the ECC circuitry. In Soft Sector Mode, only the WAM*/AMD* functions are enabled. The WAM*/AMD*/SECTOR signal (pin 39) is an input during the NRZ Data Read operation and an external ENDEC must assert low this input in order to synchronize the incoming NRZ data stream.

8.18 7DH — SECTOR FORMATTER INTERRUPT (Read/Write)

This register is reset when the RST* signal (pin 40) is asserted low, or by a Sector Formatter Reset (Register 4FH, bit 0). Each bit must be reset by the microcontroller by writing a one to that bit, thus clearing interrupts (if enabled in Register 4FH, bits 1 and 6, and Register 7EH), and receiving further updated status.

Bit 0	**INDEX DETECTED:** This bit is set by the edge programmed by the EDGE DETECT SENSITIVITY SELECTION bit (Register 77H, bit 5) of the INDEX signal (pin 37).
Bit 1	**SECTOR DETECTED:** This bit is set by the edge programmed by the EDGE DETECT SENSITIVITY SELECTION bit (Register 77H, bit 5) of the WAM*/AMD*/SECTOR signal (pin 39) when the Hard Sector Mode (Register 4FH, bit 5) is selected.
Bit 2	**INPUT DETECTED:** This bit is set by the leading (rising) edge of the INPUT signal (pin 36).
Bit 3	**SEQUENCER STOPPED DETECTED:** This bit is set by the Format Sequencer cycling to the stopped condition.
Bit 4	**BRANCH ACTIVE DETECTED:** This bit is set by the Format Sequencer meeting a programmed branch or stop condition.
Bit 5	**DATA TRANSFER DETECTED:** This bit is set by the Format Sequencer executing a Current Sequencer Word with bit 0 of the Writable Control Store (WCS) CONTROL FIELD set.
Bit 6	**SEQUENCER OUTPUT DETECTED:** This bit is set by the Format Sequencer executing a Current Sequencer Word with bit 2 of the Writable Control Store (WCS) CONTROL FIELD set.
Bit 7	**SECONDARY MISCOMPARE DETECTED:** This bit is set when the result of a secondary compare operation is not equal.

8.19 7EH — SECTOR FORMATTER INTERRUPT ENABLE (Read/Write)

This register is reset when the RST* signal (pin 40) is asserted low, or by a Sector Formatter Reset (Register 4FH, bit 0).

Bit 0	**INDEX DETECTED ENABLE:** When this bit is set, it enables the DINT* signal (pin 17) to be asserted low when the INDEX DETECTED bit (Register 7DH, bit 0) is set.
Bit 1	**SECTOR DETECTED ENABLE:** When this bit is set, it enables the DINT* signal (pin 17) to be asserted low when the SECTOR DETECTED bit (Register 7DH, bit 1) is set.
Bit 2	**INPUT DETECTED ENABLE:** When this bit is set, it enables the DINT* signal (pin 17) to be asserted low when the INPUT DETECTED bit (Register 7DH, bit 2) is set.
Bit 3	**SEQUENCER STOPPED DETECTED ENABLE:** When this bit is set, it enables the DINT* signal (pin 17) to be asserted low when the SEQUENCER STOPPED DETECTED bit (Register 7DH, bit 3) is set.
Bit 4	**BRANCH ACTIVE DETECTED ENABLE:** When this bit is set, it enables the DINT* signal (pin 17) to be asserted low when the BRANCH ACTIVE DETECTED bit (Register 7DH, bit 4) is set.
Bit 5	**DATA TRANSFER DETECTED ENABLE:** When this bit is set, it enables the DINT* signal (pin 17) to be asserted low when the DATA TRANSFER DETECTED bit (Register 7DH, bit 5) is set.
Bit 6	**SEQUENCER OUTPUT DETECTED ENABLE:** When this bit is set, it enables the DINT* signal (pin 17) to be asserted low when the SEQUENCER OUTPUT DETECTED bit (Register 7DH, bit 6) is set.
Bit 7	**SECONDARY MISCOMPARE DETECTED ENABLE:** When this bit is set, it enables the DINT* signal (pin 17) to be asserted low when the SECONDARY MISCOMPARE DETECTED bit (Register 7DH, bit 7) is set.

8.20 7FH — SECTOR FORMATTER STACK (Read Only)

This register has no initialization conditions.

Bits 0-7	The first microcontroller read of this address after a Format Sequencer operation reads the last byte that was written (enabled by the STACK ENABLE bit (bit 4) of the Writable Control Store (WCS) CONTROL FIELD) onto the stack. Each read of this address rotates the data in a ring fashion in the stack so the entire stack can be read. The data is read in LIFO (Last In, First Out) order. The stack is ten bytes deep. If more than ten bytes are written to the stack only the last ten bytes are saved. If more than ten bytes are read from the stack then the ten bytes of data are read continuously in a circular manner.

8.21 7FH — SYNCHRONIZATION COMPARE MASK (Write Only)

This register is reset when the RST* signal (pin 40) is asserted low.

Bits 0-7	This register is used to control the pattern matching of NRZ Read Data against the SYNCHRONIZATION BYTE PATTERN (Register 7CH). Each bit set in this register disables the comparison of that bit position during the pattern matching.

9. WRITABLE CONTROL STORE (WCS) FIELD DESCRIPTIONS

9.1 80H-9EH — NEXT ADDRESS FIELD (Read/Write)

The Writable Control Store (WCS) has no initialization conditions.

BITS [7:5]

If CONTROL FIELD, BIT 7 = 0

AND ((ECC = 1) AND (RG = 1))

000 = USE NEXT ADDRESS.
001 = STOP ON ECC ERROR, OTHERWISE USE NEXT ADDRESS.
010 = STOP ON PRIMARY COMPARISON NOT EQUAL, OTHERWISE USE NEXT ADDRESS.
011 = STOP ON PRIMARY COMPARISON NOT EQUAL OR ECC ERROR, OTHERWISE USE NEXT ADDRESS.
100 = USE BRANCH ADDRESS ON GOOD ECC AND PRIMARY COMPARISON EQUAL, OTHERWISE USE NEXT ADDRESS.
101 = USE BRANCH ADDRESS ON ECC ERROR, OTHERWISE USE NEXT ADDRESS.
110 = USE BRANCH ADDRESS ON PRIMARY COMPARISON NOT EQUAL, OTHERWISE USE NEXT ADDRESS.
111 = USE BRANCH ADDRESS ON PRIMARY COMPARISON NOT EQUAL OR ECC ERROR, OTHERWISE USE NEXT ADDRESS.

AND ((ECC = 0) OR (RG = 0))

000 = USE NEXT ADDRESS.
001 = STOP IF INPUT IS ASSERTED, OTHERWISE USE NEXT ADDRESS.
010 = STOP IF INDEX OR SECTOR IS ASSERTED, OTHERWISE USE NEXT ADDRESS.
011 = STOP ON PRIMARY COMPARISON NOT EQUAL, OTHERWISE USE NEXT ADDRESS.
100 = USE BRANCH ADDRESS.
101 = USE BRANCH ADDRESS ON INPUT ASSERTED, OTHERWISE USE NEXT ADDRESS.
110 = USE BRANCH ADDRESS ON INDEX OR SECTOR ASSERTED, OTHERWISE USE NEXT ADDRESS.
111 = USE BRANCH ADDRESS ON PRIMARY COMPARISON EQUAL, OTHERWISE USE NEXT ADDRESS.

If CONTROL FIELD, BIT 7 = 1

AND ((ECC = 1) AND (RG = 1))

000 = RESERVED.
001 = RESERVED.
010 = RESERVED.
011 = RESERVED.
100 = STOP ON ECC ERROR.
USE BRANCH ADDRESS ON PRIMARY COMPARISON NOT EQUAL AND GOOD ECC.
USE NEXT ADDRESS ON PRIMARY COMPARISON EQUAL, SECONDARY COMPARISON EQUAL, AND GOOD ECC.
STOP ON PRIMARY COMPARISON EQUAL, SECONDARY COMPARISON NOT EQUAL, AND GOOD ECC.
101 = STOP ON ECC ERROR.
USE BRANCH ADDRESS ON PRIMARY COMPARISON NOT EQUAL AND GOOD ECC.
USE NEXT ADDRESS ON PRIMARY COMPARISON EQUAL, SECONDARY COMPARISON EQUAL, AND GOOD ECC.
STOP ON PRIMARY COMPARISON EQUAL, SECONDARY COMPARISON NOT EQUAL, AND GOOD ECC.
110 = STOP ON ECC ERROR.
USE NEXT ADDRESS ON PRIMARY COMPARISON NOT EQUAL, OTHERWISE USE BRANCH ADDRESS.
111 = STOP ON ECC ERROR.
USE BRANCH ADDRESS ON PRIMARY COMPARISON NOT EQUAL, OTHERWISE USE NEXT ADDRESS.

AND ((ECC = 0) OR (RG = 0))

000 = RESERVED.
001 = RESERVED.
010 = STOP IF INDEX IS ASSERTED, OTHERWISE USE NEXT ADDRESS.
011 = STOP IF DISK BUFFER PARITY ERROR OCCURRED, OTHERWISE USE NEXT ADDRESS, AND SET THE INHIBIT DATA FIELD CARRY BIT.
100 = USE BRANCH ADDRESS IF INDEX IS ASSERTED, OTHERWISE USE NEXT ADDRESS.
101 = USE BRANCH ADDRESS IF INDEX IS NOT ASSERTED, OTHERWISE USE NEXT ADDRESS.
110 = USE BRANCH ADDRESS IF BOTH INDEX AND SECTOR ARE NOT ASSERTED, OTHERWISE USE NEXT ADDRESS.
111 = STOP IF DISK BUFFER PARITY ERROR OCCURRED, OTHERWISE USE NEXT ADDRESS.

9.1 80H-9EH — NEXT ADDRESS FIELD (Read/Write) *(cont.)*

Bits 0-4 **NEXT ADDRESS:** This is the address the Format Sequencer will go to after the down counter for the COUNT FIELD has reached zero and a branch has not been taken. There are 31 possible next address locations (00H-1EH). Fetching address 1FH stops the Format Sequencer.

Bits 5-7 **BRANCH COMMAND:** All branch commands are evaluated at the end of execution of the Current Sequencer Word.

NOTE: The Branch Address can be the BRANCH ADDRESS Register (78H) or the DATA/ BRANCH FIELD unless otherwise explicitly stated.

Branch commands when the ALTERNATE BRANCH COMMAND SELECT bit (bit 7) of the Writable Control Store (WCS) CONTROL FIELD is reset and all of the following conditions are true:

- the PROCESS ECC bit (bit 6) of the Writable Control Store (WCS) COUNT FIELD is set and
- the READ GATE signal (pin 43) is asserted:

000 = Use the NEXT ADDRESS FIELD.
001 = Stop on ECC error, otherwise use the NEXT ADDRESS FIELD.
010 = Stop on primary comparison not equal, otherwise use the NEXT ADDRESS FIELD.
011 = Stop on primary comparison not equal or ECC error, otherwise use the NEXT ADDRESS FIELD.
100 = Use the Branch Address on good ECC and primary comparison equal, otherwise use the NEXT ADDRESS FIELD.
101 = Use the Branch Address on ECC error, otherwise use the NEXT ADDRESS FIELD.
110 = Use the Branch Address on primary comparison not equal, otherwise use the NEXT ADDRESS FIELD.
111 = Use the Branch Address on primary comparison not equal or ECC error, otherwise use the NEXT ADDRESS FIELD.

Branch commands when the ALTERNATE BRANCH COMMAND SELECT bit (bit 7) of the Writable Control Store (WCS) CONTROL FIELD is reset and any of the following conditions are true:

- the PROCESS ECC bit (bit 6) of the Writable Control Store (WCS) COUNT FIELD is reset or
- the READ GATE signal (pin 43) is deasserted:

000 = Use the NEXT ADDRESS FIELD.
001 = Stop if the INPUT signal (pin 36) is asserted, otherwise use the NEXT ADDRESS FIELD.
010 = Stop if the INDEX signal (pin 37) or the SECTOR signal (pin 39) is asserted, otherwise use the NEXT ADDRESS FIELD.
011 = Stop on primary comparison not equal, otherwise use the NEXT ADDRESS FIELD.
100 = Use the Branch Address.
101 = Use the Branch Address when the INPUT signal (pin 36) is asserted, otherwise use the NEXT ADDRESS FIELD.

9.1 80H-9EH — NEXT ADDRESS FIELD (Read/Write) *(cont.)*

Bits 5-7 *(cont.)*

110 = Use the Branch Address when the INDEX signal (pin 36) or the SECTOR signal (pin 39) is asserted, otherwise use the NEXT ADDRESS FIELD.

111 = Use the Branch Address on primary comparison equal, otherwise use the NEXT ADDRESS FIELD.

Branch Commands when the ALTERNATE BRANCH COMMAND SELECT bit (bit 7) of the Writable Control Store (WCS) CONTROL FIELD is set and all of the following conditions are true:

- the PROCESS ECC bit (bit 6) of the Writable Control Store (WCS) COUNT FIELD is set and
- the READ GATE signal (pin 43) is asserted:

000 = RESERVED.
001 = RESERVED.
010 = RESERVED.
011 = RESERVED.
100 = Stop on ECC error.
Use the Branch Address on primary comparison not equal, and good ECC.
Use the NEXT ADDRESS FIELD on primary comparison equal, secondary comparison equal, and good ECC.
Stop on primary comparison equal, secondary comparison not equal, and good ECC.

101 = Stop on ECC error.
Use the BRANCH ADDRESS (Register 78H) on primary comparison not equal, and good ECC.
Use the NEXT ADDRESS FIELD on primary comparison equal, secondary comparison equal, and good ECC.
Use the DATA/BRANCH FIELD on primary comparison equal, secondary comparison not equal, and good ECC.

110 = Stop on ECC error.
Use the NEXT ADDRESS FIELD on primary comparison not equal, otherwise use the Branch Address.

111 = Stop on ECC error.
Use the Branch Address on primary comparison not equal, otherwise use the NEXT ADDRESS FIELD.

Branch commands when the ALTERNATE BRANCH COMMAND SELECT bit (bit 7) of the Writable Control Store (WCS) CONTROL FIELD is set and any of the following conditions are true:

- the PROCESS ECC bit (bit 6) of the Writable Control Store (WCS) COUNT FIELD is reset or
- the READ GATE signal (pin 43) is deasserted:

000 = RESERVED.
001 = RESERVED.

9.1 80H-9EH — NEXT ADDRESS FIELD (Read/Write) *(cont.)*

Bits 5-7 *(cont.)*

010 = Stop if the INDEX signal (pin 37) is asserted, otherwise use the NEXT ADDRESS FIELD.

011 = Stop if disk buffer parity error occurred, otherwise use the NEXT ADDRESS FIELD and set the INHIBIT DATA FIELD CARRY bit (Register 77H, bit 4).

100 = Use the Branch Address if the INDEX signal (pin 37) is deasserted, otherwise use the NEXT ADDRESS FIELD.

101 = Use the Branch Address if the INDEX signal (pin 37) is deasserted, otherwise use the NEXT ADDRESS FIELD.

110 = Use the Branch Address if both the INDEX signal (pin 37) and the SECTOR signal (pin 39) are deasserted, otherwise use the NEXT ADDRESS FIELD.

111 = Stop if a disk buffer parity error occurred, otherwise use the NEXT ADDRESS FIELD.

9.2 A0H-BEH — CONTROL FIELD (Read/Write)

The WCS has no initialization conditions.

Bit 0	**DATA TRANSFER:** When this bit is set, the COUNT FIELD is used as an eight-bit counter. Each byte cycle that this bit is set, a byte of data will be accessed for the serializer/deserializer from the buffer memory if the SUPPRESS TRANSFER bit (Register 77H, bit 2) is reset, or from the Writable Control Store (WCS) DATA/BRANCH FIELD if the SUPPRESS TRANSFER bit (Register 77H, bit 2) is set. If the WRITE GATE signal (pin 44) is asserted then a byte of data is read from the appropriate source. If the READ GATE signal (pin 43) is asserted then a byte of data is written to the buffer memory (if the SUPPRESS TRANSFER bit (Register 77H, bit 2) is reset).
Bit 1	**COMPARE ENABLE:** Each byte cycle that this bit is set and the READ GATE signal (pin 43) is asserted then the deserialized NRZ Read Data will be compared against the Writable Control Store (WCS) DATA/BRANCH FIELD or against the buffer memory data if a sector data field verify operation has been programmed.
Bit 2	**OUTPUT:** This bit is connected to the OUTPUT signal (pin 47) and can be used to synchronize the external circuitry or the microcontroller (through the internal interrupt circuitry, see Register 7DH, bit 6).
Bit 3	**PROCESS SPLIT/INVALID NRZ CONTROL:** When the SPLIT FIELD MODE DISABLE bit (Register 4FH, bit 7) is set, this bit is the INVALID NRZ CONTROL bit. When this bit is set and the READ GATE signal (pin 43) is asserted, the NRZ Read Data synchronization circuit is prevented from starting. NRZ data handling circuits in the Sector Formatter are also disabled. When the SPLIT FIELD MODE DISABLE bit (Register 4FH, bit 7) is reset, this bit functions as the PROCESS SPLIT control bit. This bit is used to synchronize the ECC generation or to synchronize the error detection circuitry when sharing a single ECC field over two or more data segments.
Bit 4	**STACK ENABLE:** When this bit is set, read data is pushed onto the ten-byte recirculating stack.

9.2 A0H-BEH — CONTROL FIELD (Read/Write) *(cont.)*

Bits 5-6 **CONTROL FIELD:** Bits 5-6 are encoded as follows:

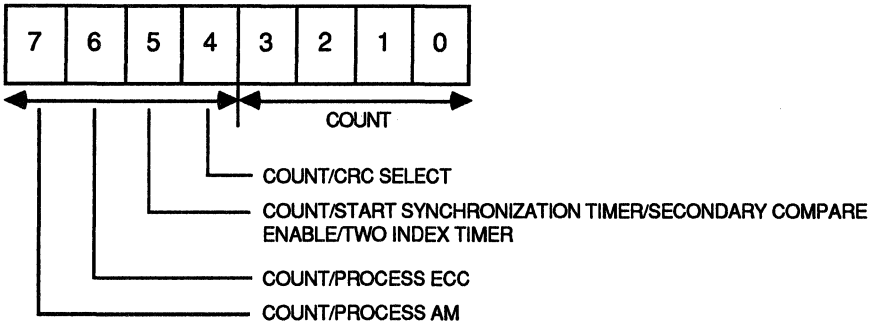
Encoded CONTROL FIELD Bits 5-6

CONTROL FIELD Bit 6	Bit 5	CODED AS	DESCRIPTION
0	0	NO CHANGE	The state of the WRITE GATE signal (pin 44) and the READ GATE signal (pin 43) is not affected.
0	1	WRITE GATE-ON	This code is used to assert the WRITE GATE signal (pin 44). The WRITE GATE signal (pin 44) is asserted during the first count of the execution of the Format Sequencer word with this bit combination set. The WRITE GATE signal (pin 44) is not asserted if the READ GATE signal (pin 43) is asserted when this bit combination is executed.
1	0	READ GATE-ON	This code is used to assert the READ GATE signal (pin 43). The READ GATE signal (pin 43) is asserted during the first count of the execution of the Format Sequencer word with this bit combination set. The READ GATE signal (pin 43) is not asserted if the WRITE GATE signal (pin 44) is asserted when this bit combination is executed. The READ GATE signal (pin 43) is deasserted at the end of ECC processing, or when the Format Sequencer goes to the stopped state.
1	1	WRITE GATE-OFF	This code is used to deassert the WRITE GATE signal (pin 44). The WRITE GATE signal (pin 44) is cleared during the last count of the execution of the Format Sequencer word with this bit combination set. The WRITE GATE signal (pin 44) is also deasserted when the Format Sequencer comes to the stop state.

Bit 7 **ALTERNATE BRANCH COMMAND SELECT:** When this bit is set, the branch conditions in the NEXT ADDRESS FIELD are redefined as described in Section 9.1).

9.3 C0H-DEH — COUNT FIELD (Read/Write)

This is the COUNT FIELD of the Writable Control Store (WCS) word. This sets the initial value of the Sequencer Counter when a new state is entered. The WCS has no initialization conditions.



Bits 0-3	**COUNT:** These bits are always used for the initial value of the low-order bits of the Format Sequencer Byte Counter for the execution of the Current Sequencer Word. The counter is decremented each byte time. When it reaches zero, a new Format Sequencer word will be fetched from the Writable Control Store (WCS). The byte counter is used in three modes of operation where unused bits are used as special control bits.
Bit 4	**COUNT/CRC SELECT:** This bit is used for two functions. **COUNT:** In this mode, this bit is used for the initial value of the Format Sequencer Byte Counter for the execution of the Current Sequencer Word. This mode is selected when the DATA TRANSFER bit (bit 0 of the Writable Control Store (WCS) CONTROL FIELD) is set, or if bits 5 and 6 of the CONTROL FIELD are not set for READ GATE-ON (bit 5 reset and bit 6 set of the Writable Control Store (WCS) CONTROL FIELD) or WRITE GATE-ON (bit 5 set and bit 6 reset of the Writable Control Store (WCS) CONTROL FIELD). **CRC SELECT:** In this mode, this bit is used to commit the ECC circuit to either the 16-bit CRC polynomial or the selected ECC polynomial. (The ECC polynomial is selected in the ECC CONTROL Register (71H).) When this bit is set, the 16-bit CRC polynomial is committed. When this bit is reset, the selected ECC polynomial is committed. This mode is selected when the DATA TRANSFER bit (bit 0) of the CONTROL FIELD is reset, and if either the WRITEGATE-ON bit code or the READGATE-ON bit code of the Writable Control Store (WCS) CONTROL FIELD is set.

9.3 C0H-DEH — COUNT FIELD (Read/Write) *(cont.)*

Bit 5 **COUNT/START SYNCHRONIZATION TIMER/SECONDARY COMPARE ENABLE/TWO INDEX TIMER:** This bit is used for four functions: (1) to specify the initial value of the Format Sequencer Byte Counter, (2) to reset and start the Synchronization Timer, (3) to enable the secondary comparison operation, and (4) to start the Two Index Count.

COUNT: In this mode, this bit is used for the initial value of the Format Sequencer Byte Counter for the execution of the Current Sequencer Word. This mode is selected when the DATA TRANSFER bit (bit 0 of the Writable Control Store (WCS) CONTROL FIELD) is set.

START SYNCHRONIZATION TIMER: In this mode, this bit is used to reset and start the Synchronization Timer. This counter is used to limit the amount of time that the Format Sequencer will wait for synchronization with the NRZ Read Data. The SYNCHRONIZATION BYTE-COUNT LIMIT (Register 70H) holds a limit for the counter. If the count limit is exhausted, the current read operation will be aborted (the Format Sequencer stopped) and the SYNCHRONIZATION TIME-OUT ERROR bit (Register 7AH, bit 4) will be set. This mode is selected when the READGATE-ON bit code (bit 5 reset and bit 6 set of the Writable Control Store (WCS) CONTROL FIELD) is set.

SECONDARY COMPARE ENABLE: In this mode, this bit is used to enable the secondary comparison operation. This mode is selected when the COMPARE ENABLE bit (bit 1 of the Writable Control Store (WCS) CONTROL FIELD) is set, and the DATA TRANSFER bit (bit 0 of the Writable Control Store (WCS) CONTROL FIELD) is not set.

START TWO INDEX COUNTER: In this mode, this bit is used to start the Two Index Count. This mode is selected when the DATA TRANSFER bit (bit 0 of the Writable Control Store (WCS) CONTROL FIELD) and the READGATE-ON bit code (bit 5 reset and bit 6 set of the Writable Control Store (WCS) CONTROL FIELD) are reset. If two Index pulses are detected after this circuit has been started then the Format Sequencer will be stopped.

Bit 6 **COUNT/PROCESS ECC:** This bit is used for two functions.

COUNT: In this mode, this bit is used for the initial value of the Format Sequencer Byte Counter for the execution of the Current Sequencer Word. This mode is selected when the DATA TRANSFER bit (bit 0 of the Writable Control Store (WCS) CONTROL FIELD) is set.

PROCESS ECC: When this bit is set, the Format Sequencer will process the current NRZ data as the ECC field. In a write operation, the generated remainder is appended to the outgoing NRZ data stream. In a read operation, the circuit is set up to evaluate the recomputed remainder for a zero syndrome. This mode is selected when the DATA TRANSFER bit (bit 0 of the Writable Control Store (WCS) CONTROL FIELD) is reset.

9.3 C0H-DEH — COUNT FIELD (Read/Write) *(cont.)*

Bit 7 **COUNT/PROCESS AM:** This bit is used for two functions.

COUNT: In this mode, this bit is used for the initial value of the Format Sequencer Byte Counter for the execution of the Current Sequencer Word. This mode is selected when the DATA TRANSFER bit (bit 0 of the Writable Control Store (WCS) CONTROL FIELD) is set.

PROCESS AM: When this bit is set, the AM ACTIVE bit (Register 79H, bit 1) will be set. In a write operation, this bit is also used to initialize the ECC circuitry. This mode is selected when the DATA TRANSFER bit (bit 0 of the Writable Control Store (WCS) CONTROL FIELD) is reset.

9.4 E0H-FEH — DATA/BRANCH FIELD (Read/Write)

Bits 0-7 This field has two functions.

In any mode, the DATA/BRANCH FIELD is used for data. This register is the source for all overhead bytes (bytes without the DATA TRANSFER bit (CONTROL FIELD, bit 0) set) of data used by the device during write operations. During read operations, it is one of the operands to the comparison logic. When the DATA TRANSFER bit (CONTROL FIELD, bit 0) is set with the WRITE GATE signal (pin 44) asserted, the source for write data will be the external buffer. When the SUPPRESS TRANSFER bit (Register 77H, bit 2) is set with the WRITE GATE signal (pin 44) asserted, the source for write data will be the contents of this register.

When the DATA/BRANCH FIELD ENABLE bit (Register 77H, bit 1) is set, bits 0-4 will be used as the branch address if a branch command is programmed and the condition is met.

NOTE: This option provides the Format Sequencer programmer with an extremely flexible branch addressing option. However, if a branch command is programmed in the same Format Sequencer word that uses the Writable Control Store (WCS) DATA/BRANCH FIELD then the contents of this field must be appropriate for both uses. This dual use is improbable, and the problem should be avoided.

10. SEQUENCER REGISTER DESCRIPTIONS

These registers contain the value of the currently executing Writable Control Store (WCS) word.

10.1 9FH — CURRENT SEQUENCER WORD — NEXT ADDRESS FIELD (Read/Write)

This register is set when the RST* signal (pin 40) is asserted low, or by a Sector Formatter Reset (Register 4FH, bit 0).

10.2 BFH — CURRENT SEQUENCER WORD — CONTROL FIELD (Read/Write)

This register is reset when the RST* signal (pin 40) is asserted low, or by a Sector Formatter Reset (Register 4FH, bit 0).

10.3 DFH — CURRENT SEQUENCER WORD — COUNT FIELD (Read/Write)

This register is reset when the RST* signal (pin 40) is asserted low, or by a Sector Formatter Reset (Register 4FH, bit 0).

10.4 FFH — CURRENT SEQUENCER WORD — DATA/BRANCH FIELD (Read/Write)

This register is reset when the RST* signal (pin 40) is asserted low, or by a Sector Formatter Reset (Register 4FH, bit 0).

11. ELECTRICAL SPECIFICATION

11.1 Absolute Maximum Ratings

Ambient temperature under bias	0° C to 70° C
Storage temperature	-65° C to 150° C
Voltage on any pin with respect to ground	GND -0.5 to VCC +0.5 Volts
Power dissipation	0.500 Watt
Power supply voltage	7 Volts

NOTE: Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

11.2 D.C. CHARACTERISTICS

Symbol	Parameter	MIN	MAX	Units	Conditions
V_{CC}	Power Supply Voltage	4.75	5.25	V	Operating
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	VCC + 0.5	V	
$V_{OL}^{1,3}$	Output Low Voltage		0.4	V	IOL = 2 mA
V_{OL}^{2}	Output Low Voltage		0.5	V	IOL = 48 mA
V_{OH}^{1}	Output High Voltage	2.4		V	IOH = -400 µA
V_{OH}^{2}	Output High Voltage	2.5		V	IOH = -400 µA
I_{CC}	Supply Current		50	mA	Operating
I_L	Input Leakage	-10	10	µA	0 < VIN < VCC
I/OL	I/O Leakage Current	-10	10	µA	0 < VIN < VCC
CIN	Input Capacitance		10	pf	
COUT	Output Capacitance		10	pf	

NOTES: 1) All output pins except for the SCSI bus signals.
2) All SCSI bus output or I/O signals.
3) IOL = 4 mA for the READ GATE signal (pin 43) and the WRITE GATE signal (pin 44).
4) All unused inputs must be tied to the inactive state to GND or VCC appropriately.
5) VOH2 = 2.5 MIN on IOH = -400 µA

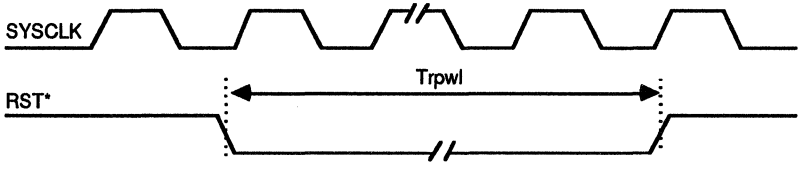
11.3 A.C. Characteristics

Unless otherwise specified the following timings are operating under the assumption that all non-SCSI outputs will drive one Schottky TTL load in parallel with 50 pF and all inputs are at TTL level. The MIN and MAX timings are conforming to the operating ranges of power supply voltage of 5V +/-5% and ambient temperature of 0° C to 70° C.

11.3.1 RESET Assertion Timing Parameters

Symbol	Parameter	MIN	MAX	Units
Trpwl	RST* pulse width low	500		ns

11.3.1.1 RESET Assertion Timing



11.3.2 Microcontroller Interface Timing Parameters

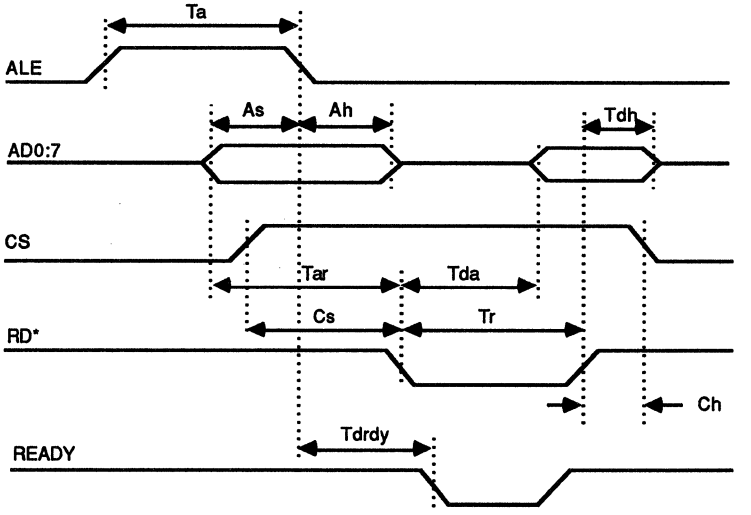
Symbol	Parameter	MIN	MAX	Units
Ta	ALE width	20		ns
Taw	Address valid to WR* ↓ or DS ↑	30		ns
Tar	Address valid to RD* ↓ or DS ↑	20		ns
Tw	WR* width	120		ns
Tr	RD* width	120		ns
As	Address valid to ALE ↓	5		ns
Ah	ALE ↓ to address invalid	12		ns
Cs	CS ↑ to RD*↓ WR*↓ or DS ↑	20		ns
Ch	RD* ↑ WR* ↑ or DS ↓ to CS ↓	5		ns
Wds	Write data valid to WR* ↑ or to DS ↓	55		ns
Wdh	WR* ↑ or DS ↓ to Write data invalid	10		ns
Tda	RD* ↓ or DS ↑ to Read data valid		100	ns
Tdh	RD* ↑ or DS ↓ to Read data invalid	10		ns
Tdz	RD* ↑ or DS ↓ to Read data undriven		50	ns
Tds	DS width	120		ns
Tdrdy	ALE ↓ to READY valid		40	ns
Tsrw	R/W* valid to DS ↑	30		ns
Thrw	DS ↓ to R/W* invalid	20		ns

NOTES: 1) ↑ indicates rising edge. ↓ indicates falling edge.

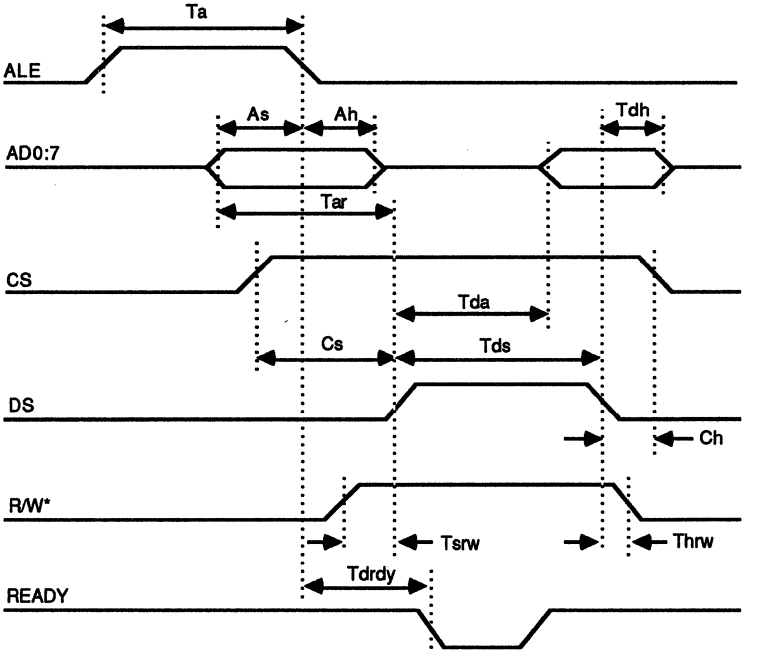
2) When the I/MC* signal (pin 24) is asserted high, the Intel bus control interface is selected. The timing diagram in Sections 11.3.2.1 and 11.3.2.3 depict a register read and write respectively with this interface selected.

3) When the I/MC* signal (pin 24) is deasserted low, the Motorola bus control interface is selected. The timing diagrams in Section 11.3.2.2 and 11.3.2.4 depict a register read and write respectively with this interface selected.

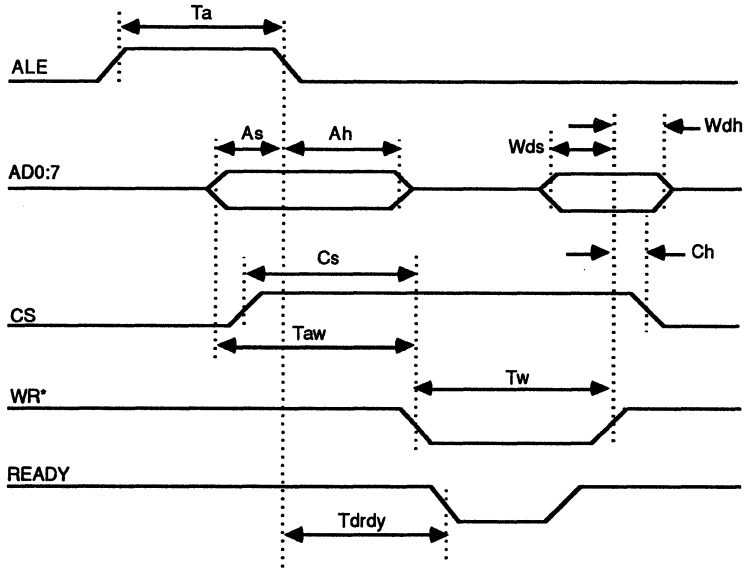
11.3.2.1 Register Read Operation in Intel Mode



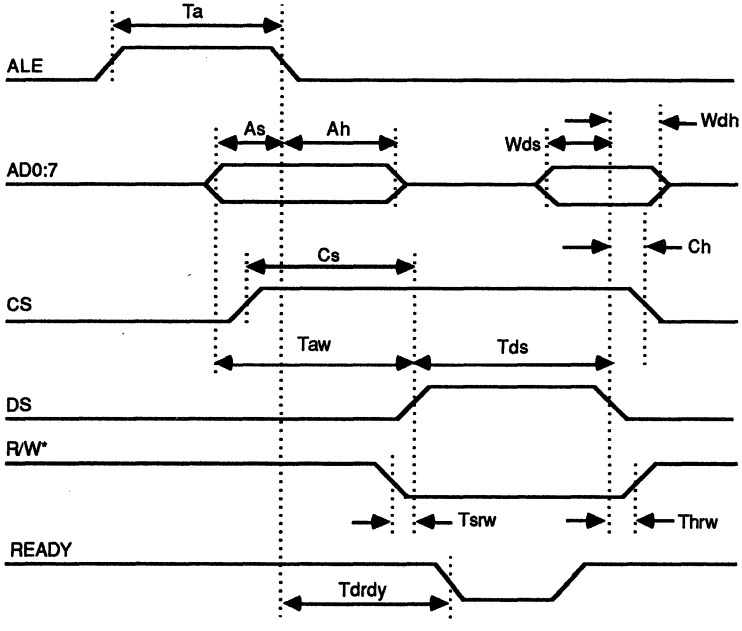
11.3.2.2 Register Read Operation in Motorola Mode



11.3.2.3 Register Write Operation in Intel Mode



11.3.2.4 Register Write Operation in Motorola Mode

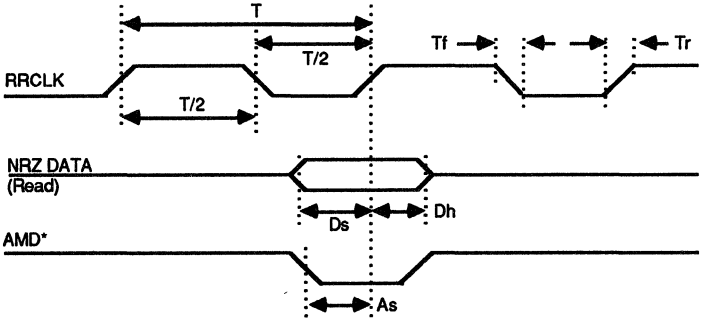


11.3.3 Disk Read/Write Timing Parameters

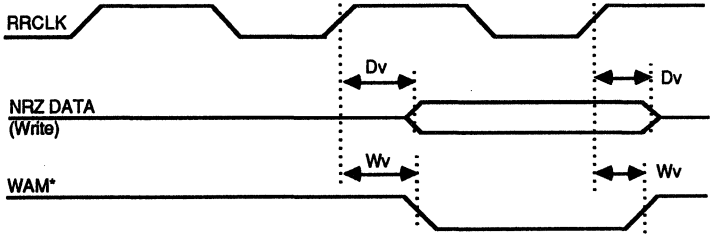
Symbol	Parameter	24 MHz MIN	24 MHz MAX	32 MHz MIN	32 MHz MAX	Units
T	RRCLK period	41		31		ns
T/2 (L)	RRCLK low at 0.8V	13		11		ns
T/2 (H)	RRCLK high at 2.0V	16		13		ns
Tr=Tf	RRCLK rise and fall time		5		4	ns
Ds	NRZ in valid to RRCLK ↑	8		8		ns
Dh	RRCLK ↑ to NRZ in invalid	5		5		ns
As†	AMD* valid to RRCLK ↑	10		10		ns
Dv	RRCLK ↑ to NRZ out	8	25	8	25	ns
Wv†	RRCLK ↑ to WAM* out	8	25	8	25	ns

NOTES: ↑ indicates rising edge.
† indicates that these specifications are only applicable in the Soft Sector Mode.

11.3.3.1 Disk Read Timing



11.3.3.2 Disk Write Timing



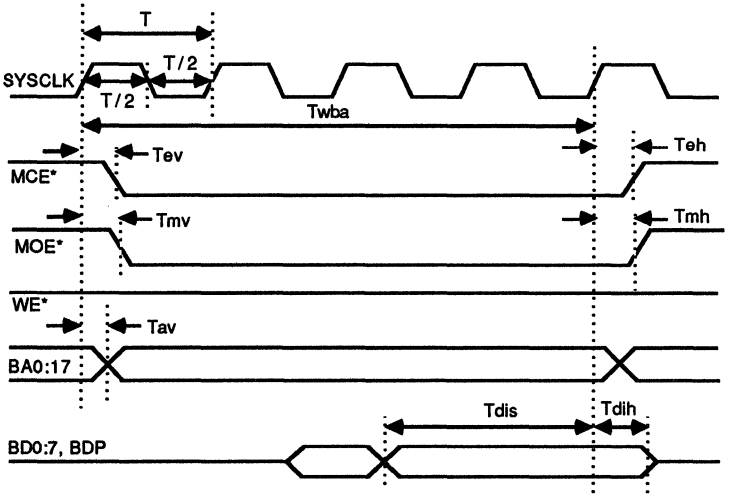
11.3.4 Buffer Memory Read/Write Timing Parameters

Symbol	Parameter	MIN	MAX	Units
T	SYSCLK period	33		ns
T/2	SYSCLK high/low time	14		ns
Tav	SYSCLK ↑ to address valid		30	ns
Tev	SYSCLK ↑ TO MCE* ↓		30	ns
Teh	SYSCLK ↑ TO MCE* ↑		30	ns
Tmv1	SYSCLK ↑ to MOE* ↓ in SRAM		30	ns
Tmh1	SYSCLK ↑ to MOE* ↑ in SRAM		30	ns
Tdov1	SYSCLK ↓ to data out valid in SRAM		30	ns
Tdoh1	SYSCLK ↑ to data out invalid in SRAM	0		ns
Tdis1	Data in valid to SYSCLK ↓ in SRAM	5		ns
Tdih1	SYSCLK ↑ to data in invalid in SRAM	20		ns
Tmv2	SYSCLK ↓ to MOE* ↓ in DRAM		30	ns
Tmh2	SYSCLK ↓ to MOE* ↑ in DRAM		30	ns
Tdov2	SYSCLK ↑ to data out valid in DRAM		33	ns
Tdoh2	SYSCLK ↑ to data out invalid in DRAM	0		ns
Tdis2	Data in valid to SYSCLK ↓ in DRAM	5		ns
Tdih2	SYSCLK ↓ to data in invalid in DRAM	20		ns
Twv	SYSCLK ↓ to WE* ↓		30	ns
Twh	SYSCLK ↓ to WE* ↑		30	ns
Trv	SYSCLK ↓ to RAS* ↓		30	ns
Trh	SYSCLK ↓ to RAS* ↑		30	ns
Trav	SYSCLK ↑ to row address valid		30	ns
Trah	SYSCLK ↑ to row address invalid		30	ns
Tcv	SYSCLK ↓ to CAS* ↓		30	ns
Tch	SYSCLK ↓ to CAS* ↑		30	ns
Tcav	SYSCLK ↑ to column address valid		30	ns
Tcah	CAS* ↓ to column address invalid	(2)		

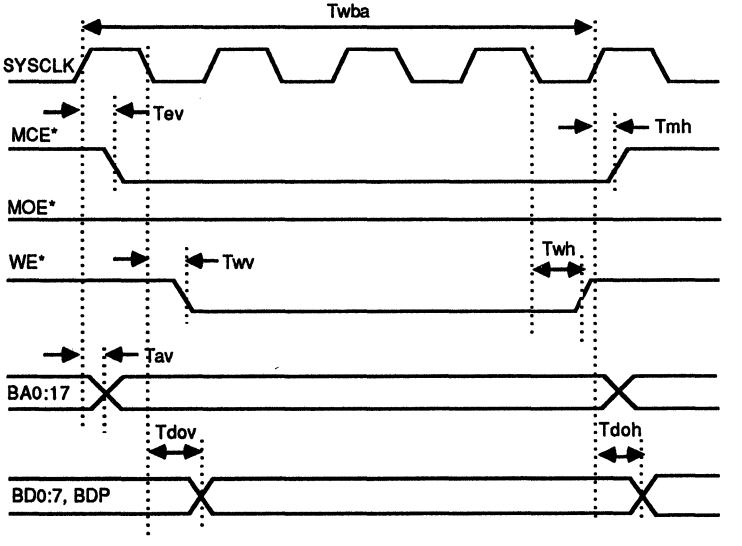
NOTES: 1) ↑ indicates rising edge. ↓ indicates falling edge.

2) Column address remains valid throughout CAS* low time.

11.3.4.1 SRAM Read Timing

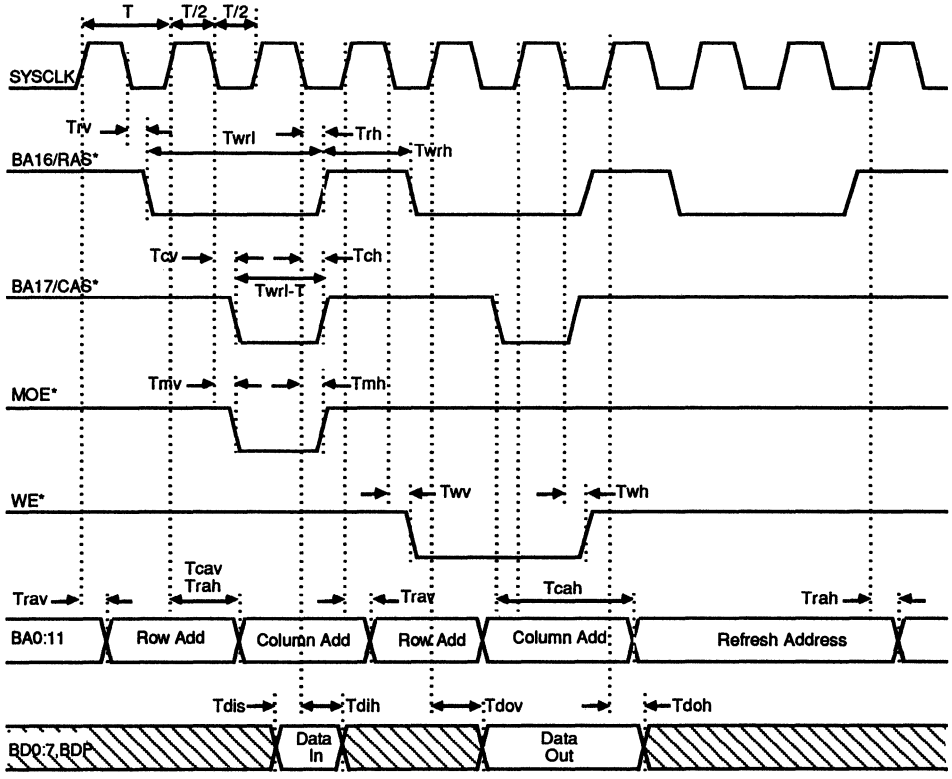


11.3.4.2 SRAM Write Timing



NOTE: Twba is a functional parameter that gives the duration of one RAM data buffer access cycle in SYSCLK periods. The value is programmed in bits 1-0 of Register 54H. These examples show Twba = 4T.

11.3.4.3 Normal DRAM Read, Write, and Refresh Cycles



NOTES:

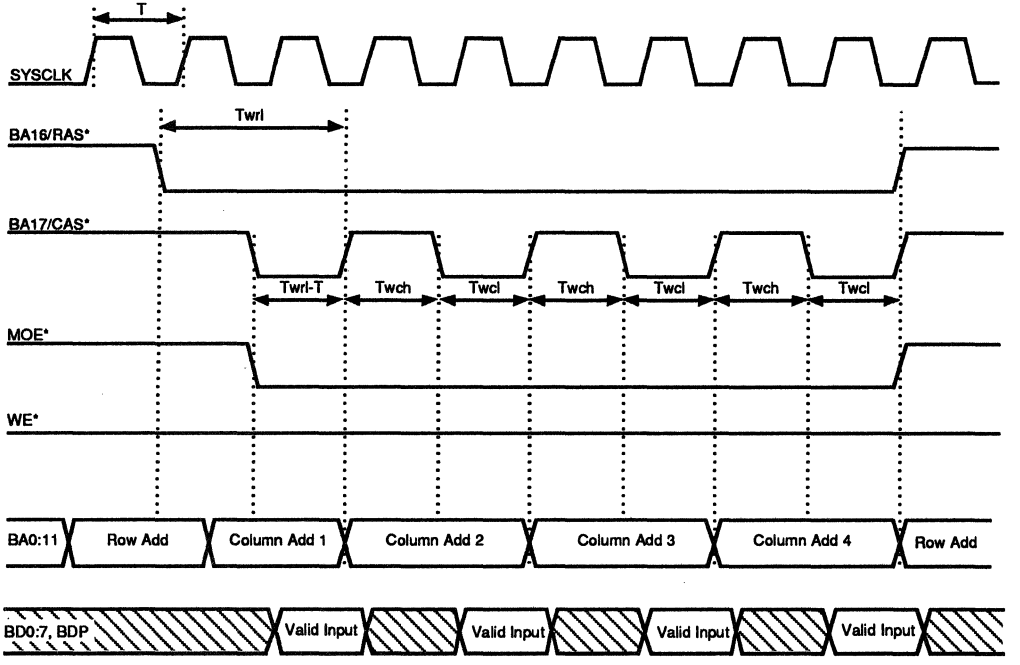
1) Twrl and Twrh are functional parameters that specify the duration of the BA16/RAS* signal (pin 14) width low and the BA16/RAS* signal (pin 14) width high (in SYSCLK periods) for a normal RAM data buffer access cycle. These values are programmed in bits 3 - 0 of Register 54H. This example shows values of Twrl = 2 and Twrh = 1.

2) The BA17/CAS* signal (pin 5) is asserted low one SYSCLK cycle after the BA16/RAS* signal (pin 14) is asserted low. The BA17/CAS* signal (pin 5) is deasserted high when the BA16/RAS* signal (pin 14) is deasserted high.

3) The MOE* signal (pin 15) is asserted low and deasserted high along with the BA17/CAS* signal (pin 5) in a read access. The MOE* signal (pin 15) is deasserted high throughout write and refresh cycles.

4) A write cycle is always an early write cycle. The WE* signal (pin 16) is asserted low and deasserted high along with the BA16/RAS* signal (pin 14). Data out is valid by the falling (leading) edge of the BA17/CAS* signal (pin 5) and is held valid while the BA17/CAS* signal (pin 5) is asserted low.

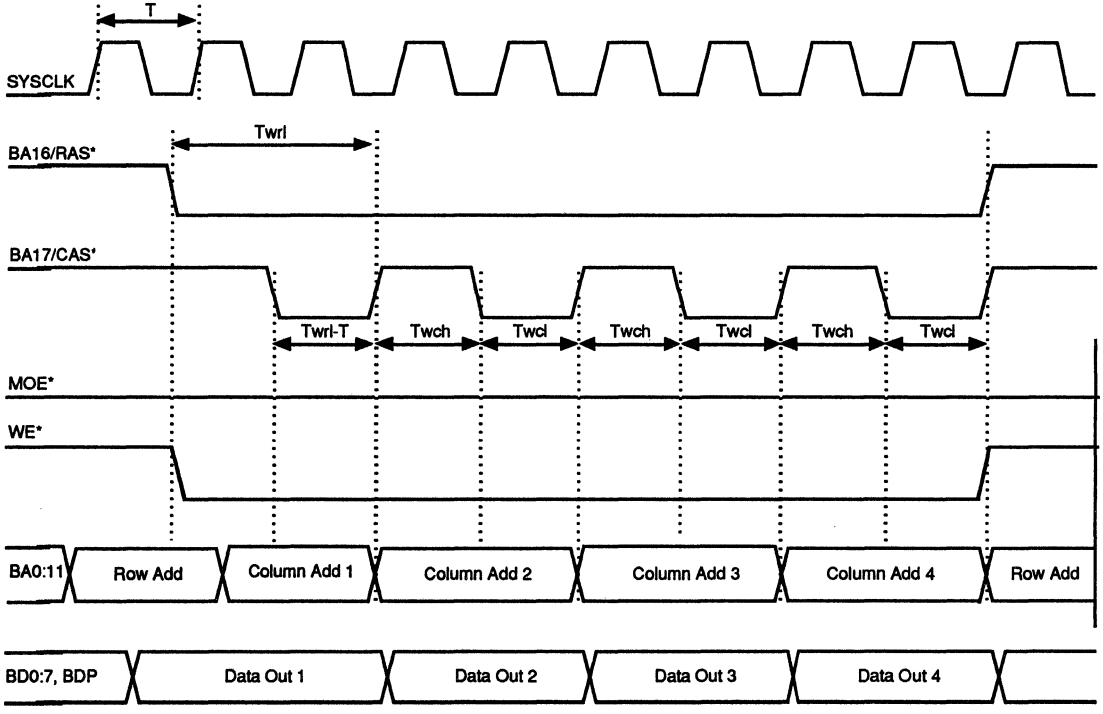
11.3.4.4 Page Mode DRAM Read Cycle



NOTES: 1) Twrl = 2, Twrh = 1, Twcl = 1, Twch = 1.

2) This is only a functional timing diagram and does not depict AC-tested parameters.

11.3.4.5 Page Mode DRAM Write Cycle



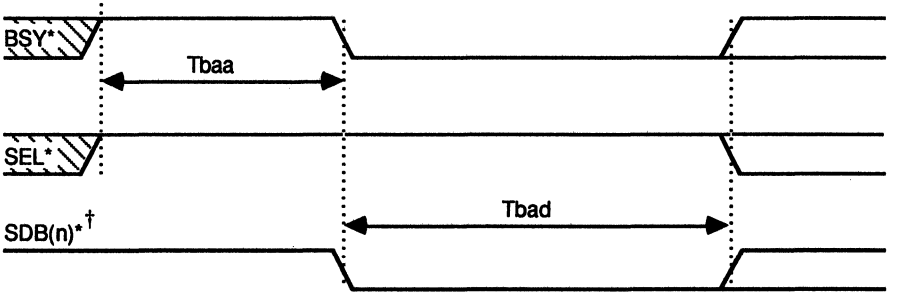
NOTES: 1) Twrl = 2, Twrh = 1, Twcl = 1, Twch = 1.
2) This is only a functional timing diagram and does not depict AC-tested parameters.

11.3.5 SCSI Arbitration Timing Parameters

Symbol	Parameter	MIN	MAX	Units
Tbaa	BSY* and SDB(n)* assertion delay from bus free detected		7Ts + 40††	ns
Tbad	Bus abritration assertion or deassertion delay		12Ts + 40††	ns

NOTE: †† Ts is the SCSI clock period, a function of SYSCLK as defined in Register 44H/64H, bits 5-7.

11.3.5.1 SCSI Arbitration Timing



NOTES: † The CL-SH351 SCSI ID signal asserted on the SCSI data bus for arbitration.
This is only a functional timing diagram and does not depict AC-tested parameters.

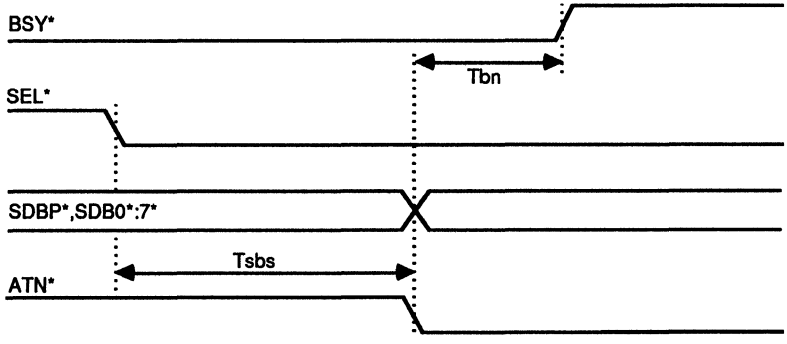
11.3.6 SCSI Select/Reselect Timing

11.3.6.1 SCSI Selection Timing Parameters

Symbol	Parameter	MIN	MAX	Units
Tsbs	SCSI bus SELECTION data assertion		6Ts + 40†	ns
Tbn	SCSI BSY* deasserted high		2Ts + 40†	ns

NOTE: † Ts is the SCSI clock period, a function of SYSCLK as defined in Register 44H/64H, bits 5-7.

11.3.6.2 SCSI Selection Timing



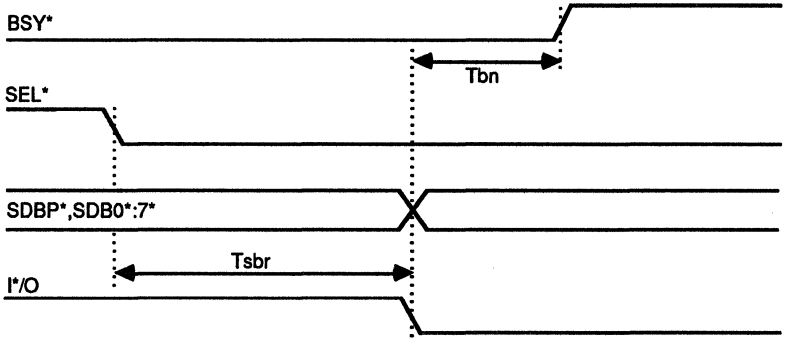
NOTE: This is only a functional timing diagram and does not depict AC-tested parameters.

11.3.6.3 SCSI Reselection Timing Parameters

Symbol	Parameter	MIN	MAX	Units
Tsbr	SCSI bus RESELECTION data assertion		6Ts + 40†	ns
Tbn	SCSI BSY* deasserted high		2Ts + 40†	ns

NOTE: † Ts is the SCSI clock period, a function of SYSCLK as defined in Register 44H/64H, bits 5-7.

11.3.6.4 SCSI Reselection Timing



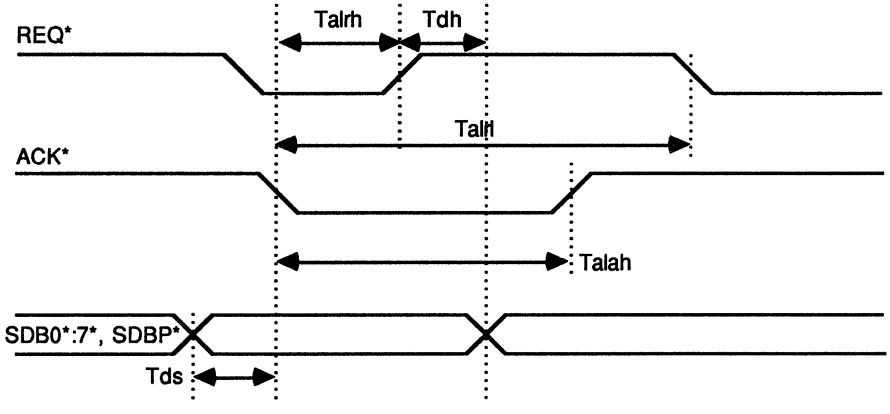
NOTE: This is only a functional timing diagram and does not depict AC-tested parameters.

11.3.7 Target Mode Asynchronous Data Transfers

11.3.7.1 Data Out Phase Timing Parameters

Symbol	Parameter	MIN	MAX	Units
Talrh	ACK* ↓ to REQ* ↑		55	ns
Talrl	ACK* ↓ to REQ* ↓		2T+55 if Talah ≤ 2T Talah+55 if Talah > 2T	ns ns
Tds	SDB0*:7*, SDBP* setup to ACK* ↓	40		ns
Tdh	SDB0*:7*, SDBP* hold from REQ* ↑	0		ns

11.3.7.2 Data Out Phase Timing

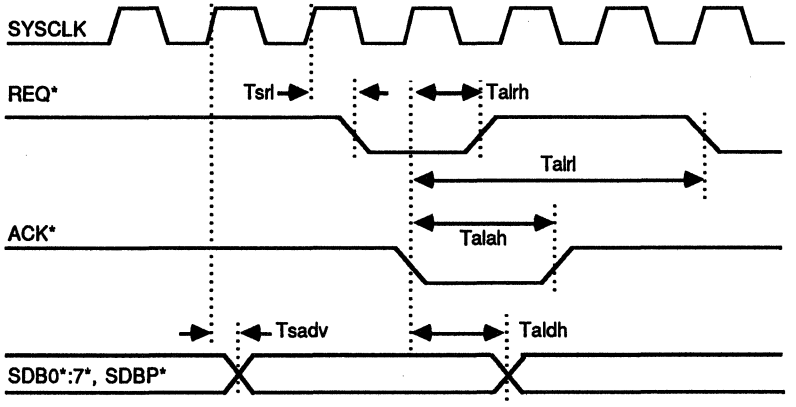


11.3.7.3 Data In Phase Timing Parameters

Symbol	Parameter	MIN	MAX	Units
Talrh	ACK* ↓ to REQ* ↑		55	ns
Talrl	ACK* ↓ to REQ* ↓		3T (4T)† + 55 if Talah ≤ 3T (4T) Talah + 55 if Talah > 3T (4T)	ns ns
Tsrl	SYSCLK ↑ to REQ* ↓		70	ns
Tsadv	SYSCLK ↑ to SDB0*:7*, SDBP* valid delay		60	ns
Taldh	SDB0*:7*, SDBP* hold from ACK* ↓	T-10		ns

NOTE: † This time is 3T if the SCSI DATA SET UP SELECT bit (Register 51H, bit 5) is reset, or the time is 4T if the SCSI DATA SET UP SELECT bit is set.

11.3.7.4 Data In Phase Timing

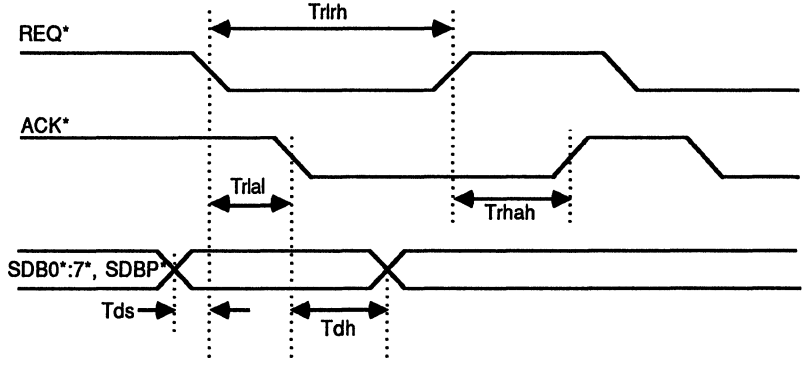


11.3.8 Initiator Mode Asynchronous Data Transfers

11.3.8.1 Data In Phase Timing Parameters

Symbol	Parameter	MIN	MAX	Units
Trlal	REQ* ↓ to ACK* ↓		55	ns
Trhah	REQ* ↑ to ACK* ↑		2T + 55 if Trlrh < 2T Trlrh + 55 if Trlrh ≥ 2T	ns ns
Tds	SDB0*:7*, SDBP* setup to REQ* ↓	40		ns
Tdh	SDB0*:7*, SDBP* hold from ACK* ↓	0		ns

11.3.8.2 Data In Phase Timing

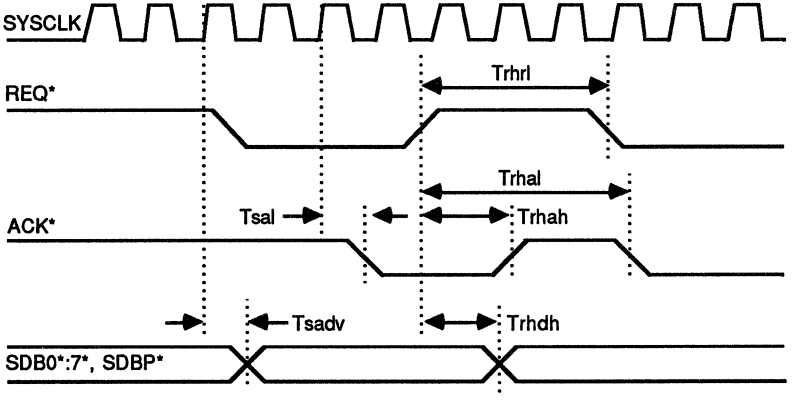


11.3.8.3 Data Out Phase Timing Parameters

Symbol	Parameter	MIN	MAX	Units
Trhah	REQ* ↑ to ACK* ↑		55	ns
Trhal	REQ* ↑ to ACK* ↓		3T (4T)† + 55 if Trhrl ≤ 3T Trhrl + 55 if Trhrl > 3T	ns ns
Tsal	SYSCLK ↑ to ACK* ↓		75	ns
Tsadv	SYSCLK ↑ to SDB0*:7*, SDBP* valid delay		55	ns
Trhdh	SDB0*:7*, SDBP* hold from REQ* ↑	0		ns

NOTE: † This time is 3T if the SCSI DATA SET UP SELECT bit (Register 51H, bit 5) is reset, or the time is 4T if the SCSI DATA SET UP SELECT bit is set.

11.3.8.4 Data Out Phase Timing

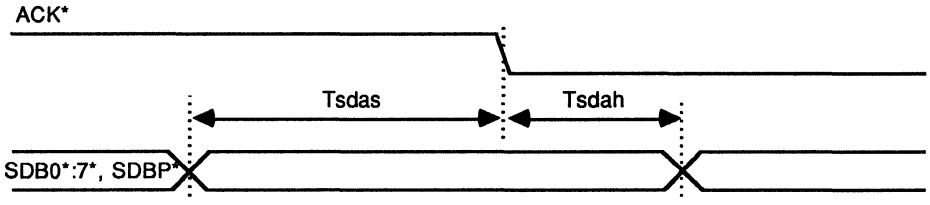


11.3.9 Target Mode Synchronous Data Transfers

11.3.9.1 Data Out Phase Timing Parameters

Symbol	Parameter	MIN	MAX	Units
Tsdas	SDB0*:7*, SDBP* set-up time to ACK* ↓	40		ns
Tsdah	ACK* ↓ to SDB0*:7*, SDBP* hold time	100		ns

11.3.9.2 Data Out Phase Timing



11.3.9.3 Data In Phase Timing Parameters

Symbol	Parameter	MIN	MAX	Units
Tsrrf	SYSCLK ↑ to REQ* ↓ delay		45	ns
Tsrrr	SYSCLK ↑ to REQ* ↑ delay		45	ns
Tsfrr	SYSCLK ↓ to REQ* ↑ delay		35	ns
Tsdv	SYSCLK ↑ to SDB0*:7*, SDBP* valid delay		55	ns
Tsfrf	SYSCLK ↑ to REQ* ↓ delay		35	ns

NOTE: For the Data In Phase, the SCSI data bus set-up and hold times in Synchronous Transfer Mode are dependent on the SYSCLK period T, in ns, and the value P which sets the synchronous transfer rate in Register 43H/63H, bits 4-7.

If P is chosen as an even number then:

SDB0*:7*, SDBP* set-up time to REQ* ↓ = $\frac{P}{2}$ • (T-15)

SDB0*:7*, SDBP* hold time from REQ* ↓ = $\frac{P}{2}$ • (T-5).

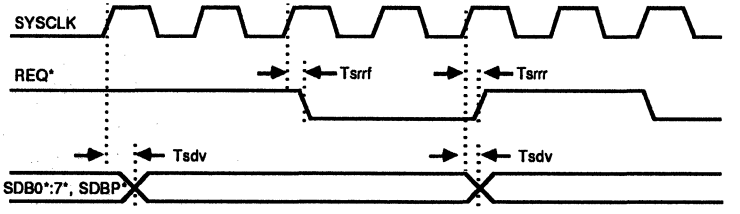
If P is chosen as an odd number then:

SDB0*:7*, SDBP* set-up time to REQ* ↓ = $\frac{P-1}{2}$ • (T-15)

SDB0*:7*, SDBP* hold time from REQ* ↓ = $\frac{P+1}{2}$ • (T-5).

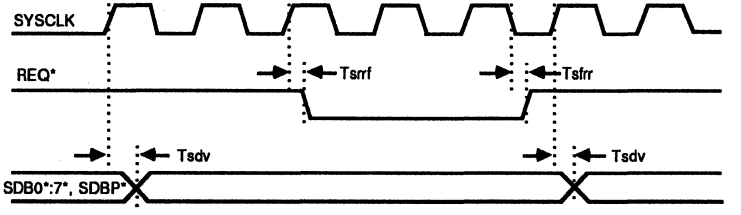
11.3.9.4 Data In Phase Timing

Even Number of SYSCLK Cycles per SCSI Synchronous Transfer Period

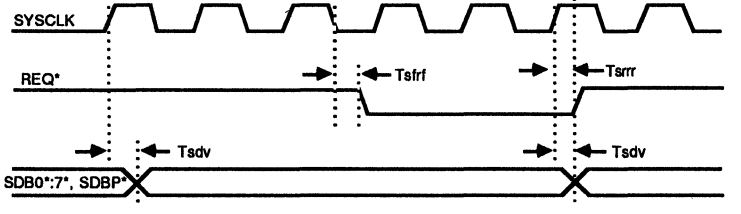


Odd Number of SYSCLK Cycles per SCSI Synchronous Transfer Period

a. SYNC SCSI DATA SET UP SELECT bit (Register 51H, bit 6) is reset.



b. SYNC SCSI DATA SET UP SELECT bit (Register 51H, bit 6) is set.

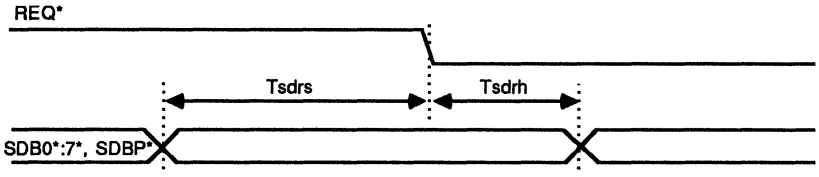


11.3.10 Initiator Mode Synchronous Data Transfers

11.3.10.1 Data In Phase Timing Parameters

Symbol	Parameter	MIN	MAX	Units
Tsdrs	SDB0*:7*, SDBP* set-up time to REQ* ↓	40		ns
Tsdrh	REQ* ↓ to SDB0*:7*, SDBP* hold time	100		ns

11.3.10.2 Data In Phase Timing



11.3.10.3 Data Out Phase Timing Parameters

Symbol	Parameter	MIN	MAX	Units
Tsraf	SYSCLK ↑ to ACK* ↓ delay		45	ns
Tsrar	SYSCLK ↑ to ACK* ↑ delay		45	ns
Tsfar	SYSCLK ↓ to ACK* ↑ delay		35	ns
Tsdv	SYSCLK ↑ to SDB0*:7*, SDBP* valid delay		55	ns
Tsfaf	SYSCLK ↓ to ACK* ↓		35	ns

NOTE: For the Data Out Phase, the SCSI data bus set-up and hold times in Synchronous Transfer Mode are dependent on the SYSCLK period T, in ns, and the value P which sets the synchronous transfer rate in Register 43H/63H, bits 4-7.

If P is chosen as an even number then:
SDB0*:7*, SDBP* set-up time to REQ* ↓ = $\frac{P}{2}$ • (T-15)

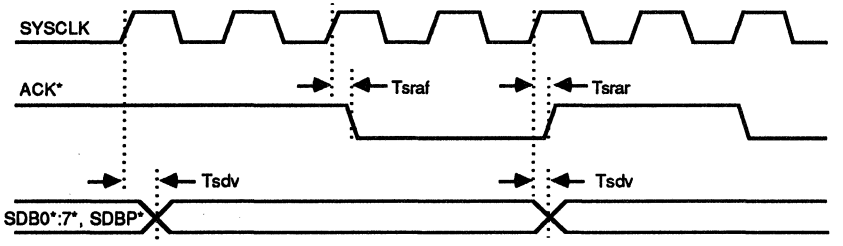
SDB0*:7*, SDBP* hold time from REQ* ↓ = $\frac{P}{2}$ • (T-5).

If P is chosen as an odd number then:
SDB0*:7*, SDBP* set-up time to REQ* ↓ = $\frac{P-1}{2}$ • (T-15)

SDB0*:7*, SDBP* hold time from REQ* ↓ = $\frac{P+1}{2}$ • (T-5).

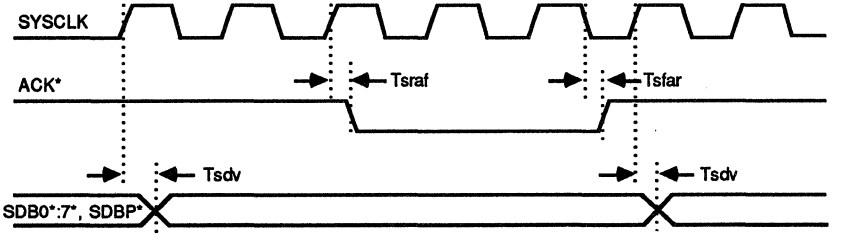
11.3.10.4 Data Out Phase Timing

Even Number of SYSCLK Cycles per SCSI Synchronous Transfer Period

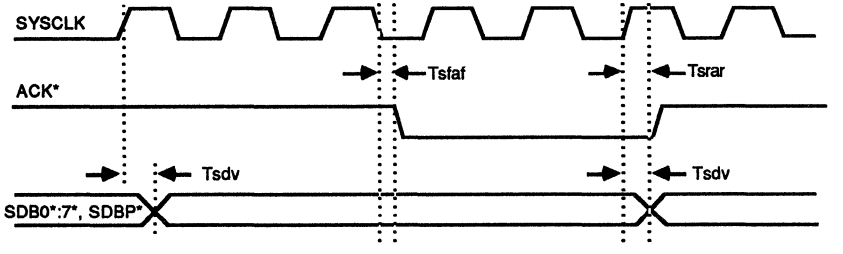


Odd Number of SYSCLK Cycles per SCSI Synchronous Transfer Period

a. SYNC SCSI DATA SET UP SELECT bit (Register 51H, bit 6) is reset.

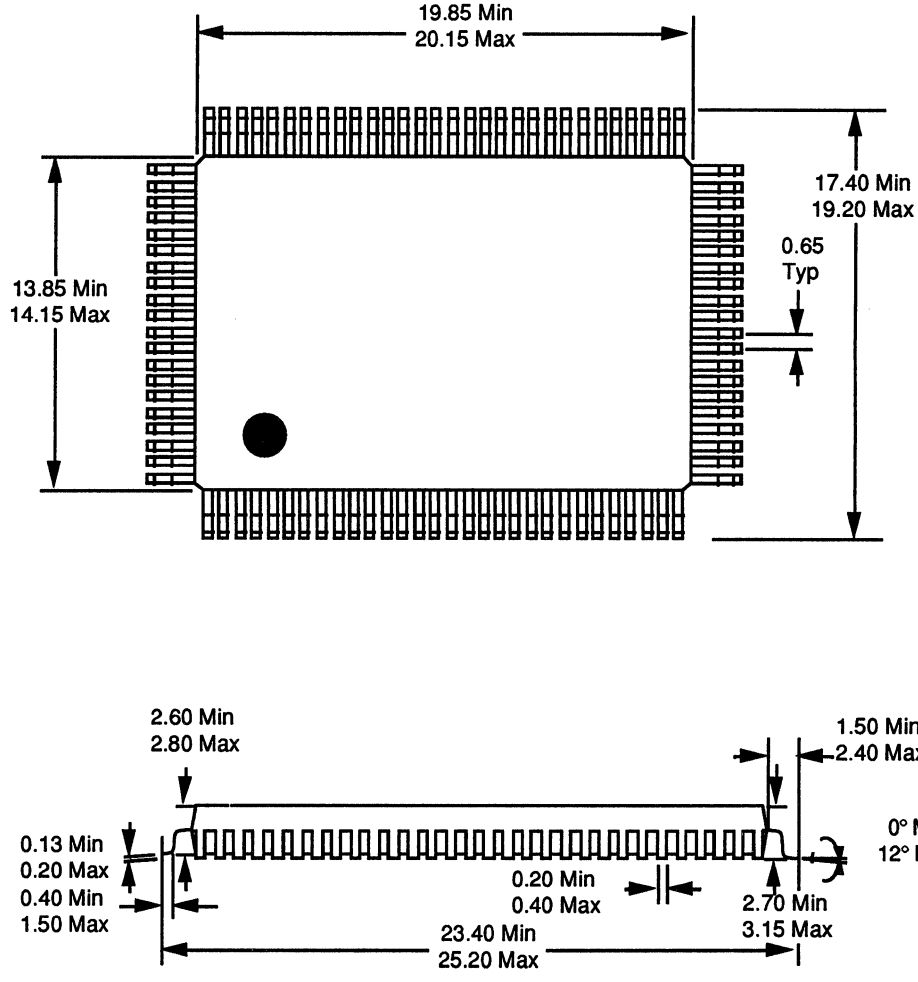


b. SYNC SCSI DATA SET UP SELECT bit (Register 51H, bit 6) is set.



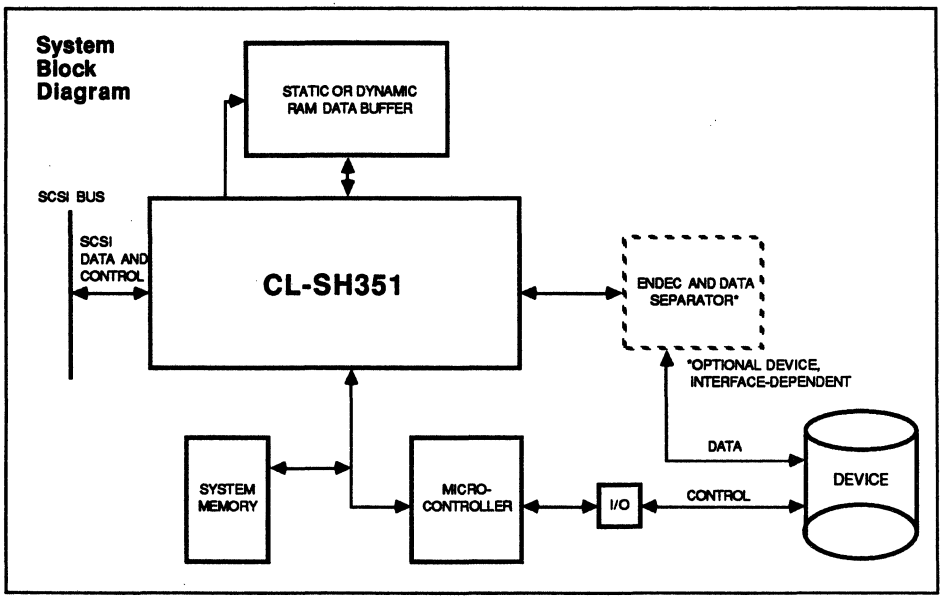
12. SAMPLE PACKAGE

12.1 100-Pin Quad Flat Pack (QFP) Sample Package



NOTE: Dimensions for the QFP package are in millimeters.

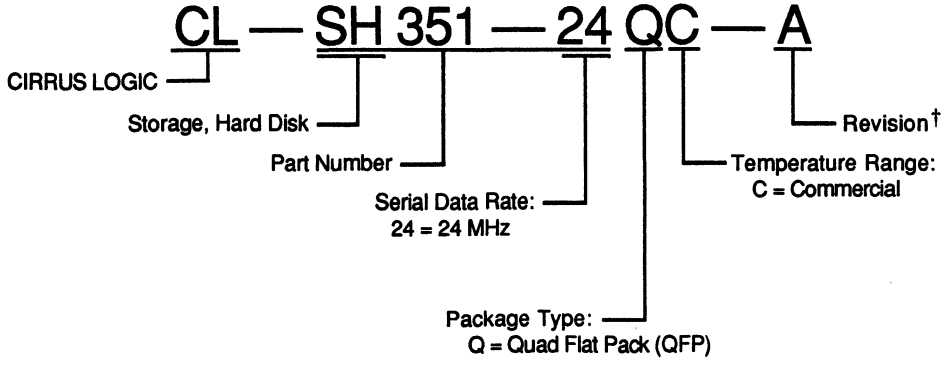
13. TYPICAL APPLICATION



Single-Ended Direct SCSI System Implementation

14. ORDERING INFORMATION

Cirrus Logic, Inc., Numbering Guide



† Contact Cirrus Logic, Inc., for up-to-date information on revisions.

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† U.S. Patent No. 4,293,783

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