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## PRODUCT GUIDE

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## FOREWORD

This book is a guide to the broadest range of electronic components and devices needed by designers of instrumentation and control systems which accept, analyze, process, convert, transmit, display and react to electronic signals. It contains not only product performance data, but also information designed to help you simplify the choice of the right product solution for your application.

## GUIDE TO THE GUIDE

There are a number of ways to use this publication depending upon your particular product needs, and knowledge of Analog Devices' product line. Generally, you can access information by:

- product number, using the model number indices printed on the inside front cover and page 272.
- product category (i.e. "Multipliers/Dividers") by using the product classification index on page 270.
- area of interest using the table of contents printed here.

Please note also that new products and improvements are featured beginning on page 4 , and are further highlighted throughout this PRODUCT GUIDE by color indication in the page margin and tables.
If you require additional information or assistance beyond that provided in this PRODUCT GUIDE, do not hesitate to contact our factory or field sales engineers, directly. Information request cards are also attached for your convenience.

January 1975

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The following are capsule descriptions of the products introduced by Analog Devices during the past year and scheduled for formal introduction during the next couple of months. In addition to new products, this selection includes brief descriptions of product improvements and product price changes. Additional information on these products can be found on the pages noted, except those entries indicated as "advance information." Unless otherwise stated, these products are currently available.

## LINEAR INTEGRATED CIRCUITS



## BIPOLAR \& FET's

INTEGRATED CIRCUIT 12-BIT D/A CONVERTER (Page 217
AD562: The AD562 is the first I.C. D/A converter with true 12-bit accuracy. Active laser trimming of thin film resistors combined with 12 precision, bipolar switches, results in a converter with $1 / 4$ LSB error at $+25^{\circ} \mathrm{C}$ and complete monotonicity over the full specified operating range.
Requiring only an external op amp and reference to complete the DAC function, the AD562 is recommended for all 12-bit D/A converter applications requiring high accuracy, small size and low cost. The AD562K is specified from $0^{\circ}$ to $+70^{\circ} \mathrm{C}$, the " A " from $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ and the " S " over the full military temperature range $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$. All versions are available in a hermetically-sealed, 24 pin DIP.

## LOW COST FET-INPUT OP AMP (Page 186)

AD540: The AD540J, AD540K and AD540S are the lowest priced, high performance I.C. FET-input operational amplifiers available which provide the user with low bias currents, high overall performance and accurately specified performance. The devices achieve a maximum bias current of 25 pA , minimum gain of 50,000, CMRR of 70 dB and a slew rate of $6 \mathrm{~V} / \mu \mathrm{sec}$.

LOW NOISE FET-INPUT OP AMP (Page 185)
AD5 14: The AD514J, AD514K, AD514L and AD514S are low noise, high accuracy FET-input amplifiers which have been designed and fully tested for low noise applications such as EKG amplifiers, pH electrodes and long term integrators. The devices offer noise voltage as low as $5 \mu \mathrm{~V}$ (p-p) max, ( 0.1 to 10 Hz ), bias currents as low as 10 pA and offset voltage as low as 20 mV .

## LOW DRIFT VOLTAGE REFERENCE (Page 216)

AD580: The AD580J, AD580K and AD580S are three-terminal, low cost, temperature compensated, bandgap voltage reference circuits which provide a fixed 2.5 V output voltage for inputs between 4.5 and 30 V . Offering a clear advantage over Zener techniques, the AD5 80 provides a temperature stability of better than $40 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ and long term stability of better than $250 \mu \mathrm{~V}$.

## HIGH SPEED FET-INPUT OP AMP (Page 203)

AD528: The AD528J, AD528K and AD528S are high speed precision FET-input operational amplifiers combining the advantages of very high slew rate and wide bandwidth with the ultra low input currents only available with FET-input designs. The devices are internally compensated for unity gain applications with a $60^{\circ}$ phase margin to insure stability, a minimum

unity gain slew rate of $50 \mathrm{~V} / \mu \mathrm{sec}$, a typical bandwidth of 10 MHz and laser-trimmed offset voltage down to 1 mV max.

LOW COST I.C. MULTIPLIER (Page 212)
AD533: The AD533J, AD533K, AD533L and AD533S are low cost I.C. multipliers, dividers, squarers, square rooters comprised of a transconductance multiplying element, stable reference and output amplifier on a monolithic silicon chip. With a basic transfer function of XY/10 and accuracy down to $0.5 \%$, the AD533 is recommended for many computational applications, such as frequency discrimination, rms computation and peak detection, where low cost is a factor.

MONOLITHIC INSTRUMENTATION AMPLIFIER (Page 196) AD521: The AD521J, AD521K and AD521S are true instrumentation amplifiers in I.C. form. Differential inputs and high CMRR make the AD521 well suited in applications where noise and large common mode signals are present. Full operation at gains from 0.1 to 1000 is obtained with the addition of only two external resistors.

## CMOS

## MONOLITHIC CMOS SWITCHES (Page 226)

AD7510 Series: A complete line of CMOS switches is now being offered, which can perform a myriad of switching functions that can be CMOS, TTL, or DTL controlled. All switching functions offer extremely low power dissipation (typically $30 \mu \mathrm{~W}$ ), low "ON" resistance, and moderate to fast switching speeds.
The AD7510/AD7511 features four independent CMOS switches (the AD7511 offers inverted control logic). The AD7512 provides a dual SPDT function. The AD7513 is a dual SPST plug-in replacement for the DG200. The AD7516 is an improved second source of the CD4016A quad SPST and the AD7519 offers a quad SPDT current steering function for D/A converters, which requires fast switching speeds.

## MONOLITHIC CMOS MULTIPLEXERS (Page 224)

AD7501 Series: The product line includes two 8-channel analog multiplexers, AD7501 and AD7503. The AD7503 offers inverted " $\mathrm{E}_{\mathrm{N}}$ " logic for specific applications.
The AD7502 is a 4 -channel differential multiplexer to handle applications requiring good common-mode-rejection. The AD7506, 16-channel multiplexer, and the AD7507, 8-channel differential multiplexer, are replacements for the DG506 and DG507.
The multiplexer product line features CMOS, DTL, and TTL logic control compatibility, binary address control, low "ON" resistance, and low power dissipation ( $30 \mu \mathrm{~W}$ for the AD7501/ $7502 / 7503$, and 1.5 mW for the AD7506/7507, typically).

MONOLITHIC CMOS D/A CONVERTERS (Page 228)
AD7520 Series: Industry's first CMOS monolithic D/A converter, the AD7520, features 8, 9, and 10 bits of linearity, 2 ppm of $\mathrm{FSR} /{ }^{\circ} \mathrm{C}$ maximum nonlinearity TEMPCO, fast current settling time, and low power dissipation of typically 20 mW . TTL, DTL, and CMOS digital control compatibility with a wide +5 V to +15 V operating voltage supply range.
The AD7521 offers all the features of the AD7520, but provides for 12 bits of resolution with a 10-bit linearity for specific applications, such as digitally controlled filters.

MONOLITHIC CMOS A/D CONVERTERS (ADVANCE INFORMATION)
AD7570 Series: The AD7570 is a CMOS monolithic successive approximation 10-bit A/D converter. The AD7570 features "tri-state" parallel outputs and a synchronized serial output. The control circuitry required to directly interface with an 8-bit microprocessor has been included on-chip for ease of application. An internal clock is available, providing for total conversions in 12 microseconds.
Additional attractive features will be an 8 -bit short cycle input, external synchronization, and low power dissipation. The AD7570 will be available in a 28 -pin DIL package. Availability: December, 1974.

## THIN FILM RESISTORS

## PRECISION RESISTOR NETWORKS

Thin Film Ladder Networks (Page 240)
The AD1850-1856 series are precision ladder networks designed to provide a high degree of accuracy for operation over limited temperature ranges, with guaranteed accuracies specified at $+25^{\circ} \mathrm{C}$. This series complements the present AD850-856 series widely used in wide temperature range applications.
General Purpose Resistor Networks (Page 236)
The AD1800-1842 series presented here is the industry's most complete standard precision thin film product line consisting of over 150 variations such as: 5 decade dividers, 10 segment binary dividers, summing networks ( 3 products) and others. All are available in standard housings, with thin film performance, competitively priced with their discrete counterparts.
Custom Resistor Networks (Page 234)
Analog Devices' thin film capabilities are available to serve your custom network needs with dedicated products designed to your specifications, from simple variations of our standard products to completely innovative concepts. Contact us before proceeding with discretes.

## THIN FILM HYBRID COMPONENTS

Cbip Resistor Networks (Page 232)
In addition to the chip versions of all of our standard products, our custom service for user designed chip networks allows you enormous design flexibility for chip functions sized from . $025^{\prime \prime}$ to $3.5^{\prime \prime}$ square with performance identical to our packaged functions.

Thin Film Coated Substrates (Page 230)
For those users that have the facilities for custom hybrid production, our complete line of $2 \& 3$ film 50 to 500 ohm/square products sized to $3.5^{\prime \prime}$ square provides a sizeable primary or secondary coated substrate source. Special products can be fabricated upon request.

## HIGH SPEED A/D (Page 98)

ADC1109, 10 BITS IN $4 \mu$ s: A high speed A/D converter packaged in a small $2^{\prime \prime} \times 3^{\prime \prime} \times 0.4^{\prime \prime}(51 \times 76 \times 10 \mathrm{~mm}$ ) module. It uses the successive approximations technique to perform complete 10 bit conversions in $4 \mu \mathrm{~s}$ ( $\max$ ) with a non-linearity error of less than $\pm 1 / 2$ LSB.


The ADC1109 accepts either unipolar or bipolar inputs and produces natural binary, offset binary, or two's complement coded outputs. A true serial output is also provided. Performance specifications include $\pm 30 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ gain TC and no missing codes over the entire 0 to $+70^{\circ} \mathrm{C}$ operating range.

HIGH PERFORMANCE A/D (Page 96)
ADC1105, DUAL SLOPE A/D USES EXTERNAL COUNTERS: A dual slope A/D converter which uses external counters and registers to produce any coding or counting scheme with resolutions up to $\mathbf{1 : 2 0 , 0 0 0}$. Its versatility is especially useful in instrumentation applications where it is desired to have outputs scaled directly in terms of engineering or physical units.
Two versions are available: The ADC1105J with $0.1 \%$ and the ADC1105K with $0.01 \%$ relative accuracy. Both versions of this $2^{\prime \prime} \times 4^{\prime \prime} \times 0.6^{\prime \prime}(51 \times 102 \times 16 \mathrm{~mm}$ ) module feature ratiometric capability and a choice of input voltage ranges. The ADC1105 is also available in a card mounted form factor.

## GENERAL PURPOSE D/A (Page 82)

DAC1118, LOW COST 12 BIT D/A WITH REGISTER: A 12 bit D/A which includes an input register and a versatile output amplifier for only $\$ 80$ in hundreds. It features $5 \mu$ s settling time to $0.01 \%, \pm 1 / 2$ LSB maximum non-linearity error, and $\pm 20 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ gain TC.
The TTL/DTL compatible input register can be ordered to accept natural binary, offset binary, BCD, or two's complement codes. The output amplifier can be programmed by the user to produce 0 to $+5 \mathrm{~V}, 0$ to $+10 \mathrm{~V}, \pm 2.5 \mathrm{~V}, \pm 5 \mathrm{~V}$, or $\pm 10 \mathrm{~V}$ outputs. Module dimensions are $2^{\prime \prime} \times 4^{\prime \prime} \times 0.4^{\prime \prime}(51 \times 102 \times$ 10 mm ).

## LOW POWER A/D (Page 100)

ADC1123, 10 BIT CMOS DEVICE: A 10 bit successive approximations A/D converter which is ideal for applications such as battery powered instruments and large data handling networks. It produces CMOS compatible parallel and serial data outputs and can be operated from a single +12 to +15 V battery.
Performance specifications include $\pm 1 / 2$ LSB maximum nonlinearity error, $100 \mu \mathrm{~s}$ maximum conversion time, and no missing codes from 0 to $+70^{\circ} \mathrm{C}$. The dimensions of this card mounted device are $3.65^{\prime \prime} \times 4.10^{\prime \prime}(92.71 \times 104.14 \mathrm{~mm})$.

## MULTIPURPOSE D/A (Page 82)

DAC1009, 12 BIT POSITIVE-TRUE LOGIC INPUT: An economical D/A converter which can be configured by the user for fixed reference or multiplying operation, current or voltage output and CMOS or TTL compatibility. The voltage output settles to $0.01 \%$ in $4 \mu \mathrm{~s}$ and the current output settles in 700ns.
Other performance features of this $2^{\prime \prime} \times 2^{\prime \prime} \times 0.4^{\prime \prime}(51 \times 51 \times$ 10 mm ) module include $\pm 11 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ gain TC and 0 to $+50^{\circ} \mathrm{C}$ monotonicity. As a multiplying D/A it has a small signal bandwidth of 950 kHz . With appropriate external circuitry, the feedthrough is less than 1 LSB at 50 kHz .

## HIGH SPEED, CURRENT OUTPUT D/A (Page 86)

DAC1106, SETTLES TO 10 BIT ACCURACY IN 50ns: A very high speed, adjustment-free D/A converter which can be ordered with either 8 or 10 bits of resolution. This $2^{\prime \prime} \times 2^{\prime \prime} \times$ $0.4^{\prime \prime}(51 \times 51 \times 10 \mathrm{~mm})$ module is designed for use in applications such as computer driven displays, automatic test equipment, and function generators.

Both versions of the DAC1106 feature $\pm 1 / 2$ LSB maximum nonlinearity error, $\pm 10 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ gain TC and $\pm 0.002 \% / \% \Delta \mathrm{~V}$ power supply rejection. The settling times to $0.2 \%, 0.1 \%$ and $0.05 \%$ are $25 \mathrm{~ns}, 40 \mathrm{~ns}$, and 50 ns respectively. A single $\pm 15 \mathrm{VDC}$ supply is the only power required.

## HIGH RELIABILITY CONVERTERS (Page 106)

ADC1111, DAC1112, SHA1114, DAC1117: Fully documented, high reliability versions of the ADC-12QM, DAC-12QS, SHA-2A, and MDA-12QD. Each unit that we build undergoes 168 hours of burn-in at $+125^{\circ} \mathrm{C}$, and temperature cycling (per method 1010 of MIL-STD-883) to ensure that it will operate reliably over the full military temperature range. Extensive qualification testing has shown that the devices are capable of operating under severe environmental conditions.

These products offer high reliability with the ease of specification and procurement normally found only in standard com-mercial-grade converters. A 15 page specification document is available for each product which lists its characteristics and capabilities in great detail. Since these are "off-the-shelf" products, we can readily quote price and delivery for one piece right up to thousands of pieces and we can normally ship you evaluation samples from stock.

## MODULAR AMPLIFIERS



FAST SETTLING, WIDEBAND, MIL-TYPE AMPLIFIER (Page 4 MODEL 51, SETTLING TO 0.05\% IN 250ns MAX: The model 51A and 51B are ultra fast, wideband, differential FET amplifiers featuring all hermetically sealed semiconductors for greater reliability and wide operating temperature range $\left(-55^{\circ} \mathrm{C}\right.$ to $+100^{\circ} \mathrm{C}$ ). Available in two drift selections; $50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, $\max$ ( 51 A ), and $20 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}, \max (51 \mathrm{~B})$, both models offer 80 MHz gain bandwidth product, slew rate of $400 \mathrm{~V} / \mu \mathrm{s}$ and $\pm 100 \mathrm{~mA}$ output current from dc to 6 MHz . Wideband input voltage noise, particularly important in display system D/A converter applications, is a low $6 \mu \mathrm{~V}, \mathrm{rms}(5 \mathrm{~Hz}$ to 2 MHz$)$.

LOW NOISE, LOW DRIFT, FET AMPLIFIER (Page 36) MODEL 52, GUARANTEED NOISE OF LESS THAN $1.5 \mu \mathrm{~V}$ : Designed for handling microvolt signals from high impedance ( $>100 \mathrm{k} \Omega$ ) sources, model 52 features low voltage noise $(1.5 \mu \mathrm{~V}$ p-p, max, 1 Hz BW ) with two low input voltage drift selections; $3 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}, \max , 52 \mathrm{~J}$ and $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, max, 52 K . High voltage gain $(120 \mathrm{~dB}, \mathrm{~min})$, high CMR $(100 \mathrm{~dB}, \mathrm{~min})$ and low input bias current ( $3 \mathrm{pA}, \mathrm{max}$ ) complete the performance profile making model 52 an ideal selection for applications such as low noise, low drift "front-end" preamplifiers for A to D converters and DVM's.

For high impedance buffering applications, model 52 offers complete protection from input transients as well as high linear common mode rejection.

## INSTRUMENTATION AMPLIFIER (Page 52)

MODEL 606, 100 kHz BANDWIDTH, $1 / 4 \mu V /{ }^{\circ} \mathrm{C}$ INPUT DRIFT, AND GUARANTEED NOISE LESS THAN $1 \mu V p-p$ : Model 606 offers virtually constant bandwidth over a gain range from 1 to $10,000 \mathrm{~V} / \mathrm{V}$ with four low max drift selections; $\mathrm{M}\left(1 / 4 \mathrm{~V} / /^{\circ} \mathrm{C}\right)$, $\mathrm{L}\left(1 / 2 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\right), \mathrm{K}\left(1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\right), \mathrm{J}\left(2 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\right)$. Input voltage noise is specified as less than $1 \mu \mathrm{~V}$ p-p ( 10 Hz Bandwidth) making model 606 the first instrumentation amplifier on the market to offer guar-

anteed low noise. Requiring only one resistor to externally program its differential gain, model 606 offers precision performance with gain nonlinearity error of $0.002 \%$, max and gain temperature stability of $15 \mathrm{ppm} /{ }^{\circ} \mathrm{C}, \max$. Add to this performance $50 \mu \mathrm{~s}$ settling to $0.01 \%$ and model 606 approaches the premium performance of rack and panel data amplifier designs, but at a fraction of their cost. Model 606 is the industry's first instrumentation amplifier to combine the best attributes of fast amplifier designs with the accuracy of slower models, producing the fastest high accuracy model.

## INSTRUMENTATION AMPLIFIER (Page 52)

MODEL 610, 50 kHz BANDWIDTH, $1 / 2 \mu V /{ }^{\circ} \mathrm{C}$ INPUT DRIFT, AND GUARANTEED NOISE LESS THAN $21 / 2 \mu \mathrm{~V} r m s$ : Analog Devices' model 610 combines good performance and low price to set an outstanding standard of value for this class of instrumentation amplifier. The 610 features guaranteed low noise performance of $2.5 \mu \mathrm{~V}$ rms, max. Other noteworthy guaranteed specifications include $0.02 \% \max$ nonlinearity, $0.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max$ offset drift and 15 ppm max gain error. When coupled with $86 \mathrm{~dB}(\mathrm{~min}) \mathrm{CMR}$, the model 610's performance characteristics enable it to maintain total amplifier errors below $0.2 \%$ over a $20^{\circ} \mathrm{C}$ temperature range.

## MEDICAL ISOLATION AMPLIFIER (Page 56)

MODEL 276J, ECONOMY, LOW NOISE, $G=3 \mathrm{~V} / \mathrm{V}$ : Offering complete patient safety and defibrillator protection, model 276 J features low input noise, $8 \mu \mathrm{~V}$ p-p ( 100 Hz bandwidth), low cost, $\$ 98$ (1-9) and high common mode rejection, 115 dB , $\min (60 \mathrm{~Hz}, 5 \mathrm{k} \Omega$ source imbalance). Pin compatible with earlier medical isolator designs (models $273 \mathrm{~J}, 273 \mathrm{~K}$ ), model 276 J provides a gain of $3 \mathrm{~V} / \mathrm{V}$ for improved low level signal processing. With $\pm 0.5 \mathrm{~V}$ input dynamic range and $100 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ output offset drift, model 276 J offers excellent performance for all low noise bio-medical and patient monitoring applications.

## INDUSTRIAL ISOLATION AMPLIFIER (Page 58)

MODEL 279J, MULTI-CHANNEL SYSTEMS, UNITY GAIN BUFFER : Designed for multi-channel isolator system applications, model 279 J joins the family of industrial isolators (models 272J, 274J) offering total ground isolation between input and output, high common mode rejection ( 150 dB , dc, balanced source), and $\pm 7.5 \mathrm{kV}$ common mode voltage capability. In multi-channel systems, oscillator interaction between model 279 J channels is eliminated by virtue of the external oscillator drive capability. Further, the internal transformercoupled* guarded isolation system of model 279J offers significant reduction of E-M noise pickup due to harsh industrial environments commonly experienced in aerospace, biomedical and industrial applications. In chemical, nuclear and metal process control systems, model 279J offers high impedance ( $10^{12} \Omega$ ) unity gain buffering with "fail safe" input circuitry.

## FUNCTION CIRCUITS

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This precision is essential in phase detection, automatic gain control and modulation/demodulation applications. Excellent low accuracy drift $\left(0.01 \% /{ }^{\circ} \mathrm{C}\right)$ and output offset drift $0.3 \mathrm{mV} /{ }^{\circ} \mathrm{C}$ $\max (435 \mathrm{~J}) ; 0.2 \mathrm{mV} /{ }^{\circ} \mathrm{C} \max (435 \mathrm{~K})$ complement the low initial errors to permit high accuracy performance over the specified operating temperature range ( 0 to $+70^{\circ} \mathrm{C}$ ). Bandwidth $(-3 \mathrm{~dB})$ is 300 kHz and wideband noise $(10 \mathrm{~Hz}$ to 10 kHz$)$ is $250 \mu \mathrm{~V}$, rms. Model 435 may be used as a direct plug-in replacement for more expensive pulse modulation type multipliers at a significantly lower price.

PRECISION, TWO QUADRANT, ANALOG DIVIDER (Page 165) MODEL 436, $1 / 4 \%$ ACCURACY, 300 kHz BANDWIDTH: Over a denominator signal range of 100 mV to 10 V (100:1), model 436 features guaranteed accuracy of $1 / 2 \%$ (436A) and $1 / 4 \%$ (436B) with no external trimming. For the ultimate in high accuracy two quadrant division, model 436 may be externally trimmed for improved performance; $0.1 \%$ (436B). Numerator nonlinearity error is less than $0.15 \%(436 \mathrm{~A})$ and $0.1 \%$ (436B) for inputs from 200 mV p-p to 20 V p-p (100:1 range). Small signal bandwidth $(-3 \mathrm{~dB})$, over the $100: 1$ signal range, is 300 kHz . Model 436 incorporates a unique voltage controlled gain trim feature, offering ease of adjustment to compensate for system errors.

## ECONOMY, TRUE RMS-TO-DC CONVERTER, IMPROVED CREST FACTOR PERFORMANCE (Page 164)

MODEL 440, $0.1 \%$ ACCURACY, DC RESPONSE: Featuring true rms-to-DC performance with high crest factor capability, model 440 offers high accuracy, $0.2 \% \max (440 \mathrm{~J}) ; 0.1 \% \max$ ( 440 K ), small size, $1.5^{\prime \prime} \times 1.5^{\prime \prime} \times 0.4^{\prime \prime}$ and low cost, $\$ 62,440 \mathrm{~J}$ (1-9). Rated accuracy is achieved for signals with crest factors as high as 5, making model 440 an excellent choice whenever rms measurements must be made independent of waveform. No external adjustments or components are required to achieve rated performance. In addition to measuring AC signals, model 440 can also measure directly the rms value of a waveform containing both AC and DC. Output offset may be externally adjusted to zero with a $20 \mathrm{k} \Omega$ trim potentiometer. For all industrial rms measurements, such as SCR motor controllers, as well as line voltage measurements with high harmonic distortion, model 440 offers economy and accuracy.

## POWER SUPPLIES

## LOW COST MODULAR POWER SUPPLIES, SEVEN NEW MODELS (Page 174)

Several new dual output ( $\pm 15 \mathrm{~V}$ and $\pm 12 \mathrm{~V}$ ) and logic ( +5 V ) supplies have been added to the popular 900 series encapsulated supplies. These new models include a low profile ( $0.87^{\prime \prime}$ case height) dual 15 V supply (model 902-2) for applications where card spacing is typically one inch. High output current models include a 2000 mA logic supply (model 922 ) as well a 350 mA dual 15 V (model 925) and a 240 mA dual 12 V (model 921). For application where it is undesirable or impractical to utilize printed circuit boards or sockets for mounting, four new chassis mount supplies are available. These supplies (models 952, 955, 970 and 971) offer the same reliable performance as previous models offered by Analog Devices, but input and output connections are made by a terminal strip rather than pins. Mounting is accomplished by four threaded inserts at the bottom of the units. Included in the chassis mount series are two 15 V duals (model $952,100 \mathrm{~mA}$; model $970,200 \mathrm{~mA}$ ) and a 5 V logic supply (model $955,1000 \mathrm{~mA}$ ).


AD2008, 4½ DIGITS, AC LINE POWERED, BECKMAN DISPLAY (Page 136)
AD2008: The AD2008 offers new versatility to users of high resolution, high accuracy DPMs. Besides offering performance that justifies a full $41 / 2$ digits of resolution (19999 counts full scale), the AD2008 has two data output options compatible to all DTL/TTL/CMOS/PMOS logic systems and an option for ratiometric operation.
The AD2008 measures voltages over a full scale range of $\pm 1.9999 \mathrm{~V}$ with a maximum error of $\pm 0.005 \%$ reading $\pm 50 \mu \mathrm{~V}$ $\pm 1$ digit. A fully floating, opto-isolated input section allows measurements to be made with common mode voltages up to 300 V rms and provides greater than 100 dB common mode noise rejection. Integration of the input voltage for three AC line periods allows greater than 60 dB of normal mode noise rejection.
The AD2008 displays the digitized data on large $0.55^{\prime \prime}$ ( 14 mm ) Beckman seven-segment gas discharge displays that are visible at distances up to 50 feet and over viewing angles of $130^{\circ}$ in all ambient fighting conditions. Data output options provide full parallel BCD data or a pulse train output for counting external to the DPM. The option for ratiometric operation allows for making measurements of the ratios of two independent input voltages.


## ORIENTATION

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## AMPLIFIER PRODUCTS

## WHICH AMPLIFIER FOR THE JOB

Selecting the best amplifier for a particular application has become almost an art when you consider the overwhelming proliferation of both operational amplifiers and committed gain amplifiers in recent years. During 1974, Analog Devices made several significant advances in operational amplifier design. Proprietary monolithic designs (IC's) moved ahead strongly with improved bias current, drift and speed characteristics challenging the high performance of today's better discrete component devices. These include both FET and bipolar input circuits.
By the same token, discrete designs also moved ahead especially in the area of fast settling, low noise, low drift and isolation amplifiers. No longer can it be said that designers should consider discretes for higher performance and monolithics for moderate performance, small size or economy. Economy and performance are now available in either form factor, making the selection process more complex than a year ago.
In the area of committed gain amplifiers, Analog Devices has added new designs which represent major improvements over models previously available. For data acquisition requirements, high speed and low drift have been achieved in its
new instrumentation amplifiers. For medical and industrial applications, isolation amplifiers appear for the first time to satisfy patient safety and equipment isolation requirements.
The following sections are intended to guide the user to the best amplifier for his application whether he be expert or new-comer to the art of selecting amplifiers. The extent of his familiarity with amplifier types and their specifications will determine how rapidly he moves to his final decision.

## HOW AMPLIFIERS ARE CLASSIFIED

To assist the designer in distinguishing among the multitude of models, many with comparable specifications, Analog Devices has listed all amplifiers in this catalog by application class. Identifying a key parameter will usually lead the designer to the best amplifier for his job. To assist in the selection process, the chart below ties the key application parameters to the relevant amplifier class which can then be located on the designated page.
Classification of Amplifiers
To assist you in selecting the best amplifier for the application, we have classified products into twelve cate-

APPLICATION GUIDE BY KEY FEATURE

| Key Feature | Application | Amplifier Classification | Page |
| :---: | :---: | :---: | :---: |
| Low drift and noise, long term stability | Medical and industrial, transducers, amplifiers, preamps | Low drift chopper <br> Low drift differential | $\begin{aligned} & 44 \\ & 46 \end{aligned}$ |
| Low bias current | High source impedance, integrators, charge amplifiers | General purpose FET electrometer | 48 |
| Wideband and fast settling | D/A, A/D converters, sample and holds, comparators | Wide bandwidth fast settling | 40 |
| Economy, moderate performance | Function generators, general designs, active filters | General purpose bipolar General purpose FET | $\begin{aligned} & 34 \\ & 36 \end{aligned}$ |
| High CMR , CMV | Long cable transmissions, noisy signal environments, instrument preamps | Isolation Instrument | $\begin{aligned} & 54 \\ & 52 \end{aligned}$ |
| Input-output isolation | Medical patient safety currents, isolation, programmable equipment | Isolation | 54 |
| Battery operation | Portable equipment, low noise, preamps | Low drift differential | 46 |
| Log or antilog | Signal compression, linearization, photometric ratios | Logarithmic | 169 |
| Voltage and/or current booster | Audio and servos, power regulators, galvanometers, current source | High output capability | 50 |

gories. In doing this we have established what we believe to be the optimum point of departure for proper amplifier selection. In some exceptional cases, an amplifier has been included in more than one category because of its outstanding versatility. But in most instances we have focused on one single attribute or key parameter for amplifier classification. For example, the chopper stabilized group focuses on low drift, but includes several models which could qualify for high output capability or wide bandwidth. We believe that low drift is the key feature.
Many designers are faced with the problem of selecting the best amplifier whether it be a microcircuit or discrete component module. To ease their task, Analog Devices has listed these devices together in this amplifier section making direct comparisons more convenient. The monolithics are also listed separately in their own section and should be referred to there when the choice must clearly be a microcircuit device.

## 1. General purpose - moderate performance

Amplifiers in this group include Analog's lowest cost devices. They are best suited for general purpose designs with moderate drift requirements in the range from 5 to $75 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, unity gain bandwidths to 1 MHz , and full power response to 100 kHz . Typical applications include summing, inverting, impedance buffering (followers) and active filtering. They are also useful for developing nonlinear transfer functions.

## 2. General purpose FET - low bias current, high $Z_{\text {IN }}$

These models should meet most design requirements, especially those which cannot be satisfied by bipolar input designs because of excessive bias currents or too low input impedance. The lower bias currents ( 1 to 100 pA ) and higher input impedances ( $10^{11} \mathrm{ohms}$ ) of FET's make them a natural choice when amplifier gain networks exceed 100 k ohms and it is necessary to minimize input loading and current offset errors for improved accuracy. Significant applications include integrators, sample and hold amplifiers, current to voltage converters and low bias current log circuits.

## 3. Wide bandwidth - fast settling

Amplifiers in this group feature both differential FET and bipolar input stages which afford a wide choice of drift and bias current specifications. They emphasize exceptionally fast response and wide bandwidths (to 100 MHz , 100 ns settling) for applications in data acquisition and pulse data transmission systems. Critical specifications are step response settling time, full power response and current output.

These amplifiers are useful for sample and hold circuits, A/D converters or as high speed buffers and integrators. Offering high output current capability, they should be considered for video or line driver circuits, D/A output amplifiers or as deflection coil amplifiers.

## 4. Low voltage drift - chopper stabilized

These amplifiers are widely accepted as the best choice when it is essential to maintain low voltage offsets and bias currents with time and temperature or whenever external offset adjustments are not practical in the application. Using carrier modulation techniques, these designs achieve bandwidths to 20 MHz , drifts to $0.1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ and long term stability of $2 \mu \mathrm{~V} /$ month. Typical applications include error summing amplifiers for servo loops, precision regulators, or as input amplifiers for laboratory grade metering instruments and test equipment.
5. Low voltage drift - differential input, high CMRR "Chopperless" low drift designs with differential inputs should be considered for high accuracy instrumentation, low level transducer bridge circuits, precision voltage comparators and for impedance buffer designs. In general, they should be selected over single ended choppers where a differential input is required or whenever possible chopper modulation spikes are objectionable in the circuit design.
Amplifiers in this group feature differential bipolar transistor input stages achieving input drifts as low as $1 / 4 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, offset voltages to $100 \mu \mathrm{~V}$ and exceptionally stable long term drifts of $3 \mu \mathrm{~V} /$ month. These devices offer differential performance with input noise of $1 \mu \mathrm{~V}$ p-p, a CMV of 10 V and 100 dB of CMR. For comparison, chopper stability approaches $1 \mu \mathrm{~V} /$ month but they are useful as single ended amplifiers only.

## 6. Electrometer - ultra low bias current

Amplifiers with bias currents less than 1 pA are classified as suitable for electrometer use where frequency response and voltage drift are usually secondary requirements. Both varactor bridge and FET input designs are employed to achieve these bias currents ranging from one picoamp $\left(10^{-12} \mathrm{~A}\right)$ to ten femptoamps ( $10^{-14} \mathrm{~A}$ ). These amplifiers are used as current-to-voltage converters with high impedance transducers such as photomultiplier tubes, flame detectors, pH cells and radiation detectors.

## 7. High output - voltage/current

Amplifiers offered here have bipolar or FET inputs with output voltage swings of $\pm 20$ volts or output current to $\pm 100 \mathrm{~mA}$. Also included is model B100, a 100 mA wideband booster for op amps. Typical applications include audio amplifiers, voltage or current regulators and driver stages for sonar transducers, galvanometers and deflection coils.

## 8. Instrumentation

The instrumentation amplifier is a committed gain amplifier with internal precision feedback networks. Its excellent drift, linearity and noise rejection capability make it a natural choice for extracting and amplifying low level signals in the presence of high common mode noise voltages. These devices are commonly used as transducer amplifiers for thermocouples, strain gage bridges, current shunts and biological probes. As preamplifiers they are capable of extracting small differential signals superimposed on large common mode voltages. Wideband designs are also available for data acquisition systems.
9. Isolation - medical, industrial

Isolation amplifiers are committed gain designs with FET and bipolar inputs and total ground isolation between input and output signals. With 120 dB of CMR, they are useful for processing millivolt signals in noisy environments (up to 5000 volts CMV) or for interrupting ground loops in medical or industrial applications. Using carrier modulation techniques and fail safe designs, the isolation amplifier is an excellent choice for ECG patient amplifier designs, offering complete patient protection, and for off-ground measurement systems.

## 10. Logarithmic Amplifier and Elements

Log modules from Analog Devices develop the instantaneous value of the log or antilog of an input signal. Contrary to communications type log amplifiers, which basically compress AC signals, the 700 series log modules operate on single polarity inputs from DC to an upper cutoff frequency. These temperature-compensated designs will work over 6 decades of input current ( 1 nA to 1 mA ) and 4 decades of voltage ( 1 mV to 10 V ). Typical applications include transducer linearization, data compression and basic computational circuits for acoustical and optical instruments in chemical, medical and industrial design.

## 11. Comparators

Comparators in this group are specialized operational amplifiers with differential inputs and two bi-stable output states. They are available with either FET or bipolar input stages and have been optimized for stable switching and threshold characteristics. These devices are useful as threshold level detectors for A/D converters, voltage to frequency converters, pulse width modulators and a wide variety of square wave and pulse generators.

## 12. Low Noise Module Amplifiers

In many applications, the key performance requirement is low noise. A special section is devoted to recommended products, for each application category, when low noise is critical. Products selected for this section include a high accuracy, low drift $\left(1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\right) \mathrm{FET}$ amplifier (model 52) with guaranteed input voltage noise less than $1.5 \mu \mathrm{~V}$ p-p ( 1 Hz BW ). In addition, a wideband ( 100 MHz BW ), fast settling amplifier (model 50 ) is included, featuring high output current $( \pm 100 \mathrm{~mA})$ and wideband noist of $6 \mu \mathrm{~V} \mathrm{rms}(5 \mathrm{~Hz}$ to 2 MHz ). For recorder preamps, bridge, and null detector applications requiring a high impedance differential preamplifier, a precision instrumentation amplifier (model 606) with guaranteed input voltage noise less than $1 \mu \mathrm{~V}$ p-p ( 10 Hz BW), is also included. Economy (model 43 K ), chopper stabilized (models 230, 234), non-inverting chopper (model 261) and bipolar (model 184) low noise amplifiers are also covered in this section.

## HOW TO SELECT OPERATIONAL AMPLIFIERS

## INTRODUCTION

In selecting the right device for a specific application, you should have clearly in mind your design objectives and a firm understanding of what published specifications mean. Beyond this, you should detail the significant variables that are pertinent to your application. The purpose of this section is to put these many decision factors into perspective to help you make the most meaningful buying decisions.
To properly choose an operational amplifier for any given set of requirements, the designer must have:

1. A complete definition of the design objectives. Signal levels, accuracy desired, bandwidth requirements, circuit impedance, environmental conditions and several other factors must be well defined before selection can beeffectively undertaken.
2. Firm understanding of what the manufacturer means by the numbers published for the parameters. Frequently, any two manufacturers may have comparable published specifications, which may have been arrived at using differing measurement techniques. This creates a pitfall in op amp selection. To avoid these difficulties, the designer must know what the published specifications mean and how these parameters are measured. He then must be able to translate these published specifications in terms meaningful to his design requirements. In the following discussion, Analog Devices provides the designer: 1) a checklist which he can apply to his application to assure that all significant factors are taken into account; 2) meaningful definitions for each of our published specifications; and 3) illustrations of how the requirements of -his design are translated in terms of these specifications to help make an effective and economical choice.

APPLICATION CHECKLIST
By way of an application checklist, the designer will need to account for the following:

Character of the application: The character of the application (inverter, follower, differential amplifier, etc.) will often influence the choice of amplifier. Chopper stabilized amplifiers, for example, are not generally applicable where differential inputs are required.
Accurate description of the input signal: It is extremely important that the input signal be thoroughly characterized. Is the input a voltage source or current source? Range of amplitude? Source impedance? Time/frequency characteristics?

Environmental conditions: What is the maximum range of temperature, time, and supply voltage over which the circuits must operate (to the required accuracy) without readjustment?
Accuracy desired: The accuracy requirement determines the extent to which the foregoing considerations are critical, and ultimately points the way to a device (or series of devices) which are acceptable. Accuracy must, of course, be defined in terms meaningful to the application with regard to bandwidth, DC offset, and other parameters.

## SELECTION PROCESS

In general, the objective of amplifier selection should be to choose the least expensive device which will meet the physical, electrical, and environmental requirements imposed by the application. This suggests that a "General Purpose" amplifier will be the best choice in all applications where the desired performance requirements can be met. Where this is not possible, it is generally because of limitations encountered in two areas - bandwidth requirements, and/or offset and drift parameters.
To make it easier to relate bandwidth requirements with the drift and offset characteristics, a capsule view of bandwidth considerations precedes the DC discussions below. The reader is then returned to an expanded discussion of gainbandwidth considerations.

Gain Bandwidth Considerations, A Capsule View Although all selection criteria must be met simultaneously, determination of the bandwidth requirements is a logical starting point because:
A) If DC information is not of interest, a suitable blocking capacitor can usually be connected at the amplifier input and all of the "drift", specifications may be ignored, and
B) Where high frequency $(>10 \mathrm{MHz})$ characteristics are of primary importance, the choice will be limited to those amplifiers designated "Wide Bandwidth/Fast Settling."
Where DC information is required and where frequency requirements are relatively modest (full power response below 100 kHz , unity gain of less than 1.5 MHz ) other criteria will probably influence the final choice. It is important, however, to choose an amplifier with which an adequate value of loop gain is assured (at the maximum frequency of interest) to obtain the desired accuracy. Loop gain is the excess of open loop gain over closed loop gain, and is responsible for the diminishing error due to fluctuations in the open loop gain due to time, temperature, etc. Typically,
a loop gain of 100 will yield an error of no more than $1 \%, 0.1 \%$ from loop gain of 1000 , etc. Where undistorted response is required, the specifications for full linear response and slewing rate should be chosen such that they are not exceeded at the highest frequency of operation.

## Offset and Drift Considerations

In the majority of op-amp applications, final selection is determined by the DC offset and drift characteristics. To undertake amplifier selection in these cases, it is necessary to translate the requirements listed above as follows. (It is assumed that bandwidth requirements have been established at this point.)

1. What input impedance must the circuit present to the signal source? This depends primarily on the source impedance, $\mathrm{R}_{\mathrm{s}}$, and the amount of loading error which is acceptable. Most amplifier circuits are designed around either the inverting or noninverting circuit of Figure 1. The choice is often made between the two to accommodate the impedance requirement. Input impedance for the inverting circuit is approximately equal to the summing impedance, $\mathrm{R}_{\mathrm{i}}$ and the upper limit on the magnitude of $\mathrm{R}_{\mathrm{i}}$ is determined by the allowable drift error because of input bias current as discussed below. The noninverting circuit offers inherently higher input impedance than the inverting circuit (due to "bootstrapping" feedback) and in this case input impedance is approximately equal to the common mode impedance of the amplifier $\mathrm{R}_{\mathrm{cm}}$.
2. How much drift error can be tolerated? The question is related to the input signal level, $\mathrm{e}_{\mathrm{s}}$, and the required accuracy. For example, to amplify or otherwise manipulate a DC input signal of one volt with an accuracy of $0.1 \%$, the offset drift error, $\mathrm{V}_{\mathrm{d}}$, must be one millivolt or less. (This assumes that other sources of error such as input loading, no ise and gain error have already been allowed for.) By the same reasoning, the allowable drift error for a 1 volt signal and $0.01 \%$ accuracy would be $100 \mu \mathrm{~V}$.
When this has been defined, the allowable limits of offset voltage ( $\mathrm{e}_{\mathrm{OS}}$ ), bias current ( $\mathrm{i}_{\mathrm{b}}$ ) and difference current can be calculated by the equations of Figure 1.

Figure 1 gives the equations which relate offset voltage ( $\mathrm{e}_{\mathrm{os}}$ ), bias current ( $\mathrm{i}_{\mathrm{b}}$ ), difference current ( $\mathrm{i}_{\mathrm{d}}$ ) and the external circuit impedances to the drift error, $\mathrm{V}_{\mathrm{d}}$, for both the inverting and the noninverting circuits. From these equations it can be seen how the input impedance requirements of the foregoing paragraphs are related to the drift error.
For example, in the case of the inverting circuit, an offset error voltage, $\mathrm{i}_{\mathrm{b}} \mathrm{R}_{\mathrm{i}}$, is generated by the bias current flowing through the summing impedance. This error increases for increasing $R_{i}$. Since $R_{i}$ also sets the input impedance, there is a conflict between high input impedance and low offset errors. Likewise, for a given offset error, higher values for $\mathrm{R}_{\mathrm{i}}$ can be used with an amplifier which has lower bias current.

Where it will otherwise function properly, the noninverting circuit generally makes a better choice for high input impedance circuits. Also, for the same source and input impedance requirement, a given amplifier will generate lower offset errors for the noninverting circuit than for the invertin circuit. This is so because the bias current flows only through $\mathrm{R}_{\mathrm{S}}$ for the noninverter and this will always be less than the input impedance, $\mathrm{R}_{\mathrm{i}}$, of the inverter. Input impedance of the noninverter (approximately $\mathrm{R}_{\mathrm{CM}}$ ) is typically $10^{7}$ ohms even for the least expensive bipolar amplifiers and up to $10^{11}$ ohms for FET types.
Unfortunately, however, the noninverting configuration can not always be used since it will not perform many circuit functions such as integration or summation. A further limitation occurs in high accuracy applications, where common mode errors may rule out this circuit configuration.
Initial offsets can usually be zeroed at room temperature so that only the maximum temperature excursion ( $\Delta \mathrm{T}$ ) from $+25^{\circ} \mathrm{C}$ need be considered. For example, over the range of -25 to $+85^{\circ} \mathrm{C}$, the maximum temperature excursion ( $\Delta \mathrm{T}$ ) from $+25^{\circ} \mathrm{C}$ would be $60^{\circ} \mathrm{C}$. As a practical matter, offset errors due to supply voltage and time drift can generally be neglected since errors due to temperature drift are usually much greater.


$$
\begin{aligned}
& \text { Input Impedance } \mathrm{R}_{\mathrm{IN}} \approx \mathrm{R}_{\mathrm{CM}} \\
& \text { \% Drift Error }=\frac{100 \mathrm{~V}_{\mathrm{d}}}{\mathrm{e}_{\mathrm{s}}}
\end{aligned}
$$

Figure 1B. Noninverting Configuration

## Current Amplifier Considerations

Before leaving the subject of offset errors, we shall discuss briefly the current amplifier configuration which is shown in Figure 2A. The obvious approach to measuring current is to develop a voltage drop across a load resistor, $\mathrm{R}_{\mathrm{f}}$, and to measure this potential with a high impedance amplifier as shown in Figure 2B.
This approach has several disadvantages as compared to the circuit of Figure 2A. First the noninverting amplifier introduces common mode errors which do not occur for Figure 2 A . Second, an ideal current meter would have zero impedance whereas, $\mathrm{R}_{\mathrm{f}}$ in Figure 2B may become very large since this resistor determines the sensitivity of the measurement. Third, the changes of input impedance, $\mathrm{R}_{\mathrm{cm}}$, for the noninverting amplifier with temperature will cause variable loading on $\mathrm{R}_{\mathrm{f}}$ and hence a change in sensitivity.

The current amplifier of Figure 2A circumvents all of these difficulties and approaches an ideal current meter; that is, there is essentially no voltage drop across the measuring circuit, since with enough open loop gain, A, the input impedance $\mathrm{R}_{\mathrm{IN}}$ becomes very small.
In selecting a current amplifier, the most important consideration is current noise, and bias current drift. Measuring accuracy is largely the ratio of current noise and drift to signal current, $\mathrm{i}_{\mathrm{s}}$. To obtain the drift of error current $\mathrm{I}_{\epsilon}$ referred to the input, use the following expression.

$$
\Delta \mathrm{I}_{\epsilon}=\left[\frac{\Delta \mathrm{e}_{\mathrm{os}}}{\Delta \mathrm{~T}}\left(\frac{\mathrm{R}_{\mathrm{f}}+\mathrm{R}_{\mathrm{s}}}{\mathrm{R}_{\mathrm{f}} \mathrm{R}_{\mathrm{s}}}\right)+\frac{\Delta \mathrm{i}_{\mathrm{B}}}{\Delta \mathrm{~T}}\right] \Delta \mathrm{T}
$$

Now, to make a proper selection you must pick an amplifier with an error current, $I_{\epsilon}$, over the operating temperature which is small compared to the signal current, $i_{s}$. Do not overlook current noise which may be more important than current drift in many applications.

Gain Bandwidth Considerations, Expanded Discussion From the previous discussion, it is apparent that most general purpose operational amplifiers will usually give adequate performance for the DC and audio frequency range applications. However, to obtain unity gain bandwidth above 2 MHz , full power response above 20 kHz and slewing rate above $6 \mathrm{~V} / \mu \mathrm{sec}$, in general, requires special design techniques. All amplifiers with wideband, fast response characteristics have been listed in the wide bandwidth group to simplify the selection for higher frequency applications.
One factor often overlooked is that stray capacitance and impedance levels of the external feedback circuit can be the major limitation in high frequency applications. For example, in Figure 1 A , if $\mathrm{R}_{\mathrm{f}}$ were one megohm and stray capacitance, $\mathrm{C}_{\mathrm{S}}$, were one picofarad then the closed loop bandwidth would be limited to $160 \mathrm{kHz}\left(1 /\left(2 \pi \mathrm{R}_{\mathrm{F}} \mathrm{C}_{\mathrm{S}}\right)\right)$ regardless of how fast the amplifier is. Moreover, output slewing rate will be limited by how fast $\mathrm{C}_{\mathrm{S}}$ can be charged which in turn is related to signal level, $\mathrm{e}_{\mathrm{s}}$, and input impedance, $\mathrm{R}_{\mathrm{i}}$, by $\mathrm{de}_{\mathrm{o}} / \mathrm{dt}=-\mathrm{e}_{\mathrm{s}} / \mathrm{R}_{\mathrm{i}} \mathrm{C}_{\mathrm{s}}$. For these reasons it is usually not possible to obtain both fast response and high input impedance for an inverting circuit since both $\mathrm{R}_{\mathrm{i}}$ and $\mathrm{R}_{\mathrm{f}}$ must be large to obtain high input impedance.
Another advantage of the noninverting circuit (Figure 1B) is that input impedance, being determined by potentiometric feedback, does not depend on the impedance levels for $\mathrm{R}_{1}$ and $\mathrm{R}_{2}$. Therefore, a low impedance can be used for $\mathrm{R}_{2}$ so that stray capacitance of $\mathrm{C}_{\mathrm{S}}$ will not limit the circuit's bandwidth. In this case the minimum value for $\mathrm{R}_{2}$ is constrained only by the output current rating of the amplifier. Again the trade-off between the frequency response and input impedance of the inverting and noninverting circuits must be evaluated in light of the common mode rejection error introduced by the noninverter.


Figure 2A. Current Amplifier

$e_{o}=\underbrace{R_{f} i_{s}}+\underbrace{e_{o s}+i_{b} R_{f}}$ for $R_{s}>R_{f}$
Signal Drift Error $=\mathrm{V}_{\mathrm{d}}$
Input Impedance $\mathrm{R}_{\mathrm{IN}} \approx \mathrm{R}_{\mathrm{f}}$
\% Drift Error $=\frac{100 \mathrm{~V}_{\mathrm{d}}}{\mathrm{R}_{\mathrm{f}} \mathrm{i}_{\mathrm{s}}}$

Figure 2B. Voltage Amplifier With Sampling Resistor

In the past, many wideband amplifiers, especially chopper stabilized units, did not offer fast response on the positive input and therefore were restricted to use in inverting circuits. However, new FET amplifiers from Analog Devices are available to meet the needs for high speed performance for either configuration.
For greater emphasis wideband applications can be separated into two categories - steady state and transient. Since the amplifier requirements for the two are somewhat different, these categories will be discussed separately.

## A. Steady State Applications

Steady state applications involve amplifying or otherwise manipulating continuous sinusoidal, complex or random waveforms. In these applications the significant issues in choosing an amplifier are as follows:

1. Is DC coupling required? If DC information is of no consequence, then the offset drift errors are not usually important and a capacitor can be used if necessary to block the output DC offset. Your only concern here is that DC offset at the output does not become so large, as might be the case with a high gain stage, that the output is saturated or the dynamic swing for AC signals is limited. One way to circumvent the latter problem is to use feedback to limit the gain at DC as shown in Figure 3. The gain of these circuits can be small at DC but large at high frequencies.
2. What closed loop gain and bandwidth are required? Closed loop gain, G, is dictated by the application. To a first approximation the intersection of the open and closed loop gain curves in Figure 4 gives the closed loop bandwidth, $\mathrm{f}_{\mathrm{c} 1}(-3 \mathrm{~dB})$. For high gain, wideband requirements, it may be necessary, or more economical, to use two amplifiers in cascade each at lower gain.
3. What loop gain is required or alternatively what gain stability, output impedance and/or linearity are necessary? The available loop gain at a particular frequencv or over a
range of frequencies is very often more important than closed loop bandwidth in selecting an amplifier. Loop gain as illustrated in Figure 4, is defined as the difference, in dB, or as the ratio, arithmetically, of the open to closed loop gain ( $\mathrm{A} \beta=\mathrm{A} / \mathrm{G}$ ). You will find in most of the equations defining the closed loop characteristic of a feedback amplifier that the loop gain ( $\mathrm{A} \beta$ ) is the determining factor in performance. Some of the more notable examples of this point are as follows:
a. Closed loop gain stability $=\triangle \mathrm{G} / \mathrm{G}$ $\Delta G / G=(\triangle A / A)[1 /(1+A \beta)]$ where $\Delta A / A$ is the open loop gain stability, usually about $1 \% /{ }^{\circ} \mathrm{C}$.
b. Closed loop output impedance $=\mathrm{Z}_{\mathrm{ocl}}=\mathrm{Z}_{\mathrm{o}} /(1+\mathrm{A} \beta)$, where $\mathrm{Z}_{\mathrm{O}}$ is the open loop output impedance, usually 200 to 5000 ohms.
c. Closed loop nonlinearity $=\mathrm{L}_{\mathrm{cl}}=\mathrm{L}_{\mathrm{ol}} /(1+\mathrm{A} \beta)$, where $\mathrm{L}_{\mathrm{ol}}$ is the open loop linearity, usually less than $5 \%$.

Loop gain of 100 , or 40 dB , is adequate for most application and this is readily achievable at DC and low frequencies. But note that loop gain decreases with increasing frequency which makes it difficult to obtain large loop gains at high frequencies. For this reason it may be necessary to use a 10 MHz unity gain amplifier in order to obtain adequate feedback over a 10 kHz bandwidth.
4. What full power response and/or slew rate are required? You should examine your expected output waveform and select an amplifier whose slewing rate exceeds the maximum rate of change of output signal. For a sinusoidal waveform with a peak voltage output equal to the rated amplifier output the frequency should not exceed $f_{p}$, the full power response of the amplifier. As the output signal voltage is reduced below the rated output voltage, the usable maximun


Figure 3. DC Feedback Minimizes Output Offset for AC Applications


Figure 4. Closed Loop Bandwidth and Loop Gain
frequency can be extended proportionately. If you do not observe these restrictions you will get distortion and unexpected DC offsets at the output of the amplifier.
There are many monolithic amplifier designs available today whose frequency response is not a simple 6 dB roll-off and which may be shaped with external RC components for improved performance. Using feed-forward or phase lag compensation networks, gain-bandwidth product and/or full power response may be shaped to meet varying design requirements. Most discrete op amps offer the stable 6 dB roll-off with specified unity gain-bandwidth and slew rate thereby limiting maximum speed and response to those published specifications.

## B. Transient Applications

In applications such as A/D and D/A converters and pulse amplifiers, the transient response of the wideband amplifier is generally more important than the gain bandwidth characteristic described above. Slewing rate, overload recovery and settling time are the specifications which determine the transient response.
When applying the high frequency amplifier, it is important to understand how amplifier performance is affected by component selection as well as impedance levels used around the amplifier.

## Settling Time

The time and frequency response of a linear, bilateral network or amplifier are related by well known mathematics. For example, the step response for a well behaved, linear, 6 dB /octave amplifier with a closed loop bandwidth of $\omega_{\mathrm{cl}}$ is shown in Figure 5.

To a first approximation, the curve in Figure 5 can be used to relate settling time to closed loop bandwidth of Figure 4. Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value (Figure 6). Settling time therefore includes the time required for the amplifier to slew from the initial value, recover from slew rate limited overload, and settle to a given error in the linear range.
However, the approximation soon breaks down since settling time is determined by a combination of amplifier characteristics (both linear and non-linear) and because it is a closed loop parameter. Therefore, it cannot be readily predicted from the open loop specifications such as slew rate, small signal bandwidth, etc.
Analog Devices specifies settling time for the condition of unity gain, relatively low impedance levels, and no capacitive loading. A full-scale step input is used to determine settling time and the step is generally unipolar - i.e.: from zero to plus or minus full scale. The settling time indicated is generally the longest time resulting from a step of either polarity and is given as a percentage of the full scale step transition.
Settling time is a non-linear function. It varies with the input signal level and it is greatly affected by impedances external to the amplifier. The non-linear dependence of settling time on these two parameters can be demonstrated by an examination of experimental data from Analog Devices' wide bandwidth model 46 amplifier.


Figure 5. Step Response for Linear 6dB/Octave Amplifier


Figure 6. Typical Settling Time Characteristics

## Settling Time vs. Signal Swing

The curves in Figure 7 illustrate model 46 settling time error versus input signal level. These " $V$ " curves are useful as a design aid for bracketing settling time versus step input level. Percentage settling time error is calculated by forming the ratio of output error to input voltage step. Shown in Figure 7 are $1 \%, 0.1 \%$ and $0.01 \%$ error points for a +10 V input step. The settling times for these errors are read off the vertical axis.
Because of nonlinear factors, extrapolation of settling times from one set of conditions to another becomes very difficult, if not impossible. This point becomes very apparent, in Figure 7, when reviewing settling time as a function of input signal swing. Using this measurement technique, the settling time error voltage, measured at point $V$, is equal to one-half of the null voltage between the input signal and the output signal.

Settling Time vs. $\mathbf{R}_{\mathbf{f}}, \mathbf{R}_{\mathbf{i}}$ and $\mathbf{C}_{\mathbf{L}}$
Experience indicates that for wide bandwidths and ultra fast settling times, $500 \Omega$ to $2.5 \mathrm{k} \Omega$, gain resistors should be used to keep stray capacitance to a minimum. The effects of various resistance values on settling time are given in the following table. In developing the data, the test circuit of Figure 7 was used, but with an output load capacitor ( $C_{L}$ ) added to the circuit.

| TABLE |  | $: \mathbf{0 . 1 \%}$ Setting Time vs $\mathbf{R}_{\mathbf{f}}, \mathbf{R}_{\mathbf{i}}, \mathbf{C}_{\mathbf{L}}$ |
| :--- | :--- | :---: |
| $\mathbf{R}_{\mathbf{f}}=\mathbf{R}_{\mathbf{i}}$ | $\mathbf{t}_{\mathbf{s}}(0.1 \%)$ | Cap Load $\left(\mathrm{C}_{\mathbf{L}}\right)$ |
| $2.5 \mathrm{k} \Omega$ | 115 nsec | $<10 \mathrm{pF}$ |
| $1.0 \mathrm{k} \Omega$ | 80 nsec | $<10 \mathrm{pF}$ |
| $500 \Omega$ | 64 nsec | $<10 \mathrm{pF}$ |
| $10.0 \mathrm{k} \Omega$ | 150 nsec | 270 pF |
| $5.0 \mathrm{k} \Omega$ | 150 nsec | 190 pF |
| $2.5 \mathrm{k} \Omega$ | 150 nsec | 100 pF |
| $1.0 \mathrm{k} \Omega$ | 150 nsec | 65 pF |
| $500 \Omega$ | 150 nsec | 55 pF |

With load capacitance set to zero, the settling time to $0.1^{1}$ error improved two-fold as $R_{f}$ and $R_{i}$ were reduced from $2.5 \mathrm{k} \Omega$ to $500 \Omega$. To show the interaction of $\mathrm{R}_{\mathrm{f}}, \mathrm{R}_{\mathrm{i}}$ and $\mathrm{C}_{\mathrm{L}}$, settling time to $0.1 \%$ error was then held constant at 150 ns while varying $R_{f}, R_{i}$ and $C_{L} . C_{L}$ was increased until settling time reached the 150 ns level. This value of $\mathrm{C}_{\mathrm{L}}$ did not create an oscillatory condition at the output, t was that value of capacitance which increased settling tim to 150 ns for a specified $\mathrm{R}_{\mathrm{f}}$ and $\mathrm{R}_{\mathrm{i}}$. Heavier capacitive load would have degraded settling time further because of rate limiting effects.
From these data, the effect of $\mathbf{R}_{f}$ and $\mathbf{R}_{\mathrm{i}}$ on performance is significant enough to recommend selecting the proper range of $R_{f}$ and $R_{i}$ with the amplifier operating in its final configuration. The small feedback capacitor placed in parallel with $\mathrm{R}_{\mathrm{f}}$ (Figure 7) partially cancels the pole forme in the loop gain response by the input resistor, $\mathrm{R}_{\mathrm{i}}$, and the amplifier input capacitance. It is selected to minimize settling time.


Figure 7A. Model 46 Inverting Configuration Test Circuit


Figure 7B. Input Voltage Step

## ERRORS DUE TO NOISE

A major criterion in the selection of an amplifier for low level signals is the amplifier input noise, since this is usually the limiting factor on system resolution. In the general case, amplifier noise can be characterized by a voltage source in series with the summing junction and a current source in parallel with the summing junction. Whenever high source impedance is encountered, current noise flowing through the source impedance will appear as an additional voltage noise, combining with the amplifier voltage noise. The sum of these noise sources will then be amplified along with the desired signal. For this reason, selection of a particular amplifier must consider both the amplifier noise performance as well as the source impedance.

Consideration must also be given to noise sources other than the amplifier whenever determining total system noise. RF noise may be fed into an amplifier through any connecting wire, including power supply and output leads. Adequate shielding and low-pass filters on all incoming leads will usually prevent noise pick-up.

Thermal noise is generated in any conductor or resistor as a result of thermal agitation of the electrons. This noise voltage source, sometimes referred to as "Johnson Noise", is generated in the resistive component of any impedance and has a value:
$e_{n}=\sqrt{4 K T B R}$
where $e_{n}=$ the rms value of the noise voltage
$\mathrm{K}=$ Boltzman's Constant $\left(1.38 \times 10^{23}\right.$ joules $\left./^{\circ} \mathrm{K}\right)$
$\mathrm{T}=$ absolute temperature of the resistance, ${ }^{\circ} \mathrm{K}$
$\mathrm{B}=$ the bandwidth in which the noise is measured
Since noise is related to the bandwidth over which the measurement is made, no noise specification is meaningful unless the bandwidth for the specification is given. Although the Thermal Noise equation may appear unweildly for practical noise calculations, all that is required to enable rapid approximations is to apply a few simple rules of thumb.

## Rules of Thumb

(1) Remember that a $100 \mathrm{k} \Omega$ resistor generates 40 nV rms in a 1 Hz bandwidth. The noise voltages generated by other values of resistances in other bandwidths can be calculated by remembering that the noise is proportional to the square root of the resistance and the bandwidth;i.e.

$$
\mathrm{e}_{\mathrm{n}}(\mathrm{rms})=(40 \mathrm{nV} / \sqrt{\mathrm{Hz}})\left(\sqrt{\frac{\mathrm{R}}{100 \mathrm{k} \Omega}(\mathrm{BW})}\right)
$$

(2) To convert the rms noise to a p-p value, a conversion factor of $6.6 \mu \mathrm{~V} \mathrm{p}-\mathrm{p} / \mu \mathrm{V}$ rms is applied for less than $0.1 \%$ probability of noise peaks exceeding calculated limits.
(3) The total rms noise contribution due to several noise sources is determined by the square root of the sum of the squares:

$$
e_{t}=\sqrt{e_{a}^{2}+e_{b}^{2}+e_{c}^{2}+\ldots e_{n}^{2}}
$$

If any noise source is less than a third of another, it may be neglected. The resulting error will be approximately $5 \%$.
(4) Restricting the bandwidth of a system to the minimum usable and using the lowest impedances possible are ways to reduce noise.

## DESIGN EXAMPLE

Figure 8A illustrates a typical circuit with noise calculations shown for each noise source. The total of the noise sources is obtained by adding each of the individual sources in a RMS fashion.
Figure 8B illustrates how the Rules of Thumb may be applied in a practical case to approximate the total output noise. In this example, model 261 J , the lowest noise non-inverting chopper type amplifier is being used with a $50 \mathrm{k} \Omega$ source impedance. The two major noise sources, in addition to the 261 J input voltage noise of $1 \mu \mathrm{~V}$ p-p, are the Johnson noise ( $58 \mu \mathrm{~V}$ p-p) and current noise ( $100 \mu \mathrm{~V}$ p-p).



Figure 8A. Noise Components


## APPLYING THE INSTRUMENTATION AMPLIFIER

The preceding discussion has focused on developing selection criteria for op amps which require external feedback networks. In transducer and certain other instrumentation applications it is important that an amplifier be able to extract signals in the presence of common mode noise while retaining its gain adjustment ability. In the conventional operational amplifier, a mismatch between the input gain setting resistors can cause substantial errors in CMRR. An instrumentation amplifier, by virtue of its committed gain configuration, employing internal feedback networks, suffers minimal degradation in CMRR as the gain is varied.

From Figure 9 the instrumentation amplifier appears to be little more than an operational amplifier operated in a differential mode. In fact, the modern instrumentation amplifier is an appreciably more sophisticated device, which usually requires three basic differential amplifiers in order to provide for the solution of "Common Mode" noise problems as found in many industrial and laboratory environments.

The appearance of this noise in the simplest possible system is shown in Figure 10. It is clear that the single ended amplifier has no ability to differentiate between the signal voltage and the "Common Mode" voltage.

A first attempt to solve the problem might involve the use of an operational amplifier in the differential mode. In principle it works. In practice, its use is restricted to fixed, low gain situations for the following reasons. To avoid source loading errors, it is necessary to use high value resistol networks which can result in troublesome bias current noise and drift. Therefore, low gains are used to keep the gain ratio $\mathrm{R}_{\mathrm{f}} / \mathrm{R}_{\text {in }}$ as low as possible.
Another problem arises in maintaining high CMR with gain changes. Since CMR is directly related to gain resistor balance, any resistor changes, as encountered when varying gain, will require a retuning. This procedure is both time consuming and impractical for most applications. These difficulties are highlighted in the example of Figure 11.
In this example a gain of $1000 \mathrm{~V} / \mathrm{V}$ is desired to amplify a 10 mV signal. To avoid loading down the $1 \mathrm{k} \Omega$ source impedance, a $1 \mathrm{M} \Omega$ resistor is used for a $0.1 \%$ loading error. The desired gain is set using a $5 \mathrm{M} \Omega$ feedback resistor and output attenuator. To preserve a CMR of 80 dB for noise rejection, the gain resistor network must be balanced to an accuracy of 1 part in 10,000 which is difficult. If the gain must now be adjusted to another value, the delicate tweaking procedure must be repeated which is one of the difficulties in using this circuit. The second obstacle obviously arises from using high gains and resistor values which lead to excessive input noise and drift.

The instrumentation amplifier, with differential inputs, overcomes these two difficulties. High input impedance is achieved without an external summing resistor and high CMRR is maintained as gain adjustments from 1 to $1000 \mathrm{~V} / \mathrm{V}$ are made by varying only one resistor. The circuit of Figure 9 demonstrates that gain adjustment using one resistor does not require changing several sets of resistors as is required to alter the gain with differential amplifiers. Close matching of internal gain resistors and other components during manufacture assures extremely high CMRR.

An output sense terminal is usually available to either convert the output for current feedback operation or to allow the use of a booster amplifier inside the feedback loop.
The equivalent model of Figure 9 reveals the main circuit elements to consider when applying this device. $\mathrm{Z}_{\mathrm{CM}}$ and $\mathrm{Z}_{\mathrm{d}}$ will yield gain errors due to loading of the source resistance and are frequency dependent. $\mathrm{Z}_{\mathrm{d}}$ will vary with gain and is specified at its minimum value. $\mathrm{Z}_{\mathrm{O}}$ will also yield small gain error under heavy loading.


## Specifying the Instrumentation Amplifier

When applying the instrumentation amplifier, several new parameters appear which are not common to the operational amplifier. For example, using a committed gain configuration eliminates open loop gain as a parameter which leads to new gain non-linearity and stability terms. Drift terms also appear differently and are gain dependent since input and output amplifiers make up the total design. Drift is specified as "referred to input (RTI) or output (RTO)" at minimum and maximum gains. Total drift, referred to input, is then calculated as: Total RTI drift $=[$ RTI drift + RTO drift/gain] $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$.
Probably the quickest way to understand and specify the instrumentation amplifier is to apply this device in a straightforward application. This is done in Figure 9. An error budget for the design is developed below to illustrate a possible selection technique.
The error calculations are based on the following considerations:
Gain Errors: Absolute gain errors become negligible by trimming $\mathrm{R}_{\mathrm{G}}$. Gain nonlinearity is $0.002 \% \max$ at 10 V f.s. This value usually can be maintained at less than full scale swings by calibrating gain at the maximum anticipated output voltage, i.e., $\pm 5 \mathrm{~V}$ out @ $\mathrm{G}=\mathbf{1 0 0 0}$. Gain drift and time stability contribute $0.015 \%$ error, with long term effects becoming negligible.

Offset Drift \& Bias Current Errors: The importance of having low offset drift is evident in this error term, since offset drift usually predominates and is crucial in high accuracy designs, even where temperature changes are moderate. Initial amplifier offset is zeroed using the balance pot.

Bias current, flowing through the $300 \Omega$ source impedance, will develop offset voltages which are trimmed to zero during initial balance. In general, the $20 \mathrm{pA} /{ }^{\circ} \mathrm{C}$ current drift error produces less than $0.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ equivalent drift for up to $100 \mathrm{k} \Omega$ bridges. For the $300 \Omega$ bridge, drift error is $0.00015 \%$. Supply voltage rejection also introduces an equivalent offset which is nulled out with initial balance. Line voltage and temperature changes may be $0.1 \%$ adding a negligible error of $0.00045 \%$.

CMR \& Noise Errors: Since the CMV is virtually constant at 5 V , the CMR error appears as an output offset which is nulled out with initial balance. However, for other applications, with widely varying CMV, high CMR is essential for low errors. The CMR is specified for CMV $= \pm 10 \mathrm{~V}$ and source imbalance of $1 \mathrm{k} \Omega$ and requires no trimming to achieve values of $90 \mathrm{~dB} \min$ ( $\mathrm{G}=1000$ ).

The input noise at $\mathbf{G}=1000$ contributes less than $0.01 \%$ in a 10 Hz bandwidth and may be reduced by heavier filtering for lower frequency applications.

## ERROR BUDGET ANALYSIS

(For Circuit of Figure 9)

| Operating Conditions | Amplifier Specifications* |
| :--- | :--- |
| $\mathrm{E}_{\mathrm{IN}}= \pm 10 \mathrm{mV}$ | $\mathrm{e}_{\mathrm{os}}$ Drift $= \pm 1 / 2 \mathrm{mV} / /^{\circ} \mathrm{C}(\mathrm{RTO}, \mathrm{G}=1000 \mathrm{~V} / \mathrm{V})$ |
| $\mathrm{E}_{\mathrm{OUT}}= \pm 10 \mathrm{~V}$ | Gain Drift $= \pm 0.0015 \% /^{\circ} \mathrm{C}$ |
| $\mathrm{E}_{\mathrm{CM}}=+5 \mathrm{~V}$ | Gain Nonlinearity $= \pm 0.002 \%$ |
| $\triangle \mathrm{~T}= \pm 10^{\circ} \mathrm{C}$ | $\mathrm{CMRR}=100 \mathrm{~dB}(\mathrm{G}=1000 \mathrm{~V} / \mathrm{V})$ |
| $\mathrm{T}_{\mathrm{AMB}}=+25^{\circ} \mathrm{C}$ | $\mathrm{Z}_{\mathrm{d}}=1000 \mathrm{M} \Omega$ |
| $\mathrm{R}_{\mathrm{LOAD}}=10 \mathrm{k} \Omega$ | $\mathrm{Z}_{\mathrm{CM}}=1000 \mathrm{M} \Omega$ |
| Bridge $=300 \Omega$ | $\mathrm{I}_{\mathrm{b}}=60 \mathrm{nA}$ |

*Model 606L used for this example

## COMPUTATION

| Error Source | \% of F.S. (10V) | Calculation |
| :---: | :---: | :---: |
| Gain Nonlinearity | $\pm 0.002 \%$ | Specified @ 10V f.s. |
| Gain Drift | $\pm 0.015 \%$ | $0.0015 \% /{ }^{\circ} \mathrm{Cx} \Delta \mathrm{T}$ |
| Offset Drift |  |  |
| Amplifier Offset | $\pm 0.05 \%$ | $\begin{gathered} 0.5 \mathrm{mV} /{ }^{\circ} \mathrm{C}(\mathrm{RTO}) \\ \mathrm{x} \Delta \mathrm{~T} \times 1 / 10 \mathrm{~V} \end{gathered}$ |
| Current Offset | $\pm 0.0006 \%$ | $\begin{gathered} 20 \mathrm{pA}{ }^{\circ} \mathrm{C} \times \mathrm{G} \times \mathrm{T} \\ \times 300 \times 1 / 10 \mathrm{~V} \end{gathered}$ |
| Power Supply Change | $\pm 0.00045 \%$ | $\begin{gathered} 0.1 \% \times 0.45 \mu \mathrm{~V} / \% \\ \times \mathrm{G} \times 1 / 10 \mathrm{~V} \end{gathered}$ |
| Noise | $\pm 0.01 \%$ | Specified ( 10 Hz BW ) |
| Total Output Error | $\pm 0.078 \% \max$ (0.03\% typical) |  |

APPLYING THE ISOLATION AMPLIFIER
Analog Devices has recently developed and introduced a series of unique DC coupled isolation amplifiers. Offering total ground isolation and low stray coupling capacitance ( $<10 \mathrm{pF}$ ) between input and output grounds, these compact modules develop extremely high CMR (126dB @ 60 Hz ) and CMV ratings (to 5 kV ) using modulation techniques with transformer isolation. Capable of transmitting millivolt signals in the presence of up to $\mathbf{5 0 0 0}$ volts common mode, with unity gain or with adjustable gain, these amplifiers are ideal for medical (ECG) applications where it is important to isolate hospital patients from potentially lethal ground fault currents, and for industrial applications, to interrupt ground loops between transducers and output conditioning circuits.

All models are designed to improve on the existing patient safety specifications of Underwriter's Laboratories and other regulatory agencies. When used for ECG and EEG patient-monitoring equipment, these amplifiers will do their job without exposing the hospital patient to the hazards of microshock and possible electrocution.
ISOLATION VS INSTRUMENTATION AMPLIFIERS There are several aspects of the isolation amplifier design which make it a useful alternative to the instrumentation amplifier for a specific set of operating conditions. In general, isolation amplifiers should be considered for applications requiring: 1) moderate gain ( 1 to $100 \mathrm{~V} / \mathrm{V}$ ); 2) high CMR and CMV under heavy source imbalance ( $5 \mathrm{k} \Omega$ ) ; 3) moderate RTO drifts (to $300 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ ); and 4) wherever it is necessary to eliminate bias currents for two wire systems or the more carefree three lead transducer hook-ups. Total signal ground isolation is an added feature which may be found useful for improving overall performance.

## Circuit Description

These designs have committed gain circuits with internal feedback networks as do instrumentation amplifiers. Each model in this series operates from DC to 2 kHz and is designed in two parts - an isolated front end amplifier section, followed by a grounded output section. The front end circuitry includes: 1) an input op amp with fixed gain (see Figure 12 for models 272,273 ) or adjustable gain (see 274 block diagram in product specification section); 2) a modulator; and 3) a DC regulator circuit, all enclosed in a floating guard-shield. The output section contains a demodulator circuit with low pass filter and power oscillator circuit operating from a single +15 VDC supply. Operating power is transformer-coupled into the shielded input circuits and capacitively or magnetically coupled (model 274) to the output demodulator circuit.

## CMR Holds Up at Low Gain

Common mode performance of isolation amplifiers is independent of amplifier gain, and is determined primarily by the amount of stray capacitance from input circuit to guard-shield (CMR 1) and from guard-shield to output common (CMR 2) (see Figure 13). Shielding and transformer design are essential to high common-mode rejection. Conversely, CMR performance of instrumentation amplifiers is gain dependent, although significantly improved over conventional differential amplifier designs.
At gains below 10, CMR is reduced to typical values of 60 dB with $1 \mathrm{k} \Omega$ source imbalance. For isolation amplifiers, typical ratings of 150 dB with a $5 \mathrm{k} \Omega$ source imbalance are not uncommon -90 dB (3000:1) improvement. High CMV ratings up to 5000 volts are also readily achieved with isolation designs which do not require the well balanced and complex circuits used in instrumentation amplifiers.

## Zero Bias Current, Low RTO Drift, Linearity

Isolation amplifiers operating with single ended input stages result in only differential current flow between input high and signal ground with zero net bias current flow. Instrument amplifiers, with differential inputs and signal ground returns, have bias current and differential current flow which require the use of a third wire return or external circuitry to accommodate these "housekeeping" bias currents.

Regarding amplifier drift: at low gains (below 10V/V), drift of instrument amplifiers (typically 100 to $500 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ RTO) usually becomes a significant part of the overall drift specification and approaches the performance of isolation amplifiers (typically $100 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ x Gain).

## GUIDELINES FOR MEDICAL APPLICATIONS

Several unique problems arise when designing front-end amplifiers for biological applications. These relate to:

1) electrode voltage offsets setting a limit on amplifier gain;
2) trading off amplifier input noise to achieve defibrillator protection; 3) dealing with multiple CMV noise sources arising along the surface of a patient's body and between patient/ amplifier ground points; and 4) providing patient protection from lethal stray leakage currents. The following discussion describes isolation amplifier features which afford some design relief when applying these devices in medical applications.

## Two CMR Ratings Available

The guard shield, enclosing the input circuitry, is brought out to an external pin for connection to a common mode
source voltage. In fact, the transformer isolation technique develops two common mode barriers, one on either side of the guard shield. This makes it possible to reject two sources of common mode error voltage. These conditions appear as CMV voltages, CMV1 and CMV2 in Figure 13, with typical values of CMR also shown.
These features are useful when CMV sources and their internal impedances are obscured or buried as might occur in fetal heart monitoring and ECG monitoring applications, whenever signal and transducer sources are not discretely defined, or when the amplifier is not in close proximity to the signal source.

Effects of Electrode Offset Voltage (ECG, EEG, etc.) Biological signals are frequently superimposed on normal mode (as opposed to common mode) offset voltages which arise from galvanic bias potentials at the patient/electrode interface. These signals, which may be as high as 500 mV (ECG) limit the amount of amplifier gain one may use before AC coupling the signal to the following high gain circuits. The unity gain buffers $(272,273,279 \mathrm{~J})$ with $\pm 3 \mathrm{~V}$ signal range are useful for processing the larger ECG signals. If amplification is desired, a gain of $20 \mathrm{~V} / \mathrm{V}$ may be taken with the 274 J to process ECG signals before saturation occurs at offsets beyond 500 mV . With lower offsets, as encountered with EEG electrodes and direct blood pressure transducer circuits, higher gains of up to $100 \mathrm{~V} / \mathrm{V}$ may be taken in the model 274J amplifier.

## Amplifier Noise Performance vs. Defibrillator Protection

 Relatively large noise voltage is developed in the large input resistor used to support repeated blasts of up to 5 kV of defi-brillator voltage. This resistor is required to limit the maximum input current to the input amplifier and to limit current out of the amplifier in the event an internal failure occurs. Unfortunately this input resistor introduces noise according to the expression

$$
\mathrm{E}_{\mathrm{n}}=0.825 \sqrt{\mathrm{R}(\mathrm{M} \Omega) \times \mathrm{BW}(\mathrm{~Hz})} \mu \mathrm{V} \text { p-p }
$$

The Johnson noise for a 1 megohm resistor is $8.25 \mu \mathrm{~V}$ p-p in a 100 Hz bandwidth, based on the above equation. Combined with $3-5 \mu \mathrm{~V}$ p-p input amplifier noise, the 273 J with 1 megohm input resistor has approximately $10 \mu \mathrm{~V}$ p-p of input noise in a 100 Hz bandwidth. Model 272J has approximately $35 \mu \mathrm{~V}$ p-p of noise; model 276 J has approximately $8 \mu \mathrm{~V}$ p-p in a 100 Hz bandwidth.

## Patient Safety

Safety is the primary concern to medical users. In medical applications, where patients may be in contact with poorly grounded equipment, the isolation amplifier reduces leakage-to-ground paths, thus preventing electrocution of the patient.
All isolation amplifiers achieve the highest safety standards for patient protection in two ways:
(1) Input Protection; the input protection resistor is made up of a series, parallel combination of the most reliable, conservatively rated resistors, capable of repeatedly absorbing the rated peak input power as well as limiting fault currents between the signal input leads.
(2) Input/Output Isolation; the "patent applied for" carrier modulation technique results in exceptionally low input/outpu1 coupling capacitance $(<10 \mathrm{pF})$.


Figure 12. Block Diagram of Unity Gain Isolation Amplifiers


Figure 13. Patient-Amplifier Interconnection Diagram

## DEFINITION OF SPECIFICATIONS


#### Abstract

Absolute Maximum Differential Under most operating conditions, feedback maintains the error voltage between inputs to near zero volts. However, in some applications, such as voltage comparators, the voltage between inputs can become large. $\mathrm{E}_{\mathrm{d}}$ defines the maximum voltage which can be applied between inputs without causing permanent damage to the amplifier.


## Common Mode Rejection

An ideal operational amplifier responds only to the difference voltage between inputs ( $\mathrm{e}+$ minus $\mathrm{e}^{-}$) and produces no out put for a common mode voltage, that is, when both inputs are at the same potential. However, due to slightly different gains between the plus and minus inputs, common mode input voltages are not entirely subtracted at the output. If the output error voltage is referred to the input (dividing by closed loop gain) it reflects the common mode error voltage between the inputs. Common mode rejection ratio (CMRR) is defined as the ratio of common mode voltage to common mode error voltage. CMRR is sometimes expressed in dB.

Precisely specifying CMRR is complicated by the fact that common mode voltage error, $\mathrm{e}_{\epsilon \mathrm{cm}}$, can be a highly nonlinear function of common mode voltage and it also varies with temperature. This is particularly true for FET input amplifiers. As a consequence, CMRR data published by Analog Devices are average figures assuming an end point measurement at the common mode voltage specified. The incremental CMRR about some large common mode voltage may be less than the average CMRR which is specified. Published CMRR specifications apply only to DC input signals. CMRR becomes lower with increasing frequency.

## Drift vs. Supply

Offset voltage, bias current and difference current vary as supply voltage is varied. Usually errors due to this effect are negligible compared to temperature drift.

Drift vs. Time
Offset voltage, bias current and difference current change with time as components age. It is important to realize that the published time drift for amplifiers does not accumulate linearly. For example, voltage drift for a chopper stabilized amplifier (which is by far the best amplifier type for long term stability) might be quoted as $1 \mu \mathrm{~V} /$ day whereas cummulative drift over 30 days would not exceed $5 \mu \mathrm{~V}$ nor $15 \mu \mathrm{~V}$ in a year. In general the drift accumulation may be extrapolated by multiplying the specified drift/day by the square root of the number of days. Since our catalog specifies drift/month, divide by $\sqrt{30}$ or 5.5 to obtain drift/ day.

## Full Power Response

The large signal and small signal response characteristics of operational amplifiers differ substantially. An amplifier will not respond to large signal changes as fast as the small signal bandwidth characteristics would predict, primarily because of slew rate limiting in the output stages. We specify full power response in two ways: Full linear response and full peak response.
Full linear response, $f_{p}$, is the maximum frequency at unity closed loop gain, for which a sinusoidal input signal will produce full output at rated load without exceeding pre-determined distortion level. Note that this specification does not relate to "response" in the sense of gain reduction with frequency but refers only to distortion in the output signal. There is no industry wide accepted value for the distortion level which determines the full linear response limitation but we use $3 \%$ as a maximum acceptable limit. One subtle point here is that in many applications the distortion which is caused by exceeding the full linear response can be comfortably ignored. But a far more serious effect, often overlooked, is that a DC offset voltage can be generated when the full linear response is exceeded. This is due to rectification of the asymmetrical feedback waveform or overloading the input stage with large distortion signals at the summing junction.
Certain amplifiers designed to optimize high frequency performance will provide full output swing substantially beyond the full linear response ( $3 \%$ distortion) limit described above. Since linear waveshape is not generally a consideration in the use of these devices, they are specified to the maximum frequency at which they will produce full output swing. This is termed "full peak response" and is indicated as such on the specification charts by the word "peak" in the row marked "Full Power Response."

## Initial Bias Current

Bias current, ib, is defined as the current required at either input from an infinite source impedance to drive the output to zero (assuming zero common mode voltage). For differential amplifiers, bias current is present at both the negative and positive inputs. All Analog Devices specifications pertain to the worst of the two (not average or mean). For single ended amplifiers, bias current refers to the current at the negative input only.

Initial bias current, $\mathrm{I}_{\mathrm{b}}$, is the bias current at either input measured at $+25^{\circ} \mathrm{C}$, rated supply voltages and zero common mode voltage. The designation ( $0 .+$ ) or ( $0 .-$ ) indicates that no internal compensation has been used to reduce initial bias current and hence the polarity is always known. The sign indicates to which power supply voltage an external
compensating resistor should be connected to zero the initial bias current. The designation ( $\pm$ ) indicates that internal compensation has been used to reduce initial bias current and that the residual bias current may be of either polarity. In general, compensating initial bias current has little effect on the bias current temperature coefficient. One should note that the bias current of FET amplifiers increases by a factor of 2 for each $10^{\circ} \mathrm{C}$ rise in temperature.

## Initial Difference Current

Difference current, id, is defined as the difference between the bias currents at each input. The input circuitry of differential amplifiers is generally symmetrical so that bias currents at both inputs tend to be equal and tend to track with changes in temperature and supply voltage. Therefore, difference current is about .1 times the bias current at either input, assuming that initial bias current has not been compensated.

## Input Impedance

Differential input impedance, $\mathrm{R}_{\mathrm{d}}$, is defined as the impedance between the two input terminals, measured at $+25^{\circ} \mathrm{C}$, assuming that the error voltage $\mathrm{e}_{\epsilon}$ is nulled or very near zero volts. To a first approximation, dynamic impedance can be represented by a capacitor, $\mathrm{C}_{\mathrm{d}}$, in parallel with $\mathrm{R}_{\mathrm{d}}$.
Common mode impedance, $\mathrm{R}_{\mathrm{cm}}$, is defined as the impedance between each input and ground (or power supply common) and is specified at $+25^{\circ} \mathrm{C}$. For most circuits common mode impedance on the negative input $\mathrm{R}_{\mathrm{cm}^{-}}$, has little significance except for the capacitance which it adds to the summing junctions. However, common mode impedance on the plus input, $\mathrm{R}_{\mathrm{cm}}+$, sets the upper limit on closed loop input impedance for the non-inverting configuration. Dynamic impedance can be represented by a capacitor, $\mathrm{C}_{\mathrm{cm}}$, in parallel with $\mathrm{R}_{\mathrm{cm}}$ which usually runs from 5 to 25 pF on the plus input.
Common mode impedance is a non-linear function of both temperature and common mode voltage. For FET amplifiers, common mode impedance is reduced by a factor of two for each $10^{\circ} \mathrm{C}$ temperature rise.

As a function of a common mode voltage, $\mathrm{R}_{\mathrm{cm}}$ is defined as average impedance for a common mode voltage change from zero to $\mathrm{E}_{\mathrm{cm}}$, that is, maximum common mode voltage. Incremental $\mathrm{R}_{\mathrm{cm}}$ about some large common mode voltage may be considerably less than the specified average $\mathrm{R}_{\mathrm{cm}}$, especially for FET input amplifiers.

## Initial Offset Voltage

Offset voltage, eos, is defined as the voltage required at the input from a zero source impedance to drive the output to
zero. Initial offset voltage, $\mathrm{E}_{\mathrm{OS}}$, defines the offset voltage at $+25^{\circ} \mathrm{C}$ and rated supply voltages. In most amplifiers, provisions are made to adjust initial offset to zero with an external trim potentiometer.

## Input Noise

Input voltage and current noise characteristics can be specified and a nalyzed very much like offset voltage and bias current characteristics. In fact, drift can be considered noise which occurs at very low frequencies. The primary difference in measuring and specifying noise as opposed to DC drift is that bandwidth must be considered. At low frequencies, 100 Hz or less, $1 / \mathrm{f}$ noise prevails which means that the noise per root cycle increases inversely with the square root of frequency. At the mid-band frequencies noise per root cycle is constant or "white."
For this reason two noise specifications are given. Low frequency noise in a bandpass of 0.01 to 1 Hz is specified as peak-to-peak with a $3.3 \sigma$ uncertainty, signifying that $99.9 \%$ of the observed peak-to-peak excursions will fall within the specified limits. Wideband noise in a bandpass of 5 Hz to 50 kHz is specified as rms.

## Maximum Common Mode Voltage

For differential input amplifiers, the voltage at both inputs can be raised above ground potential. Common mode voltage, $\mathrm{E}_{\mathrm{cm}}$, is defined as the voltage (above ground) when both inputs are at the same voltage. $\mathrm{E}_{\mathrm{cm}}$ is defined as the maximum peak common mode voltage which will produce less than a $1 \%$ error at the output. $\mathrm{E}_{\mathrm{cm}}$ establishes the maximum input voltage for the voltage follower connection.

## Open Loop Gain

Open loop gain, A , is defined as the ratio of a change of output voltage to the error voltage applied between the amplifier inputs to produce the change. Gain is usually specified only at $\mathrm{DC}\left(\mathrm{A}_{\mathrm{o}}\right)$, but in many applications the frequency dependence of gain is also important. For this reason the typical open loop gain response is published for each amplifier.

## Overload Recovery

Overload recovery, $\tau$, defines the time required for the output voltage to recover to the rated output voltage $E_{O}$ from a saturated condition. In some amplifiers the overload recovery will increase for large impedances (greater than $50 \mathrm{k} \Omega$ ) in the input circuit. Published specifications apply for low impedances and assume that overload recovery is not degraded by stray capacitance in the feedback network. Overload recovery is defined for $50 \%$ overdrive.

## Rated Output

Rated output voltage is the minimum peak output voltage which can be obtained at rated output current before
clipping or excessive non-linearity occurs. Rated output current is the minimum guaranteed value of current supplied at the rated output voltage. Load impedance less than $E_{O} / I_{O}$ can be used but $E_{O}$ will decrease, distortion may increase and open loop gain will be reduced. (All models are short circuit protected.)

## Settling Time

(See discussion in previous section on Selecting an Amplifier.)

## Slewing Rate

Slewing rate, S, usually in volts $/ \mu \mathrm{sec}$, defines the maximum rate of change of output voltage for a large input step change. $S=2 \pi \mathrm{f}_{\mathrm{p}} \mathrm{E}_{\mathrm{o}}$

## Temperature Drift

Offset voltage, bias current and difference current all change or "drift" from their initial values with temperature. This is by far the most important source of error in most applications. The temperature coefficients of these parameters, $\Delta \mathrm{e}_{\mathrm{OS}} / \Delta \mathrm{T}, \Delta \mathrm{i}_{\mathrm{b}} / \Delta \mathrm{T}$, and $\Delta \mathrm{i}_{\mathrm{d}} / \Delta \mathrm{T}$ are all defined as the average slope over a specified temperature range. In general, however, drift is a non-linear function of temperature and the slopes are greater at the extremes of temperature than around normal $\left(+25^{\circ} \mathrm{C}\right)$ ambient which generally means that for small temperature excursions, the specification is conservative.
For example, a rather popular method of specifying this extremely important parameter consists of: a) arithmetically subtracting the measured offset values at the upper and lower temperature extremes and $b$ ) dividing this difference
by the temperature excursion. This can yield an extremely misleading result, particularly where offset drifts in the same direction at the two extremes. It is obviously possible to have no difference in the two end-point measurements, yet severe slopes may exist between the two as illustrated in Figure 14. In this case the apparent (specified) drift would be zero $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$.

Analog Devices employs two methods of drift specification a "true butterfly" curve characteristic for the high performance/low drift models, and a "modified butterfly" for the lower cost amplifiers. Both overcome the deficiencies described above. A comparison of these methods is shown with definitive equations in Figure 15. Essentially, the butterfly characteristic insures that if the amplifier is adjusted to zero at room temperature $\left(\mathrm{T}_{\mathrm{r}}\right)$, the offset at any temperature would, in no case, exceed the value predicted by multiplying the specified drift rate (in $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ ) by the temperature excursion.

## Unity Gain Small Signal Response

Unity gain small signal response, $\mathrm{f}_{\mathrm{t}}$, is the frequency at which the open loop gain becomes unity or zero dB . "Small signal" indicates that in general it is not possible to obtain large output voltage swing at high frequencies because of distortion due to slew rate limiting or signal rectification. For amplifiers with symmetrical response on each input, $\mathrm{f}_{\mathrm{t}}$ may be obtained by either the inverting or non-inverting configurations. Some wideband amplifiers with feed forward design have fast response only on the negative input which restricts high speed use to the inverting circuit.


Figure 14
Figure 15

| Description | Model ${ }^{1}$ | Open Loop Gain V/V | Rated Output |  | Frequency Response |  |  | Offset Voltage vs. Temperature |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | v | mA | Unity Gain MHz | Full Power kHz | Slew Rate V/ $\mu \mathrm{s}$ | $\mu \mathbf{V} /{ }^{\circ} \mathbf{C}$ max |
| General Purpose - Bipolar |  |  |  |  |  |  |  |  |
| Moderate Performance Op Amps |  |  |  |  |  |  |  |  |
| Good Performance Economy, Low Noise | $118 \mathrm{~A} / \mathrm{K}$ | 250k | $\pm 10$ | $\pm 5$ | 1.5 | 100 min | 6.0 | $\pm 20 / \pm 5$ |
| Low Cost, 20 mA Output | $119 \mathrm{~A} / \mathrm{K}$ | 500k | $\pm 10$ | $\pm 20$ | 1.5 | 100 min | 6.0 | $\pm 20 / \pm 5$ |
| Economy, Speed, IC | AD201A | 50k | $\pm 10$ | $\pm 5$ | 1.0 | 10 | 0.5 | $\pm 15$ |
| Lowest Cost, General Purpose, IC | AD741 J/K/L* | 50k | $\pm 10$ | $\pm 10 / 5 / 5$ | 1.0 | 10 | 0.5 | $\pm 20 / \pm 15 / \pm 5$ |
| Super Beta-Low 2nA Ibias IC | AD208/A | 50k/80k | $\pm 13$ | $\pm 1.3$ | 1.0 | 10 | 0.3 | $\pm 15 / \pm 5$ |
| High Accuracy IC | AD301 AL | 80k | $\pm 10$ | $\pm 5$ | 1-10 | 0-150 | 0.25-9 | $\pm 5$ |
| General Purpose FET - |  |  |  |  |  |  |  |  |
| Low Bias Current, High $\mathbf{Z}_{\text {in }}$ Op Amps |  |  |  |  |  |  |  |  |
| Lowest Cost Discrete | $40 \mathrm{~J} / \mathrm{K}$ | 50k | $\pm 10$ | $\pm 5$ | 4.0 | 100 min | 6.0 | $\pm 50 / \pm 20$ |
| Guaranteed CMR - Low Bias, Low Noise | $43 \mathrm{~J} / \mathrm{K}$ | 50k | $\pm 10$ | $\pm 5$ | 4.0 | 100/200 min | 6.0/12.0 | $\pm 30 / \pm 5$ |
| Lowest Bias - High CMR | $41 \mathrm{~J} / \mathrm{K} / \mathrm{L}$ | 100k | $\pm 10$ | $\pm 5$ | 1.0 | 50 min | 3.0 | $\pm 25 / \pm 10 / \pm 25$ |
| Lowest Drift - 20 mA Output | 146 J/K | 100k | $\pm 10$ | $\pm 20$ | 5.0 | 150 min | 10 | $\pm 7 / \pm 2$ |
| Best Choice - Economy IC | AD503 J/K* | 20k/50k | $\pm 10$ | $\pm 5$ | 1.0 | 100 | 6.0 | $\pm 30 / \pm 10$ |
| Hybrid - Lowest Offset \& Bias, IC | AD5 11 A/B | 25k | $\pm 10$ | $\pm 5$ | 1.0 | 70 | 5.0 | $\pm 75 / \pm 25$ |
| High GBW, Slew Rate, IC | AD513 J/K* | 20k/50k | $\pm 10$ | $\pm 5$ | 1.0 | to 800 | to 50 | $\pm 75 / \pm 25$ |
| Low $\mathbf{V}_{\text {os }}$ Economy IC | AD506 J/K/L* | $50 \mathrm{k} / 120 \mathrm{k} / 100 \mathrm{k}$ | $\pm 10$ | $\pm 5$ | 1.0 | 100 | 6.0 | $\pm 30 / \pm 10 / \pm 5$ |
| Low Noise IC | AD5 $14 \mathrm{~J} / \mathrm{K} / \mathrm{L}$ | 20k/50k/50k | $\pm 10$ | $\pm 5$ | . 75 |  | 0.5 | $\pm 75 / \pm 25 / \pm 25$ |
| Low $\mathrm{V}_{\text {os }}$ Externally Compensated IC | AD5 $16 \mathrm{~J} / \mathrm{K}$ | 20k/50k | $\pm 10$ | $\pm 5$ | 1.0 | 100 | 6.0 | $\pm 75 / \pm 25$ |
| Economy IC | AD540 J/K/S | 20k/50k/50k | $\pm 10$ | $\pm 5$ | 1.0 | 100 | 6.0 | $\pm 75 / \pm 25 / \pm 50$ |
| Wide Bandwidth - |  |  |  |  |  |  |  |  |
| Fast Settling Op Amps |  |  |  |  |  |  |  |  |
| $1000 \mathrm{~V} / \mu \mathrm{s}$ Slew, 100 ns Settling, 100 mA | $46 \mathrm{~J} / \mathrm{K}$ | 25k | $\pm 10$ | $\pm 100$ | 40 | 10 MHz min | 1000 | $\pm 75 / \pm 25$ |
| $125 \mathrm{~V} / \mu \mathrm{s}, 250 \mathrm{~ns}$ Settling to $0.1 \%$ | $48 \mathrm{~J} / \mathrm{K}$ | 100k | $\pm 10$ | $\pm 20$ | 15 | 1.5 MHz (inv.) min | 125 (inv.) | $\pm 50 / \pm 15$ |
| 100 mA Output - 8 MHz fp - Diff Input | $50 \mathrm{~J} / \mathrm{K}$ | 25k | $\pm 10$ | $\pm 100$ | 40 | 8 MHz min | 500 | $\pm 50 / \pm 15$ |
| 100 mA Output - Wide Temperature Range | $51 \mathrm{~A} / \mathrm{B}$ | 50k | $\pm 10$ | $\pm 100$ | 10 | 6 MHz min | 400 | $\pm 50 / \pm 20$ |
| Lowest Cost $-1 \mu \mathrm{~s}$ Settling to $0.01 \%$ | $45 \mathrm{~J} / \mathrm{K}$ | 50k | $\pm 10$ | $\pm 20$ | 10 | 1 MHz min | 75 | $\pm 50 / \pm 15$ |
| $0.01 \%$ Buffer, $1 \mu$ s to $0.01 \%$ | $44 \mathrm{~J} / \mathrm{K}$ | 100k | $\pm 10$ | $\pm 20$ | 10 | 1 MHz min | 75 | $\pm 50 / \pm 15$ |
| 100 MHz GBW, Lowest Drift | $120 \mathrm{~A} / \mathrm{B}$ | 500k | $\pm 10$ | $\pm 25$ | 10-100 | 4 MHz min | 250 | $\pm 15 / \pm 8$ |
| FET Input, IC | AD528 J/K | 25k/50k | $\pm 10$ | $\pm 5$ | 10 | 800 | 50 | $\pm 50 / \pm 25$ |
| Wideband, $130 \mathrm{~V} / \mu \mathrm{s}$, IC | AD505 J/K* | 500 k | $\pm 10$ | $\pm 5$ | 4-10 | 2 MHz | 150 | $\pm 15 / \pm 8$ typ |
| Slew Rate, High Gain, IC | AD507 J/K* | 50k | $\pm 10$ | $\pm 10$ | 35 | 320 | 35 | $\pm 15 / \pm 15$ max |
| High Speed, Diff Input IC | AD509 J/K* | 15k | $\pm 12$ | $\pm 10$ | 1.6/2.0 | 1600/2000 | 120 | $\pm 20$ |
| High Speed, Low Cost IC | AD5 18 J/K* | 200k | $\pm 13$ | $\pm 10$ | 12 | 10,000 | 70 | $\pm 4 / \pm 2 \mathrm{mV}$ |
| Low Voltage Drift - |  |  |  |  |  |  |  |  |
| Chopper Stabilized Op Amps |  |  |  |  |  |  |  |  |
| $0.1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ Drift - Lowest Noise | 234 J/K/L | 10M | $\pm 10$ | $\pm 5$ | 2.5 | 500 min | 30 | $\pm 1.0 / \pm 0.3 / \pm 0.1$ |
| Lowest Cost - General Purpose | $233 \mathrm{~J} / \mathrm{K} / \mathrm{L}$ | 10M | $\pm 10$ | $\pm 5$ | 0.5 | 4.0 min | 0.25 | $\pm 1.0 / \pm 0.3 / \pm 0.1$ |
| Low Cost, Non-Inverting, High $\mathrm{Z}_{\text {in }}$ | 260 J/K | 5M | $\pm 10$ | $\pm 5$ | 100 Hz | $2-50 \mathrm{~Hz}$ min | 100V/sec | $\pm 0.3 / \pm 0.1$ |
| Low Noise, Non-Inverting, High $\mathrm{Z}_{\text {in }}$ | 261 J/K | 10M | $\pm 10$ | $\pm 5$ | 100 Hz | $2-50 \mathrm{~Hz}$ min | $100 \mathrm{~V} / \mathrm{sec}$ | $\pm 0.3 / \pm 0.1$ |
| General Purpose - 25 mA Output | $231 \mathrm{~J} / \mathrm{K}$ | 10 M | $\pm 10$ | $\pm 25$ | 0.5 | 3.0 min | 0.2 | $\pm 0.25 / \pm 0.1$ |
| High Bandwidth -20 mA Output | 210/211 | 100M | $\pm 10$ | $\pm 20$ | 20 | 500 | 100 | $\pm 0.5 / \pm 1.0$ |
| Low Voltage Drift - |  |  |  |  |  |  |  |  |
| Differential Input, High CMR Op Amps |  |  |  |  |  |  |  |  |
| Lowest Cost $-0.25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | 184 J/K/L | 300k | $\pm 10$ | $\pm 5$ | 1.0 | 5.0 min | 0.3 | $\pm 1.5 / \pm 0.5 / \pm 0.25$ |
| FET Input, Guaranteed Low Noise | $52 \mathrm{~J} / \mathrm{K}$ | 1M | $\pm 10$ | $\pm 5$ | 0.5 | 4.0 min | 0.25 | $\pm 3.0 / \pm 1.0$ |
| Battery Powered - General Purpose | $153 \mathrm{~J} / \mathrm{K}$ | 50k | $\pm 1.0$ | $\pm 1.0$ | 0.15 | 5.0 min | 0.02 | $\pm 5.0 / \pm 2.0$ |
| Lowest Bias, $4 \mathrm{nA}, 0.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | 180 J/K | 300k | $\pm 10$ | $\pm 2.5$ | 1.0 | 10 min | 0.6 | $\pm 1.5 / \pm 0.5$ |
| Super Beta, $3 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}, 25 \mathrm{nA}$, IC | AD508J | 4M | $\pm 10$ | $\pm 5$ | 0.3 | 1.5 | 0.12 | $\pm 3.0$ |
| Highest CMR, Low Offset and Drift, IC | AD504 J/K/L ${ }^{* 3}$ | $4 \mathrm{M} / 8 \mathrm{M} / 8 \mathrm{M}$ | $\pm 10$ | $\pm 5$ | 0.3 | 1.5 | 0.12 | $\pm 0.5 / \pm 0.5 / \pm 0.3$ |
| Electrometers - |  |  |  |  |  |  |  |  |
| Ultra Low Bias Current |  |  |  |  |  |  |  |  |
| Varactor, Inverting | $310 \mathrm{~J} / \mathrm{K}$ | 100k | $\pm 10$ | $\pm 5$ | 2 kHz | 7 Hz min | $0.4 \mathrm{~V} / \mathrm{ms}$ | $\pm 30 / \pm 10$ |
| Varactor, Non-Inverting | 311 J/K | 100k | $\pm 10$ | $\pm 5$ | 2 kHz | 7 Hz min | $0.4 \mathrm{~V} / \mathrm{ms}$ | $\pm 30 / \pm 10$ |
| Lowest Cost - High Gain FET | $42 \mathrm{~J} / \mathrm{K} / \mathrm{L}$ | 300k | $\pm 10$ | $\pm 5$ | 1.0 | 4.0 min | 0.25 | $\pm 50 / \pm 15 / \pm 25$ |
| High CMR, Wideband | $41 \mathrm{~J} / \mathrm{K} / \mathrm{L}$ | 100k | $\pm 10$ | $\pm 5$ | 1.0 | 50 min | 3.0 | $\pm 25 / \pm 10 / \pm 25$ |
| FET, Input, IC | AD523 $/$ /K/L* | $50 \mathrm{k} / 50 \mathrm{k} / 75 \mathrm{k}$ | $\pm 10$ | $\pm 5$ | 0.5 | 70 | 5.0 | $\pm 25 / \pm 15 / \pm 25$ |
| High Output Voltage or Current Op Amps |  |  |  |  |  |  |  |  |
| 100 mA Booster - Lowest Cost | B100 | 0.85 | $\pm 10$ | $\pm 100$ | - | 1 MHz min | - | $\pm 1.0 \mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| 20V, 20 mA Output - High CMR | $163 \mathrm{~A} / \mathrm{K}$ | 500k | $\pm 20$ | $\pm 20$ | 1.5 | 50 min | 6.0 | $\pm 20 / \pm 5$ |
| $20 \mu \mathrm{~V}, 5 \mathrm{~mA}$ Output - Economy | $165 \mathrm{~A} / \mathrm{K}$ | 250k | $\pm 20$ | $\pm 5$ | 1.5 | 50 min | 6.0 | $\pm 20 / \pm 5$ |
| 140 V Output | 171 J/K | 10M | $\pm 140$ | $\pm 10$ | 3.0 | 15 min | 10 | $\pm 50 / \pm 15$ |
| 100 mA Output - 8 MHz fp - Diff Input | $50 \mathrm{~J} / \mathrm{K}$ | 25k | $\pm 10$ | $\pm 100$ | 40 | 8 MHz min | 500 | $\pm 50 / \pm 15$ |
| 100 mA Output - Wide Temperature Range | $51 \mathrm{~A} / \mathrm{B}$ | 50k | $\pm 10$ | $\pm 100$ | 10 | 6 MHz min | 400 | $\pm 50 / \pm 20$ |
| Guaranteed 10 mA vs. Temp., IC | AD512 K/S | 50k | $\pm 12 / \pm 10$ | $\pm 12 / \pm 10$ | 1.0 | 10 | 0.5 | $\pm 20 / \pm 25$ |
| Instrumentation Amplifiers |  |  |  |  |  |  |  |  |
| Low Drift - Wideband - Low Noise | $606 \mathrm{~J} / \mathrm{K} / \mathrm{L} / \mathrm{M}$ | 1-10,000 | $\pm 10$ | $\pm 5$ | 1.0 | 12 | 0.8 | $\pm 2 / \pm 1 / \pm 1 / 2 / \pm 1 / 4(\mathrm{G}=1000$ ) |
| Low Drift - High CMR | $605 \mathrm{~J} / \mathrm{K} / \mathrm{L}$ | 1-1,000 | $\pm 10$ | $\pm 5$ | 0.3 | 1.5 | 0.1 | $\pm 3 / \pm 1 / \pm 0.5$ ( $\mathrm{G}=1000$ ) |
| Low Cost, General Purpose | $603 \mathrm{~J} / \mathrm{K} / \mathrm{L}$ | 1-2,000 | $\pm 10$ | $\pm 5$ | 1.0 | 10 min | 2.0 | $\pm 50 / \pm 15 / \pm 5(\mathrm{G}=1000)$ |
| Low Drift - Fixed Gains | $602 \mathrm{~J} 10 /$ |  |  |  |  |  |  |  |
|  | J100/K100 | 10/100/100 | $\pm 10$ | $\pm 4$ | 75 kHz | -1\%@ 1kHz | - | $\pm 10 / \pm 1000 / \pm 200$ |
| Low Cost, General Purpose, IC | AD5 $20 \mathrm{~J} / \mathrm{K} / \mathrm{S}$ | 1-1,000 | $\pm 10$ | $\pm 5$ | 0.2 | 75 | 4.0 | $\pm 5 / \pm 2 / \pm 2(\mathrm{G}=1000)$ |
| Isolation Amplifiers, |  |  |  |  |  |  |  |  |
| Medical, Industrial |  |  |  |  |  |  |  |  |
| EEG/ECG Inputs, Adjust Gain | 274J | 1-100 | $\pm 10$ | 0.2 | 1.2 kHz | 200 Hz | - | $\pm 200 \mathrm{RTI}, \mathrm{G}=100 \mathrm{typ}$ |
| ECG Input, 5 kV Safety | 273 K | 1.0 | $\pm 3$ | 0.06 | 4 kHz | 200 Hz | - | $\pm 100$ typ |
| Low Noise Buffer | 273J | 1.0 | $\pm 3$ | 0.06 | 4 kHz | 200 Hz | - | $\pm 100$ typ |
| ECG Input, 5 kV Safety | 272 J | 1.0 | $\pm 3$ | 0.06 | 2 kHz | 200 Hz | - | $\pm 150$ typ |
| Low Noise, Gain = 3, Economy | 276J | 3.0 | $\pm 1.5$ | 0.06 | 1 kHz | 200 Hz | - | $\pm 100$ typ, RTO |
| Multi-Channel Systems | 279J | 1.0 | $\pm 3$ | 0.06 | 4 kHz | 200 Hz | - | $\pm 100$ typ |

[^1]SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ and $\pm 15$ VDC power supply unless otherwise noted)


# GENERAL PURPOSE-MODERATE PERFORMANCE MODELS II8, II9, AD20I, AD74I, AD208, AD30IAL 

## GENERAL DESCRIPTION

Amplifiers in this group include Analog's lowest cost devices. They are best suited for general purpose designs with moderate drift requirements in the range from 5 to $40 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, unity gain band widths to 1 MHz , and full power response to 100 kHz . Using silicon bipolar transistors as the differential input stage, bias currents range from 2 to 75 nA placing upper limits of 10 k to 100 k ohms on circuit impedances for best performance. Typical applications include linear designs for summing, inverting, impedance buffering (followers) and active filtering. They are also useful for developing nonlinear transfer functions.

MODEL 118 A/K: LOWEST COST
The first op amp to consider for general purpose applications is model 118, a discrete component amplifier which surpasses the performance of lower cost IC's. It has high open loop gain and good slew rate with drifts of $20 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ (118A) and $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}(118 \mathrm{~K})$. Careful component selection and advanced design techniques yield low bias current and low thermal overshoots for improved performance over earlier discrete op amp designs.

## MODEL 119 A/K: 20mA OUTPUT

Model $119 \mathrm{~A}(\mathrm{~K})$ is identical to $118 \mathrm{~A}(\mathrm{~K})$ except for its higher 20 mA output current at $\pm 10 \mathrm{~V}$. For $\pm 20$ volt output voltage requirements, select model 163 to replace model 118, and model 165 for model 119 replacement. (See page 50, "High OutputVoltage, Current.")

## AD201/AD201A: ADJUSTABLE BANDWIDTH

The low cost AD201 series combines the dynamic response flexibility, afforded by external frequency compensation, with good DC performance. Because frequency compensation is performed externally, the AD201 provides a greater degree of design control, and permits the dynamic operating characteristics to be fitted to the specific system application. Other models to consider in this series are AD101A (military grade) and AD301A (industrial grade). The device offers full short circuit protection, external offset voltage nulling, and the absence of latch-up. (See also Linear IC Section.)

## AD301AL: LOW COST, HIGH ACCURACY, SPEED

The low cost AD301AL combines the dynamic response flexibility afforded by external frequency compensation with excellent DC performance. The amplifier increases overall accu-


[^2]racy over the standard AD201A by $30 \%$, and by a factor of 4 over the AD 301 A by reducing errors due to $\mathrm{V}_{\mathrm{OS}}, \triangle \mathrm{V}_{\mathrm{OS}} / \triangle \mathrm{T}$, $\mathrm{I}_{\mathrm{b}}$, CMRR, etc. (See also Linear IC Section.)

## AD741 J/K/L/S: LOWEST COST, HIGH ACCURACY

These low cost devices are general purpose op amps with internal frequency compensation and significantly tighter specifications which allow substantial upgrading in performance of designs desiring 741 simplicity and operating familiarity. Results of error budget analyses of typical applications show factors of improvement in accuracy ranging from 2.5 to 8 over the industry-standard AD741 and AD741C. (See also Linear IC Section.)

## AD208/208A: LOW BIAS CURRENT

Using a superbeta input device, AD208A offers low bias current, to 2 nA , for use with higher circuit impedances or for lower current drift. The " $A$ " selection has lower offset voltage and drift with specified minimum gain and CMRR ratings. Included in this series are models AD108/AD108A (military grade) and AD301/AD301A (industrial grade) with varying specifications for temperature operating range and input characteristics. (See also Linear IC Section.)


# GENERAL PURPOSE FET-LOW BIAS,HIGH $Z_{I N}$ MODELS 52, 40, 43, 4I, 42, 146, AD503, AD506, AD540, AD5II, AD514 

## GENERAL DESCRIPTION

General purpose FET amplifiers should be considered for moderate performance designs requiring high input impedance, low bias currents and bandwidths to 1 MHz . These models should meet most design requirements, especially those which cannot be satisfied by bipolar input designs because of excessive bias currents or too low input impedance. The lower bias currents ( 1 to 100 pA ) and higher input impedances ( $10^{11} \mathrm{ohms}$ ) of FETS make them a natural choice when amplifier gain networks exceed 100k ohms and it is necessary to minimize input loading and current offset errors for improved accuracy. Significant applications include integrators, sample and hold amplifiers, current to voltage converters and low bias current log circuits.

## MODEL 52 J/K: HIGH ACCURACY, LOW NOISE

Model 52 combines guaranteed voltage noise of $1.5 \mu \mathrm{~V}$ p-p $(1 \mathrm{~Hz} \mathrm{BW})$, low voltage drift, $3 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}(52 \mathrm{~J}), 1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}(52 \mathrm{~K})$, low input bias, $3 \mathrm{pA}(\mathrm{max})$ and CMR of $100 \mathrm{~dB}(\mathrm{~min})$ making it an excellent selection for high impedance, high accuracy applications. Supplied in a reliable, compact ( $1.1^{\prime \prime} \times 1.1^{\prime \prime} \times 0.4^{\prime \prime}$ ) epoxy module, model 52 offers complete protection from input transients as well as freedom from latch up when the common mode voltage range is exceeded. Short term offset stability equals the performance of chopper stabilized amplifiers, suggesting model 52 be used in auto-zero applications. Model 52 is an excellent choice to replace more expensive chopper stabilized amplifiers where significant sources of error are introduced from zero beating, "chopper spikes" and ground loop currents.

## MODEL 40 J/K: ECONOMY, LOW BIAS

The popular model 40J is a best choice for OEM designs and for the general class of applications requiring low bias current $(50 \mathrm{pA})$, moderate offset drift $\left(50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\right)$, and high input impedance ( $10^{11} \Omega$ ). Designed with minimum performance tradeoffs, it has high gain, for improved closed loop accuracy, and 4 MHz bandwidth with stable 6 dB roll-off. Select model 40 K for a lower $20 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ offset drift and a bias current of 20 pA .

## MODEL 43J : GUARANTEED 80dB CMR

Closely resembling model 40J in performance, model 43J has improved bias currents of 10 pA and offset drift of $30 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$. It is especially noted for its guaranteed CMR of 80 dB at $\pm 11$ volts for accurate noninverting buffer or differential applications. Its 10 pA bias and high input impedance are desirable for accurately amplifying small current or voltage signals approaching those levels requiring electrometer designs.

## MODEL 43K: $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, ECONOMY, LOW NOISE

This economy, low noise, low drift design features a guaranteed noise specification of $2 \mu \mathrm{~V} \mathrm{rms}(\max )$ in a 10 kHz bandwidth. Added to a $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}(\max )$ voltage drift from 0 to $+70^{\circ} \mathrm{C}$, model 43 K is an excellent choice at only $\$ 35$ (1-9). Bias current of 20 pA (max) and input impedance of $10^{11} \Omega$ are also compatible with the excellent drift and noise performance of this amplifier. Other excellent characteristics include unity gain bandwidth of 200 kHz and open loop gain of 50,000 .


MODEL $41 \mathrm{~J} / \mathrm{K} / \mathrm{L}$ : HIGH CMR, 0.5pA DIFFERENTIAL FET Model 41 has guaranteed bias currents from 0.5 pA to 0.15 pA max, typical CMR of 94 dB , and a 1 MHz bandwidth. It was specifically designed for low level current measurements demanding minimal errors when used with high impedance sources such as pH transducers, photomultipliers and long term integrators. Its speed, high CMR and low input capacitance also make it useful for medium speed automated test systems.

MODEL $42 \mathrm{~J} / \mathrm{K} / \mathrm{L}$ : LOWEST BIAS CURRENT, 110 dB GAIN Undoubtedly one of the best values for OEM designs, the model 42 is an ultra low bias current FET useful for measuring low level currents or voltages from high source impedance such as photo/ion detectors and pH transducers. Typical specifications include 110 dB open loop gain, 1 MHz bandwidth and CMR of 66 dB at $\pm 1 \mathrm{~V}$ for differential designs. Models are available with bias current as low as 75 fA and drift to $15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$. Refer to Electrometer Amplifier product group for further information. (See page 48)

## MODEL $146 \mathrm{~J} / \mathrm{K}$ : LOW VOLTAGE DRIFT, 20mA

Model 146 features low voltage and current drift for use with high impedance sources. High CMR performance make this differential FET amplifier especially useful for bridge circuits and buffer designs where good CMR performance is required for accuracy. For source impedances below $100 \mathrm{k} \Omega$, the 184 series low drift amplifiers are a good alternative to model 146 . The models 146 J and 146 K have $7 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ and $2 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ voltage drift respectively, with 80 dB CMR and 20 mA output. Other specifications include $10^{11} \Omega$ input impedance, 5 MHz bandwidth, $10 \mathrm{~V} / \mu \mathrm{sec}$ slew rates, bias currents to 20 pA and 100 dB gain for use with high speed integrators, current to voltage converters, accurate buffer designs and, in general, where speed and FET characteristics must be combined with good drift performance.

## AD503 J/K/S GENERAL PURPOSE, LOW PRICED IC

These internally compensated FET op amps, with stable 6 dB roll-off provide a good combination of economy and performance for most FET applications. In addition to their high CMRR, slew rate and low bias current, the nulling technique for trimming offset voltage results in only minor changes in drift performance - unlike other comparable IC FET designs.

## AD506 J/K/L/S HIGH ACCURACY IC

These devices are high accuracy FET-input op amps which combine the low current characteristics typical of FET amplifiers with the low initial offset voltage and offset voltage stability of bipolar amplifiers. Active laser trimming and close matching of circuit elements provide maximum warmed-up offset voltage below 1.0 mV , maximum offset voltage drift of $10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, and warmed-up bias current below 5 pA max. Other excellent characteristics include open loop gain above 75,000 and minimum CMRR of 80 dB .


[^3]
## AD540 J/K/S LOWEST COST IC

The AD540 is the lowest priced IC FET-input op amp which provides the user with low bias currents, high overall performance, and accurately specified, predictable operation. Despite its low cost, the AD540 provides such benefits as bias current and offset voltage specified under fully warmed-up conditions, gain guaranteed with the offset voltage both nulled and unnulled, and minimal variation in offset voltage drift with nulling.

AD511 A/B: HYBRID, LOWEST BIAS AND OFFSET
These devices are low cost replacements for AD501 and ADP501 type hybrid amplifiers and are manufactured by combining FET input chips with a monolithic bipolar op amp on a laser trimmed substrate. Offsets are held below 1 mV while drift and bias currents are less than $25 \mu \mathrm{~V} /^{\circ} \mathrm{C}$ and 5 pA respectively. See Linear IC section for more information.

(1) With external $499 \Omega$ trim
(2)With trim terminals open
(3)With external trim resistor supplied

AD514 J/K/L/S
The AD514 is a low noise FET-input amplifier designed for applications where low noise in addition to low bias currents are essential such as EKG amplifiers, pH electrodes and long term integrators. The device is available with 0.1 to 10 Hz voltage noise as low as $5 \mu \mathrm{~V} \max , 100 \%$ tested and guaranteed.


# WIDE BANDWIDTH-FAST SETTLING MODELS 46, 45, 50, 5I, 48, 44, 47, I20, AD505, AD507, AD509, AD518, AD528 

## GENERAL DESCRIPTION

Amplifiers in this group feature both FET and bipolar designs with differential and single ended input stages to provide a wide choice of drift and bias current specifications. They emphasize exceptionally fast response and wide bandwidths for applications in data acquisition and pulse data transmission systems. Critical specifications are step response settling time, full power response and stable 6 dB roll-off. Low output impedance and output current capability also become important for line driving applications and immunity from capacitive loads or oscillations. Typical performance numbers are unity-gain bandwidths to $80 \mathrm{MHz}, 0.1 \%$ settling times to $100 \mathrm{~ns}, 1000 \mathrm{~V} / \mu \mathrm{s}$ slew rates, and 10 MHz full power response.
These amplifiers are useful for sample and hold circuits, A/D converters, or as high speed buffers and integrators. Offering high output current capability, they should be considered for video or line driver circuits, D to A output amplifiers or as deflection control amplifiers.

## MODEL $46 \mathrm{~J} / \mathrm{K}: 1000 \mathrm{~V} / \mu \mathrm{s}$ DIFFERENTIAL, 100ns SETTLING FET, 10MHz FULL POWER

The model 46, an extremely fast amplifier, should be considered if settling time, slew rate or bandwidth are critical requirements for digital and linear signals in the 100 ns and 10 MHz region. It is an exceptionally stable FET amplifier offering guaranteed $1000 \mathrm{~V} / \mu$ s slew rate, 100 ns settling time to $0.1 \%$ and 40 MHz bandwidth with -6 dB per octave roll off.

MODEL $45 \mathrm{~J} / \mathrm{K}:$ ECONOMY, $1 \mu \mathrm{sec}$ SETTLING FET Designed for use with A to D, D to A and multiplexer circuits, the model 45 FET amplifier is the best choice for most inverting and noninverting applications. It offers a good balance between cost and performance with $75 \mathrm{~V} / \mu \mathrm{sec}$ slew rate, 10 MHz unity gain bandwidth and 20 mA output for driving up to 700 pF of capacitance. Models $45 \mathrm{~J}\left(50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\right.$, 25 pA bias) and $45 \mathrm{~K}\left(15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}, 10 \mathrm{pA}\right.$ bias) settle to $0.01 \%$ in $1 \mu \mathrm{sec}$ (max) inverting; CMR capability is 74 dB at +5 V , -10V CMV making it useful as a follower at minimum gains of $2 \mathrm{~V} / \mathrm{V}$, noninverting.

## MODEL 50: FASTEST SETTLING, 100 mA OUTPUT 100 MHz GAIN BANDWIDTH PRODUCT

Model 50 is an ultra fast wideband differential FET amplifier designed for applications requiring fast settling time with high output current in closed loop gain configurations of 2 or greater. Model 50 offers guaranteed settling of 100 ns maximum to $\pm 0.1 \%$ accuracy and 200 ns maximum to $\pm 0.05 \%$ accuracy. Figure 1 illustrates $0.1 \%$ and $0.05 \%$ settling time performance available from model 50 over closed loop gain from 1 to 10.


Unlike most high speed amplifiers, model 50 does not require high input drive voltage to achieve fast slew rate and rise time. For small signals and closed loop gains of 2 or greater, model 50 can slew faster than amplifiers having slew rate specifications of $1000 \mathrm{~V} / \mu \mathrm{s}$ and greater. Figure 2 illustrates the higher slew rate versus initial error signal along with model 46, a popular $1000 \mathrm{~V} / \mu$ s industry standard.

| Discrete |  |  |
| :---: | :---: | :---: |
| Model | Lowest Cost$1 \mu \mathrm{~s}$ to $0.01 \%$ <br> 45 <br> J | ```Fastest Settling 200ns to 0.05% at Gain of 5 5 0 J``` |
| Open Loop Gain DC Rated L.oad, V/V min | 50,000 | 25,000 |
| Rated Output, min | $\pm 10 \mathrm{~V} @ 20 \mathrm{~mA}$ | $\pm 10 \mathrm{~V}$ @ 100 mA |
| Frequency Response <br> Unity Gain, Small Signal <br> Full Power Response, min <br> Slewing Rate, min <br> Overload Recovery <br> Settling Time to 0.01\% <br> Settling Time to 0.1\% | $\begin{gathered} 10 \mathrm{MHz} \\ 1 \mathrm{MHz} \\ 75 \mathrm{~V} / \mu \mathrm{s} \\ 0.5 \mu \mathrm{~s} \\ 1.0 \mu \mathrm{~s}, \max \\ 500 \mathrm{~ns} \\ \hline \end{gathered}$ | 70 MHz 8 MHz $500 \mathrm{~V} / \mu \mathrm{s}$ $0.2 \mu \mathrm{~s}$ $200 \mathrm{~ns} \max , 0.05 \%$ $100 \mathrm{~ns} \max$ |
| Input Offset Voltage Initial, $25^{\circ} \mathrm{C}$, (Adj. to zero) <br> Avg. vs. Temp, max vs. Supply Voltage vs. Time | $\begin{aligned} & \pm 2 \mathrm{mV}^{4} \\ & \pm 50 \quad \mathrm{l} \pm 15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ & \pm 50 \mu \mathrm{~V} / \% \\ & \pm 250 \mu \mathrm{~V} / \mathrm{mo} . \end{aligned}$ | $\begin{gathered} \pm 3 \mathrm{mV}^{4} \\ \pm 50 \quad \text { \| } \pm 15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ \pm 15 \mu \mathrm{~V} / \% \\ \pm 500 \mu \mathrm{~V} / \mathrm{mo} \end{gathered}$ |
| Input Bias Current Initial, $25^{\circ} \mathrm{C}, \max$ Avg. vs. Temp, $\max$ | $\begin{gathered} 0,-50 \mathrm{pA} \text { । } 0,-25 \mathrm{pA} \\ 2 \mathrm{x} / 10{ }^{\circ} \mathrm{C} \end{gathered}$ | $\begin{aligned} & 0,-2 \mathrm{nA} \\ & 2 \mathrm{x} / 10^{\circ} \mathrm{C} \end{aligned}$ |
| Input Impedance Differential Common Mode | $\begin{aligned} & 10^{11} \Omega / 3.5 \mathrm{pF} \\ & 10^{11} \Omega / / 3.5 \mathrm{pF} \end{aligned}$ | $\begin{aligned} & 10^{10} \Omega / / 3.5 \mathrm{pF} \\ & 10^{10} \Omega / / 3.5 \mathrm{pF} \end{aligned}$ |
| ```Input Noise Voltage, 0.01 to 1Hz, p-p 5Hz to 50kHz, rms Current, 0.01 to 1Hz, p-p``` | $\begin{gathered} 5 \mu \mathrm{~V} \\ 3 \mu \mathrm{~V} \\ 0.1 \mathrm{pA} \end{gathered}$ | $\begin{gathered} 5 \mu \mathrm{~V} \\ \text { Note }^{6} \\ 1.0 \mathrm{pA} \end{gathered}$ |
| Input Voltage Range <br> Common Mode Voltage, min Common Mode Rejection @ $\pm 10 \mathrm{~V}$ Max. Safe Differential Voltage | $\begin{aligned} 74 \mathrm{~dB} & (+5,-10 \mathrm{~V}) \\ & \pm 15 \mathrm{~V} \end{aligned}$ | $\begin{gathered} \pm 10 \mathrm{~V} \\ 60 \mathrm{~dB} \text { min } \\ \pm 15 \mathrm{~V} \end{gathered}$ |
| Power Supply Range (VDC) <br> Rated Specification (VDC) | $\begin{gathered} \pm(12 \text { to } 18) \mathrm{V} \\ \pm 15 \mathrm{~V} @ 7 \mathrm{~mA} \end{gathered}$ | $\begin{aligned} & \pm(12 \text { to } 18) \mathrm{V} \\ & \pm 15 \mathrm{~V} @ 40 \mathrm{~mA} \end{aligned}$ |
| Temperature Range Operating, Rated Specifications | 0 to $+70{ }^{\circ} \mathrm{C}$ | 0 to $+70^{\circ} \mathrm{C}$ |
| Package Outline Case Dimensions | $\begin{gathered} \mathrm{QC}-1 \\ 1.12^{\prime \prime} \times 1.12^{\prime \prime} \times 0.4^{\prime \prime} \end{gathered}$ | $\frac{\mathrm{N}-1}{} 1.22^{\prime \prime} \times 1.88^{\prime \prime} \times 0.6^{\prime \prime}$ |
| $\begin{aligned} & \text { Price } \\ & \quad 1-9 \\ & 10-24 \end{aligned}$ | $\$ 38$ $\$ 48$ <br> $\$ 35$ $\$ 44$ | $\$ 75$ $\$ 92$ <br> $\$ 71$ $\$ 87$ |

(1)External trim adjustment
(2)Model 48 non-inverting slew rate- $90 \mathrm{~V} / \mu \mathrm{s}$
(3)Model 44 non-inverting slew rate- $50 \mathrm{~V} / \mu \mathrm{s}$
(4)With fixed $499 \Omega$ external trim (5) $200 \mathrm{~K} \Omega$ at $\mathrm{DC} ; 10 \mathrm{k} / / 3$ pf above 10 Hz

MODEL 51A/B: FAST SETTLING, 100 mA OUTPUT, MILTYPE

Model 51 features all hermetically sealed semiconductors for greater reliability and wide operating temperature range $\left(-55^{\circ} \mathrm{C}\right.$ to $+100^{\circ} \mathrm{C}$ ) with guaranteed settling times of 140 ns maximum to $\pm 0.1 \%$ and 250 ns maximum to $\pm 0.05 \%$. Input voltage noise ( $6 \mu \mathrm{~V} \mathrm{rms}, 5 \mathrm{~Hz}$ to 2 MHZ bandwidth) is significantly lower compared to previous designs. Other specifications are similar to model $50 \mathrm{~J} / \mathrm{K}$ (see Figures 1 and 2).




Figure 1. Settling Time vs. Gain (V/V)

MODEL $48 \mathrm{~J} / \mathrm{K}$ : 300ns SETTLING, 80dB CMR Model 48 is an ultra fast differential amplifier, optimized for D/A and A/D converter applications demanding excellent slew rate, settling time and DC characteristics. When used with these high speed circuits, its smooth settling response and wideband CMR capability are particularly useful for resolving small bit increments and for rejecting logic ground noise.
Typical specifications for this FET design include 300ns settling to $0.01 \%$ (inverting or noninverting), CMR of 80 dB at $\pm 10 \mathrm{~V}$, open loop gain of 100 dB and $125 \mathrm{~V} / \mu \mathrm{sec}$ slew rate


Figure 2. Slew Rate vs. Error Signal

| Discrete |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Fast Settling 100 mA Output Hermetically Sealed 51 <br> A <br> B | $$ | 300ns to $0.01 \%$ Smooth Settling 48 J K |  | Fast Settling Hermetically Sealed $47$ <br> A <br> B | $\begin{array}{cc} \text { Wideband } 100 \mathrm{MHz} \\ 250 \mathrm{~V} / \mu \mathrm{s} \\ & 120 \\ \text { A } & \\ \text { B } \end{array}$ |
| 50,000 | 25,000 | 100,000 | 100,000 | 100,000 | 500,000 |
| $\pm 10 \mathrm{~V} @ 100 \mathrm{~mA}$ | $\pm 10 \mathrm{~V} @ 100 \mathrm{~mA}$ | $\pm 10 \mathrm{~V} @ 20 \mathrm{~mA}$ | $\pm 10 \mathrm{~V} @ 20 \mathrm{~mA}$ | $\pm 10 \mathrm{~V}$ @ 20 mA | $\pm 10 \mathrm{~V} @ 25 \mathrm{~mA}$ |
| 56 MHz 6 MHz $400 \mathrm{~V} / \mu \mathrm{s}$ $0.2 \mu \mathrm{~s}$ 250 ns max, $0.05 \%$ 140 ns max | 40 MHz 10 MHz $1000 \mathrm{~V} / \mu \mathrm{s}$ $0.2 \mu \mathrm{~s}$ $250 \mathrm{~ns}, \max , 0.05 \%$ $100 \mathrm{~ns} \max$ | 15 MHz <br> 1.5 MHz inv $/ 1 \mathrm{MHz}$ noninv <br> $125 \mathrm{~V} / \mu \mathrm{s}^{2}$ <br> $0.5 \mu \mathrm{~s}$ <br> 300 ns <br> 250 ns | $\begin{gathered} 10 \mathrm{MHz} \\ 1 \mathrm{MHz} \\ 75 \mathrm{~V} / \mu^{3} \\ 0.5 \mu \mathrm{~s} \\ 1.0 \mu \mathrm{~s}, \max \\ 500 \mathrm{~ns} \end{gathered}$ | $\begin{gathered} 10 \mathrm{MHz} \\ 800 \mathrm{kHz} \\ 50 \mathrm{~V} / \mu \mathrm{s} \\ 0.5 \mu \mathrm{~s} \\ 1.0 \mu \mathrm{~s}, \max \\ 500 \mathrm{~ns} \\ \hline \end{gathered}$ | $\begin{gathered} 10 \text { to } 100 \mathrm{MHz}^{1} \\ 4 \mathrm{MHz} \\ 250 \mathrm{~V} / \mu_{\mathrm{s}} \\ 10 \mu_{\mathrm{s}} \\ 1.0 \mu \mathrm{~s} \\ -- \\ \hline \end{gathered}$ |
| $\begin{aligned} & \pm 3 \mathrm{mV} V^{4} \\ & \pm 50 \quad \pm 20 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ & \pm 15 \mu \mathrm{~V} / \% \\ & \pm 500 \mu \mathrm{~V} / \mathrm{mo} . \end{aligned}$ | $\begin{gathered} \pm 3 \mathrm{mV} \\ \pm 75 \pm 25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ \pm 30 \mu \mathrm{~V} / \% \\ \pm 500 \mu \mathrm{~V} / \mathrm{mo} . \end{gathered}$ |  | $\begin{gathered} \pm 50 \begin{array}{c}  \pm 2 \mathrm{mV} \\ \mathrm{I} \\ \ldots \\ \hline \end{array} \pm 15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ \pm 250 \mu \mathrm{~V} / \mathrm{mo} . \end{gathered}$ | $\begin{aligned} & \pm 50 \quad \pm 2 \mathrm{mV} V^{4} \\ & - \\ & \pm 15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ & \pm 250 \mu \mathrm{~V} / \mathrm{mo} . \end{aligned}$ | $\begin{gathered} \text { Adjust to } 0 \\ \pm 15 \mathrm{I} \stackrel{1}{ \pm} \mu \mathrm{V} /{ }^{\circ} \mathrm{C} \\ 20 \mu \mathrm{~V} / \% \\ 50 \mu \mathrm{~V} / \mathrm{mo} . \\ \hline \end{gathered}$ |
| $\begin{aligned} & 0,-2 \mathrm{nA} \\ & 2 \mathrm{x} / 10^{\circ} \mathrm{C} \\ & \hline \end{aligned}$ | $\begin{gathered} 0,-100 \mathrm{pA} \\ 2 \mathrm{x} / 10{ }^{\mathrm{g}} \mathrm{C} \end{gathered}$ | $\begin{gathered} 0,-50 \mathrm{pA} \\ 2 \mathrm{x} / 10^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} 0,-50 \mathrm{pA} \mid \\ 2 \mathrm{x} / 100^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} 0,-50 \mathrm{pA} \text { I } \\ 2 \times / 10^{\circ}{ }^{\circ} \mathrm{C} \\ 0,-25 \mathrm{pA} \\ \hline \end{gathered}$ | $0.9 \stackrel{0,+55 \mathrm{nA}}{0.7 \mathrm{nA} /{ }^{\circ} \mathrm{C} \max }$ |
| $\begin{aligned} & 10^{10} \Omega / 13.5 \mathrm{pF} \\ & 10^{10} \Omega / 13.5 \mathrm{pF} \end{aligned}$ | $\begin{aligned} & 10^{11} \Omega / 3.5 \mathrm{pF} \\ & 10^{11} \Omega / 3.5 \mathrm{pF} \\ & \hline \end{aligned}$ | $\begin{aligned} & 10^{11} \Omega / / 3.5 \mathrm{pF} \\ & 10^{11} \Omega / / 3.5 \mathrm{pF} \end{aligned}$ | $\begin{aligned} & 10^{11} \Omega / / 3.5 \mathrm{pF} \\ & 10^{11} \Omega / / 3.5 \mathrm{pF} \end{aligned}$ | $\begin{aligned} & 10^{11} \Omega / / 3.5 \mathrm{pF} \\ & 10^{11} \Omega / / 3.5 \mathrm{pF} \\ & \hline \end{aligned}$ | Note ${ }^{5}$ |
| $\begin{gathered} 5 \mu \mathrm{~V} \\ 6 \mu \mathrm{~V}(5 \mathrm{~Hz} \text { to } 2 \mathrm{MHz}) \\ 1.0 \mathrm{pA} \\ \hline \end{gathered}$ | $\begin{aligned} & 10 \mu \mathrm{~V} \\ & \text { Note }{ }^{6} \\ & 0.1 \mathrm{pA} \\ & \hline \end{aligned}$ | $\begin{gathered} 2 \mu \mathrm{~V} \\ 3 \mu \mathrm{~V} \\ 0.1 \mathrm{pA} \end{gathered}$ | $\begin{array}{r} 2 \mu \mathrm{~V} \\ 3 \mu \mathrm{~V} \\ 0.1 \mathrm{pA} \\ \hline \end{array}$ | $\begin{array}{r} 2 \mu \mathrm{~V} \\ 3 \mu \mathrm{~V} \\ 0.1 \mathrm{pA} \\ \hline \end{array}$ | $\begin{gathered} 0.5 \mu \mathrm{~V} \\ 3 \mu \mathrm{~V} \\ 100 \mathrm{pA} \\ \hline \end{gathered}$ |
| $\begin{gathered} \pm 10 \mathrm{~V} \\ 60 \mathrm{~dB}, \min \\ \pm 15 \mathrm{~V} \\ \hline \end{gathered}$ | $\begin{gathered} \pm 10 \mathrm{~V} \\ 72 \mathrm{~dB} \min \\ \pm 15 \mathrm{~V} \\ \hline \end{gathered}$ | $\begin{gathered} \pm 11 \mathrm{~V} \\ 80 \mathrm{~dB} \text { min } \\ \pm 15 \mathrm{~V} \\ \hline \end{gathered}$ | $\begin{gathered} \pm 11 \mathrm{~V} \\ 80 \mathrm{~dB}, \min \\ \pm 15 \mathrm{~V} \\ \hline \end{gathered}$ | $\begin{gathered} \pm 11 \mathrm{~V} \\ 66 \mathrm{~dB}, \mathrm{~min} \\ \pm 15 \mathrm{~V} \\ \hline \end{gathered}$ | $\begin{gathered} \text { NA } \\ \text { NA } \\ \pm 15 \mathrm{~V} \\ \hline \end{gathered}$ |
| $\begin{aligned} & \pm(12 \text { to } 18) \mathrm{V} \\ & \pm 15 \mathrm{~V} @ 40 \mathrm{~mA} \\ & \hline \end{aligned}$ | $\begin{aligned} & \pm(12 \text { to } 18) \mathrm{V} \\ & \pm 15 \mathrm{~V} @ 55 \mathrm{~mA} \end{aligned}$ | $\begin{gathered} \pm(12 \text { to } 18) \mathrm{V} \\ \pm 15 \mathrm{~V} @ 9 \mathrm{~mA} \end{gathered}$ | $\begin{gathered} \pm(12 \text { to } 18) \mathrm{V} \\ \pm 15 \mathrm{~V} @ 9 \mathrm{~mA} \end{gathered}$ | $\begin{aligned} & \pm(12 \text { to } 18) \mathrm{V} \\ & \pm 15 \mathrm{~V} @ 9 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & \pm(13 \text { to } 18) \mathrm{V} \\ & \pm 15 \mathrm{~V} @ 20 \mathrm{~mA} \\ & \hline \end{aligned}$ |
| $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 0 to $+70^{\circ} \mathrm{C}$ | 0 to $+70{ }^{\circ} \mathrm{C}$ | 0 to $+70{ }^{\circ} \mathrm{C}$ | $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | -25 to $+85{ }^{\circ} \mathrm{C}$ |
| $1.22^{\prime \prime} \times 1.88^{\prime \prime} \times 0.6^{\prime \prime}$ | $1.22^{\prime \prime} \times \begin{gathered}\mathrm{N}-1 \\ 1.88^{\prime \prime}\end{gathered} \times 0.6{ }^{\prime \prime}$ |  | $1.125^{\prime \prime} \times{ }^{\text {QC-1 }} 1.125^{\prime \prime} \times 0.4 \prime \prime$ | $\begin{gathered} \text { QC-1 } \\ 1.125^{\prime \prime} \times 1.125^{\prime \prime} \times 0.4^{\prime \prime} \end{gathered}$ | $\begin{aligned} & \mathrm{F}-3 \\ & 1.5^{\prime \prime} \times 1.5^{\prime \prime} \times 0.4^{\prime \prime} \end{aligned}$ |
| \$99 \$119 <br> $\$ 94$ $\$ 114$ | $\$ 85$ $\$ 105$ <br> $\$ 79$ $\$ 99$ | $\$ 50.50$ $\$ 61$ <br> $\$ 47.50$ $\$ 57$ | $\$ 46$ $\$ 56$ <br> $\$ 43$ $\$ 52$ | $\$ 83$ $\$ 96$ <br> $\$ 74$ $\$ 84$ | $\$ 82$ $\$ 98$ <br> $\$ 79$ $\$ 91$ |

(6) Model $46-25 \mu \mathrm{~V}$ rms, 5 Hz to 2 MHz ; Model $50-6 \mu \mathrm{~V} \mathrm{rms}, 5 \mathrm{~Hz}$ to 2 MHz .
(inverting). Extremely stable at 15 MHz bandwidths, model 48 has good immunity to oscillations under heavy load capacitance, to 750 pF . This device is available in two drift selections, $50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}(48 \mathrm{~J})$ and $15 \mu \mathrm{~V} /^{\circ} \mathrm{C}(48 \mathrm{~K})$, and uses monolithic input stages to minimize thermal feedback affects for improved small signal resolution.

## MODEL $44 \mathrm{~J} / \mathrm{K}: 0.01 \%$ BUFFER, $1 \mu \mathrm{sec}$ SETTLING FET

 Model 44 is a fast differential amplifier with guaranteed CMR of 80 dB at $\pm 10 \mathrm{~V}$ for high speed non-inverting buffer applications requiring high open loop gain and $0.01 \%$ full scale accuracy with $1 \mu \mathrm{sec}$ settling times. Capable of driving 1000 pF capacitive load, its smooth settling characteristics make it a good choice for 12 -bit D/A, A/D circuits, multiplexers, peak detectors, and sample/hold circuits where overall speed is affected by this cascaded circuit element. Other specifications include 100dB open loop gain, 10 MHz band width, $50 \mathrm{~V} / \mu \mathrm{sec}$ slew rate, 20 mA output. Model 44 J is available with $50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ drift and model 44 K with $15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ drift.
## MODEL 47 A/B: FAST SETTLING, HERMETICALLY SEALED

Model 47 with all hermetically sealed devices is recommended to upgrade models 44 and 45 for wider temperature range applications as required in military grade circuits. Settling time is $1 \mu \mathrm{~s}$ to $0.01 \%$ (inverting and noninverting) and CMR is 86 dB at $\pm 10 \mathrm{~V}$. Other specifications parallel those of model $44 \mathrm{~J} / \mathrm{K}$.

MODEL $120 \mathrm{~A} / \mathrm{B}: 100 \mathrm{MHz}$ BANDWIDTH, $1 \mu \mathrm{sec}$ SETTLING The model 120 offers design flexibility in an inverting amplifier with bipolar input stage and externally adjustable gainbandwidth product from 10 MHz to 100 MHz . Requiring only a single resistor for frequency response shaping, it is very useful for providing large gains at wide bandwidth, as used in video circuits, radar signal processing, fast Fourier Transformer or, in general, whenever fast low level signals must be amplified accurately. At lower gains, it achieves $250 \mathrm{~V} / \mu \mathrm{sec}$ slew rates and $1 \mu \mathrm{sec}$ settling with $0.01 \%$ error for use in comparators, D/A converters or in other high speed circuits.
Optimized for use with circuit impedances below $10 \mathrm{k} \Omega$, the model 120 will deliver 25 mA and is available in two versions: $120 \mathrm{~A}\left(15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\right)$ and $120 \mathrm{~B}\left(8 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\right)$.

## AD505 J/K/S: $150 \mathrm{~V} / \mu \mathrm{sec}$, HIGH DC ACCURACY, MONOLITHIC

Model 505, with bipolar input, features high gain, low voltage drift and wide bandwidth when operated in the inverting mode. Using external frequency compensation, these devices should be considered for high speed applications requiring fast slew rates and settling times or whenever high loop gain is required at wideband frequencies. Typical applications include active filters, sample/hold circuits, D/A and A/D converters.

Specifications include high open loop gain, typical slew rate of $150 \mathrm{~V} / \mu \mathrm{sec}$ and bias current below 40nA. (The AD5 05 is availa-

|  | Microcircuit |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Model | Wideband $150 \mathrm{~V} / \mu \mathrm{s}$ Inverter AD505 <br> K | J KLow Cost <br> Wideband <br> AD507 |  |  | S |  |
| Open Loop Gain <br> DC Rated L.oad, V/V min <br> Rated Output, min | $\begin{aligned} 100,000 & \text { I } 250,000 \\ & \pm 10 \mathrm{~V} @ 5 \mathrm{~mA} \end{aligned}$ | 80,000 | I | $\begin{gathered} 100,000 \\ \pm 10 \mathrm{~V} @ 10 \mathrm{~mA} \end{gathered}$ |  | 100,000 |
| Frequency Response <br> Unity Gain, Small Signal <br> Full Power Response, min <br> Slewing Rate, min <br> Overload Recovery <br> Settling Time to $0.01 \%$ <br> Settling Time to $0.1 \%$ | $$ |  |  | $\begin{gathered} 35 \mathrm{MHz} \\ 320 \mathrm{kHz} \\ 20 \mathrm{~V} / \mu \mathrm{sec} \\ - \\ - \\ - \end{gathered}$ |  |  |
| Input Offset Voltage Initial, $25^{\circ} \mathrm{C}$, (Adj. to zero) <br> Avg. vs. Temp, max vs. Supply Voltage vs. Time | $\begin{array}{l\|l\|l}  \pm 5.0 \mathrm{mV} & \pm 2.5 \mathrm{mV} & \pm 2.5 \mathrm{mV} \max \\ \pm 15 & \pm 8 & \pm 10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \text { typ } \\ & \pm 45 \mu \mathrm{~V} / \% & \end{array}$ | $\begin{gathered} \pm 5 \mathrm{mV} \\ \pm 15 \mathrm{typ} \\ \pm 30 \mu \mathrm{~V} / \% \end{gathered}$ | $\mid$ | $\begin{gathered} \pm 3 \mathrm{mV} \\ \pm 15 \max \\ \pm 15 \mu \mathrm{~V} / \% \max \end{gathered}$ |  | $\begin{aligned} & 4 \mathrm{mV} \max \\ & 0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max \\ & 5 \mu \mathrm{~V} / \% \max \end{aligned}$ |
| Input Bias Current Initial, $25^{\circ} \mathrm{C}, \max$ Avg. vs. Temp, max | 75 nA I | 25 nA | 1 | $15 \mathrm{nA}$ |  | 15 nA |
| Input Impedance <br> Differential <br> Common Mode | Note ${ }^{1}$ |  | - | $300 \times 10^{6}$ |  |  |
| ```Input Noise Voltage, 0.01 to 1Hz, p-p 50Hz to 50kHz, rms Current, 0.01 to 1Hz, p-p``` | $\begin{gathered} 8 \mu \mathrm{~V}(0.01 \mathrm{~Hz} \text { to } 10 \mathrm{~Hz}) \\ 20 \mu \mathrm{~V}(10 \mathrm{~Hz} \text { to } 1 \mathrm{MHz}) \\ 200 \mathrm{pA}(0.01 \mathrm{~Hz} \text { to } 10 \mathrm{~Hz}) \end{gathered}$ |  |  |  |  |  |
| Input Voltage Range <br> Common Mode Voltage, min <br> Common Mode Rejection @ $\pm 10 \mathrm{~V}$ <br> Max. Safe Differential Voltage | $\begin{gathered} \text { NA } \\ \text { NA } \\ \pm 10 \mathrm{~V} \end{gathered}$ |  |  | $\pm 11 \mathrm{~V}$ 100 dB $\pm 12 \mathrm{~V}$ |  |  |
| Power Supply Range (VDC) <br> Rated Specification (VDC) | $\begin{aligned} & \pm(5 \text { to } 18) \mathrm{V} \\ & \pm 15 \mathrm{~V} @ 6 \mathrm{~mA} \end{aligned}$ |  | - | $\begin{gathered} \pm(5 \text { to } 20) \mathrm{V} \\ \pm 15 \mathrm{~V} @ 4 \mathrm{~mA} \end{gathered}$ |  |  |
| Temperature Range Operating, Rated Specifications | 0 to $+70^{\circ} \mathrm{C} \quad 10$ to $+70^{\circ} \mathrm{C} \quad \mid-55$ to $+125^{\circ} \mathrm{C}$ | 0 to $+70^{\circ} \mathrm{C}$ | 1 | 0 to $+70^{\circ} \mathrm{C}$ |  | to $+125^{\circ} \mathrm{C}$ |
| Package Outline Case Dimensions | TO-100 <br> --- |  |  | TO-99 |  |  |
| $\begin{aligned} & \text { Price } \\ & 1-9 \\ & 10-24 \end{aligned}$ | $\$ 17.25$ $\$ 20.70$ $\$ 24.15$ <br> $\$ 17.25$ $\$ 20.70$ $\$ 24.15$ | $\begin{aligned} & \$ 9.50 \\ & \$ 9.50 \end{aligned}$ | 1 | $\begin{aligned} & \$ 15.00 \\ & \$ 15.00 \end{aligned}$ |  | $\begin{aligned} & \$ 22.50 \\ & \$ 22.50 \end{aligned}$ |
| (1) $2 \mathrm{M} \Omega$ at $\mathrm{DC} ; 20 \mathrm{k}$ above 20 Hz . | (2) $\mathrm{V}_{\mathrm{IN}}= \pm 5 \mathrm{~V}$ : | , |  |  |  |  |

ble in two accuracy selections: $\mathrm{J}, \mathrm{K}$ for 0 to $+70^{\circ} \mathrm{C}$ operation; and, S for $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ operation.)

## AD507 J/K/S: LOW COST, $35 \mathrm{~V} / \mu \mathrm{sec}$, HIGH ACCURACY

Model AD507 is recommended for use where low cost and allaround excellent performance, especially at high frequencies, are needed. It is particularly well suited as a fast high impedance comparator, integrator, or wideband amplifier, and in sample-and-hold circuits. It is unconditionally stable for all closed loop gains above 10 without external compensation. The frequency compensation terminal is used for stability at lower closed loop gains.
The AD507 provides a gain bandwidth of 100 MHz , minimum slew rate of $25 \mathrm{~V} / \mu \mathrm{sec}(\mathrm{K})$, maximum $\mathrm{I}_{\mathrm{b}}$ and $\mathrm{I}_{\mathrm{OS}}$ of $15 \mathrm{nA}(\mathrm{K})$ and, for wide-temperature range applications, drift below $20 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ (S).

## AD509 J/K/S: $\mathbf{2 \mu s e c}$ MAX TO $0.01 \%, 20 \mathrm{MHz}$ BANDWIDTH

 Model AD509 is a fast differential input amplifier whose combination of low cost and excellent dynamic performance makes it a preferred choice for 12 bit D/A and A/D circuits, sample/ hold circuits, multiplexers, and other applications requiring fast settling time to low error levels. The AD509 is stable for all values of closed-loop gain $>3$, and can be stabilized for any value of closed-loop gain with a single external capacitor.Specifications include maximum settling time to $0.01 \%$ of low 2 mV , maximum offset voltage drifts of $15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, and bandwidth, and $\pm 10 \mathrm{~mA}$ minimum output current at $\pm 10 \mathrm{~V}$.

## AD518 J/K/S: HIGH SPEED, LOW COST

The AD518 is a precision monolithic operational amplifier designed for applications where high slew rate and wide bandwidth are required but low cost and ease of use are essential. The devices are internally compensated for unity gain applications with a $60^{\circ}$ phase margin to insure stability, a minimum slew rate of $50 \mathrm{~V} / \mu \mathrm{sec}$, and a bandwidth of 12 MHz . The AD518's DC performance is consistent with its precision dynamic characteristics. The devices feature offset voltages below 2 mV , maximum offset voltage drifts of $10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, and offset currents below 50 nA max.
The high slew rate, fast settling time, ease of use and low cost make the AD5 18 ideal for use with D/A and A/D converters, as well as active filters, sample and hold circuits, and as a general purpose amplifier.

## AD528 J/K/S: LOW BIAS, HIGH SPEED

The AD528 is a high speed precision FET-input operational amplifier combining the advantage of very high slew rate $(50 \mathrm{~V} / \mu \mathrm{sec})$, wide bandwidth $(10 \mathrm{MHz})$ and ultra low bias currents $(15 \mathrm{pA})$. The device is internally compensated for unity gain applications with a $60^{\circ}$ phase margin to insure stability. Laser trimming provides offset voltages down to 1 mV max.

Microcircuit

| Micro circuit |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Fast Settling to High Accuracy AD509 |  |  |  |  | High Speed, Low Cost AD518 |  |  |  |  | Low Bias, Precision AD528 |  |  |  |
| J |  | K |  | S | J |  | K |  | S | J | K |  | s |
| 7,500 |  | $\begin{gathered} 10,000 \\ \pm 10 \mathrm{~V} @ 10 \mathrm{~mA} \end{gathered}$ | 1 | 10,000 | 25,000 |  | $\begin{gathered} 50,000 \\ \pm 12 \mathrm{~V} @ 10 \mathrm{~mA} \end{gathered}$ |  | $50,000$ | 25,000 | $\begin{aligned} & 1 \quad 50,000 \\ & \pm 10 \mathrm{~V} @ 5 \mathrm{~mA} \end{aligned}$ |  | $50,000$ |
| $\begin{array}{r} 120 \mathrm{kHz} \\ 80 \mathrm{~V} / \mu \mathrm{s} \\ 200 \mathrm{~ns} \mathrm{typ} \\ 1.0 \mu \mathrm{~s} \text { typ } \end{array}$ |  | $\begin{gathered} 20 \mathrm{MHz} \\ 150 \mathrm{kHz} \\ 100 \mathrm{~V} / \mu \mathrm{s} \\ - \\ 500 \mathrm{~ns} \max \\ 2.0 \mu \mathrm{~s} \max \end{gathered}$ |  | $\begin{gathered} 150 \mathrm{kHz} \\ 100 \mathrm{~V} / \mathrm{s} \\ \\ \begin{array}{c} 500 \mathrm{~ns} \max \\ 2.0 \mu \mathrm{~s} \max \end{array} \end{gathered}$ |  |  | $\begin{gathered} 12 \mathrm{MHz} \\ - \\ 50 \mathrm{~V} / \mu \mathrm{s} \\ - \\ 2 \mu \mathrm{~s} \\ 800 \mathrm{~ns} \end{gathered}$ |  |  |  |  |  |  |
| $\begin{gathered} 10 \mathrm{mV} \max \\ 20 \mathrm{typ} \\ 200 \end{gathered}$ |  | $\begin{gathered} 8 \mathrm{mV} \max \\ 30 \max \\ 100 \end{gathered}$ |  | $\begin{gathered} 8 \mathrm{mV} \max \\ 30 \mathrm{max} \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ 100 \mu \mathrm{~V} / \mathrm{V} \max \end{gathered}$ | 10 mV | I | $\begin{gathered} 4 \mathrm{mV} \\ 15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ 80 \mathrm{~dB} \end{gathered}$ | I | $4 \mathrm{mV}$ | $\begin{gathered} 3 \mathrm{mV} \\ 50 \mu \mathrm{~V} /^{\circ} \mathrm{C} \end{gathered}$ | $\left\lvert\, \begin{gathered} 1 \mathrm{mV} \\ 25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ 80 \mathrm{~dB} \end{gathered}\right.$ |  | $\underset{25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}}{1 \mathrm{mV}}$ |
| 250 nA | I | $200 \mathrm{nA}$ | 1 | 200nA | 500 nA | 1 | 250 nA | 1 | 250 nA | 30pA | 115 pA | 1 | 15pA |
| $40 \mathrm{M} \Omega \mathrm{min}$ | I | $\begin{gathered} 50 \mathrm{M} \Omega \min \\ - \end{gathered}$ | I | $50 \mathrm{M} \Omega \mathrm{min}$ |  |  | $3 \mathrm{M} \Omega$ |  |  |  | $\begin{aligned} & 10^{10} \\ & 10^{12} \end{aligned}$ |  |  |
|  |  | $\begin{aligned} & - \\ & - \\ & - \end{aligned}$ |  |  |  |  | $\begin{aligned} & - \\ & \text { - } \end{aligned}$ |  |  |  | $5 \mu \mathrm{~V} \mathrm{p}-\mathrm{p}$ |  |  |
| $74 \mathrm{~dB} \mathrm{~min}{ }^{2}$ | I | $\begin{gathered} \pm 10 \mathrm{~V} \\ 80 \mathrm{~dB} \min ^{2} \\ \pm 15 \mathrm{~V} \end{gathered}$ | I | $80 \mathrm{~dB} \min ^{2}$ | 70 dB | I | $\begin{aligned} & \pm 10 \mathrm{~V} \\ & 80 \mathrm{~dB} \end{aligned}$ $-$ | 1 | 80dB | 70dB | $\begin{gathered} \pm 10 \mathrm{~V} \\ 80 \mathrm{~dB} \\ - \end{gathered}$ | 1 | 8dB |
|  | $\begin{aligned} & \pm(5 \text { to } 20) \mathrm{V} \\ & \pm 15 \mathrm{~V} @ 4 \mathrm{~mA} \end{aligned}$ |  |  |  | $\begin{gathered} \pm(5 \text { to } 20 \mathrm{~V}) \\ \pm 15 \mathrm{~V} \end{gathered}$ |  |  |  |  | $\begin{gathered} \pm(5 \text { to } 20) \mathrm{V} \\ \pm 15 \mathrm{~V} \end{gathered}$ |  |  |  |
| 0 to $+70^{\circ} \mathrm{C}$ | I | 0 to $+70^{\circ} \mathrm{C}$ |  | $55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 0 to $+70^{\circ} \mathrm{C}$ |  | 0 to $+70^{\circ} \mathrm{C}$ |  | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 0 to $+70^{\circ} \mathrm{C}$ | 0 to $+70^{\circ} \mathrm{C}$ |  | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
|  |  | TO-99 |  |  |  |  | TO-99 |  |  |  | TO-99 |  |  |
| $\begin{aligned} & \$ 11.50 \\ & \$ 11.50 \end{aligned}$ |  | $\begin{aligned} & \$ 18.75 \\ & \$ 18.75 \end{aligned}$ |  | $\$ 26.00$ $\$ 26.00$ | $\begin{aligned} & \$ 3.00 \\ & \$ 3.00 \end{aligned}$ |  | $\begin{aligned} & \$ 7.20 \\ & \$ 7.20 \end{aligned}$ |  | $\begin{aligned} & \$ 17.95 \\ & \$ 17.95 \end{aligned}$ | $\begin{aligned} & \$ 18.00 \\ & \$ 18.00 \end{aligned}$ | $\begin{aligned} & \$ 24.00 \\ & \$ 24.00 \end{aligned}$ |  | $\begin{aligned} & \$ 42.00 \\ & \$ 42.00 \end{aligned}$ |

## LOW VOLTAGE DRIFT-CHOPPER STABILIZED MODELS 234, 233, 260, 261, 231, 210, 230

## GENERAL DESCRIPTION

Chopper stabilized amplifiers employ modulation techniques for processing the "low frequency" components of a signal and an AC coupled amplifier for the higher frequencies. This chopping technique makes it possible to process wideband signals and yet achieve superior low drift and long term stability. Analog Devices, a pioneer in the development of encapsulated chopper stabilized amplifiers, offers designs with drifts between 0.1 to $2 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, low frequency voltage noise to $1 \mu \mathrm{~V}$ p-p and bias currents from 50 to 300 pA . Long term stability averages $1 \mu \mathrm{~V} /$ month. These amplifiers are widely accepted as the best choice when it is essential to maintain either low voltage offsets and bias currents versus time or against severe environmental changes, or whenever external offset adjustments are not possible or desirable.

## MODEL 234 J/K/L: LOWEST NOISE, WIDEBAND

 This latest inverting amplifier design from Analog Devices is virtually free of chopper spikes and is singled out as the industry's quietest, wide band chopper stabilized amplifier in a low cost module.Available in three drift selections ( $1,0.3$ and $0.1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ ), model 234 specifications include voltage noise of $11 / 2 \mu \mathrm{~V}$ p-p, current noise of $2 \mathrm{pA} \mathrm{p}-\mathrm{p}$, and 2.5 MHz bandwidth. Slew rate is $30 \mathrm{~V} / \mu \mathrm{sec}$. The wide bandwidth of 234 makes it especially useful for 16 -bit $\mathrm{D} / \mathrm{A}$ converters, high speed integrators as well as for low frequency applications including control systems, DVM input amplifier designs and other precision instrumentation. Attractively priced, its consistent unit-to-unit performance makes it an ideal choice for new OEM designs.

## MODEL $233 \mathrm{~J} / \mathrm{K} / \mathrm{L}$ : LOWEST COST, $0.1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$

The popular model 233 is a good choice for many low drift, high gain applications including precision integrators, instrument preamplifiers and null detectors as used to resolve microvolt error signals.
The combination of IC's and improved design techniques in this $0.4^{\prime \prime}$ high module results in good performance at low cost for OEM designs.
Typical specifications for this inverting amplifier include 500 kHz bandwidth, $0.25 \mathrm{~V} / \mu \mathrm{sec}$ slew rate, 50 pA bias current and $6 \mu \mathrm{~V}$ p-p noise in a 10 Hz bandwidth. It is available with three drift selections: $1 ; 0.3$; and $0.1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$.
MODEL $260 \mathrm{~J} / \mathrm{K}: 10^{9} \Omega$ NONINVERTING, $0.1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ Analog Devices pioneered in the development of new "chopper" amplifier designs to provide high input impedance without compromising the excellent low frequency characteristics of chopper type amplifiers. As embodied in the model 260 , this design is useful as a noninverting buffer amplifier for processing microvolt signals with minimal source loading errors. Typical specifications for the model 260 are $10^{9} \Omega$ input impedance, drift to $0.1 \mu \mathrm{~V} /^{\circ} \mathrm{C}$ and CMR of 110 dB at $\pm 1 \mathrm{~V}$.

## MODEL 261: GUARANTEED NOISE OF LESS THAN $1 \mu \mathrm{~V}$

The model 261 is a second generation design which typically provides a significant improvement in the noise and bandwidth characteristics of model 260 and other competitive models.


| Model | Lowest Cost General Purpose 233 K |
| :---: | :---: |
| Open Loop Gain DC Rated Load, V/V min | $10^{7}$ |
| Rated Output, min | $\pm 10 \mathrm{~V}$ @ 5 mA |
| Frequency Response <br> Unity Gain, Small Signal <br> Full Power Response, min Slewing Rate, min Overload Recovery | $\begin{gathered} 500 \mathrm{kHz} \\ 4 \mathrm{kHz} \\ 0.25 \mathrm{~V} / \mu_{\mathrm{S}} \\ --- \end{gathered}$ |
| Input Offset Voltage Initial, $25^{\circ} \mathrm{C}$ (Adj. to zero) max Avg. vs. Temp $\left(0^{\circ} \mathrm{C}\right.$ to $\left.70^{\circ} \mathrm{C}\right) \max$ vs. Supply Voltage vs. Time | $\pm 50 \mu \mathrm{~V}$ $\pm 20 \mu \mathrm{~V}$ $\pm 20 \mu \mathrm{~V}$ <br> $\pm 1.0$ $\pm 0.3$ $\pm 0.1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ <br>  $\pm 0.2 \mu \mathrm{~V} / \%$  <br>  $\pm 2 \mu \mathrm{~V} / \mathrm{mo}$.  |
| Input Bias Current Initial, $25^{\circ} \mathrm{C}$, max Avg. vs. Temp $\left(0^{\circ} \mathrm{C}\right.$ to $\left.70^{\circ} \mathrm{C}\right) \max$ | $\pm 2 \quad\left\|\begin{array}{c\|c} \pm 50 \mathrm{pA} \\ \pm 1\end{array}\right\| \pm 0.5 \mathrm{pA} /{ }^{\circ} \mathrm{C}$ |
| Input Impedance Differential Common Mode | $\begin{gathered} 600 \mathrm{k} \Omega \\ \mathrm{NA} \end{gathered}$ |
| Input Noise <br> Voltage, 0.01 to $1 \mathrm{~Hz}, \mathrm{p}-\mathrm{p}$ 0.1 to $10 \mathrm{~Hz}, \mathrm{p}-\mathrm{p}$ 10 Hz to 10 kHz , rms Current, 0.01 to 1 Hz , p-p 0.1 to $10 \mathrm{~Hz}, \mathrm{p}-\mathrm{p}$ | $2 \mu \mathrm{~V}$ <br> $6 \mu \mathrm{~V}$ <br> $6 \mu \mathrm{~V}$ <br> 3 pA <br> 6 pA |
| Input Voltage Range <br> Common Mode Voltage, min Common Mode Rejection Max Safe Differential Voltage | $\begin{gathered} \text { NA } \\ \text { NA } \\ \pm 15 \mathrm{~V} \end{gathered}$ |
| Power Supply Range (VDC) <br> Rated Specification (VDC) | $\begin{aligned} & \pm(12 \text { to } 18) \mathrm{V} \\ & \pm 15 \mathrm{~V} @ 5 \mathrm{~mA} \end{aligned}$ |
| Temperature Range <br> Operating, Rated Specifications | 0 to $+70^{\circ} \mathrm{C}$ |
| Package Outline Case Dimensions | $\begin{array}{lll}  & \mathrm{F}-3 \\ 1.5^{\prime \prime} \times 1.5^{\prime \prime} \times 0.4^{\prime \prime} \end{array}$ |
| Price $1-9$ $10-24$ | $\$ 46.50$ $\$ 56$ $\$ 77$ <br> $\$ 41$ $\$ 50$ $\$ 70$ |

(1) Model 260 inverting input bias current $\pm 3 \mathrm{nA}$, max.
(2) Model 261 inverting input bias current $\pm 10$ nA, max.

Operating at a higher carrier frequency, this noninverting design features extremely low noise, $0.4 \mu \mathrm{Vp}-\mathrm{p}$ in a 1 Hz bandwidth; low drift, $0.1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$; and an output that is virtually free of chopper spikes.

Model 261 also offers a solution to beat frequency problems caused by a low frequency carrier mixing with harmonics of the AC line. The carrier frequency on this design is nearly a decade higher than that of models previously available, thereby eliminating the possibility of any interaction with the line frequency or its harmonics.

## MODELS 210/211: 100V $\mu \mathrm{sec}$ WIDEBAND, $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$

Models 210/211 with 20 mA output, are inverting chopper stabilized amplifiers for that class of application requiring low drifi performance with good high frequency performance. This design will provide slew rates of $100 \mathrm{~V} / \mu \mathrm{sec}$ and 90 dB of loop gain at 10 kHz for improved wideband accuracy. Incorporating internal limiting circuitry, these amplifiers have exceptionally fast overload recovery, $(0.2 \mu \mathrm{sec})$ and stable input characteristics for high speed integrator and comparator designs. They are available in two drift selections (model $210,1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, model 211 , $2 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ ).

MODEL $230 \mathrm{~J} / \mathrm{K} / \mathrm{L}$ : LOWEST "DC" NOISE, INVERTING Model 230 offers the best "DC" noise performance of any chopper stabilized amplifier; in a DC to 1 Hz bandwidth, voltage noise is $0.5 \mu \mathrm{~V}$ p-p. The 1 Hz BW voltage and current noise are illustrated below. Three drift selections are available;
$\mathrm{L}\left(0.1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\right), \mathrm{K}\left(1 / 4 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\right)$ and $\mathrm{J}\left(1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\right)$. Typical specifications include; 500 kHz bandwidth, $0.2 \mathrm{~V} / \mu$ s slew rate and $15 \mu \mathrm{~V}$ initial offset voltage. Complete specifications are shown on page 65.

MODEL $231 \mathrm{~J} / \mathrm{K}: 25 \mathrm{~mA}$ OUTPUT, $0.1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$
Model 231, available in two drift selections ( $231 \mathrm{~J}, 0.25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ and $231 \mathrm{~K}, 0.1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ ) is an inverting chopper stabilized amplifier with increased output current capability ( 25 mA ). With stable 3 kHz full power response and low drift, it offers higher output without use of an additional booster stage for heavier load requirements.


## LOW VOLTAGE DRIFT-DIFFERENTIAL INPUT, HIGH CMR MODELS 52, 184, 153, I80, AD508, AD504

## GENERAL DESCRIPTION

These "chopperless" amplifiers with differential input feature high open loop gain, low drift and good CMR for improved linearity and gain accuracy as required for many low level signal applications. As single ended or differential amplifiers they may be used for precision comparators, transducer and bridge circuits, or in general, to precisely amplify and process low level signals of moderate bandwidths. They should be selected over single-ended choppers whenever chopper noise and spikes are objectionable in the circuit design.
Advanced circuit techniques, coupled with careful component selection and processing, have made possible economical amplifier designs which challenge the low voltage drift of the chopper amplifier. Amplifiers in this group use differential bipolar input stages to achieve offset voltages and drifts up to $100 \mu \mathrm{~V}$ and $1 / 4 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ respectively with good offset stability of $3 \mu \mathrm{~V} /$ month. These devices offer differential performance with input noise of $1 \mu \mathrm{~V}$ p-p and 100 dB of CMR at $\pm 10 \mathrm{~V}$. For comparison, chopper stability approaches $1 \mu \mathrm{~V} /$ month and are useful as single ended amplifiers only.

## MODEL 184 J/K/L: $0.25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, 100dB CMR

These low drift "chopperless" amplifiers challenge the low drift and long term stability of choppers while avoiding "chopper noise and spikes." Their low noise ( $1 \mu \mathrm{~V}$ p-p) and low drift (to $0.25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}, 184 \mathrm{~L}$ ) also make them the best choice among other amplifier types for processing low level transducer and bridge signals with source impedances up to $100 \mathrm{k} \Omega$. With internally trimmed offsets to $100 \mu \mathrm{~V}(184 \mathrm{~K}, \mathrm{~L})$, open loop gains of 110 dB and a CMR of 100 dB , the model 184 will provide good linearity and gain stability for singleended or differential amplifier configurations.

## MODEL 153 J/K: BATTERY POWERED, 70 $\mu$ A CURRENT DRAIN

Incorporating the best features of the "chopperless" class of differential amplifiers, the model 153 has a bipolar input stage and is designed to operate from $\pm 2.7 \mathrm{VDC}$ to $\pm 15 \mathrm{VDC}$ power supply voltages. Using two 2.7 VDC batteries, power consumption is held to $190 \mu \mathrm{~W}$ at $70 \mu \mathrm{~A}$ current drain while providing $2 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ drift, 94 dB of CMR and $2 \mu \mathrm{~V} \mathrm{rms}$ of wideband noise. The model 153 is a best choice for amplifying low level signals from source impedances to $100 \mathrm{k} \Omega$ where excellent power supply rejection is demanded such as in battery operated equipment.

## MODEL $180 \mathrm{~J} / \mathrm{K}$ : LOW BIAS CURRENT

These devices, with drifts of $1.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}(180 \mathrm{~J})$ and $0.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ ( 180 K ), are companion designs to model 184 but with reduced bias currents ( 4 nA versus 25 nA for 184). This sixfold improvement in bias current is achieved using current compensation techniques thereby permitting better current drift performance with higher source impedances (to $500 \mathrm{k} \Omega$ ). Package size is reduced below that of model 184 for critical space requirements.


MODEL 52 J/K: FET, $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, 100 dB CMR, 3pA Ib
Model 52 is the most accurate FET amplifier offered by Analog Devices. Featuring guaranteed low noise ( $1.5 \mu \mathrm{~V}$ p-p max), low drift ( $3 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ and $1 \mu \mathrm{~V} /^{\circ} \mathrm{C}$ max), low input current (3pA max), high gain ( $120 \mathrm{~dB}, \mathrm{~min}$ ) and high CMR (100dB, min), model 52 is an excellent choice for precision, low noise applications such as preamplifiers in A/D converters and DVM's. Model 52's differential input, high input impedance ( $10^{12} \Omega$ ) and excellent long-term stability ( $5 \mu \mathrm{~V} / \mathrm{mo}$ ) suggest precision buffer and autozero applications. The outstanding low noise and offset stability recommend model 52 as a replacement for chopper amplifiers.
In addition to the above salient features, offset voltage is extremely stable with power supply variations ( $2 \mu \mathrm{~V} / \%$ ) offering high immunity to supply voltage noise. Operation is specified over the 0 to $+70^{\circ} \mathrm{C}$ temperature range and two drift grades are available; model $52 \mathrm{~J}\left(3 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}, \max \right)$; model 52 K ( $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}, \max$ ).

## AD504 J/K/L/M/S: LOW COST, $0.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, $0.6 \mu \mathrm{~V}$ (p-p) MAX NOISE

The monolithic AD504 is an extremely low drift, low noise operational amplifier that is designed for high precision applications where moderate source impedances are used. A double integrator circuit concept combined with a precise thermally balanced layout achieves gain greater than $10^{6}$, offset voltage
drift below $0.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, maximum noise $(0.1 \mathrm{~Hz}$ to 10 Hz$)$ of $0.6 \mu \mathrm{~V}$ (p-p), bandwidth of 300 kHz , and slew rate of $0.12 \mathrm{~V} / \mu \mathrm{sec}$. The inputs and output are fully protected, and the amplifier will drive 1000 pF of load capacitance. This combination of performance characteristics makes the AD504 ideally suited for numerous low level applications in precision measurement, telemetry, and data acquisition. It is available in $\mathrm{J} / \mathrm{K} / \mathrm{L}\left(0\right.$ to $\left.+70^{\circ} \mathrm{C}\right)$ and $\mathrm{S}\left(-55^{\circ} \mathrm{C}\right.$ to $\left.+125^{\circ} \mathrm{C}\right)$ specification versions.

## AD508J: HIGHEST ACCURACY, LOW $\mathrm{I}_{\mathrm{b}}$, LOW DRIFT

Its combination of low drift $\left(3.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max \right)$, low input currents ( $5 \mathrm{nA} \max \mathrm{IOS}_{\mathrm{O}}, 25 \mathrm{nA} \max \mathrm{I}_{\mathrm{b}}$ ), and long term stability ( $10 \mu \mathrm{~V} /$ month max) make the AD508 operational amplifier an excellent choice for all applications requiring the utmost in precise, highest accuracy performance. Guaranteed parameters also include gain greater than 250,000 , PSRR less than $25 \mu \mathrm{~V} / \mathrm{V}$, CMRR above 94 dB , and VOS below 2.5 mV . Dynamic performance is more than adequate with a unity gain slew rate of $0.12 \mathrm{~V} / \mu \mathrm{sec}$ and bandwidth of 300 kHz . The outstanding long term stability of the AD508 is attained by subjecting $100 \%$ of the devices to special stabilization burn-in.

| Discrete |  |  | Microcircuit |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Low Offset Drift Low Bias Current 180 | Battery Powered General Purpose 153 | Lowest Noise FET 52 | Low Noise <br> Low Offset, Drift, Cost AD504 |  | Highest Accuracy Low $\mathrm{I}_{\mathrm{b}}, \mathrm{V}_{\text {OS }}$, Drift AD508 |
| J K | J K | J K | J K L | M S | J |
| 300,000 | 50,000 | 1,000,000 | 250,000\| 500,000 | 1,000,000 | 250,000 |
| $\pm 10 \mathrm{~V} @ 2.5 \mathrm{~mA}$ | $\pm 1 \mathrm{~V}^{1}$ @1mA | $\pm 10 \mathrm{~V} @ 5 \mathrm{~mA}$ | $\pm 10 \mathrm{~V} @ 5 \mathrm{~mA}$ |  | $\pm 10 \mathrm{V@} \mathrm{~m}^{\text {mA }}$ |
| $\begin{gathered} 1 \mathrm{MHz} \\ 10 \mathrm{kHz} \\ 0.6 \mathrm{~V} / \mu \mathrm{s} \\ 2.0 \mathrm{~ms} \end{gathered}$ | $\begin{gathered} 150 \mathrm{kHz} \\ 5 \mathrm{kHz}(\text { peak }) \\ 0.02 \mathrm{~V} / \mu \mathrm{s} \\ 2.0 \mathrm{~ms} \end{gathered}$ | $\begin{gathered} 500 \mathrm{kHz} \\ 4 \mathrm{kHz} \\ 0.25 \mathrm{~V} / \mu \mathrm{s} \\ 130 \mu \mathrm{~s} \end{gathered}$ | $\begin{gathered} 300 \mathrm{kHz} \\ 1.5 \mathrm{kHz} \text { typ } \\ 0.12 \mathrm{~V} / \mu \mathrm{s} \text { typ } \end{gathered}$ |  | $\begin{gathered} 300 \mathrm{kHz} \\ 1.5 \mathrm{kHz} \text { typ } \\ 0.12 \mathrm{~V} / \mu \mathrm{s} \text { typ } \\ -- \\ \hline \end{gathered}$ |
| $\begin{array}{c\|c}  \pm 250 \mu \mathrm{~V} & \pm 100 \mu \mathrm{~V} \\ \pm 1.5 & \pm 0.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ & \pm 2 \mu \mathrm{~V} / \% \\ \pm 5 \mu \mathrm{~V} / \mathrm{mo} . \end{array}$ | $\begin{array}{c\|c}  \pm 1.0 \mathrm{mV} & \pm 5.0 \end{array} \left\lvert\, \begin{gathered} \pm 2.25 \mathrm{mV} \\ \pm 1.0 \mu \mathrm{~V} / \% \\ \hline 5 \mu \mathrm{~V} / \mathrm{C} \end{gathered}\right.$ | $\begin{gathered} \pm 500 \mu \mathrm{~V}^{4} \\ \pm 3.0 \mid \pm 1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ \pm 2 \mu \mathrm{~V} / \% \\ \pm 5 \mu \mathrm{~V} / \mathrm{mo} \end{gathered}$ | $\begin{array}{ccc} \begin{array}{cc}  \pm 2.5 \mathrm{my} \\ \pm 5.0 \end{array}\left\|\begin{array}{cc}  \pm 1.5 \mathrm{mV} \\ \pm 3.0 \end{array}\right\| & \pm 1.0 & \\ & \pm 15 \mu \mathrm{~V} / \mathrm{mo} . & \pm 1.0 \end{array}$ | $\begin{aligned} & \quad \pm 0.5 \mathrm{mV} \\ & \pm 0.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}^{2} \quad \mid \quad \pm 1.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ & 0 \mu \mathrm{~V} / \% \mathrm{~m} . \\ & \pm 10 \mu \mathrm{~V} / \mathrm{mo} \end{aligned}$ | $\begin{gathered} \pm 2.5 \mathrm{mV} \\ \pm 3.0 \\ \pm 1.0 \mu \mathrm{~V} / \% \\ \pm 15 \end{gathered}$ |
| $\begin{array}{ll}  & \pm 4 \mathrm{nA} \\ \pm 0.1 & \mid \pm 0.05 \mathrm{nA} /{ }^{\circ} \mathrm{C} \end{array}$ | $\begin{gathered} \pm 3 \mathrm{nA} \\ \pm 0.1 \mathrm{nA} /{ }^{\circ} \mathrm{C} \end{gathered}$ | $\begin{aligned} & 0,-3 \mathrm{pA} \\ & 2 \mathrm{x} / 10^{\circ} \mathrm{C} \end{aligned}$ | $\pm 200 \mathrm{nA}{ }^{ \pm} \pm 100 \mathrm{nA}$ | $\begin{aligned} & \quad \pm 80 \mathrm{nA} \\ & 00 \mathrm{pA} /{ }^{\circ} \mathrm{C} \text { typ } \\ & \hline \end{aligned}$ | $\begin{aligned} & \pm 25 \mathrm{nA} \\ & \pm 100 \end{aligned}$ |
| $\begin{gathered} \pm 1 \mathrm{nA} \\ \pm 0.02 \mathrm{nA} /{ }^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} \pm 3 \mathrm{nA} \\ \pm 0.05 \mathrm{nA} /{ }^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} \pm 1 \mathrm{pA} \\ 2 \mathrm{x} / 10^{\circ} \mathrm{C} \end{gathered}$ | $\pm 40 \mathrm{nA}\| \pm 15 \mathrm{nA}\| \quad \pm 50$ | ppA $/{ }^{\circ} \mathrm{C}$ typ ${ }^{ \pm 10 \mathrm{nA}}$ | $\begin{gathered} \pm 5.0 \mathrm{nA} \\ \pm 14 \end{gathered}$ |
| $\begin{gathered} 2 \times 10^{6} \Omega \\ 10^{9} \Omega \end{gathered}$ | $\begin{gathered} 10^{6} \Omega \\ 2 \times 10^{8} \Omega \end{gathered}$ | $\begin{aligned} & 10^{12} / / 3.5 \mathrm{pF} \\ & 10^{12} / / 3.5 \mathrm{pF} \end{aligned}$ | $\begin{gathered} 10^{6} \Omega \\ 10^{8} \Omega \\| 4 \mathrm{pF} \end{gathered}$ |  | $\begin{gathered} 4 \times 10^{6} \Omega \\ 10^{8} \Omega \\| 4 \mathrm{pF} \\ \hline \end{gathered}$ |
| $\begin{aligned} & 1 \mu \mathrm{~V} \\ & 4 \mu \mathrm{~V} \\ & 50 \mathrm{pA} \end{aligned}$ | $\begin{aligned} & 1 \mu \mathrm{~V}^{1} \\ & 4 \mu \mathrm{~V} \\ & 10 \mathrm{pA} \end{aligned}$ | $\begin{gathered} 1.5 \mu \mathrm{~V} \max \\ 3.0 \mu \mathrm{~V} \max (10 \mathrm{~Hz} \text { to } 10 \mathrm{kHz}) \\ 0.1 \mathrm{pA} \end{gathered}$ | $(0.1$ to 10 Hz$) 1.0 \mu \mathrm{Vp}-\mathrm{p}$   <br> $(100 \mathrm{~Hz}) 10 \mathrm{nV} / \sqrt{\mathrm{Hz}} \mathrm{rms}$ $0.6 \mu \mathrm{Vp}-\mathrm{p}$ max <br> $(1 \mathrm{kHz}) 8 \mathrm{nV} / \sqrt{\mathrm{Hz}} \mathrm{rms}$ $1 \mu \mathrm{~V} \mathrm{p}-\mathrm{p}$ <br> $9 \mathrm{nV} / \sqrt{\mathrm{Hz}} \mathrm{rms} \max \max$ $10 \mathrm{nV} / \sqrt{\mathrm{Hz}} \mathrm{rms}$  <br> $8 \mathrm{nV} / \sqrt{\mathrm{Hz}} \mathrm{rms}$   |  | $(0.1$ to 10 Hz$) 1.0 \mu \mathrm{~V}$ $(100 \mathrm{~Hz}) 12 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ $(1 \mathrm{kHz}) 10 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ |
| $\begin{gathered} \pm 10 \mathrm{~V} \\ 100 \mathrm{~dB} \\ \pm 15 \mathrm{~V} \end{gathered}$ | $\begin{aligned} & \pm 1 \mathrm{~V}^{1} \\ & 94 \mathrm{~dB} \\ & \pm 10 \mathrm{~V} \end{aligned}$ | $\begin{gathered} \pm 10 \mathrm{~V} \\ 100 \mathrm{~dB} \text { min } \\ \pm 15 \mathrm{~V} \end{gathered}$ | $\begin{aligned} & \pm 10 \mathrm{~V} \\ & 120 \mathrm{~dB} \\ & \pm 15 \mathrm{~V} \end{aligned}$ |  | $\begin{aligned} & \pm 10 \mathrm{~V} \\ & 120 \mathrm{~dB} \\ & \pm 15 \mathrm{~V} \end{aligned}$ |
| $\begin{aligned} & \pm(10 \text { to } 18) \mathrm{V} \\ & \pm 15 \mathrm{~V} @ 5.5 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & \pm(2.5 \text { to } 18) \mathrm{V} \\ & \pm 2.7 \mathrm{~V} @ 70 \mu \mathrm{~A} \end{aligned}$ | $\begin{aligned} & \pm(9 \text { to } 18) \mathrm{V} \\ & \pm 15 @ 5 \mathrm{~mA} \end{aligned}$ | $\pm(5$ to 18$) \mathrm{V}$   <br> $\pm 15 \mathrm{~V} @ 1.5 \mathrm{~mA}$ I $\pm(5$ to 22$) \mathrm{V}$ |  | $\begin{aligned} & \pm(5 \text { to } 18) \mathrm{V} \\ & \pm 15 \mathrm{~V} @ 1.5 \mathrm{~mA} \end{aligned}$ |
| 0 to $+70^{\circ} \mathrm{C}$ | 0 to $+70^{\circ} \mathrm{C}$ | 0 to $+70^{\circ} \mathrm{C}$ | 0 to $+70^{\circ} \mathrm{C} \quad \mid-50^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{O}$ |  | 0 to $+70^{\circ} \mathrm{C}$ |
| $\frac{\mathrm{Q}-1}{} 1.125^{\prime \prime} \times 1.125^{\prime \prime} \times 0.62^{\prime \prime}$ | $1.5^{\prime \prime} \times \mathrm{F}^{\mathrm{F}-1} .$ | $1.12^{\prime \prime} \times 1.12^{\prime \prime} \times 0.4^{\prime \prime}$ | TO-99 |  | $\begin{gathered} \text { TO-99 } \\ \hline \end{gathered}$ |
| $\begin{array}{l\|l} \$ 77 & \$ 97 \\ \$ 70 & \$ 91 \end{array}$ | $\$ 54$ $\$ 65$ <br> $\$ 51$ $\$ 62$ | $\$ 42$ $\$ 49$ <br> $\$ 39$ $\$ 47$ | $\left.\begin{array}{lll\|l\|}\$ 11.20 \\ \$ 11.20\end{array}\right) \begin{aligned} & \$ 19.80 \\ & \$ 19.80\end{aligned}\left\|\begin{array}{l}\$ 28.00 \\ \$ 28.00\end{array}\right\|$ | $\$ 30.00$ $\$ 32.00$ <br> $\$ 30.00$ $\$ 32.00$ | $\begin{aligned} & \$ 21.20 \\ & \$ 21.20 \end{aligned}$ |

[^4]with external $1 \mathrm{k} \Omega$ potentiometer.

# ELECTROMETER-ULTRA LOW BIAS CURRENT MODELS 310, 3II, 4I, 42, AD523 

## GENERAL DESCRIPTION

Amplifiers with bias currents less than 1 pA are classified as suitable for electrometer use where frequency response and voltage drift are usually secondary requirements. Both varactor bridge and FET input designs are employed to achieve these bias currents ranging from one pico amp $\left(10^{-12} \mathrm{~A}\right)$ to ten femptoamps $\left(10^{-14} \mathrm{~A}\right)$.
Available with either inverting, noninverting or differential inputs, these amplifiers are used as current to voltage converters with high impedance transducers such as photomultiplier tubes, flame detectors, pH cells and radiation detectors. To minimize RFI and other noise pickup problems, the varactor modulated amplifiers, operating at 10 fA , are available with shielded cases.

## VARACTOR BRIDGE ELECTROMETERS

## MODEL 310 (INVERTING), MODEL 311 (NONINVERTING)

These operational amplifiers feature extremely low input bias currents and high input impedances. They are applicable to a wide range of electrometer applications which have been traditionally fulfilled using vacuum tube types. Because of varactor bridge inputs, the solid state models 310 and 311 are best suited for applications characterized by extremely high source impedance or where infinitesimal currents must be measured or amplified accurately. In principle, the varactor bridge amplifier design is similar to that of the vibrating reed electrometers (parametric), but with the inherent advantages of solid state circuitry.
Typical specifications for models 310 and 311 include open loop gain of $100 \mathrm{~dB}, 2 \mathrm{kHz}$ unity gain response, $0.4 \mathrm{~V} / \mathrm{msec}$ slew rate, initial bias current of $10^{-14} \mathrm{~A}$, with $10^{-15} \mathrm{~A} /{ }^{\circ} \mathrm{C}$ current stability, and low current and voltage noise of $10^{-15} \mathrm{~A}$ and $10 \mu \mathrm{~V}$ p-p ( 1 Hz bandwidth) respectively. Two voltage drift selections are available: $310 \mathrm{~J}, 311 \mathrm{~J}$ with $30 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, and $310 \mathrm{~K}, 311 \mathrm{~K}$ with $10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$. Each is housed in an aluminum enclosure for improved shielding.
Model 310, with inverting input only, is most appropriate for use with current source signals such as gas chromatographs flame detectors and photomultiplier tubes. It is also useful for precision long term integrators or where extremely wide dynamic current range is needed as in log compression amplifiers. Current to voltage converters may also be developed using a feedback resistor for setting the conversion scale factor.

Model 311 has a single noninverting input for measuring voltage from very high source impedances where bias currents would create substantial offset errors. Such sources include pH cells or stored capacitor charge as found in long term track and hold applications. Common mode rejection is 100 dB at $\pm 25 \mathrm{~V}$ with $10^{14} \Omega$ impedance to ground for reduced source loading errors.

## FET INPUT ELECTROMETERS

MODELS 41, 42, AD523 (MONOLITHIC): This family of FET input amplifiers fully complements the varactor bridge


designs for electrometer applications. Available in three package sizes, these designs provide high input impedance, sub-picoamp bias currents and improved bandwidth characteristics. They may be used single-ended or differentially for making low level current or voltage measurements from photo/ion current transducers, pH cells, photometers or, in general, where speed and low input capacitance are essential for accurate measurements at high impedance levels as found in automated test systems. Other applications include fast integrators, charge amplifiers, differentiators and long term integrators. In addition, these carrier-less units overcome certain RFI problems which may arise in extremely noisy environments using the varactor bridge modulator types.
Model $42 \mathrm{~J} / \mathrm{K} / \mathrm{L}$ : Undoubtedly one of the best values for OEM designs, this differential FET amplifier has 110 dB open loop gain, for improved closed loop accuracy, 1 MHz unity gain response and CMR of 66 dB at $\pm 1 \mathrm{~V}$ CMV. It is available in three current selections ranging from 0.35 pA to 75 fA . Each device features all hermetically sealed semiconductors, with monolithic front end, in a compact module for improved reliability and good thermal transient response.

Model $41 \mathrm{~J} / \mathrm{K} / \mathrm{L}$ : This device combines outstanding bias current and drift specifications with speed and full differential input capability for use in a broad range of electrometer and integrator applications as well as for wideband differential and buffer circuitry. Typical specifications include 50 kHz full power response, 94 dB CMR at $\pm 5 \mathrm{~V}$ ( 80 dB at $\pm 10 \mathrm{~V}$ ), 100 dB gain for improved closed loop performance, and three bias current and drift selections: $41 \mathrm{~J}, 0.5 \mathrm{pA}$ and $25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} ; 41 \mathrm{~K}, 0.25 \mathrm{pA}$ and $10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$; and $41 \mathrm{~L}, 0.15 \mathrm{pA}$ and $25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$. Special packaging techniques assure $10^{13}$ input impedance, free from internal current leakage paths, and a maximum 4 pA bias current rating at $+70^{\circ} \mathrm{C}$.
Model AD5 23: This unit is a very low bias current IC op amp. It features maximum steady-state bias currents (either input) as low as 0.25 pA , in a special low-leakage TO-99 metal can package that minimizes case leakage by utilizing a special guard pin and high resistivity glass insulation. The AD5 23 is short circuit protected and offset voltage nullable, and features drift of $15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, slew rate of $4 \mathrm{~V} / \mu \mathrm{sec}$, and large signal voltage gain of $25,000 \mathrm{~V} / \mathrm{V}$. It is available in $\mathrm{J}, \mathrm{K}, \mathrm{L}\left(0\right.$ to $\left.+70^{\circ} \mathrm{C}\right)$ and $\mathrm{S}\left(-55^{\circ} \mathrm{C}\right.$ to $\left.+125^{\circ} \mathrm{C}\right)$ specification versions. (See also Linear IC Section).


# HIGH OUTPUT VOLTAGE, CURRENT MODELS BIOO, 50, 51, 163, 165, 171, AD512 

GENERAL DESCRIPTION
Amplifiers in this category are unique with respect to their output voltage and/or current capability. In general, amplifiers offered here have bipolar or FET inputs with output voltage swings of $\pm 20$ volts or output currents to $\pm 100 \mathrm{~mA}$. These amplifiers may be used to achieve higher output voltage or current swings, or as boosters for op amps. Typical applications include galvanometer amplifiers, audio amplifiers, deflection amplifier drives, voltage or current regulators and sonar transducer drives.

MODEL B100: 100 mA OP AMP BOOSTER
As a unity gain current booster, the B100 will deliver up to 100 mA at $\pm 10$ volts output and operate in a closed loop configuration with an op amp. Its 1 MHz full power response rolls off at a stable 6 dB per octave making it suitable for use with op amps designed to have crossover frequencies up to 1 MHz . B100, with short circuit protected output, is useful as a power booster for instrument servo loops, audio systems, galvanometer drivers, and wherever clean power must be delivered to loads at moderate bandwidths, to 1 MHz .

MODEL $50 \mathrm{~J} / \mathrm{K}$ : WIDEBAND 100mA DRIVER AMPLIFIER
The model 50, an extremely fast amplifier, should be considered for higher current outputs if settling time, slew rate or bandwidth are critical. This differential FET op amp will deliver 100 mA at $\pm 10$ volts, up to 8 MHz , for a wide range of high frequency designs, including boosters and driver stages as used in CRT deflection amplifiers. Typical specifications include 86 dB open loop gain, 1 nA bias, 80 ns settling to $0.1 \%$, CMR of 72 dB at $\pm 10 \mathrm{~V}$ and two drift selections: $50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}(\mathrm{J})$ and $15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}(\mathrm{K})$.
MODEL $51 \mathrm{~A} / \mathrm{B}$ : WIDEBAND, 100 mA , MIL-TYPE
Model 51 with all hermetically sealed semiconductors is recommended to upgrade models 46 and 50 for wider temperature range applications as required in military grade circuits. Settling time is 140 ns maximum to $0.1 \%$ and two drift selections are available; $50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}(51 \mathrm{~A})$ and $20 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}(51 \mathrm{~B})$. Other specifications are similar to model $50 \mathrm{~J} / \mathrm{K}$.


| SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ and $\pm 15 \mathrm{VDC}$ power supply unless otherwise noted.) | 100 mA Booster Lowest Cost B100 | 20 V Output 20 mA , High Gain 163 |
| :---: | :---: | :---: |
| Model |  | A K |
| Open Loop Gain DC Rated Load, V/V, min | 0.85 | 500,000 |
| Rated Output, min | $\pm 10 \mathrm{~V} @ 100 \mathrm{~mA}$ | $\pm 20 \mathrm{~V} @ 20 \mathrm{~mA}$ |
| Frequency Response <br> Unity Gain, Small Signal <br> Full Power Response, min Slewing Rate, min Overload Recovery | $\begin{gathered} 1 \mathrm{MHz} \\ 65 \mathrm{~V} / \mu \mathrm{s} \end{gathered}$ | 1.5 MHz <br> 50 kHz <br> $6 \mathrm{~V} / \mu \mathrm{s}$ <br> $0.5 \mu \mathrm{~s}$ |
| Input Offset Voltage Initial, $25^{\circ} \mathrm{C}$, (Adj. to zero) <br> Avg. vs. Temp, max vs. Supply Voltage vs. Time | $\begin{gathered} \pm 200 \mathrm{mV} \text { (no adj.) } \\ \pm 1 \mathrm{mV} ?^{\circ} \mathrm{C} \end{gathered}$ |  |
| Input Bias Current Initial, $25^{\circ} \mathrm{C}$, max Avg. vs. Temp, max | $\pm 500 \mathrm{nA}$ | $\pm 0.6 \quad+35 \mathrm{nA}$ |
| Input Difference Current Initial, $25^{\circ} \mathrm{C}$ <br> Avg. vs. Temp | NA | $\pm 0.1 \begin{array}{lll} \\ & \pm 3 \mathrm{nA} \\ \text { \| }\end{array}$ |
| Input Impedance Differential Common Mode | $\begin{gathered} 9 \times 10^{3} \Omega \\ \text { NA } \end{gathered}$ | $\begin{aligned} & 10^{6} \Omega \\ & 10^{9} \Omega \end{aligned}$ |
|  | $\overline{\mathrm{NA}}$ | $\begin{aligned} & 1 \mu \mathrm{~V} \\ & 2 \mu \mathrm{~V} \\ & 20 \mathrm{pA} \\ & \hline \end{aligned}$ |
| Input Voltage Range Common Mode Voltage, min Common Mode Rejection Max Safe Differential Voltage | $\begin{gathered} \text { NA } \\ \text { NA } \\ \pm 15 \mathrm{~V} \\ \hline \end{gathered}$ | $\begin{aligned} & \pm 20 \mathrm{~V} \\ & 86 \mathrm{~dB} \\ & \pm 40 \mathrm{~V} \end{aligned}$ |
| Power Supply Range (VDC) Rated Specification (VDC) | $\begin{gathered} \pm(14 \text { to } 16) \mathrm{V} \\ \pm 15 \mathrm{~V} @ 8 \mathrm{~mA} \end{gathered}$ | $\begin{aligned} & \pm(22 \text { to } 26) \mathrm{V} \\ & \pm 24 \mathrm{~V} @ 2 \mathrm{~mA} \end{aligned}$ |
| Temperature Range <br> Operating, Rated Specifications | -25 to $+85^{\circ} \mathrm{C}$ | -25 to $+85{ }^{\circ} \mathrm{C}$ 0 to $+70^{\circ} \mathrm{C}$ |
| Package Outline Case Dimensions | $\begin{gathered} \mathrm{Q}^{-3} \\ 1.1^{\prime \prime} \times 1.1^{\prime \prime} \times 0.62^{\prime \prime} \end{gathered}$ | $$ |
| Price $1-9$ $10-24$ | $\begin{array}{r} \$ 33.50 \\ \$ 32.50 \end{array}$ | $\$ 44$ $\$ 55$ <br> $\$ 42$ $\$ 52$ |

(1) 10 kHz and $1.2 \mathrm{~V} / \mu \mathrm{s}$ for non-inverting operation.
(2) With fixed $499 \Omega$ external trim.
(3) With $24.9 \mathrm{k} \Omega$ external trim.

MODEL 163 A/K: 20 VOLT/20mA ECONOMY
The model 163 offers good performance at a low cost for designs requiring higher output capability of $\pm 20$ volts at 20 mA . This differential amplifier with bipolar input stage may be used in most general purpose designs with source impedances up to $10 \mathrm{k} \Omega$ for best performance.

## MODEL 165 A/K: 20V/5mA ECONOMY

Model 165, a companion design to model 163, has reduced 5 mA output at $\pm 20$ volts with equivalent performance at even lower costs. Two offset drift selections are available: $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ (K) and $20 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ (A).

MODEL 171: $\pm 20 \mathrm{~V}$ TO $\pm 150 \mathrm{~V}$ FET AMPLIFIER
Model 171 is an extremely versatile differential FET amplifier featuring output voltages to within 10 V of the supplies, for supplies ranging from $\pm 20 \mathrm{~V}$ to $\pm 150 \mathrm{~V}$. Asymmetrical supplies may also be used with combinations of $-0 \mathrm{~V},+300 \mathrm{~V}$, or -300 V , +0 V , or any combination of + and - supplies where the difference between supplies is held to less than 300 V .
This design also features low drift of $15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ for 171 K , $7 \mu \mathrm{~V} / \mathrm{V}$ of power supply rejection and common mode rejection of greater than 100 dB for common mode voltages to within 10 V of either supply.

## AD512 K/S: HIGH CURRENT

Models AD512K and AD512S are monolithic operational amplifiers specifically designed for high output current capability. High efficiency output transistors, thermally balanced chip design and precise short circuit current control insure against gain degradation at high current levels and temperature extremes. Typical specifications include 12 mA at $\pm 10 \mathrm{~V}$ output from 0 to $+70^{\circ} \mathrm{C}, 20 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ drift, 5 nA bias current, 90 dB CMR and $0.5 \mathrm{~V} / \mu \mathrm{sec}$ slew rate at full load. The AD512S is designed to operate from $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$. (Also see Linear IC Section).


# INSTRUMENTATION AMPLIFIERS MODELS 606, 603, 605, 602, 6IO, AD520 

## GENERAL DESCRIPTION

The instrumentation amplifier is a commited gain amplifier containing precision feedback networks. Its excellent linearity and noise rejection capability make it a natural choice for extracting and amplifying low level signals in the presence of high common mode noise voltages. These devices are commonly used as transducer amplifiers for thermocouples, strain gauge bridges, current shunts, biological amplifiers, or simply as preamplifiers for processing small differential signals superimposed on common mode voltages.

MODEL $606 \mathrm{~J} / \mathrm{K} / \mathrm{L} / \mathrm{M}$ : LOW NOISE, $114 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}, 100 \mathrm{kHz}$ BW The model 606 combines the best attributes of fast instrumentation amplifier designs with the accuracy of slower models to produce the industry's fastest high accuracy module. Featuring virtually constant bandwidth over a gain range of 1 to $10,000 \mathrm{~V} / \mathrm{V}$, model 606 is available in four low drift grades; $1 / 4$, $1 / 2,1$ and $2 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max$. (RTI @ $\mathrm{G}=1000 \mathrm{~V} / \mathrm{V}$ ). Gain nonlinearity error is $0.002 \% \max (\mathrm{G}=100 \mathrm{~V} / \mathrm{V})$ and gain temperature stability is $15 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \max (\mathrm{G}=100 \mathrm{~V} / \mathrm{V})$.
The excellent wide bandwidth ( $100 \mathrm{kHz}, \mathrm{G}=100 \mathrm{~V} / \mathrm{V}$ ) and fast settling performance ( $30 \mu \mathrm{~s}, \pm 0.1 \%$ ), suggest high speed data acquisition systems. Full power response ( 12 kHz ) is independent of gain.
Voltage noise is specified as less than $1 \mu \mathrm{~V}$ p-p ( 10 Hz BW, RTI, $\mathrm{G}=1000 \mathrm{~V} / \mathrm{V}$ ) making model 606 the first instrumentation amplifier on the market to offer guaranteed low noise.
Model 606 may be applied as a high impedance ( $10^{9} \Omega$ ) differential preamplifier to accurately recover low millivolt signals carried on noisy lines at high CMV. Common mode rejection is 120 dB with a balanced source and is guaranteed at 90 dB with a $1 \mathrm{k} \Omega$ source imbalance.

## MODEL 605 J/K/L: LOW DRIFT, HIGH CMR

For moderate bandwidth applications requiring excellent drift, gain linearity and stability, the model 605 is a top performer when used with source impedance up to $10 \mathrm{k} \Omega$. This design requires one gain setting resistor for operation and includes output remote sense terminal and output reference adjust terminal. Typical specifications are $0.01 \%$ gain nonlinearity, 1 to $1000 \mathrm{~V} / \mathrm{V}$ gain range, 94 dB CMR at $\mathrm{G}=100 \mathrm{~V} / \mathrm{V}, 100_{\mathrm{n}} \mathrm{A}$ bias current and three RTI drift selections: $1 / 2 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}(\mathrm{L}), 1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ (K), and $3 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}(\mathrm{J})$ at $1000 \mathrm{~V} / \mathrm{V}$ gain. Its low RTO drift, $50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}(\mathrm{L})$ and $0.002 \%$ max gain nonlinearity ( $\mathrm{G}=1$ to $10 \mathrm{~V} / \mathrm{V}$ ), makes model 605 especially attractive for low gain applications.

MODEL $603 \mathrm{~J} / \mathrm{K} / \mathrm{L}:$ GENERAL PURPOSE, ECONOMY FET This FET input design features high input impedance and low bias current to meet most general purpose applications. Model 603 is available in three RTI drift selections $-50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}(\mathrm{J})$; $15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}(\mathrm{K})$; and $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}(\mathrm{L})$. Key specifications include: $0.2 \%$ gain nonlinearity; 1 MHz bandwidth and $40 \mu \mathrm{sec}$ settling time to $0.1 \%$, all at $1 \mathrm{~V} / \mathrm{V}$-gain; RTO drift of $500 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, and operation from 12 to 20VDC dual power supplies.


| (Specifications typical @ $+25^{\circ} \mathrm{C}$ and $\pm 15 \mathrm{VDC}$ power supply unless otherwise noted.) | Economy General Purpose FET 603 |
| :---: | :---: |
| Model | K L |
| Gain <br> Range <br> Formula <br> Deviation From Formula, max <br> vs. Temp, max <br> vs. Time <br> Nonlinearity, max $(G=100)$ | $\begin{gathered} 1 \text { to } 2000 \\ \mathrm{G}=10^{5} / \mathrm{Rg} \\ \pm 3.0 \% \\ \pm 50 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ \pm 0.2 \% / \mathrm{mo} . \\ \pm 0.2 \% \end{gathered}$ |
| Rated Output, min | $\pm 10 \mathrm{~V} @ 5 \mathrm{~mA}$ |
| Frequency Response <br> Unity Gain, Small Signal, (-3dB) $\mathrm{G}=1$ $G=1000$ <br> Full Power Response, min <br> Slew Rate <br> Unity Gain Settling Time to 0.1\% | $\begin{gathered} 1.0 \mathrm{MHz} \\ 1.0 \mathrm{kHz} \\ 10 \mathrm{kHz} \\ 2 \mathrm{~V} / \mu \mathrm{s} \\ 40 \mu \mathrm{~s}(\mathrm{G}=1) \end{gathered}$ |
|  | $\begin{array}{lc}  & \text { Adjust to } 0 \\ & \pm 0.5 \mathrm{mV} /{ }^{\circ} \mathrm{C} \\ \pm 50 \quad \mid \quad \pm \\ & \pm 15 \\ & \pm 1.0 \mathrm{mV} / \% \\ & \pm 3.5 \mu \mathrm{~V} / \% \\ \hline \end{array}$ |
| Input Bias Current Initial, $25^{\circ} \mathrm{C}$ vs. Temp | $\begin{array}{ll} 0,-50 \mathrm{pA} \mid & \begin{array}{l} 0,-20 \mathrm{pA} \mid 0,-20 \mathrm{pA} \\ 2 \mathrm{x} / 10^{\circ} \mathrm{C} \end{array} \end{array}$ |
| Input Difference Current Initial, $25^{\circ} \mathrm{C}$ vs. Temp. | $\begin{gathered} \pm 10 \mathrm{pA} \\ 2 \mathrm{x} / 10^{\circ} \mathrm{C} \end{gathered}$ |
| Input Impedance Differential Common Mode | $\begin{aligned} & 10^{12} \Omega / / 5 \mathrm{pF} \\ & 10^{12} \Omega / / 5 \mathrm{pF} \end{aligned}$ |
| Noise Referred to Input <br> Voltage Noise, 0.01 to $1 \mathrm{~Hz}, \mathrm{p}-\mathrm{p}$ $\begin{aligned} & G=1 \\ & G=1000 \end{aligned}$ <br> Voltage Noise, 10 Hz to 10 kHz , rms $\mathrm{G}=1$ | $\begin{array}{r} 100 \mu \mathrm{~V} \\ 2.0 \mu \mathrm{~V} \\ 80 \mu \mathrm{~V} \\ \hline \end{array}$ |
| Input Voltage Range Linear Differential Input Max Differential Input Common Mode, min CMR @ $\pm 10 \mathrm{~V}$, DC to 60 Hz , min ( $1 \mathrm{k} \Omega$ Imbalance) $G=1$ $G=1000$ | $\begin{gathered} \pm 10 \mathrm{~V} \\ \pm V_{\mathrm{s}} \\ \pm \mathrm{V}_{\mathrm{S}} \\ \text { 70dB @ } \pm 8 \mathrm{~V} \text { (typ) } \\ 80 \mathrm{~dB} \text { (typ) } \\ \hline \end{gathered}$ |
| Reference Terminal $\mathrm{R}_{\text {in }}$ Output Offset Range Gain <br> Bias Current | $\begin{gathered} 10^{7} \Omega \\ \pm 10 \mathrm{~V} \\ 1 \pm 0.03 \\ +0,-2 \mu \mathrm{~A} \\ \hline \end{gathered}$ |
| Power Supply Range, $\pm \mathrm{V}_{\mathbf{s}}$ (VDC) Operating, Rated Specifications (VDC) | $\begin{gathered} \pm(12 \text { to } 20) \mathrm{V} \\ \pm 15 \mathrm{~V} @ 7 \mathrm{~mA} \end{gathered}$ |
| Temperature Range Operating, Rated Specifications | 0 to $+70^{\circ} \mathrm{C}$ |
| Package Outline Case Dimensions | $\begin{gathered} \text { FA-5 } \\ 1.5^{\prime \prime} \times 1.5^{\prime \prime} \times 0.62^{\prime \prime} \end{gathered}$ |
| Price <br> 1-9 <br> 10-24 | $\$ 43$ $\$ 49.50$ $\$ 55$ <br> $\$ 40.50$ $\$ 47.50$ $\$ 49.50$ |

MODEL 602 J/K: FIXED GAIN, LOW DRIFT
Model 602 is internally trimmed for gain accuracy of $0.05 \%$ at gains of $10 \mathrm{~V} / \mathrm{V}$ and $100 \mathrm{~V} / \mathrm{V}$ with drift selections of $10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ and $2 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$.

## AD520 J/K/S: LOW DRIFT, MONOLITHIC

The model AD520 is a monolithic instrumentation amplifier which incorporates many features found in more expensive modular type designs. These include: two external resistors for setting gain from 1 to $1000 \mathrm{~V} / \mathrm{V}$; remote output sense terminal for current amplifier applications; and reference adjustment terminal for setting output level up to $\pm 10 \mathrm{~V}$ independent of gain. Other characteristics include $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ RTI drift (AD520 $\mathrm{K} / \mathrm{S}$ ); 106 dB CMR ( $1 \mathrm{k} \Omega$ imbalance), all at Gain $=1000 \mathrm{~V} / \mathrm{V}$; 40nA bias; and $0.02 \%$ gain nonlinearity.

MODEL 610J/K/L: GENERAL PURPOSE, LOW DRIFT
Model 610 is a general purpose bipolar design that is priced at the economy level and offers performance consistent with 10 bit systems. It's RTI drift of 3,1 or $1 / 2 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max, nonlinearity of $0.02 \%$ max, and noise performance at 10 kHz of $2.0 \mu \mathrm{~V} \mathrm{rms}$ max, qualify for all but the most demanding of applications (see model 606).
Gain of model 610 is externally programmed over a 10,000 to 1 range by a single resistor. Programming terminals are also provided for reference adjustment and remote output sensing.


[^5]
# MEDICAL AND INDUSTRIAL ISOLATION AMPS MODELS 272, 273, 274, 276, 279, 282, 283, 280, 280-I 

## GENERAL DESCRIPTION

Analog Devices offers a series of high quality unity gain and adjustable gain DC coupled isolation amplifiers for a wide range of medical, industrial and general purpose instrumentation applications. Incorporating a "patent applied for" carrier isolation technique, these models offer extremely high CMR and CMV ratings for operation in extremely noisy environments commonly found in industry or as required for processing low level biologic or transducer signal levels.
Offering galvanic ground isolation and low stray coupling capacitance ( $<10 \mathrm{pF}$ ) between input and output grounds, these compact designs achieve high CMR ( 126 dB @ 60 Hz ) and CMV (to $\pm 7.5 \mathrm{kV}$ ) combined with low input noise levels (to $8 \mu \mathrm{~V}$ p-p) and 4 kHz signal bandwidths. A representative isolator block diagram may be found in the section "Applying the Isolation Amplifier", page 27 and page 55.

## MEDICAL APPLICATIONS

Analog Devices' isolation amplifiers are ideal for medical applications where it is important to isolate hospital patients from potentially lethal ( $10 \mu \mathrm{~A}$ rms @ 120 VAC ) ground fault currents. All single channel models offer "fail safe" amplifier designs limiting input currents to less than $10 \mu \mathrm{~A}$ to improve on the existing patient/equipment safety specifications of regulatory agencies such as Underwriters' Laboratories, AAMI and the American Heart Association. All designs limit ground fault currents to $1.2 \mu \mathrm{~A}$ @ 117 VAC @ 60 Hz . When used for ECG, blood pressure or other critical direct patient monitoring applications, these amplifiers are designed to eliminate microshock hazards from ground fault currents and from internal amplifier failure modes.

## INDUSTRIAL APPLICATIONS

For critical nuclear and industrial control applications, the high isolation features of Analog Devices' proprietary design assure operator and equipment safety while transmitting millivolt signals in the presence of up to $\pm 7.5 \mathrm{kV}$ of common mode voltage. Another feature of this product group is its ability to provide good performance in the presence of high levels of EMI.

## MULTICHANNEL APPLICATIONS

For multichannel medical and industrial systems, synchronized oscillator drive capability is incorporated in two basic designs offering extremely high channel-to-channel separation. This feature is desired for eliminating interchannel "cross talk" which may arise when "carrier" beat frequency interference occurs. Two and three channel isolators with common guard shield exist with isolated $\pm 3 \mathrm{~V}$ and $\pm 6 \mathrm{~V}$ auxiliary power outputs for operating additional isolated circuitry. Up to 200 isolation channels with individual guarding may also be developed for systems applications using model 279 J .

## AMPLIFIER SELECTION GUIDE

The complete line of isolation amplifiers presented here have many key features in common making them desirable for both medical or industrial applications. The distinguishing characteristics which set these products apart relate primarily to input signal swing and noise levels as well as the degree of amplifier and interface fault protection offered by the high impedance input resistors.

## Medical Versus Industrial

Medical amplifiers require up to $\pm 1 / 2 \mathrm{~V}$ input signal swing and the lowest noise possible while offering 5 kV defibrillator protection. Additionally, the patient must be protected against leakage currents and amplifier fault currents exceeding $10 \mu \mathrm{~A}$ rms.
Industrial amplifier requirements should provide good signal processing characteristics in the presence of extreme common mode noise and EMI hash. Adjustable gain, improved linearity, larger dynamic range and usually the highest degree of CMV rating are desirable features.
Most Analog Devices amplifiers cover these requirements adequately and may be used for both medical and industrial applications. In the following sections, however, Analog Devices has grouped products for customers' convenience using these criteria.
current flows under these conditions．Normally，a differential amplifier has two independent bias currents，one each at the inverting and non－inverting inputs，and requires a return path for these currents．

Unlike the ordinary instrumentation amplifier，which depends upon precise component matching for its common－mode rejec－ tion，the isolation amplifier exploits its low－leakage transformer coupling to obtain a distinct interruption in the common－mode circuit．This makes it inherently immune to common－mode signals and highly insensitive to input imbalances．
In point of fact，only the unavoidable leakage capacitance between the shielded input section and the rest of the circuitry keeps the common－mode rejection ratio from being infinite． The reason is that the leakage paths are the only mechanism through which the common－mode input can affect the amplif－ ier＇s output．

Because the FET input preamplifier operates single－ended（non－ inverting），only a difference input current flows；no net bias

## HOW IT WORKS

## MODEL 272J：UNITY GAIN ISOLATOR

The remarkable performance of Analog Devices isolation ampli－ fiers（complete specifications are shown on page 60）derive from the carrier isolation technique＊，which is used to transfer both signals and power between the amplifier＇s guarded input stage and the rest of the circuitry．Because of the high carrier frequency（e．g． 125 kHz ，model 272 J ），the amplifier is able to provide a small signal bandwidth of 2 kHz and a full power response up to 200 Hz ．
The high－value resistor， $\mathrm{R}_{\mathrm{L}}$ limits the differential fault current in case one of the input FETs fails．It also keeps the differen－ tial input resistance high during periods of input－amplifier saturation．This series resistor gives the amplifier its 7500 －volt differential input rating，making it independent of linear opera－ tion of the input circuitry．

# MEDICAL ISOLATION AMPLIFIERS MODELS 273J, 273K, 276J, 282J, 283J 

## MEDICAL ISOLATORS: GENERAL DESCRIPTION

The medical isolator product line consists of five models. Models $273 \mathrm{~J}, 273 \mathrm{~K}$ and 276 J * are single channel epoxy encapsulated modules available with unity gain ( $273 \mathrm{~J}, 273 \mathrm{~K}$ ) or gain of $3 \mathrm{~V} / \mathrm{V}(276 \mathrm{~J}$ ). Models 282 J and 283 J are open card isolators designed for two and three channel ECG applications (see block diagram, Figure 3). Featuring low cost per channel, models 282J and 283 J use an external guard shield for high CMR performance and offer isolated $\pm 6 \mathrm{~V}$ and $\pm 3 \mathrm{~V}$ outputs for customer use in powering transducers, bridge networks or additional circuitry requiring isolation. All medical isolators use patent applied for carrier modulation techniques with transformer coupling for superior reliability and low cost. Small signal response is from DC to 4 kHz (models 273 J , 273 K ) and DC to 1 kHz (models $276 \mathrm{~J}, 282 \mathrm{~J}, 283 \mathrm{~J}$ ), with full power response to 200 Hz (all models).

## PATIENT AND EQUIPMENT SAFETY

Analog Devices medical isolators are well suited for a wide range of medical applications not only because of their overall performance features, but also because they are safe to use in such applications. Safety is a primary concern to medical users; the patient must be protected from the equipment (e.g., input leakage current) and the equipment itself must be protected from the environment (e.g., 5 kV defibrillator pulse). Fault currents for all medical isolators are limited to $10 \mu \mathrm{~A}$ under

[^6]amplifier failure. Ground leakage currents are limited to $1.2 \mu \mathrm{~A}$, rms @ 117 VAC 60 Hz between input and output and to the power common (see Figure 1). Leakage currents are unaffected by the power on or off conditions of the amplifier. All single channel isolators including models $272 \mathrm{~J}, 273 \mathrm{~J}, 273 \mathrm{~K}$, 276 J and 279 J will repeatedly support a 5 kV defibrillator pulse from input to output or directly across the input leads. Models 282J, 283J will support 220 V rms differentially for each input channel and 117 V rms between each channel.

## DUAL CMR FEATURE AIDS ECG

An important application of medical isolators is in cardiac monitoring where the heart signals can be masked by muscle noise, electrochemical noise, residual electrode voltages and 60 Hz power line pickup. An amplifier designed for high performance cardiac monitoring must provide the utmost in CMR in the DC to 100 Hz band, handle substantial source resistance imbalance (to $5 \mathrm{k} \Omega$ ) and separate a few millivolts of heartbeat signal from 50 to 500 mV of residual electrode potential.
An especially demanding ECG requirement is that of fetal heart monitoring. In fetal heartbeat monitoring (see Figure 2), the low input noise of models $273 \mathrm{~J}, 273 \mathrm{~K}$ and 276 J and the dual CMR capability of Analog Devices' isolators is exploited to extract the fetal ECG signals. The separation between the mother's and the baby's heartbeat is accomplished by the 60 dB of CMR between the input electrodes and guard, while the 115 dB of CMR from input to output ground screens out 60 Hz pickup and other external interference.


Figure 1. Patient and Equipment Safety Test

## SINGLE CHANNEL DESIGNS

OEM CHOICE, FULL ECG PERFORMANCE (MODEL 276J)
Pin compatible with other isolator models, this new design has been optimized for lowest cost without sacrificing critical design and safety features required in medical applications. Using a fully protected bipolar input stage, model 276 J combines improved $8 \mu \mathrm{~V}$ p-p input noise performance $(100 \mathrm{~Hz} \mathrm{BW})$ with full 5 kV defibrillator protection across its inputs, and input to output. Amplifier and ground fault currents are limited to $10 \mu \mathrm{Arms}$ for patient safety.
Other features include 5 nA bias current, $\pm 1 / 2 \mathrm{~V}$ input swing, $3 \mathrm{~V} / \mathrm{V}$ gain, $\pm 1.7 \mathrm{~V}$ output range, CMR of $115 \mathrm{~dB} @ 60 \mathrm{~Hz}$ and $5 \mathrm{k} \Omega$ source imbalance, and a CMV of 5 kV . This cost effective design should be considered for all new OEM applications for medical instruments.

## LOWEST NOISE, FET INPUT DEFIBRILLATOR PROTECTED (MODEL 273J)

This unity gain isolator with FET input now combines full 5 kV defibrillator protection with $10 \mu \mathrm{~V}$ p-p input noise levels improving over a previous specification of 400 V protection. Pin compatible with model 273 K and 272 J , model 273 J may be used to upgrade noise performance of designs now using 272 J and 273 K with FET input. Where lower noise is required and a bipolar input is adequate with reduced dynamic range, model 276 should be considered for the design. Key specifications for model 273 J include 115 dB CMR @ 60 Hz ( $5 \mathrm{k} \Omega$ source imbalance), 5 kV full defibrillator protection, max amplifier fail safe current of $10 \mu \mathrm{~A}$ and $1.2 \mu \mathrm{~A} \mathrm{rms}$ of leakage current at $115 \mathrm{VAC} @ 60 \mathrm{~Hz}$. Dynamic range is $\pm 3 \mathrm{~V}$, bandwidth, 4 kHz and input bias current $50 \mathrm{pA}\left(10^{12} \Omega\right.$ input impedance). Single polarity power supply voltage of +12 to +28 VDC is required making it suitable for portable applications.

UNITY GAIN, HIGHEST INPUT PROTECTION (MODEL 273 K) The 273 K should be considered for all medical designs requiring maximum input protection and low noise performance. This unity gain amplifier is electrically and mechanically inter-
changeable with model 273J and differs only in the value of input safety resistor. Referring to the block diagram (page 27), model 273 K uses a $2 \mathrm{M} \Omega$ input resistor versus a $1 \mathrm{M} \Omega$ for model 273 J . This change has the net effect of improving differential input protection to $\pm 7.5 \mathrm{kV}$ at a slight increase of noise. Noise levels are typically $14 \mu \mathrm{~V}$ p-p in a 100 Hz bandwidth.

## MULTICHANNEL DESIGNS WITH ISOLATED POWER OEM, ECONOMY, APPLICATION FLEXIBILITY (MODELS 282J/283J)

Offering open board construction at lowest cost-per-channel and application flexibility, these 2 and 3 channel designs are useful for medical/industrial OEM equipment. Models 282J and 283 J feature low input noise, adjustable gain from 1 to $100 \mathrm{~V} / \mathrm{V}$ and isolated, floating $\pm 6 \mathrm{~V}$ and $\pm 3 \mathrm{~V}$ power outputs. Similar in electrical performance to model 276 J , except for input protection, each isolated channel will support 220 V rms for 10 seconds, directly across the differential input. Constructed on an open printed circuit board for compact size and light weight, model 282 J has two independent, isolated channels. Model 283J has three independent isolated channels. Channel separation is 45 dB at 100 Hz for both designs.
Both model 282J and model 283J use an external guard shield. For this purpose, a guard shield assembly, model AC1043 is available from Analog Devices. See Figure 3 for block diagram of model 282 J . CMR for each channel, input-to-output at 60 Hz and $5 \mathrm{k} \Omega$ source imblance is 130 dB when operated with the ADI guard. Each isolated channel provides $\pm 0.5 \mathrm{~V}$ input signal range, $\pm 0.2 \%$ nonlinearity, $8 \mu \mathrm{~V}$ p-p input noise ( 100 Hz bandwidth), factory set gain of $3 \mathrm{~V} / \mathrm{V}$ (adjustable from 1 to $100 \mathrm{~V} / \mathrm{V}$ ) and $100 \mathrm{M} \Omega$ differential input impedance. This combination of performance makes both models 282 J and 283 J an excellent choice for all applications requiring low cost multichannel isolators. Models 282 J and 283 J will be available in December, 1974.


Figure 3. Block Diagram, Model 282J, Two Channel Isolator

## INDUSTRIAL ISOLATION AMPLIFIERS MODELS 272J, 274J, 279J, 280, 280-I

## INDUSTRIAL ISOLATORS: GENERAL DESCRIPTION

The industrial isolator product line consists of three high performance, FET input, epoxy encapsulated modules; models $272 \mathrm{~J}, 274 \mathrm{~J}$ and $279 \mathrm{~J}^{*}$. Models 272 J and 279 J are unity gain buffer amplifiers; model 274J offers adjustable gain, 1 to $100 \mathrm{~V} / \mathrm{V}$, using a single external gain setting resistor. All models achieve total input-to-output ground isolation using carrier modulation techniques with transformer coupling ${ }^{1}$. These rugged designs are fully guarded and offer excellent reliability, high RFI rejection and low cost in compact plugin modules.
All isolators are characterized by high common mode voltage capability as well as high differential input voltage protection. Models 272J and 279 J withstand up to $\pm 7.5 \mathrm{k}$ VDC common mode potential; model 274 J will withstand up to $\pm 2 \mathrm{k}$ VDC common mode. All models will withstand up to $\pm 7.5 \mathrm{kV}$ peak AC for 10 seconds ( 60 Hz burst), directly across the differential inputs (model 274J, Input \#1 only). Typical specifications for all models include 130 dB CMR ( $1 \mathrm{k} \Omega$ source imbalance, 60 Hz ), $10^{12} \Omega$ input impedance, 50 pA input difference current, leakage current of $1.2 \mu \mathrm{~A}(117 \mathrm{VAC}$, 60 Hz ), and 2 wire +15 VDC power input. Small signal response $(-3 \mathrm{~dB})$ is from DC to 1.2 kHz , model 274 J ; DC to 2 kHz , model 272J and DC to 4 kHz , model 279 J . All models have a 200 Hz full power response.

## NOISE REJECTION

All isolator designs incorporate a floating guard shield to minimize noise pickup due to ground potential differences ("ground loops") and capacitive pickup from power lines and other high frequency sources. Harsh, noisy environments, such as generated by electric motors, mechanical relay closures and solenoids are commonly experienced in power generating, industrial and process control plants when processing transducer and control signals. By connecting the isolators guard shield

[^7]terminal (see Figure 5) to a common potential point, one can, in effect, totally enclose the differential signal leads, thus protecting them from these sources of noise.

## MULTICHANNEL SYSTEMS

All carrier amplifiers are susceptible to high frequency noise sources that can cause "beat frequency" output signals. The erroneous "beat frequency" output may be caused by the radiated signal from a nearby oscillator; e.g., a second isolator mounted in close proximity. To eliminate this potential source of noise, model 279 J uses a unique external reference oscillator control. When two to ten 279 J units are configured in a multichannel isolator system using a common external reference oscillator drive, (model 280, see Figure 12, page 28), the beat output noise is eliminated by virtue of the synchronized oscillator system. When greater than ten channels of isolation are required, model 280-1 provides additional fanout capability. Up to 200 model 279 J isolators can be handled in a single multichannel system.

## APPLICATIONS IN INDUSTRIAL PROCESS CONTROL

In nuclear, chemical and metal processing control systems, it is possible to safely measure and control off-ground millivoltlevel signals in the presence of $\pm 7.5 \mathrm{kV}$ common mode potential. Models 272J, 274J and 279J will protect both control process and operator from system faults, a factor which is critical in nuclear and process control plants.

## Current Shunt Monitor

A typical application where the high 60 Hz CMR and CMV performance of the isolation amplifier is required is shown in Figure 4. In this application where the delta connection eliminates any neutral line at or near ground potential, the current shunt is inserted directly into one of the three phase lines, and readings are transferred to ground by the isolation amplifier. The amplifiers high common-mode voltage rating enables applications of this type to handle motors operating from 7500 volt peak supplies.

## LOW NOISE, ADJUSTABLE GAIN (MODEL 274J)

This design has a full $\pm 10$ volt output swing ( $50 \mathrm{k} \Omega$ load), adjustable gain and two "high" input terminals for optional degrees of input protection and noise performance. Referring to Figure 5, the two input terminals tie into the same amplifier point with terminal \#1 connected through a $2 \mathrm{M} \Omega$ series input resistor and terminal \#2 connected directly with no input amplifier protection resistor. Gain is adjustable from 1 to $100 \mathrm{~V} / \mathrm{V}$ using a single external resistor; best performance is achieved with gains from 10 to $100 \mathrm{~V} / \mathrm{V}$.
Gain is set by varying the gain ratio network formed by the internal $2 \mathrm{M} \Omega$ feedback resistor and external resistor, $\mathrm{R}_{\mathrm{g}}$. The $2 \mathrm{M} \Omega$ feedback resistor appears as a noise source, whose noise level referred to the amplifier input decreases as gain level increases and $\mathrm{R}_{\mathrm{g}}$ decreases. Increasing amplifier gain, therefore, reduces input noise. It should be noted that the output circuit and power supply are transformer isolated from each other as well as from the input circuit. The isolation rating applies from both inputs to either power or signal grounds. Output HI and LO terminals may be floated up to 200 volts continuous with respect to power ground.
The proper choice of input high terminal (\#1 or \#2) depends upon the degree of input protection required for the application. Input \#1 ( $2 \mathrm{M} \Omega$ input resistor) should be selected for $\pm 5 \mathrm{kV}$ peak pulse protection ( $1.4 \mathrm{kV} \mathrm{rms}, \mathrm{continuous)} \mathrm{over}$ the entire gain range from 1 to $100 \mathrm{~V} / \mathrm{V}$. Input noise is $10 \mu \mathrm{~V}$ $\mathrm{p}-\mathrm{p}(\mathrm{G}=100 \mathrm{~V} / \mathrm{V})$. Input \#2 should be selected for best noise performance and reduced input protection. Input noise is $5 \mu \mathrm{~V}$ p-p ( $\mathrm{G}=100 \mathrm{~V} / \mathrm{V}$ ); input protection will vary from $\pm 1.4 \mathrm{kV}$ peak pulse at $G=1 \mathrm{~V} / \mathrm{V}$ to $\pm 140 \mathrm{~V}$ peak pulse at $\mathrm{G}=100 \mathrm{~V} / \mathrm{V}$.

UNITY GAIN BUFFER, HIGHEST SAFETY (MODEL 272J) This design is available to meet the most demanding requirements for amplifier protection and for input to output circuit protection simultaneously. The input stage employs a $20 \mathrm{M} \Omega$ resistor to limit differential input fault currents to $10 \mu \mathrm{~A}$ (@ $220 \mathrm{VAC}, 60 \mathrm{~Hz}$ ). This can occur through an inadvertent con-
nection of the input leads across the AC power line. A full $\pm 7.5 \mathrm{kV}$ transient voltage is easily supported across the inputs and from all input leads to output common. The price of this protection is a relatively high amplifier noise level (typically $35 \mu \mathrm{~V} p-\mathrm{p}$ ) arising from the Johnson noise of the $20 \mathrm{M} \Omega$ resistor. Model 272 J , with $\pm 3$ volt dynamic signal swing and unity gain offers maximum amplifier protection against strong environmental signals such as RFI, EMI or lightning.

MULTICHANNEL ISOLATOR, UNITY GAIN (MODEL 279J)
Model 279J is a unity gain isolator designed for both medical and industrial systems requiring multiple, isolated channels with high channel separation. Employing a unique oscillator drive concept, model 279 J isolators may be operated in a system configuration containing from 1 to 200 isolation channels. Problems due to "cross-talk" from channel-to-channel are eliminated due to the synchronized oscillator drive. The need for special mounting techniques and shielding is eliminated.

Model 279J features high CMR (160dB @ DC, balanced source) and CMV ratings (to $\pm 7.5 \mathrm{kV}$ ). The FET input stage provides $\pm 3 \mathrm{~V}$ signal range, $\pm 0.2 \%$ nonlinearity, and only $14 \mu \mathrm{~V}$ p-p noise in a 100 Hz bandwidth.

## REFERENCE EXCITATION OSCILLATORS (MODELS 280/280-1

Models 280 and 280-1 provide in a compact inexpensive printed circuit board, an external reference oscillator signal to operate model 279 J . The model 280 reference oscillator is capable of driving up to 10 model 279 J isolators. If it is necessary to drive more than 10 isolators, a buffer, model 280-1, may be used in conjunction with the 280 . A model 280 can drive up to 20 model 280-1 buffers; each 280-1 buffer can drive up to 10279 J isolators. Thus, model 280 and 280-1 can be used together to drive up to 200 model 279 J isolators. (Both model 280 and 280-1 will be available in December 1974).


Figure 4. Motor Current Shunt Monitor


Figure 5. Block Diagram - Model 274 J

SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ and +15 VDC unless otherwise noted)

|  | MEDICAL AND INDUSTRIAL ISOLATORS |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Model | $\begin{gathered} \text { Buffer } \\ 273 \\ \mathrm{~J}(\mathrm{~K}) \\ \hline \end{gathered}$ | Economy, G = 3 Lowest Noise 276J | Buffer Ultimate Safety 272J | Adjustable Gain Low Noise 274J | Multi-Channel Systems $279 \mathrm{~J}^{8}$ |
| GAIN (NON-INVERTING) |  |  |  |  |  |
| Gain ( $50 \mathrm{k} \Omega$ Load) <br> vs. Temperature ( 0 to $+70^{\circ} \mathrm{C}$ ) <br> Accuracy <br> Nonlinearity, 4 V p-p | $\begin{gathered} 1 \mathrm{~V} / \mathrm{V} \\ \pm 0.015 \% /^{\circ} \mathrm{C} \\ \pm 3 \% \\ \pm 0.2 \% \end{gathered}$ | $\begin{gathered} 3 \mathrm{~V} / \mathrm{V} \\ \pm 0.015 \% /^{\circ} \mathrm{C} \\ \pm 2 \% \\ \pm 0.2 \%^{1} \end{gathered}$ | $\begin{gathered} 1 \mathrm{~V} / \mathrm{V} \\ \pm 0.015 \% /{ }^{\circ} \mathrm{C} \\ \pm 3 \% \\ \pm 0.2 \% \end{gathered}$ | $\begin{gathered} 1 \text { to } 100 \mathrm{~V} / \mathrm{V} \\ \pm 0.015 \% /{ }^{\circ} \mathrm{C} \\ \pm 2 \% \\ \pm 0.25 \%^{2} \end{gathered}$ | $\begin{gathered} 1 \mathrm{~V} / \mathrm{V} \\ \pm 0.015 \% /^{\circ} \mathrm{C} \\ \pm 3 \% \\ \pm 0.1 \% \end{gathered}$ |
| INPUT VOLTAGE RANGE |  |  |  |  |  |
| Linear Differential Input | $\pm 3 \mathrm{~V}, \mathrm{~min}$ | $\pm 0.5 \mathrm{~V}, \mathrm{~min}$ | $\pm 3 \mathrm{~V}, \mathrm{~min}$ | $\pm 1 \mathrm{~V}, \mathrm{~min}$ | $\pm 3 \mathrm{~V}, \mathrm{~min}$ |
| Max Safe Differential Input <br> Rms, Continuous <br> Peak Pulse, 5 ms Duration | $\begin{gathered} 700 \mathrm{~V}(1400 \mathrm{~V}) \\ \pm 5000 \mathrm{~V}^{3}\left( \pm 7500 \mathrm{~V}^{4}\right) \end{gathered}$ | $\begin{gathered} 500 \mathrm{~V} \\ \pm 5000 \mathrm{~V}^{3} \end{gathered}$ | $\begin{gathered} 2000 \mathrm{~V} \\ \pm 7500 \mathrm{~V}^{4} \end{gathered}$ | $\begin{aligned} & 1400 \mathrm{~V}^{5} \\ & \pm 5000^{4,5} \end{aligned}$ | $\begin{gathered} 1400 \mathrm{~V} \\ \pm 7500 \mathrm{~V}^{4} \end{gathered}$ |
| Max CMV, Input to Output <br> Peak AC or DC Continuous <br> Peak AC or DC, 10sec Duration | $\begin{aligned} & \pm 7500 \mathrm{~V} \\ & \pm 7500 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & \pm 2000 \mathrm{~V} \\ & \pm 5000 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & \pm 7500 \mathrm{~V} \\ & \pm 7500 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & \pm 2000 \mathrm{~V} \\ & \pm 7500 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & \pm 7500 \mathrm{~V} \\ & \pm 7500 \mathrm{~V} \end{aligned}$ |
| CMR, Input to Output, CMV $=115 \mathrm{VAC}, 60 \mathrm{~Hz}$ Balanced Source Impedance $5 \mathrm{k} \Omega$ Source Imbalance | $\begin{gathered} 126 \mathrm{~dB} \\ 115 \mathrm{~dB} \mathrm{~min} \end{gathered}$ | $\begin{gathered} 126 \mathrm{~dB} \\ 115 \mathrm{~dB} \text { min } \end{gathered}$ | $\begin{gathered} 126 \mathrm{~dB} \\ 115 \mathrm{~dB} \text { min } \end{gathered}$ | $\begin{gathered} 126 \mathrm{~dB} \\ 115 \mathrm{~dB} \text { min } \end{gathered}$ | $\begin{gathered} 126 \mathrm{~dB} \\ 115 \mathrm{~dB} \mathrm{~min} \end{gathered}$ |
| CMR, Input to Guard, CMV $=115 \mathrm{VAC}, 60 \mathrm{~Hz}$ $5 \mathrm{k} \Omega$ Source Imbalance | 60 dB | 60 dB | 60 dB | 60 dB | $60 \mathrm{~dB}$ |
| SAFETY CURRENT LIMITS ${ }^{7}$ | $1.2 \mu \mathrm{~A}, \max$ | $1.2 \mu \mathrm{~A}, \max$ | $1.2 \mu \mathrm{~A}, \mathrm{max}$ | $1.2 \mu \mathrm{~A}, \max$ | $1.2 \mu \mathrm{~A}$, max |
| INPUT IMPEDANCE <br> Differential, Linear Input Range Differential, Overload Input Common Mode | $\begin{gathered} 10^{12} \Omega / / 3 \mathrm{pF} \\ 1 \mathrm{M} \Omega(2 \mathrm{M} \Omega) \\ 10^{11} \Omega / / 20 \mathrm{pF} \end{gathered}$ | $\begin{gathered} 10^{8} \Omega / / 10 \mathrm{pF} \\ 300 \mathrm{k} \Omega \\ 5 \times 10^{10} \Omega / / 20 \mathrm{pF} \end{gathered}$ | $\begin{gathered} 10^{12} \Omega / / 3 \mathrm{pF} \\ 20 \mathrm{M} \Omega \\ 10^{11} \Omega / / 20 \mathrm{pF} \end{gathered}$ | $\begin{gathered} 10^{12} \Omega / / 3 \mathrm{pF} \\ 2 \mathrm{M} \Omega \\ 10^{11} \Omega / / 20 \mathrm{pF} \end{gathered}$ | $\begin{gathered} 10^{12} \Omega / / 3 \mathrm{pF} \\ 2 \mathrm{M} \Omega \\ 10^{11} \Omega / 120 \mathrm{pF} \end{gathered}$ |
| INPUT DIFFERENCE CURRENT <br> Initial, $25^{\circ} \mathrm{C}$ <br> vs. Temperature ( 0 to $+70^{\circ} \mathrm{C}$ ) <br> vs. Supply Voltage | $\begin{gathered} \pm 50 \mathrm{pA} \\ 2 \mathrm{x} / 10^{\circ} \mathrm{C} \\ \pm 0.1 \mathrm{pA} / \% \end{gathered}$ | $\begin{gathered} \pm 7 \mathrm{nA} \\ \pm 0.1 \mathrm{nA} /{ }^{\circ} \mathrm{C} \\ \pm 0.01 \mathrm{nA} / \% \end{gathered}$ | $\begin{gathered} \pm 50 \mathrm{pA} \\ 2 \mathrm{x} / 10^{\circ} \mathrm{C} \\ \pm 0.1 \mathrm{pA} / \% \end{gathered}$ | $\begin{gathered} \pm 50 \mathrm{pA} \\ 2 \mathrm{x} / 10^{\circ} \mathrm{C} \\ \pm 0.1 \mathrm{pA} / \% \end{gathered}$ | $\begin{gathered} \pm 50 \mathrm{pA} \\ 2 \mathrm{x} / 10^{\circ} \mathrm{C} \\ \pm 0.1 \mathrm{pA} / \% \end{gathered}$ |
| INPUT NOISE |  |  |  |  |  |
| Voltage, ( 0.05 to 100 Hz ), p-p <br> Input \#1 <br> Input \#2 | $\begin{gathered} 10 \mu \mathrm{~V}(14 \mu \mathrm{~V}) \\ \text { NA } \end{gathered}$ | $\begin{aligned} & 8 \mu \mathrm{~V} \\ & \mathrm{NA} \end{aligned}$ | $\begin{gathered} 35 \mu \mathrm{~V} \\ \mathrm{NA} \end{gathered}$ | $\begin{gathered} 10 \mu \mathrm{~V}(\mathrm{G}=100) \\ 5 \mu \mathrm{~V}(\mathrm{G}=100) \end{gathered}$ | $\begin{gathered} 14 \mu \mathrm{~V} \\ \mathrm{NA} \end{gathered}$ |
| Voltage, $(5 \mathrm{~Hz}$ to 1 kHz$)$, rms Input \#1 or \#2 <br> Current, $(0.05 \mathrm{~Hz}$ to 100 Hz$)$, rms | $\begin{gathered} 5 \mu \mathrm{~V} \\ 0.1 \mathrm{pA} \end{gathered}$ | $\begin{aligned} & 5 \mu \mathrm{~V} \\ & 4 \mathrm{pA} \end{aligned}$ | $\begin{aligned} & 15 \mu \mathrm{~V} \\ & 0.1 \mathrm{pA} \end{aligned}$ | $\begin{gathered} 7 \mu \mathrm{~V}(\mathrm{G}=100) \\ 0.1 \mathrm{pA} \end{gathered}$ | $\begin{gathered} 5 \mu \mathrm{~V} \\ 0.1 \mathrm{pA} \end{gathered}$ |
| FREQUENCY RESPONSE Small Signal, -3 dB Full Power, 4 V p-p Output, $3 \%$ THD Overload Recovery | 4 kHz <br> 200 Hz <br> 200 ms | $\begin{gathered} 1 \mathrm{kHz} \\ 200 \mathrm{~Hz}^{1} \\ 200 \mathrm{~ms} \end{gathered}$ | 2 kHz <br> 200 Hz <br> 200 ms | 1.2 kHz <br> $200 \mathrm{~Hz}^{2}$ <br> 200 ms | 4 kHz <br> 200 Hz <br> 200 ms |
| ```OUTPUT OFFSET VOLTAGE Initial, \(25^{\circ} \mathrm{C}\) vs. Temperature ( 0 to \(+70^{\circ} \mathrm{C}\) ) vs. Supply Voltage``` | $\begin{gathered} \pm 50 \mathrm{mV} \\ \pm 100 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ \pm 30 \mu \mathrm{~V} / \% \end{gathered}$ | $\begin{gathered} \pm 50 \mathrm{mV} \\ \pm 100 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ \pm 30 \mu \mathrm{~V} / \% \end{gathered}$ | $\begin{gathered} \pm 50 \mathrm{mV} \\ \pm 150 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ \pm 30 \mu \mathrm{~V} / \% \end{gathered}$ | $\begin{gathered} \pm(50+2 \mathrm{G}) \mathrm{mV} \\ \pm(200+50 \mathrm{G}) \mu \mathrm{V} /{ }^{\circ} \mathrm{C} \\ \pm(100+2 \mathrm{G}) \mu \mathrm{V} / \% \end{gathered}$ | $\begin{gathered} \pm 50 \mathrm{mV} \\ \pm 100 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ \pm 30 \mu \mathrm{~V} / \% \end{gathered}$ |
| OUTPUT <br> Rated Output, $50 \mathrm{k} \Omega$ Load Output Impedance | $\begin{gathered} \pm 3 \mathrm{~V}, \mathrm{~min} \\ 1.5 \mathrm{k} \Omega \end{gathered}$ | $\begin{gathered} \pm 1.7 \mathrm{~V}, \min \\ 1.5 \mathrm{k} \Omega \end{gathered}$ | $\begin{gathered} \pm 3 \mathrm{~V}, \mathrm{~min} \\ 1.5 \mathrm{k} \Omega \end{gathered}$ | $\begin{gathered} \pm 10 \mathrm{~V}, \min \\ 1.5 \mathrm{k} \Omega \end{gathered}$ | $\begin{gathered} \pm 3 \mathrm{~V}, \min \\ 1.5 \mathrm{k} \Omega \end{gathered}$ |
| POWER SUPPLY RANGE, (SINGLE POLARITY) <br> Voltage, Rated Specifications <br> Voltage, Operating <br> Current, Quiescent @ +15VDC | $\begin{gathered} (+12 \text { to }+28) \text { VDC } \\ (+9 \text { to }+28) \text { VDC } \\ 15 \mathrm{~mA} \end{gathered}$ | +15VDC <br> 15 mA | $\begin{gathered} (+12 \text { to }+28) \text { VDC } \\ (+9 \text { to }+28) \text { VDC } \\ 15 \mathrm{~mA} \end{gathered}$ | $\begin{gathered} +15 \mathrm{VDC} \\ - \\ 60 \mathrm{~mA} \end{gathered}$ | $\begin{gathered} (+12 \text { to }+28) \mathrm{VDC} \\ (+9 \text { to }+28) \mathrm{VDC} \\ 15 \mathrm{~mA} \end{gathered}$ |
| TEMPERATURE RANGE <br> Rated Performance Operating | $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \\ -25 \text { to }+85^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \\ -25 \text { to }+85^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \\ -25 \text { to }+85^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \\ -25 \text { to }+85^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \\ -25 \text { to }+85^{\circ} \mathrm{C} \end{gathered}$ |
| PACKAGE OUTLINE <br> Case Dimensions in Inches (mm) | $\begin{gathered} \mathrm{K}-1 \\ 3.5^{\prime \prime} \times 2.5^{\prime \prime} \times 1.25^{\prime \prime} \\ (88.9 \times 63.5 \times 32) \end{gathered}$ | $\begin{gathered} \mathrm{K}-1 \\ 3.5^{\prime \prime} \times 2.5^{\prime \prime} \times 1.25^{\prime \prime} \\ (88.9 \times 63.5 \times 32) \end{gathered}$ | $\begin{gathered} \mathrm{K}-1 \\ 3.5^{\prime \prime} \times 2.5^{\prime \prime} \times 1.25^{\prime \prime} \\ (88.9 \times 63.5 \times 32) \end{gathered}$ | $\begin{gathered} \mathrm{K}-2 \\ 3.5^{\prime \prime} \times 2.5^{\prime \prime} \times 1.25^{\prime \prime} \\ (88.9 \times 63.5 \times 32) \end{gathered}$ | $\begin{gathered} \mathrm{K}-3 \\ 3.5^{\prime \prime} \times 2.5^{\prime \prime} \times 1.25^{\prime \prime} \\ (88.9 \times 63.5 \times 32) \end{gathered}$ |
| PRICE <br> 1-9 <br> 10-24 | $\begin{gathered} \$ 109 \\ \$ 92 \end{gathered}$ | $\begin{aligned} & \$ 98 \\ & \$ 89 \end{aligned}$ | $\begin{gathered} \$ 114 \\ \$ 96 \end{gathered}$ | $\begin{aligned} & \$ 125 \\ & \$ 115 \end{aligned}$ | $\begin{aligned} & \$ 89 \\ & \$ 79 \end{aligned}$ |


| ${ }^{1} 3 \mathrm{~V}$ p-p output | ${ }^{5}$ Input \#1, G = 1 to $100 \mathrm{~V} / \mathrm{V} ;$ |
| :--- | :--- |
| 2 <br> 20 V p-p output | Input \#2, 1 kV @ $\mathrm{G}=1 ; 200 \mathrm{~V} @ \mathrm{G}=100$ |
| ${ }^{3}$ One pulse per second | ${ }^{6} \mathrm{CMV}=115 \mathrm{VAC}, 60 \mathrm{~Hz}$ |
| ${ }^{4}$ Ten seconds, 60 Hz pulse burst | ${ }^{7}$ Any input to output @ $117 \mathrm{VAC}, 60 \mathrm{~Hz}$. See figure 1. |



## GENERAL DESCRIPTION

Comparators in this group are specialized operational amplifiers with differential inputs and two bi-stable states. Used to digitize relative amplitude information, these comparators become the key element in the analog-to-digital conversion process. They are useful as threshold level detectors for A/D converters, voltage to frequency converters, pulse-width modulators and a wide variety of square wave and pulse generators. Available with either FET or bipolar input stage, they have been optimized for fast switching and stable threshold characteristics.

## MODEL 350 A/B/C: FET COMPARATOR

Model 350 is a comparator module with high impedance with FET inputs, excellent "trip point" stability, fast response and logic compatible output. Operating as an open loop amplifier with bi-stable output stages, model 350 switching and offset parameters have been optimized for use in DC to 100 kHz comparator circuits including level detectors, pulse-width modulators and fast reset pulse circuits. Typical specifications include $20 \mathrm{~V} / 400 \mu \mathrm{~V}$ sensitivity at $1.5 \mathrm{k} \Omega$ load, CMR of 60 dB at 10 V and two output ratings; $\pm 10 \mathrm{~V}$ at $\pm 7 \mathrm{~mA}$ ( 500 ns switch time) or 0 to 5 volt swing at 15 mA ( 100 ns switch time) when its output limit pin is connected for digital logic compatibility. There are three drift options available: $75 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ (A), $40 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ (B), and $25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ (C).

MODEL AD351 J/K/S
Model AD35 1 is a high performance monolithic comparator which includes additional front end circuitry, usually added externally with other IC designs, to achieve low bias and offset currents with high input impedance. Although its speed is modestly reduced by incorporating these user conveniences, AD351 fulfills the need for a high speed comparator for a wide range of applications including zero-crossing detectors, threshold detectors and window comparators. Typical specifications include 84 dB gain, 250 nA bias, CMR of 70 dB at $\pm 10 \mathrm{~V}$ and 1 to 7 volt output swing ( 400 ns switch time) with $10 \mathrm{k} \Omega$ output impedance.

| Model |  FET Comparator  <br>  350  <br> A B C | Monolithic Comparator <br>  <br> $\mathbf{3 5 1}$ <br> J |
| :---: | :---: | :---: |
| Gain, V/V, min | $50,000 @ 1.5 \mathrm{k} \Omega \mathrm{load}$ | 15,000 |
| Rated Output Voltage Levels, min | $\begin{gathered} \pm 10 \mathrm{~V} @ 7 \mathrm{~mA} \text { or } \\ +5 \mathrm{~V} @ 15 \mathrm{~mA}, 0 \mathrm{~V} @ 20 \mathrm{~mA}^{1} \end{gathered}$ | $\begin{gathered} +7 \mathrm{~V} \text { @ no load to } \\ +1 \mathrm{~V} @ 2 \mathrm{~mA} \end{gathered}$ |
| Input Bias Current, max <br> Avg. vs. Temp <br> Input Offset Voltage <br> Initial, $25^{\circ} \mathrm{C}$, (adj. to zero), max vs. Temp, max | $\left.\begin{array}{c\|c\|c}\begin{array}{l\|c}50 \mathrm{pA} \\ 5 \mathrm{nA}\end{array} & \begin{array}{c}30 \mathrm{pA} \\ 3 \mathrm{nA}\end{array} & 30 \mathrm{pA} \\ 3 \mathrm{nA}^{2}\end{array}\right]$$\pm 2 \mathrm{mV}$ <br> 75$\quad$ <br> 70 |  250 nA  <br>    <br>  $4 \mathrm{nA} /{ }^{\circ} \mathrm{C}$  <br>    <br>   $\pm 6 \mathrm{mV}$ <br>    <br>  5 $10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ |
| Input Impedance <br> Differential <br> Common Mode <br> Input Voltage Range <br> Safe Differential Voltage <br> Common Mode Rejection @ $\pm 10 \mathrm{~V}$ <br> Common Mode Voltage, min | $\begin{gathered} 10^{11} \Omega / / 3.5 \mathrm{pF} \\ 10^{11} \Omega / / 3.5 \mathrm{pF} \\ \pm 30 \mathrm{~V} \\ 60 \mathrm{~dB} \\ \pm 10 \mathrm{~V} \end{gathered}$ | $\begin{gathered} 10 \mathrm{M} \Omega / / 4 \mathrm{pF} \\ 10 \mathrm{M} \Omega / / 4 \mathrm{pF} \\ \pm 30 \mathrm{~V} \\ 70 \mathrm{~dB} \min (5 \mathrm{~V} \text { output) } \\ \pm 10 \mathrm{~V} \end{gathered}$ |
| ```Response Time Switching (0 to 5V) Output Delay``` | $\begin{aligned} & 100 \mathrm{~ns} \\ & 5 \mu \mathrm{~s}^{3} \end{aligned}$ | 400 ns $250 \mathrm{~ns}(2.5 \mathrm{~V}$ output) |
| Power Supply <br> Positive Voltage (VDC) <br> Negative Voltage (VDC) <br> Temperature Range | $\begin{aligned} & +(15 \text { to } 16) \mathrm{V} @ 3.5 \mathrm{~mA} \\ & -(15 \text { to } 16) \mathrm{V} @ 3.5 \mathrm{~mA} \\ & -25 \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | $\begin{gathered} +(7 \text { to } 18) \mathrm{V} @ 2.5 \mathrm{~mA} \\ -18 \mathrm{~V} \text { max@0.5mA } \\ 0 \text { to }+70^{\circ} \mathrm{C} \mid 0 \text { to }+70^{\circ} \mathrm{C} \mid-55 \text { to }+125^{\circ} \mathrm{C} \end{gathered}$ |
| Package Outline Case Dimensions | $\begin{array}{llll} \hline & \mathrm{F}-1 \\ 1.5^{\prime \prime} \times 1.5^{\prime \prime} \times & \\ \hline \end{array}$ | TO-100 |
| $\begin{aligned} & \text { Price } \\ & 1-9 \\ & 10-24 \end{aligned}$ | $\$ 44$ $\$ 55$ $\$ 77$ <br> $\$ 42$ $\$ 53$ $\$ 74$ | $\$ 13.45$ $\$ 20.70$ $\$ 27.60$ <br> $\$ 13.45$ $\$ 20.70$ $\$ 27.60$ |

(1) $+5 \mathrm{~V}, 0 \mathrm{~V}$ reduced swing using limit connection of 350 .
(3)Input overdrive of 10 mV .
(2)Total drift -25 to $+85^{\circ} \mathrm{C}$.

## GENERAL DESCRIPTION

A major criterion in the selection of an amplifier is the amplifier input noise, since this is usually the limiting factor on system resolution for low level signals. For this reason, amplifiers in this section have been selected because of their exceptional low noise performance and broad application capabilities. Noise performance is specified over the most useful bandwidth for that class of amplifier. Amplifier types included in this section are: instrumentation, model 606; chopper, models 230,234 , 261; F.E.T., models 43, 50, 52; bipolar, model 184; and F.E.T. input IC, model AD514. Significant performance curves are shown to enable a better selection of a particular amplifier from this section. (Refer to page 23 for discussion of noise sources and a design example illustrating how to determine their total effect.)

MODEL $52 \mathrm{~J} / \mathrm{K}:$ PRECISION FET, $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}, 1.5 \mu \mathrm{~V}$ p-p For high impedance differential applications, model 52 combines guaranteed low voltage noise of $1.5 \mu \mathrm{~V}$ p-p $\max (1 \mathrm{~Hz} \mathrm{BW})$, low voltage drift, $3 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max (52 \mathrm{~J}) ; 1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max (52 \mathrm{~K})$, low input bias current, 3 pA max and CMR of 100 dB min. Model 52 is an excellent choice to replace expensive chopper stabilized designs where significant sources of error may be introduced from zero beating, "chopper spikes" and ground loop currents.
The effect of high source impedance should be considered in determining total input voltage noise. The curves shown below indicate the added contribution of current noise due to source resistance for two low frequency bandwidths, 1 Hz and 100 Hz .

MODEL 230 J/K/L: LOWEST "DC" NOISE CHOPPER Model 230 offers the lowest "DC" noise performance of any chopper stabilized amplifier. The spectral noise density curves, shown on the following page, illustrate the excellent performance in the " $1 / \mathrm{f}$ " region (below 1 Hz ). Model 230 is an excellent choice for bandwidths below 1 Hz where ultra low noise, low drift and good stability are required. Initial offset voltage is internally trimmed to less than $\pm 15 \mu \mathrm{~V}$.

MODEL $184 \mathrm{~J} / \mathrm{K} / \mathrm{L}: \mathbf{0 . 2 5 \mu \mathrm { V } / { } ^ { \circ } \mathrm { C } \text { , BIPOLAR, 100dB CMR }}$ For source impedances up to $100 \mathrm{k} \Omega$, model 184 challenges the low drift and long term stability of chopper stabilized amplifiers while avoiding "chopper noise and spikes". Model 184 will provide good linearity and gain stability for single-ended or differential applications. Low noise of $1 \mu \mathrm{~V}$ p-p ( 1 Hz BW ) and $0.25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max drift (184L) suggest low level transducer and bridge applications. Initial offset is internally trimmed to $100 \mu \mathrm{~V}$ $\max (184 \mathrm{~K}, \mathrm{~L})$ and open loop voltage gain is $300,000 \mathrm{~V} / \mathrm{V} \mathrm{min}$.


MODEL 43 K : ECONOMY, FET, $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$
Guaranteeing voltage noise of $2 \mu \mathrm{~V}$ p-p ( 1 Hz BW ), this economy FET design also features $\pm 5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ (max) voltage drift, input bias current of 20 pA (max) and full power response of 200 kHz minimum. In a 50 kHz bandwidth, noise is also guaranteed to be less than $3 \mu \mathrm{~V}$ rms. Signal to noise performance in wideband applications is improved over similar designs, but at a significantly lower cost. Model 43 is packaged in a small $1^{\prime \prime} \times 1^{\prime \prime} \times$ $0.5^{\prime \prime}$ epoxy package.

## MODEL $50 \mathrm{~J} / \mathrm{K}$ : WIDEBAND, FET, 100 mA OUTPUT

Model 50 is an ultra fast, wideband differential FET amplifier designed for applications requiring fast settling time with high output current. Model 50 offers settling time of 100 ns maximum to $\pm 0.1 \%$ accuracy, 100 MHz gain bandwidth product and $\pm 100 \mathrm{~mA}$ output from dc to 8 MHz . Input voltage noise ( $6 \mu \mathrm{~V}$ rms, 5 Hz to 2 MHz BW ), is significantly lower than comparable models, and is particularly important in display system D/A converter applications, as illustrated below.


High Speed Current to Voltage Buffer

MODEL 234 J/K/L: WIDEBAND CHOPPER STABILIZED
For wide bandwidth, inverting applications requiring high gain and low drift, model 234 is an excellent choice. Available in three drift selections ( $1,0.3$ and $0.1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ ), model 234 is virtually free of chopper spikes and offers voltage noise of $1.5 \mu \mathrm{~V}$ p-p ( 10 Hz BW ), current noise of $2 \mathrm{pA} \mathrm{p}-\mathrm{p}(1 \mathrm{~Hz} \mathrm{BW})$ and 2.5 MHz bandwidth. It is especially useful for 16 bit D/A converters, high speed integrators as well as low frequency applications including control systems and other precision instrumentation. Shown below are plots of typical input voltage and input current noise over the frequency range of 0.01 Hz to 10 Hz . Particular care has been exercised in the design of this amplifier to reduce the noise level to that obtained by chopper stabilization.

## MODEL 261 J/K: NON-INVERTING CHOPPER

Model 261 is a low cost non-inverting chopper amplifier featuring guaranteed low voltage noise of $0.4 \mu \mathrm{~V}$ p-p $\max (1 \mathrm{~Hz} \mathrm{BW})$, ultra low voltage drift of $0.1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ and open loop gain of $10^{7} \mathrm{~V} / \mathrm{V} \mathrm{min}$. It is ideally suited for low level pre-amplifier applications where high input impedance and low noise are essential. Model 261's carrier frequency of 3500 Hz , in addition to complete internal shielding, offers freedom from beat frequency problems common in chopper stabilized designs. The graph below shows input noise versus bandwidth for both current and voltage.


Model 52 Noise vs. Source Resistance for Constant Bandwidth


Model 230 Voltage \& Current Noise per Root Hz of Bandwidth


Model 234 Voltage and Current Noise


Model 261 Noise Current \& Voltage vs. Bandwidth
Measured from 0.01 Hz


Model 606 Voltage Noise per Root Hz of Bandwidth ( $G=1000$ )


Model 606 Total Output Voltage Noise vs. Gain

606 J/K/L/M: FAST RESPONSE, INSTRUMENTATION, $1 / 4 \mu \mathrm{~V} /{ }^{\circ} \mathbf{C}, 100 \mathrm{kHz}$ BANDWIDTH ( $\mathbf{G}=\mathbf{1 0 0} \mathrm{V} / \mathrm{V}$ )
Model 606 offers virtually constant bandwidth over the differential gain range of 1 to $10,000 \mathrm{~V} / \mathrm{V}$. Combining low voltage drift ( $1 / 4 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max, 606 M ) with guaranteed low voltage noise ( $1 \mu \mathrm{~V}$ p-p max, 10 Hz BW ), model 606 is an excellent data amplifier for low level, high gain signal processing applications requiring rapid settling time ( $30 \mu \mathrm{~s}$ to $\pm 0.1 \%$ ). Model 606
requires only a single external resistor to program differential gain. High common mode rejection ( $100 \mathrm{~dB} \min \mathrm{G}=1000 \mathrm{~V} / \mathrm{V}$ ) is offered for common mode voltages up to $\pm 10$ volts min. Model 606 establishes a new level of performance with low voltage noise. Input rms voltage noise density is shown on page 63. Also illustrated are 10 Hz and 100 Hz bandwidth total output noise for gains from 1 to $10,000 \mathrm{~V} / \mathrm{V}$.

SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ and $\pm 15 \mathrm{~V}$ unless otherwise noted)

| Model | $\begin{gathered} \text { Economy FET } \\ 5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ 43 \mathrm{~K} \end{gathered}$ | $\begin{aligned} & \text { Wideband, FET } \\ & \pm 100 \mathrm{~mA} \\ & \mathbf{5 0 J}(50 \mathrm{~K}) \end{aligned}$ | High Accuracy FET 52J ( 52 K ) | $\begin{gathered} \text { Bipolar, } 1 / 4 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ 100 \mathrm{~dB} \mathrm{CMR} \\ 18+\mathrm{J}(184 \mathrm{~K})(184 \mathrm{~L}) \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: |
| OPEN LOOP GAIN DC rated load, $\min , \mathrm{V} / \mathrm{V}$ | 50,000 | 25,000 | $10^{6}$ | 300,000 |
| RATED OUTPUT <br> Voltage, min <br> Current, min <br> Load Capacitance Range | $\pm 10 \mathrm{~V}$ $\pm 5 \mathrm{~mA}$ 1000 pF | $\begin{gathered} \pm 10 \mathrm{~V} \\ \pm 100 \mathrm{~mA} \\ \text { Inv }=50 \mathrm{pF}, \text { Non-Inv }=100 \mathrm{pF} \end{gathered}$ | $\pm 10 \mathrm{~V}$ <br> $\pm 5 \mathrm{~mA}$ <br> $0.01 \mu \mathrm{~F}$ | $\begin{gathered} \pm 10 \mathrm{~V} \\ \pm 5 \mathrm{~mA} \\ 1000 \mathrm{pF} \end{gathered}$ |
| FREQUENCY RESPONSE <br> Small Signal, -3dB <br> Full Power Response, min <br> Slewing Rate, min <br> Overload Recovery <br> Settling Time, $\pm 0.1 \%, \pm 10 \mathrm{~V}$ Step | $\begin{gathered} 4 \mathrm{MHz} \\ 200 \mathrm{kHz} \\ 12 \mathrm{~V} / \mu \mathrm{s} \\ 0.5 \mu \mathrm{~s} \\ - \end{gathered}$ | $\begin{gathered} 100 \mathrm{MHz} \\ 8 \mathrm{MHz} \\ 500 \mathrm{~V} / \mu \mathrm{sec} \\ 200 \mathrm{nsec} \\ 100 \mathrm{nsec} \max (\text { Inv, G }=2) \end{gathered}$ | 500 kHz 4 kHz $0.25 \mathrm{~V} / \mu \mathrm{sec}$ $130 \mu \mathrm{sec}$ $100 \mu \mathrm{sec}$ | $\begin{gathered} 1 \mathrm{MHz} \\ 5 \mathrm{kHz} \\ 0.25 \mathrm{~V} / \mu \mathrm{sec} \\ - \\ - \end{gathered}$ |
| INPUT OFFSET VOLTAGE <br> Initial Offset, $+25^{\circ} \mathrm{C}$ <br> vs. Temp. $\left(0\right.$ to $\left.+70^{\circ} \mathrm{C}\right) \max$ <br> vs. Supply Voltage <br> vs. Time <br> Warm-Up Drift, 5 minutes | $\begin{gathered} \pm 2 \mathrm{mV} \\ \pm 5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ \pm 10 \mu \mathrm{~V} / \% \\ \pm 50 \mu \mathrm{~V} / \mathrm{mo} \end{gathered}$ | $\begin{gathered} \pm 3 \mathrm{mV} \\ \pm 50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\left( \pm 15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\right) \\ \pm 15 \mu \mathrm{~V} / \% \\ \pm 500 \mu \mathrm{~V} / \mathrm{mo} \\ - \end{gathered}$ | $\begin{gathered} \pm 0.5 \mathrm{mV} \max \\ \pm 3 \mu \mathrm{~V} /^{\circ} \mathrm{C}\left( \pm 1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\right) \max \\ \pm 12 \mu \mathrm{~V} / \mathrm{V} \\ \pm 5 \mu \mathrm{~V} / \mathrm{mo} \\ \pm 5 \mu \mathrm{~V} \end{gathered}$ | $\begin{gathered} \pm 250( \pm 100)( \pm 100) \mu \mathrm{V} \max \\ \pm 1.5( \pm 0.5)( \pm 0.25) \mu \mathrm{V} /{ }^{\circ} \mathrm{C} \\ \pm 5 \mu \mathrm{~V} / \% \\ \pm 3 \mu \mathrm{~V} / \mathrm{mo} . \end{gathered}$ |
| INPUT BIAS CURRENT <br> Initial Bias, $+25^{\circ} \mathrm{C}$, max, <br> vs. Temp. ( 0 to $+70^{\circ} \mathrm{C}$ ) max <br> vs. Supply Voltage | $\begin{aligned} & 0,-20 \mathrm{pA} \\ & 2 \mathrm{x} /+10^{\circ} \mathrm{C} \\ & \pm 1 \mathrm{pA} / \% \end{aligned}$ | $\begin{gathered} -2 \mathrm{nA} \\ 2 \mathrm{x} /+10^{\circ} \mathrm{C} \\ \pm 10 \mathrm{pA} / \% \end{gathered}$ | $\begin{gathered} -3 \mathrm{pA} \\ 2 \mathrm{x} /+10^{\circ} \mathrm{C} \\ \pm 0.01 \mathrm{pA} / \% \\ \hline \end{gathered}$ | $\begin{gathered} \quad+25 \mathrm{nA} \\ \pm 0.02 \mathrm{nA} /{ }^{\circ} \mathrm{C} \\ \pm 0.25 \mathrm{nA} /{ }^{\circ} \mathrm{C} \end{gathered}$ |
| INPUT IMPEDANCE <br> Differential Common Mode | $\begin{aligned} & 10^{11} \Omega \\| 3.5 \mathrm{pF} \\ & 10^{11} \Omega \\| 3.5 \mathrm{pF} \end{aligned}$ | $\begin{aligned} & 10^{11} \Omega \\| 3.5 \mathrm{pF} \\ & 10^{11} \Omega \\| 3.5 \mathrm{pF} \\ & \hline \end{aligned}$ | $\begin{aligned} & 10^{12} \Omega \\| 3.5 \mathrm{pF} \\ & 10^{12} \Omega \\| 3.5 \mathrm{pF} \end{aligned}$ | $\begin{gathered} 4 \mathrm{M} \Omega \\| 4 \mathrm{pF} \\ 2000 \mathrm{M} \Omega \\| 4 \mathrm{pF} \end{gathered}$ |
| INPUT NOISE <br> Voltage, 0.01 to $1 \mathrm{~Hz}, \mathrm{p}-\mathrm{p}$ <br> 0.1 to $10 \mathrm{~Hz}, \mathrm{p}-\mathrm{p}$ <br> 5 Hz to 10 kHz , rms <br> Current, 0.01 to $1 \mathrm{~Hz}, \mathrm{p}-\mathrm{p}$ | $\begin{gathered} 2 \mu \mathrm{~V}, \max \\ 2 \mu \mathrm{~V} \\ 2 \mu \mathrm{~V}, \max \\ 0.1 \mathrm{pA} \end{gathered}$ | $\begin{gathered} 5 \mu \mathrm{~V} \\ 5 \mu \mathrm{~V} \\ 6 \mu \mathrm{~V}(5 \text { to } 2 \mathrm{MHz}) \\ 1 \mathrm{pA} \end{gathered}$ | $\begin{aligned} & 1.5 \mu \mathrm{~V} \max \\ & 1.5 \mu \mathrm{~V} \\ & 3.0 \mu \mathrm{~V} \max \\ & 0.1 \mathrm{pA} \end{aligned}$ | $\begin{gathered} 1 \mu \mathrm{~V} \\ 1 \mu \mathrm{~V} \\ 3 \mu \mathrm{~V} \\ 10 \mathrm{pA} \end{gathered}$ |
| INPUT VOLTAGE RANGE <br> Common Mode Voltage, min <br> Common Mode Rejection <br> Max Safe Differential Voltage <br> Max Safe Common Mode Voltage | $\begin{gathered} \pm 11 \mathrm{~V} \\ 80 \mathrm{~dB} @+8,-10 \mathrm{~V} \\ \pm 15 \mathrm{~V} \end{gathered}$ | $\begin{gathered} \pm 10 \mathrm{~V} \\ 60 \mathrm{~dB} \text { min @ } \pm 10 \mathrm{~V} \\ \pm \mathrm{V}_{\mathrm{S}} \end{gathered}$ | $\begin{gathered} \pm 10 \mathrm{~V} \\ 100 \mathrm{~dB} \min @ \pm 10 \mathrm{~V} \\ \pm V_{\mathrm{s}} \end{gathered}$ | $\begin{gathered} \pm 10 \mathrm{~V} \\ 100 \mathrm{~dB} @ \pm 10 \mathrm{~V} \\ \pm 15 \mathrm{~V} \end{gathered}$ |
| POWER SUPPLY <br> Voltage, Rated <br> Voltage, Operating <br> Current, Quiescent | $\begin{gathered} \pm 15 \mathrm{~V} \\ \pm(12 \text { to } 18) \mathrm{VDC} \\ \pm 5 \mathrm{~mA} \end{gathered}$ | $\begin{gathered} \pm 15 \mathrm{VDC} \\ \pm(12 \text { to } 18) \mathrm{VDC} \\ \pm 40 \mathrm{~mA} \end{gathered}$ | $\begin{gathered} \pm 15 \mathrm{VDC} \\ \pm(9 \text { to } 18) \mathrm{VDC} \\ \pm 5 \mathrm{~mA} \end{gathered}$ | $\begin{gathered} \pm 15 \mathrm{VDC} \\ \pm(10 \text { to } 18) \mathrm{VDC} \\ \pm 9 \mathrm{~mA} \end{gathered}$ |
| TEMPERATURE RANGE <br> Rated Specifications <br> Operating <br> Storage | 0 to $+70^{\circ} \mathrm{C}$ <br> $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ <br> $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \\ -25^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \\ -25^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \\ -55^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \end{gathered}$ |
| PACKAGE OUTLINE Case Dimensions | $\begin{gathered} \mathrm{M}-2 \\ 1^{\prime \prime} \times 1^{\prime \prime} \times 0.5^{\prime \prime} \end{gathered}$ | $\begin{gathered} \mathrm{N}-1 \\ 1.22^{\prime \prime} \times 1.88^{\prime \prime} \times 0.6^{\prime \prime} \end{gathered}$ | $\frac{\mathrm{QC}-4}{} 1.12^{\prime \prime} \times 1.12^{\prime \prime} \times 0.4^{\prime \prime}$ | $\begin{gathered} \mathrm{F}-1 \\ 1.5^{\prime \prime} \times 1.5^{\prime \prime} \times 0.4^{\prime \prime} \end{gathered}$ |
| $\begin{aligned} & \hline \text { PRICE } \\ & (1-9) \\ & (10-24) \end{aligned}$ | $\begin{array}{r} \$ 35 \\ \$ 33 \end{array}$ | $\begin{aligned} & \$ 75(\$ 92) \\ & \$ 71(\$ 87) \end{aligned}$ | $\begin{aligned} & \$ 42(\$ 49) \\ & \$ 39(\$ 47) \end{aligned}$ | $\begin{aligned} & \$ 43(\$ 58)(\$ 68) \\ & \$ 39(\$ 55)(\$ 65) \end{aligned}$ |

[^8]
## AD514 J/K/L

The AD5 14 is a low noise FET-input IC amplifier designed for applications where low noise in addition to low bias currents are essential such as EKG amplifiers, pH electrodes and long term integrators. The device is available with 0.1 to 10 Hz voltage noise as low as $5 \mu \mathrm{~V}$ max, $100 \%$ tested and guaranteed.

| Lowest "DC" <br> Noise, Chopper $230 \mathrm{~J}(230 \mathrm{~K})(230 \mathrm{~L})$ | Wideband Chopper $234 \mathrm{~J}(234 \mathrm{~K})(234 \mathrm{~L})$ | Non-Inverting Chopper $261 \mathrm{~J}(261 \mathrm{~K})$ | Wideband, $1 / 4 \mu \mathbf{V} /{ }^{\circ} \mathbf{C}$ Instrumentation 606 J ( 606 K ) ( 606 L ) (606M) | Microcircuit Low Noise, High Accuracy AD514J (AD514K) (AD514L) |
| :---: | :---: | :---: | :---: | :---: |
| $10^{7}$ | $10^{7}$ | $10^{7}$ | 1 to 10,000 | $20,000(50,000)(50,000)$ |
| $\begin{gathered} \pm 10 \mathrm{~V} \\ \pm 4 \mathrm{~mA} \\ 0.01 \mu \mathrm{~F} \end{gathered}$ | $\begin{gathered} \pm 10 \mathrm{~V} \\ \pm 5 \mathrm{~mA} \\ 1000 \mathrm{pF} \end{gathered}$ | $\begin{gathered} \pm 10 \mathrm{~V} \\ \pm 5 \mathrm{~mA} \\ 0.001 \mu \mathrm{~F} \end{gathered}$ | $\begin{aligned} & \pm 10 \mathrm{~V} \\ & \pm 5 \mathrm{~mA} \\ & 0.1 \mu \mathrm{~F} \end{aligned}$ | $\begin{aligned} & \pm 10 \mathrm{~V} \\ & \pm 5 \mathrm{~mA} \\ & 750 \mathrm{pF} \end{aligned}$ |
| $\begin{gathered} 500 \mathrm{kHz} \\ 3 \mathrm{kHz} \\ 0.2 \mathrm{~V} / \mu \mathrm{sec} \\ 3 \mathrm{sec} \\ - \end{gathered}$ | $\begin{gathered} 2.5 \mathrm{MHz} \\ 500 \mathrm{kHz} \\ 30 \mathrm{~V} / \mu \mathrm{sec} \\ - \\ - \end{gathered}$ | $\begin{aligned} & 100 \mathrm{~Hz} \\ & 2-50 \mathrm{~Hz} \\ & 100 \mathrm{~V} / \mathrm{sec} \\ & 300 \mathrm{msec} \end{aligned}$ <br> - | $\begin{gathered} 100 \mathrm{kHz}, \mathrm{G}=100 \\ 6 \mathrm{kHz} \\ 0.4 \mathrm{~V} / \mu \mathrm{sec} \\ - \\ 30 \mu \mathrm{sec}, \mathrm{G}=100 \end{gathered}$ | $\begin{gathered} 750 \mathrm{kHz} \\ 8 \mathrm{kHz} \\ 0.5 \mathrm{~V} / \mu \mathrm{sec} \\ - \\ - \end{gathered}$ |
| $\begin{gathered} \pm 15( \pm 15)( \pm 10) \mu \mathrm{V} \\ \pm 0.25( \pm 0.25)( \pm 0.1) \mu \mathrm{V} /{ }^{\circ} \mathrm{C} \\ \pm 0.1 \mu \mathrm{~V} / \% \\ \pm 5 \mu \mathrm{~V} / \mathrm{yr} . \end{gathered}$ | $\begin{gathered} \pm 50( \pm 20)( \pm 20) \mu \mathrm{V} \\ \pm 1.0( \pm 0.3)( \pm 0.1) \mu \mathrm{V} /{ }^{\circ} \mathrm{C} \\ \pm 0.2 \mu \mathrm{~V} / \% \\ \pm 2 \mu \mathrm{~V} / \mathrm{mo} \\ - \end{gathered}$ | $\begin{gathered} \pm 25 \mu \mathrm{~V} \\ \pm 0.3( \pm 0.1) \mu \mathrm{V} /{ }^{\circ} \mathrm{C} \\ \pm 0.1 \mu \mathrm{~V} / \% \\ \pm 1 / 2 \mu \mathrm{~V} / \mathrm{mo} . \end{gathered}$ | $\begin{gathered} \pm 2( \pm 1)( \pm 1 / 2)( \pm 1 / 4) \mu \mathrm{V} /{ }^{\circ} \mathrm{C}, \mathrm{G}=1000 \\ \pm 3 \mu \mathrm{~V} / \mathrm{V} \\ \pm 6 \mathrm{ppm} / \mathrm{mo} \end{gathered}$ | $\begin{aligned} & \pm 50( \pm 20)( \pm 20) \mathrm{mV} \\ & \pm 75( \pm 25)( \pm 25) \mu \mathrm{V} /{ }^{\circ} \mathrm{C} \\ & 400(300)(300) \mu \mathrm{V} / \mathrm{V} \end{aligned}$ |
| $\begin{gathered} \pm 100( \pm 100)( \pm 50) \mathrm{pA} \\ \pm 1( \pm 0.5)( \pm 0.5) \mathrm{pA} /{ }^{\circ} \mathrm{C} \\ \pm 0.2 \mathrm{pA} / \% \end{gathered}$ | $\begin{gathered} \pm 100 \mathrm{pA} \\ \pm 4( \pm 2)( \pm 1) \mathrm{pA} /{ }^{\circ} \mathrm{C} \\ \pm 0.5 \mathrm{pA} / \% \end{gathered}$ | $\begin{gathered} +\mathrm{In}= \pm 300 \mathrm{pA},-\mathrm{In}= \pm 10 \mathrm{nA} \\ \pm 10 \mathrm{pA} /{ }^{\circ} \mathrm{C} \\ \pm 3 \mathrm{pA} / \% \end{gathered}$ | $\begin{aligned} & +50 \mathrm{nA} \max \\ & -0.2 \mathrm{nA} /{ }^{\circ} \mathrm{C} \\ & +3 \mathrm{nA} / \mathrm{V} \end{aligned}$ | $50(20)(20) \mathrm{pA}$ |
| $\begin{gathered} 300 \mathrm{k} \Omega \\ \mathrm{NA} \end{gathered}$ | $\begin{gathered} 300 \mathrm{k} \Omega \\ \text { NA } \end{gathered}$ | $\begin{aligned} & 40 \mathrm{k} \Omega \\| 0.01 \mu \mathrm{~F} \\ & 10^{9} \Omega \\| 0.02 \mu \mathrm{~F} \end{aligned}$ | $\begin{gathered} 10^{9} \Omega \\| 3 \mathrm{pF} \\ 10^{9} \Omega \\| 3 \mathrm{pF} \end{gathered}$ | $\begin{aligned} & 10^{10} \Omega \\ & 10^{11} \Omega \end{aligned}$ |
| $\begin{gathered} 0.5 \mu \mathrm{~V} \\ 10 \mu \mathrm{~V} \\ 5 \mu \mathrm{~V} \\ 10 \mathrm{pA} \end{gathered}$ | $\begin{gathered} 0.7 \mu \mathrm{~V} \\ 1.5 \mu \mathrm{~V} \\ 2 \mu \mathrm{~V} \\ 2 \mathrm{pA} \end{gathered}$ | $\begin{gathered} 0.4 \mu \mathrm{~V} \max \\ 1.0 \mu \mathrm{~V} \max \\ - \\ 8 \mathrm{pA} \end{gathered}$ | $\begin{gathered} 1.0 \mu \mathrm{~V} \\ 1.0 \mu \mathrm{~V} \max \\ 1.0 \mu \mathrm{~V}, \mathrm{G}=1000 \\ 60 \mathrm{pA}, \mathrm{G}=1000, \mathrm{f}=0.01 \text { to } 10 \mathrm{~Hz} \end{gathered}$ | $5 \mu V(10 \mu V \max )(5 \mu V \max )$ |
| $\begin{array}{r} \mathrm{NA} \\ \mathrm{NA} \\ \pm 15 \mathrm{~V} \\ - \end{array}$ | $\begin{gathered} \text { NA } \\ \text { NA } \\ \pm 15 \mathrm{~V} \\ - \end{gathered}$ | $\begin{gathered} \pm 0.5 \mathrm{~V}( \pm 1.0 \mathrm{~V}) \\ 300,000 \\ \pm 20 \mathrm{~V} \\ \pm 20 \mathrm{~V} \end{gathered}$ | $\begin{gathered} \pm 10 \mathrm{~V} \\ 90 \mathrm{~dB} \min ^{2} \\ \pm V_{\mathrm{S}} \end{gathered}$ | $\begin{gathered} \pm 10 \mathrm{~V} \\ 70 \mathrm{~dB} \\ \pm 20 \mathrm{~V} \end{gathered}$ |
| $\begin{gathered} \pm(15 \text { to } 16) \mathrm{VDC} \\ \pm(12 \text { to } 18) \mathrm{VDC} \\ \pm 10 \mathrm{~mA} \max \end{gathered}$ | $\begin{gathered} \pm 15 \mathrm{VDC} \\ \pm(12 \text { to } 18) \mathrm{VDC} \\ \pm 5 \mathrm{~mA} \end{gathered}$ | $\begin{gathered} \pm(14 \text { to } 16) \mathrm{V} \\ \pm(13 \text { to } 18) \mathrm{V} \\ \pm 7 \mathrm{~mA} \end{gathered}$ | $\begin{gathered} \pm 15 \mathrm{VDC} \\ \pm(12 \text { to } 18) \mathrm{VDC} \\ \pm 2.5 \mathrm{~mA} \end{gathered}$ | $\begin{gathered} \pm 15 \mathrm{~V} \\ \pm(5 \text { to } 18) \mathrm{V} \\ 3 \mathrm{~mA} \end{gathered}$ |
| $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \\ -25^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \\ -25^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \\ -25^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \\ -25^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \\ 0 \text { to }+70^{\circ} \mathrm{C} \\ -65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C} \end{gathered}$ |
| $\begin{gathered} \text { FA-1 } \\ 1.5^{\prime \prime} \times 1.5^{\prime \prime} \times 0.62^{\prime \prime} \end{gathered}$ | $1.5^{\prime \prime} \times 1.5^{\prime \prime} \times 0.4^{\prime \prime}$ | $\begin{gathered} \mathrm{FA}-6 \\ 1.5^{\prime \prime} \times 1.5^{\prime \prime} \times 0.62^{\prime \prime} \end{gathered}$ | $2^{\prime \prime} \times 2^{\prime \prime} \times 0.4^{\prime \prime}$ | TO-99 |
| $\begin{aligned} & \$ 105(\$ 125)(\$ 158) \\ & \$ 99(\$ 119)(\$ 152) \end{aligned}$ | $\begin{aligned} & \$ 56(\$ 65)(\$ 89) \\ & \$ 51(\$ 59)(\$ 82) \end{aligned}$ | $\begin{aligned} & \$ 51(\$ 67) \\ & \$ 41(\$ 61) \end{aligned}$ | $\begin{aligned} & \$ 69(\$ 85)(\$ 98)(\$ 150) \\ & \$ 65(\$ 80)(\$ 92)(\$ 135) \end{aligned}$ | $\begin{aligned} & \$ 8.95(\$ 11.85)(\$ 14.85) \\ & \$ 8.95(\$ 11.85)(\$ 14.85) \end{aligned}$ |

## OPEN LOOP PERFORMANCE CHARACTERISTICS GENERAL PURPOSE-MODERATE PERFORMANCE <br> MODELS 118, 119 <br>  <br>  <br> 





## WIDE BANDWIDTH-FAST SETTLING





## LOW VOLTAGE DRIFT-CHOPPER STABILIZED



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ELECTROMETER- ULTRA LOW BIAS CURRENT

MODEL 41





MODEL 171
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## HOW CONVERTER PRODUCTS ARE CLASSIFIED

The converter products in this catalog are divided into four major classes:

1. Digital-to-Analog Converters in which the analog output voltage or current is generated in accordance with a digital input data word. For convenience in selection, d/a converters are subdivided into the following categories:

- General Purpose
- High Performance
- High Speed, very high speed fixed reference converters, of the types most frequently used for spot position control in CRT displays, and for construction of very fast A/D converters.
- High Resolution, converters with 16 bit resolution, having linearity and stability appropriate for true 16 bit performance.
- Multiplying, D/A converters designed for AC or varying DC reference, rather than for fixed internal or external reference.
- High Reliability, converters specifically designed for operation in the military environment.

In addition, most DAC's are available with either current output - at very high speed - or voltage output, with the added delay of an internal operational amplifier. Voltageoutput DAC's are the most convenient to use and, with the exception of those designed specifically for high speed, will serve in all but those applications calling for $\mu \mathrm{s}$ and sub- $\mu \mathrm{s}$ settling times. Current-output DAC's are used in applications where high speed is more essential than stiff voltage output, such as in circuits with comparators (e.g., A/D converters), or where fast amplification is to be provided externally (e.g., CRT deflection amplifiers).
2. Analog-to-Digital Converters in which a digital output is generated that is proportional to the value of the analog input signal. A/D converters are subdivided into the following categories:

- General Purpose
- High Performance
- High Speed Converters, with a total conversion time of $3.5 \mu \mathrm{~s}$ or less
- High Resolution Converters, offering true state-of-the-art performance in an A/D converter with 16 bit resolution and accuracy
- Low Power Converters, intended specifically for remote or portable operation from batteries

Three analog-to-digital conversion techniques are represented in Analog Devices' A/D converters. In general, the countercomparator or staircase technique permits the building of a very inexpensive converter; the dual slope integrating approach offers excellent rejection of power line noise; and the successive approximation technique is the best choice where moderate to high speed is required.
3. Multiplexers, which are high speed analog switches that provide the capability of sharing a single D/A or A/D converter among a number of analog input or output channels.
4. Sample and Hold Amplifiers which acquire and track a signal that may be varying with time and, upon command, hold the value as of a given time constant so that it can be processed accurately by following circuits (usually A/D converters).
Several types are available, which have'primary features ranging from low cost to high speed, to very high accuracy.

Other devices frequently used as accessories in conversion subsystems may be found in other sections of this product guide. These include power supplies, isolation amplifiers, instrumentation amplifiers, analog multipliers, and operational amplifiers for buffer or signal conditioning service. $\mu$ DAC IC quad switches and thin film resistor networks may be used for construction of precision D/A and A/D converters.

## HOW TO SELECT CONVERTERS

The very large number of converter products available in the marketplace can overwhelm even an experienced engineer faced with the problem of selecting a device for a given application. Interpretation of the specifications adds a nother dimension to the task, which is further complicated by the virtual absence of standardized specification definitions among the manufacturers.
Only two basic factors hold the key to selecting the right device:
A. A complete definition of the design objectives. Factors such as signal levels, accuracy required, throughput rate, a detailed knowledge of the signal and control interface, environmental conditions and several others must be well defined before selection can be effectively undertaken.
B. A firm understanding of what the manufacturer means by his set of specifications. It should not be assumed that any two manufacturers mean the same thing when they publish identical numbers defining a given parameter. In most cases, the manufacturer has honestly attempted to provide accurate information about his
product. That information must be interpreted, however, in terms meaningful to the user's requirements, and this requires a knowledge of how the terms are defined.

## Application Checklist

The designer will generally require specific information in the following categories, before proceeding to the selection process:
A. Accurate description of input and output

1. analog signal range and source or load impedance
2. digital code needed - binary, offset binary, 2's complement, BCD, etc.
3. logic level system, i.e., TTL/DTL compatible
B. What is the needed data throughput rate?
C. What are the control interface details?
D. What does the system error budget allow for the converter?
E. What are environmental conditions - temperature range, time, supply voltage - over which the converter should operate to the desired accuracy?

## Considerations For D/A Converters

A designer faced with the need to select a $\mathrm{d} /$ a converter for a specific application should usually give consideration to each of the following application details.
A. What resolution is needed? How many bits ( $8,10,12$ or other) make up the data word that will be controlling the DAC? Must the DAC be monotonic?
B. What logic levels and logic codes can be provided by the equipment that will operate the DAC? The most popular logic system is TTL, and the most frequently used codes are binary, offset binary, two's complement, binarycoded decimal, and their complements.
C. What kind of output signal from the DAC is needed for the system, a current or a voltage? What is the desired full scale range?
D. What are the speed requirements? What is likely to be the shortest time between data changes going into the DAC? After a change in the digital input data, how long can the system wait for the output signal of the DAC to settle to the desired accuracy?
E. Over how wide a temperature range (at the module) must the converter operate? Over how much of this range must the converter perform essentially within its specifications without readjustment?
F. How stable are the terminal voltages of the power supplies that will be used for powering the DAC? Is the power supply sensitivity specification adequate to hold errors from this source to reasonable limits?
These considerations are typical of those involved in the application of most converters.

## Considerations For A/D Converters

The process of selecting an A/D converter is very similar to that involved in the selection of D/A converters. The following considerations are typical.
A. What is the analog input voltage range, and to what resolution must the signal be measured?
B. What is the requirement for linearity error (or relative accuracy error)?
C. To what extent must the various sources of error be minimized as environmental temperature changes?
D. How much time can be allowed in the system for each complete conversion?
E. How stable is the system power supply? What errors will result from power supply terminal voltage variations of this order?
F. Is monotonicity important to this application, or can the system tolerate a few missed codes (out of 4096 total true codes in a 12 bit ADC, for instance). Please note the discussion of monotonicity in the section on Definitions of Specifications.
G. What is the character of the input signal? Is it noisy, sampled, filtered, rapidly-varying, slowly-varying? What kind of pre-processing is to be (or can be) done that will affect the choice (and cost) of the converter?

## Considerations For Multiplexers And Sample-And-Holds

When a sampled data system is to be assembled, in which we will time-share one A/D converter among many input channels by using a multiplexer and a sample and hold, it is important to consider the impact of these accessory devices on the system performance.

Multiplexers
A. How many input channels are needed?
B. Is each channel single-ended or differential?
C. What kind of channel address selection code is used?
D. When switching from one channel to another, how much time is needed for settling to the desired accuracy?
E. What error is produced by the leakage current passing through the source resistance?
F. If the signals are AC, how much error is produced by crosstalk between channels?
G. Is there any danger of damage to active signal sources when power is turned off? MOSFET multiplexers are inherently "safe," since the switches open when power is removed. J-FET multiplexers usually close when power is removed, making it possible to interconnect, and therefore damage, active signal sources. (The MPX-8A uses MOSFETS as switches.)
H. What will be the dynamic range of signals feeding into the multiplexer?
I. Is it desirable to be completely flexible regarding channel switching rate - even to the point of allowing the system to be stopped on one channel, for test and calibration purposes?
J. What will be the multiplexer transfer error (error produced by voltage division of the "On" resistance of a channel feeding into the input resistance of the following sample and hold)?

## Sample-and-Hold Amplifiers

A. What is the nonlinearity?
B. Considering the slewing rate of the signal, or the desired channel switching rate of the preceding multiplexer, how much time is available for acquiring the signal in the sample and hold?
C. What is the error component produced by input bias current passing through the source resistance (source resistance includes signal source resistance and the maximum "On" resistance of the multiplexer switch)?
D. What is the offset drift error (the offset temperature coefficient multiplied by the anticipated deviation of temperature)?
E. What is the offset error due to variation in the terminal voltage of the power supply we expect to provide?
In addition to the above error sources, there exists an uncertainty due to the aperture delay jitter. That is, in a sample and hold with a given aperture time (e.g. 40ns) there usually exists an aperture time uncertainty (or jitter) of perhaps 5 ns peak. The effect of aperture time is considered to be a correctable factor, since it is comparable to a delay in the sample-to-hold switching operation. The jitter cannot be compensated, however, and a 5 ns jitter applied to a signal slewing at, say, $1 \mathrm{~V} / \mu$ s produces an uncertainty of 5 mV . Since this uncertainty is directly proportional to signal slewing rate, it can be anticipated by thorough knowledge of the nature of the input signals.

## INITIAL SELECTION CRITERIA FOR SYSTEM

 COMPONENTSIt seems that the most economical process for selection of appropriate components to meet a system requirement will probably be a method of successive approximations: make an arbitrary choice, and run through a complete error analysis to check the adequacy. Where the error analysis demonstrates either performance far in excess of need (therefore possibly unnecessarily costly) or inadequate accuracy or stability, make a new choice and run through the error analysis once again.
In practice, the usual engineering criterion appears to work: for a multi-component system, choose each component to be roughly ten times better than desired in the final system.
Thus, for a system of the $0.1 \%$ desired maximum error class, use a $0.01 \%$ converter ( 12 bits) with compatible multiplexer and sample and hold. As you will see in the typical system error analysis that follows, this approach leads to quite acceptable system errors.

## THE SELECTION PROCESS

To best illustrate the complete selection process for a converter product, we have created a hypothetical situation. With this approach, one can more easily understand specification usage and applicability to a given problem.

## The Problem

A computer data acquisition system is to be built to process data from a number of strain gages. Signal conditioning hardware, to be purchased with the gages, delivers $\pm 10 \mathrm{VFS}$ signals from 10 ohm sources. Signal channels must be sequentially scanned in no more than $50 \mu$ s per channel. Maximum allowable error of the system is approximately $0.1 \%$ of FS. System logic is to be TTL, and hardware may work in either binary or two's complement code. Parallel data readout will be used.
Probable temperature range in the equipment cabinets (including equipment temperature rise) is $+25^{\circ} \mathrm{C}$ to $+55^{\circ} \mathrm{C}$. Sufficient $\pm 15 \mathrm{~V}$ and +5 V power is available, but the $\pm 15 \mathrm{~V}$ has regulation of only 150 mV . What converter products should be chosen?

## First Approximation

Since desired accuracy is about $0.1 \%$ for the system, we first choose an A/D converter with 12-bit resolution ( $0.01 \%=1 / 2$ LSB). Reviewing the available ADC's, we find the ADC-12QM to be a possible choice. Since it is packaged in a small $2^{\prime \prime} \times 4^{\prime \prime} \times 0.4^{\prime \prime}$ module, it can be conveniently incorporated in a compact subsystem.
The ADC -12 QM completes a conversion in $25 \mu \mathrm{~s}$ and, since it is felt that a sample and hold is necessary, the

SHA-1A module is chosen because it is compatible and it has settling time of $5 \mu \mathrm{~s}$. Thus, the combination of ADC -12 QM and SHA -1 A will operate in $30 \mu$ s safely within our limit of $50 \mu \mathrm{~s}$ per channel for the system.

Since multiplexer scanning will be sequential, we won't be concerned about settling time when channels are switched. The multiplexer can be switched to the next address as soon as the SHA goes into "hold" on data from the current address. Thus it has a quite adequate $30 \mu \mathrm{~s}$ to settle before a measurement is called for. For convenience, we'll use the MPX-8A as the multiplexer; the small module package fits into the packaging concept, and the built-in complete binary address decoding makes it very easy to work with.

## Error Analysis

It's clear that the MPX-8A, the SHA- 1 A and the ADC-12QM generally meet the problem's requirements for speed and resolution. Now we must look further into the details of errors, to determine if the worst case situation is within the allowable $0.1 \%$ system error.

Error Analysis of MPX-8A Multiplexer MPX-8A multiplexer, being a MOSFET circuit, is not subject to voltage offset errors. Errors here will be due to two factors:

1. Leakage current into the "ON" channel across the source impedance.

Leakage current @ $25^{\circ} \mathrm{C}=10 \mathrm{nA}$
Source impedance $=10 \mathrm{ohms}$
Error voltage $=10 \times 10^{-8}=10^{-7} \mathrm{~V}$ or 0.01 ppm for a 10 VFS signal
(certainly can be neglected)
2. Transfer error due to voltage division across MOSFET "ON" resistance and input impedance of SHA-1A.

ON resistance $=1000$ ohms $\max$
SHA-1A R $\mathrm{IN}=10^{12} \mathrm{ohms}$
$\frac{\mathrm{E}_{\text {OUT }}}{\mathrm{E}_{\mathrm{IN}}}=\frac{10^{12}}{10^{12}+10^{3}}=\frac{10^{12}}{10^{3}\left(10^{9}+1\right)}=\frac{10^{9}}{10^{9}+1}$
Transfer error $\ll 1 \mathrm{ppm}$

## Error Analysis of SHA- 1A Sample and Hold

1. Total throughput nonlinearity is 2 mV over 20 V range, or $0.01 \%$.
2. Gain error of $-0.05 \%$ max and other gain errors in the system (if small) may be compensated for overall when calibrating the system by setting of the Gain of ADC; not considered in this system's error budget.
3. Input bias current of 1 nA (typical) causes an offset error
voltage in the source resistance.
Source resistance equals sum of "ON" resistance of MPX-8A and signal source resistance: 1010 ohms total Offset error $=1.01 \times 10^{3} \times 10^{-9}=1.01 \times 10^{-6} \mathrm{~V}$ out of 10 VFS , or 0.1 ppm .
4. Offset vs temp $=25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$.

Our housing temperature may change by $30^{\circ} \mathrm{C}$. Offset error $=25 \mu \mathrm{~V} \times 30=750 \mu \mathrm{~V}$ out of 10 V , or $0.0075 \%$.
5. Offset vs Supply $=100 \mu \mathrm{~V} / \%$.

Supply may move 150 mV out of 15 V , or $1 \%$.
Offset error is therefore $100 \mu \mathrm{~V}$ out of $10 \mathrm{~V}, 0.001 \%$.
By an analysis similar to the above, we would normally also prepare a system timing diagram, and assign operating time and settling time allowances. However, the components selected for this example allow several times more settling time than needed for $0.01 \%$ operation, consequently we can overlook the need for a formal timing analysis to determine whether settling times are adequate.

Error Analysis of ADC-12QM A/D Converter

1. Linearity error (relative accuracy) $1 / 2$ LSB or $0.01 \%$
2. Quantizing uncertainty; $1 / 2 \mathrm{LSB}$ or $0.01 \%$. This is a resolution limitation, not considered in the error budget.
3. Temperature errors:
a) Gain Tempco $5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ for our $30^{\circ} \mathrm{C}$ possible shift; 150 ppm total
Gain error: 150 ppm or $0.015 \%$
b) Zero Tempco $5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$

Zero error: 0.015\%
4. Power supply sensitivity error

Sens $=0.002 \% / \%$. Power supply may move $1 \%$,
therefore PS error $=0.002 \%$
In conclusion, the following is a summary of the significant sources of error in the system:

| SHA linearity error | $0.01 \%$ |
| :--- | :--- |
| SHA offset vs temp error | $0.0075 \%$ |
| SHA supply offset error | $0.001 \%$ |
| ADC linearity error | $0.01 \%$ |
| ADC gain tempco error | $0.015 \%$ |
| ADC zero tempco error | $0.015 \%$ |
| ADC supply offset error | $0.002 \%$ |
| Worst case sum of all errors: | $\approx 0.06 \%$ |
| Square root of sum of squares: | $\approx 0.03 \%$ |

Since these values are certainly reasonable for a system with specification error of $0.1 \%$, we should be satisfied that we have made reasonable choices in components.

## DEFINITION OF SPECIFICATIONS


#### Abstract

Absolute Accuracy Absolute accuracy error of a D/A converter is the difference between the analog output that is expected when a given digital code is applied and the output that is actually measured with that code applied to the converter.


Absolute accuracy error of an A/D converter is the difference between the analog input theoretically required to produce a given digital output code and the analog input actually required to produce that same code. Since a band of analog values can produce the same code, the "input required to produce a given digital output code" is defined as the midpoint of either the theoretical or the measured band.

Absolute accuracy error can be caused by gain error, zero error, linearity error, or any combination of the three. Absolute accuracy measurements should be made under a set of standard conditions with sources and meters traceable to an internationally accepted standard.

## Acquisition Time

The acquisition time of a sample and hold circuit is the time it takes to acquire the input signal to the given accuracy. Specifications on acquisition time given in Analog Devices' data sheets include the settling time of the output amplifier. Some manufacturers do not include settling time of the output amplifier when specifying acquisition time.

## Aperture Time

This is the time it takes in a sample and hold circuit, for the switch to open after the control command has been given. In a good SHA, this should not exceed 50 ns delay, including 10 ns uncertainty.

## Common-Mode Range

Common-mode rejection usually varies with the magnitude of the common-mode plus the differential (or "normal" mode) voltage applied to an amplifier. Common-mode range is that range of total input voltage over which optimum common-mode rejection is maintained. In good operational amplifiers, the common mode range is usually of the order of $\pm 10 \mathrm{~V}$.

## Common Mode Rejection (CMR)

The ability of an amplifier to reject the effect of voltage applied to both input terminals simultaneously. Usually expressed as the log of a "common-mode rejection ratio," i.e. $1,000,000: 1$ (CMRR) or 120 dB (CMR). A CMRR of $1,000,000$ to 1 means that a 1 V common-mode voltage passes through the amplifier as though it were a differential signal of one microvolt at the input.

## Common-Mode Voltage

An undesirable signal picked up in a transmission line by both wires making up the circuit, with reference to an arbitrary "ground." Amplifiers differ in their ability to amplify a desired signal accurately in the presence of a common-mode voltage.

## Conversion Time

The time required for a complete measurement by an analog-to-digital converter is called conversion time. In successive approximations converters, conversion times are available between $1.0 \mu \mathrm{~s}$ for the 8 bit version of the ADC1103 and $400 \mu \mathrm{sec}$ (for the ADC-16Q). The most popular general
purpose A/D converters, like the ADC-12QM, have conversion time of about $25 \mu \mathrm{~s}$.

## Crosstalk

Leakage of signals between circuits or channels of a multichannel system or device, such as a multiplexer. Crosstalk is usually determined by the impedance parameters of the physical circuit, and actual values are frequency-dependent.

## Deglitcher

When a D/A increases or decreases the input code by small changes, it passes through what is known as major and minor transitions. The major transition is at half-scale, when the $\mathrm{D} / \mathrm{A}$ switches around the MSB, and all switches change state, i.e., 01111111 to 10000000 . If the switches are faster to switch off than on, this means that, for a short time, the D/A will give a zero output and then return to the required 1 LSB above the previous reading. This large transient spike is commonly known as a "glitch," and hence, a "deglitcher" is a device which removes these glitches. It normally consists of a hold-sample circuit which holds the output constant until the switches reach equilibrium.


## Differential Linearity

Any two adjacent digital codes should correspond to analog values that are exactly 1 LSB apart ( $2^{-n}$ of full scale, for an n-bit converter). Any deviation of the measured "step" from the ideal difference is called Differential Nonlinearity. It is an important specification, because a differential nonlinearity error greater than 1LSB can lead to nonmonotonic behavior of a D/A converter, and missed codes in an A/D converter.
"Analog values," for a D/A converter, are the actual measured outputs; for an A/D converter, they are the midpoints of the quantization bands at each of the adjacent codes (if the codes exist).

## Droop Rate

When a sample-and-hold circuit using a capacitor for storage is in hold, it will not hold the information forever; droop rate is the rate at which the output voltage changes and, hence, loses the information. In practice, when using a SHA ahead of an ADC, the SHA should not droop more than 0.1 LSB during the conversion time of the ADC.

## Dual-Slope Converter

An integrating analog-to-digital converter in which the unknown signal is converted to a proportional time interval, which is then measured digitally. This is done by integrating the unknown for a predetermined time. Then a reference input is switched to the integrator, and integrates "down"
from the level determined by the unknown until a "zero" level is reached. The time for the second integration process is proportional to the average of the unknown signal level over the predetermined integrating period. A digital time interval meter (i.e., counter) is generally used as the output indicator.


## Four-Quadrant

In a multiplying DAC, "four-quadrant" refers to the fact that both the reference signal and the number represented by the input may be bipolar. A four-quadrant multiplier is expected to obey multiplication rules for algebraic sign.

## Feedthrough

A term referring to that characteristic of a circuit or device manifested by undesirable signal leakage around switches or other devices that are supposed to be turned off or provide isolation.

## Gain Adjustment

The "gain" of a converter is that analog scale factor setting that provides the nominal conversion relationship, e.g. 10 V full scale.

## Hold-to-Sample Transient

In a sample-and-hold amplifier, a switching transient usually occurs when switching from "HOLD" to "SAMPLE" modes. Such transients effectively slow the process of settling-in on the desired signal.

## Least Significant Bit (LSB)

In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the "least significant bit" is that digit (or "bit") that carries the smallest value or weight. For example, in the natural binary number 1101 (decimal 13 , or $2^{3}+2^{2}+0+1$ ), the rightmost " 1 " is the LSB.

## Linearity

Linearity error of a converter is the deviation of the analog values, in a plot of the measured conversion relationship, from a straight line. The straight line can be either a "best straight line," determined empirically by manipulation of the gain and/ or offset to equalize maximum positive and negative deviations

a. $1 / 2$ LSB Nonlinearity Achieved By Arbitrary Location of "Best Straight Line".
b. Nonlinearity Reference is Straight Line Through End Points. Nonlinearity >1⁄2LSB for Curve of a.

> Comparison of Linearity Criteria for 3-Bit D/A Converter. Straight Line Through End Points is Easier to Measure, Gives MoreConservative Specification.
of the actual transfer characteristic from this straight line; or, it can be a straight line passing through the end points of the transfer characteristic after they have been calibrated. Sometimes referred to as "end-point" nonlinearity, the latter is the definition used by Analog Devices, both because it is a more conservative measure, and because it is much easier to verify in actual practice. "End-point" nonlinearity is similar to relative accuracy error (see Relative Accuracy).

For Multiplying D/A converters, the analog linearity error at a given digital code is defined in the same way as for multipliers, i.e., by deviation from a "best straight line" through the plot of the analog output-input response.

## Line Regulation <br> Load Regulation

Stability parameters of a power supply: the variation of output voltage as a fraction of changes in input line voltage
or load current. These are among the most important specifications of a regulated supply. Regulation is often specified in terms of change in output (in either \% or volts) per incremental change in line voltage or load current (in either \% or actual change).

## Monotonic

A monotonic D/A or A/D converter never has its output decrease in response to an increasing input stimulus (or vice versa). In high-speed converters, it is not especially hard to produce a monotonic design over limited temperature ranges. In order to be monotonic over very wide temperature ranges, error components of DAC switches and resistor networks must track each other very closely with temperature change. In ADC's, the counterpart of non-monotonic behavior is the "missed code," which is produced when a transition from one quantum of the analog range to the adjacent one does not result in the adjacent digital code, but in one removed by one or more counts. Monotonic behavior in high-resolution conversion over wide temperature ranges is not easy to accomplish at the present state of the art ; consequently, converters like the $\mathrm{ADC}-\mathrm{QM}$, which are monotonic from $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$, at reasonable cost, are not commonly seen in the industry. Integrating converters, such as the ADC-I, are inherently monotonic; A/D converters of this class are also inherently slow (usually more than 35 ms for a full conversion).

## Most Significant Bit (MSB)

In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the "most significant bit" is that digit (or "bit") that carries the largest value or weight. For example, in the natural binary number 1101 (decimal 13 , or $2^{3}+2^{2}+0+1$ ), the leftmost " 1 " is the MSB, with a weight of $2^{\mathrm{n}-1}$, or 8 .

## Multiplying DAC

A multiplying DAC differs from the conventional fixedreference DAC in being designed to operate with varying (or AC) reference signals. The output signal of such a DAC is proportional to the product of the reference voltage and the fractional equivalent of the digital input number.

## Noise, Peak

Peak: The peak noise output of a DAC being an analog signal, can be an important consideration, especially in high resolution DACs, such as the DAC-14QM and DAC-16QM. The resolution is not confidently assignable when the peak noise exceeds the LSB value for a reasonable bandwidth.

For an ADC, input circuit noise may impart statistical properties to the input numbers and require additional processing for successful interpretation.

## Noise, RMS

RMS: For Gaussian noise, the RMS noise should be oneseventh of the specified peak-to-peak noise, for less than $0.1 \%$ probability of encountering greater noise peaks. Both specs should be looked at very carefully, as large spikes could be present on the output from a chopper-stabilized amplifier (or coupled into the system). These spikes will contribute very little to driving the RMS noise out of spec, but could nevertheless be of considerable amplitude. If such a DAC is used in a display system, the noise will cause distortion of the pattern and hence, loss of useful resolution.

## Offset

For almost all bipolar converters (e.g., $\pm 10$ volts output) instead of actually generating negative currents to correspond to negative numbers, a unipolar DAC is used, and the output is offset by half full scale (1MSB). For best results, this offset voltage or current is derived from the same reference supply that determines the gain of the converter.
This makes the zero point of the converter independent of thermal drift of the reference. This is because the $1 / 2$ scale offset completely cancels the weight of the MSB at zero, independently of the amplitude of both.

TRANSFER CHARACTERISTICS


## "ON" Resistance

"ON" resistance of a device such as a FET, when used as a switch performing a function (such as multiplexing), refers to the ohmic resistance while turned on. For multiplexer service, a few hundred ohms or less will usually provide adequate accuracy. For other switching service, such as in a DAC, values of 10 ohms or less are desirable.

## Power Supply Sensitivity

The sensitivity of a converter to changes in the power supplies is normally expressed in terms of percentage change in analog value ( $D / A$ output, $A / D$ input) for a one percent change in power supply; e.g. $0.05 \% / \%$ change in reading per volt change in power supply. For all good converters, the fractional change in reading should not be more than the \% equivalent of $\pm 1 / 2$ LSB at full scale for a $3 \%$ change in power supply.
When power supply voltage changes affect conversion accuracy excessively, the trouble can usually be traced to a marginal "constant-current"-circuit design for the reference zener diode.

## Quantizing Uncertainty (or "Error")

The a nalog continuum is partitioned into $2^{\mathrm{n}}$ discrete ranges for n -bit conversion. All analog values within a given range are represented by the same digital code, usually assigned to the nominal midrange value. There is, therefore, an inherent quantization uncertainty of $\pm 1 / 2 L S B$, in addition to the actual conversion errors.

## Relative Accuracy

Relative accuracy error is the deviation of the analog value at any code (relative to the full analog range of the device transfer characteristic) from its theoretical value (relative to the same range), after the full-scale range has been calibrated.
Since the discrete points on the theoretical transfer characteristic lie on a straight line, this deviation can also be interpreted as a measure of nonlinearity (see Linearity).
The "discrete points" of a D/A transfer characteristic are measured by the actual analog outputs. The "discrete points" of an A/D transfer characteristic are the midpoints of the quantization bands at each code (see Absolute Accuracy).

## Settling Time

This is the time it takes for a DAC to settle for a full scale change, usually to within $\pm 1 / 2$ LSB. For example, for the DAC- ${ }^{-}$2QS, the settling time is specified as $5 \mu \mathrm{~s}$ max, which is the time for a 0 to +10 volt change and settling to $< \pm 0.012 \%$ ( $1 / 2$ LSB of 12 bits). Another very important settling time characteristic is the settling time of a single LSB change, for example, in digital sweep generation.

## Slew Rate (or Slewing Rate)

Slew rate in an operational amplifier is a limitation in the rate of change of output voltage, usually imposed by some basic circuit consideration, such as limited current to charge a capacitor. Amplifiers with slew rate of a few volts $/ \mu \mathrm{s}$ are common, and moderate in cost. Slew rates greater than about 75 volts/ $\mu$ s are usually seen only in more sophisticated (and expensive) devices. The output slewing speed of a modern D/A converter is usually limited by the slew rate of the amplifier used at its output.

## Stability

Stability of a converter usually applies to the insensitivity of its characteristics with time, temperature, etc. All measurements of stability are difficult and time consuming,
but stability vs. temperature is sufficiently critical in most applications to warrant universal inclusion in tables of specifications. (See "Temperature Coefficient.")

## Staircase

A waveform having the appearance of a staircase.


TIME

A very simple A/D converter, of low cost, c in be built utilizing a staircase from a DAC, (generated by a digital count at its input) for comparison with the unknown input. The ADC-8S is a converter of this type.

## Successive Approximations

Successive approximations is a high speed method of comparing an unknown against a group of weighted references. The operation of a successive approximations A/D converter is generally similar to the orderly weighing of an unknown quantity on a precision chemical balance, using a set of weights such as: 1 gram, 1/2 gram, 1/4 gram, 1/8 gram, $1 / 16$ gram, etc.

## Switching Time

In a DAC, the switching time is the time it takes for the switch to change from one state to the other ("delay time" plus "rise time" from $10 \%-90 \%$ ), but does not include settling time, e.g. to $< \pm 1 / 2$ LSB.

## Temperature Coefficient

Gain: The gain of all converters will change with temperature due to two main causes.
a) The reference zener itself will have a temperature coefficient. A good zener will have a TC of $<5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$.
b) The reference circuitry and switches will add about another $3 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \max$ in very good converters. The total gain change with temperature will then be specified as $x$ parts per million change per ${ }^{\circ} \mathrm{C}$.
Unipolar Zero: The temperature stability of a unipolar DAC is almost entirely due to the voltage zero stability of the output amplifier. As the output amplifiers are normally current-to-voltage converters, they are always running at a voltage gain not too different from unity, hence, the unipolar DAC zero T.C. can be expressed in $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ and will be independent of gain setting, i.e., $0-5 \mathrm{~V}$ or $0-10 \mathrm{~V}$.

For an ADC, similar arguments apply, and its T.C. is dependent only on the voltage zero stability of the input buffer and comparator and, again, is usually expressed in $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ (of input).
Bipolar Offset: The temperature coefficient of the minus full scale point or offset of a bipolar converter is dependent on three variables:

1) The T.C. of the zener reference diode
2) The voltage zero stability of the output amplifier or input buffer and comparator
3) The tracking capability of the bipolar-offset resistors and the gain resistors.
The temperature coefficient of the minus full scale point will be specified in $\mathrm{ppm} /{ }^{\circ} \mathrm{C}$ on the above specifications, since that is the normal "all-DAC-switches-off" point.

## Transfer Accuracy

Refers to the loss of accuracy that results from the insertion of a less-than-perfect signal handling circuit into a measurement circuit.

Zero
The zero of a $0-10 \mathrm{~V}$ DAC is set to zero volts for an all-0's input code. For an ADC, the first transition is offset by one-half LSB so that all subsequent transitions occur midway between the nominal code values. That is, only $1 / 2$ LSB of analog input is required before the LSB switches on.


## HOW TO ADJUST ZERO AND GAIN OF CONVERTERS

Proper adjustment of zero and gain in DAC's and ADC's is a procedure that requires great care, and the use of extremely sensitive reference instruments. The voltmeter used to read the output of a DAC, or the voltage source used as a driving signal for the ADC, must be capable of stable and clear resolution of $1 / 10$ LSB at both ends of the range of the converter; e.g., at zero and full scale.

| Converter | Converter Range |  |  |
| :--- | :---: | :--- | :---: |
| Resolution | 20 V | 10 V | 5 V |
| 8 bits | 39.06 mV | 19.53 mV | 9.77 mV |
| 10 bits | 9.77 mV | 4.88 mV | 2.44 mV |
| 12 bits | 2.44 mV | 1.22 mV | $610 \mu \mathrm{~V}$ |
| 14 bits | $610 \mu \mathrm{~V}$ | $305 \mu \mathrm{~V}$ | $153 \mu \mathrm{~V}$ |
| 16 bits | $153 \mu \mathrm{~V}$ | $76 \mu \mathrm{~V}$ | $38 \mu \mathrm{~V}$ |

Table 1. Voltage Equivalent of $1 / 2$ LSB for
Various Resolutions and Voltage Ranges

Most DAC's and successive approximation ADC's manufactured by Analog Devices are provided with Zero and Gain adjustments which are completely independent of each other, as long as the adjustment of Zero is attempted only when the actual conversion circuit is producing Zero, and as long as the Zero (or Offset) adjustment is accurately completed before proceeding to adjustment of Gain (at full scale-1LSB). Of course, it is possible to make Zero and Gain adjustments in reverse order and at other points on the transfer function - but it must be expected that the adjustments will no longer be independent, and the procedure will require a series of successive approximations.

## Adjustment Process

Particularly for bipolar converters, fast and successful adjustment requires knowledge of the technique used in the circuit to convert the inherently unipolar DAC or ADC for bipolar operation.

1. Sign \& Magnitude Codes are generally obtained by use of a unipolar converter with separate means of reversing polarity. The Zero adjustment is always made by calling for a zero from the converter. (Logic zero into a DAC produces zero volts output, or zero volts into an ADC produces data zero output.)
2. Bipolar binary converters utilizing offset binary or two's complement coding usually employ analog offsetting to convert a unipolar design into bipolar. For instance, a 0 to +10 V DAC may have its output amplifier offset by -5 V , resulting in an output of -5 volts corresponding to 000000 input and +5 volts (minus 1 LSB ) corresponding to a 111111 input. Such a converter should have its "Zero" adjusted at -5 V .

An alternate explanation is as follows: converter Zero controls should always be set at the "All Bits Off" condition, and then Gain should be set at the "All Bits On" condition.

## Adjustment For DAC's

ZERO : set input code so that all bits are "off", then adjust pot until output signal is within $1 / 10 \mathrm{LSB}$ of proper reading, or zero.

GAIN: set input code so that all bits are "on", then adjust pot until output signal reads within $1 / 10$ LSB of Full Scale less $1 L S B$.

## Adjustment For ADC's

ZERO: set input voltage precisely at $1 / 2$ LSB above the "all bits off" specified input. Zero control should be adjusted so that the converter just switches in its LSB.

GAIN: set input voltage precisely at $1 / 2$ LSB less than "all bits on" input. Note that this is $11 / 2$ LSB's less than the nominal full scale value: i.e., all 1's value of a zero to +10 V 12 -bit ADC is actually +9.9976 . Gain adjustment should be made with an input $1 / 2$ LSB less, or +9.9962 volts. With input voltage set as described, GAIN control is rotated to the point where the last bit just comes on. For instance, in a 12 bit binary converter, reading of 1111111111110 would change to 111111111111 .

## GENERAL SPECIFICATIONS COMMON TO MOST ANALOG DEVICES CONVERTER PRODUCTS

In order to simplify the presentation of specification information in the converter section of this catalog, a number
of specification parameters common to most of the product line were omitted from the details in each table. They are:

1. All logic interfaces are compatible with TTL and DTL except for the model ADC-12QL and model AD1123 which are compatible with CMOS.
2. Positive true is our convention in defining all codes.
3. Most products are designed to operate over an ambient temperature range of $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$. Certain products are also available in extended temperature versions.
4. All converters are designed to have maximum linearity error of $< \pm 1 / 2 \mathrm{LSB}$ @ $+25^{\circ} \mathrm{C}$.
5. All Analog to Digital converters have internal clocks.
6. All Analog to Digital converters (except the ADC1105 which uses external logic) provide a status signal for interface to system controls.
7. All products are designed with very high rejection of variations in the power supply, and errors due to variations of several millivolts in the $\pm 15 \mathrm{~V}$ supplies can almost always be neglected.

Complete details of the performance specifications of Analog Devices products are listed on individual data sheets on each product, available upon request.

## CONVERTER PRODUCTS FOR EXTENDED TEMPERATURE SERVICE

Most converter products described in this catalog are intended for operation over the temperature range of 0 to $+70^{\circ} \mathrm{C}$. Performance of these converters does not usually deteriorate abruptly beyond these temperature limits, but rather degrades gradually, and finally may become unpredictable.
Several converters can be supplied in versions capable of stable operation over an extended temperature range. These ET versions are available only in the binary codes (i.e., ET versions of BCD coded units are not available).
The 8 and 10 -bit converters are specified over the range of $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$; the 12 bit converters are specified over the range of $-55^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$. All ET converters are individually tested at high, low, and room temperatures prior to shipment.
The table below shows the maximum TC's to be expected over the full ET operating temperature range. For example, a 12-bit DAC-12QS/ET would have a maximum gain TC of $\pm 11 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ from $-25^{\circ} \mathrm{C}$ to $0, \pm 7 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ from 0 to $+70^{\circ} \mathrm{C}$, and $\pm 12 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ from $+70^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$.

The most commonly requested and readily available ET converters are shown below. The extended temperature version is ordered by adding /ET to the standard model number.

| Model | Price (1-9) | Details on Page |
| :--- | :---: | :---: |
| DAC-12QM/ET | $\$ 362$ | 84 |
| DAC-12QS/ET | $\$ 299$ | 84 |
| DAC-10QS/ET | $\$ 268$ | 84 |
| DAC-8QS/ET | $\$ 221$ | 84 |
| ADC-12QM/ET | $\$ 483$ | 96 |
| ADC-10QM/ET | $\$ 441$ | 96 |
| ADC-8QM/ET | $\$ 394$ | 96 |
| ADC-12QU/ET | $\$ 494$ | 96 |

## TEMPERATURE COEFFICIENTS

|  | $-55^{\circ} \mathrm{C}$ to 0 | $-25^{\circ} \mathrm{C}$ to 0 | 0 to $+70^{\circ} \mathrm{C}$ | $+70^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | $+70^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 12 bit Models |  |  |  |  |  |
| Diff. Linearity |  | $\pm 5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 3 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 4.5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |  |
| Gain |  | $\pm 11 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 7 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 12 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |  |
| Zero (Unipolar) |  | $\pm 45 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $\pm 50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $\pm 50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ |  |
| Offset (Bipolar) |  | $\pm 6 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 6 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |  |
| 10 bit Models |  |  |  |  |  |
| Diff. Linearity | $\pm 15 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |  | $\pm 3 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |  | $\pm 12 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |
| Gain | $\pm 15 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |  | $\pm 7 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |  | $\pm 18 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |
| Zero (Unipolar) | $\pm 45 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ |  | $\pm 50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ |  | $\pm 50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ |
| Offset (Bipolar) | $\pm 12 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |  | $\pm 5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |  | $\pm 12 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |
| 8 bit Models |  |  |  |  |  |
| Diff. Linearity | $\pm 30 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |  | $\pm 3 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |  | $\pm 25 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |
| Gain | $\pm 60 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |  | $\pm 7 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |  | $\pm 50 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |
| Zero (Unipolar) | $\pm 45 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ |  | $\pm 50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ |  | $\pm 50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ |
| Offset (Bipolar) | $\pm 50 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |  | $\pm 5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |  | $\pm 50 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |

These figures include 20\% guard band over engineering test specs.

## CAPSULE SELECTION TABLE

DIGITAL-TO-ANALOG CONVERTERS
SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ unless otherwise noted)

| Product Classification | Model ${ }^{1}$ | Resolution | Linearity <br> Error | Input Code Options ${ }^{2}$ (TTL/DTL Compatible) | Input Register | Output Options | Settling Time to \% of Full Scale | $\begin{aligned} & \text { Gain } \\ & \mathrm{TC}^{4} \end{aligned}$ | Power Requirements | Package Size \& Style | $\begin{aligned} & \text { Price } \\ & (1-9) \end{aligned}$ | Price $(100+)$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| General Purpose | DAC-12QZ <br> DAC-10Z <br> MDA-10Z <br> DAC1009 <br> DAC1118 | 12 bits 10 bits 10 bits 12 bits 12 bits | $\begin{gathered} \pm 0.0125 \% \\ \pm 0.05 \% \\ \pm 0.05 \% \\ \pm 0.0125 \% \\ \pm 0.0125 \% \end{gathered}$ | $\left\{\begin{array}{c} \text { C-B, COB, CBD } \\ \text { BIN, OBN } \\ \text { BIN, OBN, BCD } \\ \text { BIN, OBN, } 2 S C, B C D \end{array}\right.$ | $\begin{array}{r} \text { NO } \\ \text { NO } \\ \text { NO } \\ \text { NO } \\ \text { YES } \end{array}$ | $\begin{gathered} \pm 5 \mathrm{~V}, \pm 10 \mathrm{~V}, \pm 2.5 \mathrm{~V},+5 \mathrm{~V},+10 \mathrm{~V} \\ -10 \mathrm{~V}, \pm 10 \mathrm{~V} \\ +2 \mathrm{~mA}, \pm 1 \mathrm{~mA} \\ \} \pm 2.5 \mathrm{~V}, \pm 5 \mathrm{~V}, \pm 10 \mathrm{~V} \\ +5 \mathrm{~V},+10 \mathrm{~V} \end{gathered}$ | $5 \mu \mathrm{~s}$ to $0.01 \%$ <br> $5 \mu \mathrm{~s}$ to $0.05 \%$ <br> 300ns to $0.05 \%$ <br> $4 \mu \mathrm{~s}$ to $0.01 \%$ <br> $5 \mu \mathrm{~s}$ to $0.01 \%$ | $\begin{aligned} & \pm 30 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ & \pm 30 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ & \pm 30 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ & \pm 11 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ & \pm 20 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \end{aligned}$ | $\begin{gathered} \pm 15 \mathrm{~V},+5 \mathrm{~V} \\ \pm 15 \mathrm{~V} \\ \pm 15 \mathrm{~V} \\ \pm 15 \mathrm{~V} \\ \pm 15 \mathrm{~V},+5 \mathrm{~V} \end{gathered}$ | $\left\{\begin{array}{l} 2^{\prime \prime} \times 2^{\prime \prime} \times 0.4^{\prime \prime}, \mathrm{C}-1 \\ 2^{\prime \prime} \times 4^{\prime \prime} \times 0.4^{\prime \prime}, \mathrm{C}-3 \end{array}\right.$ | $\begin{array}{rr} \$ & 79 \\ \$ & 49 \\ \$ & 49 \\ \$ & 84 \\ \$ & 112 \end{array}$ | $\begin{aligned} & \$ 47 \\ & \$ 27 \\ & \$ 27 \\ & \$ 54 \\ & \$ 80 \end{aligned}$ |
| High <br> Performance | DAC-8QS <br> DAC-10QS <br> DAC-12QS | 8 bits 10 bits 12 bits | $\begin{gathered} \pm 0.2 \% \\ \pm 0.05 \% \\ \pm 0.0125 \% \end{gathered}$ | C-B, COB, CBD | NO | $\left\{\begin{array}{c}  \pm 2.5 \mathrm{~V}, \pm 5 \mathrm{~V}, \pm 10 \mathrm{~V} \\ +5 \mathrm{~V},+10 \mathrm{~V} \end{array}\right.$ | $5 \mu \mathrm{~s}$ to 0.01\% | $\pm 7 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 15 \mathrm{~V},+5 \mathrm{~V}$ | $2^{\prime \prime} \times 2{ }^{\prime \prime} \times 0.4$ ", C-1 | $\begin{aligned} & \$ 147 \\ & \$ 179 \\ & \$ 200 \end{aligned}$ |  |
|  | DAC-8QM <br> DAC-10QM <br> DAC-12QM | 8 bits 10 bits 12 bits | $\begin{gathered} \pm 0.2 \% \\ \pm 0.05 \% \\ \pm 0.0125 \% \end{gathered}$ | BIN, OBN, 2SC, BCD | YES | $\} \begin{gathered} \pm 2.5 \mathrm{~V}, \pm 5 \mathrm{~V}, \pm 10 \mathrm{~V} \\ +5 \mathrm{~V},+10 \mathrm{~V}\end{gathered}$ | $5 \mu$ s to 0.01\% | $\pm 7 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 15 \mathrm{~V},+5 \mathrm{~V}$ | $2^{\prime \prime} \times 4^{\prime \prime} \times 0.4{ }^{\prime \prime}, \mathrm{C}-3$ | $\begin{array}{ll} \$ & 179 \\ \$ 221 \\ \$ & 242 \end{array}$ |  |
| Fast, Display | DAC-10DF <br> MDA-8F <br> MDA-10F <br> DAC1106-001 <br> DAC1106-002 | 10 bits 8 bits 10 bits 8 bits 10 bits | $\begin{array}{r}  \pm 0.05 \% \\ \pm 0.2 \% \\ \pm 0.05 \% \\ \pm 0.2 \% \\ \pm 0.05 \% \end{array}$ | $\begin{aligned} & \text { OBN, } 2 \mathrm{SC} \\ & \text { BIN, OBN } \\ & \text { BIN, OBN } \end{aligned}$ | $\begin{gathered} \text { YES } \\ \text { NO } \\ \text { NO } \\ \text { NO } \\ \text { NO } \end{gathered}$ | $\left\{\begin{array}{l}  \pm 2.5 \mathrm{~V}, \pm 5 \mathrm{~V}, \pm 10 \mathrm{~V} \\ \pm 2.3 \mathrm{~mA},+4.7 \mathrm{~mA} \\ \}+5 \mathrm{~mA}, \pm 2.5 \mathrm{~mA} \end{array}\right.$ | 500ns to $0.05 \%$ <br> 40 ns to $0.05 \%$ <br> 40ns to $0.05 \%$ <br> 25 ns to $0.2 \%$ <br> 50ns to $0.05 \%$ | $\begin{aligned} & \pm 50 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ & \pm 25 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ & \pm 25 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ & \pm 10 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ & \pm 10 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \end{aligned}$ | $\begin{gathered} \pm 15 \mathrm{~V},+5 \mathrm{~V} \\ \pm 15 \mathrm{~V} \\ \pm 15 \mathrm{~V} \\ \pm 15 \mathrm{~V} \\ \pm 15 \mathrm{~V} \end{gathered}$ | $\begin{gathered} 4^{1 / 2 \prime} \times 6^{\prime \prime}, \mathrm{C}-8 \\ 2^{\prime \prime} \times 4^{\prime \prime} \times 0.4^{\prime \prime}, \mathrm{C}-3 \\ \} 2^{\prime \prime} \times 2^{\prime \prime} \times 0.4^{\prime \prime}, \mathrm{CA}-1 \end{gathered}$ | $\begin{aligned} & \$ 520 \\ & \$ 254 \\ & \$ 277 \\ & \$ 119 \\ & \$ 139 \end{aligned}$ |  |
| High <br> Resolution | DAC-14QG <br> DAC-16QG <br> DAC-14QM <br> DAC-16QM | 14 bits <br> 16 bits <br> 14 bits <br> 16 bits | $\begin{gathered} \pm 0.003 \% \\ \pm 0.0015 \% \\ \pm 0.003 \% \\ \pm 0.0015 \% \end{gathered}$ | $\begin{aligned} & \} \begin{array}{l} \text { BIN, OBN, 2SC } \\ \text { BCD, SMB, SMD } \end{array} \\ & \} \text { C-B, COB, CBD } \end{aligned}$ | $\begin{gathered} \text { OPTIONAL } \\ \text { OPTIONAL } \\ \text { NO } \\ \text { NO } \\ \hline \end{gathered}$ | $\begin{gathered} \} \pm 5 \mathrm{~V}, \pm 10 \mathrm{~V},+10 \mathrm{~V} \\ \left\{\begin{array}{c}  \pm 5 \mathrm{~V}, \pm 10 \mathrm{~V},+10 \mathrm{~V} \\ \\ \pm 1 \mathrm{~mA},-2 \mathrm{~mA} \end{array}\right. \end{gathered}$ | $250 \mu$ s to $0.0015 \%$ | $\pm 7 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 15 \mathrm{~V},+5 \mathrm{~V}$ | $\begin{aligned} & \left\{4^{1 / 2 \prime \prime} \times 44^{1 / 4^{\prime \prime}}, \mathrm{C}-8\right. \\ & \} 2^{\prime \prime} \times 4^{\prime \prime} \times 0.4^{\prime \prime}, \mathrm{C}-3 \end{aligned}$ | $\begin{aligned} & \$ 840^{5} \\ & \$ 1207^{5} \\ & \$ 415 \\ & \$ 782 \end{aligned}$ |  |
| Multiplying ${ }^{3}$ | $\begin{gathered} \text { DAC-8M } \\ \text { DAC-12M } \\ \text { MDA-11MF } \end{gathered}$ | 8 bits 12 bits 11 bits | $\begin{gathered} \pm 0.2 \% \\ \pm 0.02 \% \\ \pm 0.03 \% \end{gathered}$ | BIN, OBN | NO | $\} \begin{gathered} \pm 10 \mathrm{~V} \\ \pm 2 \mathrm{~mA},+4 \mathrm{~mA} \end{gathered}$ | $\begin{gathered} 10 \mu \text { s to } 0.2 \% \\ 15 \mu \text { s to } 0.01 \% \\ 1.0 \mu \text { s to } 0.01 \% \end{gathered}$ | $\pm 25 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 15 \mathrm{~V}$ | $\begin{array}{r} \} 2^{\prime \prime} \times 2^{\prime \prime} \times 0.4^{\prime \prime}, \mathrm{C}-1 \\ 2^{\prime \prime} \times 4^{\prime \prime} \times 0.4^{\prime \prime}, \mathrm{C}-3 \end{array}$ | $\begin{aligned} & \$ 205 \\ & \$ 310 \\ & \$ 158 \end{aligned}$ |  |
| Integrated Circuit ${ }^{6}$ | AD562 AD7520 (CMOS) | 12 bits <br> 10 bits | $\pm 0.006 \%$ <br> $\pm 0.05 \%$ | BIN, BCD BIN | NO NO | $\begin{gathered} 2 \mathrm{~mA} \text { or } \pm 1 \mathrm{~mA}^{7} \\ 1 \mathrm{~mA}^{7} \end{gathered}$ | $\begin{aligned} & 1.5 \mu \mathrm{~s} \text { to } 0.01 \%^{8} \\ & 500 \text { ns to } 0.05 \% \end{aligned}$ | $\begin{gathered} \pm 3 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ \pm 10 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \end{gathered}$ | $\begin{aligned} & -15 \mathrm{~V},+5 \text { to }+15 \mathrm{~V} \\ & +5 \mathrm{~V} \text { to }+15 \mathrm{~V}^{9} \end{aligned}$ | 24 pin hermetic DIP <br> 16 pin DIP $\}$ Ceramic | $\begin{aligned} & \$ 58 \\ & \$ 15.75 \end{aligned}$ | $\begin{aligned} & \$ 39^{10} \\ & \$ 12^{11} \end{aligned}$ |
|  | $\begin{aligned} & \text { AD7521 } \\ & \text { (CMOS) } \end{aligned}$ | 12 bits | $\pm 0.05 \%$ | BIN | NO |  | 500ns to 0.05\% | $\pm 10 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | +5 V to $+15 \mathrm{~V}^{9}$ | 18 pin DIP or Plastic | \$20.75 | \$15 ${ }^{11}$ |

## NOTES

1. DAC's whose model numbers begin with MDA have current outputs, allowing the user to select the op amp of his choice. Those beginning with DAC include an internal op amp.
2. Logic Codes: BIN, Binary; C-B, Comp. Binary; OBN, Offset Binary; COB, Comp. Offset Binary; BCD, Binary Coded Decimal; CBD, Comp. BCD; 2SC, Two'sComp.; C2C, Comp. Two's Comp.; SMB, SignMagnitude Binary; SMD, Sign-Magnitude BCD.
3. Reference range of DAC-8M and DAC-12M is $\pm 10 \mathrm{~V}$. Reference range of MDA-11MF is 0 to -10 V .
4. Standard temperature range on all converters is 0 to $+70^{\circ} \mathrm{C}$. Many models are available in an extended operating temperature version at extra cost. The extended operating temperature range is normally $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$. I. C. converters also available in military range: $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$.
5. Price is for stocked unit, which includes binary coding, input register, 0 to +10 V range, 184 L output amp, and deglitcher.
6. All inputs compatible with TTL/DTL/CMOS; can be used multiplying or fixed reference; reference supply not included.
7. All units have internal feedback resistors to provide accurate voltage output, when external op amp is used.
8. With compensation recommended.
9. CMOS construction. Total power only 20 mW .
10. KD version.
11.JN version.

# GENERAL PURPOSE D/A CONVERTERS MDA-IOZ, DAC-IOZ, DACIOO9, DAC-12QZ, DACIII8 

## GENERAL DESCRIPTION

These D/A converters are characterized primarily by low cost, but this economy has been attained by judicious use of materials, careful engineering, and by high volume manufacturing techniques. Consequently, there is no compromise with quality and reliability, and as a result, these products are excellent values.

## MDA-10Z

The MDA- 10 Z is a fast 10 -bit digital-to-current converter intended for use with external amplifiers. It is available with unipolar output or bipolar output, to suit the needs of a broad variety of applications. Fixed output range is provided.

## DAC-10Z

The DAC -10 Z is a fast 10 -bit D/A converter with a built-in I.C. output amplifier. Available in unipolar or bipolar form, the DAC- 10 Z is an optimum value for applications requiring above average performance at an economy price.

## DAC1009

The DAC1009 is a multipurpose 12 -bit D/A converter which can be readily adapted to a variety of applications. This versatile device can be programmed for fixed reference or multiplying operation and for current or voltage output. It interfaces with TTL/DTL as well as CMOS logic systems.


DAC-12QZ
The DAC-12QZ is a general purpose 12 -bit D/A converter in which an outstanding value is achieved. The Analog Devices' AD550 $\mu$ DAC current switches are used in conjunction with a matched close-tracking resistor network to provide fast 12 -bit performance at an economy price. The user chooses one of five available output ranges by jumpering at the module terminals.

DAC1118
The DAC1118 is a general purpose 12 -bit D/A converter which comes complete with an input storage register and a versatile output amplifier. The TTL compatible input register can accept Binary, Offset Binary, Two's Complement, or BCD coded inputs. As with the DAC-12QZ, five jumper programmable output ranges are available.

## ORDERING GUIDES



## BLOCK DIAGRAM DAC1118



SPECIFICATION SUMMARY (Typical @ $+25^{\circ} \mathrm{C}$ unless otherwise noted)

| Model | MDA-10Z | DAC-10Z | DAC1009 | DAC-12QZ | DAC1118 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Resolution (bits) | 10 | 10 | 12 | 12 | 12 |
| Digital Inputs |  |  |  |  |  |
| Levels (Positive True) | TTL | TTL | TTL/CMOS | TTL | TTL |
| Codes |  |  |  |  |  |
| Unipolar | BIN | BIN | BIN, BCD | C-B, CBD | BIN, BCD |
| Bipolar | OBN | OBN | OBN | COB | OBN, 2SC |
| Voltage Output Ranges |  |  |  |  |  |
| Unipolar | - | 0 to -10V | 0 to $-5 \mathrm{~V}, 0$ to -10 V | 0 to $+5 \mathrm{~V}, 0$ to +10 V | 0 to $+5 \mathrm{~V}, 0$ to +10 V |
| Bipolar | - | $\pm 10 \mathrm{~V}$ | $\pm 2.5 \mathrm{~V}, \pm 5 \mathrm{~V}, \pm 10 \mathrm{~V}\}^{1}$ | $\pm 2.5 \mathrm{~V}, \pm 5 \mathrm{~V}, \pm 10 \mathrm{~V}\} 1$ | $\pm 2.5 \mathrm{~V}, \pm 5 \mathrm{~V}, \pm 10 \mathrm{~V}\}^{1}$ |
| Current Output Ranges |  |  |  |  |  |
| Unipolar | 0 to +2 mA | - | 0 to +2 mA | - | - |
| Bipolar | $\pm 1 \mathrm{~mA}$ | - | $\pm 1 \mathrm{~mA}$ | - | - |
| Settling Time |  |  |  |  |  |
| (F.S. Step to $1 / 2$ LSB) |  |  |  |  |  |
| Current Output | 300ns | - | 700 ns |  |  |
| Voltage Output | - | $5 \mu \mathrm{~s}$ | $4 \mu \mathrm{~s}$ | $5 \mu \mathrm{~s}$ | $5 \mu \mathrm{~s}$ |
| Linearity Error | $\pm 1 / 2$ LSB | $\pm 1 / 2$ LSB | $\pm 1 / 2$ LSB | $\pm 1 / 2$ LSB | $\pm 1 / 2$ LSB |
| Stability vs. Temperature |  |  |  |  |  |
| Unipolar |  |  |  |  |  |
| Gain | $30 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $30 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $11 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $30 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $20 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |
| Zero | $10 \mathrm{nA} /{ }^{\circ} \mathrm{C}$ | $100 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $12 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $30 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ |
| Bipolar |  |  |  |  |  |
| Gain | $40 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $30 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $11 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $25 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $20 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |
| Offset | $30 \mathrm{nA} /{ }^{\circ} \mathrm{C}$ | $100 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $100 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $100 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ |
| Power Required | $\pm 15 \mathrm{~V}$ @ 15 mA | $\pm 15 \mathrm{~V}$ @ 15 mA | $\pm 15 \mathrm{~V}$ @ 18 mA | +15V @ 25 mA | +15V @ 20mA |
|  |  |  |  | $\begin{aligned} & -15 \mathrm{~V} @ 30 \mathrm{~mA} \\ & +5 \mathrm{~V} @ 35 \mathrm{~mA} \end{aligned}$ | -15V@30mA $+5 \mathrm{~V} @ 125 \mathrm{~mA}$ |
| Package Style | C-1 | C-1 | C-1 | C-1 | C-3 |
| Package Dimensions | $2^{\prime \prime} \times 2{ }^{\prime \prime} \times 0.4{ }^{\prime \prime}$ | $2^{\prime \prime} \times 2{ }^{\prime \prime} \times 0.4{ }^{\prime \prime}$ | $2^{\prime \prime} \times 2^{\prime \prime} \times 0.4$ " | $2^{\prime \prime} \times 2{ }^{\prime \prime} \times 0.4{ }^{\prime \prime}$ | $2^{\prime \prime} \times 4$ " $\times 0.4$ " |
| Price (100+) | \$27. | \$27. | \$54. | \$47. | \$80. |
| (1-9) | \$49. | \$49. | \$84. | \$79. | \$112. |
| ${ }^{1}$ Customer selects range by jumpers at the module's terminals. |  |  |  |  |  |

BLOCK DIAGRAM
DAC-12QZ


$$
\begin{aligned}
& \text { NOTE: PINS SHOWN AS HAVING NO CONNECTIONS (N.C.) } \\
& \text { ARE DELETED. }
\end{aligned}
$$

BLOCK DIAGRAM DAC1009


# HIGH PERFORMANCE D/A CONVERTERS DAC-QM, DAC-QS 

## GENERAL DESCRIPTION

The DAC-QM and DAC-QS digital-to-analog converters are characterized by high stability and high performance. They use Analog Devices $\mu \mathrm{DAC}{ }^{\circledR}$ monolithic quad current switches and $\mu \mathrm{DAC}{ }^{\circledR}$ monolithic thin-film resistor networks to provide high performance at moderate cost. Each type is available in 8, 10 , and 12 bit versions.

## DAC-QM

The DAC-QM contains within its $2^{\prime \prime} \times 4$ " x $0.4^{\prime \prime}$ module a complete DAC, including $\mu \mathrm{DAC}{ }^{\circledR}$ quad switches and thinfilm resistor network, precision internal reference, a versatile output amplifier, and an input register. The user can select any of five voltage output ranges with jumpers at the module terminals.


## DAC-QS

The DAC-QS is electrically identical to the DAC-QM, except that it does not contain an input register. As a result, the DAC-QS is packaged in the smaller $2^{\prime \prime} \times 2^{\prime \prime} \times 0.4^{\prime \prime}$ module, and its lower price reflects the change. As with the DAC-QM, its performance and stability are above average.


ORDERING GUIDE: DAC-QS

| MODEL DAC | XX <br> No. of <br> Bits | SX | SXXX |
| :--- | :---: | :---: | :---: |
| Converter | 8 | QS | Input Code |
| Type | 10 |  | CBD (comp. binary) |
|  | 12 |  |  |

NOTE: C-B version is stocked. CBD version is built to order.

SPECIFICATION SUMMARY (Typical @ $+25^{\circ} \mathrm{C}$ unless otherwise noted)

| Model | DAC-QM | DAC-QS |
| :---: | :---: | :---: |
| Resolution, Bits | 8, 10, 12 |  |
| Input Logic | TTL Positive True | * |
| Input Codes |  |  |
| Unipolar | BIN ${ }^{1} \mathrm{BCD}$ | C-B ${ }^{2}$ CBD |
| Bipolar | 2SC OBN | COB |
| Strobe Input Pulse Width | $50 \mathrm{~ns} \mathrm{~min}{ }^{3}$ | N/ ${ }^{4}$ |
| Output Ranges | 0 to $+5 \mathrm{~V}, 0$ to +10 V | * |
|  | $\pm 2.5 \mathrm{~V}, \pm 5 \mathrm{~V}, \pm 10 \mathrm{~V}$ | * |
| $\begin{aligned} & \text { F.S. Settling Time } \\ & \text { (to } 1 / 2 \text { LSB } \text { ) } \end{aligned}$ | $5 \mu \mathrm{~s}$ | * |
| Temperature Coefficients Gain (of reading) | $7 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ max | * |
| Offset |  |  |
| Unipolar | $15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max | * |
| Bipolar | $30 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max | * |
| Power Requirement | +15V @ 25 mA | * |
|  | -15V @ 30mA | * |
|  | +5V @ 150 mA | +5V@ 35 mA |
| Package Style | C-3 | C-1 |
| Package Dimensions | $2^{\prime \prime} \times 4^{\prime \prime} \times 0.4{ }^{\prime \prime}$ | $2^{\prime \prime} \times 2{ }^{\prime \prime} \times 0.4{ }^{\prime \prime}$ |
| Prices (1-9) | DAC-8QM \$179. | DAC-8QS \$147. |
|  | DAC-10QM \$221. | DAC-10QS \$179. |
|  | DAC-12QM \$242. | DAC-12QS \$200. |

${ }^{1}$ DAC-QM is stocked in the BIN version (which also gives OBN code in bipolar operation). The BCD and 2SC versions are built to order.
${ }^{2}$ DAC-QS is stocked in C-B version (which also gives COB code in bipolar operation). The CBD version is built to order.
${ }^{3}$ The Strobe Input must be driven from a source capable of supplying 24 standard TTL unit loads.
${ }^{4}$ The DAC-QS does not have a strobe input because it has no input register.
*Specifications same as those for the DAC-QM.


ORDERING GUIDE: DAC-QM

| MODEL DAC |  | $\mathbf{X X}$ <br> Series | XXX Input Code |
| :---: | :---: | :---: | :---: |
| Converter Type | 8 10 12 | QM | $\begin{aligned} & \text { BIN (binary) } \\ & \text { 2SC (2's comp.) } \\ & \text { BCD } \end{aligned}$ |

NOTE: BIN version is stocked. BCD and 2SC versions are built to order.

## HIGH SPEED D/A CONVERTERS DAC-IODF, MDA-IOF, DACIIO6

## GENERAL DESCRIPTION

These D/A converters are characterized primarily by very fast settling speeds. They are ideally suited for spot position control in CRT display systems, and for use in character generators, high speed test equipment, and very high speed A/D converters.

## DAC-10DF

The DAC-10DF is a very fast voltage output D/A converter subsystem, featuring practically glitchless operation and 50 ns settling to $0.05 \%$ for 1 LSB changes. Schottky TTL is used for the input register. The unit can be ordered with either of two amplifiers, the model 48 or the model 50 . With the model 50 amplifier, the DAC-10DF can drive a terminated $100 \Omega$ coaxial cable. Output connection is made through a $\mu \mathrm{DOT}$ RF connector mounted on the DAC-10DF's P.C. board.

## MDA-F

The MDA-10F is an ultra high speed digital-to-current converter offering 40ns full-scale settling time for 10 -bit binary resolution. This exceptional speed is offered without compromise of the fine linearity and stability that is found in all Analog Devices products. The converter is packaged in a low-profile $2^{\prime \prime} \times 44^{\prime \prime}$ module.


## DAC1106

The DAC1106 is a current output D/A converter which offers ultra high speed, adjustment-free operation. This device is available in both 8 and 10 bit versions which feature settling times to $1 / 2 \mathrm{LSB}$ of 25 ns and 50 ns respectively. The DAC1106 is packaged in a compact $2^{\prime \prime} \times 2^{\prime \prime} \times 0.4^{\prime \prime}$ module.

## BLOCK DIAGRAM DAC-10DF



PIN DESIGNATIONS: DAC-10DF

| PIN | FUNCTION | PIN | FUNCTION |
| :---: | :---: | :---: | :---: |
| A | BIT 1 (MSB) | N | INTERLOCK |
| B | BIT 2 | P | INTERLOCK |
| C | BIT 3 | R | +5VDC |
| D | BIT 4 | S |  |
| E | BIT 5 | T | DIGITAL GRD |
| F | BIT 6 | U |  |
| H | BIT 7 | V $\}$ | ANALOG GRD |
| J | BIT 8 | W | ANALOG GRD |
| K | BIT 9 | X | +15VDC |
| L | BIT 10 (LSB) | Y | -15VDC |
| M | STROBE | Z | ANALOG GRD |


| ORDERING GUIDE: DAC-10DF |  |  |
| :--- | :---: | :---: |
| MODEL DAC-10DF | XXX <br> Output Range | XX <br> $\pm 2.5 \mathrm{~V}$   <br> Converter Type $\pm 5 \mathrm{~V}$ 48 <br>  $\pm 10 \mathrm{~V}$ 50 |

SPECIFICATION SUMMARY (Typical @ $+25^{\circ} \mathrm{C}$ unless otherwise noted)

${ }^{1}$ The DAC-10DF can be ordered with either of two output amplifiers. The model 48 would generally be chosen where power consumption is of concern and a high output current is not required. When used with a model 50, the DAC-10DF is intended to drive a terminated coaxial cable.
${ }^{2}$ An 8-bit version of the MDA-10DF, called the MDA-8F, is available for $\$ 254$ (1-9).
${ }^{3}$ When used with the model 50, the DAC-10DF is intended to drive a coaxial cable that is terminated in a resistance equal to the characteristic impedance of the cable.
${ }^{4}$ The settling times shown for the DAC-10DF are valid for the $\pm 2.5 \mathrm{~V}$ output range. Settling times for the $\pm 5 \mathrm{~V}$ and $\pm 10 \mathrm{~V}$ ranges are somewhat greater.
*Specifications same as those for the DAC-10DF with a model 48 output amplifier.

## BLOCK DIAGRAM

MDA-10F


# HIGH RESOLUTION D/A CONVERTERS DAC-QM, DAC-QG 

## GENERAL DESCRIPTION

These D/A converters offer the limit of today's state-of-theart in resolution, linearity, and stability. Analog Devices' $\mu \mathrm{DAC}$ monolithic quad switches and super precision thin film resistor networks provide the stability needed for 16-bit performance. These products are supplied with an error plot made during final testing, and with certification of the performance of the reference zener.

## DAC-16QM

The DAC-16QM is a complete self-contained 16 -bit D/A converter with both current and voltage outputs, offered in 16 or 14-bit linearity versions. This converter has an aged compensated reference that provides stability appropriate for high resolution converters. Settling time of the current output is about $1 \mu \mathrm{~s}$ to $0.1 \%$ for full scale changes. As can be expected, however, settling time to full accuracy ( $0.0015 \%$ ) for voltage output with the built-in IC output amplifier, is much greater. When faster settling is required, a fast external amplifier should be used. (See DAC- QM settling chart on next page.)


## DAC-QG

The DAC- QG is a manifold board for the DAC-16QM, making provisions for the most-frequently required accessories. The standard (stocked) version of the DAC-16QG has an input register wired for binary code, and has a deglitcher mounted. It is wired for +10 V output range, using the model 184 L output amplifier (the optimum amplifier choice for both stability and speed, in this application).

PIN DESIGNATIONS: DAC-QG


ORDERING GUIDE: DAC- QM

| MODEL DAC | XX | XX | XXX |
| :--- | :---: | :---: | :---: | :---: |
|  | Linearity | Series | Input Code |
| Converter Type | 14 Bits | QM | C-B (comp. binary) |
|  | 16 Bits |  | CBD (comp. BCD) |

NOTE: Stock version is complementary binary.
ORDERING GUIDE: DAC-QG


[^9]NOTES:

SPECIFICATION SUMMARY (Typical @ $+25^{\circ} \mathrm{C}$ unless otherwise noted)

| Model | DAC-QM | DAC-QG |
| :---: | :---: | :---: |
| Resolution, Bits | 14, 16 | 8-16 Bits ${ }^{1}$ |
| Input Logic | TTL Positive True | * ${ }^{*}$ |
| Input Codes | Complementary Binary Complementary BCD ${ }^{3}$ | $\begin{gathered} \operatorname{BIN}^{2}, \mathrm{BCD}, 2 \mathrm{SC} \\ \text { Sign \& Mag BIN \& BCD } \end{gathered}$ |
| Linearity Error (straight line through zero and full scale) |  |  |
| DAC-14XX | $\pm<0.003 \%$ | * |
| DAC-16XX | $\pm<0.0015 \%$ | , |
| Reference, Internal | $+6.00 \mathrm{~V} \pm 0.01 \% \pm 6 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \pm 8 \mathrm{ppm} / \mathrm{mo}$. |  |
| Temperature Coefficient- |  |  |
| Voltage Mode (in ppm of $\mathrm{FS} /{ }^{\circ} \mathrm{C}$ ) | with int. amp. | with 184L amp. |
| Gain | $\pm 15 \mathrm{ppm}$ | $\pm 7 \mathrm{ppm}$ |
| Unipolar Offset | $\pm 9 \mathrm{ppm}$ | $\pm 0.5 \mathrm{ppm}$ |
| Bipolar Offset | $\pm 15 \mathrm{ppm}$ | $\pm 7 \mathrm{ppm}$ |
| Settling Speed | See figures | See figures |
| Power Requirement | +15V @ 20 mA | +15V @ 35 mA |
|  | -15V @ 30mA | -15 V @ 50 mA |
|  | +5 V @ 40 mA | +5 V @ 220 mA |
| Package Style | $\mathrm{C}^{-3}$ | C-8 |
| Package Dimensions | $2^{\prime \prime} \times 4^{\prime \prime} \times 0.4{ }^{\prime \prime}$ | $41 / 2^{\prime \prime} \times 43 / 4^{\prime \prime} \times 0.4{ }^{\prime \prime}$ |
| Price (1-9) | DAC-14QM \$415. | DAC-16QG |
|  | DAC-16QM \$782. | (complete) ${ }^{2}$ \$1207. |
|  |  | $\begin{gathered} \text { DAC-14QG } \\ \text { (complete) }^{2} \$ 840 . \end{gathered}$ |
| ${ }^{1}$ DAC-QG can be built to order with any DAC-QM from 8 to 16 bits. |  |  |
| ${ }^{2}$ DAC-QG is stocked in a version containing the most popular options. All other versions are built to order. The stock version, available either with 14 or 16 -bit resolution, contains: Binary input code with register, 0 to +10 V range, 184L output amplifier, deglitcher to limit output switching transients to 5 mV max. |  |  |
| ${ }^{3}$ DAC-14/16QM is stocked in Complementary Binary code. Complementary BCD is built to order. <br> *Specifications same as for Model DAC-16QM. |  |  |

SETTLING CURVES


## MULTIPLYING D/A CONVERTERS DAC-M, MDA-IIMF

## GENERAL DESCRIPTION

Multiplying D/A converters are specifically designed for use with external reference signals, which may be of varying amplitude DC or AC. They act essentially as accurate digitally-controlled attenuators, and find broad application in synchro conversion, character generation for CRT displays, and hybrid computation.

## DAC-M

The DAC-M is a complete self-contained four-quadrant multiplying D/A converter optimized for applications at the lower frequency end of the spectrum. It has both an input buffer and inverter, providing for four-quadrant operation from a single polarity (or phase) of reference input, if desired. With binary logic input code, it can be operated in bipolar fashion by use of the offset coding.


## MDA-11MF

The MDA-11MF is a very high speed one or two quadrant multiplying digital-to-current converter designed particularly for the needs of the graphic display field. Operating as a single quadrant device, it can control a $10 \mathrm{~V} / \mu$ s reference ramp with 11 -bit resolution and feedthrough. An internal network provides for two quadrant operation.


## LOW FEEDTHROUGH

The very low feedthrough of the MDA-11MF when operated in the single-quadrant mode is shown below. In both photographs the lower trace is a $500 \mathrm{kHz}, 10 \mathrm{~V} / \mu \mathrm{s}$ triangle wave driving the analog input (shown with a vertical scale of $5 \mathrm{~V} / \mathrm{div}$.). The upper trace in both pictures is the amplified output of the DAC connected to an op amp such as an ADI model 48. The vertical scale is $5 \mathrm{mV} /$ div., which is approximately equal to $1 \mathrm{LSB} / \mathrm{div}$. The trace on the left shows the output with the LSB input on and all other inputs off. The right-hand trace shows the output with all digital inputs off, and clearly demonstrates that the feedthrough under these conditions is less than $1 / 2$ LSB.


Feedthrough with a 500 kHz Triangle Wave

| Model | DAC-8M | DAC-12M | MDA-11MF |
| :---: | :---: | :---: | :---: |
| Resolution, Bits | 8 | 12 | 11 |
| Relative Accuracy (Error in \% of FS) | 0.2\% | 0.02\% | 0.03\% |
| Slewing Rate | $10 \mathrm{~V} / \mu \mathrm{s}$ | * | N/ ${ }^{1}$ |
| Settling Time | $10 \mu \mathrm{~s}$ to $0.2 \%$ | $15 \mu$ s to $0.01 \%$ | $<1 \mu$ s to 0.01\% |
| Full Output Freq. ( $\pm 10 \mathrm{~V}$ ) | 200 kHz | * | N/A |
| Reference Input Voltage Impedance | $\begin{gathered} \pm 10 \mathrm{~V} \text { p-p } \\ 10 \mathrm{k} \Omega \end{gathered}$ | * | $\begin{gathered} 0 \text { to }-10 \mathrm{~V} \\ 4 \mathrm{k} \Omega \end{gathered}$ |
| Logic Input | TTL Positive True | * | * |
| Logic Code | Binary | * | Binary or Offset Binary |
| Output |  |  |  |
| Voltage | $\pm 10 \mathrm{~V}$ | * | $\pm 1 \mathrm{~V} \mathrm{max}^{1}$ |
| Current | 5 mA | * | +4 mA or $\pm 2 \mathrm{~mA}$ |
| Impedance | <1 ohm | * | 600 ohms |
| Temperature Coefficient Gain <br> Zero | $\begin{aligned} & <25 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ & <50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \end{aligned}$ | $<5 \mathrm{ppm} /_{*}^{\circ} \mathrm{C}$ | $\begin{gathered} \pm 30 \mathrm{ppm} /{ }^{\circ}{ }^{\circ} \mathrm{C} \\ \pm 75 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}^{2} \end{gathered}$ |
| Feedthrough | 2.5 mV @ 400 Hz FS | * | Unipolar Mode $<1 / 2$ LSB with $10 \mathrm{~V} / \mu$ s triangle wave |
| Power Required | $\begin{aligned} & +15 \mathrm{~V} @ 17 \mathrm{~mA} \\ & -15 \mathrm{~V} @ 20 \mathrm{~mA} \end{aligned}$ | * | $\begin{aligned} & +15 \mathrm{~V} @ 30 \mathrm{~mA} \\ & -15 \mathrm{~V} @ 10 \mathrm{~mA} \end{aligned}$ |
| Package Style | C-1 | * | C-3 |
| Package Dimensions | $2^{\prime \prime} \times 2^{\prime \prime} \times 0.4{ }^{\prime \prime}$ | * | $2^{\prime \prime} \times 4$ " $\times 0.4{ }^{\prime \prime}$ |
| Price (1-9) | \$205. | \$310. | \$158. |

${ }^{1}$ Since there is no output amplifier, the MDA- 11 MF is not slewing rate limited in the usual sense. BW and slewing rate are more than adequate for accurate transconduction of a $10 \mathrm{~V} / \mu \mathrm{s}$ reference ramp.
${ }^{2}$ Measured using an ADI Model 48 as an output amplifier.
*Specifications same as for Model DAC-8M.

BLOCK DIAGRAM
DAC-12M


# INTEGRATED CIRCUIT D/A CONVERTERS AD562, AD7520, AD752। 

## GENERAL DESCRIPTION

Analog Devices has extended its expertise in the development of D/A and A/D converters into integrated circuit technology. The converters described on this page, and more fully in the IC section of the PRODUCT GUIDE, are indicative of the commitment we are making to extend the state-of-the-art for converters to bring to the designer the latest advantages of IC technology. These products and other IC converters to come are designed by our staff and manufactured to the quality standards applied to all of our products.

## AD562 12-BIT IC DAC

The AD562, our newest IC DAC, is the industry's most accurate 12-bit D/A converter. This accuracy includes guaranteed monotonicity over the entire operating temperature range, $\pm 1 / 4 \mathrm{LSB}$ maximum total error referred to full scale, 1 ppm of Full Scale Range (FSR) $/{ }^{\circ} \mathrm{C}$ differential nonlinearity temperature coefficient, and 3 ppm of $\mathrm{FSR} /{ }^{\circ} \mathrm{C}$ maximum gain temperature coefficient. The AD562 is provided in a hermetically-sealed,

24-pin DIL package. Its TTL, DTL, and high low level CMOS compatibility and low cost make it ideal for high accuracy applications in aerospace signal conditioning, process control data acquisition, and medical instrumentation. See page 217 for further details.

## AD7520/AD7521 MONOLITHIC CMOS DAC

Our monolithic CMOS D/A converter-the industry's firstfeatures 10 -bit or 12 -bit resolution (AD7521), 8, 9, or 10-bit linearity, 20 mW power dissipation, 2 ppm of $\mathrm{FSR} /{ }^{\circ} \mathrm{C}$ maximum nonlinearity tempco, and low price. The AD7520 with its TTL, DTL, and CMOS compatibility allows digital control over a wide 5 V to 15 V operating voltage supply range. The AD7520 multiplies in four quadrants with an accuracy of $0.05 \%$ of FSR. The AD7521 offers all the features of the AD7520, but provides 10-bit linearity for specific applications, such as digitallycontrolled filters, that may require 12 -bit resolution. See page 228 for further details.

SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ unless otherwise noted)

| MODEL | AD562 | AD7520 <br> (CMOS) | AD7521 <br> (CMOS) |
| :---: | :---: | :---: | :---: |
| Resolution | 12 bits | 10 bits | 12 bits |
| Linearity Error | $\pm 0.006 \%$ | $\pm 0.05 \%$ | $\pm 0.05 \%$ |
| Input Code Options ${ }^{1}$ (TTL/DTL/CMOS Compatible) | BIN, BCD | BIN | BIN |
| Input Register | No | No | No |
| Output Options | 2 mA or $\pm 1 \mathrm{~mA}^{2}$ | $1 \mathrm{~mA}^{2}$ | $1 \mathrm{~mA}^{2}$ |
| Settling Time to \% of Full Scale | $1.5 \mu$ s to $0.01 \%^{3}$ | 500ns to 0.05\% | 500ns to 0.05\% |
| Gain TC ${ }^{4}$ | $\pm 3 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 10 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 10 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |
| Power Requirements | $-15 \mathrm{~V},+5$ to +15 V | +5 V to $+15 \mathrm{~V}^{5}$ | +5 V to $+15 \mathrm{~V}^{5}$ |
| Package Size \& Style | 24 pin hermetic DIP | 16 pin DIP Ceramic or Plastic | 18 pin DIP Ceramic or Plastic |
| $\begin{aligned} & \hline \text { Prices } \\ & (1-9) \\ & (100+) \end{aligned}$ | $\begin{aligned} & \$ 58.00^{6} \\ & \$ 39.00^{6} \end{aligned}$ | $\begin{aligned} & \$ 15.75^{7} \\ & \$ 12.00^{7} \end{aligned}$ | $\begin{aligned} & \$ 20.75^{7} \\ & \$ 15.00^{7} \end{aligned}$ |

[^10]
## CAPSULE SELECTION TABLE

ANALOG-TO-DIGITAL CONVERTERS

SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ unless otherwise noted)

| Product Classification | Model | Resolution | Error <br> (Relative to F.S.) | Conversion Time | Output Code Options ${ }^{1}$ <br> (TTL/DTL Compatible) | Analog Input Options | Input <br> Buffer | $\begin{aligned} & \text { Gain } \\ & \text { TC }^{2} \end{aligned}$ | Power Requirements | Package Size \& Style | $\begin{aligned} & \text { Price } \\ & (1-9) \end{aligned}$ | $\begin{aligned} & \text { Price } \\ & (100+) \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| General Purpose | $\begin{gathered} \text { ADC-8S } \\ \text { ADC-10Z } \\ \text { ADC-12QZ } \\ \text { ADC1100 } \end{gathered}$ | 8 bits 10 bits 12 bits $31 / 2$ digits | $\pm 0.2 \%$ $\pm 0.05 \%$ $\pm 0.0125 \%$ $\pm 0.05 \% \pm 1$ bit | 1 ms $20 \mu \mathrm{~s}$ $40 \mu \mathrm{~s}$ 42 ms | ```BIN, OBN, 2SC, BCD BIN, OBN, 2SC BIN, OBN, 2SC SMD``` | $\begin{gathered} \pm 5 \mathrm{~V}, \pm 10 \mathrm{~V},+5 \mathrm{~V},+10 \mathrm{~V} \\ \pm 199.9 \mathrm{mV} \end{gathered}$ | YES OPTIONAL OPTIONAL YES | $\begin{aligned} & \pm 60 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ & \pm 40 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ & \pm 30 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ & \pm 50 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \end{aligned}$ | $\begin{gathered} \pm 15 \mathrm{~V},+5 \mathrm{~V} \\ +5 \mathrm{~V} \end{gathered}$ | $\begin{aligned} & 2^{\prime \prime} \times 3^{\prime \prime} \times 0.4^{\prime \prime}, \mathrm{C}-2 \\ & 2^{\prime \prime} \times 4^{\prime \prime} \times 0.4^{\prime \prime}, \mathrm{C}-3 \\ & 2^{\prime \prime \prime} \times 4^{\prime \prime} \times 0.4^{\prime \prime}, \mathrm{C}-3 \\ & 2^{\prime \prime \prime} \times 4^{\prime \prime} \times 0.4^{\prime \prime}, \mathrm{C}-3 \end{aligned}$ | $\begin{array}{lr} \$ & 87 \\ \$ & 99 \\ \$ & 129 \\ \$ & 104 \end{array}$ | $\begin{aligned} & \$ 52 \\ & \$ 67 \\ & \$ 92 \\ & \$ 70 \end{aligned}$ |
| High <br> Performance | ADC-8QM ADC-10QM ADC-12QM | 8 bits 10 bits 12 bits | $\begin{gathered} \pm 0.2 \% \\ \pm 0.05 \% \\ \pm 0.0125 \% \\ \hline \end{gathered}$ | $\begin{array}{r} 18 \mu \mathrm{~s} \\ 22 \mu \mathrm{~s} \\ 25 \mu \mathrm{~s} \\ \hline \end{array}$ | BIN, OBN, 2SC, BCD | $\pm 5 \mathrm{~V}, \pm 10 \mathrm{~V},+10 \mathrm{~V}$ | YES | $\pm 5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 15 \mathrm{~V},+5 \mathrm{~V}$ | 2' $\times 4$ " $\times 0.4$ ", C-3 | $\begin{aligned} & \$ 263 \\ & \$ 294 \\ & \$ 320 \\ & \hline \end{aligned}$ |  |
|  | ADC-8QU <br> ADC-10QU <br> ADC-12QU | 8 bits 10 bits 12 bits | $\begin{gathered} \pm 0.2 \% \\ \pm 0.05 \% \\ \pm 0.025 \% \end{gathered}$ | $\begin{gathered} 6.4 \mu \mathrm{~s} \\ 8 \mu \mathrm{~s} \\ 15 \mu \mathrm{~s} \end{gathered}$ | BIN, OBN, 2SC, BCD | $\pm 5 \mathrm{~V}, \pm 10 \mathrm{~V},+5 \mathrm{~V},+10 \mathrm{~V}$ | YES | $\pm 5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 15 \mathrm{~V},+5 \mathrm{~V}$ | $2^{\prime \prime} \times 4$ " $\times 0.4$ ", C-3 | $\begin{aligned} & \$ 273 \\ & \$ 305 \\ & \$ 331 \\ & \hline \end{aligned}$ |  |
|  | $\begin{aligned} & \hline \text { ADC-14I } \\ & \text { ADC-17I } \\ & \hline \end{aligned}$ | $\begin{aligned} & 14 \text { bits } \\ & 17 \text { bits } \end{aligned}$ | $\begin{aligned} & \pm 0.01 \% \pm 1 \mathrm{bit} \\ & \pm 0.01 \% \pm 1 \mathrm{bit} \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline 40 \mathrm{~ms} \\ & 40 \mathrm{~ms} \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline \text { SMB } \\ & \text { SMD } \end{aligned}$ | $\begin{aligned} & \pm 10 \mathrm{~V} \\ & \pm 12 \mathrm{~V} \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline \text { NO } \\ & \text { NO } \\ & \hline \end{aligned}$ | $\begin{aligned} & \pm 5 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ & \pm 5 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ & \hline \end{aligned}$ | $\begin{aligned} & \pm 15 \mathrm{~V},+5 \mathrm{~V} \\ & \pm 15 \mathrm{~V},+5 \mathrm{~V} \\ & \hline \end{aligned}$ | $\begin{array}{r} 3^{\prime \prime} \times 4 \times 0.4, C-5 \\ 3^{\prime \prime} \times 4^{\prime \prime} \times 0.4^{\prime \prime}, C-5 \\ \hline \end{array}$ | $\begin{aligned} & \$ 272 \\ & \$ 272 \\ & \hline \end{aligned}$ | , |
|  | ADC1105 J <br> ADC1105K | $\begin{gathered} 1: 2000 \\ 1: 20,000 \\ \hline \end{gathered}$ | $\begin{gathered} \pm 0.1 \% \pm 1 \text { bit } \\ \pm 0.01 \% \pm 1 \text { bit } \\ \hline \end{gathered}$ | (depends on resolution) | $\begin{gathered} \text { (any sign- } \\ \text { magnitude code) } \\ \hline \end{gathered}$ | $\} \pm 10 \mathrm{~V}, \pm 1 \mathrm{~V}$ | $\begin{aligned} & \text { NO } \\ & \text { NO } \end{aligned}$ | $\begin{aligned} & \pm 10 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ & \pm 5 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ & \hline \end{aligned}$ | $\begin{aligned} & \pm 15 \mathrm{~V},+5 \mathrm{~V} \\ & \pm 15 \mathrm{~V},+5 \mathrm{~V} \\ & \hline \end{aligned}$ | $\begin{aligned} & 2^{\prime \prime} \times 4^{\prime \prime} \times 0.6^{\prime \prime}, \text { CB- } 3 \\ & 2^{\prime \prime} \times 4^{\prime \prime} \times 0.6^{\prime \prime}, \text { CB-3 } \end{aligned}$ | $\begin{aligned} & \$ 159 \\ & \$ 209 \\ & \hline \end{aligned}$ | $\begin{aligned} & \$ 115 \\ & \$ 150 \\ & \hline \end{aligned}$ |
| Fast | ADC1103-001 ADC1103-002 ADC1 103-003 | 8 bits <br> 10 bits <br> 12 bits | $\begin{gathered} \pm 0.2 \% \\ \pm 0.05 \% \\ \pm 0.025 \% \end{gathered}$ | $\begin{aligned} & 1.0 \mu \mathrm{~s} \\ & 1.5 \mu \mathrm{~s} \\ & 3.5 \mu \mathrm{~s} \end{aligned}$ | BIN, OBN, 2SC | $\pm 5 \mathrm{~V}, \pm 10 \mathrm{~V},+10 \mathrm{~V}$ | NO | $\pm 10 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 15 \mathrm{~V},+5 \mathrm{~V}$ | $2^{\prime \prime} \times 4^{\prime \prime} \times 0.75^{\prime \prime}, \mathrm{CA}-3$ | $\begin{aligned} & \$ 473 \\ & \$ 484 \\ & \$ 495 \\ & \hline \end{aligned}$ |  |
|  | ADC1109 | 10 bits | $\pm 0.05 \%$ | $4 \mu \mathrm{~s}$ | BIN, OBN | $\pm 5 \mathrm{~V},+10 \mathrm{~V}$ | NO | $\pm 30 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 15 \mathrm{~V},+5 \mathrm{~V}$ | $2^{\prime \prime} \times 3^{\prime \prime} \times 0.4{ }^{\prime \prime}, \mathrm{CA}-2$ | \$ 159 |  |
| High Resolution | ADC-16Q | 16 bits | $\pm 0.0015 \%$ | $400 \mu \mathrm{~s}$ | BIN, OBN, 2SC | $\pm 5 \mathrm{~V}, \pm 10 \mathrm{~V},+10 \mathrm{~V}$ | YES | $\pm 8 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 15 \mathrm{~V},+5 \mathrm{~V}$ | $4.5^{\prime \prime} \times 6.0^{\prime \prime}, \mathrm{C}-8$ | \$1418 |  |
| Low Power CMOS | $\begin{gathered} \mathrm{ADC}-12 \mathrm{QL} / \mathrm{J} \\ \mathrm{ADC}-12 \mathrm{QL} / \mathrm{K} \\ \mathrm{ADC} 1123 \end{gathered}$ | $\begin{aligned} & 12 \text { bits } \\ & 10 \text { bits } \end{aligned}$ | $\begin{aligned} & \pm 0.01 \% \\ & \pm 0.05 \% \end{aligned}$ | 85 to $130 \mu \mathrm{~s}$ <br> 65 to $90 \mu \mathrm{~s}$ | BIN, OBN | $\pm 5 \mathrm{~V}, \pm 10 \mathrm{~V},+5 \mathrm{~V},+10 \mathrm{~V}$ | NO | $\begin{aligned} & \pm 50 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ & \pm 20 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ & \pm 50 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \end{aligned}$ | $\pm 15 \mathrm{~V},+5 \mathrm{~V}$ | $3.6^{\prime \prime} \times 4.1^{\prime \prime}, \mathrm{C}-8$ | $\begin{aligned} & \$ 709^{4} \\ & \$ 998^{4} \\ & \$ 299 \end{aligned}$ |  |

## NOTES

1. Logic Codes: BIN, Binary; C-B, Comp. Binary; OBN, Offset Binary: COB, Comp. Offset Binary; BCD, Binary Coded Decimal; CBD, Comp. BCD; 2SC, Two's Complement; C2C, Comp. Two's Comp.; SMB, Sign-Magnitude Binary; SMD, Sign-Magnitude BCD.
2. Standard temperature range on all converters is 0 to $+70^{\circ} \mathrm{C}$. Many models are available in an extended operating temperature version at extra cost. The extended operating temperature range is normally $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$.
3. Prices are for units without input buffer. In small quantities, add $\$ 20$ to unit price for buffer.
4. Price for 1-4 pieces.

# GENERAL PURPOSE A/D CONVERTERS ADC-8S, ADC-10Z, ADC-12QZ, ADCII00 

## GENERAL DESCRIPTION

These analog-to-digital converters are characterized by low cost, achieved through skilled engineering and high volume, efficient manufacturing. They offer an extremely high performance/cost ratio.

## ADC-8S

The ADC-8S is an 8-bit A/D converter of moderate speed that even includes an input buffer. A counter generates a staircase at the output of an internal DAC, the output of which is compared against the signal input. This design requires only simple logic circuitry, helping to hold down cost. Conversion time is proportional to the magnitude of the input signal.

## ADC-10Z

The ADC-10Z is a small modular A/D converter that performs a 10 -bit conversion in $20 \mu \mathrm{~s}$ or less. It offers performance and features previously found only in much more expensive converters. It uses the successive approximations conversion technique, and contains an easy-to-use serial output.

## ADC-12QZ

The ADC-12QZ is a 12 -bit successive approximation type converter that offers reasonable speed and good performance at very low cost. Analog Devices' $\mu \mathrm{DAC}{ }^{\circledR}$ quad current switches and a unique combination of thick-film and hybrid technology has given the ADC-12QZ the basic performance of a much higher priced unit. Like the ADC-10Z, it features an easy-touse serial output.


## ADC1100

The ADC1 100 is a dual slope A/D converter in a compact $2^{\prime \prime} \times 4^{\prime \prime} \times 0.4^{\prime \prime}$ module. It can be triggered externally, or internally at a rate of about 4 conversions $/ \mathrm{sec}$, or it can be wired to start a new conversion when the conversion in progress is completed. It is ideal for driving a display, or feeding data to a computer, or for doing both jobs simultaneously. Since it requires only +5 V power, and has a normal mode noise rejection of 40 dB minimum, it is a natural choice for installation at transducer locations.

BLOCK DIAGRAM
ADC-10Z


BLOCK DIAGRAM ADC-12QZ


BLOCK DIAGRAM ADC1100


SPECIFICATION SUMMARY (Typical @ $+25^{\circ} \mathrm{C}$ unless otherwise noted)

| Model | ADC-8S | ADC-10Z | ADC-12QZ | ADC1100 ${ }^{6}$ |
| :---: | :---: | :---: | :---: | :---: |
| Resolution, Bits | 8 | 10 | 12 | 3112 BCD Digits ${ }^{7}$ |
| Linearity Error | $\pm 1 / 2$ LSB | * | * | $\pm 0.05 \%$ |
| Analog Input Ranges ${ }^{1}$ (Volts) | $\pm 5, \pm 10,+5,+10$ | * | * | $\pm 199.9 \mathrm{mV}$ |
| Impedance W/o Buffer ${ }^{2}$ W/ Buffer ${ }^{3}$ | $2.5 \mathrm{k}-10 \mathrm{k} \Omega$ $10^{8}$ ohms | $6 \mathrm{k}-12 \mathrm{k} \Omega$ $10^{9}$ ohms | $2.5 \mathrm{k}-10 \mathrm{k} \Omega$ $10^{9}$ ohms | $\overline{10^{8}} \Omega$ |
| Conversion Time | $1 \mathrm{~ms}^{4}$ | $20 \mu \mathrm{~s}$ | $40 \mu \mathrm{~s}$ | $42 \mathrm{~ms} \mathrm{max}{ }^{8}$ |
| Digital Control |  |  |  |  |
| Data Outputs Output Codes | TTL Positive True | * | * | * |
| Standard ${ }^{5}$ Optional | BIN, OBN, 2SC BCD | BIN, OBN, 2SC | BIN, OBN, 2SC | SMD |
| Status Output | " 1 " During Conversion | * | * | " 0 " During Conversión |
| Serial Data Output | No | Yes | Yes | No |
| Temperature Coefficient |  |  |  |  |
| Gain (of Reading) | $\pm 60 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 40 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 30 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 50 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ max |
| Zero (Unipolar) | $\pm 20 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 25 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | P1 |
| Offset (Bipolar) | $\pm 60 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 30 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 10 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 2 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ max |
| Power Required | +15V @ 28 mA | +15V @ 18mA | +15 V @ 20 mA | - |
|  | -15V @ 28 mA | -15 V @ 25 mA | -15V @ 30mA | - |
|  | +5 V @ 120 mA | +5 V @ 170 mA | +5 V @ 210 mA | +5 V @ 200 mA |
| Package Style | C-2 | C-3 | C-3 | C-3 |
| Package Dimensions | $2^{\prime \prime} \times 3^{\prime \prime} \times 0.4^{\prime \prime}$ | $2^{\prime \prime} \times 4^{\prime \prime} \times 0.4^{\prime \prime}$ | $2^{\prime \prime} \times 4^{\prime \prime} \times 0.4{ }^{\prime \prime}$ | $2^{\prime \prime} \times 4^{\prime \prime} \times 0.4^{\prime \prime}$ |
| Price (100+) | \$52. | \$67. | \$92. | \$70. |
| (1-9) | \$87. | \$99. ${ }^{3}$ | \$129. ${ }^{3}$ | \$104. |

${ }^{1}$ Desired input range is selected with jumpers and connections at the module's terminals.
${ }^{2}$ Input impedance without buffer depends on input range selected, but will be within the indicated limits.
${ }^{3}$ Input buffer is standard on ADC-8S, but the unit may be wired for a direct input, if desired. On $\mathrm{ADC}-10 \mathrm{Z}$ and $\mathrm{ADC}-12 \mathrm{QZ}$, input buffer is optional. In small quantities, add $\$ 20$ to price for input buffer. Units with a buffer may be wired for direct input, if desired.
${ }^{4}$ Conversion time for a full-scale input signal is approximately 1 ms . For input signals with a magnitude of less than full-scale, the conversion time is proportionately less.
${ }^{5}$ Output code is natural binary for unipolar input, but it can be either offset binary or two's complement at the user's option with a bipolar input.
${ }^{6}$ The ADC1100 has a minimum Normal Mode Rejection of 40 dB at 60 Hz ; it can also be adjusted to optimize the NMR of 50 Hz noise. An external phase locked loop can be added to increase the NMR to over 100 dB .
${ }^{7}$ Plus Sign.
${ }^{8}$ In the event of an overload, it can take as long as 70 ms to complete a conversion.
*Specifications same as for ADC-8S.

## BLOCK DIAGRAM

ADC-8S


ORDERING GUIDE

| ADC-8S |  |
| :---: | :---: |
| ADC-8S/BIN | BIN |
| ADC-8S/BCD | BCD |


| ADC-10Z |  |
| :---: | :---: |
| ADC-10Z-002 | NO BUFFER |
| ADC-10Z-022 | BUFFER |


| ADC-12QZ |  |
| :---: | :---: |
| ADC-12QZ-003 | NO BUFFER |
| ADC-12QZ-023 | BUFFER |

# HIGH PERFORMANCE A/D CONVERTERS ADC-QM, ADC-QU, ADC-14 I, ADC-17I, ADCII05 

## GENERAL DESCRIPTION

Included in this group of high performance A/D converters are two successive approximation and two dual slope devices. The successive approximation converters utilize monolithic quad current switches and thin film resistor networks to achieve the best stability and linearity generally available. The dual slope integrating converters perform conversions by integrating the input signal for a fixed period of time, and then measuring the time required to return the integrator to zero when a fixed reference signal of opposite polarity is applied. This technique provides high resolution, good differential linearity, and excellent normal mode rejection when the input integration time is set equal to an integral multiple of the power line period.

## ADC-QM

The ADC-QM is a high performance, successive approximation A/D converter packaged in a low profile $2^{\prime \prime} \times 4^{\prime \prime}(51 \times 102 \mathrm{~mm})$ module. It offers excellent stability over both time and temperature at a moderate cost. It is complete with an input buffer, and the desired input range is selected by the user with jumpers and connections at the module terminals. The ADCQM is available in 8,10 , and 12 bit versions.

## ADC-QU

The ADC-QU is a modular A/D converter that is very similar to the ADC-QM except that it offers an appreciably shorter conversion time. Conversion times for the 8,10, and 12 bit units are $6.4 \mu \mathrm{~s}, 8 \mu \mathrm{~s}$, and $15 \mu \mathrm{~s}$ respectively. The ADC-QU is pin compatible with the ADC-QM and in most applications can serve as a direct replacement for it. When mounted on an AC4451 mounting card, the ADC-QU becomes a pin compatible substitute for the older model ADC-U.


## ADC1105

The ADC1105 is a dual slope A/D converter which, when used with external counters and registers, can be configured to provide outputs of any desired resolution (to $1: 20,000$ ), coding, or counting scheme. It is available with either of two degrees of accuracy; the ADC1105J has $0.1 \%$ and the ADC1105K has $0.01 \%$ relative accuracy. Both units feature excellent zero stability, choice of input ranges, and ratiometric capability. An optional $4.5^{\prime \prime} \times 2.8^{\prime \prime}(114 \times 71 \mathrm{~mm})$ card mounted version of the ADC1105 can be ordered.

## ADC-14I AND ADC-17I

The ADC-14I and ADC-17I are complete high resolution dual slope A/D converters which are identical except for their output coding. The ADC-14I has a 14-bit binary plus sign coding, while the ADC-17I has $41 / 2 B C D$ digit plus sign output coding. Both feature a normal mode rejection ratio of 70 dB , an automatic zero correct cycle, and a gain T.C. of only $\pm 10 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$.


ORDERING GUIDE: ADC-QM and ADC-QU

| ADC-XX | XX | /XXX |
| :---: | :--- | :---: |
| No. of Bits | Series | Output Code |
| 8 | QM | BIN (binary, offset binary, |
| 10 | QU | two's complement) |
| 12 |  | BCD (binary-coded decimal) |

## ORDERING GUIDE: ADC1105

ADC1105J
ADC1105K
ADC1105J/AC1547J
ADC1105K/AC1547K
(Module Only) (Module Only)
(Module Mounted on Card)
(Module Mounted on Card)

Note: In the ADC-8QM and ADC-8QU, bit 8 is the LSB, and pins $48,50,52$ and 54 are deleted. In the ADC-10QM and ADC-10QU, bit 10 is the LSB, and pins 48 and 50 are deleted.

SPECIFICATION SUMMARY (Typical @ $+25^{\circ} \mathrm{C}$ unless otherwise noted)

${ }^{1}$ The desired input range is selected by the user with jumpers connected to the module terminals.
${ }^{2}$ The input impedance without buffer is proportional to the input voltage range.
${ }^{3}$ Maximum digital output code is 11999 which corresponds to an input of 11.999 V .
${ }^{4}$ Resolution, coding, and counting scheme are determined by the configuration of the external counter.
${ }^{5}$ The ADC1105 is also available in a version mounted on a $4.5^{\prime \prime} \times 2.8^{\prime \prime}$ printed circuit card. This card contains the necessary adjustment pots and it mates with a Cinch 251-22-30-160 dual 22 pin edge connection.


# HIGH SPEED A/D CONVERTERS ADCIIO3, ADCllo9 

## GENERAL DESCRIPTION

These analog-to-digital converters are characterized primarily by very high speed. They are especially well suited for applications requiring high throughput rates with no compromise in accuracy. They can be considered general purpose devices as well, however, and are a natural choice for large data acquisition systems. Among other typical applications are geophysical data acquisition, simultaneous sample-and-hold systems, and conversion for data entry into digital filters and correlators.

## ADC1103

The ADC1103 is a very fast successive approximation converter packaged in a small $2^{\prime \prime} \times 4^{\prime \prime}$ module. The 12 bit version performs a full conversion in less than $3.5 \mu \mathrm{~s}$. The ADC1103 is a complete self-contained converter, requiring only standard $\pm 15 \mathrm{~V}$ and +5 V power, and the usual control signals. The input range and output coding are user selected.


ADC1109
The ADC1109 uses the successive approximations technique $t$ perform complete 10 bit conversions in $4 \mu \mathrm{~s}$. The data output of this compact $2^{\prime \prime} \times 3^{\prime \prime} \times 0.4^{\prime \prime}$ module are available in both parallel and serial form. The ADC1109 can be configured by the user to accept either unipolar or bipolar inputs and produce either of three output codes.

## ORDERING GUIDE

ADC1103-XXX
-001 (8 BIT)

- 002 (10 BIT)
_003 (12 BIT)

BLOCK DIAGRAM AND PIN DESIGNATIONS ADC1103


Note: The standard model does not have a serial output, and therefore pins 58 and 61 are deleted from it. In addition, the ADC1103-002 does not contain pins 32 and 34, and the ADC1103001 does not contain pins 27,30, 32, and 34 .

SPECIFICATION SUMMARY (Typical @ $+25^{\circ} \mathrm{C}$ unless otherwise noted)

| Model | ADC1103-001 | ADC1103-002 | ADC1103-003 | ADC1109 |
| :---: | :---: | :---: | :---: | :---: |
| Resolution | 8 Bits | 10 Bits | 12 Bits | 10 Bits |
| Conversion Time | $1 \mu \mathrm{~s}$ (max) | $1.5 \mu \mathrm{~s}$ (max) | $3.5 \mu \mathrm{~s}$ (max) | $4 \mu \mathrm{~s}$ (max) |
| Accuracy |  |  |  |  |
| Error Relative to Full Scale | $\pm 112$ LSB (max) | * | $\pm 1 \mathrm{LSB}$ (max) | $\pm 1 / 2$ LSB |
| Differential Nonlinearity Error | $\pm 1 / 2 L S B(\max )$ | * | $\pm 1$ LSB (max) | $\pm 1 / 2$ LSB |
| Temperature Coefficients |  |  |  |  |
| Gain | $\pm 10 \mathrm{ppm} /{ }^{\circ} \mathrm{C}(\max )$ | * | * | $\pm 30 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |
| Zero | $\pm 5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}(\mathrm{max})$ | * | * | $\pm 200 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ |
| Offset | $\pm 10 \mathrm{ppm} /{ }^{\circ} \mathrm{C}(\max )$ | * | * | $\pm 200 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ |
| Analog Input Ranges | 0 to $+10 \mathrm{~V}, \pm 10 \mathrm{~V}, \pm 5 \mathrm{~V}$ | * | * | $\pm 5 \mathrm{~V}, 0$ to +10 V |
| Input Impedance | $5 \mathrm{k} \Omega$ on $\pm 10 \mathrm{~V}$ Range | * | * | $10 \mathrm{k} \Omega$ |
| Digital Inputs and Outputs | TTL Compatible | * | * | * |
| Output Codes |  |  |  |  |
| with Unipolar Inputs | BIN | * | * | BIN |
| with Bipolar Inputs | OBN, 2SC | * | * | OBN, 2SC |
| Status Output | " 1 " During Conversion; Complement Available | * | * | * |
| Serial Data Output | Optional | * | * | Yes |
| Power Required | +15V @ 85 mA (max) | * | * | +15V@ 40mA (max) |
|  | -15V @ 80mA (max) | * | * | -15V @ 40mA (max) |
|  | +5V @ 525 mA (max) | * | * | +5V @ 135mA (max) |
| Package Style | CA-3 | * | * | CA-2 |
| Package Dimensions | $2^{\prime \prime} \times 4^{\prime \prime} \times 0.75^{\prime \prime}$ | * | * | $2^{\prime \prime} \times 3^{\prime \prime} \times 0.4{ }^{\prime \prime}$ |
| Price (1-9) | \$473. | \$484. | \$495. | \$159. |

## BLOCK DIAGRAM AND PIN DESIGNATIONS <br> <br> ADC1109

 <br> <br> ADC1109}

## LOW POWER A/D CONVERTERS ADC-I2QL, ADCII23

## GENERAL DESCRIPTION

Low power converters have been developed to solve the problems of operation in remote areas with limited power. Ideally suited for operation from battery power, these products are particularly useful for ocean buoy installation, as well as for remote meteorlogical data acquisition. The small size and light weight also make them useful in portable medical and scientific instruments.


## ADC-12QL

The ADC-12QL is an $A / D$ converter having total power consumption of about $1 / 2000$ of that of a conventional design. Requiring only a single battery to supply all its power needs, it allows the systems engineer to make important savings in power source weight and volume. The ADC-12QL normally rests in a standby state. The converter is turned on by the convert command, fully stabilizes in a few microseconds; at the end of the conversion, it returns automatically to the standby state.

ADC1123
The ADC1123 is an economical 10 bit version of the ADC12 QL . It offers low power consumption, single battery operation and freedom from missing codes over the entire 0 to $+70^{\circ} \mathrm{C}$ operating range. The customer can order the unit with either of four input voltage ranges but, unlike the ADC-12QL, only one grade of gain stability is offered.

ORDERING GUIDE: ADC-QL
MODEL ADC - 12QL

| //X <br> Gain <br> Stability | $\mathbf{X X}$ Input Range |
| :---: | :---: |
| $\begin{aligned} & \mathrm{J}-50 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ & \mathrm{~K}-20 \mathrm{ppm} /{ }^{\circ} \mathrm{C} \end{aligned}$ | $\begin{aligned} & +5(\mathrm{~V}) \\ & \pm 5(\mathrm{~V}) \\ & +10(\mathrm{~V}) \\ & \pm 10(\mathrm{~V}) \end{aligned}$ |

PIN DESIGNATIONS: ADC-12QL

| PIN | FUNCTION | PIN | FUNCTION |
| :---: | :---: | :---: | :---: |
| 1 | N.C. | A | BIT 1 (MSB) |
| 2 | CLOCK | B | BIT 2 |
| 3 | EXTERNAL CLOCK CAP. | C | BIT 3 |
| 4 | STATUS | D | BIT 4 |
| 5 |  | E | BIT 5 |
| 6 | N.C. | F | BIT 6 |
| 7 |  | H | BIT 7 |
| 8 | SERIAL OUT | J | BIT 8 |
| $9)$ |  | K | BIT 9 |
| 10 |  | L | BIT 10 |
|  | N.C. | M |  |
| 12 |  | N | BIT 12 (LSB) |
| 13 |  | $\left.\begin{array}{l}\mathrm{P} \\ \mathrm{R}\end{array}\right)$ |  |
| 14 |  | $\left.\begin{array}{l}\mathrm{R} \\ \mathrm{S}\end{array}\right\}$ |  |
| 16 | N.C. | T | N.C. |
| 17 | LOGIC SUPPLY | U |  |
| 18 | ANALOG INPUT | V | CONVERT COMMAND |
| 19 | SIGNAL GROUND | W | N.C. |
| 20 |  | X | N.C. |
| 21 \} | N.C. | Y | ANALOG SUPPLY |
| 22 |  | Z | N.C. |

SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ unless otherwise noted)

| Model | ADC-12QL |  |  |  | ADC1123 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Resolution, Bits | $\begin{gathered} 12 \\ \pm 1 / 2 \operatorname{LSB}(\max ) \end{gathered}$ |  |  |  | 10 |
| Linearity Error |  |  |  |  | $\pm 1 / 2$ LSB (max) |
| Analog Input Ranges ${ }^{1}$ | $+5 \mathrm{~V}$ | $\pm 5 \mathrm{~V}$ | +10V | $\pm 10 \mathrm{~V}$ | * |
| Input Impedance | $4.1 \mathrm{k} \Omega$ | $8.2 \mathrm{k} \Omega$ | $8.2 \mathrm{k} \Omega$ | $16.4 \mathrm{k} \Omega$ |  |
| Conversion Time | $85 \mu$ s with +15 V logic supply $130 \mu$ s with +6 V logic supply |  |  |  | $65 \mu \mathrm{~s}$ with +15 V logic supply <br> $90 \mu$ s with +6 V logic supply |
| Digital Inputs and Outputs Parallel Data Output Serial Data Output | BIN, OBN <br> NRZ format, MSB first C-B, COB coded |  |  |  | * $\begin{aligned} & * \\ & *\end{aligned}$ |
| Convert Command Status Signal | $1 \mu$ s to $4 \mu$ s positive pulse logic " 1 " during conversion |  |  |  | * |
| Temperature Coefficient Gain (of Reading) <br> Unipolar Zero <br> Bipolar Offset | J opt $50 \mathrm{ppm} /$ $50 \mu \mathrm{~V} /{ }^{\circ}$ 20ppm/ | $\begin{aligned} & \text { ion } \\ & C(\max ) \\ & C(\max ) \\ & C(\max ) \end{aligned}$ | $\begin{array}{r} \mathrm{K} \\ 20 \mathrm{pp} \end{array}$ | option $\mathrm{m} /{ }^{\circ} \mathrm{C}(\max )$ | $50 \mathrm{ppm} /{ }^{\circ} \mathrm{C}(\max )$ |
| Power Required ${ }^{3}$ Logic Supply Analog Supply | $\begin{aligned} & +6 \mathrm{~V} \text { to }+15 \mathrm{~V} \\ & +12 \mathrm{~V} \text { to }+15 \mathrm{~V} \\ & \hline \end{aligned}$ |  |  |  | * |
| Power Consumption ${ }^{4}$ Quiescent Power Energy per Conversion | $600 \mu \mathrm{~W}$ <br> $75 \times 10^{-6}$ Joules/Conversion @ +15V <br> $57 \times 10^{-6}$ Joules/Conversion @ +12V |  |  |  | * |
| Package Style <br> Package Dimensions | $\begin{gathered} \mathrm{C}-8 \\ 4.1^{\prime \prime} \times 4.025^{\prime \prime} \times 0.35^{\prime \prime} \\ (104.1 \times 102.24 \times 8.89 \mathrm{~mm}) \end{gathered}$ |  |  |  | * |
| Price ( $1-9)^{5}$ | J option K option <br> $\$ 709$ $\$ 998$ |  |  |  | \$299 |

${ }^{1}$ The input voltage range is set at the factory.
${ }^{2}$ Low power TTL logic can be directly driven when the logic supply voltage is set to its +6 V minimum.
${ }^{3}$ The ADC-12QL and ADC1123 can be operated from a single +12 V to +15 V battery.
${ }^{4}$ The power consumption at any conversion rate equals:
Quiescent power + (Energy/Conversion) - (Conversions/Second)
${ }^{5}$ The prices shown for the $\mathrm{ADC}-12 \mathrm{QL}$ are for $1-4$ pieces.

## BLOCK DIAGRAM <br> ADC1123



ORDERING GUIDE: ADC1123
ADC1123/XX


# HIGH RESOLUTION A/D CONVERTER ADC-16Q 

## GENERAL DESCRIPTION

When maximum resolution and accuracy are required, a 16 bit state-of-the-art A/D converter is called for. An analog-to-digital converter with 65,536 distinct output codes, where an LSB is only $152 \mu \mathrm{~V}$, demands advanced engineering, skilled manufacturing, and the use of the highest quality available components, without compromise.

## ADC-16Q

The 16 bit ADC-16Q offers unprecedented linearity, accuracy, and stability in a very compact package. The $41 / 2^{\prime \prime} \times 6^{\prime \prime}$ P.C. board holds two modules: a standard DAC-16QM, and the I/O (input/output) module which contains successive approximations logic, a precision comparator, and a differential input buffer that features high common mode rejection. The no-effort-spared engineering that went into the design of the ADC-16Q took into account not only the internal design

problems, but also the system problems faced by a user who needs to make sure that the converter will perform in his system to the accuracy of which it is capable. Each ADC-16Q is supplied with a reference certificate and an error plot of its DAC made during final production test.

PIN DESIGNATIONS: ADC-16Q

| PIN | FUNCTION | PIN | FUNCTION |
| :---: | :---: | :---: | :---: |
| 1 | $\overline{\text { BIT } 1 ~(\overline{M S B}}$ ) | A | BIT 1 (MSB) |
| 2 | N.C. | B | BIT 2 |
| 3 | N.C. | C | BIT 3 |
| 4 | N.C. | D | BIT 4 |
| 5 | \} INTERLOCK | E | BIT 5 |
| 6 | f INTERLOCK | F | BIT 6 |
| 7 | N.C. | H | BIT 7 |
| 8 | \} EXTERNAL CAPACITOR | J | BIT 8 |
| 9 | f FOR CLOCK RATE | K | BIT 9 |
| 10 | N.C. | L | BIT 10 |
| 11 | BIT 14 | M | BIT 11 |
| 12 | BIT 15 | N | BIT 12 |
| 13 | BIT 16 (LSB) | P | BIT 13 |
| 14 | SERIAL OUTPUT | R | CLOCK OUTPUT |
| 15 | CONVERT INPUT | $\mathrm{S}^{\dagger}$ | SHORT CYCLE RETURN |
| 16 | STATUS OUTPUT | T | STATUS OUTPUT |
| 17 | DIGITAL 5V COMMON | U | +5VDC INPUT ( $\mathrm{V}_{\mathrm{L}}$ ) |
| 18 | +15VDC INPUT ( $+\mathrm{V}_{\mathrm{S}}$ ) | V | -15VDC INPUT ( $-\mathrm{V}_{\mathrm{S}}$ ) |
| $19 \ddagger$ | $\pm 15 \mathrm{~V}$ COMMON | W $\ddagger$ | $\pm 15 \mathrm{~V}$ COMMON |
| $20^{*}$ | SIGNAL (-) INPUT | X* | SIGNAL (-) INPUT |
| 21 | SIGNAL (+) INPUT | $\mathrm{Y}^{*}$ | SIGNAL (-) INPUT |
| 22* | SIGNAL (-) INPUT | Z* | SIGNAL (-) INPUT |

*Pins 20, 22, X, Y, Z all connected internally to signal ( - ) input. Do not use as tie points for any function other than signal input. $\ddagger$ Pins 19 and W are connected together internally. Use one for power ground and the other for signal source ground return.
${ }^{\dagger}$ Must be tied to P in $\# 17$ for 16 -bit operation.

## NOTES:

1. In buffered modes, input is true differential. Thus reversal of input connections would yield ranges of 0 to -10 V , $\pm 10 \mathrm{~V}$, and $\pm 5 \mathrm{~V}$.
2. When shipped, units will be jumpered for $\mp 10 \mathrm{~V}$ operation with buffer. User can change jumpers to select a different input voltage range, and/or omit input buffer.

SPECIFICATION SUMMARY (Typical @ $+25^{\circ} \mathrm{C}$ unless otherwise noted)

| Model | ADC-16Q |
| :---: | :---: |
| Resolution, Bits | 16 Binary |
| Linearity Error | $\pm 0.0015$ \% |
| Analog Input |  |
| Ranges (Volts) | $\pm 5, \pm 10,+10$ |
| Impedance |  |
| Direct <br> with Buffer | 5 k or 10 k ohms ${ }^{1}$ $10^{9}$ ohms |
| Conversion Time to Full Accuracy | $400 \mu \mathrm{~s}^{2}$ |
| Settling Time of Input Buffer to Full Accuracy | $3.6 \mathrm{~ms}^{2}$ |
| Digital Control |  |
| Inputs and Outputs | TTL/DTL Compatible |
| Data Outputs | TTL Positive True |
| Output Codes | BIN, OBN, 2SC |
| Output Formats | Parallel \& Serial |
| Reference | Internal precision reference |
| Temperature Coefficient |  |
| Gain | $0.0008 \% /{ }^{\circ} \mathrm{C}$ max |
| Offset | $0.0002 \% /{ }^{\circ} \mathrm{C} \pm 25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max |
| Power Required | +15V @ 18 mA |
|  | -15V @ 41 mA |
|  | +5 V @ 350 mA |
| Package Style | C-8 |
| Package Dimensions | $41^{\prime 2} 2^{\prime \prime} \times 6.0^{\prime \prime} \times 0.44^{\prime \prime}$ |
| Price (1-9) | \$1418. |
| ${ }^{1}$ Direct input impedance is 10 k ohms for $\pm 10 \mathrm{~V}$ input range, and 5 k ohms for other input ranges. |  |
| ${ }^{2} \mathrm{ADC}-16 \mathrm{Q}$ can be operated at higher speeds with reduction in accuracy, or short-cycled. |  |



## GENERAL DESCRIPTION

The MPX-8A is an accurate high-speed 8-channel MOSFET multiplexer complete with versatile binary address control logic. It can be used either with A/D converters to acquire data from a number of sources, or with D/A converters to distribute data to a number of loads.
The control logic contained within the MPX-8A allows the user to connect the unit as either an 8 -channel single-ended multiplexer, or as a 4-channel differential mode multiplexer. All of the logic needed to expand to up to 64 channels is also included.

## LOGIC FLOW DIAGRAM MPX-8A



SPECIFICATION SUMMARY (Typical @ $+25^{\circ} \mathrm{C}$ unless otherwise noted)

| Model | MPX-8A |
| :--- | :---: |
| Channels |  |
| $\quad$ Single-Ended | $8^{1,2}$ |
| $\quad$ Differential | 4 |
| Voltage Range |  |
| $\quad$ Rated Operation | $\pm 10 \mathrm{~V}$ |
| $\quad$ Overload Protection | $\pm 15 \mathrm{~V}$ |
| Transfer Error | $0.01 \%$ |
| Settling to 0.01\% | $<2 \mu \mathrm{~s}$ |
| Cross Channel Coupling | $<-80 \mathrm{~dB}$ |
| Common Mode Rejection |  |
| $\quad$ DC | 120 dB |
| 60 Hz | 106 dB |
| Channel Addressing | Binary Code |
| Address Logic | $\mathrm{TTL} \mathrm{Compatible/Positive} \mathrm{True}$ |
| Power Requirement | $+15 \mathrm{~V}, \pm 1 \mathrm{~V}$ @ 6.2 mA |
|  | $-15 \mathrm{~V},-1 \mathrm{~V},+0 \mathrm{~V}$ @ 4 mA |
| $\quad+5 \mathrm{~V}, \pm 10 \%$ @ 102 mA |  |
| Package Style | $\mathrm{C}-1$ |
| Package Dimensions | $2^{\prime \prime} \times 2^{\prime \prime} \times 0.4^{\prime \prime}$ |
| Price (1-9) | $\$ 184$ |

[^11]
# SAMPLE-AND-HOLD AMPLIFIERS SHA-IA, 2A, 3, 4, 5, 6 

## GENERAL DESCRIPTION

Analog Devices' wide selection of Sample-and-Hold Amplifiers (SHA's) permits the selection of a SHA that is well suited for virtually any application. Each type offers a unique combination of speed, accuracy, and cost.

SHA-1A
The SHA -1 A is a general purpose SHA offering moderately high speed and accuracy at a reasonable price. It settles to $0.01 \%$ in under $5 \mu \mathrm{~s}$, and its droop rate (decay when in HOLD) is no greater than $50 \mu \mathrm{~V} / \mu \mathrm{s}$.

## SHA-2A

The SHA-2A is a very fast Sample-and-Hold module with accuracy and dynamic performance that make it appropriate for use with very fast 12 bit A/D converters. It settles to $0.1 \%$ in less than 300 ns , and to $0.01 \%$ in less than 500 ns .

SHA-3 and SHA-4
These two SHA's were designed for high accuracy at longer hold times. They settle to $0.01 \%$ in $75 \mu \mathrm{~s}$ or less. The two differ in that when switched from HOLD to SAMPLE, the SHA-4 settles more rapidly than does the SHA-3.


SHA-5
The SHA-5 is a low cost general purpose sample-and-hold that offers good performance at a very low price. It settles to $0.01 \%$ in $15 \mu \mathrm{~s}$, and has a droop rate of only $20 \mu \mathrm{~V} / \mathrm{ms}$.

SHA-6
The SHA-6 was designed as a companion to the high resolution ADC-16Q A/D converter. It will acquire a signal to 16 bit accuracy $(0.00075 \%)$ in 5 ms , and then hold it long enough for the ADC-16Q to convert it to a 16 bit digital word. It features excellent gain stability over both time and temperature.

PIN DESIGNATIONS: SHA-1A

1. CONTROL IN
2. DIGITAL GROUND
3. ANALOG GROUND
4. -15VDC
5. POWER GROUND
6. +15VDC
7. ANALOG GROUND
8. ANALOG OUTPUT
9. ANALOG GROUND
10. ANALOG INPUT

PIN DESIGNATIONS: SHA-2A

| 1. INPUT | 29. +15 V |
| :---: | :---: |
| 5. FEEDBACK | 44. TRIM |
| 20. OUTPUT | 46. DIGITAL GROUND |
| 25. -15 V | 48. MODE CONTROL |
| 27. ANALOG GROUND |  |
| PIN DESIGNATIONS: SHA-3, SHA-4, SHA-5 |  |
| 1. ANALOG GROUND | 8. LOGIC GROUND |
| 2. -15 V | 9. N.C. |
| 3. +15 V | 10. EXT. CAPACITOR* |
| 4. ZERO ADJUST* | 11. N.C. |
| 5. ZERO ADJUST* | 12. ANALOG OUTPUT |
| 6. SIGNAL IN | 13. NO PIN |
| 7. CONTROL IN | 14. S-H ADJUST* |
| *N.C. ON SHA-5 |  |

SPECIFICATION SUMMARY (Typical @ $+25^{\circ} \mathrm{C}$ unless otherwise noted)

| APPLICATIONS | General Purpose | Fast | Low Droop Slow Settle | Low Droop Fast Settle | Low Cost | High Resolution |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Model ${ }^{1}$ | SHA-1A | SHA-2A ${ }^{2}$ | SHA- $3^{3}$ | SHA-4 ${ }^{3}$ | SHA-5 | SHA-6 |
| Acquisition Time | $5 \mu \mathrm{~s}$ to | 500 ns to | $75 \mu \mathrm{~s}$ to | $75 \mu$ s to | $15 \mu \mathrm{~s}$ to | 5 ms to |
|  | 0.01\% | 0.01\% | 0.01\% | 0.01\% | 0.01\% |  |
| Droop Rate | $50 \mu \mathrm{~V} / \mathrm{ms}$ max | $10 \mu \mathrm{~V} / \mu \mathrm{s}$ | $10 \mu \mathrm{~V} / \mathrm{ms}$ | $10 \mu \mathrm{~V} / \mathrm{ms}$ | $20 \mu \mathrm{~V} / \mathrm{ms}$ | $10 \mathrm{mV} / \mathrm{sec}$ max |
| Input Range | $\pm 10 \mathrm{~V}$ | $\pm 10 \mathrm{~V}$ | $\pm 10 \mathrm{~V}$ | $\pm 10 \mathrm{~V}$ | $\pm 10 \mathrm{~V}$ | $\pm 11 \mathrm{~V}$ |
| Gain | 1 | 1 | 1 | 1 | 1 | $\begin{aligned} & 1 \text { to } 1000 \\ & \pm 0.2 \%^{4} \end{aligned}$ |
| Gain Error | +0, -0.05\% | +0, -0.01\% | $\pm 0.01 \%$ | $\pm 0.01 \%$ | $\pm 0.01 \%$ |  |
| Input |  |  |  |  |  |  |
| Impedance | $10^{12} \Omega$ | $10^{11} \Omega$ | $10^{8} \Omega$ | $10^{8} \Omega$ | $4 \times 10^{9} \Omega$ | $10^{9} \Omega$ |
| Aperture Delay Aperture | 40 ns | 10 ns | 50 ns | 50 ns | 40ns | $-1.7 \mu \mathrm{~s}$ |
|  |  |  |  |  |  |  |
| Jitter | 5ns | 0.25 ns | 5ns | 5ns | 4 ns | 10 ns |
| Power Require- $\qquad$ ments $\pm 15 \mathrm{~V}$ | 15 mA | 100 mA | 15 mA | 18 mA | 30 mA | 17 mA |
| Package Size | $2^{\prime \prime} \times 2{ }^{\prime \prime} \times 0.4{ }^{\prime \prime}$ | $2^{\prime \prime} \times 3$ " $\times 0.4$ " | $11 / 8^{\prime \prime} \times 2^{\prime \prime} \times 0.4{ }^{\prime \prime}$ | $11 / 8^{\prime \prime} \times 2{ }^{\prime \prime} \times 0.4 \prime$ | $11 / 8^{\prime \prime} \times 2^{\prime \prime} \times 0.4{ }^{\prime \prime}$ | $2^{\prime \prime} \times 4{ }^{\prime \prime} \times 0.4^{\prime \prime}$ |
| Package Style | C-1 | C-2 | C-4 | C-4 | C-4 | C-3 |
| Price (1-9) | \$150. | \$236 | \$105 | \$132 | \$47. | \$394 |
|  |  |  |  |  | (100+) \$34 |  |

${ }^{1}$ Mode control input on all SHA's is TTL/DTL compatible. On all models except SHA-6, Logic " 1 " is sample and Logic " 0 " is hold. On SHA-6, Logic " 0 " is sample and Logic " 1 " is hold.
${ }^{2}$ SHA-2A may be used as a follower or inverter. It can also be used at gains higher than unity with appropriate degradation in bandwidth.
${ }^{3}$ SHA- 3 and SHA-4 differ only in that SHA-4 settles much faster when switched from HOLD to SAMPLE. Settling Time to $\pm 1 \mathrm{mV}$ is
$100 \mu s$ for SHA-3 and 20 $\mu$ s for SHA-4.
${ }^{4}$ Gain error from formula used to calculate value of gain resistor. Gain stability is $\pm 0.0002 \% / \mathrm{month}$ and $\pm 0.0002 \% /{ }^{\circ} \mathrm{C}$.

## PIN DESIGNATIONS: SHA-6

3.     + EOUT
4. -E OUT
5. -15 V
6. ANALOG COMMON
7. +15 V
8. MODE CONTROL INPUT
9. MODE CONTROL COMMON
10. $-\mathrm{E}_{\text {IN }}$
11. GAIN CONTROL
12. $+\mathrm{E}_{\mathrm{IN}}$
13. GAIN CONTROL

NOTE: The pins listed above are the only pins that appear on the SHA-6.

## ILLUSTRATION OF SPECIFICATIONS



# HIGH RELIABILITY CONVERTERS ADCIIII, DACIII2, SHAIII4, DACIII7 

## GENERAL DESCRIPTION

The ADC1111, DAC1112, SHA1114, and DAC1117 are fully documenied, high reliability converter products which are guaranteed to operate within specifications over the full military temperature range. Qualification testing has proven that these devices are capable of operating under severe environmental conditions. A specification document is available for each product which lists its characteristics and capabilities in great detail.

## ADC1111

The ADC1111 is a high reliability version of the ADC-12QM. It performs 12 bit conversions in $25 \mu$ ( $\max$ ) and has excellent stability over temperature. It comes complete with an input buffer and offers the choice of five user-programmable input voltage ranges. Module dimensions are $2^{\prime \prime} \times 4^{\prime \prime} \times 0.4^{\prime \prime}(51 \mathrm{x}$ $102 \times 10 \mathrm{~mm}$ ). $\$ 895$ (1-9).

## DAC1112

The DAC1112 is a high reliability version of the DAC-12QS. This $2^{\prime \prime} \times 2^{\prime \prime} \times 0.4^{\prime \prime}(51 \times 51 \times 10 \mathrm{~mm})$ module, which comes complete with a versatile output amplifier, settles to $0.01 \%$ accuracy in $5 \mu \mathrm{~s}$. The user can program either of five output voltage ranges by means of jumpers connected to the module's terminal pins. $\$ 475$ (1-9).


## SHA1114

The SHA1114 is a high reliability version of the SHA-2A. It is a fast sample-and-hold amplifier with a 500 ns (max) acquisition time to $0.01 \%$ accuracy. Module dimensions are $2^{\prime \prime} \times 3^{\prime \prime} \times 0.4^{\prime \prime}$ ( $51 \times 76 \times 10 \mathrm{~mm}$ ). $\$ 425$ (1-9).

## DAC1117

The DAC1117 is a high reliability 12 bit current output D/A converter packaged in a $1.5^{\prime \prime} \times 1^{\prime \prime} \times 0.4^{\prime \prime}(38 \times 25 \times 10 \mathrm{~mm})$ hermetically sealed metal enclosure. It settles to $0.01 \%$ accuracy in $3 \mu$ s when used with a high speed output amplifier. This device is also available in a non-military grade extended temperature version, the MDA-12QD/ET, and a commercial grade version, the MDA-12QD. $\$ 555$ (1-9).

## THE HIGH RELIABILITY CONVERTER PROGRAM

Analog Devices has, over the past several years, supplied a great many A/D and D/A converter modules intended for military and critical industrial applications. As a result of this experience, we know what is needed in a high reliability converter and what it takes to build one. This experience is now available to you in the form of the industry's first line of converter products intended expressly for high reliability applications.

## ADVANTAGES TO THE USER

The first big advantage is the ease of specification. As part of our development program, we have generated a separate specification drawing for each of the four products. These drawings run an average of 17 pages and specify in exact detail all pertin-
ent characteristics of the module. By copying our drawing over onto his own specification control drawing format, the user can completely specify a high reliability converter module in a very short time with a mimimum of effort.

The second advantage is that the system designer can get quick delivery of units needed for breadboarding and prototyping. Sinc the high reliability converters are standard products for us, they'r available in small quantities in a few weeks or less.

The third advantage is cost. The user is no longer in the position of having to subsidize the development of a special high reliability converter. We have sustained all the development costs and the user pays only for the modules he actually requires

THE SPECIFICATION DOCUMENT
Specification documents for all four products in the High Reliability Converter Program are organized as shown below.

| 1.0 | SCOPE |
| ---: | :--- |
| 2.0 | GENERAL REQUIREMENTS |
| 3.0 | APPLICABLE DOCUMENTS |
| 4.0 | ABSOLUTE MAXIMUM RATINGS |
| 5.0 | ELECTRICAL SPECIFICATIONS |
| 6.0 | MODULE CONNECTIONS |
| 7.0 | MECHANICAL SPECIFICATIONS |
| 8.0 | ENVIRONMENTAL SPECIFICATIONS |
| 9.0 | QUALITY CONFORMANCE INSPECTION |
| 10.0 | CALCULATED MEAN TIME BETWEEN FAILURES |
| 11.0 | COMPONENTS |
| 12.0 | PREPARATION FOR DELIVERY |

Highlights of the major sections are presented in the following paragraphs.
Electrical Specifications. The electrical specifications are listed at $-55^{\circ} \mathrm{C},+25^{\circ} \mathrm{C}$, and $+125^{\circ} \mathrm{C}$ in minimum/nominal/maximum format. In general, the room temperature specifications for the high reliability converters are identical to those of their commercial grade counterparts.

Environmental Specifications. This section lists the numerous environmental tests which the modules are capable of passing. These tests are listed below in abbreviated form.

| Test |
| :--- |
| Visual and Mechanical |
| Barometric Pressure |
| $\quad$ (Reduced) |
| Temperature Cycling |
| Moisture Resistance |
| Shock |
| Terminal Strength |
| Vibration Fatigue |
| Steady-State Life |
| Solderability |
| Salt Atmosphere |
| High Temperature Storage |
| Fungus Resistance |


| MIL-STD | Method |
| :---: | :---: |
| 883 | 2008 |
|  |  |
| 202 | 105 |
| 883 | 1010 |
| 883 | 1004 |
| 883 | 2002 |
| 202 | 211 |
| 883 | 2005 |
| 883 | 1005 |
| 883 | 2003 |
| 883 | 1009 |
| 883 | 1008 |
| MIL-I-46058 |  |

Quality Conformance Inspections. Quality conformance inspections are performed at every stage of the manufacturing process as shown on the simplified manufacturing flow chart to the right. The overall inspection system meets the requirements of MIL-I-45208. Note that the temperature cycling listed on the chart is performed in accordance with MIL-STD-883, method 1010 , condition B and that the 168 hour burn-in is performed with the unit at power at $+125^{\circ} \mathrm{C}$.

Components. All components, unless otherwise specified, must meet applicable requirements of the appropriate military specifications. For example, microcircuits qualified to MIL-M-38510, class B must be used if they are available. Second preference is given to microcircuits processed to MIL-M-38510, class B and third preference is given to microcircuits processed to the applicable requirements of MIL-STD-883, class B.
Discrete semiconductors must be hermetically sealed and meet the requirements of MIL-S-19500. Passive components must meet their appropriate military specifications. Even printed circuit boards, encapsulating compound, plastic cases, and terminal pins must meet applicable military specifications.

## SIMPLIFIED MANUFACTURING FLOW CHART



# TRACKING SYNCHRO-TO-DIGITAL CONVERTERS SDCI602, SDCI603, SDCI604 

## GENERAL DESCRIPTION

The "SDC" series converters are continuous tracking, type 2 servo loop, synchro or resolver to digital converters intended for military and industrial control applications.
Model SDC1602 is a 14 bit S to D converter with an accuracy of $\pm 4$ arc-minutes.
Model SDC1603 is a 10 bit S to D converter with an accuracy of $\pm 30$ arc-minutes.
Model SDC1604 is a 16 bit S to D converter with an accuracy of $\pm 1$ arc-minute.


Thin film networks, monolithic analog switches and M.S.I. logic functions are used in constructing the converters. These and other support circuits such as op amps and comparators can be released to the requirements of MIL-STD-883 B.

## COMMON SPECIFICATIONS

## Table I

Signal Voltages: (RMS Line-to-Line)

| Synchro 11.8V | Resolver | 11.8 V |
| :--- | :--- | ---: |
| Synchro 90.0V | Resolver | 26.0 V |
|  | Resolver | 90.0 V |
|  | Resolver | 115.0 V |

Reference Voltages: (RMS)
11.8 V or $26 \mathrm{~V} \quad 60 \mathrm{~Hz}$ or 400 Hz

90 V or $115 \mathrm{~V} \quad 60 \mathrm{~Hz}$ or 400 Hz
Signal Impedances: (As inputs to the device)
20 k ohms $\quad$ L-L balanced for 11.8 V or 26 V
200 k ohms L-L balanced for 90 V or 115 V
Reference Impedances: (As input to the device)
20 k ohms for 11.8 V or 26 V
200 k ohms for 90 V or 115 V
Transformer Isolation: 500VDC
Logic Levels: DTL/TTL Compatible

Temp. Range Storage: $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
Warm-up Time: 1 second to rated accuracy
Input or Output Coding: Natural Binary Angle
Bit $1=180^{\circ}$
Bit $2=90^{\circ}$
etc.
Resolution vs. LSB Weight:
10 bit units 1 LSB is 21 arc-minutes
14 bit units 1 LSB is 1.3 arc-minutes
16 bit units 1 LSB is 20 arc-seconds
Accuracy: Applies for following plus the listed parameters in the individual specification summaries
$\pm 5 \%$ power supply variation
$\pm 10 \%$ signal and/or reference frequency variation
$10 \%$ signal and/or reference harmonic distortion
$\pm 10 \%$ signal and/or reference amplitude variation


Block Schematic for "SDC" Series Converters

SPECIFICATION SUMMARY (typical @ $+25^{\circ} \mathrm{C}$ and $\pm 15 \mathrm{VDC}$ and +5 VDC unless otherwise noted)

|  | SDC1603 | SDC1602 | SDC1604 |
| :---: | :---: | :---: | :---: |
| Accuracy ${ }^{1}$ (max error): | $\pm 30$ arc-minutes ${ }^{2}$ | $\pm 4$ arc-minutes ${ }^{2}$ | $\pm 1$ arc-minute ${ }^{3}$ |
| Synchro and Reference Inputs: | See Table I | * | * |
| Output Resolution: | 10 bits | 14 bits | 16 bits |
| Tracking <br> Rate: $\mathbf{( 4 0 0 H z )}$ | $2880^{\circ} / \mathrm{sec}$ | $1440{ }^{\circ} / \mathrm{sec}$ | $720^{\circ} / \mathrm{sec}$ |
| $179^{\circ}$ Step Response: (to1LSB) | 200 msec | 300 msec | 400 msec |
| Operating Temp. Range: | $\begin{gathered} 0 \text { to } 70^{\circ} \mathrm{C} \text { or } \\ -55^{\circ} \mathrm{C} \text { to }+105^{\circ} \mathrm{C} \end{gathered}$ |  | $-55^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C}$ |
| Power <br> Supplies: | $\begin{aligned} & +15 \mathrm{~V} @ 35 \mathrm{~mA} \\ & -15 \mathrm{~V} @ 35 \mathrm{~mA} \\ & +5 \mathrm{~V} @ 190 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & +15 \mathrm{~V} @ 40 \mathrm{~mA} \\ & -15 \mathrm{~V} @ 40 \mathrm{~mA} \\ & +5 \mathrm{~V} @ 240 \mathrm{~mA} \\ & \hline \end{aligned}$ | $\begin{aligned} & +15 \mathrm{~V} @ 60 \mathrm{~mA} \\ & -15 \mathrm{~V} @ 60 \mathrm{~mA} \\ & +5 \mathrm{~V} @ 300 \mathrm{~mA} \\ & \hline \end{aligned}$ |
| Power <br> Dissipation: | 2.2 Watts | 2.8 Watts | 3.5 Watts |
| Converter <br> Module Size: | $3.125^{\prime \prime} \times 2.625^{\prime \prime} \times 0.8^{\prime \prime}$ | * | * |
| Transformer Module Size: | $3.125^{\prime \prime} \times 1.5^{\prime \prime} \times 1.0^{\prime \prime}$ | * | *4 |
| Weight: | 7 oz . | * | * |
| ${ }^{1}$ Accuracy applies per Table I parameters plus $\pm 20^{\circ}$ phase shift between reference and signal plus <br> ${ }^{2}$ Over the operating temp. range <br> ${ }^{3} \pm 1.3$ arc-minutes 0 to $+70^{\circ} \mathrm{C}$ or $\pm 2$ arc-minutes $-55^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ <br> ${ }^{4}$ Consult factory on form factors available for 60 Hz transformers |  |  |  |

## ORDERING GUIDE - SDC SERIES

1. Specify the basic model number per the following table. 60 Hz versions of the 10 and 14 bit units and 400 Hz or 60 Hz versions of the 16 bit units, require separate transformer modules.

| \# of Bits | Temp. Range | Freq. | Converter | Transformers | Price |
| :--- | :--- | :--- | :--- | :--- | :--- |
| 16 | 0 to $+70^{\circ} \mathrm{C}$ | 400 Hz | SDC1604507 | STM163251Z | $\$ 1065+\$ 135$ |
| 16 | $-55^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 400 Hz | SDC1604707 | STM163271Z | $\$ 1465+\$ 175$ |
| 16 | 0 to $+70^{\circ} \mathrm{C}$ | 60 Hz | SDC1604507 | STM163252Z | $\$ 1065+\$ 135$ |
| 16 | $-55^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 60 Hz | SDC1604707 | STM163272Z | $\$ 1465+\$ 175$ |
| 14 | 0 to $+70^{\circ} \mathrm{C}$ | 400 Hz | SDC160251Z | Integral | $\$ 640$ |
| 14 | $-55^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ | 400 Hz | SDC160261Z | Integral | $\$ 720$ |
| 14 | 0 to $+70^{\circ} \mathrm{C}$ | 60 Hz | SDC1602507 | STM163152Z | $\$ 630+\$ 70$ |
| 14 | $-55^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ | 60 Hz | SDC1602607 | STM163162Z | $\$ 690+\$ 90$ |
| 10 | 0 to $+70^{\circ} \mathrm{C}$ | 400 Hz | SDC160351Z | Integral | $\$ 445$ |
| 10 | $-55^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ | 400 Hz | SDC160361Z | Integral | $\$ 520$ |
| 10 | 0 to $+70^{\circ} \mathrm{C}$ | 60 Hz | SDC1603507 | STM163052Z | $\$ 430+\$ 60$ |
| 10 | $-55^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ | 60 Hz | SDC1603607 | STM163062Z | $\$ 485+\$ 80$ |

2. Z is replaced by a number from 1 through 8 to specify synchro or resolver input plus signal/reference voltage range.
$\mathrm{Z}=1$ signifies synchro 11.8 V L-L with 26 V reference
$\mathrm{Z}=2$ signifies synchro 90 V L-L with 115 V reference
$\mathrm{Z}=3$ signifies resolver 11.8 V L-L with 11.8 V reference
$\mathrm{Z}=4$ signifies resolver 26 V L-L with 26 V reference
$\mathrm{Z}=5$ signifies resolver 90 V L-L with 90 V reference
$\mathrm{Z}=6$ signifies resolver 115 V L-L with 115 V reference
$\mathrm{Z}=8$ signifies resolver 11.8 V L-L with 26 V reference
3. Resolver input devices, with $Z=3,4,5,6$ or 8 , are identified as RDC1602513, RTM1630625 and the like. An R replaces the S as the first letter in the part number.

## TWO SPEED S/D CONVERTERS TSL AND TSDC SERIES

## GENERAL DESCRIPTION

## Two speed Processors for Coarse/Fine Synchro Systems.

The TSL and TSDC series of converters provide a digital solution to the problem of combining the multiple speed outputs from a pair of two speed synchros to a single speed output word. The outputs from the mechanically or electrically geared coarse/fine synchros must first be converted to parallel binary angle words. The TSL or TSDC compare the fine output (multiple speed) with the coarse output ( 1 X ) and corrects the coarse reading if an ambiguity exists. The fine reading is digital divided by the speed ratio and added to the corrected coarse reading to provide a single speed output.
The TSDC series provides a dual function: conversion of coarse channel synchro data to 10 bit binary via a tracking $S$ to $D$ converter plus performing two speed processing for binary speed ratios. The converter portion is identical to the SDC1603 specified elsewhere. Binary ratios of $8: 1,16: 1,32: 1$ and $64: 1$ together with a 10 bit converter are provided by the TSDC1608, TSDC1609 , TSDC1610 and TSDC1611 series respectively. A fine channel converter of up to 16 bits binary completes this two speed set.
The TSL1612 provides the two speed logic for the non-binary speed ratios of either $36: 1$ or $18: 1$ (36:2) or $9: 1$ by simple programming of the input/outputs. The TSL1612 accepts a binary angle input of up to 14 bits from a fine channel converter plus a second input of up to 7 bits from a coarse channel converter and provides a single speed output word of up to 19 bits parallel binary angle. The module may be used with any synchro converters which produce a parallel binary output regardless of the conversion process used (tracking or multiplexed).
The number of bits taken from the coarse channel converter $(1 \mathrm{X})$ is equal to $\log _{2} \mathrm{~N}$ where N is the speed ratio. For nonbinary ratios of $36: 1,18: 1$ and $9: 1 \mathrm{~N}$ is 5, 4 and 3 respectively. The coarse channel converter resolution must be $\mathrm{N}+2$ bits minimum, the extra two bits used for ambiguity correction against the fine channel converter output. The fine channel
converter may be any number of bits, up to 14 max. with the TSL, up to 14 or 16 with the TSDC. The length of the combined single speed output word is equal to N plus length of fine channel word.

In a two speed system, the electrical accuracy is the accuracy of the fine channel converter divided by N (the speed ratio).


General Schematic of 36:1 Two Speed System


General Schematic of 32:1 Two Speed System
(typical @ $+25^{\circ} \mathrm{C}$ and +5 VDC unless otherwise noted)

| Fine Synchro Input: | up to 14 bits parallel binary angle |
| :--- | :--- |
| Coarse Synchro Input: | up to 7 bits parallel binary angle |
| Output: | up to 19 bits parallel binary angle |
| Logic Levels: | DTL/TTL compatible |
| Fan In: | 5 TTL loads |
| Fan Out: | 8 TTL loads |
| Conversion Time: | 500 nanoseconds |
| Power: | $+5 \mathrm{~V} \pm 5 \%$ at 750 mA |
| Size: | $3.125^{\prime \prime} \times 2.625^{\prime \prime} \times 0.8^{\prime \prime}$ |
| Temperature: | 0 to $+70^{\circ} \mathrm{C}$ |
| Consult factory for extended temperature range versions |  |
| Price: | $\$ 355$ |
|  |  |

## ORDERING GUIDE

1. Select basic $\mathrm{P} / \mathrm{N}$ from following:

| TSDC1608 | $8: 1$ ratio |
| :--- | :--- |
| TSDC1609 | 16:1 ratio |
| TSDC1610 | $32: 1$ ratio |
| TSDC1611 | $64: 1$ ratio |

2. Select 3 digit suffice from following:

| Suffice | Temp. Range | Freq. | Transformer | Price |
| :--- | :--- | :--- | :--- | :--- |
| 507 | 0 to $+70^{\circ} \mathrm{C}$ | 60 Hz | STM163052Z | $\$ 620+\$ 60$ |
| 607 | $-55^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ | 60 Hz | STM163062Z | $\$ 700+\$ 80$ |
| 51 Z | 0 to $+70^{\circ} \mathrm{C}$ | 400 Hz | Integral | $\$ 635$ |
| 61 Z | $-55^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ | 400 Hz | Integral | $\$ 735$ |

3. Select a number to replace letter Z per Note 2 of SDC ordering guide.
4. Combine selection from 1, 2, 3 above.

Examples:
TSDC1609512 is $16: 1$ ratio, 0 to $70^{\circ} \mathrm{C}, 400 \mathrm{~Hz}$, synchro input, 115 V ref.
TSDC1611607 plus STM1630621 is $64: 1$ ratio, $-55^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}, 60 \mathrm{~Hz}$, synchro input, 26 V ref.

## SPECIFICATION SUMMARY

The TSDC series units are SDC1603 units to which two speed logic has been added for binary ratios. All specifications are the same as an equivalent SDC1603 series unit except:

1. Speed ratio per Ordering Guide
2. A and $B$ digital inputs

## BINARY-TO-BCD CONVERTERS

## GENERAL DESCRIPTION

The BDM series are binary to BCD converters which are scaled to be compatible with an angular range of 0 to 360 mechanical degrees. The parallel input is in binary angle measure (MSB = $180^{\circ}$, next $=90^{\circ}$ etc.) and the output is 5 decade BCD, 8421 coding. Input/outputs are TTL. Conversion time is 500 nanoseconds. Consult factory for extended temperature range versions.

SPECIFICATION SUMMARY (typical @ $+25^{\circ} \mathrm{C}$ and +5 VDC unless otherwise noted)

|  | BDM1615500 | BDM1616500 | BDM1617500 | BDM1618500 |
| :--- | :---: | :---: | :---: | :---: |
| Input: | 14 bits | 14 bits | 16 bits | 16 bits |
| Full Scale <br> Output: | $359.98^{\circ}$ | $359^{\circ} 59^{\prime}$ | $359.99^{\circ}$ | $359^{\circ} 59^{\prime}$ |
| Rounding <br> Error: | $0.02^{\circ}$ | $0.8^{\prime}$ | $0.005^{\circ}$ | $0.25^{\prime}$ |
| Size: | $2^{\prime \prime} \times 4^{\prime \prime} \times .4^{\prime \prime}$ |  |  | $3.125^{\prime \prime} \times 2.625^{\prime \prime} \times 0.8^{\prime \prime}$ |
| Power: | $+5 \mathrm{~V} @ 350 \mathrm{~mA}$ | $*$ | +5 V @ 400 mA | $*$ |
| Temp. <br> Range: | 0 to $+70^{\circ} \mathrm{C}$ | $*$ | $*$ | $*$ |
| Price: | $\$ 190$ | $\$ 190$ | $\$ 210$ | $\$ 210$ |

## DIGITAL-TO-SYNCHRO CONVERTERS DSCl605, DSCI606, DSCI607

## GENERAL DESCRIPTION

The "DSC" series are digital to synchro converters. The inputs are parallel natural binary angle plus an analog reference signal. The outputs are suitable for directly driving a synchro control transformer or resolver, or via external power amplifiers and transformers to drive torque receivers.
Model DSC1605 is a 14 bit D to S converter with an accuracy of $\pm 4$ arc-minutes.

Model DSC1606 is a 10 bit D to S converter with an accuracy of $\pm 30$ arc-minutes.
Model DSC1607 is a 16 bit D to S converter with an accuracy of $\pm 1$ arc-minute.

SPECIFICATION SUMMARY (typical @ $+25^{\circ} \mathrm{C}$ and $\pm 15 \mathrm{VDC}$ and +5 VDC unless otherwise noted)

|  | DSC1606 | DSC1605 | DSC1607 |
| :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Accuracy }^{1} \\ & \text { (max error): } \end{aligned}$ | $\pm 30$ arc-minutes ${ }^{2}$ | $\pm 4$ arc-minutes ${ }^{2}$ | $\pm 1$ arc-minute ${ }^{3}$ |
| Input Resolution: | 10 bits | 14 bits | 16 bits |
| Reference Input: | See Table I (transformer isolated) | * | $\begin{gathered} 2 \mathrm{~V} \mathrm{rms} \\ \text { into } 47 \mathrm{k} \text { ohms } \end{gathered}$ |
| Output Voltages | Synchro 11.8V L-L <br> Synchro 90.0V L-L <br> Resolver 11.8V L-L <br> Resolver 26.0 V L-L <br> Resolver 115.0V L-L |  | $\operatorname{Sin} \theta$ @ 7.5V rms <br> $\operatorname{Cos} \theta$ @ 7.5 V rms |
| Output Load (minimums): | Synchro 11.8V 100 ohms Synchro 90.0V 5K6 ohms Resolver 11.8V 68 ohms Resolver 26.0V 340 ohms Resolver 115.0V 6K8 ohms |  | 2k ohms SPA1641 will drive 13 W at 400 Hz |
| Output | Synchro 11.8V 5 ohms Synchro 90.0V 280 ohms Resolver 11.8 V 5 ohms Resolver 26.0 V 17 ohms Resolver 115.0V 330 ohms |  |  |
| Settling Time: | $80 \mu \mathrm{sec}$ | - $100 \mu \mathrm{sec}$ | $150 \mu \mathrm{sec}$ |
| Power |  |  | DSC1607 plus SPA1641 |
| Supplies: <br> a) No load <br> b) Mean with full load <br> c) Peak with full load $+5 \mathrm{~V}$ | $\left.\begin{array}{c} 40 \mathrm{~mA} \\ 250 \mathrm{~mA} \\ 650 \mathrm{~mA} \\ 10 \mathrm{~mA} \end{array}\right\} @ \pm 15 \mathrm{~V}$ | $\left.\begin{array}{c} 40 \mathrm{~mA} \\ 250 \mathrm{~mA} \\ 650 \mathrm{~mA} \\ 10 \mathrm{~mA} \end{array}\right\} @ \pm 15 \mathrm{~V}$ | $\left.\begin{array}{l} 60 \mathrm{~mA} \\ 2 \mathrm{amps} \\ 2.8 \mathrm{amps} \\ 20 \mathrm{~mA} \end{array}\right\} @ \pm 15 \mathrm{~V}$ |
| Temperature Range ${ }^{4}$ : | $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \text { or } \\ -55^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \end{gathered}$ | * | * |
| Size ${ }^{5}$ : | $3.125^{\prime \prime} \times 2.625^{\prime \prime} \times 0.8$ ' | * | * |

[^12]The DSC1605 and DSC1606 are completely self contained units which include reference and signal transformers, sine/cosine multipliers and power amplifiers capable of 2 watts at $85^{\circ} \mathrm{C}$ or 1 watt at $105^{\circ} \mathrm{C} .60 \mathrm{~Hz}$ versions require an external transformer module.


## Diagram Showing the Principle of the DSC1605

The DSC1607, due to the added circuit complexity for 16 bits, does not include the power amplifiers or transformers within the module. It should be used with the SPA1641 which is a card mounted 13 watt power amplifier plus signal and reference transformers. The SPA1641 card allows the associated DSC1607 to be plugged onto it.


Servo Using D to S Converter

## ORDERING GUIDE

1. Specify the basic model number per the following table. 60 Hz versions of the 10 and 14 bit units require separate transformers. The 16 bit units always need external transformers.

| $\#$ \# of bits | Temp. Range | Freq. | Converter | Transformers | Price |
| :--- | :--- | :--- | :--- | :--- | :--- |
| 16 | 0 to $+70^{\circ} \mathrm{C}$ | 400 Hz | DSC1607517 | - | $\$ 1015$ |
| 16 | $-55^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 400 Hz | DSC1607717 | - | $\$ 1425$ |
| 14 | 0 to $+70^{\circ} \mathrm{C}$ | 400 Hz | DSC160551Z | Integral | $\$ 495$ |
| 14 | $-55^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}^{*}$ | 400 Hz | DSC160571Z | Integral | $\$ 595$ |
| 14 | 0 to $70^{\circ} \mathrm{C}$ | 60 Hz | DSC1605507 | STM163452Z | $\$ 485+\$ 70$ |
| 14 | $-55^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}^{*}$ | 60 Hz | DSC1605707 | STM163472Z | $\$ 575+\$ 90$ |
| 10 | 0 to $+70^{\circ} \mathrm{C}$ | 400 Hz | DSC160651Z | Integral | $\$ 375$ |
| 10 | $-55^{\circ} \mathrm{C}$ to $+85^{\circ}{ }^{\circ} \mathrm{C}^{*}$ | 400 Hz | DSC160671Z | Integral | $\$ 445$ |
| 10 | 0 to $+70^{\circ} \mathrm{C}$ | 60 Hz | DSC1606507 | STM163352Z | $\$ 360+\$ 65$ |
| 10 | $-55^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}^{*}$ | 60 Hz | DSC1606707 | STM163372Z | $\$ 415+\$ 85$ |

Notes 2 and 3 of SDC series ordering guide apply.
*Operation to $+105^{\circ} \mathrm{C}$ possible with linear derating of output to half power at $+105^{\circ} \mathrm{C}$.

## SOLID STATE CONTROL DIFF TRANSMITTER

## GENERAL DESCRIPTION

The SCDX Series are solid state control differential transmitters. Their function is analogous to an electromechanical CDX except that the mechanical input of the CDX has been replaced by a binary input angle. The solid state differential transmitter accepts a digital angle input together with either a 3 wire Synchro (or 4 wire resolver) angle input and gives as output synchro or resolver signals representing the difference between the two input angles. Thus the outputs can be described by A sin wt $\sin$ ( $\theta-\phi$ ) and $\mathrm{A} \sin$ wt $\cos (\theta-\phi)$ where $\theta$ represents the synchro or resolver input angle, $\phi$ represents the binary input angle (14 bits) and wt is the synchro excitation frequency.

The outputs from the SCDX resemble in their function the outputs from a conventional resolver but they are not transformer isolated. The outputs are from a pair of operational amplifiers ( 5.0 volts rms at maximum) which can be fed into a power amplifier and Scott transformer to provide either 3 wire synchro or 4 wire resolver outputs at appropriate voltage levels.


SPECIFICATION SUMMARY (typical @ $+25^{\circ} \mathrm{C}$
and $\pm 15 \mathrm{VDC}$ and +5 VDC unless otherwise noted)
SCDX1623

|  | SCDX1623 |
| :--- | :---: |
| Accuracy ${ }^{\mathbf{1}}$ <br> (max error): | $\pm 4$ arc-minutes |
| Input <br> Resolution: | 14 bits |


| Synchro | See Table I |
| :--- | :---: |
| Inputs: | Transformer isolated |
| Reat |  |


| Reference: | Not required |
| :--- | :--- |
| Output 5V rms into 2k ohms min <br> (not transformer isolated)  |  |
| Ooltages: |  |


| Output | $360^{\circ}$ |
| :--- | :--- |
| Angle Range: |  |
| Power | +15 V @ 45 mA |
| Supplies: | -15 V @ 45 mA |
|  | +5 V @ 20 mA |


| Power <br> Dissipation: | 1.6 Watts |
| :--- | :--- |


| Size: | $3.125^{\prime \prime} \times 2.625^{\prime \prime} \times 0.8^{\prime \prime}$ |
| :--- | :---: |
| Operating | 0 to $+70^{\circ} \mathrm{C}$ or |
| Temperature: | $-55^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ |
| Weight | 7 oz. |
| NOTES: | 1. Accuracy applies over the operating temp. range plus Table |
| I parameters |  |

## ORDERING GUIDE

1. Specify the basic model number per the following table. 60 Hz versions require separate transformers.

| $\#$ of Bits | Temp. Range | Freq. | Converter | Transformers | Price |
| :--- | :--- | :--- | :--- | :--- | :--- |
| 14 | 0 to $+70^{\circ} \mathrm{C}$ | 400 Hz | SCDX162351Z | Integral | $\$ 685$ |
| 14 | $-55^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ | 400 Hz | SCDX162361Z | Integral | $\$ 785$ |
| 14 | 0 to $+70^{\circ} \mathrm{C}$ | 60 Hz | SCDX1623507 | STM163152Z | $\$ 660+\$ 70$ |
| 14 | $-55^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ | 60 Hz | SCDX1623607 | STM163162Z | $\$ 735+\$ 90$ |

Notes 2 and 3 of SDC series ordering guide apply

## SOLID STATE CONTROL TRANSFORMER

## GENERAL DESCRIPTION

This SSCT1621 is a solid state control transformer which performs an identical function to an electromechanical control transformer except that the mechanical input of the latter has been replaced by a digital input. The SSCT1621 accepts a 3 wire synchro input together with a digital angle input and outputs the sine of the difference of the two input angles. The output can be described by A $\sin w t \sin (\theta-\phi)$
 where " $\phi$ " represents a 14 bit parallel binary input angle, " $\theta$ " represents a 3 wire synchro input angle, and " $w t$ " is the synchro excitation frequency.


The scaling of the SSCT1621 is 0.4 volts/degree and the nominal output voltage range is $\pm 5$ volts. This implies a span of $\pm 12.5^{\circ}$ for full scale output. The SSCT1621 is intended for use as an error generator in follow up servo systems and for this reason the span of the device is more than adequate for all such systems. The A.C. output of the SSCT1621 is transformer isolated.

SPECIFICATION SUMMARY (typical @ $+25^{\circ} \mathrm{C}$ and $\pm 15 \mathrm{VDC}$ unless otherwise noted)

| SSCT1621 |  | Power <br> Supplies: | +15 V @ 40 mA <br> -15 V @ 40 mA <br> No +5 V required |
| :---: | :---: | :---: | :---: |
| Accuracy ${ }^{1}$ (max) error): | $\pm 4$ arc-minutes |  |  |
| Input |  |  |  |
| Resolution: | 14 bits | Power Dissipation: | 1.3 Watts |
| Synchro |  |  |  |
| Inputs: | See Table I <br> Transformer Isolated | Size: | $3.125^{\prime \prime} \times 2.625^{\prime \prime} \times 0.8^{\prime \prime}$ |
| Reference: | Not Required | Operating <br> Temperature: | $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \text { or } \\ -55^{\circ} \mathrm{C} \text { to }+105^{\circ} \mathrm{C} \end{gathered}$ |
| Output <br> Voltages: | 5 V rms into 2 k ohms min (transformer isolated) | Weight: | 7 oz |
| Output <br> Angle Range: | $\pm 12.5{ }^{\circ}$ | NOTE: ${ }^{1}$ Accuracy applies over the operating temp. range plus Table I parameters. |  |

The SSCT1621 provides an attractive alternative to digital-tosynchro converters in follow up servo applications since the distribution of system power dissipation, and the elimination of balanced output transformers removes constraints associated with $D$ to $S$ converters.

## ORDERING GUIDE

1. Specify the basic model number per the following table. 60 Hz versions require separate transformers.

| \# of Bits | Temp. Range | Freq. | Converter | Transformers | Price |
| :--- | :--- | :--- | :--- | :--- | :--- |
| 14 | 0 to $+70^{\circ} \mathrm{C}$ | 400 Hz | SSCT162151Z | Integral | $\$ 430$ |
| 14 | $-55^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ | 400 Hz | SSCT162161Z | Integral | $\$ 530$ |
| 14 | 0 to $+70^{\circ} \mathrm{C}$ | 60 Hz | SSCT1621507 | STM163652Z | $\$ 405+\$ 75$ |
| 14 | $-55^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ | 60 Hz | SSCT1621607 | STM163662Z | $\$ 485+\$ 95$ |

Notes 2 and 3 of SDC series ordering guide apply.

# ANGLE POSITION INDICATOR 

## GENERAL DESCRIPTION

Model API 1620 gives a digital display of angles measured by synchros and resolvers. It has a full scale range equivalent to 359.99 mechanical degrees. It has an accuracy of 0.01 degrees and uses a converter which has a resolution of 20 arc-seconds.
Two separate input channels are provided which may be alternately switched into the synchro converter. High level or low level synchros or resolvers can be connected to these inputs and the accuracy or the shaft position of two separate devices can be directly compared.
The meter will work with any reference voltage from 3 volts rms to 115 volts rms and from any reference frequency from 45 Hz to 1100 Hz . A two position "bite" is incorporated which self checks the meter at $45^{\circ}$ and $225^{\circ}$. This is manually operated by a front panel switch.
A push button display check exercises the L.E.D. dot matrix readout and indicates "all 8 's". The internal power unit requires 17 VA 45 to 400 Hz . A power line selector allows voltages of either 115 VAC or 230 VAC to be chosen. A 5 decade binary or BCD output is available. A data hold capability is provided. This allows a display and output data to be frozen.

SPECIFICATIONS (typical @ $+25^{\circ} \mathrm{C}$ unless otherwise noted)

| Accuracy | $\pm 0.01^{\circ} \pm 1$ digit |
| :---: | :---: |
| Angle Range Signal | $\begin{gathered} 000.00^{\circ} \text { to } 359.99^{\circ} \text { continuous } \\ \text { rotation } \end{gathered}$ |
| Temperature Range | $0-50^{\circ} \mathrm{C}$ |
| Power | $115 / 230$ VAC selectable <br> $17 \mathrm{VA} .47 \mathrm{~Hz}-400 \mathrm{~Hz}$ |
| Input Signal Voltages Synchro or Resolver Frequency | $11.8 \mathrm{~V} / 26 \mathrm{~V} / 90 \mathrm{~V}$ <br> Same as Reference |
| Reference Voltage Frequency | 3 volts to 115 volts rms 47 Hz to 1100 Hz |
| Input Impedance Reference Signals | 200k ohms 2 meg ohms |
| Phase Relative to Reference | $20^{\circ}$ |
| Display | 5 digit, dot matrix LED |
| Data Outputs |  |
| Angle | 5 decades BCD (Binary optional) continuously available |
| Inhibit | " 1 " track " 0 " hold |
| Converter Busy | $\begin{aligned} & " 0 " \text { = Data stable } \\ & " 1 "=\text { converter busy } \end{aligned}$ |
| Display Enable | $\begin{gathered} " 0 "=\text { Update (follows) } \\ " 1 "=\text { Hold } \end{gathered}$ |
| Price | \$2800 |




## DIGITAL PANEL METERS

## INTRODUCTION

Today's digital panel meters (DPM's) are extremely useful and valuable components for making precise electrical measurements. They are capable of providing accurate, unambiguous readouts which satisfy a wide range of application requirements for test and laboratory instrumentation. The availability of digital output signals in some DPM designs extend their usefulness in data acquisition systems where it is desirable to interface with data logging or digital control instrumentation.

## GENERAL CONFIGURATION OF DPM's

A basic understanding of how a DPM works can give the user a firmer basis for the selection and application of DPM's. A DPM is basically an analog-to-digital converter with a visual readout. The DPM samples the input voltage, converts the voltage to a digital signal, and presents the data as a visual display and data interface outputs.
There are four functional sections in a digital panel meter: the input section, including the input signal conditioning and conversion circuitry, the display, the data outputs, and the power supply inputs.

## Processing the Input Signal

The primary function of the input section is converting an input voltage to a digital signal for display. In many applications, the DPM must also reject noise picked up on input lines, measure the ratio of two voltages, or compensate for large variations in operating temperature. These requirements must be satisfied by design of the input section.
In its simplest form, the input section is only an analog-todigital converter with a single-ended input. The dual slope converter used in most high accuracy DPM's provides normal mode rejection of high frequency noise by averaging the input signal over a fixed sampling period. By adjusting the averaging period to line frequency, very high rejection of power line noise can be achieved. The staircase converter sometimes used in lowresolution, low-accuracy, low-cost DPM's requires RC filtering of the input signal to provide normal mode noise rejection.
To further reduce the noise picked up on signal lines, one can isolate the input of the DPM with a differential input amplifier. Signals appearing on both input leads simultaneously will be attenuated by the common mode rejection ratio. Besides reducing noise, a differential input allows measurement of differences between two voltages as required in bridge or balanced circuits.
Reduction in the effects of ground loops can be made by isolating the analog and digital sections of the DPM. Optical or transformer isolation of the digital control logic and transformer coupling the DC to DC converter power supply section results in a fully floating analog section. The use of such techniques provides high quality isolation between the analog input section and the display and BCD output registers, and very large ( $>300 \mathrm{~V}$ ) common mode voltages can be accommodated.
Dual slope converters compare the input voltage to a stable reference voltage generated in the input section. By providing an external input for the reference voltage, the input can be compared to any user supplied reference, and the meter reading will be a function of the ratio of the two voltages.

To preserve the accuracy of the DPM over changes of time and temperature, one must correct for zero offset and gain drifts. Automatic zero correction circuitry can be designed into the DPM to reestablish the correct zero level between each measurement. Careful component specification and selection can greatly reduce aging and temperature effects.


## Displaying the Data - Which Display for the Job?

Once the input signal has been processed into digital data bits, it is decoded and displayed for visual readout. Numerous types of displays are available today, including liquid crystal, gas discharge (e.g. Beckman), light-emitting diode (LED), or incandescent (e.g. RCA Numitron). Although liquid crystals have very low power requirements, they do not have good readability in all conditions, and Analog Devices feels that their reliability has not yet been proven sufficient for DPM applications. LED's are extremely rugged and reliable. The availability of LED displays integrated with MSI counters and latches simplifies DPM design, enhances reliability and allows extremely small DPM packages. The $0.27^{\prime \prime}$ character size of these LED displays makes them easily readable for bench-top or other close-in operating conditions (less than $8^{\prime}$ ), under normal ambient lighting.

The large Beckman and Numitron displays are the most visible, being easily readable at distances of 10 feet or more even in high ambient light conditions. Beckman displays require high voltage and are, therefore, generally used in AC line-powered DPM's. The Numitron display works well with logic-powered DPM's, and their "white" light output allows filtering for color coded displays.

## Light-Emitting Diode (0.27" high)



## Producing Digital Outputs

Since the data display is decimal, DPM's use binary-coded decimal ( 8421 BCD ) counters in the conversion circuitry. For display simplicity, the data outputs are usually available in parallel, that is all BCD data bits are available simultaneously on separate lines. Although serial data makes wiring simpler (you need $13+$ lines for $31 / 2$ digits BCD parallel, versus 2 lines for BCD serial), decoding of the data must be done at the receiving end of the serial line, increasing circuit complexity. If serial data is desired, Analog Devices' new serial control modules (see SERDEX section) can provide for conversion to serial data as well as providing interfaces to teletypes and other data terminals.
Parallel data outputs can be unlatched, latched, or buffered. Unlatched outputs are taken directly from the counter in the converter circuit, and erroneous data will be present on the data lines during conversion. Unlatched outputs simplify circuitry and are perfectly adequate if proper care is taken in interfacing these outputs.
Latched outputs accept the data from the converter section and hold the data for display and processing during the next conversion. At the end of each conversion, the data being held in the latches are updated. Latched outputs simplify processing since the data are available during relatively long time periods and no noise is present on the data lines during conversion.
Buffered outputs are similar to latched outputs except the output data is gated onto the data lines by an external "STROBE" signal. Buffered outputs make multiplexing of digital data easier, since many devices can share common data lines and each can be gated onto the lines sequentially. However, buffered outputs require gates for each data output line to allow strobing data, requiring, for example $17+$ AND gates for a $41 / 2$ digit DPM. The added circuit complexity and cost can rarely be justified for a DPM, and is not often used.
Output data and control inputs are commonly DTL/TTL compatible since DTL/TTL is the most widely used digital logic. The AD2008 and many future DPMs will provide CMOS and PMOS compatibility.

## Powering the DPM

Line Power or Logic Power? Analog Devices pioneered the design of +5 VDC logic-powered digital panel meters. By operating the DPM from the +5 V power supply commonly available in today's instrumentation, the size, weight, and cost of the meter can be greatly reduced, and the DPM can operate in a cooler environment. In addition, DPM's using line power often require

Numitron (0.40" high)
shielding of the low level inputs from AC power lines. Even operational testing is safer, since no AC line voltage is present on the panel.
However, 5 VDC powered DPM's may draw 0.5 to 1.5 A current from the instrument power supply. In addition, the current required by the display can vary by a factor of 3 in extreme cases (all 1's to all 8 's) requiring a power supply with good transient regulation. If sufficient +5 VDC power is not available or power supply regulation cannot prevent interactions with other system logic, an AC line powered DPM will provide easier integration into the measurement system. •

## A Word About Reliability and Quality

A highly competitive market has brought about greatly reduced DPM prices leading to their widespread usage in scientific and medical instrumentation, industrial control equipment, environmental systems, and aerospace and military systems which require extremely high reliability. A DPM must, therefore, be designed for low cost but not at the expense of reliability.
Designing a unit for high reliability and competitive cost requires devising simple circuits with a low parts count and making extensive use of high-reliability integrated circuits. Analog Devices uses high-volume buying and manufacturing techniques as well as utilizing in-house components to further lower cost without sacrificing quality and reliability.
Good quality assurance includes incoming inspection of components and selection and grading of components in a controlled environment. Continuous visual and electrical inspections and tests are conducted during production. Final testing and calibration are followed by a 7 day burn-in period to insure that all DPM's meet our exacting requirements for performance and reliability.


## WHICH METER FOR THE APPLICATION - DIGITAL

 OR ANALOG?With the new low costs for DPM's, it is reasonable to consider DPM's for new instrument designs which previously used analog displays. Described below are several benefits to be gained by selecting a DPM for the design.
First the digital display is completely free of ambiguity or interpolation errors. Even the most unskilled personnel can accurately read the large digital display. Secondly, it is not necessary for the operator to be close to or directly in front of the meter, thereby avoiding parallax errors. DPM's can be easily read at distances of 10-30 feet or more as well as over wide viewing angles.
The high resolution and large dynamic signal range of a DPM is also important. An analog meter will require considerable range switching to equal the performance of a $31 / 2$ or $41 / 2$ digit DPM. The resolution of a DPM can conveniently extend the useable range of measurements and accuracy of instruments formerly limited by the resolution of analog meters.
The all solid state input circuitry of a DPM also provides several other distinct advantages. Because the DPM uses solid state input circuitry and feedback techniques, high input impedances (above 100 Megohms) are easily achieved and source loading errors are thereby avoided. Input bias currents are typically below 100 nanoamps. However, it is not uncommon for a high accuracy analog meter to draw $0.1-1 \mathrm{~mA}$ of source current at full scale. At this level, unless a low impedance signal source is available, source loading errors can become significant and a high input impedance op amp may be required to reduce loading errors. The complexity of the meter installation increases significantly, thereby defeating the analog meter's asset of application simplicity.
The DPM's fast conversion rate and its ability to be externally triggered makes multiplexing of several inputs to one meter an easy task. Interfacing the BCD data outputs to a line printer can eliminate the need for any manual data logging. These outputs may also be used as parts of a digital loop for sensing signal levels and controlling instrumentation digitally.
The physical size of the DPM is now an advantage. A $0.5 \%(21 / 2$ digit) DPM requires only a $3^{\prime \prime} \times 2$ " panel space; a d'Arsonval meter of equivalent resolution requires a scale length of about $7^{\prime \prime}$ and about $7^{\prime \prime} \times 6^{\prime \prime}$ of front panel space. The all solid state DPM circuitry makes for a very rugged component, thus modernday requirements for small size, light weight, ruggedness and portability often dictate the ase of a DPM.

## Are Digital Meters Always the Best Choice? Other Considerations

One cannot draw the conclusion that DPM's are always a better choice than analog meters. The lowest cost DPM's are still in the $\$ 50$ price range and many applications require low cost, low resolution meters out of the DPM range. And in many applications, an experienced operator can derive much useful information from the "acceleration" and fluctuations of the pointer of an analog meter. Anticipatory adjustment and control often hinges on estimating rate and acceleration, making an analog display mandatory in such circumstances.
The electronic nature of the DPM can also negate its usefulness in some applications. The IC circuits require a separate power supply ( +5 VDC or AC Line) which may not be easily available in the instrument design. Installing an analog meter in a circuit is relatively easy, whereas the possible circuit interactions of a DPM (such as ground loops and digital noise) require more careful circuit design.

## SELECTION OF A DPM

To select the proper DPM, one must review the design requirements of the application. This review should include a characterization of the input signal: its range, polarity, resolution, and accuracy required, whether any common mode voltage is present, and if noise pickup may be a problem. Maximum viewing distance and viewing angle may dictate the type of visual display required. Is +5 VDC logic power available or is a linepowered unit necessary? Are data outputs required for data logging or feedback control?

Once the required specifications of the application have been identified, they must be compared to the specifications provided by the DPM manufacturers. Since no industry standards for DPM specifications exist, it is very important to understand how a manufacturer defines his particular specifications. The checklist below can be used as a guide to the proper selection of a DPM.

## Selection Checklist

WHAT PERFORMANCE IS DESIRED? What resolution and accuracy are required? These specifications will determine the number of display digits and the level of accuracy need. A $21 / 2$ digit meter can be used to replace most analog meters, a $31 / 2$ digit DPM is usually adequate for general purpose applications, and a $41 / 2$ digit DPM provides high resolution capability.
WHAT INPUTS ARE TO BE MEASURED? The designer must know the range of voltages to be measured, bipolar or unipolar, the source impedance, what common mode voltage must be accommodated (if any), and if ratiometric measurements must be made with respect to external reference voltages.
ARE ENVIRONMENTAL CONDITIONS HARSH? If the DPM is to be used in a noisy electrical environment, good CMR and NMR are necessary. A large range of operating temperatures requires a good temperature coefficient.

## WHAT INPUT POWER IS AVAILABLE? Will the DPM

 share the +5 VDC power supply used for other logic circuitry or will a separate +5 VDC power supply be needed? Are there limitations on power drain? Is only AC line power available? Is signal and power line ground isolation necessary?WHAT DISPLAY TYPE IS DESIRED? Must the display be large enough to be read from a long distance? Is color coding necessary? Is ruggedness a factor? Is ambient light level high?
IS PACKAGE SIZE CRITICAL? Is there any restriction on the size of the DPM, either in panel space or depth? Is internal heat rise critical, as in small portable instrument designs?

ARE DATA OUTPUTS NECESSARY? If automatic data logging is desired or if external feedback control, via a data link, is part of the design, then BCD digital data outputs from the DPM must be available for interfacing to other system circuitry. Are latched outputs needed? Are the proper logic levels available? Is conversion speed adequate for the system? Is logic ground isolation required?

## Understanding Performance Specifications

Currently, there are no industry standards on DPM specifications, and comparing specifications of DPM's from different manufacturers may require some analysis. A section of DPM specification definitions has been included, but an elaboration on several of these is included below to help in understanding fully how specifications relate to performance requirements.
Resolution, Accuracy, and Stability -- these three specs are very important in the selection of a DPM. Although more digits may mean more resolution, the digits themselves are useless unless the accuracy is sufficient for the digits to have real meaning. Therefore, accuracy and resolution should be comparable.
Independent of temperature, there are three components which lead to DPM inaccuracies. They are zero offset error, gain error, and digital indecision. In any device using a counter and clock to determine a digital output, there is always a potential $\pm 1$ count error in the output. This is caused by the timing of the input gate of the counter; when the gate closes asynchronously with the clock, a clock pulse that occurs just as the gate closes may or may not be counted, hence the fixed $\pm 1$ digit inaccuracy.

Zero level offsets in the analog circuitry cause errors specified as a percentage of full scale reading. These errors can be corrected by a zero calibration potentiometer requiring periodic resetting, or by internal calibration circuits that set the zero level automatically between each reading, assuring no zero level contribution to the error.
Gain variations occur as a function of signal level in the analog circuitry and produce errors which are specified as a percentage of the reading. These are the hardest errors to design out of a DPM circuit, but they can be minimized by component specification and selection. A range potentiometer is used for periodic adjustment of the gain.

Since all the electronic components used in the design of a DPM have some temperature dependence, one can expect the accuracy of the DPM to be affected by changes in operating temperature. If automatic zero correction circuitry is not used, the zero level may drift with temperature. Variations in the reference voltage circuitry and its associated switches will cause changes in the gain of the DPM, but careful selection and matching of components can minimize this error.

Operational amplifiers used on DPM inputs typically use FET inputs which double their bias current for every $+10^{\circ} \mathrm{C}$ rise in temperature. Many Analog Devices' DPM's use linear IC op amps with superbeta transistor inputs to reduce the bias currents and provide greater bias current stability. By providing a more stable input bias current, one can reduce loading errors.
To illustrate these specifications, consider a $31 / 2$ digit DPM (1999 counts full scale). The resolution of the unit is the value of one digit, 1 part in 2000 or $0.05 \%$ of full scale. If the accuracy is comparable to the resolution (exclusive of digital indecision), the DPM should have a maximum error of $\pm 0.05 \%$ $\pm 1$ digit.
Temperature coefficient specifications for a DPM should be very good to maintain the accuracy. A tempco of only $50 \mathrm{ppm} /{ }^{\circ} \mathrm{C}\left(0.005 \% /^{\circ} \mathrm{C}\right)$ will produce an additional error of $\pm 0.05 \%$ over a range of only $\pm 10^{\circ} \mathrm{C}$.

Since each manufacturer tends to use a different method of specifying accuracy and temperature coefficients, specifications must be expressed in common terms to be comparable. For example, one may find specifications for $31 / 2$ digit DPM's in the formats shown below.

Unit 1: max error: $\pm 0.05 \% \mathrm{R} \pm 1$ digit, tempco: $\pm 50 \mathrm{ppm}(\mathrm{R}) /{ }^{\circ} \mathrm{C}$
Unit 2: max error: $\pm 0.02 \% \mathrm{R} \pm 0.03 \%$ F.S. $\pm 1$ digit, tempco: $\pm 0.004 \% \mathrm{R} \pm 0.001 \%$ F.S. $/{ }^{\circ} \mathrm{C}$
Unit 3: max error: $\pm 0.05 \% \mathrm{R} \pm 0.05 \%$ F.S. $\pm 1$ digit, for temperature $+15^{\circ} \mathrm{C}$ to $+35^{\circ} \mathrm{C}$

To compare the three units, one must establish a common ground : full scale reading, temp range $+15^{\circ} \mathrm{C}$ to $+35^{\circ} \mathrm{C}$ $\left( \pm 10^{\circ} \mathrm{C}\right)$. The specification then becomes:

$$
\begin{aligned}
\text { Unit 1: } & \pm 0.05 \% \text { F.S. } \pm 1 \operatorname{digit} \pm\left(50 \mathrm{ppm}(\mathrm{~F} . S .) /{ }^{\circ} \mathrm{C} x \pm 10^{\circ} \mathrm{C}\right) \\
& = \pm 0.05 \% \text { F.S. } \pm 1 \text { digit } \pm 0.05 \% \text { F.S. } \\
& =0.1 \% \text { F.S. } \pm 1 \text { digit } \\
\text { Unit } 2 & \pm(0.02 \% \text { F.S. } \pm 0.03 \% \text { F.S. }) \pm 1 \text { digit }(0.004 \% \text { F.S. } \\
& \pm 0.001 \% \text { F.S. }))^{\circ} \mathrm{C} x \pm 10^{\circ} \mathrm{C} \\
& =0.05 \% \text { F.S. } \pm 1 \text { digit } \pm 0.05 \% \text { F.S. } \\
& =0.1 \% \text { F.S. } \pm 1 \text { digit } \\
\text { Unit 3: } & \pm 0.05 \% \text { F.S. } \pm 0.05 \% \text { F.S: } \pm 1 \text { digit } \\
& =0.1 \% \text { F.S. } \pm 1 \text { digit }
\end{aligned}
$$

Even though all units are specified differently, they have equivalent performance.

## APPLICATIONS OF DPM'S

The ability of the DPM to provide accurate measurements over a wide range of voltage inputs has led to its widespread usage in instrumentation for medical, scientific, and industrial applications, as well as test instrumentation. When digital data outputs are provided, the DPM becomes a useful data acquisition element, providing data logging and feedback control as well as a visual output. Since the DPM input is easily scaled using attenuation or amplification, the DPM can be scaled to read directly in any engineering or physical units.

## Typical Applications for DPM's Include:

- Medical, Analytical, and Scientific Instrumentation

| Measuring: | Temperature | Reflectance \& Transmittance |
| ---: | :--- | ---: |
| Pressure | pH |  |
|  | Power | Size |
|  | Color Difference | Cardiac \& Pulmonary Functions |

- Systems Applications providing digital readout, automatic data logging, and digital feedback control


## - Precision Differential Measurement

Described below are several applications illustrating the versatility and simplicity of DPM's for a wide variety of applications.

DIGITAL INDICATING MICROMETER: Linear variable differential transformers (LVDT) produce a DC output voltage proportional to the magnitude of a linear displacement. A typical LVDT may have a range of $\pm 1$ " and a maximum linearity error of $\pm 0.001^{\prime \prime}$. The typical output voltage varies $2 \mathrm{mV} / 0.001^{\prime \prime}$ ( $2 \mathrm{~V} /$ inch). By using a $31 / 2$ digit ( 199.9 mV range) DPM such as the AD2003 and attenuating the LVDT output with a $20: 1$ voltage divider, the DPM will read directly in $0.001^{\prime \prime}$ increments over the full range of the LVDT. The proper decimal point can be activated to provide direct readings in inches.

DIGITAL WEIGHING PLATFORM SCALE: Platform transducers can be used to measure loads up to 1000 pounds. These transducers are strain gauge bridge units, typically producing 15 mV at full scale loads with 10 V excitation. By using an operational amplifier providing a gain of $6.67,1000$ pound load will produce a voltage of 100 mV , measurable by a $31 / 2$ digit DPM (AD2003, AD2010). The readout will be directly in pounds.


Digital Scale

## RATIOMETRIC MEASUREMENTS

Ratiometric operation allows readings to be normalized to an external reference. This is useful where the analog voltage to be measured is accurate relative to an external reference which in itself is not accurate. Ratiometric applications are shown below. For potentiometric transducers, a single-ended input DPM such as the AD2010/R is sufficient. On bridge transducers, a differential input is essential; single-ended inputs can be buffered with a differential instrumentation amplifier or a differential input DPM with ratiometric operation such as the AD2006 can be used as shown. In either application the output will be normalized to compensate for variations in the reference voltage and the accuracy will be retained.


Ratiometric Measurement with a Potentiometric Transducer


Digital Micrometer


Bridge Transducer Measurements Using AD2006

CIRCUIT APPLICATION GUIDELINES FOR DPM's The successful application of DPM's in an instrument design hinges on understanding the specifications and the interactions of the DPM with the rest of the instrument circuit. The following information will facilitate the application of the DPM.

Ground Loops: Correct grounding of a single-ended input, +5 VDC powered DPM within the instrumentation system is essential for accurate readings. Since heavy supply currents ( $\sim 1 \mathrm{~A}$ ) flow through the power ground, under no circumstance should the input voltage be applied between the analog input and power ground. The voltage drop across even the few milliohms of contact resistance can produce erratic and variable offsets in the readings. Connections to power supplies should also be checked to insure that multiple ground connections are not causing ground loops. If shorting the inputs does not produce a zero reading, ground loops are most certainly present.

$\beta_{c}=$ CONNECTOR CONTACT RESISTANCE


Right \& Wrong Input Connections
Power Supplies: Besides ground loops, +5 VDC power supplies can also affect DPM readings if there is noise present on the power lines. If large noise spikes or large voltage variations are present, better filtering or regulation of the power supply may be necessary.


Power Supply Connections to Prevent Ground Loops
AC Line Power: Noise on power lines can also affect AC powered DPM's. Signal input should be physically separated from the AC power lines to prevent noise pickup. A noisy AC line may require filtering to prevent interference with DPM operation.
Digital Noise: Insure that all digital control lines (e.g., hold and trigger) connected to the DPM have a minimum of noise pickup. Noise on these lines can cause false triggering, prevent proper triggering, or affect the analog circuitry.

If necessary, use coaxial cable for data lines to prevent noise pickup or connect the control lines to proper logic levels through a $1 \mathrm{k} \Omega$ series resistor to prevent false triggering (e.g., if the "Hold" should be at logic " 1 " for normal operation, connect the "Hold" input to +5 V through a $1 \mathrm{k} \Omega$ resistor).
Attenuators: If an attenuator is used to scale the input signal to the DPM or to calibrate the readout in engineering or physical units, the attenuator network should be located as close as possible to the input terminals of the DPM. This avoids processing the attenuated signal over long lines, thereby reducing potential noise susceptibility.


$$
\text { Attenuation Network, Attenuation }=\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}+\mathrm{R}_{2}}
$$

Resistors used in attenuator networks should be chosen for temperature coefficients at least twice as good as the DPM to avoid any additional temperature effects. In addition, keeping the source loading of the DPM below $10 \mathrm{k} \Omega$ will minimize the effects of bias current changes due to temperature.

The attenuator network shown below can be used with differential input DPM's to extend the common mode voltage by a factor equal to the attenuation. Care must be taken to match the resistor networks exactly for proper operation.


Differential Attenuator, $\mathrm{R}_{\mathbf{1}}=\mathrm{R}_{\mathbf{3}}, \mathrm{R}_{\mathbf{2}}=\mathrm{R}_{\mathbf{4}}$,

$$
\text { Attenuation }=\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}+\mathrm{R}_{2}}
$$

Measuring Current: A shunt resistor can be placed across the input of the DPM for current measurement. Since few current measurements are made with respect to ground, a differential or floating input DPM will facilitate application. Shunt resistors should be chosen for their temperature coefficients to insure accuracy over variations in operating temperature, and the resistors should be of sufficient wattage rating to prevent excessive heating. For large currents, four terminal meter shunts can be used.

Temperature Operating Range and Thermal Effects: DPM's can measure voltages with resolution as fine as $100 \mu \mathrm{~V}$, requiring consideration to be given to operating temperature. Input bias currents may change by several nA over the operating temperature range, but the effect on measurement can be minimized by keeping source impedance low ( 1 nA through $10 \mathrm{k} \Omega$ produces only a $10 \mu \mathrm{~V}$ drop, $<0.1$ digit). Dissimilar metallic junctions in the wiring can produce thermocouple-type effects of up to $50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$; especially be wary of electromechanical relays. Calibration of the DPM in the measurement system should be done only after the system is fully warmed up and at a stable operating temperature.

Common-Mode Interference: Stray pickup, input circuit impedance, line resistance, and shunt capacitance, if sufficiently unbalanced, can introduce common-mode errors even if the DPM has infinite CMR. Capacitance unbalance should be kept to a minimum; if needed, it can be further reduced by placing a shunt capacitor between the inputs at the meter.
More information on application of digital measuring devices to instrumentation systems can be found in Analog Devices' Analog-Digital Conversion Handbook.

## DEFINITIONS—DPM TERMS AND SPECIFICATIONS

Accuracy (absolute): DPM's are calibrated with respect to a reference voltage which is in turn calibrated to a recognized voltage standard. The absolute accuracy error of the DPM is the tolerance of the full-scale set point referred to the absolute voltage standard.
Accuracy (relative): Relative accuracy error is the difference between the nominal and actual ratios to full scale of the digital output corresponding to a given analog input. See also: linearity.
Automatic Zero: To achieve zero stability, a time interval during each conversion is provided to allow the circuitry to compensate for drift errors, thereby, providing virtually no zero drift error.
Bias Current: The current required from the source at zero signal input by the input circuit of the DPM. Bias current is normally specified at typical and maximum values. Analog Devices' DPM's using transistor input circuitry are bias current sinks.

Binary Coded Decimal (BCD): Data coding where each decimal digit is represented by a group of 4 binary coded digits (called "quads"). Each quad has bits corresponding to $8,4,2,1$ and 10 permissible levels with weights $0-9$. BCD is normally used where a decimal display is needed.
Common-Mode Rejection: A differential-input DPM will reject any input signals present at both input terminals simultaneously if they are within the common mode voltage range. Common mode rejection is expressed as a ratio and usually given in dB. $(\mathrm{CMR}=20 \log \mathrm{CMRR}) .120 \mathrm{~dB}$ of common-mode rejection (CMRR $=10^{6}$ ) means that a 10 V common-mode voltage is processed as though it were an additive-differential input signal of $10 \mu \mathrm{~V}$ magnitude.
Common Mode Voltage: A voltage that appears in common at both input terminals of a device, with respect to its ground.
Conversion Rate: The frequency at which readings may be processed by the DPM. Specifications are typically given for internally clocked rates and maximum permissible externallytriggered rates.
Conversion Time: The maximum time required for a DPM to complete a reading cycle, specified for the full scale reading.
Dual-Slope Conversion: An integrating A/D conversion technique in which the unknown signal is converted to a proportional time interval, which is then measured digitally. This is done by integrating the unknown for a predetermined time. Then a reference input is switched to the integrator, and integrates "down" from the level determined by the unknown, until a "zero" level is reached. The time for the second integration process is proportional to the average of the unknown signal level over the predetermined integrating period.


Input Impedance: The complex ratio of signal voltage to signal current at the input terminals. For DPM's, the input impedanc is measured at DC.

Linearity: The conventional definition for nonlinearity of a DPM is the deviation from a "best" straight line which has been fitted to a calibration curve. Analog Devices, defines nonlinearity as the deviation from a straight line drawn between the zero and full scale end points. Not only is this an easier method for customer calibration, it is also a more conservative method of specifying nonlinearity.


Normal Mode Rejection: Filtering or integrating the input signal improves noise rejection of undesired signals present at the analog high input. Normal mode rejection is expressed as the ratio of the actual value of the undesired signal to its measured value over a specified frequency range. (NMR (dB) $=20 \log$ NMRR, e.g. NMR $=40 \mathrm{~dB}$ means an attenuation of $100: 1$ ).
Overload: An input voltage exceeding the full scale range of the DPM produces an overload condition. An overload conditic
is usually indicated by conspicuous manipulation of the display such as all dashes, flashing zeros, etc. On a $31 / 2$ digit DPM with a range of $199.9 \mathrm{mV}, \mathrm{a} \geqslant 200 \mathrm{mV}$ signal will produce an overload condition.

Overrange: An input signal that exceeds full scale on a DPM, but is less than an overload. On a $31 / 2$ digit DPM with a full scale range of 199.9 mV , full scale is $0-99.9 \mathrm{mV}$, and signals from $100-199.9 \mathrm{mV}$ are said to fall in the $100 \%$ overrange region. Some DPM's have higher overrange capability. A $33 / 4$ digit DPM has a full scale range of 3.999 or $300 \%$ overrange.
Overvoltage Protection: The input section of the DPM must provide protection from large overloads. Specifications are given for sustained DC voltages that can be tolerated.
Range (Temperature Operating): The range of temperatures over which the DPM will meet or exceed its performance specifications.
Range (Full Scale): The range of input signals that can be measured by a DPM before reaching an overload condition. A $31 / 2$ digit DPM provides three digits full scale and 100 percent overrange capability.

Ratiometric: Dual Slope DPM's compare voltage inputs to a stable internal reference voltage. In some systems, the voltage being measured is a function of another voltage, and accurate measurements should be made as the ratio of the two voltages. Some DPM's provide inputs for external reference voltages for ratiometric measurements.
Resolution: The smallest voltage increment that can be measured by a DPM. It is a function of the full scale range and number of digits of a DPM. For example, if a $31 / 2$ digit DPM has a resolution of 1 part in $2000(0.05 \%)$ over a full scale range of 199.9 mV , the DPM can resolve 0.1 mV .

| Digits | Counts (F.S.) | Resolution (\% F.S.) |
| :---: | :--- | :---: |
| $21 / 2$ | 199 | $0.5 \%$ |
| 3 | 999 | $0.1 \%$ |
| $31 / 2$ | 1999 | $0.05 \%$ |
| $33 / 4$ | 3999 | $0.025 \%$ |
| 4 | 9999 | $0.01 \%$ |
| $41 / 2$ | 19999 | $0.005 \%$ |
| $43 / 4$ | 39999 | $0.0025 \%$ |

Staircase Conversion: A simple analog-to-digital conversion technique in which a clock and counter drives a digital-toanalog converter which produces an output voltage wavefurm resembling a staircase. A comparator stops the counter when the voltage exceeds the input voltage and the content of the counter is the digitized output.


Temperature Coefficient: The additive error term (ppm/ ${ }^{\circ} \mathrm{C}$ or $\%$ Reading $/{ }^{\circ} \mathrm{C}$ ) caused by effects of variations in operating temperature on the electronic characteristics of the DPM. Unipolar Input DPM: A DPM designed to measure input voltages of only one polarity.

## TECHNICAL INNOVATION

In 1972, Analog Devices entered the digital panel meter market with a totally new concept: a DPM that operates from the +5 VDC power supply commonly used for logic circuits. The user and application benefits of this concept have been well proven. In addition, input circuits have been developed that sense and correct offset drift between each reading, providing more accurate DPM performance and longer periods between calibration. The "limited differential" input of the AD2010 provides protection from ground loop problems in a singleended +5 V powered DPM, at a lower cost than true differential inputs. Technical innovation in new products is devoted to providing better performance, easier application and longer life at a reasonable cost.

## AN EXPANDING PRODUCT LINE

Analog Devices' DPM Product Line has expanded from the original AD2001 to include seven models: offering a choice of AC line or +5 VDC power, $21 / 2,31 / 2$, or $41 / 2$ digits, with LED, Numitron or Beckman displays. As one can see from the capsule selection guide, an Analog Devices DPM is available for most every application. Even more DPMs are being planned: DPMs with extended measurement capability, DPMs designed to utilize the very latest technology, and DPMs designed to be more economical for the OEM user.

## COMPACT PACKAGING

Compact package size and simple installation is a feature of all Analog Devices' DPMs. This makes designing an Analog Devices DPM into a product or a system much simpler, since it takes less space on and behind the front panel and does not require extensive mounting hardware. The lens assembly can be ordered without the Analog Devices logo, if desired, and it can be silkscreened or hot-stamped with measurement units, company logo or other information. The snap-in case design used on all our DPMs except the AD2001 and AD2008 was awarded an "Excellence of Design" award from Industrial Design Magazine in their 1972 Design Review Competition. The design was selected for its functional simplicity, flexibility and overall aesthetic appeal.

## QUALITY ASSURANCE

From design to shipment, Analog Devices works hard at quality control. Each DPM shipped by Analog Devices has received a full seven-day failure-free burn-in. Quality control inspections throughout the manufacturing process insure good workmanship. All DPMs are built from components bought from selected vendors who meet our quality standards, and they have been fully tested for reliability in typical operating environments.

## FULL SUPPORT FOR THE OEM USER

Analog Devices has anticipated the needs of the OEM user of DPMs. Besides offering attractive large quantity price discounts, Analog Devices stands behind its customers with world-wide sales and service facilities. Application assistance and technical information are available when needed, to aid in the selection of the most economical DPM for each application. Analog Devices' quality assurance programs keep field failures to a minimum and repair departments offer fast turnaround times when needed.


CAPSULE SELECTION GUIDE DIGITAL PANEL METERS

| Model |  | AD2001 | AD2002 | AD2003 | AD2004 | AD2006 | AD2008 | AD2010 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Resolution (digits) and Range | $2^{1 / 2}$ |  | - |  |  |  |  |  |
|  | $31 / 2$ | - |  | - |  | - |  | - |
|  | 41/2 |  |  |  | - |  | - |  |
| Input Type | Single-Ended | - | - |  |  |  |  | $\bullet$ |
|  | Differential |  |  | - | - | - |  | , |
|  | Floating |  |  |  | - |  | - |  |
|  | Unipolar |  | - |  |  |  |  |  |
|  | Bipolar | - |  | - | - | - | - | - |
| Display | Numitron | - | - | - |  |  |  |  |
|  | LED |  |  |  | - |  |  | - |
|  | Beckman |  |  |  |  | $\bigcirc$ | - |  |
| Data Outputs | Parallel BCD | - | ${ }^{1}$ |  |  | $\bigcirc$ |  |  |
|  | Parallel BCD, Latched |  |  | - | - |  | ${ }^{3}$ | - |
| Power | +5VDC | - | - | - | - | ${ }^{2}$ |  | - |
|  | AC Line |  |  |  |  | - | - |  |
| Connector | PC Card | - |  | ${ }^{2}$ |  | ${ }^{2}$ | - | - |
|  | Multipin |  | - | - | - | - |  |  |
| Applications | Low Cost Analog |  |  |  |  |  |  |  |
|  | Replacement |  | - |  |  |  |  | - |
|  | General Purpose | - |  | - |  | - |  | $\bigcirc$ |
|  | Instrumentation Amp Input |  |  | - |  | - | - |  |
|  | High Noise Immunity |  |  | - | - | - | $\bigcirc$ | - |
|  | Off Ground Measurements |  |  |  | - | - | $\bigcirc$ |  |
|  | Ratiometric Measurements |  |  |  |  | - | - | - |
|  | High Visibility Display ( $>8-10^{\prime}$ \& high ambient light) | - | - | - |  | $\bullet$ | - |  |
|  | Extremely Rugged Display |  |  |  | - |  |  | - |

[^13]
## AD2001

# 31/2 Digit DPM For OEM Applications 

## FEATURES

- Low Cost
- Small Size: $1.8^{\prime \prime} \mathrm{H} \times 3.1^{\prime \prime} \mathrm{W} \times 1.5^{\prime \prime} \mathrm{D}$
- +5 VDC Powered
- Maximum Error: $0.05 \% \pm 1$ Digit
- Bright Sharp Display
- High Reliability


## GENERAL DESCRIPTION

The AD2001 is a $31 / 2$ digit panel meter designed for original equipment requiring high performance at a low price. The maximum error of the AD2001 is $0.05 \%$ of reading $\pm 1$ digit with a temperature coefficient of $\pm 50 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$. An unusual A/D converter approach-ANALOK ${ }^{T M}$-yields a minimum component and high accuracy design. ANALOK ${ }^{\text {TM }}$ allows the unit to operate from a single 5VDC power source and is the key to the AD2001's small size and low cost.

## DISPLAY FEATURES

The AD2001 display uses incandescent RCA Numitron display tubes which provide a bright, sharp, easily readable display over a wide range of ambient light. Other standard features of the display are: automatic polarity, programmable decimal points, automatic zero, full scale $\pm 199.9 \mathrm{mV}$ and automatic overload indication. The display rate is 5 readings per second, up to 20 conversions are possible under external control.

## DESIGN EFFICIENCY FOR THE OEM

The AD2001 is not only a nearly direct replacement for the most common size of panel meters (whose errors specifications are usually of the $1-2 \%$ class), but it is considerably smaller than the $51 / 2^{\prime \prime}$ to $71 / 2^{\prime \prime}$ width typical of the most accurate and expensive analog meters.
The front bezel design of the AD2001 allows easy installation and removal, and its light weight allows the unit to be used in hinged panel equipment. The complete unit is housed in an aluminum case which provides structural strength, optimum heat dissipation, and shielding from external noise. Overvoltage protection is also provided.
The AD2001 logic levels are compatible with DTL \& TTL integrated circuits. The AD2001 can operate from the user's 5VDC system supply-eliminating the shielding, decoupling, etc. normally needed when the AC line must be routed near signal leads. Separate DC inputs to the converter and display, allow

the designer to minimize effects of display transients on conversion accuracy, economize regulated power and, by use of an external circuit, to blank the display.

## DATA PROCESSING EQUIPMENT INTERFACING

The AD2001 provides an excellent economy digital panel meter for display purposes. The ANALOKTM circuit also provides BCD outputs, polarity sign, overrange, and overload signals which can be used under restricted conditions for data processing equipment interfacing.

The logic "one" on the overload output line can be generated by either an actual "overload" ( $>199.9 \mathrm{mV}$ ) at the input or an input polarity change. It is recommended that in data processing interface applications the data logger or computer equipment be programmed to ignore the BCD output data whenever the logic " 1 " appears on the overload line.


AD2001 Simplified Block Diagram

## CONNECTOR RECOMMENDATION

- 30 Pin 0.156 spacing Viking No. 2 Vk 15D/1-2
- Optional - specify AC 1501


# Low Cost $21 / 2$ Digit DPM For Analog Meter Replacement 

## FEATURES

- Low Cost
- Small Size: $1.8^{\prime \prime} \mathrm{H} \times 3^{\prime \prime} \mathrm{W} \times 1.5^{\prime \prime} \mathrm{D}$
- +5 VDC Powered
- High Reliability
- $0.5 \% \pm 1$ Digit Maximum Error
- Bright, Sharp Display
- Fast Conversion Time
- Optional BCD Data Outputs


## GENERAL DESCRIPTION

Analog Devices' AD2002 is a $21 / 2$ digit Digital Panel Meter offering high performance at a low price. It is a 5 VDC powered DPM designed as a minimum-cost replacement for analog meters used in OEM equipment requiring accuracy to $0.5 \%$. Economy and reliability of the AD2002 are achieved through the use of a "staircase" conversion technique and the resulting lower component count.
Other features of the AD2002 include: $0.5 \% \pm 1$ digit maximum error; data processing system interface capability (optional); 7 segment filament test; and a ruggedly designed $1.8^{\prime \prime} \mathrm{H}$ $\times 3^{\prime \prime} \mathrm{W} \times 1.5^{\prime \prime} \mathrm{D}$ aluminum case. The unit provides highly accurate and stable readings of unipolar, single-ended input signals over a full scale range of 0 to +1.99 V with automatic overload indication. Readings can be held indefinitely upon command. The temperature coefficient is $1 / 20 \mathrm{digit} /{ }^{\circ} \mathrm{C}$. Prior to shipment, all AD2002 units are burned in for a seven day period to assure high reliability.
Typical applications for the AD2002 include: scientific, industrial, and medical instrument designs; measurement, control, and data acquisition systems.

## BRIGHT, SHARP DISPLAY

The AD2002 utilizes green filtered RCA Numitron tubes. The green filter provides optimum matching with the optical response of the human eye. The result is a bright, sharp and highly readable display over a wide range of ambient light without operator fatigue. This precise digital display offers the added advantage over analog meters of totally unambiguous readings.
Standard features of the display are: programmable decimal points; 7 segment filament test; 4 readings/sec display rate with an optional trigger and hold feature for up to 200 readings/sec.


## SMALL BUT RUGGED

The compact size of the AD2002 allows it to be easily substituted for conventional analog meters, in many cases requiring even less space than the analog meter. It is housed in an aluminum case providing light weight, structural strength, optimum heat dissipation, and shielding against external noise. The case, which easily snaps into the panel from the front, offers a clean modern look. Its light weight is ideal for installation in hinged panel equipment.


## AD2002 Simplified Block Diagram

## MODES OF OPERATION

To use the panel meter for visual readout as a conventional measuring component, only 5 connections, are required. For use in data processing equipment, connections for BCD outputs, "status" signal, overrange, overload signals, and external read and hold features are available with the low cost DP option.

## ORDERING GUIDE

AD2002 - Standard 2 $1 / 2$ digit DPM without DP option
AD2002/DP - Standard 21/2 digit DPM with DP option (BCD data and control signals)
Connector for use with AD2002 - None Required Connector for use with AD2002/DP (optional) -

AC5002 3M mating connector part No. 3399-1000
AC5003 6 feet of decade color coded wire mated with the above 3M connector part No. 3399-1000

## FEATURES

- +5VDC Powered
- True Differential Input
- High Common Mode Rejection: 80 dB Minimum at $\pm 2.5 \mathrm{~V}$
- Excellent Data Processing Interfacing
- $0.05 \% \pm 1$ Digit Maximum Error
- Bright, Sharp Display
- Green, Filtered Display
- Small Size: $1.8^{\prime \prime} \mathrm{H} \times 3^{\prime \prime} \mathrm{W} \times 2^{\prime \prime} \mathrm{D}$
- Tool Free Insertion and Removal
- Low Price


## GENERAL DESCRIPTION

Analog Devices' AD2003 is a $31 / 2$ digit Digital Panel Meter offering high performance and versatility at a low price. The 5VDC powered AD2003 has a differential instrumentation amplifier input, high common mode rejection -80dB minimum at $\pm 2.5 \mathrm{~V}$ and better than 40 dB of normal mode rejection.

Other standard features of the AD2003 include $0.05 \% \pm 1$ digit maximum error, $\pm 50 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ temperature coefficient, data processing interface capability with fully latched data outputs, 7 segment filament test and a ruggedly designed $1.8^{\prime \prime} \mathrm{H} \times 3^{\prime \prime} \mathrm{W}$ $x 2^{\prime \prime} \mathrm{D}$ aluminum case. The AD2003 provides highly accurate and stable readings of bipolar, differential input signals over a full scale range of 0 to $\pm 199.9 \mathrm{mV}$ with automatic overload and polarity indication. Readings can be held indefinitely upon command. Prior to shipment all AD2003 are burned in for a seven day period to assure high reliability.
Typical applications for the AD2003 include': scientific, industrial, and medical instrument designs; measurement, control, and data acquisition systems.
BRIGHT, SHARP DISPLAY
The AD2003 utilizes green filtered RCA Numitron tubes. The green filter provides optimum matching with the optical response of the human eye. The result is a bright, sharp and highly readable display over a wide range of ambient light without operator fatigue. The clean modern look of the lens and case design further enhance the visual attractiveness of the display. This precise digital display offers the added advantage over analog meters of totally unambiguous readings.
Standard features of the display are: programmable decimal points: 7 segment, polarity sign and decimal point

filament test; automatic zero; 5 readings/second with external trigger-and-hold feature to allow display rates of up to 16 readings/second.

## SYSTEMS INTERFACING

The excellent drift, linearity, and noise rejection capability of the AD2003 makes it a natural choice for extracting and displaying low level signals in the presence of high common mode noise voltages. The AD2003 is an excellent DPM for use with transducers such as thermocouples, strain gage bridges, current shunts and biological probes. The latched BCD outputs and 60 ms conversion time also allow the AD2003 to serve as a superior component for data acquisition systems.


## AD2003 Simplified Block Diagram

## EASY TO USE IN NEW DESIGNS

The AD2003 was designed with the equipment of the 70's in mind. Its logic levels are compatible with DTL and TTL integrated circuits. The AD2003 can operate from the user's 5VDC system supply eliminating the shielding, decoupling, etc., needed for line-powered units when the AC line must be
routed near signal leads. Separate DC inputs to the converter and the display allow the OEM designer to minimize effects of display transients on conversion accuracy, economize regulated power, and by use of an external circuit, blank the display independently of the converter.

## APPLICATIONS - REDUCING COMMON MODE INTERFERENCE

The specified minimum common-mode rejection of 80 dB (CMRR $=10,000$ ) means that a 1 V common-mode signal appearing on both input leads will cause an error equivalent to at most 1 digit ( 100 microvolts). A common-mode signal is a dc or ac voltage, which may be related or unrelated to the input signal, appearing on both input leads. It may be caused in a number of ways (in any combination): In a balanced circuit, such as a bridge, receiving excitation from a grounded supply, the output is the difference between two voltages approximately midway between the supply voltage and ground. The average level of the two voltages is the common-mode voltage, $\mathrm{V}_{\mathrm{CM}}=1 / 2\left(\mathrm{~V}_{1}+\mathrm{V}_{2}\right)$. The desired output is the difference voltage $\left(V_{1}-V_{2}\right)$.


## AD2003 Used With Balanced Transducer Bridge Circuit

In a measurement circuit that shares a common "single-ended" system ground, common-mode potentias may be induced thermally, electrically, etc., in series with the ground lead The differential input capability of the AD2003 allows measurements to be made independently of the actual local ground potential (within ratings).


## AD2003 Used With an Unbalanced Source

Stray pickup, input circuit impedance, line resistance, and shunt capacitance, if sufficiently balanced, can introduce common-mode errors, even if the measuring device (the meter) has "infinite" CMR. For this reason, the CMR specification is written in terms of a $1 \mathrm{k} \Omega$ input circuit unbalance and a range of frequencies, dc to 1 kHz , to account for a realistic set of electrical conditions. It is good circuit practice to shield the input leads, with the shield connected in one place only, either at the common-mode level of the source or to a guard potential at a level close to that of the commonmode voltage. Capacitive unbalance should be kept to a minimum. It can be further reduced by shunt capacitance between the inputs at the meter.*

## ORDERING GUIDE

- AD2003 - Standard AD2003 as described above - Tuned for peak normal mode rejection at 60 Hz and its harmonics. 3M multipin connector
- AD2003/E - Standard AD2003 as described above - tuned for peak normal mode rejection at 50 Hz and its harmonics. 3 M multipin connector
- AD2003/C - Standard AD2003 with PC card edge connector.
- AD2003/E/C - Standard AD2003/E with PC card edge connector.


## CONNECTORS

- AC1600 - 3 M connector \#3414. (optional) AC1600-connector and $6^{\prime}(1.83 \mathrm{~m})$ woven cable
- AC1601-connector only
- AD2003/C requires 30 pin, 0.156 spacing, Viking No. 2VK 15D/1-2 or Cinch type 251 No. 5030A30.
- AD2003/C (optional) - Order AC1501
* More information on circuit practice to minimize common-mode errors in data acquisition can be found in the Analog Devices Analog-Digital Conversion Handbook.


## FEATURES

- Floating Optically Isolated Analog Section
- Excellent Common Mode Rejection: 120dB at $\pm 300 \mathrm{~V}$
- High Normal Mode Rejection: 60 dB
- +5VDC Powered
- Automatic Zero with Maximum Error: $0.01 \% \pm 1$ Digit
- LED Display with Latched Digital Outputs
- Small Size: $1.8^{\prime \prime} \mathrm{H} \times 3^{\prime \prime} \mathrm{W} \times 2.5^{\prime \prime} \mathrm{D}$
- Low Price


## GENERAL DESCRIPTION

Analog Devices' model AD2004 represents an advance in price/ performance capabilities of $41 / 2$ digit digital panel meters. The AD2004 offers a $0.01 \% \pm 1$ Digit accuracy, resolution of 0.1 mV , common mode voltage (CMV) of $\pm 300 \mathrm{~V}$ with a common mode rejection ratio (CMRR) of 120 dB .
Using optically coupled isolation techniques for the signal channel, this new design is capable of performing precision measurements of floating differential voltages in noisy environments or under widely varying common mode voltage levels of up to $\pm 300 \mathrm{~V}$. The optically isolated design assures ground loop elimination and permits critical measurement of off ground signals such as those found in the nuclear and process control industries.

The AD2004 features a $41 / 2$ digit light-emitting-diode (LED) display with a full scale range of 0 to $\pm 1.9999$ Volts and latched digital data outputs and control interface signals. Automatic-zero correction circuitry measures and compensates for offset and offset drift errors thereby providing virtually no zero error.
The conversion rate of the AD2004 is normally 4 readings per second. However, an external trigger may be applied to vary the sampling rates from a maximum of 8 readings per second down to an indefinite hold rate. During conversion, the previous reading is held by the latched logic. The numeric readout is available as BCD data. Application of the metering system in a computer or data logging system is made easy with the availability of the "overrange," "polarity," "overload," and "status" signals.
The AD2004 can operate from the users 5VDC system supply, thereby, eliminating the shielding and decoupling needed for line powered units when the AC line must be routed near signal leads.


## TYPICAL APPLICATIONS INCLUDE:

- Ground loop elimination between input transducer and output circuit functions.
- High resolution monitoring of small signals impressed on high off-ground voltages of up to $\pm 300 \mathrm{~V}$.
- Electronic indicating weighing systems for industrial applications. Numerical output may be interfaced with a digital computer or data logging system.
- Digitally controlled industrial process where analog and digital signal isolation is required.
- Balanced strain gage bridge output measurement for industrial requirements.
- Digital indicating micrometer using a linear variable differential transformer (LVDT). Due to the high normal mode rejection ratio of the AD2004, the AC excitation of the LVDT does not induce errors into the system.
- Analytic and Scientific Instrument displays with isolated numeric readout.


## LED's GIVES LONG LIFE, SHARP DISPLAY

The numeric outputs are displayed using $0.27^{\prime \prime}$ high, 7 segment, red LED's. The LED's provide the physical ruggedness typical of IC's, with a life expectancy in excess of 100,000 hours. The displayed numerals are sharp and easily readable at distances of up to 8 feet. The clean uncluttered look of the lens and case design further enhance the visual attractiveness of the display.
Optical features of the display include: a minimum photometric brightness of 200 foot-lamberts, and a 6300 angstrom, wavelength at peak emission (red). Other display features include programmable decimal points, automatic zero, 4 readings per second display rate with trigger and hold feature for externally programmed 0 to 8 readings per second, and flashingzeros overload indication.

## FLOATING DIFFERENTIAL INPUT OFFERS HIGH CMV

## AND CMR

The AD2004, requiring only 5VDC input power, utilizes a fully floating dual-slope, integrating A-to-D converter. The simplified block diagram shown illustrates the isolation technique used to achieve high CMV and CMR. Optical coupling is used for the digital control signals and


Simplified Block Diagram
transformer coupling in the DC to DC converter section to transmit operating power to the floating converter. The use of these techniques provides high quality isolation between the analog input signals and the display and BCD output registers. Troublesome ground loops are eliminated and excellent CMRR of 120 dB over the common mode voltage range of $\pm 300 \mathrm{~V}$ is achieved.

## IMPROVED NOISE IMMUNITY, ACCURACY AND ZERO STABILITY

Dual-slope integration, as described in the theory of operation section offers several design benefits.

- Conversion accuracy for example, is independent of both the timing capacitor value and the clock frequency, since they affect in the same way the up ramp and down ramp integration period. Linearity is also improved because the analog conversion technique is free from discontinuities.
- Normal mode noise at line frequencies or its harmonics is rejected since the average value of this noise is zero over the integration period.
- To achieve zero stability, a time interval during each conversion is provided to allow the automatic-zero correction circuitry to measure and compensate for offset and offset drift errors, thereby, providing virtually no zero error.


## INTERFACING THE DPM

The latched digital data outputs and control interface signals are available on a " $3 \mathrm{M}^{\prime}$ " receptacle at the rear of the AD2004. The signals may be interfaced with the system using either the AC1600 or the AC1601 connector schemes.

The AD2004 requires 1.4 A maximum input current at +5 VDC for power. To minimize voltage drops on the connecting cable assembly, two lines for +5 V and two lines for power supply ground are provided. It is recommended that all 4 lines be used, especially with long connecting cables.

## ORDERING GUIDE

- AD2004 - Standard AD2004 as described above tuned for peak normal mode rejection at 60 Hz and its harmonics.
- AD2004/E - Standard AD2004 as described above - tuned for peak normal mode rejection at 50 Hz and its harmonics.


## CONNECTORS (optional)

- AC1600 6 feet of decade coded wire mated with " 3 M " Connector (Part No. 3414)
- AC1601 " 3 M " mating connector (Part No. 3414) only


# AC Powered 31⁄2 Digit DPM with Beckman Display 

## FEATURES

- AC Line Powered ( +5 VDC Powered Optional)
- $0.55^{\prime \prime}$ Beckman Display
- Differential Input
- Maximum Error: $\pm 0.05 \% \pm 1$ Digit
- AC Terminal Strip for Safety
- Ratiometric Operation
- Power Outputs for External Circuitry


## GENERAL DESCRIPTION

Analog Devices' model AD2006 is an AC line-powered, $3^{1 / 2}$ digit panel meter with Beckman displays for high visibility. The design of the AD2006 includes ratiometric operation and external power outputs to increase its application versatility.
The AD2006 provides high accuracy measurements of bipolar, differential input signals over a full scale range of $\pm 1.999 \mathrm{~V}$, with a maximum error of $\pm 0.05 \%$ (Reading) $\pm 1$ digit. For most applications, the differential input section provides greater than 70 dB of common mode rejection (CMRR) at common mode voltages (CMV) up to $\pm 5 \mathrm{~V}$. In addition, the AD2006 can be floated on the AC power supply in the singleended mode, allowing common mode voltages up to $\pm 300 \mathrm{~V}$ to be accommodated with common mode rejection exceeding 100 dB . To insure the safety of operational personnel and interconnected equipment, especially at high CMV, a terminal strip is provided for connection of AC power. For operation in noisy environments, an optional input filter can provide 40 dB normal mode rejection.
For best visual readout, the AD2006 is internally programmed to make 5 readings per second. For data acquisition applications, up to 90 conversions per second can be externally triggered. DTL/TTL compatible parallel BCD data outputs and control signals are provided for interfacing to other digital data systems. To extend its versatility, external power outputs suitable for powering op amps and IC circuits are available to facilitate scaling or buffering inputs and driving external logic. Standard ratiometric operation allows normalizing inputs to an external reference voltage for making compensated measurements with bridge and potentiometric transducers.
In addition to AC line powered versions, the $\mathrm{AD} 2006 / \mathrm{D}$ is available for operation from +5 VDC power supplies commonly used for digital logic circuitry. The AD2006/D has

identical performance specifications to all other AD2006 versions, except that it cannot be floated on the power supply for measurements at high common mode voltages and, of course, the +5 VDC output is not available.

## LARGE CLEAR DISPLAY ENHANCES READABILITY

The AD2006 uses large ( $0.55^{\prime \prime}$ ) Beckman, seven-segment, planar gas-discharge displays which appear as continuous solid digits. The display size, brightness, and contrast ratio makes the AD2006 readable at distances up to 40 feet or more and in any ambient lighting condition including bright sunlight. The display is filtered to provide bright red digits and is readable without distortion over a $130^{\circ}$ viewing angle. Overload conditions are indicated by displaying all dashes and the polarity sign remains valid. Decimal points are externally programmed and may optionally be specified for DTL/TTL compatibility. The polarity sign can be blanked for display in engineering units where polarity indication is unnecessary.

## OPTIONAL FEATURES EXTEND VERSATILITY

Several options are available with the AD2006 to allow the unit to be tailored to specific applications. Versions for all variations in power line voltages found throughout the world are standard. The AD2006/D is available for applications where the Beckman display is desired, but the DPM must operate from +5 VDC logic power supplies. The AD2006/N option is an input filter to provide 40 dB normal mode rejection at 60 Hz , with a 2 sec . settling time to $0.05 \%$. The AD2006/P option provides TTL/DTL compatible decimal point selection. The AD2006/C has a card edge connector instead of the standard 3 M multipin connector. Combinations of any of the above options except power supplies can be specified.


## AD2006 Simplified Block Diagram

## RATIOMETRIC OPERATION EXTENDS APPLICATIONS

The AD2006 has provision for making measurements normalized to an external reference voltage. This feature allows compensation for transducer outputs sensitive to excitation voltage variations, by making all measurements with reference to the excitation voltage. The next figure shows the AD2006 used with a bridge transducer which may be measuring temperature, pressure or any other physical parameter. The excitation voltage of the transducer is used as the reference input of the DPM. When used in the ratiometric mode, reference inputs in the range of +5.8 to 6.8 volts must be presented to the REFERENCE INPUT. The reference input must be relatively stable since the
DPM measures $\frac{\int_{t} E_{\text {in }} d t}{\int_{t} E_{r e f} d t}$ not $\int_{t} \frac{E_{\text {in }}}{E_{\text {ref }}} d t$, and any variations in the reference voltage during conversion may produce erroneous readings.


## Bridge Transducer Measurements Using the AD2006's Ratiometric Input

The REFERENCE OUTPUT can be used for driving transducers if it is properly buffered using an external op amp. A thermistor temperature measuring circuit can be built using the AD2006 to power the entire measurement system. The REFERENCE INPUT is a high impedence input which will not load any reference source, but this input is not protected from overload damage. If normal operation of a AD2006 is required, connection of the Reference Output to the Reference Input will allow operation using the internal +6.4 V reference source.


## AD2006 Thermistor Temperature Measurement System

## DC OUTPUTS CAN POWER EXTERNAL CIRCUITRY

Since the circuitry of the AD2006 requires $\pm 15 \mathrm{~V}$ and +5 V to be generated internally, these voltages are made available to allow operation of external circuitry used in conjunction with the DPM. Sufficient power is available to drive op amps to scale inputs or even buffer the reference output to drive transducers such as in the thermistor application shown above. The +5 V output (not available on AD2006/D models) can be used for external logic. In many measurements systems, these power outputs will be sufficient to power all the circuitry external to the DPM. Although the regulation and ripple are adequate for the sensitive analog and digital circuitry of the AD2006, further filtering may be necessary for components that are extremely power supply sensitive.

## OPTIONAL FEATURES \& ORDERING GUIDE

- Power Supply Inputs (only one may be specified)
$\left.\begin{array}{ll}\text { AD2006 } & 115 \mathrm{VAC} \pm 10 \% \\ \mathrm{AD} 2006 / \mathrm{E} & 220 \mathrm{VAC} \pm 10 \% \\ \mathrm{AD} 2006 / \mathrm{H} & 240 \mathrm{VAC} \pm 10 \% \\ \mathrm{AD} 2006 / \mathrm{F} & 100 \mathrm{VAC} \pm 10 \% \\ \text { AD2006/D } & +5 \mathrm{VDC} \pm 5 \%\end{array}\right\}(50-60 \mathrm{~Hz})$
(any combination of the following options may be specified)
- Normal Mode Rejection Filter: AD2006/N provides $>40 \mathrm{~dB}$ normal mode rejection $50-60 \mathrm{~Hz}$.
- Decimal Point Selection by DTL/TTL logic levels: AD2006/P.
- Card Edge Connector: AD2006/C
- Any combination of the above options -- excluding power inputs -- can be specified. When ordering, specify power supply option first, then the other options desired. For example, an AD2006/E/P/N operates on 220VAC, and has the decimal point and normal mode rejection filter options.


## CONNECTORS

- AC1600 (optional) - 3 M connector \#3414 and $6^{\prime}(1.83 \mathrm{~m})$ woven cable
- AC1601-connector only
- AD2006/C requires 30 pin, 0.156 spacing, Viking No. 2 VK 15D/1-2 or Cinch type 251 No. 5030 A 30 .
- AD2006/C optional - Order AC1501
- AC Power Line Cords are not supplied by ADI.


## FEATURES

- AC Line Powered
- Bright Seven-Segment Gas-Discharge Display
- Floating Input: $>100 \mathrm{~dB}$ CMRR, 300 V rms CMV
- NMR $>60 \mathrm{~dB}$ @ 50 or 60 Hz
- $\pm 0.005 \% \mathrm{R} \pm 50 \mu \mathrm{~V} \pm 1$ Digit Max Error
- Auto-Zero Correction
- Optional Ratiometric Operation
- Versatile Data Output Options - DTL/TTL/CMOS/PMOS Compatible


## GENERAL DESCRIPTION

Analog Devices' AD2008 is a $41 / 2$ digit AC line powered DPM designed for making high accuracy measurements in adverse electrical environments. The AD2008 measures bipolar voltages with a full scale range of $\pm 1.9999 \mathrm{~V}$ and an accuracy of $\pm 0.005 \%$ reading $\pm 50 \mu \mathrm{~V} \pm 1$ digit. The full floating, opto-isolated input section provides $>100 \mathrm{~dB}$ of common mode noise rejection at common mode voltages up to 300 V RMS even with control signals and optional data outputs connected. In addition, the dual slope integrating conversion technique allows $>60 \mathrm{~dB}$ of normal mode noise rejection at 50 or 60 Hz without filtering.

## LARGE, BRIGHT, EASILY READ DISPLAY

The AD2008 presents a visual readout on large 0.55 inch $(14 \mathrm{~mm})$ Beckman seven-segment gas-discharge displays. These displays are easily read at distances up to 50 feet ( 15 meters) and over viewing angles of $130^{\circ}$ in all ambient lighting conditions. Four decimal points are externally programmable. Controls are also available for display testing by illuminating all display segments, and independently blanking either the polarity sign or the entire display. The display lens is color matched to the gas discharge display. The lens has a non-glare, scratch-resistant finish and is easily marked with company logo or measurement units.

## VERSATILE DATA OUTPUT OPTIONS

The AD2008 uses a MOS/LSI integrated circuit that provides $41 / 2$ decades of counters and latches with considerable savings in size and power consumption. The data from this chip is provided in a character serial format, one decade at a time, which is used to multiplex the display. Since this data is not

easily interfaced to other data devices, two extra cost options are available for applications requiring BCD data interfacing. The AD2008/B provides full parallel latched BCD data for $41 / 2$ digits, overload and polarity. The AD2006/X provides a pulse train output and a polarity output, and the data must be counted external to the DPM. To extend application versatility, digital data output options are compatible to all DTL/TTL/ CMOS/PMOS logic systems.
The AD2008 normally provides 2.5 conversions per second. Externally triggered rates up to 5 conversions per second or automatic recycling at 5-10 conversions per second are also possible.

## OPTIONAL RATIOMETRIC OPERATION

The AD2008/R option allows the DPM to be used to measure the ratio of two input voltages. This is very useful when measuring with a transducer whose output is dependent on its excitation voltage. The DPM measures the ratio of the two voltages and thereby compensates for any variations caused by instability in the excitation voltage. Both the analog input and the external reference input are floating. For operation in the ratiometric mode, the AD2008/R is supplied without internal references; both positive and negative references must be supplied externally.


## AD2008 Simplified Block Diagram

## APPLICATION VERSATILITY

The high accuracy, good noise immunity, ratiometric option and versatile data output options make the AD2008 easy to integrate in many types of measurement systems. Some typical applications include:

- In-house test equipment for instruments and components where a bright, easily-read display, high accuracy and long term stability are needed.
- Digital weighing systems, using the ratiometric option for accurately reading the output of bridge-type transducers. The AD2008 can be calibrated easily to read out in the proper units. Long term stability is a plus here, too.
- Analytical and scientific instrumentation where high accuracy and wide dynamic range of measurement are necessary.
- Process control monitoring in an industrial environment, where E-M noise and high common mode voltages are commonplace.


## DESIGNED AND BUILT FOR RELIABILITY

High reliability has been designed into the AD2008. In the AD2008, the latest IC technology is utilized to minimize parts count and lower heat dissipation for cooler operation. Manufacturing processes are controlled by continuous quality assurance inspections to insure proper workmanship and testing. Like every other Analog Devices' DPM, the AD2008 is fully tested for electronic specifications, vibration tested to $1 \%$ AQL and given one full week of failure-free burn-in before shipment. The design, manufacturing and testing procedures at Analog Devices are designed to insure reliable DPM's.

## OPTIONAL FEATURES AND ORDERING GUIDE

- Power Supply Inputs ${ }^{1}$

| AD2008 | $115 \mathrm{VAC} \pm 10 \%$ @ 60 Hz |
| :--- | :--- |
| AD2008/E | $220 \mathrm{VAC} \pm 10 \%$ @ 50 Hz |
| AD2008/H | $240 \mathrm{VAC} \pm 10 \%$ @ 50 Hz |
| AD2008/F5 | $100 \mathrm{VAC} \pm 10 \%$ @ 50 Hz |
| AD2008/F6 | $100 \mathrm{VAC} \pm 10 \%$ @ 60 Hz |

- Data Output Options ${ }^{2}$ (DTL/TTL/CMOS/PMOS Compatible) AD2008/B - Parallel BCD Data AD2008/X - Count Data Output
- AD2008/R - Ratiometric Operation
${ }^{1}$ Only one power supply option may be specified.
${ }^{2}$ Only one data output option may be specified. If data outputs are not needed, no option should be ordered.
Either data output option and/or ratiometric operation can be ordered with any power supply option.


## CONNECTORS

- P1 36 Pin, 0.156 inch spacing card edge connector, Viking No. 2Vk 18D/1-2 or equivalent
- P1 Optional - Order AC2610 @ \$5.00 each
- P2 $30 \mathrm{Pin}, 0.156$ inch spacing card edge connector, Viking No. 2Vk 15D/1-2 or equivalent
- P2 Optional - Order AC1501, \$3.50 each


## AD2010

## Low Cost 3 $1 / 2$ Digit DPM For OEM Applications

## FEATURES

- LED Display with Latched Digital Outputs
- Small Size: $1.8^{\prime \prime} \mathrm{H} \times 3^{\prime \prime} \mathrm{W}$ x $3 / 4$ " ; Lightweight: 4 oz .
- Automatic Zero Correction; Max Error: $0.05 \% \pm 1$ Digit
- High Normal Mode Rejection: Adjustable to $>60 \mathrm{~dB} @ 60 \mathrm{~Hz}$
- Optional Ratiometric Operation
- Leading " 0 " Display Blanking
- +5 VDC Powered
- Low Cost


## GENERAL DESCRIPTION

Analog Devices' model AD2010 represents an advance in size/ performance capabilities of $31 / 2$ digit digital panel meters. The AD2010 offers $0.05 \% \pm 1$ digit maximum error with bipolar, single ended input, resolution of $100 \mu \mathrm{~V}$, a common mode rejection ratio of 60 dB (CMRR) at $\pm 200 \mathrm{mV}$ (CMV) and an ultrasmall, snap-in case design.
The AD2010 features a light-emitting-diode (LED) display with a full scale range of 0 to $\pm 199.9$ millivolts, latched digital data outputs and control interface signals, and leading zero display blanking. Automatic-zero correction circuitry measures and compensates for offset and offset drift errors, thereby providing virtually no error. Another useful feature of the AD2010 is its 5VDC operation. The AD2010 can operate from the users' 5VDC system supply, thereby eliminating the shielding and decoupling needed for line powered units when the AC line must be routed near signal leads.
To satisfy most application requirements, the conversion rate of the AD2010 is normally 4 readings per second. However, an external trigger may be applied to vary the sampling rates from a maximum of 24 readings per second down to an indefinite hold time. The AD2010 can also be connected for automatic conversion at its maximum conversion rate. During conversion, the previous reading is held by the latched logic. The numeric readout is available as BCD data. Application of the metering system in a computer or data logging system is made easy with the availability of the "overrange," "polarity," "overload," and "status" signals.
IMPROVED NOISE IMMUNITY, ACCURACY AND ZERO STABILITY
Dual-slope integration, as used in the AD2010 offers several design benefits.


- Conversion accuracy, for example, is independent of both the timing capacitor value and the clock frequency, since they effect both the up ramp and down ramp integration in the same ratio.
- Normal mode noise at line frequencies or its harmonics is rejected since the average value of this noise is zero over the integration period.
- To achieve zero stability, a time interval during each conversion is provided to allow the automatic-zero correction circuitry to measure and compensate for offset and offset drift errors, thereby, providing virtually no zero error.


## LED's GIVE LONG LIFE, SHARP DISPLAY

The numeric outputs are displayed using $0.27^{\prime \prime}$ high, 7 segment, red LED's. The LED's provide the physical ruggedness typical of IC's, with a life expectancy in excess of 100,000 hours. The displayed numerals are sharp and easily readable at distances of up to 8 feet. The clean uncluttered look of the lens and case design further enhance the visual attractiveness of the display.
Optical features of the display include: a minimum photometric brightness of 200 foot-lamberts, and a 6300 angstrom, wavelength at peak emission (red). Other display features include programmable decimal points, automatic zero, 4 readings per second display rate, external trigger-and-hold rate of up to 24 readings per second, flashing-zeros overload indication, and leading "zero" display blanking.


Simplified Block Diagram

## WHAT IS A "LIMITED-DIFFERENTIAL" INPUT?

The AD2010 eliminates most ground loop problems by means of a "limited differential" input circuit. The analog ground is connected to the digital and power supply grounds by a $47 \Omega$ resistor, and the analog input is designed to tolerate greater than 200 mV variations between analog and digital grounds. Although not providing true "differential" performance, the AD2010 input ground can follow the "low" side of input signals at common mode voltages exceeding the full scale range of the DPM and provide greater than 60 dB of common mode rejection.

The AD2010 can be used in instrument designs where the measurement system and the DPM share a common power supply and ground loops may exist. Although good system design practice requires all grounds to be tied together at a common point, current flowing in the ground lines can produce variations in the ground levels around the system of several hundred millivolts. The $47 \Omega$ isolation resistor in the AD2010 is much larger than the system interconnection resistance and limits the current flowing in the DPM section of the circuit to a few milliamps. This "limited differential" input can, therefore, allow operation in a simplified systems layout without ground loop problems.

## LEADING ZERO SUPPRESSION

The AD2010 has provision for suppressing leading zeroes to enhance readability, allowing a readout of 018 to be displayed as 18 , for example. If the leading zero suppression line, pin R , is grounded or connected to a DTL/TTL logic " 0 ", all leading zeroes will be blanked. Returning the line to logic " 1 " or open circuit will restore normal operation.

## AD2010 RATIOMETRIC OPERATION

The ratiometric option (AD2010/R) allows readings to be normalized to an external reference voltage. This option allows accurate measurements to be made with transducers that are sensitive to excitation supply variations. Since the dual-slope converter compares each input voltage with an accurate internal reference, the reading is a ratio of two voltages. If an external reference, such as the transducer excitation supply, is used, the reading then becomes the ratio of the transducer output to the excitation voltage, and any variations in the transducer output are compensated. One must always remember, however, that the AD2010/R
measures $\frac{\int_{t} E_{\text {in }} d t}{\int_{t} E_{\text {ref }} d t}$ not $\int_{t} \frac{E_{\text {in }}}{E_{\text {ref }}} d t$, and any variations
of the reference during conversion can produce erroneous readings. To maintain accuracy, the reference voltage must be in the range of +100 mV to +300 mV .

Since the AD2010/R has a single-ended input, measurements cannot be made with bridge transducers. A differential instrumentation amplifier, such as the AD520, can provide the proper inputs to the AD2010.


## AD2010/R Bridge Transducer Measurement Circuit

In addition, the reference output of any AD2010 can be used as a stable excitation voltage for a transducer. The reference output can supply only a few microamps of current, but buffering with an external op amp can provide sufficient current capability for most transducers, and scale the reference output to provide the proper excitation voltage for the transducer.


## Using the AD2010 Reference Output to Drive a Transducer

## ORDERING GUIDE

- AD2010 - Standard AD2010 as described above - tuned for peak normal mode rejection at 60 Hz and its harmonics.
- AD2010/E - Standard AD2010 as described above tuned for peak normal mode rejection at 50 Hz and its harmonics.
- AD2010/R - Standard AD2010 as described above with Ratiometric option
- AD2010/E/R - Standard AD2010/E as described above with Ratiometric option


## CONNECTORS

- 30 Pin 0.156 spacing, Viking No. 2Vk 15D/1-2 or Cinch type 251 No. 5030A30.
- Optional - Order AC1501

SPECIFICATION SUMMARY (Typical @ $+25^{\circ} \mathrm{C}$ unless otherwise noted)

| Model | AD2001 | AD2002 | AD2003 | AD2004 |
| :---: | :---: | :---: | :---: | :---: |
| Display |  |  |  |  |
| Number of Digits | $3^{1 / 2}$ | $2^{1 / 2}$ | $3^{1 / 2}$ | $4^{1 / 2}$ |
| Type | Numitron | Numitron | Numitron | LED |
| Overload Indication | Zero's + "1" Flashes | Dashes | Dashes | Flashing Zeros |
| Decimal Points | Selectable at Input | Selectable at Input | Selectable at Input | Selectable at Input |
| Filament Test | No | Yes | Yes | No |
| Input |  |  |  |  |
| Type | Single-ended | Single-ended | Differential | True Floating |
| Zero | Automatic | N/A | Automatic | Automatic |
| Polarity | Bipolar | Unipolar | Bipolar | Bipolar |
| Full Scale Range | 0 to $\pm 199.9 \mathrm{mV}$ | 0 to +1.99 V | 0 to $\pm 199.9 \mathrm{mV}$ | 0 to $\pm 1.9999 \mathrm{~V}$ |
| Bias Current | 1.5 nA | 70 nA | 3 nA | 1 nA |
| Impedance | $100 \mathrm{M} \Omega$ | $100 \mathrm{M} \Omega$ | $100 \mathrm{M} \Omega$ | $100 \mathrm{M} \Omega$ |
| Overvoltage Protection w/o damage (sustained) | $\pm 20 \mathrm{~V}$ | $\pm 50 \mathrm{~V}$ | $\pm 50 \mathrm{~V}$ | $\pm 50 \mathrm{~V}$ |
| Accuracy |  |  |  |  |
| Maximum Error of Reading ${ }^{3}$ | $0.05 \% \pm 1$ Digit | 0.5\% $\pm 1$ Digit | 0.05\% $\pm 1$ Digit | 0.01\% $\pm 1$ Digit |
| Resolution | 0.1 mV | 10 mV | 0.1 mV | 0.1 mV |
| Temperature Range Operating ${ }^{4}$ | 0 to $+60^{\circ} \mathrm{C}$ | 0 to $+60^{\circ} \mathrm{C}$ | 0 to $+60^{\circ} \mathrm{C}$ | 0 to $+50^{\circ} \mathrm{C}$ |
| Temperature Coefficient | $\pm 50 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 50 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | $\pm 15 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |
| Conversion Rate |  |  |  |  |
| Internal Conversions/sec | 5 | 4 | 5 | 4 |
| External Conversions/sec max | 20 | 200 (w/DP Option) | 16 | 8 |
| Hold \& Read on Command | Std | w/DP Option | Std | Std |
| Interface Signals (DTL/TTL Compatible) |  |  |  |  |
| Inputs |  |  |  |  |
| Externally Triggerable | Std | DP Option | Std | Std |
| External Hold | Std | DP Option | Std | Std |
| Outputs |  |  |  |  |
| BCD Digits | Std | DP Option | Std, Latched | Std, Latched |
| Overrange Signal | Std | DP Option | Std, Latched | Std, Latched |
| Overload Signal | Std | DP Option | Std, Latched | Std, Latched |
| Status Signal | Std | DP Option | Std, Latched | Std, Latched |
| Polarity Signal | Std | User Programmable | Std | Std |
| Connector ${ }^{1}$ | PCB | Multipin (DP Option) | Multipin or PCB (C Option) | ) Multipin |
| Normal Mode Rejection (@) $50-60 \mathrm{~Hz}$ ) | N/A | Requires Filter | 40 dB | 60 dB |
| Common Mode Rejection <br> (DC-1 $\mathrm{kHzw} / 1 \mathrm{k} \Omega$ unbalance) | N/A | N/A | 80 dB | 120 dB |
| Common Mode Voltage | N/A | N/A | $\pm 2.5 \mathrm{~V}$ | $\pm 300 \mathrm{VDC}, 600 \mathrm{~V}$ p-p |
| Power | $+5 \mathrm{~V}, 1 \mathrm{~A}$ | $+5 \mathrm{~V}, 750 \mathrm{~mA}$ | $+5 \mathrm{~V}, 1 \mathrm{~A}$ | $+5 \mathrm{~V}, 1.4 \mathrm{~A}$ |
| Warm Up To Rated Accuracy | Essentially none | Essentially none | Essentially none | 30 min |
| Adjustments | Range Potentiometer | Range Potentiometer | Range Potentiometer | Range Potentiometers <br> Zero Potentiometers |
| Size, inches mm Case Mounting | $\begin{gathered} 3^{\prime \prime} \mathrm{W} \times 1.75^{\prime \prime} \mathrm{H} \times 1.5^{\prime \prime} \mathrm{D} \\ 76.2 \times 44.5 \times 38.1 \\ \text { Bezel } \\ \hline \end{gathered}$ | $\begin{gathered} 3^{\prime \prime} \mathrm{W} \times 1.8^{\prime \prime} \mathrm{H} \times 1.5^{\prime \prime} \mathrm{D} \\ 76.2 \times 45.7 \times 38.1 \\ \text { Snap-In } \\ \hline \end{gathered}$ | $\begin{gathered} 3^{\prime \prime} \mathrm{W} \times 1.8^{\prime \prime} \mathrm{H} \times 2^{\prime \prime} \mathrm{D} \\ 76.2 \times 45.7 \times 50.8 \\ \text { Snap-In } \\ \hline \end{gathered}$ | $\begin{gathered} 3^{\prime \prime} \mathrm{W} \times 1.8^{\prime \prime} \mathrm{H} \times 2.5^{\prime \prime} \mathrm{D} \\ 76.2 \times 45.7 \times 63.5 \\ \text { Snap-In } \\ \hline \end{gathered}$ |
| Price (1-9), (100's) qty. | \$142, \$89 | \$93, \$59 | \$156, \$99 | \$314, \$199 |
| Options Price (1-9), (100's) qty. |  | AD2002/DP - \$99, \$62 | AD2003/C - \$156, \$99 AD2003/E - \$156, \$99 AD2003/E/C - \$156, \$99 | AD2004/E \$314, \$199 |

[^14]

[^15]Optional lenses and connectors are described and priced in the Mechanical Section.


# SERDEX MODULES <br> A NEW APPROACH TO DIGITAL COMMUNICATION AND CONTROL SYSTEMS 

Analog Devices' SERDEX ${ }^{\text {tm }}$ SERial Data EXchange Modules offer a revolutionary approach to the design and implementation of digital communication and control systems. Through the use of five building block module types, systems can be built ranging in complexity from the simple single channel system shown below to very complex systems with thousands of channels.
All systems built with SERDEX Modules have one thing in common, however: they are controlled either manually using a standard teletypewriter or any teletypewriter compatible CRT terminal or under computer control by any computer that has a teletypewriter port. The controlling teletypewriter or computer transmits data to, receives data from, and issues control commands to the system to which it is connected.
The modules themselves perform several functions. They are used to convert the parallel output data from devices such as analog-to-digital converters into standard serial ASCII data that can be transmitted long distances over a single pair of wires and then handled directly by a standard teletypewriter. Conversely, they translate the ASCII serial data received from a teletypewriter or computer into the parallel data required by digital input devices such as digital-to-analog converters. In addition, the modules recognize nine standard printing ASCII characters that are used to control the modules themselves, and to control such system components as valves, sensors, motors, and contactors. SERDEX Modules can be used in designing and constructing data communication and control systems for such applications as:

- Inventory and control of material storage tanks (such as: petroleum, milk, grain, cement)
- Monitor and control of remote pipeline pumping stations
- Data logging and control of complex laboratory experiments involving chromatographs, spectrophotometers, mass spectrometers, and the like
- Chemical and food process control
- Factory control
- Automatic test systems
- Programming and control of processing furnaces and ovens
- Data logging and control of broadcasting transmitters
- Hospital and medical laboratory data communication
- Environmental and pollution monitoring


The system shown below is a very simple example of the SERDEX Modules approach. A standard teletypewriter is connected via a single unshielded twisted pair of wires to a remotely located SERDEX Serial Transmitter Module. This module is the heart of a simple system used to determine the liquid level in a storage tank, and on the basis of that information, turn a fill valve on or off.
Someone wanting to know the level in the tank could type the following statement:

## WHAT IS THE LEVEL IN THE TANK?

The Serial Transmitter Module will do nothing until it recognizes one of its control characters, and the only control character transmitted in the above statement was the question mark. The English sentence allows a clear understanding of what is taking place, but does not affect system operation.
Upon recognition of the question mark control character, the Serial Transmitter issues a convert command to the analog-todigital converter. After the A/D conversion has been completed, the converter's parallel output data is converted into serial ASCII data by the Serial Transmitter, and sent back to the teletypewriter, where it would be printed:

## WHAT IS THE LEVEL IN THE TANK?496

The operator may then decide that more liquid should be added to the tank, and would type:

TURN THE VALVE ON*
Upon recognition of the asterisk control character, the Serial Transmitter Module produces a short pulse that, in this example, is fed to a valve controller. The operator can continue to query the system periodically to monitor the level of the tank as it is being filled, perhaps foregoing the English description and typing only the necessary control character:

## ? 582 P610 7718

When the desired level has been reached, the check-and-fill cycle is completed by typing:

TURN THE VALVE OFF!

STX1003 SERIAL TRANSMITTER MODULE (Figures $1 \& 2$ ) The Serial Transmitter Module can send a string of up to eight ASCII numerical characters, which typically would be the parallel output data of a BCD coded A/D converter. It can also transmit output data from a binary coded A/D converter when the bits are arranged into groups of three for transmission as octal digits. With the use of external shift registers, the STX1003 can be expanded to transmit any desired ASCII characters, including plus sign, minus sign, decimal point, space, carriage return, and alphabetic characters. The Serial Transmitter Module can also be expanded with external shift registers to transmit a string of characters of any desired length.

The STX1003 recognizes eight control characters. Two, the question mark and slash mark, are used to control the operation of the module itself. The question mark is normally used to iniate an A/D conversion, while the slash mark initiates a retransmission of a test message that can be wired up at the user's option. The remaining six characters are the asterisk, exclamation point, dollar sign, equal sign, apostrophe, and percent sign. Upon receipt of any of these characters, the Serial Transmitter Module puts out a short pulse on a particular module pin that can be used for control of system components.

## ELEMENTARY SYSTEMS



Figure 1. STX1003 Serial Transmitter (For details of this system, request SERDEX Note 1 "Interfacing the teletype with . . . ADC1100 A/D converter")


Figure 2. Teletype or Computer-Controlled 8-channel DataLogger. Typing an ! advances the address counter. Typing a \% resets the counter to the first channel, and typing a ? initiates serial data transmission from the selected channel to the teletype.

## SRX1005 SERIAL RECEIVER MODULE (Figures 3 \& 4)

The Serial Receiver Module can receive up to eight data characters, which would typically be decimal digits that are decoded into data inputs for a BCD coded D/A converter. It can also be used with binary coded D/A converters when the binary data is grouped three bits to a character for transmission as octal digits. The SRX1005 can be expanded to receive and recognize other ASCII characters, such as alphabetic characters. It can also be expanded with external shift registers to accept a string of characters of any desired length.
The SRX1005 recognizes the same eight control characters as does the STX1003, but they are used in a slightly different way. The equal sign clears the SRX1005's internal register and prepares it to accept new data. After the data has been sent, the dollar sign is used as a termination character; once it has been sent, no further data will be accepted until another equal sign has been transmitted. A typical transmission would be:

## SET FLOW RATE $=137 \$$

The remaining six characters (* !'\% ? /) are available for system control.

## SMX1004/SMC1007

SERIAL MULTIPLEXER MODULES (Figures 5 \& 6)
An SMX1004 Serial Multiplexer Module and SMC1007 Serial Multiplexer Control Module are used together to form an eight channel multiplexer. The desired channel is selected with the controlling teletypewriter or computer by transmitting the number symbol (\#) followed by the channel number. The channel addresses are the numbers zero through seven.
A 16 channel multiplexer can be formed using two SMX1004's with one SMC1007. In this instance, eight channels are addressed with the numbers zero through seven, and eight with the letters P through W. Multiple-ranking of the SMX1004/SMC1007 permits access to more than 16 channels.

## SCL1006 CLOCK MODULE

The Clock Module is an accessory module; it supplies clock pulses and -15 V power to the STX1003, SRX1005, and SMC1007 Modules. One SCL1006 Module is required at each location where there is at least one of these other modules. The Clock Module can feed up to four of the other modules, if they are all located together.


Figure 3. SRX1005 Serial Receiver (For details of this system, request SERDEX Note 2 "Interfacing the teletype with. . . DAC120M-BCD D/A converter")


Figure 4. Self-Multiplexed Analog Output. Several D/A converters with registers are connected in parallel to one SRX1005. The \%,!, or * strobes the input register of the desired D/A converter.


Figure 5. SMC1007/SMX1004 Serial Multiplexer


Figure 6. A Complex 3-channel Data Acquisition and Control System. To read the analog input signal, the operator would type \#1? and wait for print-out of the data. To set the output voltage at mid-scale, he would type \#2 = 500\$. Likewise, \#3* would turn on the light

## SPECIFICATIONS

## SYSTEM PERFORMANCE

Transmission Format:
Bit Rate
Via Isolated 20 mA . Current Loop
Direct TTL:
Clock Rate:
Sampling Rate (at 4,800 Baud, using multiplexer, assuming 4 BCD digits per sample):
Cable Requirements:
Logic Inputs and Outputs:
Operating Temperature:
Storage Temperature:
Terminals:

## ASCII-coded, asynchronous, serial

User-programmed up to 4,800 Baud
User-programmed up to 20,000 Baud
16 x Bit Rate
$\approx 50$ samples per second
Twisted-pair up to 10,000 feet (See Figure 7)
TTL-Compatible
0 to $+70^{\circ} \mathrm{C}$
$-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$
0.025 in. sq. suitable for wire-wrap,
solder, or sockets


Figure 7. Maximum Length of Twisted Pair as a Function of Baud Rate

## INDIVIDUAL MODULES

|  | STX1003 <br> SERIAL TRANSMITTER | SRX1005 <br> SERIAL RECEIVER | SMC1007/SMX1004 SERIAL MULTIPLEXER | SCL1006 <br> CLOCK MODULE |
| :---: | :---: | :---: | :---: | :---: |
| DEVICE FUNCTION | Interfaces A/D converter or similar parallel-output devices directly with a teletypewriter or with a computer having asynchronous, serial signal lines. In addition, six independent control commands are available for system control. (Figure 1) | Interfaces D/A converter or similar parallel-programmed devices directly with a teletypewriter or with a computer having asynchronous, serial signal lines. In addition, six independent control commands are available for system control. (Figure 3) | Interfaces a teletypewriter or computer with any number of STX1003's and/or SRX1005's. One SMC1007 and one SMX1004 form an 8-channel bidirectional serial multiplexer. An additional SMX1004 permits access to 16 channels. (Figure 5) | Provides sixteen pin-selectable clock frequencies and -15 volt power to the other modules. Only +5 volt power is required. Each SCL1006 can service up to 4 other modules if they are located in close proximity. |
| KEYBOARD COMMANDS | Typing a question mark (?) causes the STX1003 to initiate an A/D conversion and transmit the resulting data back to the teletypewriter: ?1364 <br> Alternatively, a STATUS input may be strobed at the remote location to initiate transmission. | A remote D/A converter with storage registers may be updated by typing an equal sign (=), the data, and finally a dollar sign (\$): $=693 \$$ <br> A READY signal provides indication that received data is available. | A channel is selected from the keyboard by typing the number symbol (\#) followed by the channel number(s). The resulting channel remains open until a new channel is selected. Examples: <br> SINGLE RANK ( $\leqslant 16$ channels): \#3 DUAL RANK ( $\leqslant 256$ channels): \#42 TRIPLE RANK ( $\$ 4096$ channels): \#517 | NONE |
| CONTROL COMMANDS | Typing any of the six control characters causes a high-level to low-level pulse to appear on six associated STX1003 terminals: $\%,{ }^{*},{ }^{\prime},!,=, \$$ | Typing any of the six control characters causes a high-level to low-level pulse to appear on six associated SRX1005 terminals: \%, *, ', !, ?, l | NONE | NONE |
| MESSAGE LENGTH \& CHARACTER SET | Up to eight BCD or octal digits. May be expanded with external shift registers to transmit any number of characters and/or the entire ASCII character set. | Up to eight BCD or octal digits. May be expanded with external shift registers to receive any number of characters and/or the entire ASCII character set. | An unlimited number of characters selected from the entire 128 -character ASCII code may be transmitted or received. External shift registers are not required. | NONE |


| SIGNAL INTERFACE | Optically-isolated 20 mA current loop in which the 20 mA is supplied either by the data terminal or by an external loop supply voltage. Isolation breakdown is greater than 300 volts. In addition, direct TTL interface is provided. (See Figure 8) | Optically-isolated 20 mA current loop in which the 20 mA is supplied either by the data terminal or by an external loop supply voltage. Isolation breakdown is greater than 300 volts . In addition, direct TTL interface is provided. (See Figure 8) | Data Terminal Interface: <br> Optically-isolated 20 mA current loop in which the 20 mA is supplied either by the data terminal or by an external loop supply voltage: Isolation breakdown is greater than 300 volts. In addtition, direct TTL interface is provided. Channel Interfaces: A current regulator per channel each will sink 20 mA to the multiplexer ground. Only a single unregulated loop voltage is needed to interface the data channels with other SERDEX Modules. | NONE |
| :---: | :---: | :---: | :---: | :---: |
| USER-PROGRAMMED OPTIONS | 6,7 , or 8 data bits per asynchronous serial character; odd, even, or no parity; 1 or 2 stop bits; echo of test message. | 7 or 8 data bits per asynchronous serial character; odd, even, or no parity; 1 or 2 stop bits; acknowledgement of error-free data transmission. | 6, 7 , or 8 data bits per asynchronous serial character; odd, even, or no parity; 1 or 2 stop bits per character. | Pin-selectable Baud Rate: $110,150,220$, $300,440,600,880,1.2 \mathrm{k}, 1.76 \mathrm{k}, 2.4 \mathrm{k}$, $3.52 \mathrm{k}, 4.8 \mathrm{k}, 7.04 \mathrm{k}, 9.6 \mathrm{k}, 14.1 \mathrm{k}$, and 19.2 k |
| CURRENT REQUIREMENTS | $\begin{aligned} & +5 \mathrm{~V} \pm 5 \% \text { at } 350 \mathrm{~mA} \\ & -15 \mathrm{~V} \pm 20 \% \text { at } 20 \mathrm{~mA} \\ & +12 \mathrm{~V} \text { to }+20 \mathrm{~V} \text { at } 20 \mathrm{~mA} \text { for supplying } \\ & \quad \text { loop current (see Note 1) } \end{aligned}$ | $\begin{aligned} & +5 \mathrm{~V} \pm 5 \% \text { at } 300 \mathrm{~mA} \\ & -15 \mathrm{~V} \pm 20 \% \text { at } 20 \mathrm{~mA} \\ & +12 \mathrm{~V} \text { to }+20 \mathrm{~V} \text { at } 20 \mathrm{~mA} \text { for supplying } \\ & \quad \text { loop current (see Note } 1 \text { ) } \end{aligned}$ | SMC1007 SMX1004 <br> $+5 \mathrm{~V} \pm 5 \%$ at 300 mA $+5 \mathrm{~V} \pm 5 \%$ at 150 mA <br> $-15 \mathrm{~V} \pm 20 \%$ at 20 mA +12 V to +20 V for <br> +12 V to +20 V at supplying the channel <br> 20 mA for supplying loop currents; 20 mA <br> loop current per data channel. <br> (see Note 1)   | $+5 \mathrm{~V} \pm 5 \%$ at 200 mA , plus 75 mA per module serviced In addition, the SCL1006 supplies $-15 \mathrm{~V} \pm 20 \%$ at up to 80 mA . |
| PRICE (1-9) | \$197 | \$197 | \$153 \$83 | \$72 |
| MOUNTING CARDS | Three printed circuit boards with approp receiver, or multiplexer subsystem will b | ERDEX modules interconnected as a rea ble in early 1975. Consult factory for de | use transmitter, |  |

Note 1 . Not required if loop current is supplied by the data terminal or the SMX1004. Loop current may be supplied by 20 mA current regulator or by a regulated voltage source in series with a resistor, as shown in Figure 8
Specifications subject to change without notice.

## SERIAL TRANSMISSION USING 20MA CURRENT LOOP



Figure 8. Each teletype serial character consists of one start bit, seven ASCII-coded data bits, a parity bit, and two stop bits. Prior to transmitting a character, all loop switches are closed and 20 mA flows. A start bit, followed by the data bits, is transmitted by operating one of the transmitter switches. The receiver amplifiers detect the presence or absence of loop current.

## HOW THE SERDEX MODULES WORK

## STX1003 SERIAL TRANSMITTER MODULE (Figure 9)

When one of the control characters is received (\%, *, \$, =, !, or '), a pulse is issued at the appropriate terminal. If a question mark (?) is received, and A/D conversion is initiated. When the converter's status level changes, indicating that conversion is complete, it causes the resulting digital data to be transmitted serially back to the control center. As Figure 9 shows, up to 8 BCD digits can be sent, or up to 24 binary bits (if they are arranged in groups of 3 for transmission as octal digits). By the use of external shift registers, the STX1003's word output can be expanded to transmit a string of characters of any desired length, including outputs of additional A/D converters or such ASCII characters as plus and minus signs, decimal point, space, carriage return, and alphabetic characters.
The serial output of the STX1003's parallel-loaded shift register (and any external extensions) is fed to the parallel-to-ASCII converter, where it is transmitted one-character-at-a-time to the teletypewriter or computer.


Figure 9. Block Diagram of the STX1003 Serial Transmitter

## SRX1005 SERIAL RECEIVER MODULE (Figure 10)

Upon receiving one of the control characters (\%, ?, !, ', /, *), the Serial Receiver emits a pulse on the appropriate pin. The equal sign (=) clears the internal register and the ready flip-flop. The data characters that follow can enter the shift register,


Figure 10. Block Diagram of the SRX1005 Serial Receiver
until a terminating dollar sign (\$) is received. The \$ sets the ready flip-flop, strobes the data into the converter, and inhibits acceptance of additional data until the next $=$ arrives.
The SRX 1005 can receive up to 8 BCD digits, or up to 24 binary bits, if the bits are grouped in 3 's and transmitted as octal digits. If external shift registers are added, the SRX1005 can be expanded to receive other ASCII characters, such as alphabetics, or to accept a string of characters of any desired length.

## SMX1004/SMC1007 SERIAL MULTIPLEXER MODULES (Figure 11)

The SMX1004 and SMC1007 together form an 8-channel bidirectional multiplexer. For up to 16 channels, 1 additional SMX1004 is used. The first eight channels ( $0-7$ ) are addressed from the teletypewriter or computer by transmitting the number symbol ( $\#$ ), followed by a digit from zero (channel 0) through 7 (channel 7); for the second set of eight channels, \# is followed by a letter from $P$ through $W$ (i.e., 8 through 15).

Multiple ranking of the SMX1004/SMC1007 combination permits communication with an unlimited number of channels. For example, in a dual-rank configuration (e.g., $8 \times 8=64$ channels), channel 3 of the first rank and channel 6 at the second rank would be addressed if the multiplexers received the characters \#36.

Serial data received from the teletypewriter or computer is converted to parallel form, decoded to extract the number symbol and channel address, then converted back to serial data for transmission to the selected channel. Data returning from the remote channel is merely relayed back to the central control station.


Figure 11. Block Diagram of a SMX1004/SMC1007 Multiplexer

## SCL1006 CLOCK MODULE

By programming the oscillator for either high or low frequency and selecting one of the 8 divider outputs, one can choose among 16 clock frequencies, ranging from 110 Baud (i.e., bits/second) up to 19.2 kilobaud. The SCL1006 also converts +5 VDC to -15 VDC and furnishes it to the associated modules.

## HOW TO ORDER

Listed Here are the Major Components Required to Assemble the Elementary Systems Shown in Figures 1, 3 and 5. Also Required are Various Resistors, Potentiometers, TTL Buffers, Twisted-Pair Wire and Mounting Hardware. For Further Information, Request the Literature Listed Below.

| Component Description <br> (All Manufactured by Analog Devices Except Teletype) |  | Transmitter <br> System <br> Figure 1 | Receiver <br> System <br> Figure 3 | Multiplexer <br> System <br> Figure 5 |
| :---: | :---: | :---: | :---: | :---: |
| SERDEX Modules (Prices Listed in Specifications) | STX1003 Serial Transmitter SRX1005 Serial Receiver SMC1006 Multiplexer Controller SMX1004 Serial Multiplexer SCL1006 Clock Module | 1 Required <br> 1 Required | 1 Required <br> 1 Required | 1 Required <br> 1 Required <br> 1 Required |
| A/D Converter | ADC1100 or Equivalent | 1 Required |  |  |
| D/A Converter | DAC12QM-BCD, DAC1118-025 or Equivalent |  | 1 Required |  |
| Power Supplies | ```Logic Supply - Model 905 ( \(5 \mathrm{~V}, 1 \mathrm{amp}\) ) Analog Supply - Model 904 \(( \pm 15 \mathrm{~V}, 50 \mathrm{~mA})\) TTY Loop Supply - Model 915 \((15 \mathrm{~V}, 25 \mathrm{~mA})\) Data Channel Loop Supply - Model 920 ( \(15 \mathrm{~V}, 200 \mathrm{~mA}\) )``` | 1 Required <br> 1 Required | 1 Required <br> 1 Required <br> 1 Required | 1 Required <br> 1 Required <br> 1 Required |
| Teletypewriter | Teletype Model 33 KSR , or Equivalent 60 Hz Power: \#3310/3EC <br> 50Hz Power: \#3310/3SE | 1 Required | 1 Required | 1 Required |

## APPLICATION NOTES AND INSTRUCTION MANUALS (AVAILABLE UPON REQUEST):

SERDEX Note 1: "Interfacing the Teletype Model 33KSR with Analog Devices' Model ADC1100 A/D Converter" SERDEX Note 2: "Interfacing the Teletype Model 33 KSR with Analog Devices' Model DAC12QM-BCD D/A Converter"
SERDEX Note 3: "Using the Teletypewriter to Program Remote Relays, Solenoids or Other Power Devices"
SERDEX User's Guide: Serial Transmitter STX1003 and SCL1006
SERDEX User's Guide: Serial Receiver SRX1005 and SCL1006
SERDEX User's Guide: Serial Multiplexer SMX1004/SMC1007 and SCL1006

## DIMENSIONS



[^16]Figure 12. STX1003, SRX1005, and SMC1007 (Note that Pins B1-B24 and C1-C24 are Omitted on the SMC1007.)


Figure 13. SMX1004 and SCL 1006 (Note that Pins A1, A2, $A 3, A 16, A 17, A 18, B 1, B 2, B 3, B 16, B 17$, and $B 18$ are omitted on the SCL 1006.)

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# FUNCTION MODULES MULTIPLIERS/DIVIDERS 

## PRODUCT PROFILE

Multipliers from Analog Devices use solid state techniques to develop the transfer function $+\mathrm{XY} / \mathbf{1 0}$. Most models are capable of performing division according to the function $+10(Z / X)$, hence the term multiplier/divider. Except for models 424, 530 and 531 , all units are factory trimmed to guaranteed accuracies and require no further adjustments unless higher accuracies are required for the job. External trimming of offsets, feedthrough and scale factor terms may yield up to a two-fold improvement in accuracy.
Multiplier/Divider circuits are a fundamental system component. Despite their fundamental nature, the historical high cost and application complexity of multiplier/divider modules limited their use by OEM's. Recent developments in transconductance and pulse width, pulse height modulation design techniques have yielded multiplier modules which are internally trimmed for ease of application at a greatly reduced price. These multiplier and divider designs, which provide a new dimension in accuracy, speed and stability have not only gained wide acceptance as fundamental system building blocks, but they also are making feasible for the first time more complex circuit functions.
For 1975, Analog Devices offers a comprehensive selection of multiplier/divider modules for a wide range of applications. Fourteen models are available with performance characteristics ranging from complete $1 \%$ monolithic multiplier/dividers (AD532) to models with accuracies from $0.1 \%$ to $0.2 \%$, wide bandwidths to 10 MHz and low error drifts to $0.01 \% /{ }^{\circ} \mathrm{C}$.
With these models, Analog Devices offers the broadest multiplier/divider product line available. Our continuing development program will further expand the range of price and performance alternatives for your applications.
Analog Devices has available a "Nonlinear Circuits Handbook" which combines information on principles, circuitry, performance, specifications, testing and application of the class of devices specially designed to be purchased for use in nonlinear applications. This Handbook provides invaluable, definitive engineering examples which will enable the designer to use Analog Devices' function modules to optimum advantage.

## APPLICATIONS FOR MULTIPLIERS/DIVIDERS

Multiplier/divider modules are highly versatile in their application. They can be utilized to develop the following circuit functions:

- Squarer
- RMS Circuit
- Phase Sensitive

Demodulator

- Modulator
- Phase Locked Loops
- Square Root
- AGC Circuit
- Vector Transformation
- Correlator
- Voltage Controlled Filter

In each particular application, there is usually a dominant and a secondary parameter which influence multiplier choice. For low frequency applications (DC to audio), which is by far the most common application class, overall accuracy and drift are key parameters. At frequencies beyond 100 kHz , feedthrough and nonlinearity terms are key.
Since all multipliers from Analog Devices operate over four quadrants, signal polarity restrictions may be ignored. For divider and square root circuits, signal polarity and magnitude restrictions are placed on the inputs with operation restricted to two quadrants. Dividers also are subject to reduced accuracy and bandwidth because of the basic feedback circuit configuration: If the best performance is required for the divider, high accuracy multipliers are usually specified.
In general, each multiplier/divider requirement should be carefully studied to ascertain which features are critical and where tradeoffs may be made to assure best price/ performance. The following discussion is intended to assist the user in choosing the best multiplier/divider for his application, whether he be expert or newcomer in the use and selection of these devices.
For customer convenience, a selection guide for multipliers by key parameter, is listed below. The relevant model descriptions and specifications follow this section.

APPLICATION GUIDE BY KEY FEATURE

| Key Feature | Multiplier Application | Multiplier Model |
| :---: | :---: | :---: |
| Highest precision, lowest noise \& drift | Analog computation, dividers, servo multipliers, correlators | 424, 427, 435, 436 |
| Low drift, good accuracy, lower cost | Wide temperature range, general purpose multiply/divide | 428, AD530, AD5 33 |
| Bandwidth, accuracy | Graphic displays, dividers | 429, 422 |
| Wide dynamic divide range, accuracy | Root and power generation | 433, 434, 436 |
| External trim for accuracy | R \& D, medical, laboratory, analog computation | 424, 425, 435 |
| Economy, size | OEM designs, general purpose AD530 multiply/divide | 426, 432, AD531, AD5 32, AD5 33 |
| MIL spec. available | Military grade design AD530, | AD531, 432, 428, AD532, AD5 33 |

## CIRCUIT TECHNIQUES FOR DEVELOPING MULTIPLIERS

In discussing multiplier selection, it is appropriate to review several of the more popular circuit techniques used with today's solid state multipliers. A comparison table of these alternate techniques is presented below highlighting their respective capabilities in five key performance areas multiplier accuracy, stability, offset drift, bandwidth and slew rate.
As with most designs, the choice of circuit technique essentially determines the performance range of the multiplier in each of the five specification areas. The user should carefully review these criteria to assure the best device for the job.
TRANSCONDUCTANCE MULTIPLIERS exploit a useful property of the bipolar transistor: namely, that the forward collector current and the transconductance are linearly related. In most designs, the $\mathbf{X}$ signal is internally attenuated to a low level, and applied to the base of a transistor, and the $Y$ signal linearly modulates the value of a current source producing $I_{c}$, and thereby modulates the transconductance of the transistor. The result is a signal proportional to the product $\mathrm{X} \cdot \mathrm{Y}$.
These multipliers can be made to exhibit good accuracy and bandwidth, are low in cost, and well suited to most applications. Only wide temperature range and extreme stability requirements can displace this technique in favor of some alternate.
PULSE-WIDTH/AMPLITUDE MODULATION MULTIPLIERS are often called "averaging" multipliers, because the output is the average value of a pulse whose amplitude is modulated by X, and whose "ON" time (width, or duty-cycle) is modulated by Y . The average of such a pulse is proportional to the $\mathrm{X} \circ \mathrm{Y}$ product. By making the pulse-repetition (carrier)
frequency high, the averaging time may be shortened to permit remarkably fast response.
These multipliers are exceptionally accurate and stable, and reasonably fast. While not as low in cost as the transconductance type, they are significantly superior for applications demanding the best accuracy attainable, over a wide temperature variation.

## PIECEWISE-LINEAR APPROXIMATION (QUARTER-

SQUARE) MULTIPLIERS: This class of multipliers uses biased-diode and resistor networks to generate approximate square-law responses to the sum and difference of the $\mathbf{X}$ and $Y$ inputs, and then a fairly complex (and expensive) operational amplifier circuit to calculate the $\mathrm{X}-\mathrm{Y}$ product as follows:

$$
E_{o}=\frac{1}{K}\left[\left(\frac{X+Y}{2}\right)^{2}-\left(\frac{X-Y}{2}\right)^{2}\right]
$$

Unfortunately, the approximations involved in the squaring operations cause a "lumpy" error characteristic, and (even more unfortunately) cause "glitches" at the diode breakpoints, which severely limit the usefulness of these multipliers in many applications. Frequency response and accuracy can be good, but only at fairly high intrinsic cost . . . and this circuit must be classified as approaching obsolescence.
TRIANGLE-AVERAGING MULTIPLIERS: These circuits are very similar to pulse-width/height-modulated multipliers, but do not quite attain the accuracy or stability of the pulse averaging technique. Usually, they provide somewhat inferior performance to the pulse-averaging multipliers, at the same cost. (Some advanced transconductance multipliers will actually perform as well, at lower cost.) A recommended lower cost equivalent is the model 428 multiplier. This transconductance design combines good drift and linearity characteristics over wide signal ranges.

COMPARATIVE CHARACTERISTICS OF MULTIPLIER AND DIVIDER TYPES \& CLASSES

| Type | Performance Class (See Note) | Maximum Error, \% of F.S. | Accuracy <br> Stability | Offset Stability | $\begin{gathered} \text { Bandwidth } \\ (-3 \mathrm{~dB}, \text { Small Signal }) \end{gathered}$ | Slewing Rate | Recommended ADI Models | Additional Notes |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Transconductance | Moderate Accuracy \& Bandwidth | 1\%, 2\% | $0.04 \%{ }^{\circ} \mathrm{C}$ | $2 \mathrm{mV} /{ }^{\circ} \mathrm{C}$ | 400 kHz | $5 \mathrm{~V} / \mathrm{\mu sec}$ | $\begin{gathered} 426,432 \\ \text { AD530, AD531 } \\ \text { AD5 32, AD533 } \end{gathered}$ | General purpose. <br> Lowest cost. |
|  | High Accuracy, Moderate Bandwidth | 0.5\% | 0.02\% ${ }^{\circ} \mathrm{C}$ | $200 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | 300 kHz | $5 \mathrm{~V} / \mu \mathrm{sec}$ | $\begin{gathered} 428 \\ \text { AD530L, AD531L } \end{gathered}$ | Maintains $1 \%$ max. error over $\pm 25^{\circ} \mathrm{C}$ temperature range. |
|  | High Accuracy Fast Slew Rate | $\begin{aligned} & 0.25 \%, \\ & 0.1 \% \end{aligned}$ | $0.01 \%{ }^{\circ} \mathrm{C}$ | $\begin{aligned} & 0.3 \mathrm{mV} /{ }^{\circ} \mathrm{C}, \\ & 0.2 \mathrm{mV} /{ }^{\circ} \mathrm{C} \end{aligned}$ | 300 kHz | 2V/usec | 435 | High Accuracy and wide bandwidth. |
|  | High Accuracy 2-Quadrant Divider | $\begin{aligned} & 0.5 \%, \\ & 0.25 \% \end{aligned}$ | $0.01 \%{ }^{\circ} \mathrm{C}$ | $0.5 \mathrm{mV} /{ }^{\circ} \mathrm{C}$ | 300 kHz | 2V/usec | 436 | Most Accurate Divider |
|  | High Accuracy Wideband | 0.5\% | 0.04\% $/{ }^{\circ} \mathrm{C}$ | $1 \mathrm{mV} /{ }^{\circ} \mathrm{C}$ | 10 MHz | 120V/ $/$ sec | 429 | Fastest of any type |
| Pulse-Width/ Height | High Accuracy Very Slow Response | 0.1\% | 0.02\% $/{ }^{\circ} \mathrm{C}$ | $100 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $100 \mathrm{~Hz}$ $1 \mathrm{kHz}$ | $\begin{gathered} \hline 0.6 \mathrm{~V} / \mathrm{msec} \\ \text { to } \\ 6 \mathrm{~V} / \mathrm{msec} \end{gathered}$ | Substitute <br> ADI 427 | Low bandwidth restricts use to "DC." Lowest T.C. of all. |
| Averaging | High Accuracy, <br> Moderate <br> Bandwidth | 0.1\% | 0.02\% ${ }^{\circ} \mathrm{C}$ | $150 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | 100 kHz | $3 \mathrm{~V} / \mu \mathrm{sec}$ | $\begin{gathered} 424,425 \\ 427 \end{gathered}$ | Best for high-accuracy dynamic computing |
| PiecewiseLinear Approx. | High Accuracy Wide Bandwidth | 0.25\% | $0.05 \%{ }^{\circ} \mathrm{C}$ | $500 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | 1 MHz | $2 \mathrm{~V} / \mu \mathrm{sec}$ | Substitute <br> ADI 427 | Pulse-width type offers better accuracy and T.C. for bandwidths to 100 kHz . |
| Triangle Averaging | High Accuracy Slow Response | 0.5\% | 0.03\% ${ }^{\circ} \mathrm{C}$ | $200 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | 1 kHz | 5V/msec | Substitute ADI 428 | Replaced by high-accuracy transconductance |

[^17]
## MULTIPLIER CIRCUIT

In theory, a multiplier has an output which is ideally the product of two input variables, X and Y . However, the practical multiplier is subject to various offset errors and nonlinearities which must be accounted for in its application. The discussion below is intended to assist the designer in understanding and interpreting multiplier specifications and to offer him insight into its operation.
In practice, the multiplier is designed in two parts, one of which contains a multiplying cell, M, whose output feeds into a gain conditioning op amp, A. Also summed at the op amp input is the variable, $Z$, which is used as an input in the divide mode. Z is normally connected to the output during multiplication. To divide, Z and X become inputs and Y is tied to the output. Shown below is a practical multiplier illustrating both offset and nonlinear components, (Figure 1). Although the circuit details are quite sophisticated, the concept and block diagram are reasonably straightforward. The basic equation for the multiplier, including offsets $\left(\mathrm{X}_{\mathrm{O}}, \mathrm{Y}_{\mathrm{O}}, \mathrm{Z}_{\mathrm{O}}\right.$ ) and nonlinearity ( $\mathrm{F}[\mathrm{X}, \mathrm{Y}]$ ) is given here. Multiplier specifications may be readily interpreted from this expression and are described below.

ESTIMATING SMALL-SIGNAL MULTIPLIER ERRORS After all the adjustments have been made, multipliers have an irreducible error called "nonlinearity," a function of both $x$ and $y,[f(x, y)]$. In general, it is small near zero and increases rapidly near full scale. By taking advantage of nonlinearity specifications on the data sheet, you can often use a less-costly multiplier to obtain adequate small-signal
accuracy, and you can determine which input to use for best accuracy, if one of the input signals has a small range of variation.
This is done by using the approximation:
$\mathrm{f}(\mathrm{x}, \mathrm{y}) \cong|\mathrm{x}| \epsilon_{\mathrm{x}}+|\mathrm{y}| \epsilon_{\mathrm{y}}$, where $\epsilon_{\mathrm{x}}$ and $\epsilon_{\mathrm{y}}$ are the fractional nonlinearities specified for the x and y inputs
EXAMPLE: For Model 426, $\epsilon_{\mathrm{x}}=0.6 \%, \epsilon_{\mathrm{y}}=0.3 \%$. What maximum error can one expect for $x=5 \mathrm{~V}, \mathrm{y}=1 \mathrm{~V}$ ? Can one get less by interchanging inputs?

1. Nominal output is $x y / 10=(5)(1) / 10=500 \mathrm{mV}$
2. Expected error is $(5)(0.006)+(1)(0.003)=$ $33 \mathrm{mV}, 6.6 \%$ of output ( $0.33 \%$ F.S.)
3. Interchanging inputs, (1) $(0.006)+(5)(0.003)=$ $21 \mathrm{mV}, 4.2 \%$ of output ( $0.21 \%$ F.S.)
Compare this with the overly-conservative error predicted by the overall $1 \%$ of full scale specification: 100 mV , or $20 \%$ of output.

## DIVIDER CIRCUIT

High accuracy multipliers are recommended for divider operation because of their high linearity and low drift, which become critical in the divide mode since these errors are inversely dependent on denominator, X , as expressed in the equation here. The multiplier of Figure 1 is shown connected as a divider, in Figure 2.
$\mathrm{E}_{\mathrm{NL}}$ and $\epsilon_{\mathrm{d}}$, described previously as $\mathrm{F}(\mathrm{X}, \mathrm{Y})$ and offset error drift, appear at the output of the multiplier cell, M. With $X$ at full scale, the output divider error is the same as that of the multiplier for full scale outputs. However, as X decreases, divider errors (and noise to a lesser extent) increase inversely with amplitude which severely limits its useful dynamic range. Bandwidths vary directly with divisor, X , since the multiplier appears as a variable resistor in parallel with roll-off capacitor, C.


Figure 1


Figure 2

OFFSET AND OFFSET DRIFT: Output offset is the output voltage observed when $\mathrm{X}=\mathrm{Y}=0$ :

$$
\mathrm{E}_{\mathrm{OS}}=\left.\mathrm{E}_{\mathrm{O}}\right|_{\mathrm{X}=\mathrm{Y}=0}
$$



NOISE is specified and measured with both inputs at zero signal and zero impedance (i.e., shorted). For low frequency applications, filtering the output of the multiplier may improve small signal resolution significantly.
FEEDTHROUGH: Assume now that both inputs are at zero, and the output offset is trimmed to zero. Ideally, the output should remain at zero even if only one of either input is at zero. In fact, it should not matter what the value of the non-zero input signal is, within ratings; the product of that signal and zero should yield zero output (Figure A). In practical multipliers, however, there is always a small but finite output error under these conditions, and this output is called the feedthrough. If we set $\mathrm{X}=0$, and measure the Y-channel feedthrough at, say, $\mathrm{Y}=20 \mathrm{~V}$ p-p, we define Y feedthrough offset as:

$$
E_{F Y}=\left.E_{O}\right|_{\left\lvert\, \begin{array}{l}
X=0 \\
Y=20 V ~ p-p, 50 H z \tag{1}
\end{array}\right.}
$$

Now, for $\mathrm{Y}=0$, there is an analogous X-channel feedthrough.

$$
E_{F X}=\left.E_{o}\right|_{Y=0} ^{Y} \begin{align*}
& X=20 \mathrm{Vp}-\mathrm{p}, 50 \mathrm{~Hz} \tag{2}
\end{align*}
$$



Figure $A$


Y-Channel ac feedthrough
Figure B

NONLINEARITY: While errors due to output offset, feedthrough and scale factor can be substantially reduced by internal (and external) adjustments, nonlinearity remains as a basic, irreducible limitation to achievable accuracy. Nonlinearity is measured by applying a full scale DC signal to one input and a low frequency sine wave with full scale peak-topeak amplitude to the other. The AC output is then nulled against the AC input and the Scale Factor is adjusted for minimum error voltage. The residual peak-to-peak error voltage is then a measure of nonlinearity referred to a best straight line. This method of measuring and defining nonlinearity includes the nonlinear terms of the transfer function as well as the feedthrough functions.

GAIN ERRORS: The overall gain of the multiplier is not constant for any combination of inputs, therefore, we must expect a scale-factor error, $\mathrm{B} \approx 1$, which can be trimmed to unity. Gain, in general, also varies with time, temperature, power supply voltage, signal level (nonlinearity) and, most significant, with frequency. Except in the most critical applications, the only gain error of any consequence is usually that caused by bandwidth. Also associated with gain error is a phase lag at the output. Note also that slewing rate errors (inability to "track" large, rapid output changes) limit the response time on full scale changes in output.

SLEW RATE BEHAVIOR


MULTIPLIER ACCURACY: As one measure of product performance, Analog Devices has chosen to combine all error contributions in one multiplier specification, multiplier output error. This error is the deviation of actual value from predicted value of the multiplier output voltage. It is given as a percentage of full scale output, $\pm 10 \mathrm{~V}$, at a specified ambient temperature, $+25^{\circ} \mathrm{C}$, and it includes scale-factor error, offset, nonlinearity and feedthrough terms combined. Therefore, because these factors have been accounted for in the overall error specifications, it is important not to duplicate these terms in your calculations when developing an error budget. Note that overall accuracy is specified, which due to error cancellation is usually less than the rms sum of its constituents. To account for temperature variations in overall error, add to the basic error term above the specified accuracy drift.

# MULTIPLIERS/DIVIDERS MODELS 435, 428, 436, 429, 422, 426, 432, AD530, AD53I, AD532, AD533, 427, 424, 425 

## MULTIPLIER CLASSIFICATION AND PRODUCT DESCRIPTION

To assist in selecting the best multiplier for the application, we have classified products according to the technique used to develop the multiply function which essentially determines the capabilities of the device. Analog Devices has focused on the pulse-width/height technique and the variable transconductance technique to develop the multiply/divide function. These two approaches are considered complementary and were selected because of their inherent ability to provide a good balance between performance and cost.

## VARIABLE TRANSCONDUCTANCE TYPES

The popular variable transconductance technique complements the PWH approach and should be considered whenever wider bandwidths, to 10 MHz , are required along with lower costs and good overall performance. Both discrete and monolithic devices are available using this design approach.
Multiplier specifications include accuracies from $0.1 \%$ to $2 \%$, bandwidths from 300 kHz to 10 MHz and drifts from $200 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ to $2 \mathrm{mV} /{ }^{\circ} \mathrm{C}$. Each model is capable of 4 -quadrant multiplication, or 2 -quadrant division. Because the transconductance technique can be optimized in different ways to yield highly specialized performance, models may be classified as: general purpose (models 426, 432, 530 and 531 ; high performance (models 435,428 ); and wide bandwidth (models 429 and 422).

## High Performance

MODEL 435 (HIGH ACCURACY, LOW DRIFT): The model 435 combines the high accuracy of pulse-width type multipliers with the bandwidth and low cost of transconductance designs. Models 435 J and 435 K offer factory trimmed accuracy to within $0.25 \%$ and $0.1 \%$ respectively together with a 300 kHz small signal bandwidth ( -3 dB ). Optional trimming may be used to further improve accuracy, typically by a factor of two. Very low output offset drift of only $0.002 \% /{ }^{\circ} \mathrm{C} \max (435 \mathrm{~K})$ insures high precision performance over a wide temperature range.
The superb operating specifications of model 435 make it ideally suited for use as a precision divider, squarer or square rooter. Model 435 finds use in such applications as phase detection, power measurement and automatic gain control.


Model 435 K also features low nonlinearity ( $0.05 \% \max$ ) and feedthrough ( $10 \mathrm{mV} \mathrm{p}-\mathrm{p}$ ). Both the 435 J and 435 K provide excellent noise performance of 1 mV rms in a bandwidth of 10 Hz to 10 kHz .
In addition, model 435 provides a unique scale factor (gain) adjustment control which permits the user to easily compensate for system errors. The external scale factor (gain) pot provides an adjustment range of at least $\pm 1 \%$ and may be located away from the 435 module for operator convenience.

MODEL 428: (LOW DRIFT): This device meets high performance requirements for many applications where component price and accuracy are key factors. As a transconductance multiplier, it approaches the performance of more expensive multipliers, using modulation techniques, but at lower costs. Factory trimmed to $0.5 \%$ with offset drift of $200 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, enables model 428 K to operate over a $50^{\circ} \mathrm{C}$ temperature range with less than $1 \%$ error increase.
Both 428 J and 428 K may be externally trimmed for an improved accuracy of $0.25 \%$ and operated as dividers and square root circuits. The nonlinearity component of error is particularly low in this unit, resulting in excellent performance as a divider. For example: 50 mV maximum error for a 10:1 dynamic range of denominator.
In addition to its excellent DC performance, it has 300 kHz small signal bandwidth ( -3 dB ) and full power output to beyond 70 kHz , considerably exceeding the audio range.

## MODEL 436 (HIGH ACCURACY TWO-QUADRANT DIVIDER)

 Model 436 is a precision, two quadrant, analog divider featuring guaranteed accuracy of $\pm 0.5 \%$ (model 436 A ) and $\pm 0.25 \%$ (model 436B) over 100:1 denominator signal range $(+100 \mathrm{mV}$ to +10 V ) with no external adjustments. Model 436 may be plugged into existing sockets using expensive precision PWH type multipliers to improve accuracy over a wider dynamic range. Complete discussion of the 436 specifications is available in the divider section on page 168 .
## Wideband

MODEL 429 (HIGH ACCURACY): This unit should be considered for all new multiplier/divider designs requiring the best possible speed, drift and accuracy performance. The model 429 factory trimmed, is available as a $429 \mathrm{~A}(1 \%$, $2 \mathrm{mV} /{ }^{\circ} \mathrm{C}$ ) and 429B( $0.5 \%, 1 \mathrm{mV} /{ }^{\circ} \mathrm{C}$ ) both with 10 MHz response. Capable of multiplying or dividing, models 429 A/B may be easily converted to the divide mode with external pin interconnections. Accuracies may be improved upon for models 429A (from 1\% to 0.7\%) and 429B (from $0.5 \%$ to $0.3 \%$ ) with external trimming. Note, that although model 429 is an improvement over model 422, these devices are not pin compatible.

MODEL 422 (HIGH FREQUENCY): This unit is available as a $1 \%$ multiplier with a 5 MHz bandwidth, and may be operated as a divider when connected with an external op amp. Model 422 A and 422 K , with $2 \mathrm{mV} /{ }^{\circ} \mathrm{C}$ and $1 \mathrm{mV} /{ }^{\circ} \dot{\mathrm{C}}$ offset drifts respectively, may be externally trimmed for $0.7 \%$ accuracy to improve on the $1 \%$ factory trimmed specification.

## General Purpose

MODEL 426 (GENERAL PURPOSE 1\%, 0.5\%): Available as an internally trimmed $1 \%(\mathrm{~J}, \mathrm{~K})$ or $0.5 \%(\mathrm{~L})$ accurate multiplier/divider, Model 426 should be considered as a first choice for most general purpose designs and OEM applications. External trimming further improves performance to $0.6 \%(\mathrm{~J}, \mathrm{~K})$ and $0.35 \%(\mathrm{~L})$. Nonlinearities are held to a low $0.6 \%(\mathrm{X})$ and $0.3 \%(\mathrm{Y})$ for models $426(\mathrm{~J} \& \mathrm{~K})$, allowing the user to assign that input signal with the widest dynamic range to the $0.3 \%(\mathrm{Y})$ input terminal for better accuracy. For even better performance, model 426 L should be selected for lowest drift and good linearity and feedthrough characteristics.
MODEL 432 (ECONOMY): Using hermetically sealed components, the models $432 \mathrm{~J}(\mathrm{~K}), 2 \%(1 \%)$ multiplier/ dividers, are internally trimmed and are available in a compact package for low cost OEM applications requiring field interchangeable modules with no additional trimming. External trimming will improve accuracy from $2 \%(1 \%)$ to $1 \%(0.6 \%)$. Performance, reliability and bandwidth are comparable to model 530. OEM discounts are available.

MODEL AD530 (MONOLITHIC): With the transfer function $\mathrm{XY} / 10$, the AD530 is the first IC multiplier/divider to include the transconductance multiplying element, the built-in reference and the output op amp all on the same chip. Available in both industrial (AD530 J, K or L) and military grades (AD530S), its compact package and good performance make it an ideal choice for high reliability assignments. The AD530 needs only four trim pots to achieve accuracies to $\pm 0.5 \%$ of full scale. Bandwidth is 1 MHz and slew rate $45 \mathrm{~V} / \mu \mathrm{sec}$. The AD5 30 is available in both the TO-100 metal can and TO-116 ceramic dual-in-line packages.

## MODEL AD531 (MONOLITHIC): TRANSFER FUNCTION

( $X_{1}-X_{2}$ )Y/Z. Not just a multiplier, the AD5 31 is truly a computation circuit that is ideally suited to such applications as AGC, True rms-to-DC conversion, ratio determination, absolute value and vector computation. Like the AD5 30, the AD531 combines the transconductance element, a precision stable reference and the output op amp on a single monolithic structure. Flexibility of operation is achieved by virtue of the programmable scale factor capability and the differential input feature. In addition to verification of accuracy at $+25^{\circ} \mathrm{C}$, the AD531L and AD531S are further tested for maximum error limits of $\pm 1.5 \%$ and $\pm 3.0 \%$, respectively, at their extreme operating temperature limits. The AD5 31 is available in the TO-116 ceramic dual-in-line package.
MODEL AD532 (MONOLITHIC-INTERNALLY TRIMMED): TRANSFER FUNCTION $\left(X_{1}-X_{2}\right)\left(Y_{1}-Y_{2}\right) / 10$. The AD532J, AD5 32 K and AD532S are the industry's first internally-trimmed monolithic multiplier/dividers. They guarantee maximum multiplying errors of $\pm 2.0 \%, \pm 1.0 \%$ and $\pm 1.0 \%$ of full scale $(10 \mathrm{~V})$ at $+25^{\circ} \mathrm{C}$, respectively, without the need for any external trim networks or output op amp. In addition, the differential X and Y inputs provide significant operating flexibility for both algebraic computation and transducer instrumentation applications. Further, the AD5 32 can be used as a direct replacement for some popular IC multipliers that require external trimming, such as the AD530. The AD532J and AD5 32 K are rated for operation from 0 to $+70^{\circ} \mathrm{C}$. The AD532S will operate from $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ with a maximum multiplying error of $\pm 4.0 \%$ of full scale. All designs are available in both the TO-100 metal can and the TO116 ceramic dual-in-line packages.
MODEL AD533 (MONOLITHIC): TRANSFER FUNCTION $X Y / 10$. Where cost is a factor, the AD5 33 offers the user an IC multiplier/divider with $2.0 \%$ accuracy ( J ) at a price as low as $\$ 5.95$ in 100's. Like it predecessor, the AD530, the AD533 includes the transconductance multiplying element, built-in reference and output op amp on one chip. One percent and half percent versions ( K and L respectively) are available as well as a MIL version (S) specified from $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$. All versions of this low cost device come in either the TO-100 metal can or the TO-116 CER DIP.

## PULSE-WIDTH-HEIGHT MODULATION PRECISION MULTIPLIERS (PWH)

The pulse-width-height modulation technique is capable of producing multipliers of the highest precision. Typical specifications include accuracies from $0.1 \%$ to $0.25 \%$, offset drifts to $100 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, output noise of $50 \mu \mathrm{~V}$ rms and bandwidths to 100 kHz . Multipliers in this group should be used for wide temperature range applications, for analog computing elements, for dividers because of their inherently good drift, noise and low non-linearities, and, in general, for exacting multiplier/divider applications where wide dynamic signal swings are anticipated. Products in this group include models 427. 424, and 425.
MODEL 427 (HIGH ACCURACY): Based on the highly successful Model 424 , the 427 K is internally trimmed to specified accuracy and requires no external adjustments for multiplication. It uses pulse-width modulation to obtain accuracies to $0.2 \%$ (FS), offset drifts as low as $200 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, and nonlinearity of $0.04 \%$ maximum, for both inputs. All semiconductors used in this design are hermetically sealed.

Unlike most high accuracy multipliers embodying the modulation principle, 427's high carrier frequency allows a bandwidth rating of 100 kHz for -3 dB response with no carrier ripple on output. Depending on how it is connected, the 427 can be used for multiplying, dividing, squaring, or square rooting.
The true capability of a multiplier can be best demonstrated when the unit is used in the divide mode, particularly with small denominators. Because the 427 features excellent small signal linearity, the errors are very much smaller than one would predict using $10 / \mathrm{x}$ for divider error.
MODEL 424 (HIGH ACCURACY): The model $424 \mathrm{~J} / \mathrm{K}$ is an untrimmed multiply-only module with performance comparable to that of model 427. In every respect, except for the divide and external trim features, the 424 will perform the 427 task at lower component cost and should be considered for laboratory and industrial applications where external trimming may be conveniently performed to achieve the highest possible accuracies. When externally trimmed, model 424 will perform with $0.2 \%(424 \mathrm{~J})$ and $0.1 \%(424 \mathrm{~K})$ accuracies with bandwidths to $100 \mathrm{kHz}(-3 \mathrm{~dB})$. It may be used to perform division when operated with an external op amp.
MODEL 425: Customers may purchase the model 424 mounted on a PC card which contains all necessary adjustment potentiometers to trim the multiplier to its rated accuracies. Designated model 425 J (with 424 J ) and 425 K (with 424 K ), these models are factory trimmed and offered at a nominal cost above that of 424 alone.


Figure 1. Multiplier Applications for Power and Energy Measurements

## MULTIPLIERS/DIVIDERS (Discrete)

SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ and $\pm 15 \mathrm{VDC}$ unless otherwise specified)

|  | VARIABLE TRANSCONDUCTANCE TYPES |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Models ${ }^{1}$ | Economy 432J (432K) | General Purpose 426A (426K) (426L) | $\begin{aligned} & \text { Wideband } \\ & \text { 422A (422K) } \end{aligned}$ | Accurate Wideband 429A (429B) |
| Full Scale Accuracy ${ }^{2}$ | 2\% (1\%) | 1\% (1\%) (0.5\%) | 1\% | 1\% (0.5\%) |
| Divides and Square Roots | YES | YES | Division requires external amp | YES |
| Multiplication Characteristics |  |  |  |  |
| Output Function | XY/10 | XY/10 | XY/10 | XY/10 |
| Error, Internal Trim ( $\pm$ ) | 2\% (1\%) max | 1\% (1\%) (0.5\%) max | 1\% (1\%) max | 1\% (0.5\%) max |
| Error, External Trim ( $\pm$ ) | 1.0\% (0.6\%) | 0.6\% (0.6\%) (0.35\%) | 0.7\% (0.7\%) | 0.7\% (0.3\%) |
| Accuracy vs. Temperature ( $\pm$ ) | $0.06 \% /{ }^{\circ} \mathrm{C}\left(0.04 \% /{ }^{\circ} \mathrm{C}\right)$ | $0.05 \% /{ }^{\circ} \mathrm{C}\left(0.04 \% /{ }^{\circ} \mathrm{C} \max \right)\left(0.04 \% /{ }^{\circ} \mathrm{C} \max \right)$ | $0.05 \% /{ }^{\circ} \mathrm{C}\left(0.04 \% /{ }^{\circ} \mathrm{C} \max \right)$ | $0.05 \% /{ }^{\circ} \mathrm{C}\left(0.04 \% /{ }^{\circ} \mathrm{C} \max \right)$ |
| Accuracy vs. Supply ( $\pm$ ) | 0.1\%/\% | 0.03\%/\% | 0.05\%/\% | 0.05\%/\% |
| Warm up Time to Specifications | 1 min | 1 sec | 1 sec | 1 sec |
| Output Offset ( $\pm$ ) |  |  |  |  |
| Initial | $20 \mathrm{mV}(25 \mathrm{mV}$ max) | 20 mV | 25 mV | $20 \mathrm{mV}(10 \mathrm{mV})$ max |
| Average vs. Temperature 0 to $+70^{\circ} \mathrm{C}$ | $2 \mathrm{mV} /{ }^{\circ} \mathrm{C}\left(1 \mathrm{mV} /{ }^{\circ} \mathrm{C}\right)$ | $2 \mathrm{mV} /{ }^{\circ} \mathrm{C}\left(1 \mathrm{mV} /{ }^{\circ} \mathrm{C} \max \right)\left(1 \mathrm{mV} /{ }^{\circ} \mathrm{C} \max \right)$ | $2 \mathrm{mV} /{ }^{\circ} \mathrm{C}\left(1 \mathrm{mV} /{ }^{\circ} \mathrm{C} \max \right)$ | $2 \mathrm{mV} /{ }^{\circ} \mathrm{C}\left(1 \mathrm{mV} /{ }^{\circ} \mathrm{C}\right.$ max $)$ |
| Average vs. Supply | $10 \mathrm{mV} / \mathrm{\%}$ | 2mV/\% | $1 \mathrm{mV} / \%$ | $1 \mathrm{mV} / \%$ |
| Scale Factor ( $\pm$ ) |  |  |  |  |
| Initial Error | 1\% (0.5\%) | 0.5\% (0.5\%) (0.25\%) | 0.5\% | 0.5\% (0.25\%) |
| Nonlinearity ( $\pm$ ) |  |  |  |  |
| X Input ( $\mathrm{X}=20 \mathrm{~V}$ p-p, $\mathrm{Y}= \pm 10 \mathrm{VDC}$ ) | 0.8\% (0.6\% max) | 0.6\% (0.6\%) (0.25\%) max | 0.6\% max | 0.5\% (0.2\%) max |
| Y Input ( $\mathrm{Y}=20 \mathrm{~V}$ p-p, $\mathrm{X}= \pm 10 \mathrm{VDC}$ ) | 0.4\% (0.3\% max) | 0.3\% (0.3\%) (0.25\%) max | 0.3\% max | 0.3\% (0.2\%) max |
| Feedthrough |  |  |  |  |
| $\begin{aligned} & \mathrm{X}=0, \mathrm{Y}=20 \mathrm{~V} \text { p-p } 50 \mathrm{~Hz} \\ & \text { with external trim } \end{aligned}$ | $\begin{gathered} 80 \mathrm{mV}(50 \mathrm{mV}) \mathrm{p}-\mathrm{p} \max \\ 30 \mathrm{mV} \text { p-p } \end{gathered}$ | $\begin{aligned} & 60 \mathrm{mV}(\underset{20 \mathrm{mV}}{(60 \mathrm{mV})(40 \mathrm{mV}) \mathrm{p}-\mathrm{p} \max } \\ & 20 \end{aligned}$ | $\begin{gathered} 50 \mathrm{mV} \text { p-p } \max \\ 8 \mathrm{mV} \text { p-p } \end{gathered}$ | $50 \mathrm{mV}(20 \mathrm{mV}) \text { p-p } \max$ $16 \mathrm{mV}(10 \mathrm{mV}) \mathrm{p}-\mathrm{p}$ |
| $\mathrm{Y}=0, \mathrm{X}=20 \mathrm{~V} \mathrm{p}-\mathrm{p} 50 \mathrm{~Hz}$ | 120 mV ( 100 mV ) p-p max | $100 \mathrm{mV}(100 \mathrm{mV})(40 \mathrm{mV}) \mathrm{p}-\mathrm{p} \max$ | 100 mV p-p max | 100 mV ( 30 mV ) p-p max |
| with external trim | N/A | $60 \mathrm{mV}(60 \mathrm{mV})(20 \mathrm{mV}) \mathrm{p}-\mathrm{p}$ | 35 mV p-p | 50 mV ( 20 mV ) p-p |
| Feedthrough vs. Temperature, each input | $1 \mathrm{mV} \mathrm{p-p/} /{ }^{\circ} \mathrm{C}$ | $2 \mathrm{mV} \mathrm{p-p/}{ }^{\circ} \mathrm{C}$ | $2 \mathrm{mV} \mathrm{p-p/} /{ }^{\circ} \mathrm{C}$ | $2 \mathrm{mV} \mathrm{p-p/} /{ }^{\circ} \mathrm{C}$ |
| Bandwidth |  |  |  |  |
| -3dB Small Signal | 1 MHz | 400 kHz | 5 MHz min | 10 MHz |
| Full Power Response | 700 kHz | 80 kHz | 2 MHz min | 2 MHz min |
| Slew Rate | $45 \mathrm{~V} / \mu \mathrm{sec}$ | $5 \mathrm{~V} / \mu \mathrm{sec}$ | $120 \mathrm{~V} / \mu \mathrm{sec} \mathrm{min}$ | $120 \mathrm{~V} / \mu \mathrm{sec} \mathrm{min}$ |
| Small Signal Amplitude Error ( $\pm$ ) | $1 \%$ @ 40 kHz | $1 \%$ at 40 kHz | $1 \%$ at 300 kHz min | $1 \%$ at 300 kHz min |
| Small Signal Vector Error ( $\pm$ ) | $1 \%$ @ 10 kHz | $1 \%$ at 10 kHz | $1 \%$ at 50 kHz min | $1 \%$ at 50 kHz min |
| Settling Time for $\pm 10 \mathrm{~V}$ Step | $1 \mu \mathrm{sec}$ to $2 \%$ | $3 \mu \mathrm{sec}$ to 1\% | $0.4 \mu \mathrm{sec}$ to $1 \%$ | $0.5 \mu \mathrm{sec}$ to $1 \%$ |
| Overload Recovery | $3 \mu \mathrm{sec}$ | $3 \mu \mathrm{sec}$ | $0.15 \mu \mathrm{sec}$ | $0.15 \mu \mathrm{sec}$ |
| Output Noise |  |  |  |  |
| 5 Hz to 10 kHz | $600 \mu \mathrm{~V}$ rms | $500 \mu \mathrm{~V}$ rms | $500 \mu \mathrm{~V}$ rms | $200 \mu \mathrm{~V}$ rms |
| 5 Hz to 5 MHz | 3 mV rms | 2.5 mV rms | 2.5 mV rms | 1.5 mV rms |
| Output Characteristics ${ }^{4}$ |  |  |  |  |
| Voltage at Rated Load (min) | $\pm 10 \mathrm{~V}$ | $\pm 11 \mathrm{~V}$ | $\pm 11 \mathrm{~V}$ | $\pm 11 \mathrm{~V}$ |
| Current (min) | $\pm 5 \mathrm{~mA}$ | $\pm 11 \mathrm{~mA}$ | $\pm 11 \mathrm{~mA}$ | $\pm 11 \mathrm{~mA}$ |
| Load Capacitance Limit | $0.001 \mu \mathrm{~F}$ | $1 \mu \mathrm{~F}$ | $0.01 \mu \mathrm{~F}$ | $0.01 \mu \mathrm{~F}$ |
| Input Resistance |  |  |  |  |
| X/Y/Z Input | $10 \mathrm{M} \Omega / 10 \mathrm{k} \Omega / 36 \mathrm{k} \Omega$ | $25 \mathrm{k} \Omega / 25 \mathrm{k} \Omega / 200 \mathrm{k} \Omega$ | $10 \mathrm{k} \Omega / 11 \mathrm{k} \Omega / \mathrm{N} / \mathrm{A}$ | $10 \mathrm{k} \Omega / 11 \mathrm{k} \Omega / 13 \mathrm{k} \Omega$ |
| Input Bias Current |  |  |  |  |
| X/Y/Z Input | $2 \mu \mathrm{~A}$ each | $+100 \mathrm{nA} /+100 \mathrm{nA} /-50 \mu \mathrm{~A}$ | +100 nA each | $+100 \mathrm{nA} /+100 \mathrm{nA} / \pm 40 \mathrm{nA}$ |
| Maximum Input Voltage |  |  |  |  |
| For Rated Accuracy | $\pm 10.1 \mathrm{~V}$ | $\pm 10.5 \mathrm{~V}$ | $\pm 10.5 \mathrm{~V}$ | $\pm 10.5 \mathrm{~V}$ |
| Safe Level | $\pm \mathrm{V}_{\text {S }}$ | $\pm 18 \mathrm{~V}$ | $\pm 16 \mathrm{~V}$ | $\pm 16 \mathrm{~V}$ |
| Power Supply ( $\mathrm{V}_{\mathrm{s}}$ ) |  |  |  |  |
| Rated Performance | $\pm 15 \mathrm{~V}$ | $\pm 14.7$ to $\pm 15.3 \mathrm{~V}$ | $\pm 14.7$ to $\pm 15.3 \mathrm{~V}$ | $\pm 14.7$ to $\pm 15.3 \mathrm{~V}$ |
| Operating | $\pm 12$ to $\pm 18 \mathrm{~V}$ | $\pm 11.5$ to $\pm 18 \mathrm{~V}$ | $\pm 14$ to $\pm 16 \mathrm{~V}$ | $\pm 14$ to $\pm 16 \mathrm{~V}$ |
| Quiescent Current | $\pm 4.5 \mathrm{~mA}$ | $\pm 5 \mathrm{~mA}$ | $\pm 12 \mathrm{~mA}$ | $\pm 12 \mathrm{~mA}$ |
| Temperature Range |  |  |  |  |
| Rated Performance |  | -25 to $+85^{\circ} \mathrm{C}\left(0\right.$ to $\left.+70^{\circ} \mathrm{C}\right)\left(0\right.$ to $\left.+70^{\circ} \mathrm{C}\right)$ | $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}\left(0\right.$ to $\left.+70^{\circ} \mathrm{C}\right)$ | $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |
| Operating | $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |
| Storage | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| Package Outline | QC-2 | FA-4 | F-8 | FA-4 |
| Case Dimensions | $1.1^{\prime \prime} \times 1.1^{\prime \prime} \times 0.4{ }^{\prime \prime}$ | $1.5{ }^{\prime \prime} \times 1.5^{\prime \prime} \times 0.6^{\prime \prime}$ | $1.5^{\prime \prime} \times 1.5^{\prime \prime} \times 0.6{ }^{\prime \prime}$ | $1.5^{\prime \prime} \times 1.5^{\prime \prime} \times 0.6^{\prime \prime}$ |
| mm | $(27.9 \times 27.9 \times 10.1)$ | (38.1 $\times 38.1 \times 15.2$ ) | ( $38.1 \times 38.1 \times 15.2$ ) | ( $38.1 \times 38.1 \times 15.2$ ) |
| Prices (1-9) | \$30 (\$46.50) | \$47.50(\$62)(\$68) | \$120(\$142) | \$109 (\$139) |
| (10-24) | \$28 (\$44.50) | \$45.00 (\$60) (\$65) | \$114 (\$131) | \$104 (\$129) |

## NOTES:

${ }^{1}$ Parentheses indicate specification for the high performance (K or L version) model of each multiplier when it differs from the $J$ or $A$ version. For example, order model 427J for $0.25 \%$ accuracy, model 427 K for $0.2 \%$ accuracy.
${ }^{2}$ All accuracy and error specifications, when expressed as percentages, refer to \% of full scale (10V)
${ }^{3}$ Model 424 available for $\$ 22$ additional on printed circuit board with preadjusted trim pots. Card socket supplied. Order model 425 J or 425 K .

|  |  |  | PRECISION (PWH) TYPES |  |
| :---: | :---: | :---: | :---: | :---: |
| Accurate Low Drift 428J (428K) | High Accuracy $435 \mathrm{~J}(435 \mathrm{~K})$ | High Accuracy 2-Quadrant Divider 436A (436B) | High Accuracy $424 \mathrm{~J}(424 \mathrm{~K}) 425^{3}$ | High Accuracy <br> 427J (427K) |
| 0.5\% | 0.25\% (0.1\%) | 0.5\% (0.25\%) | 0.2\% (0.1\%) | 0.25\% (0.2\%) |
| YES | YES | DIVIDE ONLY | Division requires external amp | YES |
| $\begin{gathered} \mathrm{XY} / 10 \\ 0.5 \%(0.5 \%) \max \\ 0.25 \%(0.25 \%) \\ 0.02 \% /{ }^{\circ} \mathrm{C}(\max ) \\ 0.02 \% / \% \\ 1 \mathrm{~min} \end{gathered}$ | $\begin{gathered} \mathrm{XY} / 10 \\ 0.25 \%(0.1 \%)_{\max } \\ 0.15 \%(0.08 \%) \\ 0.01 \% /^{\circ} \mathrm{C}\left(0.01 \% /^{\circ} \mathrm{C} \max \right) \\ 0.01 \% / \% \\ 5 \mathrm{~min} \end{gathered}$ | $\begin{gathered} 10 \mathrm{Z} / \mathrm{X} \\ 0.5 \%(0.25 \%) \max ^{5} \\ 0.3 \%(0.1 \%) \max ^{5} \\ 0.04 \% /{ }^{\circ} \mathrm{C}\left(0.02 \% /^{\circ} \mathrm{C}\right) \max \\ 0.02 \% / \% \\ 5 \mathrm{~min} \end{gathered}$ | $\begin{gathered} \text { XY/10 } \\ \text { Untrimmed } \\ 0.2 \%(0.1 \%)_{\max } \\ 0.02 \% /{ }^{\circ} \mathrm{C}(\max ) \\ 0.02 \% / \% \\ 1 \mathrm{~min} \end{gathered}$ | $\begin{gathered} \text { XY/10 } \\ 0.25 \%(0.2 \%) \max \\ 0.15 \%(0.1 \% \max ) \\ 0.02 \% /^{\circ} \mathrm{C} \max \\ 0.02 \% / \% \\ 1 \min \end{gathered}$ |
| $\begin{gathered} 10 \mathrm{mV} \\ 0.5 \mathrm{mV} /{ }^{\circ} \mathrm{C}\left(0.2 \mathrm{mV} /{ }^{\circ} \mathrm{C} \max \right) \\ 2 \mathrm{mV} / \% \end{gathered}$ | $\begin{gathered} 10 \mathrm{mV}(5 \mathrm{mV}) \max \\ 0.3 \mathrm{mV} /{ }^{\circ} \mathrm{C}\left(0.2 \mathrm{mV} /{ }^{\circ} \mathrm{C}\right) \max \\ 1 \mathrm{mV} / \% \end{gathered}$ | $\begin{gathered} 10 \mathrm{mV} \mathrm{~V}_{\mathrm{X}}=+10 \mathrm{~V} \\ 0.5 \mathrm{mV} /{ }^{\circ} \mathrm{C} \\ 50 \mu \mathrm{~V} / \% \end{gathered}$ | Adj. to zero $\begin{gathered} 0.2 \mathrm{mV} /{ }^{\circ} \mathrm{C}\left(0.2 \mathrm{mV} /{ }^{\circ} \mathrm{C} \max \right) \\ 2 \mathrm{mV} / \% \end{gathered}$ | $\begin{gathered} 5 \mathrm{mV} \\ 0.2 \mathrm{mV} /{ }^{\circ} \mathrm{C}\left(0.2 \mathrm{mV} /{ }^{\circ} \mathrm{C} \max \right) \\ 1 \mathrm{mV} / \% \end{gathered}$ |
| 0.25\% | 0.1\% (0.05\%) | 0.1\% | Adj. to 0.1\% (0.05\%) | 0.1\% (0.05\%) |
| $\begin{aligned} & 0.25 \% \max \\ & 0.25 \% \max \end{aligned}$ | 0.1\% (0.05\%) max $0.1 \%(0.05 \%)$ max | $\left[\begin{array}{c}0.1 \%(0.05 \%) \\ 0.1 \mathrm{~V} \leqslant \mathrm{~V}_{\mathrm{x}} \leqslant 10 \mathrm{~V}\end{array}\right]$ | $\begin{aligned} & 0.08 \%(0.04 \%) \max \\ & 0.08 \%(0.04 \%) \max \end{aligned}$ | $\begin{aligned} & 0.08 \%(0.04 \%) \max \\ & 0.08 \%(0.04 \%) \max \end{aligned}$ |
| $\begin{gathered} 40 \mathrm{mV} \text { p-p max } \\ 10 \mathrm{mV} \text { p-p } \\ 40 \mathrm{mV} \mathrm{p}-\mathrm{p} \max \\ 10 \mathrm{mV} \mathrm{p}-\mathrm{p} \\ 1 \mathrm{mV} \mathrm{p}-\mathrm{p} /{ }^{\mathrm{o}} \mathrm{C} \\ \hline \end{gathered}$ | $\qquad$ | $-$ | $\begin{gathered} \text { N/A } \\ 2 \mathrm{mV}(1 \mathrm{mV}) \mathrm{p}-\mathrm{p} \\ \mathrm{~N} / \mathrm{A} \\ 4 \mathrm{mV}(2 \mathrm{mV}) \mathrm{p}-\mathrm{p} \\ 0.2 \mathrm{mV} \mathrm{p}-\mathrm{p} /{ }^{\circ} \mathrm{C} \end{gathered}$ | $\begin{aligned} & 20 \mathrm{mV} \text { p-p max } \\ & 4 \mathrm{mV} \text { p-p } \\ & 20 \mathrm{mV} \text { p-p } \max \\ & 5 \mathrm{mV} \text { p-p } \\ & 0.2 \mathrm{mV} \text { p-p } /{ }^{\circ} \mathrm{C} \\ & \hline \end{aligned}$ |
| 300 kHz <br> 70 kHz <br> $4 \mathrm{~V} / \mu \mathrm{sec}$ <br> $1 \%$ at 40 kHz <br> $1 \%$ at 2 kHz <br> $5 \mu \mathrm{sec}$ to $0.5 \%$ <br> $3 \mu \mathrm{sec}$ | 300 kHz <br> 30 kHz <br> $2 \mathrm{~V} / \mu \mathrm{sec}$ $1 \%$ @ 40 kHz <br> $1 \%$ @ 3 kHz <br> $10 \mu \mathrm{sec}$ to $0.1 \%$ <br> $2 \mu \mathrm{sec}$ | $300 \mathrm{kHz}^{5}$ $30 \mathrm{kHz}^{5}$ $2 \mathrm{~V} / \mu \mathrm{sec}$ - - $10 \mu \mathrm{sec}$ to $0.5 \%$ $5 \mu \mathrm{sec}$ | 100 kHz 40 kHz $3 \mathrm{~V} / \mu \mathrm{sec}$ $0.1 \%$ at 4 kHz $1 \%$ at 700 Hz $15 \mu \mathrm{sec}$ to $0.1 \%$ $10 \mu \mathrm{sec}$ | 100 kHz 30 kHz $2 \mathrm{~V} / \mu \mathrm{sec}$ $0.1 \%$ at 4 kHz $1 \%$ at 700 Hz $20 \mu \mathrm{sec}$ to $0.1 \%$ $10 \mu \mathrm{sec}$ |
| $\begin{aligned} & 500 \mu \mathrm{~V} \mathrm{rms} \\ & 2.5 \mathrm{mV} \mathrm{rms} \end{aligned}$ | $\begin{gathered} 250 \mu \mathrm{~V} \mathrm{rms} \\ 1 \mathrm{mV} \mathrm{rms} \end{gathered}$ | $\left[\begin{array}{c} 750 \mu \mathrm{~V} \text { rms } \\ 10 \mathrm{~Hz} \text { to } 10 \mathrm{kHz}, \mathrm{~V}_{\mathrm{X}}=+10 \end{array}\right]$ | $\begin{aligned} & 50 \mu \mathrm{~V} \mathrm{rms} \\ & 1 \mathrm{mV} \mathrm{rms} \end{aligned}$ | $\begin{gathered} 50 \mu \mathrm{~V} \mathrm{rms} \\ 1 \mathrm{mV} \mathrm{rms} \end{gathered}$ |
| $\begin{gathered} \pm 11 \mathrm{~V} \\ \pm 11 \mathrm{~mA} \\ 0.001 \mu \mathrm{~F} \end{gathered}$ | $\begin{aligned} & \pm 10 \mathrm{~V} \\ & \pm 5 \mathrm{~mA} \\ & 0.01 \mu \mathrm{~F} \end{aligned}$ |  | $\begin{array}{r}  \pm 10 \mathrm{~V} \\ \pm 7 \mathrm{~mA} \\ 0.01 \mu \mathrm{~F} \end{array}$ | $\begin{gathered} \pm 10.2 \mathrm{~V} \\ \pm 7 \mathrm{~mA} \\ 0.01 \mu \mathrm{~F} \end{gathered}$ |
| $25 \mathrm{k} \Omega / 25 \mathrm{k} \Omega / 200 \mathrm{k} \Omega$ | $100 \mathrm{k} \Omega / 100 \mathrm{k} \Omega / 70 \mathrm{k} \Omega$ | $25 \mathrm{k} \Omega, \mathrm{X} / 9 \mathrm{k} \Omega \mathrm{Z}$ | $10 \mathrm{k} \Omega / 11 \mathrm{k} \Omega / \mathrm{N} / \mathrm{A}$ | $10 \mathrm{k} \Omega / 10 \mathrm{k} \Omega / 33 \mathrm{k} \Omega$ |
| $+100 \mathrm{nA} /+100 \mathrm{nA} /-50 \mu \mathrm{~A}$ | $50 \mathrm{nA} / 100 \mathrm{nA} / 70 \mu \mathrm{~A}$ | - | $\pm 3 \mu \mathrm{~A}$ each | $\pm 3 \mu \mathrm{~A} / \pm 3 \mu \mathrm{~A} / \pm 10 \mu \mathrm{~A}$ |
| $\begin{gathered} \pm 10.5 \mathrm{~V} \\ \pm 18 \mathrm{~V} \end{gathered}$ | $\begin{aligned} & \pm 10 \mathrm{~V} \\ & \pm \mathrm{V}_{\mathrm{S}} \end{aligned}$ | $\begin{gathered} \pm 10 \mathrm{~V} \\ \pm \mathrm{V}_{\mathrm{S}} \end{gathered}$ | $\begin{aligned} & \pm 10: 5 \mathrm{~V} \\ & \pm 16 \mathrm{~V} \end{aligned}$ | $\begin{gathered} \pm 10.5 \mathrm{~V} \\ \pm 16 \mathrm{~V} \end{gathered}$ |
| $\begin{gathered} \pm 14.7 \text { to } \pm 15.3 \mathrm{~V} \\ \pm 11.5 \text { to } \pm 18 \mathrm{~V} \\ +5 \mathrm{~mA} \end{gathered}$ | $\begin{gathered} \pm 15 \mathrm{~V} \\ \pm 12 \text { to } \pm 18 \mathrm{~V} \\ \pm 6 \mathrm{~mA} \end{gathered}$ | $\begin{gathered} \pm 15 \mathrm{~V} \\ \pm 12 \mathrm{to} \pm 18 \mathrm{~V} \\ \pm 9 \mathrm{~mA} \end{gathered}$ | $\begin{gathered} \pm 14.8 \text { to } \pm 16 \mathrm{~V} \\ \pm 14.8 \text { to } \pm 16 \mathrm{~V} \\ \pm 16 \mathrm{~mA} \end{gathered}$ | $\begin{gathered} \pm 14.8 \text { to } \pm 15.3 \mathrm{~V} \\ \pm 14.8 \text { to } \pm 16 \mathrm{~V} \\ \pm 16 \mathrm{~mA} \end{gathered}$ |
| $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \\ -25^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \\ -25^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \end{gathered}$ | $\begin{aligned} & -25^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ & -25^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ & -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \\ -25^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \\ -25^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \end{gathered}$ |
| $\begin{gathered} \text { FA-4 } \\ 1.5^{\prime \prime} \times 1.5^{\prime \prime} \times 0.6^{\prime \prime} \\ (38.1 \times 38.1 \times 15.2) \end{gathered}$ | $\begin{gathered} \text { D-2 } \\ 1.65^{\prime \prime} \times 3.07^{\prime \prime} \times 0.65^{\prime \prime} \\ (41.9 \times 77.9 \times 16.5) \end{gathered}$ | $\begin{gathered} \text { FA-8 } \\ 1.5^{\prime \prime} \times 1.5^{\prime \prime} \times 0.62^{\prime \prime} \\ (38.1 \times 38.1 \times 15.2) \end{gathered}$ | $\begin{gathered} \mathrm{D}-1 \\ 1.6^{\prime \prime} \times 3.0^{\prime \prime} \times 0.6^{\prime \prime} \\ (40.6 \times 76.2 \times 15.2) \end{gathered}$ | $\begin{gathered} \text { D-2 } \\ 1.6^{\prime \prime} \times 3.0^{\prime \prime} \times 0.6^{\prime \prime} \\ (40.6 \times 76.2 \times 15.2) \end{gathered}$ |
| $\begin{aligned} & \hline \$ 93(\$ 114) \\ & \$ 83(\$ 103) \end{aligned}$ | $\begin{aligned} & \$ 98(\$ 145) \\ & \$ 92(\$ 135) \end{aligned}$ | $\begin{aligned} & \$ 75(\$ 95) \\ & \$ 69(\$ 87) \end{aligned}$ | $\begin{aligned} & \hline \$ 153(\$ 191) \\ & \$ 139(\$ 173) \end{aligned}$ | $\$ 175(\$ 231)$ $\$ 157(\$ 208)$ |

${ }^{4}$ All models are short-circuit-proof, from output to ground. Multipliers are not guaranteed short-circuit-proof from output to $+\mathrm{V}_{\mathrm{s}}$ or $-\mathrm{V}_{\mathrm{s}}$.
${ }^{5}$ Specification holds over denominator ( $\mathrm{V}_{\mathrm{x}}$ ) signal range from 100 mV to 10 V .

SPECIFICATION SUMMARY (Typical @ $+25^{\circ} \mathrm{C}$ and $\pm 15 \mathrm{VDC}$, unless otherwise specified.)
VARIABLE TRANSCONDUCTANCE TYPES

| Models | $530 \mathrm{~J}(530 \mathrm{~K})(530 \mathrm{~L})(530 \mathrm{~S})$ | 531J (531K) (531L) (531S) |
| :---: | :---: | :---: |
| Full Scale Accuracy | 2\% (1\%) (0.5\%) (1\%) | 2\% (1\%) (0.5\%) (1\%) |
| Divides and Square Roots | YES | YES |
| Multiplication Characteristics |  |  |
| Output Function | XY/10 | XY/ $\mathbf{I}_{\text {REF }}$ |
| Error, Internal Trim ( $\pm$ ) | N/A | N/A |
| Error, External Trim ( $\pm$ ) max | 2\% (1\%) (0.5\%) (1\%) | 2\% (1\%) (0.5\%) (1\%) |
| Accuracy vs. Temperature ( $\pm$ ) | $0.06(0.03)(0.01)(0.02 \mathrm{max}) \% /{ }^{\circ} \mathrm{C}$ | $0.06(0.03)(0.01)(0.02 \mathrm{max}) \% /{ }^{\circ} \mathrm{C}$ |
| Accuracy vs. Supply ( $\pm$ ) | 0.2\%/\% | 0.2\%/\% |
| Warm up Time to Specifications | 1 sec | 1 sec |
| Output Offset ( $\pm$ ) |  |  |
| Initial |  |  |
| Average vs. Temperature 0 to $+70^{\circ} \mathrm{C}$ | $0.2 \mathrm{mV} /{ }^{\circ} \mathrm{C}$ | $0.2 \mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Average vs. Supply | $70 \mathrm{mV} / \mathrm{V}$ | $70 \mathrm{mV} / \mathrm{V}$ |
| Scale Factor ( $\pm$ ) | Fixed | Dynamically Variable |
| Initial Error | Adj. to 1\%(0.5\%)(0.2\%)(0.5\%) | Adj. to 1\%(0.5\%)(0.2\%)(0.5\%) |
| Non Linearity ( $\pm$ ) |  |  |
| $X$ Input ( $\mathrm{X}=20 \mathrm{~V} \mathrm{p}-\mathrm{p}, \mathrm{Y}= \pm 10 \mathrm{VDC}$ ) | 0.8\%(0.5\%)(0.3\%)(0.5\%) | 0.8\%(0.5\%)(0.3\%)(0.5\%) ${ }^{(1)}$ |
| $Y \operatorname{Input}(\mathrm{Y}=20 \mathrm{~V} \mathrm{p}-\mathrm{p}, \mathrm{X}= \pm 10 \mathrm{VDC}$ ) | 0.3\%(0.2\%)(0.2\%)(0.2\%) | 0.3\%(0.2\%)(0.2\%)(0.2\%) ${ }^{(1)}$ |


| Feedthrough |  |  |
| :---: | :---: | :---: |
| $\mathrm{X}=0, \mathrm{Y}=20 \mathrm{~V}$ p-p 50 Hz | - | - |
| with external trim | $150 \mathrm{mV}(80 \mathrm{mV})(40 \mathrm{mV})(80 \mathrm{mV}) \mathrm{p}-\mathrm{p} \max$ | $150 \mathrm{mV}(80 \mathrm{mV})(40 \mathrm{mV})(80 \mathrm{mV}) \mathrm{p}-\mathrm{p} \max ^{(1)}$ |
| $\mathrm{Y}=0, \mathrm{X}=20 \mathrm{~V}$ p-p 50 Hz | - | - |
| with external trim | $100 \mathrm{mV}(60 \mathrm{mV})(30 \mathrm{mV})(60 \mathrm{mV}) \mathrm{p}-\mathrm{p} \max$ | $100 \mathrm{mV}(60 \mathrm{mV})(30 \mathrm{mV})(60 \mathrm{mV}) \mathrm{p}-\mathrm{p} \max ^{(1)}$ |
| Feedthrough vs. Temperature, each input | $2 \mathrm{mV} \mathrm{p-p/}{ }^{\circ} \mathrm{C}$ | $2 \mathrm{mV} \mathrm{p}-\mathrm{p} /{ }^{\circ} \mathrm{C}$ |
| Bandwidth |  |  |
| -3dB Small Signal | 1 MHz | 1 MHz |
| Full Power Response | 750 kHz | 750 kHz |
| Slew Rate | $45 \mathrm{~V} / \mu \mathrm{sec}$ | $45 \mathrm{~V} / \mu \mathrm{sec}$ |
| Small Signal Amplitude Error ( $\pm$ ) | 1\% @ 100kHz | 1\%@100kHz |
| Small Signal Vector Error ( $\pm$ ) | $1 \%$ @ 10kHz | $1 \%$ @ 10kHz |
| Settling Time for $\pm 10 \mathrm{~V}$ Step | $1 \mu \mathrm{sec}$ to $2 \%$ | $1 \mu \mathrm{sec}$ to $2 \%$ |
| Overload Recovery | $1 \mu \mathrm{sec}$ | $1 \mu \mathrm{sec}$ |
| Output Noise |  |  |
| 5 Hz to 10 kHz | $600 \mu \mathrm{~V}$ rms | $600 \mu \mathrm{~V}$ rms |
| 5 Hz to 5 MHz | 3 mV rms | 3 mV rms |
| Output Characteristics |  |  |
| Voltage at Rated Load (min) | $\pm 10 \mathrm{~V}$ | $\pm 10 \mathrm{~V}$ |
| Current (min) | $\pm 5 \mathrm{~mA}$ | $\pm 5 \mathrm{~mA}$ |
| Load Capacitance Limit | $0.001 \mu \mathrm{~F}$ | $0.001 \mu \mathrm{~F}$ |


| Input Resistance X/Y/Z Input ${ }^{2}$ | $10 \mathrm{M} \Omega / 6 \mathrm{M} \Omega / 36 \mathrm{k} \Omega$ | $10 \mathrm{M} \Omega / 6 \mathrm{M} \Omega / 36 \mathrm{k} \Omega$ |
| :---: | :---: | :---: |
| Input Bias Current X/Y/Z Input | $2 \mu \mathrm{~A} / 2 \mu \mathrm{~A} / 5 \mu \mathrm{~A}$ | $2 \mu \mathrm{~A} / 2 \mu \mathrm{~A} / 5 \mu \mathrm{~A}$ |
| Maximum Input Voltage <br> For Rated Accuracy <br> Safe Level | $\begin{aligned} & \pm 10.1 \mathrm{~V} \\ & \pm \mathrm{V}_{\mathrm{S}} \end{aligned}$ | $\begin{aligned} & \pm 10.1 \mathrm{~V} \\ & \pm \mathrm{V}_{\mathrm{S}} \end{aligned}$ |
| Power Supply ( $\mathrm{V}_{\mathbf{s}}$ ) <br> Rated Performance <br> Operating <br> Quiescent Current | $\begin{gathered} \pm 15 \mathrm{~V} \\ \pm 12 \text { to } \pm 18 \mathrm{~V} \\ \pm 4 \mathrm{~mA} \end{gathered}$ | $\begin{gathered} \pm 15 \mathrm{~V} \\ \pm 12 \text { to } \pm 18 \mathrm{~V} \\ \pm 4.5 \mathrm{~mA} \end{gathered}$ |
| Temperature Range <br> Rated Performance <br> Operating <br> Storage | $\begin{gathered} \mathrm{J}-0 \text { to }+70^{\circ} \mathrm{C} \mathrm{~K}-0 \text { to }+70^{\circ} \mathrm{C} \\ \mathrm{~L}-0 \text { to }+70^{\circ} \mathrm{C} \mathrm{~S}-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\ -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\ -65^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} \mathrm{J}-0 \text { to }+70^{\circ} \mathrm{C} \mathrm{~K}-0 \text { to }+70^{\circ} \mathrm{C} \\ \mathrm{~L}-0 \text { to }+70^{\circ} \mathrm{C} \mathrm{~S}-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\ -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\ -65^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \end{gathered}$ |
| Package Outline | TO-100 + TO-116 | TO-116 |
| Price 1-24 <br> Price 25-99 | $\begin{aligned} & \$ 22.50(\$ 33.50)(\$ 45.00)(\$ 51.00) \\ & \$ 18.00(\$ 27.00)(\$ 36.00)(\$ 41.00) \end{aligned}$ | $\begin{aligned} & \$ 11.95(\$ 17.95)(\$ 45.00)(\$ 48.50) \\ & \$ 9.50(\$ 14.35)(\$ 37.00)(\$ 39.50) \end{aligned}$ |

(1) $I_{\text {REF }}=$ full scale.
(2) Z input current is proportional to Z input voltage.

| 532J (532K) (532S) | 533 J (533K) (533L) (533S) |
| :---: | :---: |
| 2\% (1\%) (1\%) | 2\% (1\%) (0.5\%) (1\%) |
| YES | YES |
| $\begin{gathered} \left(\mathrm{X}_{1}-\mathrm{X}_{2}\right)\left(\mathrm{Y}_{1}-\mathrm{Y}_{2}\right) / 10 \\ 2 \%(1 \%)(1 \%) \\ \mathrm{N} / \mathrm{A} \\ 0.06(0.03)(0.02) \% /{ }^{\circ} \mathrm{C} \\ 0.2 \% / \% \\ 1 \mathrm{sec} \\ \hline \end{gathered}$ | $\begin{gathered} \mathrm{XY} / 10 \\ \mathrm{~N} / \mathrm{A} \\ 2 \%(1 \%)(0.5 \%)(1 \%) \\ 0.04(0.03)(0.01)(0.01) \% /{ }^{\circ} \mathrm{C} \\ 0.5 \% / \% \\ 1 \mathrm{sec} \end{gathered}$ |
| $\begin{gathered} \pm 50 \mathrm{mV} \max ( \pm 20 \mathrm{mV} \max )( \pm 20 \mathrm{mV} \max ) \\ 0.7(0.7)(2.0 \max ) \mathrm{mV} /{ }^{\circ} \mathrm{C} \\ 60 \mathrm{mV} / \mathrm{V} \\ \hline \end{gathered}$ | $\begin{gathered} \text { Adj. to zero } \\ 0.7 \mathrm{mV} /{ }^{\circ} \mathrm{C} \\ 70 \mathrm{mV} / \mathrm{V} \\ \hline \end{gathered}$ |
| Fixed Adj. to $1 \%(0.5 \%)(0.5 \%)$ | Fixed Adj. to 1\% |
| $\begin{aligned} & 0.8 \%(0.5 \%)(0.5 \%) \\ & 0.3 \%(0.2 \%)(0.2 \%) \end{aligned}$ | $\begin{aligned} & 0.8 \%(0.5 \%)(0.5 \%)(0.5 \%) \\ & 0.3 \%(0.2 \%)(0.2 \%)(0.5 \%) \end{aligned}$ |
| $\begin{gathered} 200 \mathrm{mV}(100 \mathrm{mV})(100 \mathrm{mV}) \mathrm{p}-\mathrm{p} \max \\ - \\ 200 \mathrm{mV}(100 \mathrm{mV})(100 \mathrm{mV}) \mathrm{p}-\mathrm{p} \max \\ - \\ 2 \mathrm{mV} \text { p-p/ } /{ }^{\circ} \mathrm{C} \\ \hline \end{gathered}$ | $\begin{aligned} & 150 \mathrm{mV}(100 \mathrm{mV})(50 \mathrm{mV})(100 \mathrm{mV}) \mathrm{p}-\mathrm{p} \max \\ & - \\ & 200 \mathrm{mV}(100 \mathrm{mV})(50 \mathrm{mV})(100 \mathrm{mV}) \mathrm{p}-\mathrm{p} \max \\ & 2 \mathrm{mV} \mathrm{p-p} /^{\circ} \mathrm{C} \end{aligned}$ |
| 1 MHz <br> 750 kHz <br> $45 \mathrm{~V} / \mu \mathrm{sec}$ <br> $1 \%$ @ 100 kHz <br> $1 \%$ @ 10 kHz <br> $1 \mu \mathrm{sec}$ to $2 \%$ <br> $1 \mu \mathrm{sec}$ | 1 MHz <br> 750 kHz <br> $45 \mathrm{~V} / \mu \mathrm{sec}$ $1 \%$ @ 100 kHz <br> $1 \%$ @ 10 kHz <br> $1 \mu \mathrm{sec}$ to $2 \%$ <br> $1 \mu \mathrm{sec}$ |
| $\begin{gathered} 600 \mu \mathrm{~V} \mathrm{rms} \\ 3 \mathrm{mV} \mathrm{rms} \\ \hline \end{gathered}$ | $\begin{gathered} 600 \mu \mathrm{~V} \mathrm{rms} \\ 3 \mathrm{mV} \\ \hline \end{gathered}$ |
| $\begin{gathered} \pm 10 \mathrm{~V} \\ \pm 5 \mathrm{~mA} \\ 0.001 \mu \mathrm{~F} \end{gathered}$ | $\begin{gathered} \pm 10 \mathrm{~V} \\ \pm 5 \mathrm{~mA} \\ 0.001 \mu \mathrm{~F} \end{gathered}$ |
| $10 \mathrm{M} \Omega / 10 \mathrm{M} \Omega / 36 \mathrm{k} \Omega$ | $10 \mathrm{M} \Omega / 6 \mathrm{M} \Omega / 36 \mathrm{k} \Omega$ |
| $2 \mu \mathrm{~A} / 3 \mu \mathrm{~A} / 5 \mu \mathrm{~A}$ | $3 \mu \mathrm{~A}(7.5 \mu \mathrm{~A} \max )(5 \mu \mathrm{~A} \max )(7.5 \mu \mathrm{~A} \max )$ |
| $\begin{aligned} & \pm 10.1 \mathrm{~V} \\ & \pm \mathrm{V}_{\mathrm{S}} \end{aligned}$ | $\begin{gathered} \pm 10.1 \mathrm{~V} \\ \pm \mathrm{V}_{\mathrm{s}} \end{gathered}$ |
| $\begin{gathered} \pm 15 \mathrm{~V} \\ \pm 10 \text { to } \pm 18 \mathrm{~V} \\ \pm 4 \mathrm{~mA} \end{gathered}$ | $\begin{gathered} \pm 15 \mathrm{~V} \\ \pm 12 \text { to } \pm 18 \mathrm{~V} \\ \pm 4 \mathrm{~mA} \end{gathered}$ |
| $\begin{aligned} & 0 \text { to }+70^{\circ} \mathrm{C}\left(0 \text { to }+70^{\circ} \mathrm{C}\right)\left(-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C}\right) \\ &-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\ &-65^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $\begin{gathered} \mathrm{J}-0 \text { to }+70^{\circ} \mathrm{C} \mathrm{~K}-0 \text { to }+70^{\circ} \mathrm{C} \\ \mathrm{~L}-0 \text { to }+70^{\circ} \mathrm{C} \mathrm{~S}--55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\ -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\ -65^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \end{gathered}$ |
| TO-100 + TO-116 | TO-100 + TO-116 |
| $\begin{aligned} & \$ 26.00(\$ 36.00)(\$ 49.00) \\ & \$ 21.00(\$ 30.00)(\$ 40.00) \end{aligned}$ | $\begin{aligned} & \$ 8.90(\$ 14.90)(\$ 42.50)(\$ 46.50) \\ & \$ 7.10(\$ 11.90)(\$ 33.50)(\$ 37.50) \end{aligned}$ |



MODEL 440: LOW COST, GENERAL PURPOSE CONVERTER
Model 440 is a compact economy true rms to DC converter module featuring performance usually found in higher priced units. In addition to measuring AC signals, model 440 can also measure directly the rms value of a waveform containing both AC and DC.
Model 440 is available in two accuracy grades; model 440 K features total error of $\pm 5 \mathrm{mV} \pm 0.1 \%$ reading, while model 440 J has total error of $\pm 15 \mathrm{mV} \pm 0.2 \%$ reading. No external adjustments or components are required to achieve rated performance. For users who require the utmost in accuracy, a $20 \mathrm{k} \Omega$ optional trim potentiometer may be used to zero the output offset voltage, a feature not found on many RMS converters.

## IMPROVED CREST FACTOR PERFORMANCE

OEM instrument designers will find the high accuracy of model 440 makes it an excellent choice whenever rms measurements must be made independent of waveform. The most important criteria for rms conversion is error versus signal crest factor.
Crest factor of an input signal is the ratio of peak input signal to the rms level. Most rms measurements require signal crest factors less than 3 . The excellent crest factor capability of model 440 is shown in the curve below. Rated accuracy is achieved for crest factors as high as 5 . For the most demanding applications, less than $\pm 1 \%$ reading error occurs with signal crest factor as high as 10 .


SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{S}}= \pm 15$ VDC
unless otherwise noted)

| MODEL | 440J (440K) |
| :---: | :---: |
| TRANSFER EQUATION | $\mathrm{e}_{\mathrm{O}}=\sqrt{\operatorname{avg}\left(\mathrm{e}_{\mathrm{in}}\right)^{2}}$ |
| ACCURACY ${ }^{1}$ |  |
| Total Error |  |
| No External Adjustment | $\pm 15 \mathrm{mV} \pm 0.2 \%,( \pm 5 \mathrm{mV} \pm 0.1 \%) \mathrm{Max}$ |
| External Adjustment | $\pm 10 \mathrm{mV} \pm 0.1 \%$, ( $\pm 2 \mathrm{mV} \pm 0.05 \%) \mathrm{Max}$ |
| vs. Temperature ( 0 to $+70^{\circ} \mathrm{C}$ ) | $\pm(0.2 \mathrm{mV} \pm 0.02 \%) /{ }^{\circ} \mathrm{C}, \mathrm{Max}$ |
| vs. Supply Voltage | $\pm 0.2 \mathrm{mV} / \mathrm{V}$ |
| CREST FACTOR |  |
| Rated Accuracy | 5 Min |
| $\pm 1 \%$ Reading Error | 10 |
| FREQUENCY RESPONSE, Sinewave |  |
| Rated Accuracy |  |
| Input Range, 0.1 to $7 \mathrm{~V}_{\mathrm{rms}}$ | 10 kHz , Min |
| $\pm 1 \%$ Reading Error |  |
| Input, $7 \mathrm{~V}_{\text {rms }}$ | 50kHz, Min |
| Input, $0.7 \mathrm{~V}_{\text {rms }}$ | 100 kHz , Min |
| Bandwidth, -3 dB |  |
| Input Range, 0.7 to $7 \mathrm{~V}_{\text {rms }}$ | 500 kHz |
| Internal Filter Time Constant | 10 ms |
| External Filter Time Constant | $50 \mathrm{~ms} / \mu \mathrm{F}$ |
| Total Averaging Time Constant | $10 \mathrm{~ms}+50 \mathrm{~ms} / \mu \mathrm{F}$ |
| OUTPUT SPECIFICATIONS |  |
| Rated Output |  |
| Voltage | +10.0V, Min |
| Current | +10.0 mA , Min |
| Resistance | $0.1 \Omega$ |
| Offset Voltage |  |
| Internally Trimmed External Trim | $\pm 5 \mathrm{mV},( \pm 2 \mathrm{mV}) \mathrm{Max}$ <br> Adjustable to Zero |
| INPUT SPECIFICATIONS |  |
| Voltage |  |
| Signal Range | $\pm 10 \mathrm{~V}$, Peak |
| Safe Input | $\pm V_{\text {S }}$, Max |
| dB Range, Referred to 1V | -20 dB to 17 dB |
| dBm Range, referred to 0.775 V ( 1 mW in $600 \Omega$ ) | -18 dBm to 19 dBm |
| Impedance | $8.3 \mathrm{k} \Omega \pm 2 \%$ |
| Offset Voltage <br> vs. Temperature ( 0 to $+70^{\circ} \mathrm{C}$ ) | $\begin{aligned} & \pm 3 \mathrm{mV}, \mathrm{Max} \\ & \pm 10 \mu \mathrm{~V} /^{\circ} \mathrm{C} \end{aligned}$ |
| POWER SUPPLY |  |
| Voltage, Rated Performance | $\pm 15 \mathrm{VDC}$ |
| Voltage, Operating | $\pm(6$ to 18$) \mathrm{VDC}$ |
| Current, Quiescent | $\pm 10 \mathrm{~mA}$ |
| TEMPERATURE RANGE |  |
| Rated Performance | 0 to $+70^{\circ} \mathrm{C}$ |
| Operating | $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |
| Storage | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| PACKAGE | F-7 |
| Case Dimensions | $\begin{aligned} & 1.5^{\prime \prime} \times 1.5^{\prime \prime} \times 0.4^{\prime \prime} \\ & (38.1 \times 38.1 \times 10.2) \end{aligned}$ |
| PRICE |  |
| (1-9) | \$62 (\$77) |
| (10-24) | \$56 (\$69) |

${ }^{1}$ Total output error is specified as the sum of two components; a fixed term plus a percentage of peak output signal. Model 440K, for example, has a rated accuracy of $\pm 5 \mathrm{mV} \pm 0.1 \%$ which for a one volt rms sinewave, results in a $\pm 6 \mathrm{mV}$ maximum error. The fixed error component is composed of output offset and input offset errors. Output offset may be trimmed to zero by external adjustment of an optional $20 \mathrm{k} \Omega$ potentiometer. The $\%$ of reading error is attributed to nonlinearity and scale factor errors. Scale factor error may be reduced by external adjustment of an optional $5 \mathrm{k} \Omega$ potentiometer.

## DIVIDERS AND MULTIFUNCTION MODULES MODELS 436, 434, 433

## PRODUCT PROFILE

## MODEL 436: TWO-QUADRANT DIVIDER

Model 436 is a precision, two-quadrant variable transconductance analog divider featuring guaranteed accuracy of $\pm 0.5 \%$ (model 436A) and $\pm 0.25 \%$ (model 436B) over a $100: 1$ denominator signal range $(+100 \mathrm{mV}$ to $+10 \mathrm{~V})$ with no external adjustments. With the use of optional external trimming, accuracy may be improved to $\pm 0.05 \%$ (436B) over a 1000 : 1 denominator signal range. In addition to this excellent accuracy, model 436 offers a small signal bandwidth $(-3 \mathrm{~dB})$ of 300 kHz and numerator nonlinearity of $\pm 0.05 \%$.
Output offset drift vs. temperature of the model 436 remains fairly constant over a 100:1 range of denominators. Total error drift is typically $1 \mathrm{mV} /{ }^{\circ} \mathrm{C}$ at $\mathrm{V}_{\mathrm{X}}=+10 \mathrm{~V}$ and $2 \mathrm{mV} /{ }^{\circ} \mathrm{C}$ at $\mathrm{V}_{\mathrm{X}}=$ +100 mV . Model 436 is therefore capable of maintaining outstanding accuracy over a wide range of temperature. Thus, in divider applications requiring high accuracy and wide bandwidth over a wide denominator range, the model 436 provides significant advantages over $0.1 \%$ multipliers used in the inverted multiplier divide mode. An untrimmed 436 yields better overall accuracy than the most accurate available multiplier for a 100:1 change in denominator.
Through the use of hermetically sealed semiconductors, the model 436 affords exceptional reliability over a wide operating temperature range $\left(-25^{\circ} \mathrm{C}\right.$ to $\left.+85^{\circ} \mathrm{C}\right)$.
The model 436 divider is useful for direct readout of such ratios as efficiencies, losses or gains, \% distortion, impedance magnitudes, elasticity (stress/strain). Ratios may be taken of instantaneous, average, RMS or peak quantities. Furthermore, in conjunction with sample/hold devices, ratios may be taken of any of these measurements at different instants of time.


## MODEL 434 : ONE QUADRANT DIVIDER

The Model 434 is an accurate one quadrant analog divider capable of accepting either current or voltage inputs over a 100:1 signal range with no external trimming required. A voltage controlled scale factor feature permits external programming of gain. In analog computation applications, the scale factor input may be used as an analog input facilitating simultaneous multiplication and division of three analog variables in a single module.

The basic transfer functions of Model 434 are:

$$
e_{o}=\frac{10}{9} V_{y} \frac{V_{z}}{V_{x}} \quad \text { OR: } e_{o}=\frac{10}{9} V_{y} \frac{I_{z}}{I_{x}}
$$



## EXAMPLES OF MODEL 433 TRANSFER FUNCTIONS

General Expression: $\mathrm{V}_{\mathrm{o}}=\frac{10}{9} \mathrm{~V}_{\mathrm{y}}\left(\mathrm{V}_{\mathrm{z}} / \mathrm{V}_{\mathrm{x}}\right)^{\mathrm{m}}$
Limits: $\quad 1 / 5 \leqslant m \leqslant 5,0<V_{x}, V_{y}, V_{z} \leqslant 10 \mathrm{~V}$
Using two programming resistors only:

| Multiply: | $\mathrm{V}_{\mathrm{o}}=\mathrm{K} \mathrm{V}_{\mathrm{y}} \mathrm{V}_{\mathrm{z}}$ | Divide: | $\mathrm{V}_{\mathrm{o}}=\mathrm{K}\left(\mathrm{V}_{\mathrm{z}} / \mathrm{V}_{\mathrm{x}}\right)$ |
| :--- | :--- | :--- | :--- |
| Square: | $\mathrm{V}_{\mathrm{o}}=\mathrm{K}\left(\mathrm{V}_{\mathrm{z}}\right)^{2}=\mathrm{K} \mathrm{V}_{\mathrm{z}} \mathrm{V}_{\mathrm{y}}$ | Square Root: | $\mathrm{V}_{\mathrm{O}}=\mathrm{K}\left(\mathrm{V}_{\mathrm{z}}\right)^{1 / 2}$ |
| Powers: | $\mathrm{V}_{\mathrm{o}}=\mathrm{K} \mathrm{V}_{\mathrm{y}}\left(\mathrm{V}_{\mathrm{z}} / \mathrm{V}_{\mathrm{x}}\right)^{1<\mathrm{m} \leqslant 5}$ | Roots: | $\mathrm{V}_{\mathrm{o}}=\mathrm{K} \mathrm{V}_{\mathrm{y}}\left(\mathrm{V}_{\mathrm{z}} / \mathrm{V}_{\mathrm{x}}\right)^{1 / 5 \leqslant \mathrm{~m}<1}$ |
| P/V/T: | $\mathrm{V}_{\mathrm{o}}=\mathrm{K} \mathrm{V}_{\mathrm{y}} \mathrm{V}_{\mathrm{z}} / \mathrm{V}_{\mathrm{x}}$ | Reciprocal: | $\mathrm{V}_{\mathrm{o}}=\mathrm{K} / \mathrm{V}_{\mathrm{x}}$ |

Using External Amplifiers:
True RMS to $\mathrm{DC}: \mathrm{V}_{\mathrm{o}}=\sqrt{\overline{\mathrm{V}_{1}{ }^{2}}}$
Vector: $\quad V_{0}=\sqrt{\mathrm{V}_{1}{ }^{2}+\mathrm{V}_{2}{ }^{2}}$

## MODEL 433: MULTIFUNCTION MODULE

The model 433 is a multifunction module, consisting of all hermetically sealed semiconductors, which may be used to implement a wide range of computational circuits. Requiring only two external resistors for programming the exponent, $m$, the model 433 will perform multiplication, division or exponentiation up to the 5 th power or root according to the expression, $\mathrm{Y}(\mathrm{Z} / \mathrm{X})^{\mathrm{m}}$. It may also be used to develop more complex functions such as RMS or vector sums using inexpensive external operational amplifiers. Examples of these transfer functions are listed below along with a model 433 block diagram design.
The model 433 has proven to be extremely useful for generating both linear and nonlinear functions for on-thespot computations and for linearizing a wide range of transducer characteristics in medical, industrial and process control equipment design. Its excellent accuracy performance and programmability make it ideal for analog computation or simulation, test equipment designs or, in general, where one function module may be used to fulfill several design objectives. Model 433 is attractively priced for new OEM equipment designs.

## MODEL 433J: 0.5\% DIVIDER, WIDE DYNAMIC RANGE

 Probably the most impressive performance improvement owing to model 433's log/antilog circuit approach, is its ability to hold high divider accuracies over wide, $100: 1$, input signal ranges. For example, when compared to a precision $0.1 \%$ multiplier/divider of conventional design, the model 433 offers greater than a tenfold improvement. As shown in Figure 1, the model 433 J has only 30 mV of error for a denominator of 100 mV , as opposed to 300 to 500 mV of error for the conventional multiplier/divider.When using a conventional multiplier/divider as a divider, accuracy, offset drift, and noise performance are all degraded as the denominator is decreased. But, for model 433, accuracy, offset drift, and noise performance are all virtually independent of denominator level as illustrated in Figure 1, and this performance is obtained with no external trims.
It is apparent that as a one-quadrant divider, model 433's performance exceeds by wide margins those of higher accuracy dividers costing two to three times more.

## CIRCUIT TECHNIQUES

The model 433, using log circuit techniques, is designed in two parts and consists of $\log$ circuits followed by an antilog section. The log ratio section operates on inputs X and Z to develop the function, $\log \mathrm{Z} / \mathrm{X}$. This ratio is then either amplified or attenuated, using external programming resistors, R1 and R2, to establish the exponent, m , where $\mathrm{m}>1$ for powers, $\mathrm{m}<1$ for roots. The signal, $\mathrm{m} \log \mathrm{Z} / \mathrm{X}$, is then summed with the $\log \mathrm{Y}$; and the anti$\log$ is developed to realize the final transfer function, $(10 / 9)(\mathrm{Y})(\mathrm{Z} / \mathrm{M})^{\mathrm{m}}$. The exponent, $m$, may have any value from $1 / 5$ to 5 . As with all log designs, operation is limited to one quadrant.
An internal reference voltage, $\mathrm{V}_{\text {ref }}$, is also made available for the convenience of the user. When setting up the desired transfer function, all unused input terminals should be connected to $\mathrm{V}_{\text {ref }}$. This reference voltage is temperature compensated, as is the entire 433 design, for good performance from 0 to $+70^{\circ} \mathrm{C}$.


Figure 1. Comparison of Divider Error vs. Denominator Level for Model 433 and a Conventional Multiplier/Divider


Figure 2. Block Diagram Model 433

MODEL 433B: HIGHER ACCURACY, 0.25\%
Model 433B, an improved version of model 433J, offers $1 / 4 \%$ accuracy for denominator levels of 100 mV to 10 V , has a lower initial offset voltage than the 433J, and offers guaranteed drift performance over a wider temperature range. Like the 433 J , this new design contains all hermetically sealed semiconductors.

## FEEDBACK TECHNIQUE VS DIRECT IMPLEMENTATION

The reason for the significant improvement of model 433 over other divider designs is apparent if one considers the basic sources of error arising from each design approach. Conventional divider circuits are implemented by using a multiplier cell in a feedback loop. As with all feedback designs, overall accuracy is directly tied to the accuracy and gain setting of the feedback element, a multiplier in this case. In this configuration, as X decreases, loop gain decreases, and divider accuracy therefore varies inversely with the denominator signal, $X$. The governing equation for this design is derived and presented in Figure 3 to illustrate its basic limitations.
Good performance for these designs requires using a fast, highaccuracy multiplier and a low-drift amplifier in the divider loop.

In contrast, the model 433 log circuit directly implements the divide function. Its accuracy, as shown in Figure 3, is virtually independent of denominator amplitude for constant signal ratios, thereby improving on the conventional divider approach. Drift nonlinearity and noise are also independent of denominator amplitude in contrast to feedback designs. Its only drawback is that operation is restricted to one quadrant (which is not usually a handicap for many applications).

## MODEL 434: HIGH ACCURACY DIVIDER, VOLTAGE/ CURRENT INPUTS <br> $$
e_{o}=V_{y} \frac{I_{z}}{I_{x}} \text { or } V_{y} \frac{V_{z}}{V_{x}}
$$

Model 434, a new member of the 433 family, contains all hermetically sealed semiconductors, is optimized for one quadrant divider applications, and may be trimmed externally to eliminate all DC offset errors. With no external trimming; accuracy is guaranteed to within $1 / 2 \%$ for model 434A and to $1 / 4 \%$ for model 434B. In order to facilitate the implementation of complex circuits, such as vector computations, the model 434 has input pins brought directly to the internal summing junctions. Current summing can then be done directly at the input pin without the use of an external amplifier. A separate set of input pins is brought out for voltage operation thereby offering complete flexibility on combinations of input signals.
Model 434 may be easily connected as a precision, wide dynamic range square rooter by jumper connecting the output to the denominator input. In the square root mode, model 434B will accept input signals over a $1000: 1$ dynamic range ( 10 mV to 10 V ) with a total maximum error of $\pm 0.25 \%$.


Figure 3. Divider Model


Figure 4. Simplified Logarithmic Divider. Error is a Constant Plus a Constant Fraction of Output.

SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ and $\pm 15 \mathrm{~V}$ unless otherwise noted)


[^18]
# FUNCTION MODULES LOGARITHMIC AMPLIFIERS AND ELEMENTS 

## A Note On Nomenclature

Log modules from Analog Devices develop the instantaneous value of the log or antilog of an input signal. Contrary to communications type log amplifiers, which basically compress AC signals, the 700 series log modules operate on single polarity inputs from DC to an upper cutoff frequency. These temperature compensated designs will work over 6 decades of input current ( 1 nA to 1 mA ) and 4 decades of voltage ( 1 mV to 10 V ).

## GENERAL DESCRIPTION

Analog Devices offers four types of circuit modules which may be used to develop the log or antilog of an input signal. Depending upon the user's expertise in log amplifier design, or the need for specialized performance, the designer may select: 1) the model 755, a versatile yet complete log/antilog amplifier; 2) the model 756 a versatile and complete log ratio module; 3) the model 752 log module requiring one external op amp to complete the design at lower cost; or 4) the model 751 log element requiring two external op amps and several other components for log operation. The external op amps are usually selected to reduce voltage drift or bias currents for improved performance over extended input signal ranges.
Typical applications for these circuits include data compression, transducer linearization, exponentiation, root extraction, and other computational functions for use in gas chromatography, acoustical and light measurements as well as medical and seismic instrumentation.

Circuit Techniques: In contrast to earlier techniques using diode-resistor breakpoint networks, all Analog Devices' log circuits use a combination of selected dual transistor networks that make use of the relationship between base emitter voltage and collector current. When properly temperature compensated, as supplied by Analog Devices, these improved circuits operate over wider dynamic ranges with better log conformity than most other techniques available. Reduced cost and compact circuitry are other user benefits of this design approach.

Logarithmic Circuits and Sources of Error: Voltage and current log amplifiers are identical in design, except for an input voltage summing resistor, and operate on the input current supplied directly to terminal $\mathrm{I}_{\mathbf{I N}}$. The obvious sources of error for log amplifiers arise from three areas: 1) amplifier offset and drift errors, 2) log conformity errors and 3) frequency limitations. These errors restrict both the static and dynamic range of performance.

Voltage and current offsets of the input amplifier, with their attendant drift and noise, limit the smallest value of input signal to be detected. Base spreading resistance of antilog transistor elements, on the other hand, set the maximum signal level for a given accuracy.
For completeness, offset error and drift terms are expressed by the transfer function in the specification table. From the table, it becomes apparent that voltage offset ( $\mathrm{E}_{\mathrm{os}}$ ) should be trimmed to a small value compared to the lowest level of input voltage to be processed. For example, if $\mathrm{E}_{\text {IN }}$ is 1 mV and $\mathrm{E}_{\mathrm{os}}$ is $1 / 20(50 \mu \mathrm{~V}$ or $5 \%)$ of $\mathrm{E}_{\mathrm{IN}}$, the output error is compressed to $2 \%$ of a decade ( $\log 1.05=2$ ).
Assuming that offset and base resistance errors did not exist, there would still remain the question of how well the logging element conforms to the ideal log transfer characteristic. This is defined as log conformity and is expressed as a percent of the input signal. Typical nonlinearity (i.e. departure from a straight line on a semilog plot) ranges from $0.5 \%$ to $1 \%$ over several decades of signal change. This adds to those errors arising from the voltage offset and drift terms described above.

Since the gain-bandwidth product of the logging element is relatively constant, a change in gain will vary the bandwidth. This gain change occurs as the input current to the logging element varies with signal level. Consequently, frequency response and slew rate are specified as a function of signal level and will vary accordingly. At higher currents, amplifier
frequency response is usually the limiting factor and not log elements.

Circuit Configurations: Shown below, with their appropriate transfer functions, are log and antilog amplifier configurations for models 755 and 752 . Note that model 755 has an adjustable scale factor ( $2 \mathrm{~V}, 1 \mathrm{~V}$, or $2 / 3 \mathrm{~V} /$ decade) which is selected with external pin connections. The corresponding transfer curves for these circuit configurations are presented on page 172 .
Each model, available from Analog Devices (models 755, 752,751 ), is specified with an N or P suffix for operation with positive or negative input signals, respectively. It should be recalled that the log of zero is asymtotic ; the appropriate polarity module is required depending upon whether the input signal is positive or negative.

LOG OF VOLTAGE/CURRENT: MODEL 755N


LOG OF VOLTAGE/CURRENT: MODEL 752N


ANTILOG OF VOLTAGE: MODEL 755 OR 752


IDEALIZED TRANSFER FUNCTIONS

$$
\begin{aligned}
\mathrm{e}_{\text {out }} & =-\mathrm{K} \log _{10} \frac{\mathrm{e}_{\text {in }}}{\mathrm{E}_{\text {REF }}} \quad ; \text { log of voltage } \\
\mathrm{e}_{\text {out }} & =-\mathrm{K} \log _{10} 0 \frac{i_{\text {in }}}{\mathrm{I}_{\mathrm{REF}}} \quad ; \text { log of current } \\
\mathrm{e}_{\text {out }} & =\mathrm{E}_{\text {REF }} 10^{-\mathrm{ein} / K} ; \text { antilog of voltage }
\end{aligned}
$$

# LOGARITHMIC AMPLIFIERS AND ELEMENTS MODELS 755, 752, 75I, 756 

## MODEL 755, COMPLETE LOG/ANTILOG AMPLIFIER

The model 755 , a complete logarithmic amplifier with FET input, provides a choice of six decades of current logging ( 1 nA to 1 mA ), or four decades of voltage logging ( 1 mV to 10 V ). For increased flexibility, three scale factors (2V, 1V, $2 / 3 \mathrm{~V} /$ decade) and log or antilog operation may be selected through appropriate terminal pin connections. When two such amplifiers are connected in tandem, as a log and antilog amplifier, a wide range of fractional powers and roots may be developed for computational purposes. The model 755 offers the greatest value in a complete log/antilog amplifier and is the first choice for the application. Specify 755 N for positive, and 755P for negative input signals, respectively.

## MODEL 752, VERSATILE LOG/ANTILOG AMPLIFIER ELEMENT

The model 752, when operated with an external FET amplifier (e.g., model 40J), will perform over the same input dynamic range as the 755 ; six decades of current ( 1 nA to 1 mA ) and four decades of voltage ( 1 mV to 10 V ). The module contains a temperature compensated log element and scaling resistors for good performance and $1 \mathrm{~V} /$ decade sensitivity. Using an external input resistor and two adjustment pots, the scale factor, reference current and input dynamic range may be varied to suit a specific log or antilog application.
Another key feature of model 752 is the design freedom available to the user. He may select the best amplifier to optimize his design. For example, when used with a chopper stabilized amplifier (e.g., 233 J ), offset voltage errors are minimized for the most demanding applications. For economy, combining 752 with a general purpose FET amplifier (model 40 J ) will provide good current or voltage performance at prices below that of model 755 . Specify 752 N or 752P for use with positive or negative input signals, respectively.

## MODEL 751, TEMPERATURE COMPENSATED LOG ELEMENT

Model 751, a log element building block, is considered the best choice for performance and economy when developing log ratio circuits as well as any other general purpose logcircuit. The 751 contains temperature compensated logging transistors with precision scaling networks which together yield a 1 volt per decade log ratio amplifier when combined with three op amps and several other components. Detailed application notes are available from Analog Devices to aid in applying 751 to a wide variety of circuit designs. Specify 751 N for positive input signals or 751P for negative signals.

## MODEL 756: NEW LOG RATIO MODULE

Capable of either current log ratio or voltage log ratio, the model 756 is the first module of its kind to be offered to the industry. This design consists of a complete log ratio module with two continuously variable signal inputs. Channel 1 features a high performance, 10 pA bias current, FET amplifier that is capable of processing up to four decades of input current. The second channel, intended to be used as a reference,

is also capable of signal processing, but the range is limited to 3 decades.

Designed primarily for photometer applications, model 756 replaces two log modules, a subtractor, and associated circuitry. The signal sources for these applications are usually photo diodes which should be operated in the zero-volt mode (short circuit current). When connected as shown in Figure 2, the summing junctions provide virtual grounds, thereby forcing the input currents to be the short circuit current of the photo diodes.

## Principles of Operation

CURRENT LOG RATIO
Current log ratio is accomplished by model 756 when two currents, $I_{\text {sig }}$ and $I_{\text {ref }}$, are applied directly to the input terminals. The two log amps process these signals providing voltages which are proportional to the log of their respective inputs. These voltages are then subtracted and applied to an output amplifier. The scale factor, when connected as shown, is $1 \mathrm{~V} /$ dec. However, other scale factors may be achieved by using an external/feedback resistor for $\mathrm{A}_{3}$ instead of the internal $15 \mathrm{k} \Omega$. The governing equation for this optional adjustment is:

$$
\mathrm{R} \approx\left(\frac{15 \mathrm{k} \Omega}{\mathrm{~V}}\right) \mathrm{K}_{\mathrm{DES}}
$$

where R represents the total feedback resistance of $\mathrm{A}_{3}$, and $\mathrm{K}_{\mathrm{DES}}$ is the desired scale factor.

As a specific example of gain setting assume it is desired to set the scale factor to 2 V . For this application the feedback resistor must be approximately $\frac{15 \mathrm{k} \Omega}{\mathrm{V}} \times 2 \mathrm{~V}$ or $30 \mathrm{k} \Omega$. To accomplish this, the designer could either insert a $15 \mathrm{k} \Omega$ resistor from the output Pin to Pin 1, or he could leave Pin 1 open and connect a $30 \mathrm{k} \Omega$ resistor from Pin 2 to the output. In either case, the total feedback resistance is $30 \mathrm{k} \Omega$, and the desired scale factor will be achieved.

## VOLTAGE LOG RATIO

The principle of operation for voltage log ratio is identical to that of current log ratio after the voltage signal has been converted to a current. To accomplish this conversion, an external resistor is attached from the voltage signal to the appropriate input current terminal of the 756 . Input currents are then determined by:

$$
I_{\text {sig }}=\frac{e_{1}}{R_{1}}, I_{\text {ref }}=\frac{e_{2}}{R_{2}}
$$



Log of Current


Log of Voltage


SPECIFICATIONS (Typical @ $25^{\circ} \mathrm{C}$ and $\pm 15$ VDC) TRANSFER FUNCTIONS DYNAMIC RANGE

Log of Voltage

$$
e_{\text {out }}=-K \log _{10} \frac{e_{\text {in }}-E_{O S}}{E_{\text {REF }}}
$$

Log of Current

$$
e_{\text {out }}=-K \log _{10} \frac{i_{\mathrm{in}}-I_{\mathrm{OS}}}{I_{\mathrm{REF}}}
$$

## 120 dB

$$
10^{-9} \mathrm{~A} \leqslant\left|\mathrm{i}_{\text {in }}\right| \leqslant 10^{-3} \mathrm{~A}
$$

Antilog of Voltage

$$
e_{\text {out }}=E_{\text {REF }} 10^{-\mathrm{ein} / K^{\prime}} \pm \mathrm{e}_{\text {os }} \quad 10^{-3} \mathrm{~V} \leqslant\left|\mathrm{e}_{\text {out }}\right| \leqslant 10 \mathrm{~V}
$$

TRANSFER FUNCTION COEFFICIENTS MODELS 755, 752, 751

| Symbol | Value | Tolerance | Drift | See Notes |
| :--- | :---: | :---: | :---: | :---: |
| $\mathrm{K}=$ | $2,1,2 / 3 \mathrm{~V}$ | $\pm 1 \%$ | $\pm 0.04 \% /{ }^{\circ} \mathrm{C}$ | $1,2,5$ |
| $\mathrm{E}_{\text {REF }}=$ | $10^{-1} \mathrm{~V}$ | $\pm 2 \%$ | $\pm 0.05 \% /{ }^{\circ} \mathrm{C}$ | $1,3,5$ |
| $\mathrm{I}_{\text {REF }}=$ | $10^{-5} \mathrm{~A}$ | $\pm 2 \%$ | $\pm 0.05 \% / \circ^{\circ} \mathrm{C}$ | $1,3,5$ |
| $\mathrm{E}_{\text {OS }}=$ | $0 \mathrm{~V} \pm$ tol. | $\pm 400 \mu \mathrm{~V}$ | $\pm 10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | 4 |
| $\mathrm{I}_{\text {OS }}=$ | $\mathrm{O} \mathrm{A} \pm$ tol. | $0,-10 \mathrm{pA}$ | $2 \mathrm{X} / 10^{\circ} \mathrm{C}$ | 4 |

ACCURACY OF LOG CONFORMITY (Referred To Input)
MODELS 755, 752, 751

| Input Current <br> Range | Accuracy | Input Voltage <br> Range | Accuracy |
| :---: | :---: | :---: | :---: |
| 1 nA to 10 nA | $\pm 1 \%$ |  |  |
| 10 nA to $100 \mu \mathrm{~A}$ | $\pm 0.5 \%$ | 1 mV to 1 V | $\pm 0.5 \%$ |
| $100 \mu \mathrm{~A}$ to 1 mA | $\pm 1 \%$ | 1 V to 10 V | $\pm 1 \%$ |

NOTES:

1. Positive for positive input (N types), negative for negative inputs ( P types).
2. For model 755, select by external pin connections. For model 752, adjust externally from .5 V .
3. Model 752; $\mathrm{I}_{\mathrm{REF}}, \mathrm{E}_{\mathrm{REF}}$ are externally adjustable.
4. For 752 and 751 , offset is a function of external op amp selection.
5. Parameter is a function of 751 log circuit design.

| MODELS (N \& P TYPES) | ES) 755 | 752/751 |
| :---: | :---: | :---: |
| Small Signal Frequency Response of $i_{\text {in }}(-3 \mathrm{~dB}$ down) |  |  |
| $10^{-9} \mathrm{~A}$ | 80 Hz | 80 Hz |
| $10^{-7} \mathrm{~A}$ | 1 kHz | 1 kHz |
| $10^{-4} \mathrm{~A}$ | 40 kHz | Depends on op amp |
| $10^{-3} \mathrm{~A}$ | 200 kHz | Depends on op amp |
| Rated Output | $\pm 10 \mathrm{~V}$ @ 5 mA | Depends on op amp |
| Power Supply $\pm 15$ | $\pm 15 \mathrm{VDC} \pm 1 \%$ @ 10 mA | Depends on op amp |
| Temperature, Rated Performance | $0-70^{\circ} \mathrm{C}$ | $0-70^{\circ} \mathrm{C}$ |
| Package Outline | F-4 | QB-2/M-3 |
| Case Dimensions (mm) | $\begin{gathered} 1.5^{\prime \prime} \times 1.5^{\prime \prime} \times 0.4^{\prime \prime} \\ (38.1 \times 38.1 \times 10.1) \end{gathered}$ |  |
| Price (1-9) | \$58. | \$33.50/\$40 |
| Sperify P 24) | \$53. | \$29.50/\$26.50 |
| Specify P Type for Negative Inputs; N Types for Positive Inputs. |  |  |

$\left.\begin{array}{ll}\hline \begin{array}{l}\text { Current Log Ratio } \\ \text { Transfer Equation }\end{array} & e_{0}=-K \log \frac{i_{1}}{i_{2}}, i_{1}=\operatorname{sig} \\ i_{2}=r e f\end{array}\right]$

| Voltage Log Ratio <br> Transfer Equation | $e_{0}=-K \log \left[\frac{e_{1}}{e_{2}} \times \frac{R_{2}}{R_{1}}\right]$ |
| :--- | :--- |
| Transfer Equation including <br> Error Terms | $e_{0}=-K\left[\log \left(\frac{\frac{e_{1}-E_{o s 1}}{R_{1}}-I_{b 1}}{\frac{e_{2}-E_{o s 2}}{R_{2}}}-I_{b 2}\right)+E_{o s 3}\right]$ |


| Parameter | Value |
| :---: | :---: |
| Signal Current, $\mathrm{i}_{1}{ }^{1}$ | 10 nA to $100 \mu \mathrm{~A}$ ( 4 decades) |
| Reference Current, $\mathrm{i}_{2}{ }^{1}$ | 100 nA to $100 \mu \mathrm{~A}$ ( 3 decades) |
| Log Conformity ${ }^{2}$ | $\pm 0.5 \%$ ( 2 decades, $\mathrm{i}_{2}$ constant) |
|  | $\pm 1.0 \%$ (4 decades, $\mathrm{i}_{2}$ constant) |
| Scale Factor, $\mathrm{K}^{\mathbf{1 , 3}}$ | $1 \mathrm{~V} \pm 1 \% \pm 0.04 \% /{ }^{\circ} \mathrm{C}$ |
| Bias Current, $\mathrm{I}_{\mathrm{b} 1}$ | 10pA, doubles $110^{\circ} \mathrm{C}$ |
| Bias Current, $\mathrm{I}_{\mathrm{b} 2}$ | $10 \mathrm{nA}, \max , \pm 1 \% /{ }^{\circ} \mathrm{C}$ |
| Signal Input Offset Voltage, $\mathrm{E}_{\text {os } 1}{ }^{3}$ | $\pm 1 \mathrm{mV}, \max , 25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ |
| Reference Input Offset Voltage, $\mathrm{E}_{\text {os2 }}$ | $0.5 \mathrm{mV}, \max , 30 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max$ |
| Output Offset, $\mathrm{E}_{\text {os } 3}{ }^{3}$ | $\pm 10 \mathrm{mV}, \max , 85 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ |
| Package Outline | F-6 |
| $\underset{(\mathrm{mm})}{\text { Case }}$ | $\begin{gathered} 1.5^{\prime \prime} \times 1.5^{\prime \prime} \times 0.4^{\prime \prime} \\ (38.1 \times 38.1 \times 10.1) \end{gathered}$ |
| Price (1-9) | \$75. |
| (10-24) | \$65. |

${ }^{1}$ Positive for positive inputs ( N type), negative for negative inputs ( P type).
${ }^{2}$ The log conformity specification is referred to input (R.T.I.). Note: $1 \%$ error R.T.I. is equivalent to 4.3 mV of error at output for $\mathrm{K}=1 \mathrm{~V}$.
${ }^{3}$ Externally trimmable.


Figure 1. Functional Block Diagram of Model 756
Figure 2. Photometry Application of Model 756

## ACCESSORIES <br> MODULAR POWER SUPPLIES



900 SERIES: GENERAL PURPOSE POWER SUPPLIES
The 900 series power supplies from Analog Devices have been widely accepted by designers as industry standards for reliability and performance. Useful in industrial and laboratory applications, these companion products to op amps are capable of delivering clean, well regulated power to IC and discrete op amps, digital converter products, and to transducer elements. These modular devices are available in molded plastic, aluminum and thermal-barrier packages. Most modules can be soldered directly into printed circuit boards or can be plugged into an optional mating socket.
Plastic molded cases are used on designs capable of dissipating up to 3 watts. Low thermal resistance aluminum cases are employed on supplies which dissipate between 3-6 watts. Supplies that can provide output power of over 10 watts are packaged in "thermal barrier" housings. The "thermal barrier"
design isolates the heat generating components from those that are heat sensitive and allows high power devices, like the 922 and 925 , to fit into standard $3.50^{\prime \prime} \times 2.50^{\prime \prime}$ profiles.
All designs are line operated. International voltage ratings are offered. Available models feature short circuit protection and current limiting (with over-voltage protection on 903, 905,922 ). Current output is $\pm 25 \mathrm{~mA}$ to $\pm 350 \mathrm{~mA}$ for dual outputs and 250 mA to 2 amps for single outputs. To service its customers, Analog Devices maintains an off-the-shelf stock for immediate delivery. Substantial OEM discounts are available.


## CHASSIS MOUNT SUPPLIES

This series of supplies consists of the same reliable designs as described above but input and output connections are made by a terminal strip rather than pins. They are intended for use in designs where it is either undesirable or impractical to utilize printed circuit boards or sockets. Mounting is readily accomplished by four threaded inserts on the bottom of the unit.

SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ and 115 VAC unless otherwise noted)

|  | Output Current ${ }^{2}$ | Model | Output <br> Error (Max) | Regulation |  | Temperature Coefficient ( ${ }^{\circ} \mathrm{C}$ ) | $\begin{gathered} \text { Ripple \& } \\ \text { Noise } \\ \text { RMS (Max) } \end{gathered}$ | Options ${ }^{4}$ | Package | Price(1-9) | $\begin{aligned} & \text { Price } \\ & (10-24) \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | $\begin{aligned} & 105 \text { to } 125 \\ & \text { VAC (Max) } \end{aligned}$ | $\begin{aligned} & \text { Load, } 0 \text { to } \\ & \text { 100\% (Max) } \end{aligned}$ |  |  |  |  |  |  |
| $\pm 15 \mathrm{~V}$ | @ 350 mA | 925 | $\pm 1 \%$ | 0.02\% | 0.02\% | 0.015\% | 0.5 mV | E, F, H | H-1 | \$99 | \$93 |
|  | @ 200 mA | 920 | $\begin{gathered} +300 \mathrm{mV} \\ -0 \mathrm{mV} \end{gathered}$ | 0.02\% | 0.02\% | $\begin{aligned} & 0.015 \% \\ & 0.015 \% \end{aligned}$ | 0.5 mV | E, F, H | HA-1 | \$72 | \$65 |
|  | (3) 200 mA | 970 | $\pm 2 \%$ | 0.05\% | 0.05\% | 0.015\% | 1 mV | E, F, H | J | \$79 | \$72 |
|  | @ 100 mA | 902 | $\begin{gathered} +300 \mathrm{mV} \\ -0 \mathrm{mV} \end{gathered}$ | 0.02\% | 0.02\% | 0.015\% | 0.5 mV | E, F, H, I | HA-1 | \$51 | \$49 |
|  | (a) 100 mA | 902-2 | $\begin{gathered} +300 \mathrm{mV} \\ -0 \mathrm{mV} \end{gathered}$ | 0.02\% | 0.02\% | 0.015\% | 0.5 mV | E, F, H, I | HB-1 | \$51 | \$49 |
|  | @ 100 mA | 952 | $\pm 2 \%$ | 0.05\% | 0.05\% | 0.015\% | 1 mV | E, F, H | J | \$58 | \$56 |
|  | @ 50 mA | 904 | $\begin{gathered} +200 \mathrm{mV} \\ -0 \mathrm{mV} \end{gathered}$ | 0.02\% | 0.02\% | 0.015\% | 0.5 mV | E, F, H, I | HB-1 | \$41 | \$40 |
|  | ( 25 mA | 915 | $\pm 1 \%$ | 0.2\% | 0.2\% | 0.015\% | 1 mV | E, F, H, I | HB-1 | \$24 | \$23 |
| $+5 \mathrm{~V}^{3}$ | ( ) 2000 mA | 922 | $\pm 1 \%$ | 0.02\% | 0.05\% | 0.015\% | 1 mV | E, F, H | H-1 | \$89 | \$83 |
|  | ( 1000 mA | 905 | $\pm 1 \%$ | 0.02\% | 0.05\% | 0.015\% | 1 mV | E, F, H | HA-1 | \$72 | \$69 |
|  | ( 1000 mA | 955 | $\pm 2 \%$ | 0.05\% | 0.15\% | 0.015\% | 2 mV | E, F, H | J | \$79 | \$76 |
|  | @ 500 mA | 903 | $\pm 1 \%$ | 0.02\% | 0.04\% | 0.015\% | 1 mV | E, F, H | HA-1 | \$51 | \$49 |
|  | @ 250 mA | 906 | $\pm 1 \%$ | 0.02\% | 0.04\% | 0.015\% | 1 mV | - | HB-1 | \$41 | \$40 |
| $\pm 12 \mathrm{~V}$ | (a) 240 mA | 921 | $\begin{gathered} +300 \mathrm{mV} \\ -0 \mathrm{mV} \end{gathered}$ | 0.02\% | 0.02\% | 0.015\% | 0.5 mV | E, F, H | HA-1 | \$72 | \$65 |
|  | ( 240 mA | 971 | $\pm 2 \%$ | 0.05\% | 0.05\% | 0.015\% | 1 mV | E, F, H | J | \$79 | \$72 |
|  | (a) 100 mA | 908 | $\pm 1 \%$ | 0.02\% | 0.02\% | 0.015\% | 1 mV | - | HB-1 | \$51 | \$49 |
|  | ( 50 mA | 909 | $\pm 1 \%$ | 0.02\% | 0.02\% | 0.015\% | 1 mV | - | HB-1 | \$41 | \$40 |
|  | ( 25 mA | 907 | $\pm 1 \%$ | 0.2\% | 0.2\% | 0.015\% | 1 mV | - | HB-1 | \$24 | \$23 |
| $\pm 18 \mathrm{~V}$ | @ 100 mA | 932 | $\pm 1 \%$ | 0.02\% | 0.02\% | 0.015\% | 1 mV | - | HA-1 | \$52 | \$49 |
|  | ( 50 mA | 935 | $\pm 1 \%$ | 0.02\% | 0.02\% | 0.015\% | 1 mV | - | HB-1 | \$41 | \$40 |
|  | (a) 25 mA | 931 | $\pm 1 \%$ | 0.2\% | 0.2\% | 0.015\% | 1 mV | - | HB-1 | \$24 | \$23 |
| $\pm 24 \mathrm{~V}$ | (a) 100 mA | 934 | $\pm 1 \%$ | 0.02\% | 0.02\% | 0.015\% | 1 mV | - | HA-1 | \$68 | \$65 |
|  | ( ${ }^{\text {a }} 50 \mathrm{~mA}$ | 933 | $\pm 1 \%$ | 0.02\% | 0.02\% | 0.015\% | 1 mV | - | HB-1 | \$52 | \$49 |



## MODEL 194 AMPLIFIER MANIFOLD

The model 194 manifold is ideal for experimenting, breadboarding, and/or teaching with op amps. Completely selfcontained, it includes a $\pm 15$ VDC 100 mA power supply, and accepts up to 5 amplifiers in the popular 7 pin "Q" case configuration. Adapters are available for other configurations and provisions are made for a balance potentiometer for each amplifier. The unit is designed for maximum flexibility, with all connection points $3 / 4 \mathrm{in}$. apart. Price is $\$ 325$ each (1-9), substantially less in higher quantities.
MODEL 950: POWER SUPPLY MANIFOLD
This manifold permits use of the 900 series modules on the design bench. In combination with these supplies the 950 provides a safe, convenient, and inexpensive bench supply for breadboarding, testing, or general laboratory use. Price is $\$ 18$ each (1-9).

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## LINEAR INTEGRATED CIRCUITS

## INTRODUCTION

The integrated circuits specified on these pages are indicative of a commitment to product expertise in IC technology concurrent with Analog Devices' position of leadership in analog and converter modules. Achieving the optimum price/performance product is our goal; combining almost 10 years of analog product design is our vehicle. In addition to that expressed by our products, our IC commitment is manifested in two other important ways . . . communication and cooperation.
Because we manufacture devices that are a cut above the usual IC in performance and applicability, and because we realize that your interest in these products is indicative of your need for excellent system performance, our service goes beyond product, price and delivery.
To get the most out of our circuits, you must clearly know how best to use them. This dictates the need for a high level of communication . . provided by the completeness of our product data sheets and application notes, and by a team of circuit design-oriented engineers who are well versed in solving product and applications problems. And if our products do not meet the requirements of your system application, if a max drift must be lower or a minimum gain higher, or if you need special device processing, we are ready to cooperate to meet your requirement.
Our broad line of IC products is presented in this section for the designer who specifically requires microcircuit products. For applications in which the choice of microcircuits is not dictated, these products are also presented on a functionally comparative basis with Analog Devices' modular amplifiers, converters, and multipliers in these product sections.
We offer field-effect (FET), bipolar, and thin-film technologies for our IC products, to provide the ultimate in application possibilities. Our FET devices include CMOS, MOS, and JFET products to provide true state-of-the-art performance. For users who assemble their own hybrids, most of our IC products are available in chip form. In addition, our Resistor Products Division offers a complete line of coated substrates and precircuits for users who desire to do their own etching. The thin-film resistor networks are also available either in chip form, or packaged in machine-mountable DIPs or Flatpaks.
Introductory to the product descriptions, we have provided below: a brief overview of our current state-of-the-art production capability; a product line profile; and an abbreviated reference to the MIL 883 reliability standard to which our IC's may be specified.

## IC TECHNOLOGY AT ANALOG DEVICES: FIELD-EFFECT, BIPOLAR, AND THIN-FILM

Our broad line of linear IC's is produced with a combination of design, processing, test capabilities, and innovations, with stringent process control.
High dersity CMOS processing combines the low power dissipation of conventional CMOS with a two-layer metal process
for increased circuit packing density, the highest breakdown voltages technologically feasible with CMOS, and SiliconNitride passivation for increased stability and reliability.
Active-operation laser trimming of thin-film resistors deposited on the monolithic chip is an IC technology breakthrough unique with Analog Devices. It is used to manufacture the AD5 32 internally trimmed monolithic multiplier and the AD562, 12-bit, IC digital to analog converter. Conventional laser trimming is also performed on thin-film resistors depos ited on ceramic substrates to permit FET op amp offset voltag to be specified below 1.0 millivolt.
Thin film deposition on monolithic chips results in resistors that match within 50 ppm and track within 5 ppm to produce voltage drifts below $0.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ and multiplication error below $2 \%$ over the military temperature range.
Dual FET fabrication on a single chip employs uniform epitaxial, low dislocation diffusion techniques. and silicon nitride passivation. This produces devices with ultra low gate leakage currents below 0.1 pA , extremely low noise, tight matching characteristics, with linear tracking over temperature guaranteeing a temperature drift nonlinearity (TDN) of $\pm 1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$.

Super beta transistors produce gains of 2500 to 3000 with breakdown voltages of 20 to 35 volts.
Hybrid assembly techniques provide circuits that combine the best individual characteristics of FET and bipolar chips into operational amplifiers that offer 250 femtoamp input currents and 6 volt $/ \mu \mathrm{sec}$ slew rates.
Thermal balancing of the chip layout is a primary design criterium for all circuits to minimize the effects of the power dissipation which causes thermal feedback, mismatching the critical input stage.
Stringent in-process control and $100 \%$ stress conditioning include pre-cap visual chip and bonding inspection, high temperature storage, high impact acceleration, and temperature cycling to eliminate defective units before they reach the customer.
Computerized and fully automatic equipment tests the circuits for all guaranteed DC parameters, and combines with a user-oriented philosophy to produce such nononsense criteria as measuring FET op amp gain with the offset voltage automatically nulled, and measuring multiplier accuracy in all four quadrants at three temperatures.
Thus, Analog Devices has uniquely combined the numerous design, processing, and manufacturing capabilities necessary to produce its broad line of high performance integrated circuits.

## PRODUCT PROFILES

The IC product line is divided into several functional area: such as operational amplifiers, multiplier/dividers, converters, resistors and switches. Within these areas are more than three dozen product series with more than 250 standard variations.

## FET Input Operational Amplifiers

The AD503, AD506, AD513, AD514, AD516, AD523, AD528, and AD540 series all share the common functional characteristic of being able to accurately measure low level currents or small voltages from high impedance sources where bias current can be a primary source of error. Their FET inputs provide fully warmed-up maximum bias currents as low as 0.25 pA (AD523K), with offset voltages below 1.0 mV (obtained with internal laser trimming) (AD506L), gains of 20 k to 50 k and CMRR's of 70 to 80 dB . Offset voltage drifts with temperature are guaranteed as low as $10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ (AD506L), and vary very little with $\mathrm{V}_{\mathrm{OS}}$ trimming. These amplifiers have a typical small signal bandwidth of 1.0 MHz and a settling time to $0.1 \%$ of $10 \mu \mathrm{sec}$. Higher first stage current levels permit minimum slew rates of $3.0 \mathrm{~V} / \mu \mathrm{sec}$ for internally compensated devices, and as high as $50 \mathrm{~V} / \mu \mathrm{sec}$ (AD513) where external compensation is possible. Lower first stage current levels reduce voltage noise to $5 \mu \mathrm{~V}$ p-p (AD5 14).

## High Accuracy Operational Amplifiers

The AD504 and AD508 series, and the AD301AL and AD741 J/K/L/S are specially designed, processed, and tested to achieve the highest possible accuracy and stability with both temperature and time, and permit error budgets as low as a few parts per million at surprisingly low cost. They provide gains ranging from 50 k to more than 1 million (AD504, AD508), offset voltages as low as 0.5 mV , offset voltage drifts from $20 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ to below $0.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, bias currents from 200 nA to less than 15 nA (AD508), offset currents as low as 1.0 nA , and minimum CMRR's from 80 to 110 dB . Typical noise is 1.0 to $3.0 \mu \mathrm{~V}(\mathrm{p}-\mathrm{p})$ in the 0.01 Hz to 10 Hz bandwidth, and the AD504M guarantees maximum $0.6 \mu \mathrm{~V}(\mathrm{p}-\mathrm{p})$ noise from 0.1 to 10 Hz . An added benefit of the thermally balanced design of these amplifiers is their excellent output performance of up to $\pm 10 \mathrm{~V}$ minimum into a $1 \mathrm{k} \Omega$ load at $+70^{\circ} \mathrm{C}$. Although these amplifiers are basically 300 kHz to 1.0 MHz small signal bandwidth devices, several may be externally compensated, permitting considerable variation in bandwidth and slew rate.

## Instrumentation Amplifiers

The AD520 is the industry's first IC instrumentation amplifier. It is a closed loop gain block with differential inputs and an accurately predictable input-to-output gain relationship. The AD520's performance is unlike that of conventional IC op amps because of an internal feedback design which permits gain adjustment from 1 to 1000 by varying the value of a single resistor. High $\mathrm{Z}_{\mathrm{in}}$ is achieved at both inputs and both $\mathrm{Z}_{\mathrm{in}}$ and CMRR remain high at all gain settings.

## Fast, Wideband Operational Amplifiers

The AD505, AD507, AD509, AD518, and AD528 operational amplifiers are specifically designed for applications requiring wide bandwidth, high slew rate, fast settling time to high accuracy, predictable operation and low cost. Their excellent ac performance is characterized by small signal bandwidths up to 35 MHz (AD507), slew rates above $120 \mathrm{~V} / \mu \mathrm{sec}$ (AD505), and settling times guaranteed below $2 \mu \mathrm{sec}$ to $0.01 \%$ (AD509K). A high level of dc accuracy is maintained with gains above 80k, offset voltages below 1.0 mV , and input bias currents below 10 pA . Because these amplifiers are optimized for wideband, fast settling operation, certain practical stabilization and interconnection techniques are described in their specification sheets to insure proper operation and to minimize user experimentation.

## General Purpose DC Operational Amplifiers

The AD101A, AD108, AD108A, AD502, and AD741 operational amplifiers are characterized by good to excellent dc per-
formance provided by medium gain of 20 k to 50 k , offset voltages below 7.5 mV , bias and offset currents as low as 0.2 nA (AD108/108A), and common mode rejection ratios above 80 dB . They typically have a small signal bandwidth of 1.0 MHz , slew rates of 0.3 to $1.0 \mathrm{~V} / \mu \mathrm{sec}$, and settling times to $0.1 \%$ of $10 \mu \mathrm{sec}$. Several of them may be externally compensated, and their ac performance can be significantly improved by applying various compensation schemes. In keeping with their general purpose applicability, these amplifiers are supplied in a number of packages, including the TO-99 metal can, TO-116 ceramic DIL, plastic mini-DIP, and TO-91 flat package.

## Multipliers/Dividers

The AD5 30, AD5 31, AD532, and AD5 33 provide Analog with several IC multiplier firsts. The AD5 30 is the industry's first IC multiplier to include the transconductance multiplying element, stable reference, and output amplifier on a single monolithic chip. The AD531 is the first to provide a variable scale factor, and the AD532 is the first internally trimmed monolithic multiplier. The devices multiply and square in 4 quadrants; divide in 2 quadrants, and square root in one quadrant; the AD5 30 and AD5 32 with a fixed scale factor of 10 , and the AD5 31 with a variable scale factor of kIz in volts. When multiplying, the AD5 30 provides the transfer function $\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\mathrm{X}} \cdot \mathrm{V}_{\mathrm{Y}} / 10$, the AD532, because of its differential inputs, $\mathrm{V}_{\text {OUT }}=\left(\mathrm{V}_{\mathrm{X}_{1}}-\mathrm{V}_{\mathrm{X}_{2}}\right)\left(\mathrm{V}_{\mathrm{Y}_{1}}-\mathrm{V}_{\mathrm{Y}_{2}}\right) / 10$, and the AD531 $\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\mathrm{X}} \cdot \mathrm{V}_{\mathrm{Y}} / \mathrm{V}_{\mathrm{Z}}$ with $\mathrm{V}_{\mathrm{Z}}$ set by an external resistor, or varied dynamically by an externally derived reference current. Both the AD530 and AD531 series are specified for max multiplying errors (with external trimming) as low as $0.5 \%$ at $+25^{\circ} \mathrm{C}, 1.5 \%$ from 0 to $+70^{\circ} \mathrm{C}$, and $3.0 \%$ from $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$. The AD5 32 (requiring no external trimming) is specified for errors below $1 \%$ at $+25^{\circ} \mathrm{C}$, and $4 \%$ from $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$. The AD5 33 provides the user with a low cost version of the AD530, also with three levels of accuracy and a fullMIL range device.

## Converter Products

As the world's first IC digital-to-analog converter with true 12-bit accuracy, the AD562 represents a bold new dimension in Analog Devices' IC technology. By combining a precision switch chip with a compatible, high stability, thin-film resistor chip, monotonic $\mathrm{d} / \mathrm{a}$ conversion is obtained over the entire operating temperature range. The device is TTL and CMOS compatible with either unipolar or bipolar outputs. With the addition of an external op amp and reference to complete the DAC function, the AD562 settles to $1 / 2$ LSB in less than $3.5 \mu \mathrm{sec}$.

The key to the AD562's accuracy lies in active laser trimming of the resistor ladder network; Analog Devices' computercontrolled laser trimming can trim up to 18 resistors to 20 ppm accuracy in 60 seconds. This technology, which was developed by Analog Devices, will be responsible for an entire line of converters, soon to be introduced.

The world's first CMOS monolithic D/A converter, the AD7520, features 8, 9, or 10-bit accuracy, and $0.5 \mu$ s to $0.05 \%$ current settling time. The AD7521 offers all the features of the AD7520, but provides 12 bits of resolution for applications requiring 10-bit linearity.

Analog's IC conversion components, which are used in our own modular D/A and A/D converters, provide the user with a do-it-yourself kit for the construction of very small and reliable D/A and A/D converters, which provide extremely high accuracy and resolution over the military temperature range. The components include integrated circuit switches and associated
thin-film resistor networks which form the heart of D/A and A/D converters having 8-to-12-bit accuracy.
Two basic series are available: the AD550 switch uses current switching techniques, and is recommended where accuracy requirements are paramount; the AD555 quad voltage switch is optimized for applications where both digital and analog signals vary, such as digital-to-synchro conversion or multiplying DAC applications.
Compatible thin-film resistor networks for binary current summing are also available: the AD850 (12-bit resolution), and the AD852/853 (8 bits/4bits) set for use with the AD550; the AD855 is a 12 -bit R/2R network for voltage switching, and is used with the AD555.

## Dual Monolithic FET's and Transistors

Analog Devices has applied precise, linear IC production processes coupled with advanced silicon nitride passivation techniques in the fabrication of high performance dual monolithic transistors. Consequently, it is now possible to routinely fabricate (with high yields) dual monolithic transistors which provide high breakdown voltages, and closely matched parameters.

## ADVANTAGES OF MONOLITHIC DUAL TRANSISTORS

Dual monolithic transistor designs offer significant advantages over two-chip duals.

1. Thermal Tracking is improved for two reasons:
a. The temperature gradient which exists between devices is very small due to their close proximity and excellent thermal coupling characteristics.
b. There is a higher probability that the device parameters will be closely matched if both devices are located on the same die and diffused and processed together.
2. Excellent Thermal Transient Rejection is another feature of a monolithic dual. The differential offset voltage caused by a thermal transient from an external spot heat source will be significantly reduced by the low thermal resistance between devices. In addition, the time required to recover from an offset caused by an external thermal transient or by internal differential dissipation is greatly reduced.
3. High Reliability is an inherent advantage of monolithics over two-chip type devices since no extra chip handling beyond the normal wafer sort and assembly is performed.
4. Low Cost can be passed on due to less assembly handling, and the fact that the matching is a result of wafer yields in lieu of tedious and costly sorting procedures.

## ADVANTAGES OF MONOLITHIC DUAL FET'S

Early investigations showed that the isolated matched junction FET could not be produced because of restrictions
imposed by the nonuniformity of the epitaxial layer. However, recent improvements in the control of the epitaxial silicon layer uniformity allow noninterdigitated devices to be made at high yields, thereby eliminating the restrictions imposed by the common back gate of typical interdigitated structures. In addition, the use of a proprietary deposited diffusion technique provides gate diffusion uniformities heretofore unattainable from standard gas diffusion sources. The uniform concentration of doping in the gate diffusion results in reduced variation in gate voltage and allows a high yield of matched devices with low-offset and significantly-improved temperature characteristics. At the same time, large improvement in the leakage and gate current characteristics can be obtained by careful control of the other diffusions and formation of the surface passivating layer. Analog Devices' new technique utilizing silicon nitride and low-dislocation diffusion techniques has allowed the routine manufacture of devices with gate currents below 0.1 pA .

TRAK-FETS offer a myriad of advantages over conventional two-chip (hybrid) duals.

1. Thermal Tracking linearity is so excellent that a new specification, the TDN (Temperature Drift Nonlinearity), was created to characterize them. It is obtained by making a three-point temperature measurement and comparing the $\Delta \mathrm{V}_{\mathrm{GS}}^{1-2} 1 \Delta \mathrm{~T}$ for the two intervals.
2. Low Gate Leakage at normal circuit operating voltages (i.e., $15 \mathrm{~V} \mathrm{~V}_{\mathrm{DS}}$ ) is another advantage of the processing used by Analog Devices. For example, the AD830 series provides input leakages as low as 0.1 pA .
3. Thermal Transient Rejection is improved since the temperature gradient which exists between devices is small due to their close proximity and excellent thermal matching characteristics. In addition, the time required to recover from an offset caused by an external thermal transient or by internal differential dissipation is greatly reduced.
4. Tight $G_{f s}$ and $Y_{o s}$ Matching. Due to proper geometry selection in the design, the $\mathrm{G}_{\mathrm{fs}}$ and (especially) the $\mathrm{Y}_{\mathrm{os}}$ matching is exceptionally good. Furthermore, since these parameters are determined largely by channel geometry, they don't change appreciably for large variations of operating current--allowing the designer additional latitude in minimizing common mode errors for differential applications.
5. High Reliability is an inherent advantage of monolithic duals, since no chip handling beyond normal wafer sort and assembly is performed.
6. Low Cost. Eliminating costly and tedious assembly handling and sorting procedures in favor of a wafer "yield" system improves manufacturing efficiency.

## CMOS TECHNOLOGY AT ANALOG DEVICES

A state-of-the-art technology - Complementary Metal Oxide Semiconductor (CMOS) - is used for a new generation of analog and digital/analog high density monolithic integrated systems, which are now available from Analog Devices. This technology allows simpler designs and greatly reduced power dissipations for a particular function.
The complete line of high performance CMOS d/a converters, switches, and multiplexers result from developed expertise in state-of-the-art process technology. The entire CMOS product line is fabricated, featuring:

- a sophisticated two-layer metal process for maximum circuit packing density.
- highest breakdown voltages technologically feasible in CMOS processing.
- Silicon-Nitride passivation for increased stability and reliability.
- ion-implantation for exact gate surface control.


## Monolithic CMOS Converters - D/A

The industry's first CMOS monolithic D/A converter, the AD7520, features 8,9 , and 10 bits of linearity, 2 ppm of FSR/ ${ }^{\circ} \mathrm{C}$ maximum nonlinearity, fast current settling time, and low power dissipation of typically 20 mW . TTL, DTL, and CMOS compatibility allow digital control over a wide +5 V to +15 V operating voltage supply range.
The AD7521 offers all the features of the AD7520, but provides 12 bits of resolution with 10 -bit linearity for specific applications, such as digitally controlled filters.

## Monolithic CMOS Switches

A complete line of CMOS switches performs a myriad of switching functions that can be CMOS, TTL, or DTL controlled. All switching functions offer extremely low power dissipation (typically $30 \mu \mathrm{~W}$ ), low "ON" resistance, and moderate to fast switching speeds.
The AD7510/AD7511 features four independent CMOS switches (the AD7511 offers inverted control logic). The AD7512 provides a dual SPDT function. The AD7513 is a dual SPST plug-in replacement for the DG200. The AD7516 is an improved second source of the CD4016A quad SPST and the AD7519 offers a quad SPDT current steering function for D/A converters, which require fast switching speeds.

## Monolithic CMOS Multiplexers

The product line includes two 8-channel analog multiplexers, AD7501 and AD7503. The AD7503 offers inverted " $E_{N}$ " logic for specific applications.
The AD7502 is a 4-channel differential multiplexer to handle applications requiring good common-mode-rejection. The AD7506, 16-channel multiplexer, and the AD7507, 8-channel differential multiplexer, are replacements for the DG506 and DG507.
The multiplexer product line features CMOS, DTL, and TTL logic control compatibility, binary address control, low "ON" resistance, and low power dissipation ( $30 \mu \mathrm{~W}$ for the AD7501/ $7502 / 7503$, and 1.5 mW for the AD7506/7507, typically).

## THIN-FILM RESISTORS

Analog Devices' nichrome thin-film resistor networks are fabricated from our own coated substrates, allowing the entire process to be under our control. Valuable benefits include the advantages of high-yield batch-processing techniques, highvolume assembly, and automatic laser-trimming. Our advanced technology contributes to high performance and reliability; our DIP and Flatpak configurations provide efficient use of board space. Chip versions facilitate hybrid assembly.

## NiCr Thin Film Coated Substrates

The AD1900 series standard coated substrate products provide the industry's widest selection of resistive/conductive substrates with sheet resistivities from 50 to 500 ohms per square, sizes $0.025^{\prime \prime}$ square to $3.5^{\prime \prime}$ square, power dissipation to 50 watts/ square inch ratio resistance stability to $\pm 0.01 \% /$ year at $+25^{\circ} \mathrm{C}$, certifiable to MIL-STD-9858A, and tracking temperature coefficient of resistance to $\pm 0.5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$. User designed parameters can be fabricated upon request. Two and three film systems are offered.

## NiCr Thin Film Precircuits

The thin film precircuit is a microcircuit innovation consisting of resistor-conductor patterns, on a ceramic chip. Using Analog Devices thin film coated substrates as a foundation, user designed precircuits can be rapidly fabricated in production quantities to display the following characteristics: resistance ratio tracking to $\pm 0.001 \%$; tracking TCR to $\pm 0.5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$; up to 250 megohms per square inch resistance density; trim range up to several orders of magnitude; 50 watts/square inch power density; several hundred elements per square inch; line control to $\pm 0.0001$ inch; and rapid delivery.
The thin film precircuit can be utilized to solve a wide variety of design problems, such as: a mother board to hybridize a function; actively trimmable element of a circuit; resistor functions to be bonded onto a hybrid mother board and network simplification by packaging many resistors into a machine mountable package.

## User Designed Resistor Networks

The next level of fabrication of thin film precircuits is the fully packaged resistor network. Analog Devices has the facilities, technology and 6 years of experience in fabricating highly reliable precision resistor networks which have been in constant use under the most stringent environmental conditions. Our resistor networks can be supplied in a wide variety of packages such as: TO-100, TO-99, TO-116, TO-87; 8, 14, 16, 24 DIP's, Flatpaks etc., to satisfy virtually every design requirement.
You may find it useful to investigate our complete and ever expanding standard product line prior to your decision to proceed with a dedicated network. The combination of one or more standard products may allow you to obtain the proper function, at a lower cost, and with off the shelf availability. If, however, you require a custom design, Analog Devices' Resistor Products Division has the engineering experience, layout sophistication, processing skill, fabrication technology, and inclination to respond rapidly to your product requirements.

## Standard Resistor Network Products

Described in the following pages, in capsule form, is the nucleus of a complete standard thin film resistive function product offering. While the resistor is as old as the industry itself, our concerted effort to provide this broad range of networks, with the excellent NiCr film characteristics at user oriented prices, in production quantities and with rational delivery, will irrevocably alter the traditional approach to circuit design. Look for additional product offerings throughout the year that will complement the listing here.

DIVIDERS/ATTENUATORS - Precise tracking can be obtained with NiCr characteristics. The AD1803, providing up to 5 orders of magnitude within a single 16 pin DIP, is an indication of the advance provided by our thin film technology. The AD1800 quad divider can be obtained for use with or without TrimpotsTM. The AD1807 switchable binary attenuators offer precise tracking with the flexibility needed to replace Trimpots ${ }^{T M}$.

CIRCUIT ELEMENT BLOCKS - Network simplification is made feasible by utilizing resistive element blocks which are user interconnected. The product listing here is the initial steps toward a complete line of multipurpose functions.

## Binary and R/2R Ladder Networks

Analog Devices has been for some time a highly respected ladder network supplier. Our present AD850, 851, 852/3, 855, 856 products have been in continuous use for up to 4 years in industrial and hi-rel applications. Now, in addition to the original product line, we are introducing here our AD1850, 1851, 1852/3, 1855, 1856 industrial ladder networks for use in systems where high accuracy is required, but operation is limited to within a few degrees of $+25^{\circ} \mathrm{C}$. The two series offer maximum flexibility for cost effective designs.

## MIL STANDARD 883

Analog Devices manufactures its modular, converter, and integrated circuit products to standards of quality that meet and consistently exceed our customers' requirements for high reliability applications in military, aerospace, instrumentation, and industrial systems. Because of their minimum number of interconnections, integrated circuits offer the highest inherent reliability to the user. We hermetically sealed packages, low component count, and optimize this reliability by adherence to exact manufacturing control, and to the processing and inspection requirements of MIL-STD-883, a government processing, testing, and inspection standard that defines the following levels of screening for integrated circuits.

1. Class A - "Devices intended for use where maintenance and replacement are extremely difficult or impossible and reliability is imperative."
2. Class B - "Devices intended for use where maintenance and replacement can be performed, but are difficult and expensive, and where reliability is vital."
3. Class C - "Devices intended for use where maintenance and replacement can be readily accomplished and downtime is not a critical factor."

Further guidance is provided:
"Since it is not possible to prescribe an absolute level of quality or reliability which would result from a particular screening level or to make a precise value judgment on the cost of a failure in an anticipated application, three levels have been arbitrarily chosen. The method provides flexibility on the choice of conditions and stress levels to allow the screens to be further tailored to a particular source, product or application based on user experience. The user is cautioned to collect experience data so that a legitimate value judgment can be made with regard to specification of screening levels. Selection of a level better than that required for the specific product and application will, of course, result in unnecessary expense and a level less than that required will result in an unwarranted risk that reliability and other requirements will not be met. In the absence of specific experience data, the Class B screening level is recommended for military applications." Where particularly specified by the user, Analog Devices will supply its integrated circuits screened to Class A, B or C of MIL-STD-883 Method 5004. Standard highreliability products, denoted by a / 883 suffix on the part number (e.g., AD530S/883), are screened to Level B.

Analog Devices resistor networks are fabricated with process control and manufacturing documentation to meet or exceed the screening requirements of MIL-STD-883. Our standard screening procedures are described by our DWG \#16-100455 as listed below. MIL-STD-883, Method 5004, with notice 4 applies:

1) INTERNAL VISUAL - Method 2010.1, Condition B
2) STABILIZATION BAKE - Method 2008, Condition C ( $24 \mathrm{hrs} . \min @ 150^{\circ} \mathrm{C}$ )
3) TEMPERATURE CYCLE - Method 1010, Condition C ( 10 cycles, $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ )
4) CONSTANT ACCELERATION - Method 2001, Condition $D(20,000 \mathrm{~g}$ in Y1 plane)
5) FINE LEAK TEST - Method 1014, Condition A (Limit $5 \times 10^{-7} \mathrm{cc} / \mathrm{sec}$ )
6) GROSS LEAK TEST - Method 1014, Condition C, Step 1 (FC-43 @ $125 \pm 5^{\circ} \mathrm{C}$ )
7) BURN-IN - Method 1015, Condition B (Rated power @ $125^{\circ} \mathrm{C}$ for 168 hours)
8) ELECTRICAL TEST - per applicable part test specification.

# HIGH ACCURACY FET-INPUT OP AMP <br> PIN CONFIGURATION <br> AD506 

Top View


TO-99

## GENERAL DESCRIPTION

The AD506J, AD506K, AD506L and AD506S are high accuracy FET-input op amps which combine the low current characteristics typical of FET amplifiers with the low initial offset voltage and offset voltage stability of bipolar amplifiers. Active laser trimming and close matching of circuit elements provide maximum warmed-up offset voltage below 1.0 mV , maximum offset voltage drift of $10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, and warmed-up bias current
below 5 pA max. Other excellent characteristics include open loop gain above 75,000 and minimum CMRR of 80 dB . User-oriented circuit design and testing philosophy insure that full advantage can be taken of the high performance specifications of the AD506. Offset voltage nulling is accomplished without affecting the operating current of the FET's and results in small changes in temperature drift characteristics. For example, the drift induced by nulling the AD506 is only $\pm 0.8 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ per millivolt of nulled offset voltage. Further, the AD506 is guaranteed to meet its maximum $\mathrm{I}_{\mathrm{b}}$ and $\mathrm{V}_{\text {OS }}$ specs after full device warm-up caused by self-heating of the chip due to internal power dissipation. The bias current is specified as a maximum at each input, not as the average of the two inputs. Finally, gain is measured with the offset voltage nulled. Nulling a FET-input op amp can cause the gain to decrease below its specified limit. The minimum gain of the AD506 is guaranteed with $\mathrm{V}_{\text {OS }}$ both nulled and unnulled. All models are supplied in the TO-99 metal can package. The AD506J, K and L are specified for operation from 0 to $+70^{\circ} \mathrm{C}$; the AD506S from $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$.

ELECTRICAL SPECIFICATIONS (Typical at $+25^{\circ} \mathrm{C}$ and $\pm 15 \mathrm{VDC}$, unless otherwise noted)

| Parameter | AD506J | AD506K | AD506L | AD506S |
| :---: | :---: | :---: | :---: | :---: |
| Open Loop Gain (Note 1) |  |  |  |  |
| $\mathrm{V}_{\text {OUT }}= \pm 10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega$ | 20,000 min | 50,000 min | 75,000 min | 50,000 min |
| $\mathrm{T}_{\mathrm{A}}=\min$ to $\max$ | 15,000 min | 40,000 min | 50,000 min | 25,000 min |
| Output Characteristics |  |  |  |  |
| Voltage @ $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=\min$ to max | $\pm 10 \mathrm{~V}$ min | * | * | * |
| ( ) $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=\min$ to max | $\pm 12 \mathrm{~V}$ min | * | * | * |
| Load Capacitance (Note 2) | 1000 pF | * | * | * |
| Short Circuit Current | 25 mA | * | * | * |
| Frequency Response |  |  |  |  |
| Unity Gain, Small Signal | 1.0 MHz | * | * | * |
| Full Power Response | 100 kHz | * | * | * |
| Slew Rate, Unity Gain | $3.0 \mathrm{~V} / \mu \mathrm{sec} \mathrm{min}$ | * | * | * |
| Settling Time, Unity Gain | $10 \mu \mathrm{sec}$ | * | * | * |
| Input Offset Voltage (Note 3) | 3.5 mV max | 1.5 mV max | $1.0 \mathrm{mV} \max$ | 1.5 mV max |
| vs. Temperature, $\mathrm{T}_{\mathrm{A}}=\min$ to $\max$ | $75 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max | $25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max | $10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max | $50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max |
| vs. Supply, $\mathrm{T}_{\mathrm{A}}=\min$ to $\max$ | $200 \mu \mathrm{~V} / \mathrm{V}$ max | $100 \mu \mathrm{~V} / \mathrm{V}$ max | $100 \mu \mathrm{~V} / \mathrm{V}$ max | $100 \mu \mathrm{~V} / \mathrm{V}$ max |
| Input Bias Current |  |  |  |  |
| Either Input (Note 4) | $15 \mathrm{pA} \max$ | 10 pA max | 5 pA max | $10 \mathrm{pA} \max$ |
| Input Impedance |  |  |  |  |
| Differential | $10^{11} \Omega \\| 2 \mathrm{pF}$ | * | * |  |
| Common Mode | $10^{12} \Omega \\| 2 \mathrm{pF}$ | * | * | , |
| Input Noise |  |  |  |  |
| Voltage, 0.1 Hz to 10 Hz | $15 \mu \mathrm{~V}$ (p-p) | * | * |  |
| $\mathrm{f}=10 \mathrm{~Hz}$ | $280 \mathrm{nV} / \sqrt{ } \mathrm{Hz}$ | * | * | * |
| $\mathrm{f}=100 \mathrm{~Hz}$ | $70 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ | * | * | * |
| $\mathrm{f}=1 \mathrm{kHz}$ | $25 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ | * | * | * |
| Input Voltage Range |  |  |  |  |
| Differential | $\pm 4 \mathrm{~V}$ | * | * | * |
| Common Mode, $\mathrm{T}_{\mathrm{A}}=\min$ to max | $\pm 10 \mathrm{~V}$ min | ${ }^{*}$. | ${ }^{*}$. | ${ }^{*}$ * |
| Common Mode Rejection, $\mathrm{V}_{\mathrm{in}}= \pm 10 \mathrm{~V}$ | 70 dB min | 80 dB min | 80 dB min | 80 dB min |
| Power Supply |  |  |  |  |
| Rated Performance | $\pm 15 \mathrm{~V}$ | * | * | * ${ }^{*}$ |
| Operating | $\pm(5$ to 18$) \mathrm{V}$ | * | * | \pm (5 to 22$) \mathrm{V}$ |
| Quiescent Current | 7 mA max | * | * | * |
| Temperature |  |  |  |  |
| Operating, Rated Performance Storage | $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \\ -65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C} \end{gathered}$ | * | * | $-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C}$ |
| Price (1-24) | \$13.00 | \$15.50 | \$24.00 | \$26.50 |
| (25-99) | \$11.00 | \$12.80 | \$19.20 | \$21.80 |
| (100-999) | \$9.50 | \$11.00 | \$16.00 | \$17.60 |

1.Open Loop Gain is specified with $\mathrm{V}_{\mathrm{OS}}$ both nulled and unnulled. 2.A conservative design would not exceed 750 pF of load capacitance. 3.Input offset voltage specifications are guaranteed after 5 minutes of operation at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.
4.Bias current specifications are guaranteed after 5 minutes of operation at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$. For higher temperatures, the current doubles every $+10^{\circ} \mathrm{C}$.
*Specifications same as for AD506J.

# HIGH SPEED FET-INPUT OP AMPS AD513, AD516 

## GENERAL DESCRIPTION

The AD513 and AD516 high speed FET op amps combine high DC accuracy with excellent dynamic response by utilizing the flexibility of external compensation. With simple lag compensation, the AD513 and AD516 achieve slew rate of $20 \mathrm{~V} / \mu \mathrm{sec}$, and gain bandwidth of 1 MHz at unity gain and 10 MHz for gains greater than 100 . With feedforward compensation a slew rate of $50 \mathrm{~V} / \mu \mathrm{sec}$ and gain bandwidth of 30 MHz can be achieved. High accuracy DC specifications in clude max bias current as low as 20 pA , a minimum gain of 50,000 , and CMRR of 80 dB .

The AD513 is suggested for all general purpose FET input amplifier requirements where low cost and frequency response flexibility are of prime importance. The AD516, with specifications otherwise similar to the AD513, offers significant improvement in offset voltage by supplementing the AD513 configuration with internal laser trimming of thin film resistors to provide typical offset voltages below 1 mV .
The devices are also fully short circuit protected and can be externally offset voltage nulled. All the circuits are supplied in the TO-99 package in the same pin configuration as the AD101A and AD108/108A. The AD513J/AD516J and $\mathrm{AD} 513 \mathrm{~K} / \mathrm{AD} 516 \mathrm{~K}$ are specified for 0 to $+70^{\circ} \mathrm{C}$ temperature range operation; the AD513S/AD516S for operation from $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$.

## PIN CONFIGURATION

Top View
TYPICAL COMPENSATING SCHEMES


TO-99
Offset Nulling Scheme


| Gain (Inv) | 1 | 1 | 10 | 10 | 10 | 100 | 100 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathrm{R}_{1}(\Omega)$ | 10 k | 10 k | 10 k | 1 k | 1 k | 1 k | 100 |
| $\mathrm{R}_{2}(\Omega)$ | 10 k | 10 k | 100 k | 10 k | 10 k | 100 k | 10 k |
| $\mathrm{C}_{1}(\mathrm{pF})$ | 30 | 1 | 8 | 1 | 0 | 1 | 0 |
| $\mathrm{C}_{2}(\mathrm{pF})$ | 0 | 12 | 0 | 12 | 8 | 0 | 39 |
| $\mathrm{C}_{3}(\mathrm{pF})$ | 0 | 150 | 0 | 0 | 150 | 0 | 0 |
| $\mathrm{BW}^{\mathrm{BW}}(\mathrm{kHz})$ | 1000 |  |  |  |  |  |  |
| Slew Rate $(\mathrm{V} / \mu \mathrm{s})$ | 5 | 1000 | 500 | 1000 | 1000 | 100 | 000 |

ELECTRICAL SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ and $\pm 15$ VDC unless otherwise specified.)

| Parameter | AD513J/AD516] | AD513K/AD516K | AD513S/AD516S |
| :---: | :---: | :---: | :---: |
| Open Loop Gain (Note 1) |  |  |  |
| $\mathrm{V}_{\text {OUT }}= \pm 10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega$ | 20,000 min | 50,000 min | 50,000 min |
| $\mathrm{T}_{\mathrm{A}}=\min$ to $\max$ | 15,000 min | 40,000 min | 40,000 min |
| Output Characteristics |  |  |  |
| Voltage at $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=\min$ to max | $\pm 10 \mathrm{~V}$ min | * | * |
| at $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=$ min to max | $\pm 12 \mathrm{~V}$ min | * | * |
| Load Capacitance, Unity Gain (Note 2) | 1000 pF | * |  |
| Short Circuit Current | 25 mA | * | * |
| Frequency Response |  |  |  |
| Unity Gain, Small Signai (Feedforward) | 1 MHz | * |  |
| Slew Rate, Unity Gain (Feedforward) | $50 \mathrm{~V} / \mu \mathrm{sec}$ | * | 20- * 1.5 mV |
| Input Offset Voltage (Note 3) | 50 mV max $/ 3.5 \mathrm{mV}$ max | 20 mV max $/ 1.5 \mathrm{mV}$ max | 20 mV max $/ 1.5 \mathrm{mV}$ max |
| vs Temperature, $\mathrm{T}_{\mathrm{A}}=\min$ to max | $75 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max | $25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max | $50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max |
| vs Supply, $\mathrm{T}_{\mathrm{A}}=\min$ to max | $300 \mu \mathrm{~V} / \mathrm{V}$ max | $200 \mu \mathrm{~V} / \mathrm{V}$ max | $200 \mu \mathrm{~V} / \mathrm{V}$ max |
| Input Bias Current |  |  |  |
| Either Input (Note 4) | 30 pA max | 20 pA max | 20pA max |
| Input Impedance |  |  |  |
| Differential | $10^{11} \Omega \\| 2 \mathrm{pF}$ | * | * |
| Common Mode | $10^{11} \Omega \\| 2 \mathrm{pF}$ | * | * |
| Input Noise |  |  |  |
| Voltage, 0.1 Hz to 10 Hz | $15 \mu \mathrm{~V}$ (p-p) | * | * |
| 5 Hz to 50 kHz | $5 \mu \mathrm{~V}$ (rms) | * | * |
| $\mathrm{f}=1 \mathrm{kHz}$ (spot noise) | $25 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ | * | * |
| Input Voltage Range |  |  |  |
| Differential | $\pm 2 \mathrm{~V}$ S | * |  |
| Common Mode, $\mathrm{T}_{\mathrm{A}}=\min$ to max | $\pm 10 \mathrm{~V}$ min | * | * |
| Common Mode Rejection, $\mathrm{V}_{\text {in }}= \pm 10 \mathrm{~V}$ | 70 dB min | * | * |
| Power Supply |  |  |  |
| Rated Performance | $\pm 15 \mathrm{~V}$ | * |  |
| Operating | $\pm(5$ to 18$) \mathrm{V}$ | * | * |
| Quiescent Current | 7 mA max | * | * |
| Temperature $\quad * \quad-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |  |  |  |
|  |  |  |  |
| Storage | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ | * |  |
| Price |  |  |  |
| (1-24) | \$16.45/\$19.45 | \$20.15/\$23.20 | \$31.40/\$39.70 |
| (25-99) | \$13.45/\$16.45 | \$16.10/\$19.20 | \$25.10/\$32.55 |
| (100-999) | \$11.20/\$14.20 | \$13.45/\$16.45 | \$20.95/\$26.35 |

## NOTES:

1. Open Loop Gain is specified with $\mathrm{V}_{\text {os }}$ both nulled and unnulled. *Specifications same as for AD513J.
2. A conservative design would not exceed 500 pF of load capacitance.
3. Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_{A}=+25^{\circ} \mathrm{C}$.
4. Bias Current specifications are guaranteed after 5 minutes of operation at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$. For higher temperatures, the current doubles every $+10^{\circ} \mathrm{C}$.

## HIGH SPEED, PRECISION, FET-INPUT OP AMP

## PIN CONFIGURATION

## PRODUCT DESCRIPTION

The AD5 14 is a low noise, high accuracy, FET-input amplifier which has been designed for applications where low bias currents, low noise, and accurately specified predictable operation are required, but low cost is essential. The device offers maximum bias currents as low as 10 pA , offset voltages below 20 mV , and a $5 \mu \mathrm{~V}(\mathrm{p}-\mathrm{p})$ max input noise voltage ( 0.1 to 10 Hz bandwidth).
All devices are free from latch-up and are short circuit protected. No external compensation is required as the internal 6 dB /octave roll-off provides stability in closed loop applications.

The AD5 14 is suggested for all low noise FET-input amplifier requirements where low cost is a prime consideration. The combination of low noise and low bias current make the AD514 ideal for EKG amplifiers, pH electrode amplifiers, and for long term integrators.

Top View


All versions of the AD514 are supplied in the hermeticallysealed, 8 -pin, TO-99 package. The AD514J, K and L are specified for 0 to $+70^{\circ} \mathrm{C}$ applications, while the AD514S is offered for operation over the full military temperature range of -55 to $+125^{\circ} \mathrm{C}$.

| SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{VDC}$ unless otherwise specified) |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| MODEL | AD5 14J | AD5 14K | AD5 14L | AD5 14S |
| OPEN LOOP GAIN (Note 1) |  |  |  |  |
| $\mathrm{V}_{\text {out }}= \pm 10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega$ | 20,000 min (50,000 typ) | 50,000 | ** | ** |
| $\mathrm{T}_{\mathrm{A}}=\min$ to max | 15,000 min | 40,000 | ** | 25,000 |
| OUTPUT CHARACTERISTICS |  |  |  |  |
| Voltage @ $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=\min$ to $\max$ | $\pm 10 \mathrm{~V}$ min $( \pm 13 \mathrm{~V}$ typ) | * | * | * |
| @ $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=\min$ to $\max$ | $\pm 12 \mathrm{~V}$ min ( $\pm 14 \mathrm{~V}$ typ) | * | * | * |
| Load Capacitance (Note 2) | 750 pF | * | * | * |
| Short Circuit Current | 25 mA | * | * | * ${ }^{\text {* }}$ |
| FREQUENCY RESPONSE |  |  |  |  |
| Unity Gain, Small Signal | 750 kHz | * | * | * |
| Full Power Response | 8 kHz | * | * | * |
| Slew Rate, Unity Gain | $0.5 \mathrm{~V} / \mu \mathrm{sec}$ | * | * | * |
| INPUT OFFSET VOLTAGE (Note 3) | 50 mV max ( 20 mV typ) |  |  | ** ${ }^{\text {* }}$ |
| vs. Temperature, $\mathrm{T}_{\mathrm{A}}=\min$ to max | $75 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max \left(30 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\right.$ typ $)$ | $25 \mu \mathrm{~V} /^{\circ} \mathrm{C} \max \left(15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \text { typ }\right)$ | ** | $50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max \left(15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\right.$ typ $)$ |
| vs. Supply, $\mathrm{T}_{\mathrm{A}}=\min$ to max | $400 \mu \mathrm{~V} / \mathrm{V} \max (200 \mu \mathrm{~V} / \mathrm{V}$ typ $)$ | $300 \mu \mathrm{~V} / \mathrm{V} \max (200 \mu \mathrm{~V} / \mathrm{V}$ typ) | ** | ** |
| INPUT BIAS CURRENT |  |  |  |  |
| Either Input (Note 4) | $50 \mathrm{pA} \max (5 \mathrm{pA}$ typ) | $20 \mathrm{pA} \max (5 \mathrm{pA}$ typ) | $10 \mathrm{pA} \max (5 \mathrm{pA}$ typ) | ** |
| INPUT IMPEDANCE |  |  |  |  |
| Differential | $10^{10} \Omega \\| 2 \mathrm{pF}$ | * | * | * |
| Common Mode | $10^{11} \Omega \\| 2 \mathrm{pF}$ | * | * | * |
| INPUT NOISE |  |  |  |  |
| Voltage, 0.1 to 10 Hz |  | $10 \mu \mathrm{~V}(\mathrm{p}-\mathrm{p}) \max (5 \mu \mathrm{~V}(\mathrm{p}-\mathrm{p})$ typ $)$ | $5 \mu \mathrm{~V}(\mathrm{p}-\mathrm{p}) \max (2 \mu \mathrm{~V}(\mathrm{p}-\mathrm{p})$ typ $)$ | ** |
| (a) 10 Hz | $130 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ |  | * | * |
| (a) 100 Hz | $70 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ |  | * | * |
| (a) 1000 Hz | $30 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ | * | * | * |
|  |  |  |  |  |
| Differential (Note 5) | $\pm 20 \mathrm{~V}$ | * | * | * |
| Common Mode, $\mathrm{T}_{\mathrm{A}}=\min$ to $\max$ | $\pm 10 \mathrm{~V} \min ( \pm 12 \mathrm{~V} \text { typ })$ | * | * | * |
| Common Mode Rejection, $\mathrm{V}_{\text {in }}= \pm 10 \mathrm{~V}$ | $70 \mathrm{~dB} \min (90 \mathrm{~dB}$ typ) | * | * | * |
| POWER SUPPLY |  |  |  |  |
| Rated Performance | $\pm 15 \mathrm{~V}$ | * | * | * |
| Operating | $\pm(5$ to 18$) \mathrm{V}$ | * | * | * |
| Quiescent Current | $7 \mathrm{~mA} \max$ ( 3 mA typ) | * | * | * |
| TEMPERATURE ${ }^{\text {a }}$ |  |  |  |  |
| Operating, Rated Performance | 0 to $+70^{\circ} \mathrm{C}$ | * | * | -55 to $+125^{\circ} \mathrm{C}$ |
| Storage | -65 to $+150^{\circ} \mathrm{C}$ | * | * | * |
| PRICE $\$ 8.85$ |  |  |  |  |
| (1-24) | $\$ 8.85$ |  |  |  |
| $(25-99)$ | $\$ 7.10$ | $\$ 9.50$ | $\$ 11.90$ | \$14.30 |
| $(100-999)$ | \$5.90 | \$7.90 | \$9.90 | \$11.90 |
| NOTES: $\quad$ * Specifications same as AD514] |  |  |  |  |
| 1. Open Loop Gain is specified with $\mathrm{V}_{\text {os }}$ both nulled and unnulled. <br> ** Specifications same as AD514J. |  |  |  |  |
| 3. Input off set voltage specifications are guaranteed after 5 minutes <br> of operation at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  |  |  |  |
| 4. Bias current specifications are guaranteed after 5 minutes of operation at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$. For higher temperatures, the current doubles every $10^{\circ} \mathrm{C}$. |  |  |  |  |
| 5. Defined as voltage between inputs such that neither exceeds $\pm 10 \mathrm{~V}$ from ground. |  |  |  |  |

AD540

## PRODUCT DESCRIPTION

The AD540 is the lowest cost, high accuracy FET-input op amp available which provides the user with low bias currents, high overall performance, and accurately specified predictable operation. The device offers maximum bias currents as low as 25 pA , offset voltages below 20 mV , maximum offset voltage drift below $25 \mu \mathrm{~V} /{ }^{8} \mathrm{C}$ and a minimum gain of 50,000 .
All devices are free from latchup and are short-circuit protected. No external compensation is required as the internal 6dB/octave roll-off provides stability in closed loop applications.
The AD540 is suggested for all FET-input amplifier requirements where low cost is of prime importance. Its performance is comparable to modular FET op amps, but its IC construction reduces the price significantly below that of modules.

## PIN CONFIGURATION

Top View


All versions of the AD540 are supplied in the hermeticallysealed, 8-pin, TO-99 package. The AD540J and AD540K are specified for 0 to $+70^{\circ} \mathrm{C}$ applications, while the AD540S is offered for operation over the full military temperature range of -55 to $+125^{\circ} \mathrm{C}$.

SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{S}}= \pm 15$ VDC unless otherwise specified)

| MODEL | AD540J | AD540K | AD540S |
| :---: | :---: | :---: | :---: |
| OPEN LOOP GAIN (Note 1) |  |  |  |
| $\mathrm{V}_{\text {out }}= \pm 10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega$ | 20,000 min | 50,000 min | ** |
| $\mathrm{T}_{\mathrm{A}}=\min$ to max | 15,000 min | 25,000 min | ** |
| OUTPUT CHARACTERISTICS |  |  |  |
| Voltage @ $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=\min$ to max | $\pm 10 \mathrm{~V}$ min $( \pm 13 \mathrm{~V}$ typ) | * | * |
| Voltage @ $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=\min$ to max | $\pm 12 \mathrm{~V}$ min ( $\pm 14 \mathrm{~V}$ typ) | * | * |
| Short Circuit Current | 25 mA | * | * |
| FREQUENCY RESPONSE |  |  |  |
| Unity Gain, Small Signal | 1.0 MHz |  |  |
| Full Power Response | 100 kHz | - | * |
| Slew Rate, Unity Gain | $6.0 \mathrm{~V} / \mu \mathrm{sec}$ | * | * |
| INPUT OFFSET VOLTAGE (Note 2) | 50 mV max |  |  |
| vs. Temperature | $75 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max | $25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max$ | $50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max |
| vs. Supply, $\mathrm{T}_{\mathrm{A}}=\min$ to $\max$ | $400 \mu \mathrm{~V} / \mathrm{V}$ max | $300 \mu \mathrm{~V} / \mathrm{V}$ max | ** |
| INPUT BIAS CURRENT <br> Either Input (Note 3) | 50pA max | 25 pA max | ** |
| INPUT IMPEDANCE |  |  |  |
| Differential | $10^{10} \Omega \\| 2 \mathrm{pF}$ | * | * |
| Common Mode | $10^{1:} \Omega \\| 2 \mathrm{pF}$ | * | * |
| INPUT VOLTAGE RANGE |  |  |  |
| Differential (Note 4) | $\pm 20 \mathrm{~V}$ | * | * |
| Common Mode | $\pm 10 \mathrm{~V}$ min ( $\pm 12 \mathrm{~V}$ typ) | * | * |
| Comımon Mode Rejection, $\mathrm{V}_{\text {in }}= \pm 10 \mathrm{~V}$ | 70 dB min | * | * |
| POWER SUPPLY |  |  |  |
| Rated Performance | $\pm 15 \mathrm{~V}$ | * | * |
| Operating | $\pm$ ( 5 to 18) V | * | * |
| Quiescent Current | $7 \mathrm{~mA} \max (3 \mathrm{~mA}$ typ) | * | * |
| TEMPERATURE RANGE |  |  |  |
| Operating, Rated Performance | 0 to $+70^{\circ} \mathrm{C}$ | * | -55 to $+125^{\circ} \mathrm{C}$ |
| Storage | -65 to $+150^{\circ} \mathrm{C}$ | * |  |
| PRICE |  |  |  |
| (1-24) | \$6.45 | \$8.95 | \$14.95 |
| (25-99) | \$5.70 | \$7.20 | \$11.95 |
| (100-999) | \$4.45 | \$5.95 | \$ 9.95 |

NOTE:

1. Open Loop Gain is specified with $\mathrm{V}_{\mathrm{os}}$ both nulled and unnulled.
. Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.
2. Bias Current specifications are guaranteed after 5 minutes of operation at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$. For higher temperatures, the current doubles every $10^{\circ} \mathrm{C}$.
. Demperatures, the current doubles eveltage between inputs, such that
Defined as voltage between inputs,
neither exceeds $\pm 10 \mathrm{~V}$ from ground.

## GENERAL DESCRIPTION

The AD503 IC FET-input op amp provides medium to high performance at low cost for all general purpose applications where the measurement of low-level currents, or small voltages from high impedance sources is a primary requirement. Despite low cost, this model offers such benefits as bias current (maximum for either input) and offset voltage specified under fully warmed-up conditions, minimum gain guaranteed with the offset voltage both nulled and unnulled, and minimal variation in offset voltage drift with nulling. The AD503 series provides higher accuracy with maximum bias currents below 10 pA , maximum offset voltage of less than 20 mV , maximum offset voltage drift below $25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ and minimum CMRR above 80 dB .

## PIN CONFIGURATION

Top View


This circuit has excellent dynamic performance, with a typical slew rate of $6 \mathrm{~V} / \mu \mathrm{sec}$, and is supplied in the TO-99 package for operation from 0 to $+70^{\circ} \mathrm{C}$ and $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$.

ELECTRICAL SPECIFICATIONS (Typical at $+25^{\circ} \mathrm{C}$ and $\pm 15 \mathrm{VDC}$, unless otherwise noted)

| PARAMETER | AD503J | AD503 K | AD503S |
| :---: | :---: | :---: | :---: |
| Open Loop Gain (Note 1) |  |  |  |
| $\mathrm{V}_{\text {OUT }}= \pm 10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega$ | 20,000 min | 50,000 min | 50,000 min |
| $\mathrm{T}_{\mathrm{A}}=\min$ to max | 15,000 min | 40,000 min | 25,000 min |
| Output Characteristics |  |  |  |
| Voltage @ $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=$ min to max | $\pm 10 \mathrm{~V}$ min | * | * |
| @ $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=\min$ to max | $\pm 12 \mathrm{~V}$ min | * | * |
| Load Capacitance | 750 pF | * | * |
| Short Circuit Current | 25 mA | * | * |
| Frequency Response |  |  |  |
| Unity Gain, Small Signal | 1.0 MHz | * | * |
| Full Power Response | 100 kHz | * | * |
| Slew Rate, Unity Gain | $3.0 \mathrm{~V} / \mu \mathrm{sec} \mathrm{min}$ | * | * |
| Settling Time, Unity Gain (to 0.1\%) | $10 \mu \mathrm{sec}$ | * | * |
| Input Offset Voltage (Note 2) | 50 mV max | 20 mV max | 20 mV max |
| vs Temperature, $\mathrm{T}_{\mathrm{A}}=\min$ to max | $75 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max | $25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max | $50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max |
| vs Supply, $\mathrm{T}_{\mathrm{A}}=\min$ to max | $400 \mu \mathrm{~V} / \mathrm{V}$ max | $200 \mu \mathrm{~V} / \mathrm{V}$ max | $200 \mu \mathrm{~V} / \mathrm{V}$ max |
| Input Bias Current |  |  |  |
| Either Input (Note 3) | 15 pA max | 10 pA max | 10 pA max |
| Input Impedance |  |  |  |
| Differential | $10^{11} \Omega \\| 2 \mathrm{pF}$ | * | * |
| Common Mode | $10^{12} \Omega \\| 2 \mathrm{pF}$ | * | * |
| Input Noise |  |  |  |
| Voltage, 0.1 Hz to 10 Hz | $15 \mu \mathrm{~V}$ (p-p) | * | * |
| 5 Hz to 50 kHz | $5.0 \mu \mathrm{~V}$ (rms) | * | * |
| $\mathrm{f}=1 \mathrm{kHz}$ (spot noise) | $30.0 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ | * | * |
| Input Voltage Range |  |  |  |
| Differential | $\pm 3.0 \mathrm{~V}$ | * | * |
| Common Mode, $\mathrm{T}_{\mathrm{A}}=\min$ to max | $\pm 10 \mathrm{~V}$ min | * | * |
| Common Mode Rejection, $\mathrm{V}_{\text {in }}= \pm 10 \mathrm{~V}$ | 70 dB min | 80 dB min | 80 dB min |
| Power Supply |  |  |  |
| Rated Performance | $\pm 15 \mathrm{~V}$ | * | * |
| Operating | $\pm$ (5 to 18)V | * | $\pm(5$ to 22$) \mathrm{V}$ |
| Quiescent Current | 7 mA max | * | * |
| Temperature ${ }^{\text {a }}$ |  |  |  |
| Operating, Rated Performance Storage | $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \\ -65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C} \end{gathered}$ | * | $-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C}$ |
| Price |  |  |  |
| (1-24) | \$16.80 | \$23.00 | \$29.00 |
| (25-99) | \$14.00 | \$18.80 | \$23.50 |
| (100-999) | \$11.40 | \$16.00 | \$20.00 |

## NOTES:

1. Open Loop gain is specified with $\mathrm{V}_{\text {OS }}$ both nulled and unnulled.
2. Input offset specs are guaranteed after 5 minutes of operation at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.
3. Bias current specs are guaranteed after 5 minutes of operation at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$. For higher temperatures, the current doubles every $+10^{\circ} \mathrm{C}$.

- Same as for AD503J.

MODEL AD0042C
The AD0042C is a low cost, high accuracy FET-input op amp which provides the user with low bias currents, high overall performance, and accurately specified predictable operation. The device offers maximum bias currents as low as 50 pA , offset voltages below 20 mV , maximum offset voltage drift below $25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ and a maximum gain of 25,000 .
The AD0042C is free from latchup and is short-circuit protected. No external compensation is required as the internal $6 \mathrm{~dB} /$ octave roll-off provides stability in closed loop applications.

The AD0042C is suggested for all FET-input amplifier requirements where low cost is of prime importance. Its performance is comparable to modular FET op amps, but its IC construction reduces the price significantly below that of modules.
The AD0042C is supplied in the hermetically-sealed, 8-pin, TO-99 package, and is specified for 0 to $+70^{\circ} \mathrm{C}$ applications.

## MODEL AD3542J

The AD3542J is the lowest cost, high accuracy FET-input op amp available which offers low bias currents, high overall performance, and accurately specified operation. The device features maximum bias currents as low as 25 pA , offset voltages below 20 mV , maximum offset voltage drift below $50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ and a minimum gain of 25,000 .
The AD3542J is free from latchup and is short-circuit protected. Internal compensation with a $6 \mathrm{~dB} /$ octave roll-off provides stability in closed loop applications. The AD3542J is recom-
mended for all FET-input amplifier requirements where low cost is of prime importance. Its performance is comparable to modular FET op amps, but its IC construction reduces the price significantly below that of modules.
The AD3542J is supplied in the hermetically-sealed, 8-pin, TO-99 package, and is specified for 0 to $+70^{\circ} \mathrm{C}$ applications.

## MODEL AD8007C

The AD8007C is a low cost, high accuracy FET-input op amp providing the user with low bias currents, ( 50 pA ) and accurately specified predictable operation. Offset voltage runs below 50 mV , with offset voltage drift below $75 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$. Gain is in excess of 20,000 .
The AD8007C is short-circuit protected and internally compensated with a $6 \mathrm{~dB} /$ octave roll-off for stability in closed loop applications. This device is also free from latchup.
The AD8007C is suggested for all FET-input amplifier requirements where low cost is of prime importance. Its performance is comparable to modular FET op amps, but its IC construction reduces the price significantly below that of modules.
The AD8007C is supplied in the hermetically-sealed, 8-pin, TO-99 package, and is specified for 0 to $+70^{\circ} \mathrm{C}$ applications.

SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{VDC}$ unless otherwise specified)

| Model | AD0042C | AD3 542J | AD8007C |
| :---: | :---: | :---: | :---: |
| OPEN LOOP GAIN (Note 1) |  |  |  |
| $\mathrm{V}_{\text {OUT }}= \pm 10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ | 25,000 min | 25,000 min | 20,000 min |
| $\mathrm{T}_{\mathrm{A}}=$ min to max | 15,000 min | 15,000 min | 15,000 min |
| OUTPUT CHARACTERISTICS |  |  |  |
| Voltage @ $\mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=\min$ to max | $\pm 10 \mathrm{~V}$ min | $\pm 10 \mathrm{~V}$ min | $\pm 10 \mathrm{~V}$ min |
| Voltage @ $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=$ min to max | $\pm 12 \mathrm{~V}$ | $\pm 12 \mathrm{~V}$ min | $\pm 12 \mathrm{~V}$ min |
| Short Circuit Current | 20 mA | 25 mA | 25 mA |
| FREQUENCY RESPONSE |  |  |  |
| Unity Gain, Small Signal | 1 MHz | 1.0 MHz | 1.0 MHz |
| Full Power Response | 100 kHz | 8.0 kHz | 100 kHz |
| Slew Rate, Unit Gain | $6.0 \mathrm{~V} / \mu \mathrm{sec}$ | $0.5 \mathrm{~V} / \mu \mathrm{sec}$ | $6.0 \mathrm{~V} / \mu \mathrm{sec}$ |
| INPUT OFFSET VOLTAGE (Note 2) | 20 mV max | 20 mV max | 50 mV max |
| vs. Temperature | $25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max | $50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max | $75 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max |
| vs. Supply, $\mathrm{T}_{\mathrm{A}}=\min$ to max | $400 \mu \mathrm{~V} / \mathrm{V}$ max | $400 \mu \mathrm{~V} / \mathrm{V}$ max | $600 \mu \mathrm{~V} / \mathrm{V}$ max |
| INPUT BIAS CURRENT |  |  |  |
| Either Input (Note 3) | 50 pA max | 25 pA max | 50pA max |
| INPUT IMPEDANCE |  |  |  |
| Differential | $10^{12} \Omega$ | $10^{11} \Omega$ | $10^{12} \Omega$ |
| Common Mode | $10^{12} \Omega$ | $10^{11} \Omega$ | $10^{11} \Omega$ |
| INPUT VOLTAGE RANGE |  |  |  |
| Differential (Note 4) | $\pm 20 \mathrm{~V}$ | $\pm 15 \mathrm{~V}$ (max safe input) | $\pm 20 \mathrm{~V}$ |
| Common Mode | $\pm 10 \mathrm{~V}$ min | $\pm 10 \mathrm{~V}$ | $\pm 10 \mathrm{~V}$ min |
| Common Mode Rejection, $\mathrm{V}_{\text {in }}= \pm 10 \mathrm{~V}$ | 70 dB min | 80 dB | 70 dB min |
| POWER SUPPLY |  |  |  |
| Rated Performance | $\pm 15 \mathrm{~V}$ | $\pm 15 \mathrm{~V}$ | $\pm 15 \mathrm{~V}$ |
| Operating | $\pm(5$ to 18$) \mathrm{V}$ | $\pm(5$ to 20)VDC | $\pm(5$ to 18$) \mathrm{V}$ |
| Quiescent Current | 4.0 mA max | $\pm 4 \mathrm{~mA}$ | 6.0 mA max |
| TEMPERATURE RANGE |  |  |  |
| Operating, Rated Performance | 0 to $+70^{\circ} \mathrm{C}$ | 0 to $+70^{\circ} \mathrm{C}$ | 0 to $+70^{\circ} \mathrm{C}$ |
| Storage | $-55^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| PRICES |  |  |  |
| 1-24 | \$5.80 | \$6.45 | \$7.50 |
| 25-99 | \$5.25 | \$5.50 | \$6.00 |
| 100-999 | \$4.45 | \$4.25 | \$5.00 |

## NOTES:

1. Open Loop Gain is specified with $V_{o s}$ both nulled and unnulled.
2. Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $+25^{\circ} \mathrm{C}$.
3. Bias Current specifications are guaranteed after 5 minutes of operation at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.

For higher temperatures, the current doubles every $+10^{\circ} \mathrm{C}$.
4. Defined as voltage between inputs, such that neither exceeds $\pm 10 \mathrm{~V}$ from ground.

## ELECTROMETER FET-INPUT OP AMP

AD523

## GENERAL DESCRIPTION

The AD5 23J, AD5 23 K , and 523 L are internally compensated FET input IC operational amplifiers that feature sub-picoamp bias current performance, low drift, high common mode rejection, and high gain. Maximum bias currents as low as 0.25 pA under warmed-up operating conditions are achieved by combining matched small geometry FET chips with a specially designed monolithic chip within a low leakage TO-99 package. The package is manufactured with high resistivity glass insulation and a guard pin connected to the can to minimize surface leakage currents, power supply induced input noise, and capacitive pickup. The AD523 is fully short circuit protected and offset voltage nullable, and offers maximum voltage drift of $30 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, minimum CMRR of 80 dB , and minimum gain of $40,000 \mathrm{~V} / \mathrm{V}$. The AD523J, K , and L

PIN CONFIGURATION
 are specified for operation over the $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$
temperature range.
ELECTRICAL CHARACTERISTICS (Typical @ $+25^{\circ} \mathrm{C}$ and $\pm 15 \mathrm{VDC}$, unless otherwise noted)

| Parameter | AD523J | AD523 K | AD523L |
| :---: | :---: | :---: | :---: |
| Open Loop Gain |  |  |  |
| $\mathrm{V}_{\text {OS }} \geqslant 0, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ | 20,000 min (50,000 typ) | 40,000 min ( 75,000 typ) | 40,000 min ( 75,000 typ) |
| (1) $\mathrm{T}_{\mathrm{A}}=0$ to $+70^{\circ} \mathrm{C}$ | 15,000 min | 25,000 min | 25,000 min |
| Output Characteristics |  |  |  |
| Voltage @ $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=0$ to $+70^{\circ} \mathrm{C}$ | $\pm 10 \mathrm{~V}$ min ( $\pm 12 \mathrm{~V}$ typ) | * | * |
| Current, $\mathrm{T}_{\mathrm{A}}=0$ to $+70^{\circ} \mathrm{C}$ | $\pm 5 \mathrm{~mA} \mathrm{~min}$ | * | * |
| Load Capacitance | 1000 pF | * | * |
| Short Circuit Current | 25 mA | * | * |
| Frequency Response |  |  |  |
| Unity Gain, Small Signal | 500 kHz | * | * |
| Full Power Response | 50 kHz | * | , |
| Slew Rate, Unity Gain | $3 \mathrm{~V} / \mu \mathrm{sec} \min (5 \mathrm{~V} / \mu \mathrm{sec} t y p)$ | * | - |
| Input Offset Voltage |  |  |  |
| Initial |  |  |  |
| vs. Temp $\mathrm{T}_{\mathrm{A}}=0$ to $+70^{\circ} \mathrm{C}$ | $90 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max \left(25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\right.$ typ $)$ | $30 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max \left(15 \mu \mathrm{~V} /^{\circ} \mathrm{C} \text { typ }\right)$ | $60 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max \left(25 \mu \mathrm{~V} /^{\circ} \mathrm{C} \text { typ }\right)$ |
| vs. Supply | $200 \mu \mathrm{~V} / \mathrm{V}$ max | $100 \mu \mathrm{~V} / \mathrm{V}$ max | $100 \mu \mathrm{~V} / \mathrm{V}$ max |
| Input Bias Current |  |  |  |
| Initial, each input, $\mathrm{V}_{\text {diff }} \leqslant 4 \mathrm{~V}$ ( Note 1) | $-1.0 \mathrm{pA} \max (-0.4 \mathrm{pA}$ typ) | -0.5pA max ( -0.2 pA typ) | $-0.25 \mathrm{pA} \max \left({ }^{( } 0.1 \mathrm{pA}\right.$ typ) |
| Input Impedance |  |  |  |
| Differential | $10^{12} \\| 3 \mathrm{pF}$ | * | * |
| Common Mode | $10^{13} \\| 3 \mathrm{pF}$ | * | * |
| Input Noise |  |  |  |
| Voltage, 0.01 to 1 Hz | $20 \mu \mathrm{~V}$ p-p | * | * |
| 5 Hz to 50 kHz | $15 \mu \mathrm{~V} \mathrm{rms}$ | * | * |
| Input Voltage Range |  |  |  |
| Differential, max safe | $\pm 10 \mathrm{~V}$ | * | * |
| Common Mode Rejection @ $\pm 8 \mathrm{~V}$ |  |  |  |
| $\mathrm{T}_{\mathrm{A}}=0 \text { to }+70^{\circ} \mathrm{C}$ | $70 \mathrm{~dB} \min (80 \mathrm{~dB}$ typ) | 80 dB min ( 90 dB typ) | 80 dB min ( 90 dB typ) |
| Power Supply |  |  |  |
| Rated Performance | $\pm 15 \mathrm{~V}$ | * | * |
| Operating | $\pm(5$ to 18$) \mathrm{V}$ | * | * |
| Current, quiescent | $\pm 7.0 \mathrm{~mA} \mathrm{max}( \pm 5.0 \mathrm{~mA} \mathrm{typ})$ | * | * |
| Temperature Range |  |  |  |
| Rated Performance |  | * | * |
| Operating | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | * | * |
| Storage | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ | * | * |
| Prices (1-24) | \$21.00 | \$25.00 | \$28.00 |
| (25-99) | 16.50 | 20.00 | 22.50 |
| (100-999) | 14.00 | 16.75 | 18.75 |

NOTE 1: Bias Current specification guaranteed after 5 minutes of operation at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$. (For higher ambient temperatures, the current doubles every $+10^{\circ} \mathrm{C}$.)
*Specifications same as AD523J.

## FET-INPUT GENERAL PURPOSE OP AMPS <br> PIN CONFIGURATIONS

Bottom View


ADM501


PIN 1: INVERTING INPUT
PIN 2: NON-INVERTING INPUT
PIN 3: + 15 VDC
PIN 4: -15 VDC
PIN 5: OUTPUT


AD501

## GENERAL DESCRIPTION

The Analog Devices Model AD501 is a microcircuit FET input operational amplifier that is supplied in the industrystandard axial-lead and plug-in molded packages, and in the hermetically sealed TO-8 type of package. The AD501 features offset voltages of less than 1 mV , offset voltage drifts below $25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ and bias currents of less than 5 pA . The circuits are manufactured with strictly controlled hybrid assembly techniques, which have proven their high reliability and fault-free performance through three years of system usage. The AD501 is supplied in the end-lead mini-package; the ADP501 in the bottom-lead mini-package; and the ADM501 in the TO-8-type package.

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{S}}= \pm \mathbf{1 5 V}, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, ${ }^{*}$ unless otherwise noted)

| Parameter | Conditions | 501A P501A M501A | $\begin{gathered} \text { 501B } \\ \text { P501B } \\ \text { M501B } \end{gathered}$ | 501C P501C M501C | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Initial Input Offset Voltage (max) | $\mathrm{R}_{\mathrm{S}} \leqslant 100 \mathrm{k} \Omega$ | 2.0 | 1.0 | 1.0 | mV |
| Average Temp Coef of Input Offset Voltage (max) | $\begin{aligned} \mathrm{T}_{\mathrm{A}}= & -25^{\circ} \mathrm{C} \text { to } \\ & +85^{\circ} \mathrm{C} \end{aligned}$ | 75 | 25 | 25 | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| Initial Input Bias Current (max)** |  | $\begin{gathered} 25 \\ \text { (10pA M501) } \end{gathered}$ | 10 | 5.0 | pA |
| Average Temp Coef of Input Bias Current (typ)** | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | $\begin{gathered} { }^{2.5} \\ \left(1 \mathrm{pA} /{ }^{\circ} \mathrm{C}\right. \text { M501) } \end{gathered}$ | 1.0 | 0.5 | $\mathrm{pA} /{ }^{\circ} \mathrm{C}$ |


| ALL DEVICES |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Parameter | Conditions | MIN | TYP | MAX | Units |
| Large Signal Voltage Gain | $\mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega$ | 25,000 | 100,000 |  | V/V |
|  | $\mathrm{V}_{\mathrm{O}}= \pm 10 \mathrm{~V}$ |  |  |  |  |
| Input Resistance | Differential |  | $10^{11}$ |  | $\Omega$ |
|  | Common Mode |  | $10^{11}$ |  | $\Omega$ |
| Input Capacitance |  |  | 4 |  | pF |
| Input Noise Voltage (rms) | 5 Hz to 50 kHz |  | 6 |  | $\mu \mathrm{V}$ |
| Input Voltage Range |  | $\pm 10$ | $\pm 12$ |  | V |
| Common Mode Rejection | $\mathrm{V}_{\text {IN }}= \pm 5 \mathrm{~V}$ |  | 80 |  | dB |
| Supply Voltage Rejection |  |  | 50 |  | $\mu \mathrm{V} / \%$ |
| Output Voltage Swing | $\mathrm{R}_{\mathrm{L}} \geqslant 10 \mathrm{k} \Omega$ | $\pm 12$ | $\pm 14$ |  | V |
|  | $\mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega$ | $\pm 10$ | $\pm 13$ |  | V |
| Output Short Circuit Current |  |  | 25 |  | mA |
| Supply Current |  |  |  | 9 | mA |
| Slew Rate |  | 3 | 5 |  | $\mathrm{V} / \mu \mathrm{s}$ |
| Unity Gain Bandwidth |  |  | 4 |  | MHz |
| Full Power Response | $\begin{aligned} & \mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega \\ & \mathrm{~V}_{\mathrm{O}} \geqslant 10 \mathrm{~V} \end{aligned}$ | 70 |  |  | kHz |
| Price (1-9) | 501 | 39.00 | 45.50 | 52.00 | \$ |
|  | P501 | 39.00 | 45.50 | 52.00 | \$ |
|  | M501 | 45.50 | 52.00 | 58.50 | \$ |

[^19]
# FET-INPUT GENERAL PURPOSE OP AMPS <br> AD5II, ADP5II 

PIN CONFIGURATIONS

## GENERAL DESCRIPTION

The Analog Devices AD511 and ADP511 series of FETinput operational amplifiers are low cost pin-for-pin replacements for the 501 and P501, 20-008 and 20-108, $\mathrm{C}-118$ and 140801 FET op amps. They feature offset voltages of less than 1 mV , offset voltage drifts below $25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, and bias currents of less than 5 pA . The AD511 and ADP5 11 series are manufactured by combining separate specially designed monolithic bipolar amplifier and FET chips on a laser-trimmed thick-film substrate. This technique provides extremely high performance and reliability at a significant reduction in assembly cost - making possible a low selling price. The circuits are available in A, B and C specification variations for

operation over the $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ temperature range. The AD511 is supplied in the end-lead mini-package; the ADP511 in the bottom-lead mini-package.

| ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted) |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Parameter | Conditions | $\begin{aligned} & \text { 511A } \\ & \text { P511A } \\ & \hline \end{aligned}$ | $\begin{aligned} & \text { 511B } \\ & \text { P511B } \\ & \hline \end{aligned}$ | $\begin{aligned} & \text { 511C } \\ & \text { P511C } \end{aligned}$ | Units |
| Initial Input Offset Voltage (max) | $\mathrm{R}_{\mathrm{S}} \leqslant 100 \mathrm{k} \Omega$ | 3.5 | 1.5 | 1.0 | mV |
| Average Temp Coef of Input Offset Voltage (max) | $\begin{aligned} \mathrm{T}_{\mathrm{A}}= & -25^{\circ} \mathrm{C} \text { to } \\ & +85^{\circ} \mathrm{C} \end{aligned}$ | 75 | 25 | 25 | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| Initial Input Bias Current (max) ${ }^{* *}$ |  | 25 | 10 | 5.0 | pA |
| Average Temp Coef of Input Bias Current (typ)** | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | 2.5 | 1.0 | 0.5 | $\mathrm{pA} /{ }^{\circ} \mathrm{C}$ |


| ALL DEVICES |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Parameter | Conditions | MIN | TYP | MAX | Units |
| Large Signal Voltage Gain | $\mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega$ | 25,000 | 100,000 |  | V/V |
|  | $\mathrm{V}_{\mathrm{O}}= \pm 10 \mathrm{~V}$ |  |  |  |  |
| Input Resistance | Differential |  | $10^{11}$ |  | $\Omega$ |
|  | Common Mode |  | $10^{12}$ |  | $\Omega$ |
| Input Capacitance |  |  | 2 |  | pF |
| Input Noise Voltage (rms) | 4 Hz to 10 kHz |  | 7 |  | $\mu \mathrm{V}$ |
| Input Voltage Range |  | $\pm 10$ | $\pm 12$ |  | V |
| Common Mode Rejection |  | 70 | 86 |  | dB |
| Ratio |  |  |  |  |  |
| Supply Voltage Rejection Ratio |  |  | 100 |  | $\mu \mathrm{V} / \mathrm{V}$ |
| Output Voltage Swing | $\mathrm{R}_{\mathrm{L}} \geqslant 10 \mathrm{k} \Omega$ | $\pm 12$ | $\pm 14$ |  | V |
|  | $\mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega$ | $\pm 10$ | $\pm 13$ |  | V |
| Output Resistance |  |  | 75 |  | $\Omega$ |
| Output Short Circuit Current |  |  | 25 |  | mA |
| Supply Current |  |  |  | 7 | mA |
| Slew Rate |  | 3 | 5 |  | $\mathrm{V} / \mu \mathrm{s}$ |
| Unity Gain Bandwidth |  |  | 1 |  | MHz |
| Full Power Response | $\begin{aligned} & \mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega \\ & \mathrm{~V}_{\mathrm{O}} \geqslant 10 \mathrm{~V} \end{aligned}$ |  | 70 |  | k Hz |
| Transient Response | $\mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega$, |  |  |  |  |
| Rise Time | $\mathrm{C}_{\mathrm{L}} \leqslant 100 \mathrm{pF}$ |  | 300 |  | ns |
| Overshoot |  |  | 5 |  | \% |
| Overload Recovery |  |  | 6 |  | $\mu \mathrm{s}$ |
| Price (1-9) |  | 20.00 | 24.00 | 29.00 | \$ |
| (10-24) |  | 18.00 | 21.00 | 26.00 | \$ |

*Typical Junction Temperature $\left(\mathrm{T}_{\mathrm{j}}\right)$ is $10^{\circ} \mathrm{C}$ above Ambient Temperature ( $\mathrm{T}_{\mathrm{A}}$ )
after 15 minutes warm-up at $\mathrm{V}_{\mathrm{S}}= \pm \mathbf{1 5 V}$
** Doubles every $10^{\circ} \mathrm{C}$

# LOW DRIFT, LOW NOISE OP AMP <br> PIN CONFIGURATION <br> Top View 

## GENERAL DESCRIPTION

The AD504J, AD504K, AD504L, AD504M and AD504S are moderately priced operational amplifiers which combine ultra-low drift and noise and extremely high gain with the frequency response and slew rate of general purpose I.C. op amps. A new double integrator circuit concept combined with a precise thermallybalanced layout achieves maximum nulled offset drift below $0.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, max input noise voltage of $0.6 \mu \mathrm{~V}(\mathrm{p}-\mathrm{p})$, and minimum gain of $10^{6}$. Unity gain small signal bandwidth is 300 kHz and the slew rate is $1.2 \mathrm{~V} / \mu \mathrm{sec}$ at a gain of 10 . The amplifier is externally compensated for unity gain with a single 390 pF capacitor; no compensation is required for gains above 500. The AD504 has fully protected inputs, which permit differential input voltages of up to $\pm \mathrm{V}_{\mathrm{S}}$ without voltage gain or bias current degradation due to reverse breakdown. The output is also pro-

tected from short circuits to ground and/or either supply voltage, and is capable of driving 1000 pF of load capacitance. The $\mathrm{J}, \mathrm{K}, \mathrm{L}$, and M models are specified for operation over the 0 to $+70^{\circ} \mathrm{C}$ temperature range, and are supplied in the TO-99 can package. The $S$ version, in the same package, is specified for $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ operation.

| ELECTRICAL SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ and $\pm 15 \mathrm{VDC}$, unless otherwise noted) |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| MODEL | AD504J | AD504K | AD504L | AD504M | AD504S |
| $\begin{aligned} & \text { OPEN LOOP CAIN } \\ & \mathrm{V}_{\mathrm{os}}= \pm 10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega \\ & {\text { (a) } \mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to }+70^{\circ} \mathrm{C}}^{\text {an }} \text {. } \end{aligned}$ | $\begin{aligned} & 250,000 \mathrm{~min} \\ & 125,000 \mathrm{~min} \end{aligned}$ | $\begin{aligned} & 500,000 \mathrm{~min} \\ & 250,000 \mathrm{~min} \end{aligned}$ | $\begin{gathered} 10^{6} \mathrm{~min} \\ 500,000 \mathrm{~min} \end{gathered}$ | $\begin{gathered} 10^{6} \mathrm{~min} \\ 500,000 \mathrm{~min} \end{gathered}$ | $\begin{aligned} & 10^{6} \mathrm{~min} \\ & 250,000 \end{aligned}$ |
| OUTPUT CHARACTERISTICS <br> Voltage (a) $\mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ <br> Load Capacitance <br> Output Current <br> Short Circuit Current | $\begin{gathered} \pm 10 \mathrm{~V} \min ( \pm 13 \mathrm{~V} \text { typ }) \\ 1000 \mathrm{pF} \\ 10 \mathrm{~mA} \min \\ 25 \mathrm{~mA} \end{gathered}$ |  |  | * | * ${ }_{*}^{*}$ |
| FREQUENCY RESPONSE <br> Unity Gain, Small Signal, $\mathrm{C}_{\mathrm{c}}=390 \mathrm{pF}$ <br> Full Power Response, $\mathrm{C}_{\mathrm{C}}=390 \mathrm{pF}$ <br> Slew Rate, Unity Gain, $\mathrm{C}_{\mathrm{C}}=390 \mathrm{pF}$ | $\begin{gathered} 300 \mathrm{kHz} \\ 1.5 \mathrm{kHz} \\ 0.12 \mathrm{~V} / \mu \mathrm{sec} \end{gathered}$ |  | * $*$ $*$ |  |  |
| ```INPUT OFFSET VOLTAGE Initial Offset, \(\mathrm{R}_{\mathrm{S}} \leqslant 10 \mathrm{k} \Omega\) vs. Temp., \(\mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}, \mathrm{V}_{\text {os }}\) nulled \(\mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\), \(\mathrm{V}_{\text {os }}\) unnulled (Note 1) vs. Supply (a) \(\mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) vs. Time``` | 2.5 mV max <br> $5.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max$ <br> $10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max <br> $25 \mu \mathrm{~V} / \mathrm{V} \max$ <br> $40 \mu \mathrm{~V} / \mathrm{V}$ <br> $20 \mu \mathrm{~V} / \mathrm{mo}$ | $\begin{gathered} 1.5 \mathrm{mV} \max \\ 3.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max \\ 5.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max \\ 15 \mu \mathrm{~V} / \mathrm{V} \max \\ 25 \mu \mathrm{~V} / \mathrm{V} \max \\ 15 \mu \mathrm{~V} / \mathrm{mo} \end{gathered}$ | $\begin{gathered} 0.5 \mathrm{mV} \max \\ 1.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max \\ 2.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max \\ 10 \mu \mathrm{~V} / \mathrm{V} \max \\ 15 \mu \mathrm{~V} / \mathrm{V} \max \\ 10 \mu \mathrm{~V} / \mathrm{mo} \end{gathered}$ | $\begin{gathered} 0.5 \mathrm{mV} \max \\ 0.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max \\ 1.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max \\ 10 \mu \mathrm{~V} / \mathrm{V} \max \\ 15 \mu \mathrm{~V} / \mathrm{V} \max \\ 10 \mu \mathrm{~V} / \operatorname{mo} \end{gathered}$ | $0.5 \mathrm{mV} \max$ $1.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max <br> $2.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max $10 \mu \mathrm{~V} / \mathrm{V} \max$ $20 \mu \mathrm{~V} / \mathrm{V}$ max $10 \mu \mathrm{~V} / \mathrm{mo}$ |
| INPUT OFFSET CURRENT <br> (a) $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | $40 \mathrm{nA} \max$ | 15 nA max | 10 nA max | $10 \mathrm{nA} \max$ | 10 nA max |
| INPUT BIAS CURRENT Initial <br> (a) $\mathrm{T}=0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ <br> vs. Temp., $\mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 200nA max $300 n \mathrm{~A}$ max $300 \mathrm{pA} /{ }^{\circ} \mathrm{C}$ | $100 n A \max$ $150 n A \max$ $250 \mathrm{pA} /{ }^{\circ} \mathrm{C}$ | $80 n A \max$ <br> $100 \mathrm{nA} \max$ <br> $200 \mathrm{pA} /{ }^{\circ} \mathrm{C}$ | $80 n A \max$ $100 n \mathrm{~A}$ max $200 \mathrm{pA} /{ }^{\circ} \mathrm{C}$ | $80 n A \max$ 200nA max $200 \mathrm{pA} /{ }^{\circ} \mathrm{C}$ |
| INPUT IMPEDANCE <br> Differential Common Mode | $\begin{gathered} 0.5 \mathrm{M} \Omega \\ 100 \mathrm{M} \Omega \\| 4 \mathrm{pF} \end{gathered}$ | $1.0 \mathrm{M} \Omega$ | $\begin{gathered} 1.3 \mathrm{M} \Omega \\ * \\ \hline \end{gathered}$ | $\underset{*}{1.3 \mathrm{M} \Omega}$ | $1.3 \mathrm{M} \Omega$ |
| $\begin{aligned} & \text { INPUT NOISE } \\ & \text { Voltage, } 0.11 \mathrm{~Hz} \text { to } 10 \mathrm{~Hz} \\ & \mathrm{f}=100 \mathrm{~Hz} \\ & \mathrm{f}=1 \mathrm{kHz} \\ & \text { Current, } \mathrm{f}=10 \mathrm{~Hz} \\ & \mathrm{f}=100 \mathrm{~Hz} \\ & \mathrm{f}=1 \mathrm{kHz} \end{aligned}$ | $\begin{gathered} 1.0 \mu \mathrm{~V}(\mathrm{p}-\mathrm{p}) \\ 10 \mathrm{nV} / \sqrt{\mathrm{Hz}}(\mathrm{rms}) \\ 8 \mathrm{nV} / \sqrt{\mathrm{Hz}}(\mathrm{rms}) \\ 1.0 \mathrm{pA} / \sqrt{\mathrm{Hz}}(\mathrm{rms}) \\ 0.6 \mathrm{pA} / \sqrt{\mathrm{Hz}}(\mathrm{rms}) \\ 0.5 \mathrm{pA} / \sqrt{\mathrm{Hz}}(\mathrm{rms}) \end{gathered}$ |  |  | $0.6 \mu \mathrm{~V}(\mathrm{p}-\mathrm{p})$ max $10 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ (rms) max $9 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ (rms) max $1.3 \mathrm{pA} / \sqrt{\mathrm{Hz}}$ (rms) max $0.6 \mathrm{pA} / \sqrt{\mathrm{Hz}}$ (rms) max $0.3 \mathrm{pA} / \sqrt{\mathrm{Hz}}(\mathrm{rms}) \max$ |  |
| INPUT VOLTAGE RANGE <br> Differential or Common Mode, max safe Common Mode Rejection, $\mathrm{V}_{\text {in }}= \pm 10 \mathrm{~V}$ | $\begin{gathered} \pm \mathrm{V}_{\mathrm{S}} \\ 94 \mathrm{~dB} \text { min } \end{gathered}$ | 100 dB min | 110 dB min | 110 dB min | 110 dB min |
| POWER SUPPLY <br> Rated Performance Operating Current, Quiescent | $\begin{gathered} \pm 15 \mathrm{~V} \\ \pm(5 \text { to } 18) \mathrm{V} \\ \pm 4.0 \mathrm{~mA} \mathrm{max} \\ \hline \end{gathered}$ | $\pm 3.0 \mathrm{~mA} \max$ | $\pm 3.0 \mathrm{~mA} \max$ | $\pm 3.0 \mathrm{~mA} \max$ | $\pm 3.0 \mathrm{~mA} \max$ |
| TEMPERATURE RANGE Operating, Rated Performance Storage | $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \\ -65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C} \end{gathered}$ | * | * | * | $-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C}$ |
| $\begin{aligned} & \text { PRICE } \\ & \quad(1-24) \\ & \quad(25-99) \\ & \quad(100-999) \end{aligned}$ | $\begin{array}{r} \$ 11.20 \\ 9.55 \\ 8.40 \end{array}$ | $\begin{array}{r} \$ 19.80 \\ 16.80 \\ 15.30 \end{array}$ | $\begin{array}{r} \$ 28.00 \\ 21.80 \\ 20.40 \end{array}$ | $\begin{array}{r} \$ 30.00 \\ 23.80 \\ 22.00 \end{array}$ | $\begin{array}{r} \$ 32.00 \\ 25.80 \\ 24.00 \end{array}$ |

[^20]
# LOWEST COST HIGH ACCURACY OP AMPS AD30IAL, AD74IJ/K/L/S 

## GENERAL DESCRIPTION

The AD301AL and AD741J/K/L/S op amps provide the user with the highest possible performance achieved by the two most popular IC op amp series, combined with the lowest possible cost. Their performance approaches that of precision amplifiers, and offers the user the additional advantage of using op amps with which he is already familiar.
The AD301AL offers a $30 \%$ improvement in accuracy over the AD201A by reducing errors due to offset voltage $(0.5 \mathrm{mV}$ $\max$ ), offset voltage drift ( $5.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max$ ), bias current ( 30 nA $\max$ ), offset current ( $5 \mathrm{nA} \max$ ), voltage gain ( $80,000 \mathrm{~min}$ ), PSRR ( $90 \mathrm{~dB} \min$ ), and CMRR ( $90 \mathrm{~dB} \min$ ).

The AD741J, AD741K, and AD741L substantially increase overall accuracy over the standard AD741C by providing maximum limits on voltage drift, and significantly reducing errors due to offset voltage, bias and offset currents, gain, PSRR and

CMRR. Similarly, the AD741S provides considerably improved performance over the AD741 for wide temperature range applications. Results of a typical error analysis indicate a factor of 8 improvement in accuracy of the AD741L, a factor of 5 using the AD741K, and a factor of 2.5 using the AD741J. The AD741S achieves a 3.5 times improvement over the AD741.
All models are supplied in both the TO-99 metal can and molded minidip DIL packages.

AD301AL pin configurations same as standard AD101A series. (See page 207.) AD741 J/K/L/S pin configurations same as standard AD741. (See page 207.)

SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ and $\pm 15$ VDC, unless otherwise specified)

| Model | AD301AL | Model | AD741J | AD741 K | AD741 L | AD741S |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Open Loop Gain |  | Open Loop Gain |  |  |  |  |
| $\mathrm{V}_{\mathrm{O}}= \pm 10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega$ | $80,000 \mathrm{~min}$ | $\mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{O}}= \pm 10 \mathrm{~V}$ | $50,000 \mathrm{~min}$ |  |  | * |
| $\mathrm{T}_{\text {min } / \text { max }}$ | $40,000 \mathrm{~min}$ | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{O}}= \pm 10 \mathrm{~V}$ |  | 50,000 min | $50,000 \mathrm{~min}$ |  |
| Output Characteristics |  | Over Temp Range, $\mathrm{T}_{\min / \text { max }}$, |  |  |  |  |
| Voltage, $\mathrm{R}_{\mathrm{L}} \geqslant 10 \mathrm{k} \Omega, \mathrm{T}_{\text {min/max }}$ | $\pm 12 \mathrm{~V}$ min | same loads as above | 25,000 min | * | * | * |
| $\mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega, \mathrm{~T}_{\min / \max }$ <br> Short Circuit Current | $\pm 10 \mathrm{~V}$ min 25 mA | Output Characteristics <br> Voltage @ $\mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega, \mathrm{T}_{\min } / \max$ | $\pm 10 \mathrm{~V} \text { min }$ |  |  | * |
| Frequency Response |  | Voltage @ $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\min / \text { max }}$ |  | $\pm 10 \mathrm{~V}$ min | $\pm 10 \mathrm{~V}$ min |  |
| Small Sig., $\mathrm{A}=1, \mathrm{C}_{\mathrm{C}}=30 \mathrm{pF}$ | 1 MHz | Short Circuit Current | 25 mA | * | * | * |
| Feedforward | 10 MHz | Frequency Response |  |  |  |  |
| $\mathrm{F}_{\mathrm{P}}, \mathrm{C}_{\mathrm{C}}=30 \mathrm{pF}$ | 6 kHz | Unity Gain, Small Signal | 1 MHz | * | * | * |
| Feedforward | 150 kHz | Full Power Response | 10 kHz | * | * | * |
| Slew Rate $\mathrm{A}=1, \mathrm{C}_{\mathrm{C}}=30 \mathrm{pF}$ Feedforward | $0.25 \mathrm{~V} / \mu \mathrm{sec}$ $9 \mathrm{~V} / \mu \mathrm{sec}$ | Slew Rate, Unity Gain | $0.5 \mathrm{~V} / \mu \mathrm{sec}$ | * | * | * |
| Input Offset Voltage |  | Input Offset Voltage |  |  |  |  |
| Initial, $\mathrm{R}_{\mathrm{S}}<50 \mathrm{k} \Omega$ | $0.5 \mathrm{mV} \max$ | Initial, $\mathrm{R}_{\mathrm{S}} \leqslant 10 \mathrm{k} \Omega$ | 3 mV max | 2 mV max | $0.5 \mathrm{mV} \max$ | 2 mV max |
| vs. Temperature, $\mathrm{T}_{\min / \mathrm{max}}$ | $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max |  | 4 mV max | 3 mV max | 1 mV max | * |
| vs. Supply | 90 dB min | $T_{\text {min }} /$ max <br> Avg vs Temperature (untrim.) | $20 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max$ |  | $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max$ | $15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max$ |
| (a) $\mathrm{T}_{\mathrm{A}}=0$ to $+70^{\circ} \mathrm{C}$ | 80 dB min | vs Supply, $\mathrm{T}_{\min } / \max$ | $100 \mu \mathrm{~V} / \mathrm{V} \max$ | $15 \mu \mathrm{~V} / \mathrm{V} \max$ | $15 \mu \mathrm{~V} / \mathrm{V} \max$ |  |
| Input Offset Current |  | Input Offset Current |  |  |  |  |
| Initial <br> (a) $\mathrm{T}_{\min / \max }$ | 5nA max <br> 10nA max | Initial | $50 n A \max$ | 10 nA max | 5 nA max | 10 nA max |
| vs. Temperature, $\mathrm{T}_{\min / \mathrm{max}}$ | $0.1 \mathrm{nA} /{ }^{\circ} \mathrm{C}$ max | $\mathrm{T}_{\text {min } / \text { max }}$ | $100 n A$ max | 15 nA max | 10nA max | 25 nA max |
|  |  | Avg vs Temperature | $0.1 \mathrm{nA} /{ }^{\circ} \mathrm{C}$ | $0.2 \mathrm{nA} /{ }^{\circ} \mathrm{C}$ max | $0.1 \mathrm{nA} /{ }^{\circ} \mathrm{C}$ max | $0.25 \mathrm{nA} /{ }^{\circ} \mathrm{C} \max$ |
| Input Bias Current |  | Input Bias Current |  |  |  |  |
| Initial | 30nA max | Initial |  |  |  |  |
| ( $\mathrm{T}_{\min / \mathrm{max}}$ | 45 nA max |  | 200nA max | $75 n A \max$ | 50 nA max | $75 n A \max$ |
| $\begin{aligned} & \text { Input Voltage Noise } \\ & \qquad \mathrm{f}=10 \mathrm{~Hz} \end{aligned}$ | $35 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ | Avg vs Temperature | $0.6 \mathrm{nA} /{ }^{\circ} \mathrm{C}$ | $\begin{aligned} & 120 \mathrm{nA} \max \\ & 1.5 \mathrm{nA} /{ }^{\circ} \mathrm{C} \max \end{aligned}$ | $\begin{aligned} & 100 \mathrm{nA} \max \\ & 1 \mathrm{nA} /^{\circ} \mathrm{C} \max \end{aligned}$ | $\begin{aligned} & 250 n A \max \\ & 2 \mathrm{nA} /^{\circ} \mathrm{C} \max \end{aligned}$ |
| $\mathrm{f}=100 \mathrm{~Hz}$ | $28 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ | Input Impedance |  |  |  |  |
| $\mathrm{f}=1 \mathrm{kHz}$ | $22 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ | Differential | $1 \mathrm{M} \Omega$ | $2 \mathrm{M} \Omega$ | $2 \mathrm{M} \Omega$ | $2 \mathrm{M} \Omega$ |
| Input Impedance | $1.5 \mathrm{M} \Omega \mathrm{min}$ | Input Voltage Range (Note 1) |  |  |  |  |
| Input Voltage Range |  | Differential, max safe | $\pm 30 \mathrm{~V}$ | * | * | * |
| Diff. or CM, max safe | $\pm \mathrm{V}_{\mathrm{S}}, \mathrm{V}_{\mathrm{S}} \leqslant 15 \mathrm{~V}$ | Common Mode Rejection | $\pm 15 \mathrm{~V}$ |  |  |  |
| Common Mode Rejection Ratio | 90 dB min | $\mathrm{T}_{\min / \max }$ | 80 dB min | 90 dB min | 90 dB min | * |
| @ $\mathrm{T}_{\min / \mathrm{max}}$ | 80 dB min |  |  |  |  |  |
| Power Supply |  | Power Supply |  |  |  |  |
| Rated Performance | $\pm 15 \mathrm{~V}$ | Rated Performance | $\pm 15 \mathrm{~V}$ | * ${ }^{*}$ | * | ${ }^{*}$ |
| Operating | $\pm 18 \mathrm{~V}$ | Operating | $\pm(5$ to 18$) \mathrm{V}$ | $\pm(5$ to 22$) \mathrm{V}$ | $\pm(5$ to 22$) \mathrm{V}$ | $\pm(5$ to 22$) \mathrm{V}$ |
| Quiescent Current | 3 mA max | Current, Quiescent | 3.3 mA max | 2.8 mA max | 2.8 mA max | 2.8 mA max |
|  |  |  |  |  |  |  |
| Operating, Rated Performance Storage | $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \\ -65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C} \end{gathered}$ | Operating, Rated Performance Storage | $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \\ -65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C} \end{gathered}$ | * | * | $-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C}$ |
| Price |  |  |  |  |  |  |
| (1-24) | \$6.00 |  | \$1.85 | \$3.40 | \$9.00 | \$4.95 |
| (25-99) | \$4.80 |  | \$1.50 | \$2.70 | \$7.20 | \$4.00 |
| (100-999) | \$4.00 |  | \$1.25 | \$2.25 | \$6.00 | \$3.30 |

[^21]*Specifications same as AD741J.

## CHOPPERLESS LOW DRIFT OPERATIONAL AMPLIFIER

## GENERAL DESCRIPTION

The Analog Devices AD508 is the highest accuracy IC operational amplifier presently available. Its combination of low drift ( $3.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max), low offset current ( 5.0 nA max), and long term stability ( $10 \mu \mathrm{~V} /$ month $\max$ ) make it the choice for all applications requiring the utmost in precise performance from an IC op amp. Guaranteed parameters also include gain greater than 250,000 , PSRR less than $25 \mu \mathrm{~V} / \mathrm{V}$, CMRR above 94 dB , and offset voltage below 2.5 mV - nullable to zero. In addition, the AD508's superbeta input transistor quad results in maximum offset and bias currents of 5 nA and 25 nA , while permitting the input stage to operate at sufficiently high current levels to provide a unity gain slew rate of $0.12 \mathrm{~V} / \mu \mathrm{sec}$ and small signal bandwidth of 300 kHz .
The outstanding long term stability of the AD508 is attained by subjecting $100 \%$ of the devices to a 100 hour stabilization burn-in. The AD508J is supplied in the TO-99 package for operation over the 0 to $+70^{\circ} \mathrm{C}$ temperature range.
ELECTRICAL SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ and $\pm 15$ VDC, unless otherwise specified)

| Parameter | AD508J |  |
| :---: | :---: | :---: |
| $\begin{aligned} & \text { Open Loop Gain } \\ & \mathrm{V}_{\mathrm{O}}= \pm 10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega \\ & \text { @ } \mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to }+70^{\circ} \mathrm{C} \end{aligned}$ | $\begin{gathered} 250,000 \min \left(4 \times 10^{6} \text { typ }\right) \\ 125,000 \min \left(10^{6} \text { typ }\right) \end{gathered}$ |  |
| Output Characteristics Voltage, $\mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ Output Current | $\begin{gathered} \pm 10 \mathrm{~V} \min ( \pm 13 \mathrm{~V} \text { typ }) \\ 10 \mathrm{~mA} \min \end{gathered}$ |  |
| Frequency Response <br> Unity Gain, Small Signal, $\mathrm{C}_{\mathrm{C}}=390 \mathrm{pF}$ <br> Full Power Response, $\mathrm{C}_{\mathrm{C}}=390 \mathrm{pF}$ <br> Slew Rate, Unity Gain, $\mathrm{C}_{\mathrm{C}}=390 \mathrm{pF}$ | $\begin{gathered} 300 \mathrm{kHz} \\ 1.5 \mathrm{kHz} \\ 0.12 \mathrm{~V} / \mu \mathrm{sec} \end{gathered}$ |  |
| Input Offset Voltage <br> Initial Offset, $\mathrm{R}_{\mathrm{S}} \leqslant 100 \Omega$ <br> vs. Temperature, <br> $\mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{OS}}$ nulled <br> $\mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{OS}}$ unnulled $\dagger$ <br> vs. Supply <br> (a) $\mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ <br> vs. Time | $\begin{gathered} \pm 2.5 \mathrm{mV} \max ( \pm 1.0 \mathrm{mV} \text { typ }) \\ \pm 3.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max \left( \pm 0.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \text { typ }\right) \\ \pm 10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max \left( \pm 1.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \text { typ }\right) \\ \pm 25 \mu \mathrm{~V} / \mathrm{V} \max \\ \pm 40 \mu \mathrm{~V} / \mathrm{V} \\ \pm 15 \mu \mathrm{~V} / \mathrm{mo} \end{gathered}$ |  |
| ```Input Offset Current Initial vs. Temp, \(\mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) Input Bias Current Initial vs. Temp, \(\mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)``` | $\begin{gathered} \pm 5.0 \mathrm{nA} \max ( \pm 2.5 \mathrm{nA} \text { typ }) \\ \pm 14 \mathrm{pA} \cdot{ }^{\circ} \mathrm{C} \\ 25 \mathrm{nA} \max (10 \mathrm{nA} \text { typ }) \\ \pm 100 \mathrm{pA} /^{\circ} \mathrm{C} \end{gathered}$ |  |
| Input Noise Voltage, 0.01 to 10 Hz 100 Hz 1 kHz Current, 100 Hz 1 kHz | $\begin{gathered} 1.0 \mu \mathrm{~V}(\mathrm{p}-\mathrm{p}) \\ 12 \mathrm{nV} / \sqrt{\mathrm{Hz}}(\mathrm{rms}) \\ 10 \mathrm{nV} / \sqrt{\mathrm{Hz}}(\mathrm{rms}) \\ 0.3 \mathrm{pA} / \sqrt{\mathrm{Hz}}(\mathrm{rms}) \\ 0.2 \mathrm{pA} / \sqrt{\mathrm{Hz}}(\mathrm{rms}) \end{gathered}$ |  |
| Input Voltage Range <br> Differential or Common Mode, Max Safe <br> Common Mode Rejection, $V_{\text {in }}= \pm 10 \mathrm{~V}$ <br> Power Supply <br> Current, Quiescent <br> Temperature Range <br> Operating, Rated Performance <br> Storage | $\begin{gathered} \pm \mathrm{V}_{\mathrm{S}} \\ 94 \mathrm{~dB} \min (120 \mathrm{~dB} \text { typ }) \\ \pm 4.0 \mathrm{~mA} \max ( \pm 1.5 \mathrm{~mA} \text { typ }) \\ 0^{\circ} \mathrm{C} \text { to }+70^{\circ} \mathrm{C} \\ -65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C} \end{gathered}$ |  |
| $\begin{aligned} \hline \text { Price } & (1-24) \\ & (25-99) \\ & (100-999) \end{aligned}$ | $\begin{aligned} & \hline \$ 21.00 \\ & \$ 16.80 \\ & \$ 14.00 \end{aligned}$ |  |

[^22]$\dagger$ This parameter is not $100 \%$ tested; typically, $90 \%$ of the units meet this limit.

# INSTRUMENTATION AMPLIFIERS <br> AD520, AD52 

## GENERAL DESCRIPTION

The AD520 and AD521 are complete instrumentation amplifiers in integrated circuit form with differential inputs and an accurately programmable gain relationship.

The AD520 and AD521 should not be confused with an operational amplifier, even though op amps can be used as building blocks in variable gain instrumentation amplifier circuits. An op amp is merely a high gain component requiring the addition of external feedback to complete the amplification function. Because of the limitations of resistor matching in the external feedback circuit and the relatively low input impedance resulting from the input resistors, an instrumentation amplifier circuit designed around op amps frequently provides less than satisfactory performance. Since the AD520 and AD521 are complete amplification circuits which do not depend upon external resistor matching for input-output isolation, they maintain their high CMRR in any application.

The AD520 and AD521 are ideally suited for all general purpose, high accuracy amplifier requirements. Their small size, low cost and complete on-a-chip ease of application offer the circuit designer an attractive alternate to both modular instrumentation amplifier packages and user-wired collections of IC op amps and precision external components. For increased versatility, the amplifiers have a remote sense terminal for current-controlled load applications. A separate output reference terminal is also provided so that the output can be biased independently of the gain setting.
' $J$ ' and ' $K$ ' versions are specified over the temperature range 0 to $+70^{\circ} \mathrm{C}$, while the ' S ' version is available for operation over the full military temperature range, -55 to $+125^{\circ} \mathrm{C}$. All versions come in the 14-pin DIP.

SPECIFICATIONS (Typical at $\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ unless otherwise noted)

| Parameter | AD520J | AD520K | AD520S |
| :---: | :---: | :---: | :---: |
| Gain Equation | $\mathrm{G}=\left(10^{5} / \mathrm{R}_{\text {gain }}\right) \mathrm{V} / \mathrm{V}$ | * | * |
| Range | 1 to 1000 | * | * |
| Error from Equation | adjustable to zero | * | * |
| Nonlinearity | $\pm 0.05 \%$ | * | * |
| Output Rating (min) | $\pm 10 \mathrm{~V}$ @ $\pm 5 \mathrm{~mA}$ | * | * |
| Small Signal Bandwidth, G $=1$ | 200 kHz | * | * |
| $G=1000$ | 25 kHz | * | * |
| Full Power Response | 50 kHz | * | * |
| Slew Rate | $4 \mathrm{~V} / \mu \mathrm{sec}$ | * | * |
| Input Offset Voltage (max) | must be nulled | * | * |
| vs. Temperature (max) | $10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}(\mathrm{G}=1000)$ | ** |
| vs. Supply | $\pm 50 \mu \mathrm{~V} / \mathrm{V}$ | * | * |
| Output Offset Voltage (max) | - | - | - |
| vs. Temperature (max) | - | - | - |
| vs. Supply | - | - | - |
| Bias Current (max) | 80 nA | 40nA | ** |
| Offset Current (max) | 40 nA | 20nA | ** |
| Input Impedance, Differential | $2 \times 10^{9} \Omega$ | * | * |
| Common Mode | $2 \times 10^{9} \Omega$ | * | * |
| Noise, 0.1 to 10 Hz (p-p) | $5 \mu \mathrm{~V}$ RTI ( $\mathrm{G}=1000$ ) | * | * |
| Differential Input Voltage | $\pm \mathrm{V}_{\text {S }}$ (safe) | * | * |
| Common Mode | $\pm 10 \mathrm{~V}$ (safe) | * | * |
| CMRR, dc to 60 Hz (min), $1 \mathrm{k} \Omega$ imbalance |  |  |  |
| $\mathrm{G}=1$ | 65 dB | 70 dB | ** |
| $\mathrm{G}=1000$ | 95 dB | 106dB | ** |
| Supply Voltage Range | $\pm 5 \mathrm{~V}$ to $\pm 18 \mathrm{~V}$ | * | * |
| Quiescent Current (max) | $\pm 6 \mathrm{~mA}$ | * | * |
| Temperature Range | 0 to $+70^{\circ} \mathrm{C}$ | * | -55 to $+125^{\circ} \mathrm{C}$ |
| Price |  |  | ' |
| 1-24 | \$18.00 | \$24.00 | \$33.00 |
| 25-99 | \$14.40 | \$19.20 | \$26.50 |
| 100-999 | \$12.00 | \$16.00 | \$22.00 |

*Specifications same as 'J' version.
${ }^{* *}$ Specifications same as ' $K$ ' version.

PIN CONFIGURATION


PIN CONFIGURATION


| AD521J | AD521K | AD521S |
| :---: | :---: | :---: |
| $\mathrm{G}=\mathrm{R}_{\mathrm{S}} / \mathrm{R}_{\mathrm{G}} \mathrm{V} / \mathrm{V}$ | * | * |
| 0.1 to $>1000$ | * | * |
| $( \pm 0.25-0.004 \mathrm{G}) \%$ | * | * |
| $\pm 0.1 \%$ | * | * |
| $\pm 10 \mathrm{~V}$ @ $\pm 5 \mathrm{~mA}$ | * | * |
| $>2 \mathrm{MHz}$ | * | * |
| 40 kHz | * | * |
| 100 kHz | * | * |
| $10 \mathrm{~V} / \mu \mathrm{sec}$ | * | * |
| 3 mV | 1.5 mV | ** |
| $15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | ** |
| $3 \mu \mathrm{~V} / \%$ | * | * |
| 400 mV | 200 mV | ** |
| $400 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $150 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | ** |
| $0.005\left(\mathrm{~V}_{\mathrm{OS}_{0}}\right) / \%$ | * | * |
| 80nA | 40nA | ** |
| 20 nA | 10 nA | ** |
| $3 \times 10^{9} \Omega$ | * | * |
| $6 \times 10^{10} \Omega$ | * | * |
| $0.5 \mu \mathrm{~V}$ RTI ( $\mathrm{G}=1000$ ) | * | * |
| $\pm 30 \mathrm{~V} \text { (safe) }$ | * | * |
| 15 V beyond $\mathrm{V}_{\mathrm{S}}$ (safe) | * | * |
|  |  | ** |
| $100 \mathrm{~dB}$ | $110 \mathrm{~dB}$ | ** |
| $\pm 5 \mathrm{~V} \text { to } \pm 18 \mathrm{~V}$ | * | * |
| $\pm 5 \mathrm{~mA}$ | * | - |
| 0 to $+70^{\circ} \mathrm{C}$ | * | -55 to $+125^{\circ} \mathrm{C}$ |
| \$12.75 | \$18.00 | \$30.00 |
| $\$ 10.20$ | $\$ 14.40$ | \$24.00 |
| \$8.50 | $\$ 12.00$ |  |

## HIGH SPEED OPERATIONAL AMPLIFIER AD505

The AD505J, AD505K and AD505S are monolithic operational amplifiers that are specifically designed for applications requiring high slew rate and fast settling time to high accuracy. The AD505 achieves a minimum slew rate of $120 \mathrm{~V} / \mu \mathrm{sec}$, provides an adjustable unity gain bandwidth product of 4 MHz to 10 MHz , and settles to $0.1 \%$ in 800 nsec . In addition to its superior dynamic characteristics, the AD505 maintains high gain, maximum offset voltage drift of $15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, maximum bias currents of 25 nA and high output swing.
The circuit has a stable 6 dB /octave rolloff for closed loop operation. It is also capable of being externally adjusted for up to 35 dB of additional closed loop gain at high frequencies, without causing the small signal or large signal bandwidth to decrease, and without increasing settling times.

The AD505 is designed for high speed inverting applications by using a feed-forward technique. It can drive capacitive loads in excess of 1000 pF and is short circuit protected.

All the circuits are supplied in the TO-100 package. The AD505J and AD505K are specified for $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ temperature range operation; the AD505S for operation from $-55^{\circ} \mathrm{C}$ to $+100^{\circ} \mathrm{C}$.

## PIN CONFIGURATION

Top View
feedforward


TO-100

| ELECTRICAL CHARACTERISTICS ( $\left.\mathrm{V}_{\mathrm{S}}= \pm \mathrm{T}_{\mathrm{A}}=\boldsymbol{+ 2 5}{ }^{\circ} \mathrm{C}\right)$ |  |  |  |
| :---: | :---: | :---: | :---: |
| Parameter | AD505J | AD505K | AD505S |
| OPEN LOOP GAIN |  |  |  |
| $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{O}}= \pm 10 \mathrm{~V}$ | 100,000 min ( $500,000 \mathrm{typ}$ ) | 200,000 min (500,000 typ) | ** |
| Over Temp Range ( $\mathrm{T}_{\text {min }}$ to $\mathrm{T}_{\text {max }}$ ) | 75,000 min | 150,000 min | 100,000 min |
| OUTPUT CHARACTERISTICS |  |  |  |
| Voltage @ $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  |
| Over Temp Range ( $\mathrm{T}_{\text {min }}$ to $\mathrm{T}_{\text {max }}$ ) | $\pm 10 \mathrm{~V}$ min ( $\pm 12 \mathrm{~V}$ typ) | * | * |
| Current @ $\mathrm{V}_{\mathrm{O}}= \pm 10 \mathrm{~V}$ | $\pm 10 \mathrm{~mA}$ | * | * |
| Short Circuit Current | 25 mA | * | * |
| FREQUENCY RESPONSE |  |  |  |
| Unity Gain, Small Signal | 4-10MHz (adjustable) | * | * |
| Full Power Response | $2.0 \mathrm{MHz} \min (2.5 \mathrm{MHz}$ typ) | * | * |
| Slew Rate | $120 \mathrm{~V} / \mu \mathrm{sec} \min (150 \mathrm{~V} / \mu \mathrm{sec}$ typ) | * | * |
| Settling Time |  |  |  |
| to 0.1\% | 800nsec | * | * |
| to $0.01 \%$ | $2.0 \mu \mathrm{sec}$ | * | * |
| INPUT OFFSET VOLTAGE |  |  |  |
| Initial, $\mathrm{R}_{\mathrm{S}} \leqslant 10 \mathrm{k} \Omega$ | 5.0 mV max ( 1.0 mV typ) | 2.5 mV max ( 1.0 mV typ) | ** |
| Avg vs Temp ( $\mathrm{T}_{\text {min }}$ to $\mathrm{T}_{\text {max }}$ ) | $15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max \left(8 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\right.$ typ) | $20 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max \left(10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\right.$ typ) |
| vs Supply ( $\mathrm{T}_{\text {min }}$ to $\mathrm{T}_{\text {max }}$ ) | $150 \mu \mathrm{~V} / \mathrm{V} \max (80 \mu \mathrm{~V} / \mathrm{V}$ typ) | * |  |
| INPUT BIAS CURRENT |  |  |  |
| Initial | 75 nA max ( 15 nA typ) | $75 \mathrm{nA} \max (15 \mathrm{nA}$ typ) | 75 |
| Over Temp Range ( $\mathrm{T}_{\min }$ to $\mathrm{T}_{\text {max }}$ ) | 100 nA max | $100 \mathrm{nA} \max$ | 150 nA max |
| Avg vs $\mathrm{Temp}^{( } \mathrm{T}_{\text {min }}$ to $\mathrm{T}_{\text {max }}$ ) | $0.1 \mathrm{nA} /{ }^{\circ} \mathrm{C}$ | * | * |
| INPUT IMPEDANCE |  | - |  |
| DC | 2M $\Omega$ | * | * |
| Above 10Hz | $20 \mathrm{k} \Omega$ | * | * |
| INPUT NOISE |  |  |  |
| Voltage, 0.01 to $10 \mathrm{~Hz}(\mathrm{p}-\mathrm{p})$ | $2.5 \mu \mathrm{~V}$ | * | * |
| 0.01 to $1.0 \mathrm{MHz}(\mathrm{rms})$ | $10 \mu \mathrm{~V}$ | * | * |
| Current, 0.01 to $10 \mathrm{~Hz}(\mathrm{p}-\mathrm{p})$ | 0.1 nA | * | * |
| POWER SUPPLY |  |  |  |
| Rated Performance | $\pm 15 \mathrm{~V}$ | * | * |
| Operating, Derated Performance | $\pm(5$ to 20$) \mathrm{V}$ | * | * |
| Current, Quiescent | 8.0 mA max ( 6.0 mA typ ) | * | * |
|  |  |  |  |
|  |  |  |  |
| Operating | $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | * | $-55^{\circ} \mathrm{C}$ to $+100^{\circ} \mathrm{C}$ (Note 1) |
| Storage | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ | * |  |
| PRICE |  |  |  |
| (1-24) | \$17.25 | \$20.70 | \$24.15 |
| (25-99) | \$13.80 | \$16.55 | \$19.30 |
| (100-999) | \$11.50 | \$13.80 | \$16.10 |

${ }^{1}+125^{\circ} \mathrm{C}$ operation is possible with a $100^{\circ} \mathrm{C} / \mathrm{W}$ heat sink.
*Specifications same as AD505J.
**Specifications same as AD505K.

# WIDEBAND, FAST SLEWING GENERAL PURPOSE OP AMP AD507 

## GENERAL DESCRIPTION

The AD507J, AD507K, and AD507S are low cost high performance monolithic operational amplifiers that combine slew rates of $35 \mathrm{~V} / \mu \mathrm{sec}$ and 100 MHz gain bandwidth with bias and offset currents below 10 nA , and gain of $150,000 \mathrm{~V} / \mathrm{V}$. They are intended for applications where performance superior to that of the popular AD741 or AD101A series is required, and are especially well suited for use in fast high impedance comparators, integrators, wideband amplifiers, and in sample-and-hold circuits. The AD507 is stable at closed loop gains above ten due to its internal 6 dB per octave rolloff. External compensation provides stability to unity gain, and permits flexibility for special frequency applications. The circuit is short circuit protected and offset voltage nullable. Both the AD507J and AD507K

are supplied in the TO-99 package for operation over the 0 to $+70^{\circ} \mathrm{C}$ temperature range. The AD507S is specified for operation from $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$.

| SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ and $\pm 15 \mathrm{VDC}$ unless otherwise noted) |  |  |  |
| :---: | :---: | :---: | :---: |
| Model | AD507J | AD507 K | AD507S |
| Open Loop Gain |  |  |  |
| $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ | $80,000 \mathrm{~min}(150,000$ typ $)$ | $100,000 \mathrm{~min}(150,000$ typ) | $100,000 \mathrm{~min}(150,000$ typ $)$ |
| Over Temp Range ( $\mathrm{T}_{\text {min }}$ to $\mathrm{T}_{\text {max }}$ ) | 70,000 min | 85,000 min | $70,000 \mathrm{~min}$ |
| Output Characteristics |  |  |  |
| Voltage @ $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |  |
| Over Temp Range ( $\mathrm{T}_{\text {min }}$ to $\mathrm{T}_{\text {max }}$ ) | $\pm 10 \mathrm{~V}$ min $( \pm 12 \mathrm{~V}$ typ $)$ | * | * |
| Current @ $\mathrm{V}_{\mathrm{o}}= \pm 10 \mathrm{~V}$ | $\pm 10 \mathrm{~mA} \mathrm{~min}( \pm 20 \mathrm{~mA} \mathrm{typ})$ | * | $\pm 15 \mathrm{~mA}$ min $( \pm 22 \mathrm{~mA}$ typ) |
| Short Circuit Current | 25 mA | * | * |
| Frequency Response |  |  |  |
| Unity Gain, Small Signal |  |  |  |
| (a) $\mathrm{A}=1$ (open loop) | 35 MHz | * | * |
| (a) $\mathrm{A}=100$ (closed loop) | 100 MHz | ${ }^{*}$ | * ${ }^{*}$ |
| Full Power Response | 320 kHz min ( 600 kHz typ) | 400 kHz min ( 600 kHz typ) | 400 kHz min ( 600 kHz typ) |
| Slew Rate | $\pm 20 \mathrm{~V} / \mu \mathrm{sec} \mathrm{min}( \pm 35 \mathrm{~V} / \mu \mathrm{sec}$ typ $)$ | $\pm 25 \mathrm{~V} / \mu \mathrm{sec} \min ( \pm 35 \mathrm{~V} / \mu \mathrm{sec}$ typ $)$ | $\pm 20 \mathrm{~V} / \mu \mathrm{sec}( \pm 35 \mathrm{~V} / \mu \mathrm{sec}$ typ) |
| Settling Time (to 0.1\%) | 900 ns | * | * ${ }^{*}$ |
| Input Offset Voltage |  |  |  |
| Initial | $5.0 \mathrm{mV} \max (3.0 \mathrm{mV}$ typ) | $3.0 \mathrm{mV} \max (1.5 \mathrm{mV}$ typ) | $4.0 \mathrm{mV} \max (0.5 \mathrm{mV}$ typ) |
| Avg vs Temp, ( $\mathrm{T}_{\min }$ to $\mathrm{T}_{\text {max }}$ ) | $15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $15 \mu \mathrm{~V} /^{\circ} \mathrm{C} \max \left(8 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \text { typ }\right)$ | $20 \mu \mathrm{~V} /^{\circ} \mathrm{C} \max \left(8 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \text { typ }\right)$ |
| vs Supply, ( $\mathrm{T}_{\min }$ to $\mathrm{T}_{\max }$ ) | $200 \mu \mathrm{~V} / \mathrm{V} \max$ | $100 \mu \mathrm{~V} / \mathrm{V} \max$ | $100 \mu \mathrm{~V} / \mathrm{V} \max$ |
| Input Bias Current |  |  |  |
| Initial | 25 nA max | 15 nA max | 15 nA max |
| Over Temp Range ( $\mathrm{T}_{\min }$ to $\mathrm{T}_{\max }$ ) | $40 n \mathrm{~A}$ max | 25 nA max | 35 nA max |
| Input Offset Current ${ }^{\text {min }}$ max ${ }^{\text {max }}$ |  |  |  |
| Initial | $25 n \mathrm{n}$ max | 15 nA max | 15 nA max |
|  |  |  | $35 \mathrm{nA} \max$ |
| Avg vs Temp ( $\mathrm{T}_{\min }$ to $\mathrm{T}_{\max }$ ) | $0.5 \mathrm{nA} /{ }^{\circ} \mathrm{C}$ | $0.2 \mathrm{nA} /{ }^{\circ} \mathrm{C}$ | $0.2 \mathrm{nA} /{ }^{\circ} \mathrm{C}$ |
| Input Impedance |  |  |  |
| Differential | $40 \mathrm{M} \Omega \min (300 \mathrm{M} \Omega$ typ) | * | * |
| Common Mode | $1000 \mathrm{M} \Omega$ | * | * |
| Input Voltage Noise |  |  |  |
| $\mathrm{f}=10 \mathrm{~Hz}$ | $100 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ | * | * |
| $\mathrm{f}=100 \mathrm{~Hz}$ | $30 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ | * | * |
| $\mathrm{f}=100 \mathrm{kHz}$ | $12 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ | * | * |
| Input Voltage Range |  |  |  |
| Differential, Max Safe | $\pm 12.0 \mathrm{~V}$ | * | * |
| Common Mode Voltage Range |  |  |  |
| $\mathrm{T}_{\min }$ to $\mathrm{T}_{\max }$ | $\pm 11.0 \mathrm{~V}$ | * | * |
| Common Mode Rejection @ $\pm 15 \mathrm{~V}$ |  |  |  |
| $\mathrm{T}_{\min }$ to $\mathrm{T}_{\text {max }}$ | 74 dB min ( 100 dB typ) | 80 dB min ( 100 dB typ) | 80 dB min ( 100 dB typ) |
| Power Supply |  |  |  |
| Rated Performance | $\pm 15 \mathrm{~V}$ | * | * |
| Operating | $\pm(5$ to 20$) \mathrm{V}$ | * | * |
| Current, Quiescent | 4.0 mA max ( 3.0 mA typ ) | * | * |
| Temperature Range |  |  |  |
| Rated Performance | 0 to $+70^{\circ} \mathrm{C}$ | * | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| Storage | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ | * | . |
| Price |  |  |  |
| (1-24) | \$9.50 | \$15.00 | \$22.50 |
| (25-99) | \$8.10 | \$12.00 | \$18.00 |
| (100-999) | \$6.95 | \$10.00 | \$15.00 |
| *Specifications same as AD507J. |  |  |  |

## HIGH SPEED, FAST SETTLING OPERATIONAL AMPLIFIER AD509 <br> PIN CONFIGURATION <br> Top View

## GENERAL DESCRIPTION

The AD509J, AD509K and AD509S are fast differential input operational amplifiers whose combination of low cost and excellent dynamic characteristics make them well suited for 12bit D/A and A/D circuits, sample/hold circuits, multiplexers, and other applications requiring fast settling time to low error levels. Of particular significance are the maximum settling time specifications of $2.0 \mu \mathrm{sec}$ to $0.01 \%$ and 500 nsec to $0.1 \%$ of the AD509K and AD509S.

Other excellent specifications include unity gain small signal bandwidth of 20 MHz , slew rate of $120 \mathrm{~V} / \mu \mathrm{sec}$, and $\pm 10 \mathrm{~mA}$ minimum output current at $\pm 10 \mathrm{~V}$. The AD509 is stable for

all values of closed loop gain greater than 3 without external compensation, and can be stabilized with a single external capacitor for any value of closed-loop gain. The AD509J and AD509K are specified for operation from 0 to $+70^{\circ} \mathrm{C}$; the AD509S from $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$. All models are supplied in the TO-99 metal can package.

SPECIFICATION SUMMARY (Typical @ $+25^{\circ} \mathrm{C}$ and $\pm 15 \mathrm{VDC}$, unless otherwise specified)

| Model | AD509J | AD509K | AD509S |
| :---: | :---: | :---: | :---: |
| Open Loop Gain $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ <br> (@ $T_{A}=\min$ to $\max$ | $\begin{gathered} 7,500 \min (15,000 \mathrm{typ}) \\ 5,000 \mathrm{~min} \end{gathered}$ | $\begin{gathered} 10,000 \min (15,000 \text { typ }) \\ 7,500 \mathrm{~min} \end{gathered}$ | ** |
| Output Characteristics <br> Voltage @ $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=\min$ to $\max$ <br> Current @ $\mathrm{V}_{\mathrm{O}}= \pm 10 \mathrm{~V}$ <br> Short Circuit Current | $\begin{gathered} \pm 10 \mathrm{~V} \min ( \pm 12 \mathrm{~V} \text { typ }) \\ \pm 10 \mathrm{~mA} \min ( \pm 20 \mathrm{~mA} \text { typ }) \\ 25 \mathrm{~mA} \end{gathered}$ | 俍 | * |
| ```Frequency Response Unity Gain, Small Signal Full Power Response, \(\mathrm{V}_{\mathrm{O}}= \pm 10 \mathrm{~V}\) Slew Rate, \(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{O}}= \pm 10 \mathrm{~V}, \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\) Settling Time to \(0.1 \%\) to \(0.01 \%\)``` | 20 MHz $120 \mathrm{kHz} \min (1.6 \mathrm{MHz}$ typ $)$ $80 \mathrm{~V} / \mu \mathrm{sec} \min (120 \mathrm{~V} / \mu \mathrm{sec}$ typ $)$ 200 nsec $1 \mu \mathrm{sec}$ | $150 \mathrm{kHz} \min (2 \mathrm{MHz}$ typ) $100 \mathrm{~V} / \mu \mathrm{sec} \min (120 \mathrm{~V} / \mu \mathrm{sec}$ typ) <br> 500nsec max (200nsec typ) $2 \mu \mathrm{sec} \max (1 \mu \mathrm{sec}$ typ) | ** |
| Input Offset Voltage <br> Initial <br> $\mathrm{T}_{\mathrm{A}}=\min$ to $\max$ <br> Avg vs Temperature, $\mathrm{T}_{\mathrm{A}}=\min$ to $\max$ vs Supply, $\mathrm{T}_{\mathrm{A}}=\min$ to $\max$ | $\begin{gathered} 10 \mathrm{mV} \max (5 \mathrm{mV} \text { typ }) \\ 14 \mathrm{mV} \max \\ 20 \mu \mathrm{~V} / \circ^{\circ} \mathrm{C} \\ 200 \mu \mathrm{~V} / \mathrm{V} \max \end{gathered}$ | $\begin{gathered} 8 \mathrm{mV} \max (4 \mathrm{mV} \text { typ }) \\ 11 \mathrm{mV} \max \\ 30 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max \left(20 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \text { typ }\right) \\ 100 \mu \mathrm{~V} / \mathrm{V} \max \end{gathered}$ | ** |
| Input Bias Current Initial $\mathrm{T}_{\mathrm{A}}=\min$ to $\max$ | $\begin{gathered} 250 \mathrm{nA} \max (125 \mathrm{nA} \text { typ }) \\ 500 \mathrm{nA} \max \\ \hline \end{gathered}$ | $\begin{gathered} 200 \mathrm{nA} \max (100 \mathrm{nA} \text { typ) } \\ 400 \mathrm{nA} \max \\ \hline \end{gathered}$ | *** |
| Input Offset Current Initial $\mathrm{T}_{\mathrm{A}}=\min$ to $\max$ | $\begin{gathered} 50 \mathrm{nA} \max (20 \mathrm{nA} \text { typ }) \\ 100 \mathrm{nA} \max \\ \hline \end{gathered}$ | $\begin{gathered} 25 \mathrm{nA} \max (10 \mathrm{nA} \text { typ) } \\ 50 \mathrm{nA} \max \end{gathered}$ | ** |
| Input Impedance Differential | $40 \mathrm{M} \Omega \min (300 \mathrm{M} \Omega$ typ) | $50 \mathrm{M} \Omega \min (300 \mathrm{M} \Omega$ typ) | ** |
| Input Voltage Range <br> Differential, max safe <br> Common Mode Voltage Range, $\mathrm{T}_{\mathrm{A}}=\min \text { to } \max$ <br> Common Mode Rejection @ $\pm 5 \mathrm{~V}$, $\mathrm{T}_{\mathrm{A}}=\min \text { to } \max$ | $\begin{gathered} \pm 15 \mathrm{~V} \\ \pm 10 \mathrm{~V} \\ 74 \mathrm{~dB} \min (90 \mathrm{~dB} \text { typ }) \end{gathered}$ | $80 \mathrm{~dB} \min (90 \mathrm{~dB} \text { typ) }$ |  |
| Power Supply Rated Performance Operating Current, Quiescent | $\begin{gathered} \pm 15 \mathrm{~V} \\ \pm(5 \text { to } 20) \mathrm{V} \\ \text { 6mA max (4mA typ) } \end{gathered}$ |  |  |
| Temperature Range Rated Performance Storage | $\begin{array}{r} 0 \text { to }+70^{\circ} \mathrm{C} \\ -65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C} \\ \hline \end{array}$ | * ${ }^{*}$ | $-55^{\circ} \mathrm{C} \text { to }+125^{\circ}$ |
| $\begin{aligned} & \text { Price } \\ & \quad(1-24) \\ & (25-99) \\ & (100-999) \end{aligned}$ | $\begin{gathered} \$ 11.50 \\ \$ 10.20 \\ \$ 8.50 \\ \hline \end{gathered}$ | $\begin{aligned} & \$ 18.75 \\ & \$ 15.00 \\ & \$ 12.50 \end{aligned}$ | $\begin{aligned} & \$ 26.00 \\ & \$ 22.00 \\ & \$ 19.00 \end{aligned}$ |

*Specifications same as AD509 J.
${ }^{* *}$ Specifications same as AD509K.

# HIGH SPEED,LOW COST, OPERATIONAL AMPLIFIER 

## GENERAL DESCRIPTION

The AD518J, AD518K, and AD518S are precision high speed monolithic operational amplifiers designed for applications where high slew rate and wide bandwidth are required but low cost and ease of use are essential. The devices are internally compensated for unity gain applications with a $60^{\circ}$ phase margin to insure stability, a minimum slew rate of $50 \mathrm{~V} / \mu \mathrm{sec}$, and a typical bandwidth of 12 MHz . In addition, in inverting applications, external feedforward compensation may be added to increase the slew rate to over $100 \mathrm{~V} / \mu \mathrm{sec}$, and nearly double the bandwidth. If desired, settling time to $0.1 \%$ can be reduced to under $1 \mu \mathrm{sec}$ with a single external capacitor.
The AD518's dc performance is consistent with its precision dynamic characteristics. The devices feature offset voltages below 2 mV , maximum offset drifts of $10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, and offset currents below 50 nA max.


The high slew rate, fast settling time, ease of use, and low cost of the AD518 make it ideal for use with the D/A and A/D converters, as well as active filters, sample and hold circuits, and as a general purpose amplifier. The AD5 18 is supplied in the TO-99 package. The AD518J and AD518K are specified for operation over the 0 to $+70^{\circ} \mathrm{C}$ temperature range; the AD518S for operation from $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$.


ELECTRICAL SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ and $\pm 15 \mathrm{VDC}$, unless otherwise noted.)

| Parameter | AD518J | AD518K | AD518S |
| :---: | :---: | :---: | :---: |
| Open Loop Gain $\begin{aligned} & \mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k}, \mathrm{~V}_{\mathrm{O}}= \pm 10 \mathrm{~V} \\ & \text { @ } \mathrm{T}_{\mathrm{A}}=\min \text { to } \max \end{aligned}$ | $\begin{gathered} 25,000 \mathrm{~min}(200,000 \mathrm{typ}) \\ 20,000 \mathrm{~min} \end{gathered}$ | $\begin{gathered} 50,000 \min (200,000 \mathrm{typ}) \\ 25,000 \mathrm{~min} \end{gathered}$ | $\begin{gathered} 50,000 \mathrm{~min}(200,000 \text { typ }) \\ 25,000 \mathrm{~min} \\ \hline \end{gathered}$ |
| Output Characteristics <br> Voltage @ $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}=\min$ to $\max$ <br> Current (@ $\mathrm{V}_{\mathrm{O}}= \pm 10 \mathrm{~V}$ <br> Short Circuit Current | $\begin{gathered} \pm 12 \mathrm{~V} \min ( \pm 13 \mathrm{~V} \text { typ }) \\ \pm 10 \mathrm{~mA} \min \\ 25 \mathrm{~mA} \end{gathered}$ |  |  |
| Frequency Response <br> Unity Gain, Small Signal <br> Slew Rate, Unity Gain <br> Settling Time to $0.1 \%$ <br> (Single Capacitor Compensation) <br> Phase Margin, Uncompensated at Unity Gain Crossover Frequency | 12 MHz typ $50 \mathrm{~V} / \mu \mathrm{sec} \min (70 \mathrm{~V} / \mu \mathrm{sec}$ typ $)$ 800 nsec $+60^{\circ}$ | $10 \mathrm{MHz} \min (12 \mathrm{MHz}$ typ) | $10 \mathrm{MHz} \min (12 \mathrm{MHz} \text { typ) }$ |
| Input Offset Voltage <br> Initial, $\mathrm{R}_{\mathrm{S}} \leqslant 10 \mathrm{k} \Omega$ <br> $\mathrm{T}_{\mathrm{A}}=\min$ to $\max$ <br> Avg vs Temp, $\mathrm{T}_{\text {min }}$ to $\mathrm{T}_{\text {max }}$ <br> Avg vs Supply, $\mathrm{T}_{\text {min }}$ to $\mathrm{T}_{\text {max }}$ | $\begin{gathered} 10 \mathrm{mV} \max (4 \mathrm{mV} \text { typ }) \\ 15 \mathrm{mV} \max \\ 10 \mu \mathrm{~V} / /^{\circ} \mathrm{C} \\ 65 \mathrm{~dB} \min (80 \mathrm{~dB} \text { typ }) \end{gathered}$ | $\begin{gathered} 4 \mathrm{mV} \max (2 \mathrm{mV} \text { typ }) \\ 6 \mathrm{mV} \max \\ 10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max \left(5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \text { typ }\right) \\ 70 \mathrm{~dB} \min (80 \mathrm{~dB} \text { typ }) \end{gathered}$ | $\begin{gathered} 4 \mathrm{mV} \max (2 \mathrm{mV} \text { typ }) \\ 6 \mathrm{mV} \max \\ 10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max \left(5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \text { typ }\right) \\ 70 \mathrm{~dB} \min (80 \mathrm{~dB} \text { typ }) \\ \hline \end{gathered}$ |
| Input Bias Current Initial $\mathrm{T}_{\mathrm{A}}=\min$ to $\max$ | $\begin{gathered} 500 \mathrm{nA} \max (120 \mathrm{nA} \text { typ) } \\ 750 \mathrm{nA} \max \\ \hline \end{gathered}$ | $\begin{gathered} 200 \mathrm{nA} \max (120 \mathrm{nA} \text { typ }) \\ 400 \mathrm{nA} \max \\ \hline \end{gathered}$ | $\begin{gathered} 200 \mathrm{nA} \max (120 \mathrm{nA} \text { typ }) \\ 400 \mathrm{nA} \max \end{gathered}$ |
| Input Offset Current Initial <br> $\mathrm{T}_{\mathrm{A}}=\min$ to $\max$ | $\begin{gathered} 200 \mathrm{nA} \max (30 \mathrm{nA} \text { typ }) \\ 300 \mathrm{nA} \max \\ \hline \end{gathered}$ | $\begin{gathered} 50 \mathrm{nA} \max (6 \mathrm{nA} \text { typ }) \\ 100 \mathrm{nA} \max \\ \hline \end{gathered}$ | $\begin{gathered} \text { 50nA max }(6 \mathrm{nA} \text { typ }) \\ 100 \mathrm{nA} \max \end{gathered}$ |
| Input Impedance Differential | $0.5 \mathrm{M} \Omega \min (3 \mathrm{M} \Omega$ typ $)$ | * | * |
| $\begin{aligned} & \text { Input Voltage Range } \\ & \quad \text { Differential, max safe } \\ & \text { Common Voltage Rejection Ratio } \\ & \hline \end{aligned}$ | $\begin{gathered} \pm \mathrm{V}_{\mathrm{S}}, \mathrm{~V}_{\mathrm{S}} \leqslant 15 \mathrm{~V} \\ 70 \mathrm{~dB} \min (100 \mathrm{~dB} \text { typ }) \end{gathered}$ | $80 \mathrm{~dB} \min (100 \mathrm{~dB} \text { typ })$ | $80 \mathrm{~dB} \min (100 \mathrm{~dB}$ typ) |
| Power Supply Rated Performance Operating Current, Quiescent | $\begin{gathered} \pm 15 \mathrm{~V} \\ \pm(5 \text { to } 20) \mathrm{V} \\ 10 \mathrm{~mA} \max (5 \mathrm{~mA} \text { typ }) \end{gathered}$ |  | $7 \mathrm{~mA} \stackrel{*}{*} \max (5 \mathrm{~mA}$ typ $)$ |
| Temperature Range Rated Performance Storage | $\begin{gathered} 0 \text { to }+70^{\circ} \mathrm{C} \\ -65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C} \end{gathered}$ | $*$ $*$ | $-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C}$ |
| Price $\begin{aligned} & (1-24) \\ & (25-99) \\ & (100-999) \end{aligned}$ | $\begin{aligned} & \$ 3.00 \\ & \$ 2.40 \\ & \$ 1.95 \end{aligned}$ | $\begin{aligned} & \$ 7.20 \\ & \$ 6.00 \\ & \$ 4.95 \end{aligned}$ | $\begin{aligned} & \$ 17.95 \\ & \$ 14.35 \\ & \$ 11.95 \end{aligned}$ |

*Specifications same as for AD518J.

# LOW COST, HIGH SPEED, IC OP AMPS ADXII8, ADX218, ADX318 

## PRODUCT DESCRIPTION

The ADX318, ADX218, and ADX118 are high speed precision monolithic operational amplifiers designed for applications where slew rate and wide bandwidth are required, but low cost and ease of use are essential. The devices are internally compensated for unity gain applications with a $60^{\circ}$ phase margin to insure stability, a minimum unity gain slew rate of $50 \mathrm{~V} / \mu \mathrm{sec}$ and a typical bandwidth of 12 MHz . In addition, in inverting applications external feedforward compensation may be added to increase the slew rate to over $100 \mathrm{~V} / \mu \mathrm{sec}$, and nearly double the bandwidth. If desired, settling time to $0.1 \%$ can be reduced to under $1 \mu \mathrm{sec}$ with a single external capacitor.
The ADX118/218/318's dc performance is consistent with its precision dynamic characteristics. The devices feature offset voltages below 2 mV , offset drifts of $15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, and offset currents below 50 nA max.

# PIN CONFIGURATION 



The high slew rate, fast settling time, ease of use, and low cost of the ADX118 series make it ideal for use with D/A and A/D converters, as well as active filters, sample-and-hold circuits, and as a general purpose, fast, wideband amplifier.
The ADX318 is specified for operation over the 0 to $+70^{\circ} \mathrm{C}$ temperature range, the ADX218 for operation over the $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ temperature range, and the ADX118 for operation from $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$.
SPECIFICATIONS (Typical at $+25^{\circ} \mathrm{C}$ and $\pm 15 \mathrm{~V}$ unless otherwise noted)

| PARAMETER | ADX318 | ADX218 | ADX118 |
| :---: | :---: | :---: | :---: |
| ABSOLUTE MAXIMUM RATINGS |  |  |  |
| Supply Voltage | $\pm 20 \mathrm{~V}$ | * | * |
| Power Dissipation (Note 1) | 500 mW | * | * |
| Differential Input Current (Note 2) | $\pm 10 \mathrm{~mA}$ | * | * |
| Input Voltage (Note 3) | $\pm 15 \mathrm{~V}$ | * | * |
| Output Short Circuit Duration | Indefinite | * | * |
| Operating Temperature Range | 0 to $+70^{\circ} \mathrm{C}$ | $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ | ${ }^{*}$ |  |
| Lead Temperature (Soldering, 10 sec ) | $+300^{\circ} \mathrm{C}$ | * | * |
| INPUT OFFSET VOLTAGE, |  |  |  |
| INPUT OFFSET CURRENT, |  |  |  |
| INPUT BIAS CURRENT, |  |  |  |
| INPUT RESISTANCE, |  |  |  |
| SUPPLY CURRENT |  |  |  |
| $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | 10 mA Max ( 5 mA Typ ) | $8 \mathrm{~mA} \mathrm{Max}(5 \mathrm{~mA} \mathrm{Typ})$ | ** |
| $\mathrm{T}_{\mathrm{A}}=+125^{\circ} \mathrm{C}$ | -- | $7 \mathrm{~mA} \mathrm{Max} \mathrm{( } 4.5 \mathrm{~mA} \mathrm{Typ}$ ) | ** |
| LARGE SIGNAL VOLTAGE GAIN |  |  |  |
| $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{~V}_{\mathrm{S}}= \pm 15 \mathrm{~V},$ |  |  |  |
| SLEW RATE, $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, $\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}, \mathrm{~A}_{\mathrm{v}}=1$ | 50V/ $/ \mathrm{s}$ Min ( $70 \mathrm{~V} / \mathrm{\mu s}$ Typ) | * | * |
| SMALL SIGNAL BANDWIDTH |  |  |  |
| $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$ | 15 MHz | * | * |
| INPUT OFFSET VOLTAGE | 15 mV Max | 6 mV Max | ** |
| INPUT OFFSET CURRENT | 300nA Max | 100 nA Max | ** |
| INPUT BIAS CURRENT | 750 nA Max | 500 nA Max | ** |
| LARGE SIGNAL VOLTAGE GAIN $\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}, \mathrm{~V}_{\mathrm{OUT}}= \pm 10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega$ | $20 \mathrm{~V} / \mathrm{mV}$ Min | $25 \mathrm{~V} / \mathrm{mV}$ Min | ** |
| OUTPUT VOLTAGE SWING | $\pm 12 \mathrm{~V}$ Min ( $\pm 13 \mathrm{~V}$ Typ) | * | * |
| INPUT VOLTAGE RANGE, $\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$ | $\pm 11.5 \mathrm{~V}$ Min | * | * |
| COMMON MODE REJECTION RATIO | 70 dB Min ( 100 dB Typ) | 80 dB Min ( 100 dB Typ) | ** |
| SUPPLY VOLTAGE REJECTION RATIO | 65 dB Min ( 80 dB Typ) | 70 dB Min ( 80 dB Typ) | ** |
| PRICES |  |  |  |
| (1-24) | \$2.95 | \$16.40 | \$26.90 |
| (25-99) | \$2.35 | \$13.10 | \$21.55 |
| (100's) | \$1.95 | \$10.95 | \$17.95 |
| NOTE 1. The maximum junction temperature of the ADXi 18 is $+150^{\circ} \mathrm{C}$, of the $\operatorname{ADX} 218$ is $+100^{\circ} \mathrm{C}$, while that of the $\operatorname{ADX} 318$ is $+85^{\circ} \mathrm{C}$. For operating at elevated temperatures, devices in the TO- 5 package must be derated based on a thermal resistance of $150^{\circ} \mathrm{C} / \mathrm{W}$, junction to ambient, or $45^{\circ} \mathrm{C} / \mathrm{W}$, junction to case. For the flat package, the derating is based on a thermal resistance of $185^{\circ} \mathrm{C} / \mathrm{W}$ when mounted on a $1 / 16$-inch-thick epoxy glass board with ten, 0.03 -inch-wide, 2 -ounce copper conductors. The thermal resistance of the dual-in-line package is $100^{\circ} \mathrm{C} / \mathrm{W}$, junction to ambient. |  |  |  |
| NOTE 2. The inputs are shunted with back differential input voltage in exce | or overvoltage protection. Theref between the inputs unless some | , excessive current will flow if a miting resistance is used. |  |
| NOTE 3. For supply voltages less than $\pm 15 \mathrm{~V}$ NOTE 4. These specifications apply for $\pm 5 \mathrm{~V}$ | naximum input voltage is equal to | he supply voltage. |  |
| NOTE 4. These specifications apply for $\pm 5$ cations are limited to $-55^{\circ} \mathrm{C} \leqslant \mathrm{T}_{A}$ $\leqslant+70^{\circ} \mathrm{C}$. Also, power supplies m | nless otherwise specified. With th the ADX218, $-25^{\circ} \mathrm{C} \leqslant \mathrm{T}_{\mathrm{A}} \leqslant+85^{\circ}$ with $0.1 \mu \mathrm{~F}$ disc capacitors. | ADX118, all temperature specifi; with the ADX $318,0^{\circ} \mathrm{C} \leqslant \mathrm{T}_{\mathrm{A}}$ |  |
| *Specification same as ADX318. <br> **Specification same as ADX218. |  |  |  |

## LOW NOISE, LOW COST, FET-INPUT OP AMP

## PRODUCT DESCRIPTION

The AD528J, AD528K and AD528S are high speed, precision FET-input operational amplifiers combining the advantages of very high slew rate and wide bandwidth with the ultra-low input currents only available with FET-input designs. The devices are internally compensated for unity gain applications with a $60^{\circ}$ phase margin to insure stability, a minimum unity gain slew rate of $50 \mathrm{~V} / \mu \mathrm{sec}$, and a typical bandwidth of 10 MHz In addition, in inverting applications external feed forward compensation may be added to increase the slew rate to over $100 \mathrm{~V} / \mu \mathrm{sec}$, and nearly double the bandwidth. If desired, settling time to $0.1 \%$ can be reduced to under $1 \mu \mathrm{sec}$ with a single external capacitor.

The AD528 offers the user dc performance previously unavailable in conventional high speed designs. The devices offer maximum bias currents under 15 pA , laser-trimmed offset voltages below 1 mV , and offset voltage drifts below $25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$.

## PIN CONFIGURATION

Top View
BALANCE
COMPENSATION 2


The high slew rate, wide bandwidth, and low input currents of the AD528 make it ideal for use in sample-hold circuits, A/D, D/A and sampled data systems, and high speed integrators. The AD528 is supplied in the TO-99 package. The AD528J and AD528K are specified for operation over the 0 to $+70^{\circ} \mathrm{C}$ temperature range; the AD 528 S for operation from -55 to $+125^{\circ} \mathrm{C}$.

SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ and $\pm 15$ VDC unless otherwise specified)

| MODEL | AD528J | AD528K | AD528S |
| :---: | :---: | :---: | :---: |
| OPEN LOOP GAIN |  |  |  |
| $\mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{O}}= \pm 10 \mathrm{~V}$ | 25,000 min (100,000 typ) | $50,000 \mathrm{~min}(100,000$ typ $)$ | ** |
| (a) $\mathrm{T}_{\mathrm{A}}=\min$ to $\max$ | $25,000 \mathrm{~min}$ | 25,000 | ** |
| OUTPUT CHARACTERISTICS |  |  |  |
| Voltage (a) $\mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=\min$ to $\max$ | $\pm 10 \mathrm{~V} \mathrm{~min}$ | * | * |
| Current @ $\mathrm{V}_{\mathrm{O}}= \pm 10 \mathrm{~V}$ | $\pm 10 \mathrm{~mA}$ | * | * |
| Short Circuit Current | 25 mA | * | * |
| FREQUENCY RESPONSE |  |  |  |
| Unity Gain, Small Signal | 10 MHz | * | * |
| Slew Rate, Unity Gain | $50 \mathrm{~V} / \mu \mathrm{sec} \mathrm{min}(70 \mathrm{~V} / \mu \mathrm{sec}$ typ $)$ | * | * |
| Settling Time to $0.1 \%$ |  |  |  |
| (Single Capacitor Compensation) | 800 nsec | * | * |
| Phase Margin, Uncompensated at |  |  |  |
| Unity Gain Crossover Frequency | $60^{\circ}$ | * | * |
| INPUT OFFSET VOLTAGE |  |  |  |
| Initial, $\mathrm{R}_{\mathrm{S}} \leqslant 10 \mathrm{k} \Omega$ | $3 \mathrm{mV} \max (1 \mathrm{mV}$ typ) | $1 \mathrm{mV} \max (0.3 \mathrm{mV}$ typ) | ** |
| (a) $\mathrm{T}_{\mathrm{A}}=\min$ to $\max$ | 5 mV max | 2 mV max | 3 mV max |
| Avg vs Temp, $\mathrm{T}_{\mathrm{A}}=\min$ to $\max$ | $50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max \left(25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\right.$ typ $)$ | $25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \max \left(10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\right.$ typ $)$ | ** |
| Avg vs Supply, $\mathrm{T}_{\mathrm{A}}=\min$ to $\max$ | 70 dB min ( 90 dB typ) | 80 dB min (90dB typ) | ** |
| INPUT BIAS CURRENT |  |  |  |
| Warmed up at $25^{\circ} \mathrm{C}$ | $30 \mathrm{pA} \max (10 \mathrm{pA}$ typ) | $15 \mathrm{pA} \max$ ( 5 pA typ) | ** |
| INPUT OFFSET CURRENT |  |  |  |
| Warmed up at $25^{\circ} \mathrm{C}$ | 5pA max | 2pA max | ** |
| INPUT NOISE |  |  |  |
| Voltage, 0.1 to 10 Hz | $5 \mu \mathrm{~V}(\mathrm{p}-\mathrm{p})$ | * | * |
| INPUT IMPEDANCE |  |  |  |
| Differential | $10^{12} \Omega \\| 6 \mathrm{pF}$ | * | * |
| INPUT VOLTAGE RANGE |  |  |  |
| Differential (Note 1) | $\pm 20 \mathrm{~V}$ | * | * |
| Common Mode, max safe | $\pm \mathrm{V}_{\text {S }}$ | * | * |
| Common Mode Rejection Ratio | 70 dB min ( 90 dB typ) | 80 dB min $(90 \mathrm{~dB}$ typ) | ** |
| POWER SUPPLY |  |  |  |
| Rated Performance | $\pm 15 \mathrm{~V}$ | * |  |
| Operating | $\pm(5$ to 20$) \mathrm{V}$ | * | * |
| Current, Quiescent | $7 \mathrm{~mA} \max$ ( 5 mA typ) | * | * |
| TEMPERATURE RANGE |  |  |  |
| Rated Performance | $0 \text { to }+70^{\circ} \mathrm{C}$ | * | -55 to $+125^{\circ} \mathrm{C}$ |
| Storage | $-65 \text { to }+150^{\circ} \mathrm{C}$ | * |  |
| PRICE |  |  |  |
| (1-24) | \$18.00 | \$24.00 | \$42.00 |
| (25-99) | \$14.40 | \$19.20 | \$33.60 |
| (100-999) | \$12.00 | \$16.00 | \$28.00 |
| *Specifications same as AD528J. <br> **Specifications same as AD528K. | TE 1. Defined as voltage betwee $\pm 10 \mathrm{~V}$ from ground. | inputs such that neither exceeds |  |

# LOW IB, HIGH ACCURACY BIPOLAR OP AMPS 

 ADIO8, ADIO8ATop View



## GENERAL DESCRIPTION

The AD108 and AD108A series offer a level of input isolation ranging between that of general purpose op amps, such as the AD741 or AD101A families, and the high performance FET op amps, such as the AD506 or AD516 series. The use of superbeta transistors in the input stage, combined with extremely precise processing results in guaranteed input currents nearly a thousand times lower than those of the AD741. The AD108, AD208, and AD308 feature excellent input characteristics, with typical $I_{b}$ of less than $1.0 n A, I_{O S}$ of less than 100 pA , and $\mathrm{V}_{\text {OS }}$ of less than 1.0 mV . In addition, the devices are tightly specified for temperature drift operation, with a maximum voltage drift of $15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ for the AD108 and AD208, and $30 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$
for the AD308. The " A " series offer several improved specifications, including maximum $V_{O S}$ of 0.5 mV , minimum gain of 80,000 , maximum voltage drift of $5.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$, and minimum CMRR of 96 dB . The capability of both series to operate with supply voltages as low as $\pm 2 \mathrm{~V}$, and their extremely low power consumption, make them ideal for battery-powered applications. Frequency compensation is accomplished externally, in most cases with a single capacitor.
All the amplifiers are supplied in the TO-99 metal can package; the AD108 and AD108A are specified for operation from $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$, the AD208 and AD208A from $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$, and the AD308 and AD308A from 0 to $+70^{\circ} \mathrm{C}$.

SPECIFICATION SUMMARY (Typical @ $+25^{\circ} \mathrm{C}$ and $\pm 15$ VDC power supply unless otherwise noted.)

| Model | AD108 | AD208 | AD308 | AD108A | AD208A | AD308A |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Open Loop Gain |  |  |  |  |  |  |
| DC Rated, Load, V/V Min | 50,000 | 50,000 | 25,000 | 50,000 | 50,000 | 25,000 |
| Rated Output, Min, $\mathrm{R}_{\mathrm{L}} \geqslant 10 \mathrm{k} \Omega$ | $\pm 13 \mathrm{~V}$ | * | * | * | * | * |
| Frequency Response |  |  |  |  |  |  |
| Unity Gain, Small Signal (Variable |  |  |  |  |  |  |
| With External Compensation) | 0.3 to 3.0 MHz | * | * | * | * | * |
| Slewing Rate (Variable as Above) | 0.3 to $1.3 \mathrm{~V} / \mu \mathrm{sec}$ | * | * | * | * | * |
| Input Offset Voltage |  |  |  |  |  |  |
| Initial, $+25^{\circ} \mathrm{C}$, min | 2.0 mV | 2.0 mV | 7.5 mV | 0.5 mV | 0.5 mV | 0.5 mV |
| Avg. vs. Temp, max | $15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $30 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $5.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $5.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $5.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ |
| Supply, min, $\mathrm{T}_{\mathrm{A}}$ min to max | 80 dB | 80 dB | 80 dB | 96 dB | 96 dB | 96 dB |
| Input Bias Current |  |  |  |  |  |  |
| Initial, $+25^{\circ} \mathrm{C}, \max$ | 2.0 nA | $2.0 n A$ | 7.0 nA | 2.0 nA | 2.0 nA | 7.0 nA |
| Input Difference Current |  |  |  |  |  |  |
| Initial, $+25^{\circ} \mathrm{C}, \max$ | 0.2 nA | 0.2 nA | 1.0 nA |  |  |  |
| Avg. vs. Temp, max | $2.5 \mathrm{pA} /{ }^{\circ} \mathrm{C}$ | $2.5 \mathrm{pA} /{ }^{\circ} \mathrm{C}$ | $10 \mathrm{pA} /{ }^{\circ} \mathrm{C}$ | $2.5 \mathrm{pA} /{ }^{\circ} \mathrm{C}$ | $2.5 \mathrm{pA} /{ }^{\circ} \mathrm{C}$ | $10 \mathrm{pA} /{ }^{\circ} \mathrm{C}$ |
| Input Voltage Range |  |  |  |  |  |  |
| Common Mode Voltage, min | $\pm 14 \mathrm{~V}$ | * | * | * | * |  |
| Common Mode Rejection, min | 85 dB | 85 dB | 80 dB | 96 dB | 96dB | 96 dB |
| Differential Input Current (Note 1) | $\pm 10 \mathrm{~mA}$ | * | * | * | * | * |
| Power Supply Range (VDC) | $\pm(2$ to 20$) \mathrm{V}$ | $\pm(2$ to 20$) \mathrm{V}$ | $\pm(2$ to 15$) \mathrm{V}$ | $\pm(2$ to 20$) \mathrm{V}$ | $\pm(2$ to 20$) \mathrm{V}$ | $\pm(2$ to 15$) \mathrm{V}$ |
| Rated Specification (VDC) | $\pm(5$ to 20$) \mathrm{V}$ | $\pm(5$ to 20$) \mathrm{V}$ | $\pm(5$ to 15$) \mathrm{V}$ | $\pm(5$ to 20$) \mathrm{V}$ | $\pm(5$ to 20$) \mathrm{V}$ | $\pm(5$ to 15$) \mathrm{V}$ |
| Quiescent Current, max | 0.6 mA | 0.6 mA | 0.3 mA typ | 0.6 mA | 0.6 mA | 0.3 mA typ |
| Temperature Range |  |  |  |  |  |  |
| Operating, Rated Specification Storage | $\begin{aligned} & -55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\ & -65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C} \end{aligned}$ | $-25^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C}$ | $0 \text { to }+70^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C}$ | $-25^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C}$ | $0 \text { to }+70^{\circ} \mathrm{C}$ |
| Price |  |  |  |  |  |  |
| (1-24) | \$18.75 | \$10.50 | \$3.00 | \$26.50 | \$21.00 | \$10.50 |
| (25-99) | \$15.00 | \$8.50 | \$2.35 | \$21.00 | \$16.75 | \$8.40 |
| (100-999) | \$12.50 | \$4.75 | \$1.75 | \$17.50 | \$14.00 | \$7.00 |

Note 1. Current must be limited to $\pm 10 \mathrm{~mA}$. Inputs have shunt-diode protection.
*Specifications same as for AD108.

# LOW INPUT CURRENT 709, 74I REPLACEMENTS AD801, AD502 



## GENERAL DESCRIPTION

The AD801 and AD502 are low input current replacements for the popular 709 and 741 operational amplifiers. Levels of $I_{b}$ below 4 nA and $\mathrm{I}_{\mathrm{OS}}$ below 1 nA are achieved by utilizing a Darlington input modification of the basic 709 and 741 designs, with no significant change in other operating parameters. Thus the user is afforded the opportunity of upgrading performance in his 709 and 741 sockets without resorting to a new amplifier design. The AD801 offers the 709's flexibility of external compensation; the AD502, like the 741, is internally compensated. Both devices are supplied in the TO-99 metal can package.

SPECIFICATION SUMMARY (Typical @ $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$ unless otherwise noted)

| Model | AD801A | AD801B | AD801S | AD502J | AD502K | AD502L |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Open Loop Gain |  |  |  |  |  |  |
| $\mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega, \mathrm{E}_{0}= \pm 10 \mathrm{~V}, \mathrm{~min}$ | 15,000 | * | * | 20,000 | ** | ** |
| Rated Output Voltage $\mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega$, min | $\pm 10 \mathrm{~V}$ | * | * | $\pm 10 \mathrm{~V}$ | ** | ** |
| Frequency Response |  |  |  |  |  |  |
| Unity Gain, Small Signal | 500 kHz (note 1) | * | * | 1 MHz | ** | ** |
| Full Power Response | 200 kHz (note 2) | * | * | 10 kHz | ** | ** |
| Slew Rate | $10 \mathrm{~V} / \mu \mathrm{sec}$ (note 2) | * | * | $0.5 \mathrm{~V} / \mu \mathrm{sec}$ | ** | ** |
| Input Offset Voltage |  |  |  |  |  |  |
| Over Temp Range ( $\mathrm{T}_{1}$ to $\mathrm{T}_{\mathrm{h}}$ ), max | $\pm 7.4 \mathrm{mV}$ | $\pm 5.6 \mathrm{mV}$ | $\pm 7.0 \mathrm{mV}$ | $\pm 7.5 \mathrm{mV}$ | $\pm 6 \mathrm{mV}$ | $\pm 6 \mathrm{mV}$ |
| Avg. vs Temp ( $\mathrm{T}_{1}$ to $+25^{\circ} \mathrm{C}$ to $\mathrm{T}_{\mathrm{h}}$ ), max | $\pm 40 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $\pm 10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $\pm 20 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $\pm 40 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $\pm 20 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $\pm 10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ |
| vs Supply Voltage, max | $\pm 200 \mu \mathrm{~V} / \mathrm{V}$ | * | * | $\pm 150 \mu \mathrm{~V} / \mathrm{V}$ | ** | ** |
| Input Bias Current |  |  |  |  |  |  |
| @ $+25^{\circ} \mathrm{C}, \max$ | 4 nA | * | * | 25 nA | 7 nA | 4nA |
| Over Temp Range ( $\mathrm{T}_{1}$ to $\mathrm{T}_{\mathrm{h}}$ ), max | 11 nA | * | 16 nA | 50 nA | 15 nA | 10 nA |
| Input Difference Current |  |  |  |  |  |  |
| @ $+25^{\circ} \mathrm{C}, \max$ | $\pm 2 \mathrm{nA}$ | $\pm 1 \mathrm{nA}$ | $\pm 2 \mathrm{nA}$ | $\pm 12 \mathrm{nA}$ | $\pm 4 \mathrm{nA}$ | $\pm 1 \mathrm{nA}$ |
| Over Temp Range ( $\mathrm{T}_{1}$ to $\mathrm{T}_{\mathrm{h}}$ ), max | $\pm 8 \mathrm{nA}$ | $\pm 2 \mathrm{nA}$ | $\pm 5 \mathrm{nA}$ | $\pm 24 \mathrm{nA}$ | $\pm 8 \mathrm{nA}$ | $\pm 2 \mathrm{nA}$ |
| Input Impedance . ${ }^{\text {a }}$ |  |  |  |  |  |  |
| Differential, min | $25 \mathrm{M} \Omega$ | * | * | $25 \mathrm{M} \Omega$ | ** | ** |
| Common Mode | $500 \mathrm{M} \Omega$ | * | * | $500 \mathrm{M} \Omega$ | ** | ** |
| Input Voltage Noise ${ }^{1}$ |  |  |  |  |  |  |
| 0.01 to $10 \mathrm{~Hz}, \mathrm{p}-\mathrm{p}$ | $100 \mu \mathrm{~V}$ | * | * | $100 \mu \mathrm{~V}$ | ** | ** |
| 10 Hz to 5 kHz , rms | $6 \mu \mathrm{~V}$ | * | * | $6 \mu \mathrm{~V}$ | ** | ** |
| Input Voltage Range |  |  |  |  |  |  |
| Common Mode Voltage, Min | $\pm 8 \mathrm{~V}$ | * | * | $\pm 10 \mathrm{~V}$ | ** | ** |
| Common Mode Rejection, Min | 65 dB | * | * | 70 dB | ** | ** |
| Max Safe Differential Voltage | $\pm 10 \mathrm{~V}$ | * | * | $\pm \mathrm{V}_{\text {S }}$ | ** | ** |
| Power Supply |  |  |  |  |  |  |
| Voltage, Rated Specification | $\pm(15$ to 16$) \mathrm{V}$ | * | * | $\pm(15$ to 16$) \mathrm{V}$ | ** | ** |
| Voltage, Derated Specification | $\pm(5$ to 18$) \mathrm{V}$ | * | * | $\pm(5$ to 18$) \mathrm{V}$ | ** | ** |
| Current, Quiescent, max | $\pm 6 \mathrm{~mA}$ | * | * | $\pm 2.8 \mathrm{~mA}$ | ** | ** |
| Temperature Range <br> Operating, Rated Specifications |  |  |  |  |  |  |
| Operating, Rated Specifications | $\begin{gathered} \mathrm{T}_{1}=-25^{\circ} \mathrm{C}, \\ \mathrm{~T}_{\mathrm{h}}=+85^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} \mathrm{T}_{1}=-25^{\circ} \mathrm{C}, \\ \mathrm{~T}_{\mathrm{h}}=+85^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} \mathrm{T}_{1}=-55^{\circ} \mathrm{C}, \\ \mathrm{~T}_{\mathrm{h}}=+125^{\circ} \mathrm{C} \end{gathered}$ | $\begin{gathered} \mathrm{T}_{1}=0, \\ \mathrm{~T}_{\mathrm{h}}=+70^{\circ} \mathrm{C} \end{gathered}$ | ** | ** |
| Operating, Derated Specifications | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | ${ }^{\text {h }}$ * | ${ }^{\text {h }}$ * | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | ** | ** |
| Storage | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ | * | * | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ | ** | ** |
| Mechanical <br> Case Style - Pin Configuration | TO-99 | * | * | TO-99 | ** | ** |
| Price |  |  |  |  |  |  |
| 1-24 | \$16.10 | \$21.85 | \$26.45 | \$5.15 | \$10.35 | \$21.85 |
| 25-99 | \$13.80 | \$17.60 | \$23.00 | \$4.15 | \$8.30 | \$17.25 |
| 100-999 | \$11.20 | \$16.10 | \$17.25 | \$3.45 | \$6.90 | \$14.40 |

NOTES:

1. $\mathrm{C}_{1}=5000 \mathrm{pF}, \mathrm{R}_{1}=1.5 \mathrm{k} \Omega, \mathrm{C}_{2}=200 \mathrm{pF}\left(\mathrm{A}_{\mathrm{CL}}=1\right) . \quad *$ Specifications same as for AD801A.
2. $\mathrm{C}_{1}=10 \mathrm{pF}, \mathrm{R}_{1}=0 \Omega, \mathrm{C}_{2}=3 \mathrm{pF}\left(\mathrm{A}_{\mathrm{CL}}=1000\right) . \quad * *$ Specifications same as for AD502J.

# HIGH OUTPUT CURRENT OPERATIONAL <br> AMPLIFIER AD512 

## GENERAL DESCRIPTION

The AD512K and AD512S are monolithic operational amplifiers specifically designed for high output current capability. High efficiency output transistors, thermally balanced chip design and precise short circuit current control insure against gain degradation at high current levels and temperature extremes. The AD 512 K specifies a minimum gain of 20,000 swinging $\pm 12$ volts into a $1 \mathrm{k} \Omega$ load from 0 to $+70^{\circ} \mathrm{C}$; the AD512S specifies a minimum gain of 15,000 swinging $\pm 10$ volts into a $1 \mathrm{k} \Omega$ load from $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$. In addition, the devices offer excellent input characteristics and common mode and power supply rejection ratios, and are internally compensated. Both are available in the TO-99 package; the AD512K for 0 to $+70^{\circ} \mathrm{C}$ temperature range operation, and the AD512S for operation from $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$.


ELECTRICAL SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ and $\pm 15 \mathrm{VDC}$, unless otherwise noted.)

| Model | AD512K | AD512S |
| :---: | :---: | :---: |
| Open Loop Gain |  |  |
| $\mathrm{V}_{\text {OS }}= \pm 10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}} \geqslant 1 \mathrm{k} \Omega$ | 50,000 min (200,000 typ) | * |
| @ $\mathrm{T}_{\mathrm{A}}=\min$ to $\max$ | 25,000 min | * |
| Output Characteristics |  |  |
| Voltage @ $\mathrm{R}_{\mathrm{L}} \geqslant 1 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=\min$ to max | $\pm 10 \mathrm{~V}$ min $( \pm 13 \mathrm{~V}$ typ) | * |
| Short Circuit Current | 25 mA | * |
| Frequency Response |  |  |
| Unity Gain, Small Signal | 1 MHz | * |
| Full Power Response | 10 kHz | , |
| Slew Rate, Unity Gain | $0.5 \mathrm{~V} / \mu \mathrm{sec}$ | * |
| Input Offset Voltage |  |  |
| Initial, $\mathrm{R}_{\mathrm{S}} \leqslant 10 \mathrm{k} \Omega$ (Adjustable to Zero) | 3 mV max ( 1 mV typ) | * |
| $\mathrm{T}_{\text {min }}$ to $\mathrm{T}_{\text {max }}$ | 5 mV max |  |
| Avg vs Temperature (Untrimmed) | $20 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max | $25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max |
| vs Supply, $\mathrm{T}_{\mathrm{A}}=\min$ to $\max$ | $100 \mu \mathrm{~V} / \mathrm{V} \max (30 \mu \mathrm{~V} / \mathrm{V}$ typ) | * |
| Input Offset Current |  |  |
| Initial | $50 \mathrm{nA} \max (5 \mathrm{nA} \mathrm{typ})$ | * |
| $\mathrm{T}_{\text {min }}$ to $\mathrm{T}_{\text {max }}$ | 100 nA max | 150nA max |
| Input Bias Current |  |  |
| Initial | 200nA max (40nA typ) | $200 n A \max (40 n A$ typ $)$ |
| $\mathrm{T}_{\text {min }}$ to $\mathrm{T}_{\text {max }}$ | 400nA max | $600 n A \max$ |
| Input Impedance Differential | $1 \mathrm{M} \Omega$ | * |
| Input Voltage Range (Note 1) |  |  |
| Differential, Max Safe | $\pm 30 \mathrm{~V}$ | * |
| Common Mode, Max Safe | $\pm 15 \mathrm{~V}$ | * |
| Common Mode Rejection |  |  |
| $\mathrm{R}_{\mathrm{S}} \leqslant 10 \mathrm{k} \Omega, \mathrm{T}_{\text {min }}$ to $\mathrm{T}_{\text {max }}$, |  |  |
| $\mathrm{V}_{\text {IN }}= \pm 12 \mathrm{~V}$ | 80 dB min ( 90 dB typ) | * |
| Power Supply |  |  |
| Rated Performance | $\pm 15 \mathrm{~V}$ | * |
| Operating | $\pm(5$ to 18$) \mathrm{V}$ | $\pm(5$ to 22$) \mathrm{V}$ |
| Current, Quiescent | 3.3 mA max ( 2.0 mA typ) | * |
| Temperature Range |  |  |
| Operating, Rated Performance | 0 to $+70^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| Storage | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ | * |
| Price |  |  |
| (1-24) | \$6.90 | \$10.35 |
| (25-99) | \$5.50 | \$8.30 |
| (100-999) | \$4.60 | \$6.90 |

Note 1: For supply voltages less than $\pm 15 \mathrm{~V}$, the absolute maximum input voltage is equal to the supply voltage.
*Same specifications as AD512K.

# LOW COST, GENERAL PURPOSE OP AMPS <br> AD74I, ADIOIA 

PIN CONFIGURATIONS

## GENERAL DESCRIPTION

The AD741 and AD101A amplifier series are Analog Devices' versions of the two most popular IC op amps. They are designed for general purpose use where medium performance is acceptable and economy is mandatory. Both offer full short circuit protection, external offset voltage nulling, high common mode range, and the absence of latch-up. The AD741 and AD741C emphasize simplicity of use, requiring no external compensation. The AD101A, AD201A and AD301A provide somewhat higher DC accuracy and require external compensation, thus affording the user the opportunity to fit the amplifier's dynamic characteristics to its specific application. The AD741 is available in the TO-99 metal can package for operation from $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$; the AD741C is packaged in both the TO-99 and plastic mini-DIP DIL and operates from 0 to $+70^{\circ} \mathrm{C}$. The AD101A is specified in both the TO-99 and ceramic flat packages from $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$; the AD201A is available in the TO-99, mini-DIP and flat packages for $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ and 0 to $+70^{\circ} \mathrm{C}$ operation; and the AD301A is packaged in the TO-99 and mini-DIP, and operates from 0 to $+70^{\circ} \mathrm{C}$.
Top View

AD101A



TO-99


SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ and $\pm 15$ VDC power supply unless otherwise noted.)

| Model | AD741 | AD741C | AD101A | AD201A | AD301A |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Open Loop Gain |  |  |  |  |  |
| DC Rated Load, V/V Min | 50,000 | 20,000 | 50,000 | 50,000 | 25,000 |
| Rated Output, Min, $\mathrm{R}_{\mathrm{L}} \geqslant 2 \mathrm{k} \Omega$ | $\pm 10 \mathrm{~V}$ | * | * | * | * |
| Frequency Response |  |  |  |  |  |
| Unity Gain, Small Signal | 1.0 MHz | * | 1.0 to 8.0 MHz | 1.0 to 8.0 MHz | 1.0 to 8.0 MHz |
| Slewing Rate | $0.5 \mathrm{~V} / \mu \mathrm{s}$ | * | 0.5 to $10 \mathrm{~V} / \mathrm{\mu s}$ | 0.5 to $10 \mathrm{~V} / \mu \mathrm{s}$ | 0.5 to $10 \mathrm{~V} / \mathrm{\mu s}$ |
| Input Offset Voltage |  |  |  |  |  |
| Initial, $+25^{\circ} \mathrm{C}$ (Adj. to Zero) Min | 5.0 mV | 6.0 mV | 2.0 mV | 2.0 mV | 7.5 mV |
| Avg vs Temperature, Max | - | - | $15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $30 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ |
| vs Supply Voltage | $30 \mu \mathrm{~V} / \mathrm{V}$ | * | 96 dB | 96 dB | 96 dB |
| Input Bias Current |  |  |  |  |  |
| Input Difference Current |  |  |  |  |  |
| Initial, $+25^{\circ} \mathrm{C}, \mathrm{Max}$ | 200nA | * | 10 nA | 10 nA | 50 nA |
| Avg vs Temperature, Max | - | - | $0.2 \mathrm{nA} /{ }^{\circ} \mathrm{C}$ | $0.2 \mathrm{nA} /{ }^{\circ} \mathrm{C}$ | $0.6 \mathrm{nA} /{ }^{\circ} \mathrm{C}$ |
| Input Impedance |  |  |  |  |  |
| Differential | $2.0 \mathrm{M} \Omega$ | * | $4.0 \mathrm{M} \Omega$ | $4.0 \mathrm{M} \Omega$ | $2.0 \mathrm{M} \Omega$ |
| Input Voltage Range |  |  |  |  |  |
| Common Mode Voltage, Min | $\pm 12 \mathrm{~V}$ | * | * | * | * |
| Common Mode Rejection, Min | 70 dB | * | 80 dB | 80 dB | 70 dB |
| Differential Voltage | $\pm 30 \mathrm{~V}$ | * | * | * | * |
| Power Supply Range (VDC) | $\pm(5$ to 22$) \mathrm{V}$ | $\pm(5$ to 18$) \mathrm{V}$ | $\pm(5$ to 22$) \mathrm{V}$ | $\pm(5$ to 22$) \mathrm{V}$ | $\pm(5$ to 18$) \mathrm{V}$ |
| Rated Specification (VDC) | $\pm 15 \mathrm{~V}$ | * | * | * | * |
| Quiescent Current, Max | 2.8 mA | * | 3.0 mA | 3.0 mA | 3.0 mA |
| Temperature Range Operating, Rated Specification | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 0 to $+70^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}{ }^{1}$ | 0 to $+70^{\circ} \mathrm{C}$ |
| Package Outline | TO-99 | TO-99, mini-DIP | TO-99, flat pack | TO-99, flat pack, mini-DIP | TO-99, mini-DIP |
| Price ${ }^{2}$ |  |  |  |  |  |
| (1-24) | \$3.00 | \$1.50 | \$4.50 | \$3.00 | \$1.50 |
| (25-99) | \$2.40 | \$1.20 | \$3.60 | \$2.40 | \$1.20 |
| (100-999) | \$2.00 | \$1.00 | \$2.25 | \$1.75 | \$1.00 |

${ }^{1} \mathrm{O}$ to $+70^{\circ} \mathrm{C}$ in mini-DIP package.
${ }^{2}$ TO-99 package, and mini-DIP package (where listed).
*Same specifications as AD741;

# MULTIPLIER/DIVIDER COMPUTATION CIRCUITS AD530, AD531, AD532, AD533 

## GENERAL DESCRIPTION

Models AD5 30, AD5 31, AD5 32 and AD5 33 utilize the Gilbert linearized transconductance technique to perform the basic functions of multiplying, dividing, squaring and square rooting. In addition to being most useful operations in themselves, these functions are excellently applied in circuitry for modulation and demodulation, frequency discrimination, phase detection, automatic gain control, vector computation, function generation, and true RMS-to-DC conversion.
Each multiplier offers the user specific choices in the areas of performance, flexibility, ease of use, and cost, and should be carefully evaluated to ascertain which is best suited for the particular application. Certain performance features are common to all models, and are described here. The differences are covered in the individual product descriptions.
Since all the multipliers operate over four quadrants, there are no restrictions as to signal polarity. The guaranteed maximum error specifications include the contributions from all sources ... feedthrough, offset, scale factor, and nonlinearity . . in the four quadrants. Further, in addition to the transconductance element, the design of the four models incorporates a stable reference and output amplifier on the monolithic chip.

AD530: $\mathrm{V}_{\mathrm{x}} \cdot \mathrm{V}_{\mathbf{y}} / \mathbf{1 0} ; \mathbf{2 \%}, \mathbf{1 \%}, \mathbf{0 . 5 \%}$ MAX ERRORS
The AD530 multiplies in four quadrants with a transfer function of XY/10, divides in two quadrants with a $10 \mathrm{Z} / \mathrm{X}$ transfer function, and square roots in one quadrant with a transfer function of $-\sqrt{10 Z}$. Due to its design completeness, which includes the output amplifier, frequency compensation, level shifting, and scaling on the chip, the AD530's complement of external components is confined to feedthrough, output zero and gain adjusting trim pots.
The AD530J, AD530K, and AD530L operate from 0 to $+70^{\circ} \mathrm{C}$ and are specified for maximum full scale multiplying errors of $\pm 2 \%, \pm 1 \%$, and $\pm 0.5 \%$, respectively, at $+25^{\circ} \mathrm{C}$. The AD530S, designed for wide temperature range requirements, is guaranteed for a maximum multiplying error of $\pm 1 \%$, at $+25^{\circ} \mathrm{C}$, and is $100 \%$ temperature tested to less than $\pm 3 \%$ error from $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$. The high accuracy AD 530 L is also $100 \%$ tested to guarantee a maximum error of $\pm 1.5 \%$ from 0 to $+70^{\circ} \mathrm{C}$. These low maximum errors over temperature are indicative of the excellent temperature stability of the AD5 30; performance that is unmatched by any IC multipliers except those supplied by Analog Devices.

## AD531: $\mathbf{V}_{\mathbf{x}} \cdot \mathbf{V}_{\mathbf{y}} / \mathbf{V}_{\mathbf{z}} ; \mathbf{2 \%}, \mathbf{1 \%}, \mathbf{0 . 5 \%}$ MAX ERRORS

The AD5 31 is the first monolithic multiplier/computation circuit to provide the true transfer function $\mathrm{V}_{\mathrm{x}} \cdot \mathrm{V}_{\mathrm{y}} / \mathrm{kIz}$ without the need for an external level shifting op amp at the output. Significant flexibility of operation is achieved by means of the variable scale factor kIz , which can be set by an external resistor or varied dynamically by an externally derived reference current to obtain the overall transfer function $\mathrm{V}_{\mathbf{x}} \cdot \mathrm{V}_{\mathbf{y}} / \mathrm{V}_{\mathrm{z}}$. This provision for the direct computation of three variables greatly simplifies the design of such complex circuits as the true RMS-to-DC converter, AGC, vector computation, and absolute value. Further, multipliers less flexible than the AD5 31
must put the multiplying element in the feedback of an op amp to obtain division, often with significant sacrifice in accuracy and bandwidth.
The unique features of the AD5 31 include a differential $\mathrm{V}_{\mathbf{x}}$ input with 75 dB of CMR, an internally derived stable reference for use in fixed scale applications, and a sense feedback terminal for simple load sensing or special applications. The circuit's complement of required external components is limited to feedthrough and output zero adjusting trim pots, and passive or active adjustment of the scaling current $\mathrm{I}_{\mathrm{z}}$.
The AD5 31J, AD531K, and AD531L operate from 0 to $+70^{\circ} \mathrm{C}$ and have maximum multiplying errors of $\pm 2 \%, \pm 1 \%$, and $\pm 0.5 \%$ ot full scale respectively, at $+25^{\circ} \mathrm{C}$. The AD531L is also guaranteed to have less than $\pm 1.5 \%$ error from 0 to $+70^{\circ} \mathrm{C}$. The AD5 31S is guaranteed for a maximum error of $\pm 1 \%$ at $+25^{\circ} \mathrm{C}$, and is also 100 tested to guarantee a maximum error of $\pm 3 \%$ from $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$.

## AD532: $\left(\mathrm{V}_{\mathrm{x}_{1}}-\mathrm{V}_{\mathrm{x}_{2}}\right)\left(\mathrm{V}_{\mathrm{y}_{1}}-\mathrm{V}_{\mathrm{y}_{2}}\right) / \mathbf{1 0} ; \mathbf{2 \%}, \mathbf{1 \%}$; INTERNALLY TRIMMED

The AD5 32 is the first totally self-contained monolithic multiplier/divider. Because it needs no external components for accuracy trimming or output level shifting, the AD5 32 provides design engineers who require analog multiplication [ $\left(\mathrm{V}_{\mathrm{x}_{1}}-\mathrm{V}_{\mathrm{x}_{2}}\right)\left(\mathrm{V}_{\mathrm{y}_{1}}-\mathrm{V}_{\mathrm{y}_{2}}\right) / 10$ in four quadrants] , division [10Z/( $\left.\mathrm{X}_{1}-\mathrm{X}_{2}\right)$ in two quadrants], square rooting $( \pm \sqrt{10 \mathrm{Z}}$ in one quadrant), and squaring, with the best in-board combination of low cost, small size, and simplicity of use. It can be inserted directly into the circuit board - much as an internally compensated IC op amp - thus saving the user the time and expense of providing external trimming resistors and of performing the relatively sophisticated adjustment procedure.
In addition to the benefits of internal trimming, the AD5 32, which can be used in the same socket as the AD5 30 by omitting the external trim connections, offers significant versatility in new applications by providing differential X and Y inputs (typical 75 dB CMR), and an output null terminal which permits an independent setting of the output offset.
The AD5 32J and AD532K operate from 0 to $+70^{\circ} \mathrm{C}$ and have maximum multiplying errors of $\pm 2 \%$ and $\pm 1 \%$ of full scale at $+25^{\circ} \mathrm{C}$. The AD532S is guaranteed for a maximum error of $\pm 1 \%$ at $+25^{\circ} \mathrm{C}$, and is $100 \%$ temperature tested to guarantee a maximum error of $\pm 4 \%$ from $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$.

## AD533: $\mathrm{V}_{\mathrm{x}} \cdot \mathrm{V}_{\mathrm{y}} / \mathbf{1 0} ; \mathbf{2 \%}, \mathbf{1 \%}, \mathbf{0 . 5 \%}$ MAX ERRORS

Where cost is a factor, the AD533 offers the user a complete multiplier/divider with output amplifier, frequency compensation, level shifting and scaling on a monolithic chip - at a price below that of any IC multiplier on the market ( $\$ 5.95$ in hundreds). Like its predecessor, the AD530, the AD533 multiplies in 4 quadrants, divides in 2 quadrants and square roots in one quadrant. Three levels of accuracy are available over the commercial temperature ( 0 to $+70^{\circ} \mathrm{C}$ ) and one specified over the full MIL temperature range $\left(-55^{\circ} \mathrm{C}\right.$ to $+125^{\circ} \mathrm{C}$ ).

AD530 SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$, externally trimmed and $\pm 15$ VDC. unless otherwise specified )

| PARAMETER | AD530J (530K)(530L)(530S) |
| :---: | :---: |
| MULTIPLIER SPECIFICATIONS |  |
| Transfer Function | $\mathrm{V}_{\mathrm{Xin}} \cdot \mathrm{V}_{\mathrm{y}_{\text {in }} / 10 \text { volts }}$ |
| Total Error (\% FS @ $+25^{\circ} \mathrm{C}$ ) |  |
| $\left(\mathrm{T}_{\mathrm{A}}=\min\right.$ to $\max$ ) | $2.5 \%(1.5 \%)(1.5 \% \max )(3.0 \% \max )$ |
| vs. Temperature |  |
| $\left(\mathrm{T}_{\mathrm{A}}=\min\right.$ to $\left.\max \right)$ | 0.04(0.03)(0.01)(0.02 max) \% $/{ }^{\circ} \mathrm{C}$ |
| Nonlinearity |  |
| X.input | 0.8\%(0.5\%)(0.3\%)(0.5\%) |
| Y input | 0.3\%(0.2\%)(0.2\%)(0.2\%) |
| Feedthrough |  |
| X input | 150(80)(40)(80)mV max |
| Y input | 100(60)(30)(60)mV max |
| DIVIDER SPECIFICATIONS* |  |
| Transfer Function | $10 \cdot \mathrm{~V}_{\mathrm{z}_{\text {in }}} / \mathrm{V}_{\mathrm{x}_{\text {in }}}$ volts |
| Total Error (\% FS) | 1.0\%(0.5\%)(0.2\%)(0.5\%) |
| SQUARER SPECIFICATIONS |  |
| Transfer Function | $\mathrm{V}_{\mathrm{xin}}{ }^{2 / 10}$ |
| Total Error (\% FS) | 0.8\%(0.4\%)(0.2\%)(0.4\%) |


| SQUARE ROOTER SPECIFICATIONS |  |
| :---: | :--- |
| Transfer Function | $-\sqrt{10 \mathrm{~V}_{\mathrm{Z}_{\mathrm{in}}}{ }^{*}}$ |
| Total Error (\% FS) | $0.8 \%(0.4 \%)(0.2 \%)(0.4 \%)$ |

INPUT SPECIFICATIONS
Input Resistance

| X input | $10 \mathrm{M} \Omega$ |
| :--- | :--- |
| Y input |  |
| Z input* | $6 \mathrm{M} \Omega$ |
| nput Bias Current | $36 \mathrm{k} \Omega$ |
| $\mathrm{X}, \mathrm{Y}$ inputs |  |
| Z input* | $3.0(4.0 \max )(2.0 \max )(4.0 \max ) \mu \mathrm{A}$ |
|  | $10(15 \max )(15 \max )(15 \max ) \mu \mathrm{A}$ |

Input Voltage (for rated accuracy)
$\mathrm{V}_{\mathrm{x}}, \mathrm{V}_{\mathrm{y}}, \mathrm{V}_{\mathrm{z}}$
( $\mathrm{T}_{\mathrm{A}}=\min$ to max) $\quad \pm 10 \mathrm{~V}$
Null Input Voltage (required to trim)
$\mathrm{V}_{\mathrm{xo}}, \mathrm{V}_{\mathrm{yo}}, \mathrm{V}_{\mathrm{zo}} \quad \pm 15( \pm 10)( \pm 10)( \pm 10) \mathrm{V} \max$
DYNAMIC SPECIFICATIONS
Small Signal, Unity Gain $\quad 1.0 \mathrm{MHz}$
Full Power Bandwidth 750 kHz
Slew Rate $\quad 45 \mathrm{~V} / \mu \mathrm{sec}$
Small Signal Amplitude Error
Small Signal 1\% Vector Error
Settling Time
Overload Recovery
$1 \%$ at 75 kHz

Output Voltage Swing $\left(\mathrm{T}_{\mathrm{A}}=\min\right.$ to $\left.\max \right)$
Output Offset Voltage vs. Temperature
$0.7(0.7)(1.0 \max )(2.0 \max ) \mathrm{mV} /{ }^{\circ} \mathrm{C}$

*With Z (feedback) terminal used as an input terminal.
5 kHz
$1 \mu \mathrm{sec}$ to $2 \%$
$2 \mu \mathrm{sec}$ to $2 \%$

## CIRCUIT FUNCTIONS



SQUARER


SQUARE
ROOTER


PIN CONFIGURATIONS


Top View



AD531 SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$, externally trimmed and $\pm 15$ VDC, unless otherwise specified.)

| PARAMETER | AD531J (531K)(531L)(531S) |
| :---: | :---: |
| PERFORMANCE SPECIFICATIONS |  |
| Transfer Function | $\mathrm{V}_{\mathrm{x}} \cdot \mathrm{V}_{\mathrm{y}} / \mathrm{kIz}$ |
| Total Error (\% FS, kIz $=10 \mathrm{~V}$ ) |  |
| $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | 2.0\%(1.0\%)(0.5\%)(1.0\%) max |
| $\mathrm{T}_{\mathrm{A}}=\min$ to $\max$ | 2.5\%(1.5\%)(1.5\% max $)(3.0 \% \max )$ |
| Terminal Limits |  |
| Input Voltage | $-10 \mathrm{~V} \leqslant \mathrm{~V}_{\mathrm{x}} \cdot \mathrm{V}_{\mathrm{y}} \leqslant+10 \mathrm{~V}$ |
| Reference Cursent | $0<\mathrm{kIz} \leqslant+10 \mathrm{~V}, \mathrm{~V}_{\mathbf{x}} / \mathrm{kIz}<2.5$ |
| Nonlinearity |  |
| X input | 0.8(0.5)(0.3)(0.5)\% |
| Y input | 0.3(0.2)(0.2)(0.2)\% |
| Z input ( $0.1<\mathrm{klz}<10 \mathrm{~V}$ ) | 0.5(0.5)(0.5)(0.5)\% |
| Feedthrough |  |
| X input | 150(80)(40)(80)mV max |
| Y input | $100(60)(30)(60) \mathrm{mV}$ max |
| Z input ( $1 \leqslant \mathrm{kIz} \leqslant 10 \mathrm{~V}$ ) | 50(50)(50)(50)mV typ |
| INPUT SPECIFICATIONS |  |
| X terminal |  |
| Differential Input |  |
| Resistance | $10 \mathrm{M} \Omega$ |
| Common Mode |  |
| Input Resistance | $80 \mathrm{M} \Omega$ |
| Input Bias Current | $8 \mu \mathrm{~A} \max$ |
| Common Mode |  |
| Voltage Range | $\pm 10 \mathrm{~V}$ min |
| CMRR | 60 dB |
| Y terminal |  |
| Input Resistance | $6 \mathrm{M} \Omega$ |
| Input Bias Current | $8 \mu \mathrm{~A}$ max |
| Z terminal |  |
| Reference Current (for $\mathrm{kIz}=10 \mathrm{~V}$ ) | $+320 \mu \mathrm{~A} \leqslant \mathrm{I}_{\mathrm{Z}} \leqslant+490 \mu \mathrm{~A}$ |
| Sense Terminal |  |
| Input Resistance | $36 \mathrm{k} \Omega$ |
| Input Bias Current | $15 \mu \mathrm{~A}$ max |
| Null Input Voltages |  |
| $\mathrm{V}_{\mathrm{yo}}, \mathrm{V}_{\text {os }}$ | $\pm 15( \pm 10)( \pm 10)( \pm 10) \mathrm{V}$ max |
| $\mathrm{V}_{\text {xo }}$ | $+10 \mathrm{~V}<\mathrm{V}_{\mathrm{xo}}<+15 \mathrm{~V}$ |
| DYNAMIC SPECIFICATIONS |  |
| Small Signal, Unity Gain | 1.0 MHz |
| Full Power Bandwidth | 750 kHz |
| Slew Rate | $45 \mathrm{~V} / \mu \mathrm{sec}$ |
| Small Signal Amplitude |  |
| Error | $1 \%$ at 75 kHz |
| Small Signal 1\% Vector |  |
| Error | 5 kHz |
| Settling Time | $1 \mu \mathrm{sec}$ to $2 \%$ |
| Overload Recovery | $2 \mu \mathrm{sec}$ to $2 \%$ |
| OUTPUT AMPLIFIER SPECIFICATIONS |  |
| Output Voltage Swing |  |
| Output Offset Voltage vs. Temperature | $0.7(0.7)(1.0 \max )(2.0 \mathrm{max}) \mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| POWER SUPPLY SPECIFICATIONS |  |
| Supply Voltage |  |
| Rated | $\pm 15 \mathrm{~V}$ |
| Operating | $\begin{aligned} & \pm 15 \text { to } 18)(10 \text { to } 18)(10 \text { to } 18) \\ & \quad(10 \text { to } 22) \mathrm{V} \end{aligned}$ |
| Supply Current, quiescent | $\pm 6 \mathrm{~mA}$ max |
| Power Supply Variation |  |
| (includes effects of recommended null pots) |  |
| Multiplier Accuracy | $\pm 0.5 \% / \%$ |
| Output Offset | $\pm 10 \mathrm{mV} / \%$ |
| Scale Factor | $\pm 0.1 \% / \%$ |
| Feedthrough | $\pm 10 \mathrm{mV} / \%$ |
| PRICE (1-24) | \$11.95(\$17.95)(\$45.00)(\$48.50) |

## CIRCUIT FUNCTIONS

MULTIPLIER, DIVIDER (DYNAMIC SCALE FACTOR CONNECTION)


MULTIPLIER, SQUARER (FIXED SCALE FACTOR CONNECTION)


TRUE RMS-TO-DC CONVERTER


PIN CONFIGURATION
Top View


D SUFFIX

AD532 SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ and $\pm 15 \mathrm{VDC}$, unless otherwise specified.)

## PARAMETER <br> AD532J (AD532K)(AD532S)

| MULTIPLIER SPECIFICATIONS Transfer Function | $\left(\mathrm{V}_{\mathrm{x}_{1}}-\mathrm{V}_{\mathrm{x}_{2}}\right)\left(\mathrm{V}_{\mathrm{y}_{1}}-\mathrm{V}_{\mathrm{y}_{2}}\right) / 10 \mathrm{~V}$ |
| :---: | :---: |
| Total Error (\% FS @ $+25^{\circ} \mathrm{C}$ ) | 2.0\%(1.0\%)(1.0\%) max |
| $\left(\mathrm{T}_{\mathrm{A}}=\min\right.$ to max) | 2.5\%(1.5\%)(4.0\% max) |
| vs. Temperature |  |
| $\left(\mathrm{T}_{\mathrm{A}}=\right.$ min to max) | $0.04(0.03)(0.02 \mathrm{max}) \%{ }^{\circ} \mathrm{C}$ |
| Nonlinearity |  |
| X input | 0.8\%(0.5\%)(0.5\%) |
| Y input | 0.3\%(0.2\%)(0.2\%) |
| Feedthrough |  |
| X input | 150(80)(80)mV max |
| Y input | 100(60)(60)mV max |
| DIVIDER SPECIFICATIONS* |  |
| Transfer Function | $10 \mathrm{Z} /\left(\mathrm{X}_{1}-\mathrm{X}_{2}\right)$ |
| Total Error (\% FS) | 2.0\%(1\%)(1\%) |
| SQUARER SPECIFICATIONS <br> Transfer Function | $\pm \mathrm{X}^{2} / 10$ |
| Total Error (\% FS) | 0.8\%(0.4\%)(0.4\%) |
| SQUARE ROOTER SPECIFICATIONS <br> Transfer Function | $-\sqrt{10 \mathrm{~V}_{\mathrm{z}_{\text {in }}}}{ }^{*}$ |
| Total Error (\% FS) | 0.8\%(0.4\%)(0.4\%) |
| INPUT SPECIFICATIONS |  |
| CMRR $\mathrm{X}_{\text {in }}, \mathrm{Y}_{\text {in }}= \pm 10 \mathrm{~V}$ | 40(60)(60) dB min |
| Input Resistance |  |
| X input | $10 \mathrm{M} \Omega$ |
| Y input | $10 \mathrm{M} \Omega$ |
| Z input* | $36 \mathrm{k} \Omega$ |
| Input Bias Current |  |
| $\mathrm{X}, \mathrm{Y}$ inputs | $3.0(4.0 \max )(4.0 \max ) \mu \mathrm{A}$ |
| Z input* | $10(15 \mathrm{max})(15 \mathrm{max}) \mu \mathrm{A}$ |
| Input Voltage (for rated accuracy) |  |
| $\mathrm{V}_{\mathrm{x}}, \mathrm{V}_{\mathbf{y}}, \mathrm{V}_{\mathrm{z}}$ |  |
| ( $\mathrm{T}_{\mathrm{A}}=\min$ to max) | $\pm 10 \mathrm{~V}$ |
| Null Input Voltage (required to trim) |  |
| Vos | $\pm 15 \mathrm{~V}$ max |
| DYNAMIC SPECIFICATIONS |  |
| Small Signal, Unity Gain | 1.0 MHz |
| Full Power Bandwidth | 750 kHz |
| Slew Rate | $45 \mathrm{~V} / \mu \mathrm{sec}$ |
| Small Signal Amplitude Error | $1 \%$ at 75 kHz |
| Small Signal 1\% Vector Error | 5 kHz |
| Settling Time | $1 \mu \mathrm{sec}$ to $2 \%$ |


| OUTPUT AMPLIFIER SPECIFICATIONS |  |
| :---: | :---: |
| Output Voltage Swing |  |
| ( $\mathrm{T}_{\mathrm{A}}=\min$ to max) | $\pm 10 \mathrm{~V} \mathrm{~min}$ @ 5 mA |
| Output Offset Voltage** | $\pm 50( \pm 20)( \pm 20) \mathrm{mV}$ max |
| vs Temperature | $0.7(0.7)(2.0 \mathrm{max}) \mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| POWER SUPPLY SPECIFICATIONS |  |
| Supply Voltage |  |
| Rated | $\pm 15 \mathrm{~V}$ |
| Operating | $\pm 15$ to 18(10 to 18)(10 to 22)V |
| Supply Current, Quiescent | $\pm 6 \mathrm{~mA}$ max |
| Power Supply Variation |  |
| Multiplier Accuracy | $\pm 0.5( \pm 0.5 \mathrm{max})( \pm 0.5 \mathrm{max}) \% / \%$ |
| Output Offset | $\pm 10( \pm 10 \mathrm{max})( \pm 10 \mathrm{max}) \mathrm{mV} / \%$ |
| Scale Factor | $\pm 0.1( \pm 0.1)( \pm 0.1) \% / \%$ |
| Feedthrough | $\pm 10( \pm 10 \mathrm{max})( \pm 10 \mathrm{max}) \mathrm{mV} / \%$ - |
| PRICE |  |
| (1-24) | \$26.00(\$36.00)(\$49.00) |

*With Z (feedback) terminal used as an input terminal.
**Trimmable to zero.

## CIRCUIT FUNCTIONS

MULTIPLY


DIFFERENCE OF SQUARES



PIN CONFIGURATIONS
Top View
H SUFFIX


TO-100


DIVIDE

D SUFFIX
TO-116


AD533 SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$, externally trimmed and $\pm 15$ VDC, unless otherwise specified.)
PARAMETER
AD533J (533K)(533L)(533S)
MULTIPLIER SPECIFICATIONS
Transfer Function $\quad \mathrm{V}_{\mathrm{x}_{\text {in }}} \cdot \mathrm{V}_{\mathrm{y}_{\text {in }} / 10 \text { volts }}$
Total Error (\% FS @ $+25^{\circ} \mathrm{C}$ ) $\quad 2.0 \%(1.0 \%)(0.5 \%)(1.0 \%) \max$
$\left(\mathrm{T}_{\mathrm{A}}=\min\right.$ to $\left.\max \right) \quad 3.0 \%(2.0 \%)(1.0 \%)(1.5 \%)$
vs. Temperature
$\left(\mathrm{T}_{\mathrm{A}}=\min\right.$ to $\left.\max \right) \quad 0.04(0.03)(0.01)(0.01 \max ) \% /{ }^{\circ} \mathrm{C}$
Nonlinearity
X input $\quad 0.8 \%(0.5 \%)(0.5 \%)(0.5 \%)$
$Y$ input $\quad 0.3 \%(0.2 \%)(0.2 \%)(0.2 \%)$
Feedthrough
$X$ input $\quad 150(100)(50)(100) \mathrm{mV}$ max
Y input $\quad 200(100)(50)(100) \mathrm{mV} \max$
DIVIDER SPECIFICATIONS*
Transfer Function $\quad 10 \cdot \mathrm{~V}_{\mathrm{Z}_{\text {in }}} / \mathrm{V}_{\mathbf{x}_{\text {in }}}$ volts

| Total Error (\% FS) | $1.0 \%(0.5 \%)(0.2 \%)(0.5 \%)$ |
| :--- | :--- |
| SQUARER SPECIFICATIONS |  |
| Transfer Function | $\mathrm{V}_{\mathrm{xin}_{\mathrm{in}}}{ }^{2} / 10$ |
| Total Error (\% FS) | $0.8 \%(0.4 \%)(0.2 \%)(0.4 \%)$ |


| SQUARE ROOTER SPECIFICATIONS |  |
| :--- | :--- |
| Transfer Function | $-\sqrt{10 \mathrm{~V}_{\mathrm{Z}_{\mathrm{in}}}{ }^{*}}$ |
| Total Error (\% FS) | $0.8 \%(0.4 \%)(0.2 \%)(0.4 \%)$ |

INPUT SPECIFICATIONS
Input Resistance

| X input | $10 \mathrm{M} \Omega$ |
| :--- | :--- |
| Y input | $6 \mathrm{M} \Omega$ |
| Z input |  |
| nput Bias Current | $36 \mathrm{k} \Omega$ |
| $\mathrm{X}, \mathrm{Y}$ inputs <br> Z input* | $3.0(7.5 \mathrm{max})(5.0 \mathrm{max})(7.5 \mathrm{max}) \mu \mathrm{A}$ |
|  | $25 \mu \mathrm{~A}$ |

    Input Voltage (for rated accuracy)
        \(V_{x}, V_{y}, V_{z}\)
        \(\left(\mathrm{T}_{\mathrm{A}}=\min\right.\) to max) \(\quad \pm 10 \mathrm{~V}\)
    Null Input Voltage (required to trim)
        \(\mathrm{V}_{\mathrm{xo}}, \mathrm{V}_{\mathrm{yo}}, \mathrm{V}_{\mathrm{zo}} \quad \pm 15( \pm 10)( \pm 10)( \pm 10) \mathrm{V} \max\)
    | DYNAMIC SPECIFICATIONS |  |
| :--- | :--- |
| Small Signal, Unity Gain | 1.0 MHz |
| Full Power Bandwidth | 750 kHz |
| Slew Rate | $45 \mathrm{~V} / \mu \mathrm{sec}$ |
| Small Signal Amplitude |  |
| $\quad$ Error | $1 \%$ at 75 kHz |
| Small Signal 1\% Vector |  |
| $\quad$ Error | 5 kHz |
| Settling Time | $1 \mu \mathrm{sec}$ to $2 \%$ |
| Overload Recovery | $2 \mu \mathrm{sec}$ to $2 \%$ |


*With Z (feedback) terminal used as an input terminal.

## CIRCUIT FUNCTIONS



SQUARE ROOTER


PIN CONFIGURATIONS
H SUFFIX
Top View D SUFFIX



## GENERAL DESCRIPTION

The converter components discussed in this section were designed to form the heart of current and voltage switched D/A and A/D converters.

## CURRENT STEERING CONVERTERS

The AD550 is a quad current switch that can be provided in matched sets to build 4,8 and 12 -bit converters. It consists of four logic-operated current steering switches with a reference transistor on a single monolithic chip. Further, the switch emitter areas are geometrically proportioned to achieve constant current density and thus attain virtually perfect $\mathrm{V}_{\text {BE }}$ matching and tracking between switches. The reference transistor is provided to compensate the external voltage reference, which powers the binary current determining resistor ladder network (e.g., AD850) for $\mathrm{V}_{\mathrm{BE}}$.

The basic operation of the current steering switch is shown in Figure 1. For a nominal full scale output current of 2.0 mA (less than one LSB), a stable reference zener and precision resistor can be used to establish a reference current of $1 / 8 \mathrm{~mA}$
(LSB weight) into the reference transistor $\mathrm{Q}_{2}$. The op amp then adjusts the common base rail so that the individual bit currents will assume their correct values, as shown. These bit currents are then steered from the load or the +5 V supply according to the logic level at each input. A complete 12 -bit converter is shown on the page describing the AD5 50.

## VOLTAGE SWITCHING CONVERTERS

The AD555 is a dielectrically-isolated quad voltage switch that can be provided in matched sets to build 4,8 and 12 -bit converters. Comprising four logic-operated single pole, double throw (SPDT) switches, the AD555 can switch AC signals at its reference terminals, making it ideal for multiplying and D/S and S/D converter applications.
Voltage switching involves the switching of resistor legs of an R/2R ladder network (e.g., AD855) between two continuously variable voltage references as shown in Figure 2. Depending on the logic state of the input terminals, the 2 R leg of the $\mathrm{R} / 2 \mathrm{R}$ network will be connected to the voltage appearing on either Ref A or Ref B. The R/2R network has the property that, no matter what state the digital inputs are in, the impedance seen from the $\mathrm{R} / 2 \mathrm{R}$ output (non-inverting terminal of the output amplifier) is always $R$. A complete 12 -bit D/A converter is shown on the page describing the AD555 switch. (See pgs. for ladder networks.)


Figure 1. Precision Converter with Full Compensation; 4 Bits Shown for Clarity) Simplified Circuit.


Figure 2.

## MONOLITHIC CURRENT SWITCH

 AD550
## GENERAL DESCRIPTION

The AD5 50 is a quad current switch for building 4,8 and 12bit accurate A/D and D/A converters. It features monolithic construction to obtain tight switch matching and tracking with temperature and high reliability for military and avionics applications.

To obtain 12-bit linearity it is important that the AD550 switch be ordered and used as matched sets. Units shipped as matched sets will be marked with a " $\mathrm{V}_{\mathrm{BE}}$ group number" ( -9 to +9 ) following the grade selection for the TO-116 package (e.g., $550 \mathrm{~K}+3 \mathrm{D}$ where +3 is the grade selection and $D$ the package suffix) and following the pin 1 designator for the flat pack (e.g., $\bullet+5 \mathrm{XXXX}$, where $\bullet$ is the pin 1 designator and XXXX the date code).

## APPLICATION



NOTE AD850 includes the binary resistors, interquad attenuators, gain resistors, a bipolar option
and reterence current resistors on a single substrate

ELECTRICAL CHARACTERISTICS (Typical @ $+25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Parameter | AD5 50 |
| :---: | :---: |
| Logic Inputs |  |
| "0" (Switch ON) | 0.8 V max, 1.6 mA nom. <br> (Avg. Sum of 4) |
| "1" (Switch OFF) | $2.0 \mathrm{~V} \min , 100 \mu \mathrm{~A} \max$ |
| Common Base Bias Voltage | $-2.0 \mathrm{~V} \max (-5.0 \mathrm{~V}$ min) |
| Input Coding | Complementary Binary |
| Output Current (Nominal) |  |
| Bit 1 | 1.0 mA |
| Bit 2 | 0.5 mA |
| Bit 3 | 0.25 mA |
| Bit 4 | 0.125 mA |
| Bit 5 | N/A |
| Output Voltage Limit OV (Amplifier $\Sigma$ pt) |  |
| Unloaded | 0V (Amplifier $\Sigma \mathrm{pt}$ ) |
| Resistor Load | -2 V to +10 V |
| Switch Speed |  |
| Switching Time (to turn on LSB) | 500nsec |
| Settling Time to $\pm 1 / 2$ LSB |  |
| 12 Bits | $1.8 \mu \mathrm{sec}$ |
| 10 Bits. | $0.8 \mu \mathrm{sec}$ |
| Accuracy (\% Full Scale, With 10V |  |
| Across Resistor Network) |  |
| Linearity J/S | 1.0\% max |
| K/T | 0.1\% max |
| $\mathrm{L} / \mathrm{U}$ | 0.01\% max |
| Temperature Coefficient | $2 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |
| Power Requirements |  |
| +5VDC ( $\pm 5 \%$ ) | $\pm 12 \mathrm{~mA}$ max |
| -15VDC ( $\pm 3 \%$ ) | -9 mA max |
| Packages | $\begin{gathered} \text { TO-87 (F.P.) } \\ \text { TO-116A (DIL) } \end{gathered}$ |
| Operating Temperature Range |  |
|  |  |
| S, T, U | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| *Same as AD550. |  |

ORDERING GUIDE
AD550 X Y* Z X = Performance/Temperature Grade J, K, L, S, T, U
$\mathrm{Y}=\mathrm{V}_{\mathrm{BE}}$ Characteristic ( -9 to +9 )
$\mathrm{Z}=\mathrm{JEDEC}$ Package Designation $\mathrm{D}=\mathrm{TO}-116, \mathrm{~F}=\mathrm{TO}-87$
*Do not specify unless ordering a replacement part. Units ordered as 12 bit matched sets will automatically be shipped with the same $\mathrm{V}_{\mathrm{BE}}$ characteristic.
PRICES: Consult the factory or your local representative for the latest pricing.

## GENERAL DESCRIPTION

The AD555 is a dielectrically isolated quad voltage switch which is optimized for applications where both digital and analog signals vary - such as in digital to synchro conversion or multiplying DAC applications. Temperature coefficient has been specified to insure full 12 bit linearity when used with a $50 \mathrm{k} \Omega \mathrm{R}-2 \mathrm{R}$ ladder network, such as the AD855.

## APPLICATION



| ELECTRICAL CHARACTERISTICS |  |
| :---: | :---: |
| Parameter | AD555 |
| Input Signals |  |
| Digital | " 0 " $<0.8 \mathrm{~V}$ max @ $-500 \mu \mathrm{~A}, \max$ |
|  | " 1 " $>2.0 \mathrm{~V}$ min @ $+100 \mu \mathrm{~A}, \max$ |
| Analog 1. Ref A and/or Ref B |  |
| in any combinations | -3 Volts, min to +3 Volts, max |
| 2. Ref A Alone |  |
| (Ref B Grounded) | -4 Volts, min to +4 Volts, max |
| Analog Input Current |  |
| (Ref A or Ref B) | -1.5mA, max |
| Output Voltage Range | $\pm 4$ Volts |
| Switch Offset Voltage, $\mathrm{E}_{\text {os }}$ | $555 \mathrm{~J} / \mathrm{S}+10 \mathrm{mV}$, max |
|  | $555 \mathrm{~K} / \mathrm{T}+3 \mathrm{mV}$, max |
|  | $555 \mathrm{~L} / \mathrm{U}+2 \mathrm{mV}$, max |
| Switch Offset Mismatch, $\Delta \mathrm{E}_{\text {os }}$ | AD5 $55 \mathrm{~L} / \mathrm{U} \pm 1 \mathrm{mV}$, max |
| Switch on Resistance, $\mathrm{R}_{\mathrm{S}}$ | $555 \mathrm{~J} / \mathrm{S} 100 \Omega$, max |
|  | $555 \mathrm{~K} / \mathrm{T} 40 \Omega$, max |
|  | $555 \mathrm{~L} / \mathrm{U} 25 \Omega$, max |
| On Resistance Mismatch, $\Delta \mathbf{R}_{\mathbf{S}}$ | $555 \mathrm{~L} / \mathrm{U}$ 10 ${ }^{\text {, max }}$ |
| Switch Load Current | 0.5 mA , max |
| Settling Time (0.01\%) | $5 \mu \mathrm{sec}$ |
| Switch Leakage Current | 1.5 nA, max |
| Error Temp Coefficient | $\pm 5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |
| Power Requirements | $\pm 15 \mathrm{~V} \pm 20 \% @+7 \mathrm{~mA}$ |
|  | $-4 \mathrm{~V} \pm 1 \%$ @ -3 mA 130 mW (typ) ${ }^{\text {a }}$ (max) |
| Dissipation | 130 mW (typ), 200 mW (max) |
| Packages | TO-87 Flat Pack |
|  | TO-116 Dual In-Line |
| Operating Temperature Range | Types J, K, L $\quad 0$ to $+70^{\circ} \mathrm{C}$ |
|  | Types S, T, U $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |

Prices: Consult the factory or your local representative for the latest pricing.

## IC, LOW DRIFT VOLTAGE REFERENCE

AD580

## PRODUCT DESCRIPTION

The AD580 is a three-terminal, low cost, temperature compensated, bandgap voltage reference which provides a fixed 2.5 V output voltage for inputs between 4.5 V and 30 V . A unique combination of advanced circuit design and sophisticated thin film resistor processing capability provides the AD580 with a temperature stability of better than $40 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ and long term stability of better than $250 \mu \mathrm{~V}$. In addition, the low quiescent current drain of 1.5 mA max offers a clear advantage over classical zener techniques.
The AD580 is recommended as a stable reference for all 8-bit and 10-bit D-to-A converters that require an external reference. In addition, the wide input range of the AD580,

## PIN CONFIGURATION

TO-52


BOTTOM VIEW allowing operation with 5 volt logic supplies, makes the AD580 a good choice for all digital panel meter applications.
The AD580J and AD580K are specified for operation over the 0 to $+70^{\circ} \mathrm{C}$ temperature range ; the AD 580 S is specified for operation over the extended temperature range of -55 to $+125^{\circ} \mathrm{C}$.

SPECIFICATIONS (Typical @ $\mathrm{E}_{\text {in }}=+15 \mathrm{~V}$ and $+25^{\circ} \mathrm{C}$ unless otherwise specified)

| MODEL | AD580J | AD580K | AD580S |
| :---: | :---: | :---: | :---: |
| ABSOLUTE MAX RATINGS |  |  |  |
| Input Voltage | $40 \mathrm{VE} \mathrm{E}_{\text {in }}$ | * | * |
| Power Dissipation @ $+25^{\circ} \mathrm{C}$ |  |  |  |
| Ambient Temperature | $350 \mathrm{~mW}$ | * | * |
| Derate Above $+25^{\circ} \mathrm{C}$ | $2.8 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ | * | * |
| Operating Junction Temp Range | -55 to $+150^{\circ} \mathrm{C}$ | * | * |
| Storage Temperature Range | -65 to $+175^{\circ} \mathrm{C}$ | * | * |
| Lead Temperature (soldering, 10 sec ) | $+300^{\circ} \mathrm{C}$ | * | * |
| Thermal Resistance |  |  |  |
| Junction-to-Case | $100^{\circ} \mathrm{C} / \mathrm{W}$ | * | * |
| Junction-to-Ambient | $360^{\circ} \mathrm{C} / \mathrm{W}$ | * | * |
| Operating Temperature Range | 0 to $+70^{\circ} \mathrm{C}$ | * | -55 to $+125^{\circ} \mathrm{C}$ |
| OUTPUT VOLTAGE | $2.425 \mathrm{~V} \min (2.575 \mathrm{~V} \max )$ | 2.450 V min $(2.550 \mathrm{~V}$ max) | 2.425 V min $(2.575 \mathrm{~V}$ max) |
| OUTPUT TURN-ON SETTLING TIME ${ }^{1}$ | $6.0 \mu \mathrm{sec}$ to $0.04 \%$ | * | * |
| OUTPUT VOLTAGE CHANGE |  |  |  |
| $\mathrm{T}_{\text {min }}$ to $\mathrm{T}_{\text {max }}$ | 15 mV max | 7 mV max | 25 mV max |
| LINE REGULATION |  |  |  |
| $7 \mathrm{~V} \leqslant \mathrm{~V}_{\text {in }} \leqslant 30 \mathrm{~V}$ | $6 \mathrm{mV} \max (0.6 \mathrm{mV}$ typ) | $4 \mathrm{mV} \max (0.6 \mathrm{mV}$ typ) | $6 \mathrm{mV} \max (0.6 \mathrm{mV}$ typ) |
| $4.5 \mathrm{~V} \leqslant \mathrm{~V}_{\text {in }} \leqslant 7 \mathrm{~V}$ | $3 \mathrm{mV} \max$ ( 0.3 mV typ) | 2 mV max ( 0.3 mV typ) | 3 mV max ( 0.3 mV typ) |
| LOAD REGULATION |  |  |  |
| $\triangle \mathrm{I}=10 \mathrm{~mA}$ | 10 mV max | * | * |
| QUIESCENT CURRENT | 1.5 mA max ( 1.0 mA typ) | * | * |
| NOISE (0.1 to 10 Hz ) | $60 \mu \mathrm{~V}$ (p-p) | * | * |
| STABILITY |  |  |  |
| Long Term | $250 \mu \mathrm{~V}$ | * | * |
| Per Month | $25 \mu \mathrm{~V}$ | * | * |
| PRICE |  |  |  |
| (1-24) | \$3.00 | \$6.00 | \$11.25 |
| (25-99) | \$2.40 | \$4.80 | \$9.00 |
| (100-999) | \$2.00 | \$4.00 | \$7.50 |

NOTE 1: Self-heating time constant will depend on heat sinking, raw supply voltage and load conditions.
*Specification same as AD580J.

## INTEGRATED CIRCUIT I2-BIT D/A CONVERTER

## PRODUCT DESCRIPTION

The AD562 is an integrated circuit 12-bit digital-to-analog converter consisting of a specially designed precision bipolar switch and control amplifier chip and a compatible high stability silicon chromium thin film resistor chip. The two IC chips are internally connected and mounted in a hermetically-sealed ceramic 24 -lead dual-in-line package.

A unique combination of advanced circuit design, high stability SiCr thin film resistor processing, and laser trimming technology provides the AD562 with true 12-bit accuracy. The maximum error at $+25^{\circ} \mathrm{C}$ is limited to $\frac{1}{4}$ LSB ( S version) and the gain temperature coefficient is limited to $3 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ max. Monotonicity is guaranteed over the full operating temperature range of the devices.

The AD562 is recommended for all high accuracy 12-bit D/A converter applications where true 12 -bit performance is required and small size and low cost are primary considerations. The AD562 is also ideal for use in constructing A/D conversion systems and as a building block for higher resolution D/A systems. The AD 562 K is specified for operation over the 0 to $+70^{\circ} \mathrm{C}$ temperature range, the AD562A for operation over the -25 to $+85^{\circ} \mathrm{C}$ temperature range, and the AD562S for operation over the full extended temperature range of -55 to $+125^{\circ} \mathrm{C}$.


[^23]SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ and 10 V Ref. unless otherwise specified)

|  BINARY <br> MODEL BINARY CODED DECIMAL | AD562KD/BIN AD562KD/BCD | AD562AD/BIN <br> AD562AD/BCD | AD562SD/BIN | AD562SD/BCD |
| :---: | :---: | :---: | :---: | :---: |
| DATA INPUTS |  |  |  |  |
| TTL, $\mathrm{V}_{\mathrm{cc}}=+5 \mathrm{~V}$, Pin 2 Open Ckt |  |  |  |  |
|  |  |  |  |  |
| Bit OFF "Logic 0" | $\leqslant 0.8 \mathrm{~V} @-100 \mu \mathrm{~A}$ max | * | * | * |
| CMOS |  |  |  |  |
| $4.75 \mathrm{~V} \leqslant \mathrm{~V}_{\mathrm{cc}} \leqslant 15.8 \mathrm{~V}$, Pin 2 tied to Pin 1 |  |  |  |  |
| Bit ON "Logic 1" | $\geqslant 70 \% \mathrm{~V}_{\text {cc }}$ @ 100 nA max | * | * | * |
| Bit OFF "Logic 0" | $\leqslant 30 \% \mathrm{~V}_{\mathrm{cc}}$ @ $-100 \mu \mathrm{~A}$ max | * | * | * |
| OUTPUT |  |  |  |  |
| Current |  |  |  |  |
| Unipolar | 0 to $-2 \mathrm{~mA}, \pm 10 \%$ | * | * | * |
| Bipolar | -1 to $+1 \mathrm{~mA}, \pm 10 \%$ | * | * |  |
| Resistance | $8.0 \mathrm{k} \Omega$ | * | * | * |
| Leakage (all bits OFF) | 0.03\% of F.S. max | * | * | * |
| Capacitance | 33 pF | * | * |  |
| Compliance Voltage | +10 to -1.5 V | * | * | * |
| RESOLUTION | 12 bits | * | * | * |
| NONLINEARITY (Line referred to F.S.) | $\pm 1 / 2 \mathrm{LSB}$ (max) | * | $\pm 1 / 4$ LSB max | $\pm 1 / 10$ LSB $\max$ |
| SETTLING TIME TO $1 / 2$ LSB (Note 1 ) <br> All bits ON-to-OFF or OFF-to-ON | $3.5 \mu \mathrm{~s}$ max current settling into short circuit | * | * | * |
| MAJOR CARRY SWITCHING TRANSIENT TO 90\% COMPLETE | 400ns | * | * | * |
| NOISE |  |  |  |  |
| POWER REQUIREMENT |  |  |  |  |
| $\mathrm{V}_{\text {CC }}$ | +4.75 to +15.8 VDC @ 15 mA | * | * | * |
| $\mathrm{V}_{\text {EE }}$ | $-15 \mathrm{VDC} \pm 5 \%$ @ 20 mA | * | * | - |
| POWER SUPPLY SENSITIVITY OF GAIN |  |  |  |  |
| $\mathrm{V}_{\text {CC }}$ @ +5VDC | 1 ppm of F.S./\% max | * | * | * |
| $\mathrm{V}_{\mathrm{CC}}$ @ +15VDC | 1 ppm of F.S./\% max | * | * | * |
| VEE@-15VDC | 2ppm of F.S./\% max | * | * | * |
| TEMPERATURE RANGE Operating Storage | $\begin{aligned} & 0 \text { to }+70^{\circ} \mathrm{C} \\ & -55 \text { to }+150^{\circ} \mathrm{C} \\ & \hline \end{aligned}$ | $-25 \text { to }+85^{\circ} \mathrm{C}$ | $-55 \text { to }+125^{\circ} \mathrm{C}$ | $-55 \text { to }+125^{\circ} \mathrm{C}$ |
| TEMPERATURE COEFFICIENT |  |  |  |  |
| Leakage Current |  |  |  |  |
| 0 to $+70^{\circ} \mathrm{C}$ | 1 ppm of F.S. ${ }^{\circ} \mathrm{C}$ max | $-{ }^{-}$ | - | - |
| -25 to $+85^{\circ} \mathrm{C}$ | - | 1 ppm of F.S. ${ }^{\circ} \mathrm{C}$ max |  | - |
| -55 to $+125^{\circ} \mathrm{C}$ | - |  | 2ppm of F.S. ${ }^{\circ} \mathrm{C}$ max | 2ppm of F.S. ${ }^{\circ} \mathrm{C}$ max |
| Bipolar Offset | 4ppm of F.S. ${ }^{\circ} \mathrm{C}$ max | * | * |  |
| Gain (exclusive of Reference Voltage) | 3 ppm of F.S. $I^{\circ} \mathrm{C}$ max | * |  |  |
| Differential Nonlinearity | 2 ppm of F.S. $/{ }^{\circ} \mathrm{C}$ | * | 1ppm of F.S. $/^{\circ} \mathrm{C}$ | 1 ppm of F.S. $/^{\circ} \mathrm{C}$ |
| MONOTONICITY | Guaranteed over full operating temp range | * | * | * |
| EXTERNAL ADJUSTMENTS |  |  |  |  |
| Gain Adjustment Range (see Fig. 1 \& Table I) | $\pm 0.25 \%$ of F.S. | * | * | * |
| Binary Bipolar Offset Range <br> (see Fig. 1 \& Table I) | $\pm 0.25 \%$ of F.S. | * | * | * |
| Binary Coded Decimal Bipolar Offset Range (see Fig. 1 \& Table I) | $\pm 0.17 \%$ of F.S. | * | * | * |
| RANGES PROGRAMMABLE |  |  |  |  |
| (see Figure 1 \& Table I) | 0 to +5 V | * | * | * |
|  | -2.5 to +2.5 V | * | * | * |
|  | 0 to +10 V | * | * | * |
|  | -5 to +5 V | * | * | * |
|  | -10 to +10 V | * | * | * |
| REFERENCE VOLTAGE INPUT |  |  |  |  |
| Input Impedance | $20 \mathrm{k} \Omega, \pm 10 \%$ | * | * | * |
| Range | 0 to +10 V | * | * | * |
| MULTIPLYING MODE PERFORMANCE (All Models) |  |  |  |  |
| Quadrants | Two (2): bipolar operation at digital input only. |  |  |  |
| Reference Voltage | 0 to +10 V , unipolar. Digital input code multiplies reference voltage. |  |  |  |
| Accuracy | 10 bits ( $\pm 0.05 \%$ of reduced F.S.) for 1VDC reference voltage. |  |  |  |
| Reference Feedthrough (unipolar mode, all bits OFF, and 0 to $+10 \mathrm{~V}[\mathrm{p}-\mathrm{p}]$, sinewave |  |  |  |  |
| Output Slew Rate (all bits ON and 10V |  |  |  |  |
| Output Settling Time (all bits ON and |  |  |  |  |
| Control Amplifier Small-Signal Closed-Loop |  |  |  |  |
| PRICE |  |  |  |  |
| 1-24 | \$58 | \$74 | \$150 | \$150 |
| 25-99 | \$47 | \$59 | \$120 | \$120 |
| 100-249 | \$39 | \$49 | \$100 | \$100 |

[^24]
## APPLICATIONS CONSIDERATIONS



4-Digit BCD DAC


## 4-DIGIT BCD DAC

Two (2) AD562/BCD's can be used to construct a 4 -digit ( $0.01 \%$ ) DAC. The least significant digit DAC's current output is attenuated by a factor of 1000 via the $100 \Omega$ and $100 \mathrm{k} \Omega$ resistors. This current is summed with the current output of the MSD DAC to give a 9.999 V full scale voltage output.

## 4-DIGIT DAC ZERO <br> AND SCALE ADJUST.

Turn all bits OFF, adjust R1 until output of DAC is 0 volts.

Turn 8 and 1 bit ON for MSD, 100's, and 10 's digits, adjust R2 until output of DAC is 9.990 volts.

Leaving 8 and 1 bit ON for first three digits, turn 8 and 1 bits ON for LSD digit, adjust R3 until output of DAC is 9.999 V .

## 12-BIT SUCCESSIVE APPROXIMATION A/D CONVERTER

The most popular medium speed ( 1 to $10 \mu \mathrm{sec} / \mathrm{bit}$ ) A/D converter is the successive approximation type, in which the digital output equivalent of the analog input is formed by comparing a programmed D/A converter output with the analog input. The digital output is successively compared, one bit at a time, until the final comparison is within $1 / 2$ LSB of the AD562.

The conversion speed of a successive approximation A/D converter is determined by the settling time of the MSB to $1 / 2$ LSB, the speed of the comparator, and the switching speed of the "SAR." The A/D converter configuration shown will convert at a 40 kHz rate for 12 bits.

## DUAL MONOLITHIC FET'S AND BIPOLAR TRANSISTORS

DUAL MONOLITHIC FIELD EFFECT TRANSISTORS
AD3954/2N3954 SERIES: Medium geometry, general purpose design gives high $\mathrm{Y}_{\mathrm{fs}}$ and good frequency response. Optimized for $200 \mu \mathrm{~A}$.
2N5900 SERIES: Small geometry, optimized for $30 \mu \mathrm{~A}$, gives gate current less than 1 pA .
AD830 SERIES: Small geometry, optimized for $30 \mu \mathrm{~A}$, features gate current of only 0.1 pA maximum.
AD835 SERIES: Medium geometry designed for high transconductance.
AD840 SERIES: Large geometry designed for low noise $(15 \mathrm{nV} / \sqrt{\mathrm{Hz}} @ 10 \mathrm{~Hz})$, low drift and low initial offset.

DUAL MONOLITHIC BIPOLAR TRANSISTORS
AD810 SERIES: General purpose NPN provides good log conformance and drift characteristics as well as low noise.

AD814 SERIES: Super beta NPN dual featuring V CEO $^{\text {of }}$ 20 V and $\mathrm{h}_{\mathrm{fe}}$ of 2000 . Superior design and processing also provide typical offset of $200 \mu \mathrm{~V}$ and typical drift of $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$.

AD818: This geometry provides nearly ideal log conformance. $\mathrm{R}_{\mathrm{e}}$ exhibits excellent conformance over 8 current decades with a deviation from the ideal typically less than one ohm.

AD820: General purpose PNP provides high beta, low offset and low temperature drift.

## DUAL MONOLITHIC BIPOLAR TRANSISTORS

| TYPE | $\begin{aligned} & \mathbf{v}_{\mathbf{B E}_{\mathbf{1}}} \\ & -\mathbf{v}_{\mathbf{B E}_{\mathbf{2}}} \\ & \text { MAX. } \end{aligned}$ | $\frac{\Delta \mathbf{V}_{\mathbf{B E}_{1}}-\mathrm{V}_{\mathrm{BE}_{2}}}{\Delta \mathrm{~T}}$ <br> MAX. | $\mathrm{I}_{\mathrm{B}_{1}}-\mathrm{I}_{\mathrm{B}_{2}}$ <br> max. | $\frac{\Delta \mathbf{I}_{\mathbf{B}_{1}}{ }^{-\mathbf{I}_{\mathbf{B}_{2}}}}{\Delta \mathrm{~T}}$ <br> MAX. | $\mathrm{h}_{\mathrm{FE}}$ | $\begin{aligned} & { }^{\mathbf{B V} V_{\text {CEO }}} \\ & { }^{\mathbf{I}} \mathbf{C}=5 \mu \mathrm{~A} \end{aligned}$ | $\begin{gathered} { }^{\mathrm{I}} \mathrm{CBO} \\ \mathbf{v}_{\mathrm{CB}}=80 \% \\ \text { of } \mathbf{v}_{\mathrm{CEO}} \\ \text { MAX. } \end{gathered}$ | $\begin{aligned} & \mathrm{C}_{\mathrm{OB}} \\ & \mathrm{I}_{\mathrm{E}=0} \\ & \mathrm{v}_{\mathrm{CB}}=5 \mathrm{~V} \\ & \quad \text { MAX. } \end{aligned}$ | $\mathrm{f}_{\mathbf{T}}$ | TEST CONDITIONS | PRICE |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  | MIN./MAX. | MIN. |  |  |  |  | 1-99 | 100-999 |
| MONOLITHIC DUAL NPN TRANSISTORS - General Purpose; Good Log Conformance (TO-52 CAN) |  |  |  |  |  |  |  |  |  |  |  |  |
| AD810 | 3 mV | $15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | 20 nA | . $6 \mathrm{nA} / /^{\circ} \mathrm{C}$ | 100/-- | 45 V | . 2 nA | 2 pF | 200 MHz | ${ }^{\mathrm{I}} \mathrm{C}=10 \mu \mathrm{~A}$ | \$2.00 | \$1.32 |
| AD811 | 1.5 mV | $7.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | 10 nA | . $3 \mathrm{nA} /{ }^{\circ} \mathrm{C}$ | 200/600 | 45 V | . 2 nA | 2 pF | 200 MHz | $\mathrm{V}_{\mathrm{CE}}=5 \mathrm{~V}$ | 2.60 | 1.85 |
| AD812 | 1.0 mV | $5.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | 2.5 nA | . $3 \mathrm{nA} /{ }^{\circ} \mathrm{C}$ | 400/1000 | 35 V | 2nA | 2 pF | 200 MHz | $\mathrm{f}_{\mathrm{T}}{ }^{\text {( } \mathrm{I}_{\mathrm{C}}=1 \mathrm{~mA}}$ | 3.80 | 2.50 |
| AD813 | 0.5 mV | $2.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | 5 nA | . $3 \mathrm{nA} /{ }^{\circ} \mathrm{C}$ | 200/600 | 45 V | . 2 nA | 2 pF | 200 MHz | $\mathrm{v}_{\mathrm{CE}}=5 \mathrm{~V}$ | 4.75 | 3.30 |
| SUPER BETA MONOLITHIC DUAL NPN TRANSISTORS - Super Beta with Exceptionally High $\mathbf{V}_{\text {CEO }}$ (TO-52 CAN) |  |  |  |  |  |  |  |  |  |  |  |  |
| AD814 | 1 mV | $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | 1 nA | -- | 1000/-- | 35 V | 10 pA | .8pF | 100 MHz | ${ }^{1} \mathrm{C}^{\text {c }}=10 \mu \mathrm{~A}$ | 5.00 | 4.00 |
| AD815 | 1 mV | $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | .5nA | -- | 2000/-- | 20 V | 10 pA | .8pF | 100 MHz | $\mathrm{v}_{\mathrm{CE}}=5 \mathrm{~V}$ | 6.50 | 5.50 |
| AD816 | 1 mV | $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | . 5 nA | -- | 2000/-- | 10 V | 10 pA | .8pF | 100 MHz | $\begin{aligned} & \mathrm{f}_{\mathrm{T} \text { @ } \mathrm{I}_{\mathrm{C}}=200 \mu \mathrm{~A}}^{\mathrm{v}_{\mathrm{CE}}=5 \mathrm{~V}} \end{aligned}$ | 5.75 | 4.60 |
| MONOLITHIC DUAL PNP TRANSISTORS - General Purpose (TO-52 CAN) |  |  |  |  |  |  |  |  |  |  |  |  |
| AD820 | 5 mV | $20 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | -- | -- | 100/-- | 25 V | .2nA | 2 pF | -- | $\mathrm{I}_{\mathrm{C}}=10 \mu \mathrm{~A}$ | 2.10 | 1.45 |
| AD821 | 1 mV | $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | 10 nA | . $3 \mathrm{nA} / /^{\circ} \mathrm{C}$ | 150/600 | 45 V | . 2 nA | 2 pF | 200 MHz | $\mathrm{v}_{\mathrm{CE}}=5 \mathrm{~V}$ | 2.75 | 1.85 |
| AD822 | . 5 mV | $2.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | 5 nA | . $3 \mathrm{nA} / /^{\circ} \mathrm{C}$ | 200/600 | 60 V | . 2 nA | 2 pF | 200 MHz |  | 5.25 | 3.50 |
| MONOLITHIC DUAL NPN LOG CONFORMANCE TRANSISTORS - Excellent Log Conformance (TO-52 CAN) |  |  |  |  |  |  |  |  |  |  |  |  |
| AD818 | 1.0 mV | $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $10 n \mathrm{~A}$ | . $3 \mathrm{nA} / /^{\circ} \mathrm{C}$ | 200/600 | 20 V | . 2 nA | 2 pF | 200MHz | $\begin{aligned} & \Delta \mathrm{r}_{\mathrm{e}}=1 \Omega \text { from } \\ & \text { ideal @ } \mathrm{I}_{\mathrm{C}}=10- \\ & 100-1000 \mu \mathrm{~A} \end{aligned}$ | 5.00 | 3.50 |
|  |  |  |  |  |  |  |  |  |  | $\mathrm{v}_{\mathrm{CE}}=5 \mathrm{~V}$ <br> conditions same <br> as 810 series. |  |  |

## PIN OUT INFORMATION

DUAL FETS

## (Bottom View)



DUAL TRANSISTORS

## NPN <br> (Bottom View)



PNP (Bottom View)


## DUAL MONOLITHIC FIELD EFFECT TRANSISTORS

| TYPE | ${ }^{\mathbf{I}} \mathbf{G}$ | $\mathbf{V G S}_{\mathbf{1 - 2}}$ | $\Delta \mathbf{V}_{\mathbf{G S}}^{1-2}{ }^{1}$ | TDN ${ }^{2}$ | $\mathbf{Y}_{\text {fs }}$ | $\begin{gathered} \mathbf{B V}_{\mathbf{G S S}} \\ \text { MIN. } \end{gathered}$ | ${ }^{I_{\text {DSS }}}$ <br> MIN. | $\mathrm{V}_{\mathrm{p}}$ | TEST <br> CONDITION | PRICE |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  | MAX. | MAX. | MAX. |  |  |  |  | MAX. |  | 1-99 | 100-999 |
| MEDIUM GEOMETRY, LOW NOISE, GENERAL PURPOSE DUAL MONOLITHIC N-CHANNEL FETS (TO-71 CAN) |  |  |  |  |  |  |  |  |  |  |  |
| AD3954A | 50 pA | 10 mV | $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $700 \mu \mathrm{mho}$ | 40 V | $500 \mu \mathrm{~A}$ | 4.5 V | $\mathrm{V}_{\text {DG }}$ or | \$ 6.90 | \$ 5.80 |
| AD3954 | 50 pA | 10 mV | $10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $700 \mu \mathrm{mho}$ | 40 V | $500 \mu \mathrm{~A}$ | 4.5 V | $\mathrm{V}_{\mathrm{DS}}=20 \mathrm{~V}$ | 5.65 | 4.65 |
| AD3955 | 50 pA | 25 mV | $25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $700 \mu \mathrm{mho}$ | 40 V | $500 \mu \mathrm{~A}$ | 4.5 V | $\mathrm{I}_{\mathrm{D}}=200 \mu \mathrm{~A}$ | 4.25 | 3.55 |
| AD3956 | 50 pA | 25 mV | $50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $700 \mu \mathrm{mho}$ | 40 V | $500 \mu \mathrm{~A}$ | 4.5 V | $\mathrm{I}_{\mathrm{D}}=200 \mu \mathrm{~A}$ | 3.00 | 2.00 |
| AD3958 | 50 pA | 25 mV | $100 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $700 \mu \mathrm{mho}$ | 40 V | $500 \mu \mathrm{~A}$ | 4.5 V |  | 2.25 | 1.38 |
| 2N3954A | 50 pA | 5 mV | $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $700 \mu \mathrm{mho}$ | 50 V | $500 \mu \mathrm{~A}$ | 4.5 V | $\mathrm{V}_{\text {DG }}$ or | 7.35 | 6.00 |
| 2N3954 | 50 pA | 5 mV | $10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $700 \mu \mathrm{mho}$ | 50 V | $500 \mu \mathrm{~A}$ | 4.5 V |  | 5.95 | 4.95 |
| 2N3955A | 50 pA | 5 mV | $15 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $700 \mu \mathrm{mho}$ | 50 V | $500 \mu \mathrm{~A}$ | 4.5 V | $\mathrm{I}_{\mathrm{D}} \mathrm{DS}=200 \mu \mathrm{~A}$ | 5.65 | 4.65 |
| 2N3955 | 50 pA | 10 mV | $25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $700 \mu \mathrm{mho}$ | 50 V | $500 \mu \mathrm{~A}$ | 4.5 V | $\mathrm{I}_{\mathrm{D}}=200 \mu \mathrm{~A}$ | 4.55 | 3.75 |
| 2N3956 | 50 pA | 15 mV | $50 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $700 \mu \mathrm{mho}$ | 50 V | $500 \mu \mathrm{~A}$ | 4.5 V |  | 3.45 | 2.35 |
| 2N3957 | 50 pA | 20 mV | $75 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $700 \mu \mathrm{mho}$ | 50 V | $500 \mu \mathrm{~A}$ | 4.5 V |  | 3.00 | 2.00 |
| 2N3958 | 50pA | 25 mV | $100 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $700 \mu \mathrm{mho}$ | 50 V | $500 \mu \mathrm{~A}$ | 4.5 V |  | 2.25 | 1.38 |
| SMALL GEOMETRY, VERY LOW $\mathrm{I}_{\mathbf{G}}$ DUAL MONOLITHIC N-CHANNEL FETS (TO-78 CAN) |  |  |  |  |  |  |  |  |  |  |  |
| 2N5906 | 1 pA | 5 mV | $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $100 \mu \mathrm{mho}$ | 40 V | $30 \mu \mathrm{~A}$ | 4.5 V | $\mathrm{V}_{\text {DG }}$ or | 17.95 | 15.10 |
| 2N5907 | 1 pA | 5 mV | $10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $100 \mu \mathrm{mho}$ | 40 V | $30 \mu \mathrm{~A}$ | 4.5 V | $\mathrm{V}_{\text {DS }}=10 \mathrm{~V}$ | 13.35 | 10.50 |
| 2N5908 | 1 pA | 10 mV | $20 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $100 \mu \mathrm{mho}$ | 40 V | $30 \mu \mathrm{~A}$ | 4.5 V | $\mathrm{I}_{\mathrm{D}}=30 \mu \mathrm{~A}$ | 9.25 | 7.40 |
| 2N5909 | 1 pA | 15 mV | $40 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $100 \mu \mathrm{mho}$ | 40 V | $30 \mu \mathrm{~A}$ | 4.5 V | $\mathrm{I}_{\mathrm{D}}=30 \mu \mathrm{~A}$ | 6.50 | 5.10 |
| 2N5905 | 3 pA | 15 mV | $40 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $100 \mu \mathrm{mho}$ | 40 V | $30 \mu \mathrm{~A}$ | 4.5 V |  | 5.35 | 4.35 |
| SMALL GEOMETRY, EXTREMELY LOW $\mathrm{I}_{\mathbf{G}}$ DUAL MONOLITHIC N-CHANNEL FETS (TO-78 CAN) |  |  |  |  |  |  |  |  |  |  |  |
| AD830 | .1pA | 25 mV | $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $100 \mu \mathrm{mho}$ | 40 V | $30 \mu \mathrm{~A}$ | 4.5 V | $\mathrm{V}_{\text {DG }}$ or | 13.40 | 11.10 |
| AD831 | .1pA | 25 mV | $10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $100 \mu \mathrm{mho}$ | 40 V | $30 \mu \mathrm{~A}$ | 4.5 V | $\mathrm{V}_{\mathrm{DS}}=10 \mathrm{~V}$ | 10.70 | 8.90 |
| AD832 | .1pA | 25 mV | $20 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $100 \mu \mathrm{mho}$ | 40 V | $30 \mu \mathrm{~A}$ | 4.5 V | $\mathrm{I}_{\mathrm{D}}=30 \mu \mathrm{~A}$ | 8.60 | 7.20 |
| AD833A | .1pA | 25 mV | $40 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $100 \mu \mathrm{mho}$ | 40 V | $30 \mu \mathrm{~A}$ | 4.5 V | $\mathrm{D}^{-}=30 \mu \mathrm{~A}$ | 7.00 | 5.60 |
| AD833 | . 5 pA | 25 mV | $75 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $100 \mu \mathrm{mho}$ | 40 V | $30 \mu \mathrm{~A}$ | 4.5 V |  | 5.10 | 4.25 |
| LARGE GEOMETRY, HIGH TRANSCONDUCTANCE DUAL MONOLITHIC N-CHANNEL FETS (TO-71 CAN) |  |  |  |  |  |  |  |  |  |  |  |
| AD835 | 20pA | 5 mV | $10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | 1500 umho | 30 V | $500 \mu \mathrm{~A}$ | 3.5 V | $\mathrm{V}_{\text {DG }}$ or | 5.95 | 4.95 |
| AD836 | 20pA | 10 mV | $10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1500 \mu \mathrm{mho}$ | 30 V | $500 \mu \mathrm{~A}$ | 3.5 V | $\mathrm{V}_{\text {DS }}=15 \mathrm{~V}$ | 4.85 | 4.10 |
| AD837 | 20 pA | 10 mV | $25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1500 \mu \mathrm{mho}$ | 30 V | $500 \mu \mathrm{~A}$ | 3.5 V | $\mathrm{I}_{\mathrm{D}}=200 \mu \mathrm{~A}$ | 4.25 | 3.75 |
| AD838 | 20 pA | 15 mV | $25 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1500 \mu \mathrm{mho}$ | 30 V | $500 \mu \mathrm{~A}$ | 3.5 V | $\mathrm{D}_{\mathrm{D}}$ | 3.75 | 3.50 |
| AD839 | 20 pA | 20 mV | $40 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1500 \mu \mathrm{mho}$ | 30 V | $500 \mu \mathrm{~A}$ | 3.5 V |  | 3.50 | 3.25 |

LARGE GEOMETRY; LOW DRIFT, EXTREMELY LOW NOISE: $15 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ @ 10 Hz max. DUAL MONOLITHIC N-CHANNEL FETS (TO-71 CAN)

| AD840 | 50 pA | 5 mV | $5 \mu \mathrm{~V} /{ }^{\circ}{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $800 \mu \mathrm{mho}$ | 40 V | $500 \mu \mathrm{~A}$ | 4.5 V | $\mathrm{~V}_{\mathrm{DG}}$ or | 9.40 |
| :--- | ---: | ---: | ---: | ---: | :--- | :--- | :--- | :--- | :--- | :--- |
| AD841 | 50 pA | 5 mV | $10 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $800 \mu \mathrm{mho}$ | 40 V | $500 \mu \mathrm{~A}$ | 4.5 V | $\mathrm{~V}_{\mathrm{DS}}=20 \mathrm{~V}$ | 7.80 |
| AD842 | 50 pA | 25 mV | $40 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ | $1 \mu \mathrm{~V} /^{\circ} \mathrm{C}$ | $800 \mu \mathrm{mho}$ | 40 V | $500 \mu \mathrm{~A}$ | 4.5 V | $\mathrm{I}_{\mathrm{D}}=200 \mu \mathrm{~A}$ | 3.50 |

NOTES:

1. $\mathrm{T}_{\mathrm{A}}=-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$.
2. Temperature Drift Nonlinearity $=1 / 2\left[\frac{\Delta \mathrm{~V}_{\mathrm{GS}}^{1-2}}{}-\frac{\Delta \mathrm{V}_{\mathrm{GS}}^{1-2}}{} \operatorname{Tr}_{\left(-55 \text { to }+25^{\circ} \mathrm{C}\right)}^{\Delta \mathrm{T}_{\left(+25 \text { to }+125^{\circ} \mathrm{C}\right)}}\right]$

## MONOLITHIC CMOS <br> SWITCHES AND MULTIPLEXERS

Analog Devices manufactures the industry's most complete line of monolithic CMOS analog switching elements, featuring low power dissipation and TTL/DTL/CMOS logic compatibility. They are excellent choices for use in any circuit where analog signals are to be switched, routed, or time-multiplexed.
A proprietary device surface stabilization process utilizes silicon nitride passivation and die glassivation to ensure excellent longterm stability and high reliability.

MULTIPLEXER SUMMARY

AD7501, AD7503
8-Channel MUX
TTL/DTL/CMOS Direct Interface Output "Enable" Control
Power Dissipation: $30 \mu \mathrm{~W}$
AD7503 Replaces HI-1818

AD7502, AD7507
4- \& 8-Channel Differential MUX TTL/DTL/CMOS Direct Interface Output "Enable" Control AD7507 is superior plug-in replacement for DG-507

AD7506<br>16-Channel MUX<br>TTL/DTL/CMOS Direct Interface<br>Output "Enable" Control<br>Power Dissipation: 1.5 mW<br>Superior replacement for DG-506

TRUTH TABLES

| AD7501 |  |  |  |  | AD7503 |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{A}_{2}$ | $\mathrm{A}_{1}$ | $\mathrm{A}_{0}$ | $\mathrm{E}_{\mathrm{N}}$ | "ON" | $\mathrm{A}_{2}$ | $\mathrm{A}_{1}$ | $\mathrm{A}_{0}$ |  | "ON" |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 2 | 0 | 0 | 1 | 0 | 2 |
| 0 | 1 | 0 | 1 | 3 | 0 | 1 | 0 | 0 | 3 |
| 0 | 1 | 1 | 1 | 4 | 0 | 1 | 1 | 0 | 4 |
| 1 | 0 | 0 | 1 | 5 | 1 | 0 | 0 | 0 | 5 |
| 1 | 0 | 1 | 1 | 6 | 1 | 0 | 1 | 0 | 6 |
| 1 | 1 | 0 | 1 | 7 | 1 | 1 | 0 | 0 | 7 |
| 1 | 1 | 1 | 1 | 8 | 1 | 1 | 1 | 0 | 8 |
| X | X | X | 0 | None | X | X | X | 1 | None |

TRUTH TABLES

| $\mathrm{AD}^{4} 502$ |  |  |  |
| :--- | :--- | :--- | :--- |
| $\mathrm{~A}_{1}$ | $\mathrm{~A}_{0}$ | $\mathrm{E}_{\mathrm{N}}$ | "ON" |
| 0 | 0 | 1 | $1 \& 5$ |
| 0 | 1 | 1 | $2 \& 6$ |
| 1 | 0 | 1 | $3 \& 7$ |
| 1 | 1 | 1 | $4 \& 8$ |
| X | X | 0 | None |


| AD 7507 |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{~A}_{2}$ | $\mathrm{~A}_{1}$ | $\mathrm{~A}_{0}$ | $\mathrm{E}_{\mathrm{N}}$ | "ON" |  |
| 0 | 0 | 0 | 1 | $1 \& \&$ | 9 |
| 0 | 0 | 1 | 1 | $2 \& 10$ |  |
| 0 | 1 | 0 | 1 | $3 \& 11$ |  |
| 0 | 1 | 1 | 1 | $4 \& 12$ |  |
| 1 | 0 | 0 | 1 | $5 \& 13$ |  |
| 1 | 0 | 1 | 1 | $6 \& 14$ |  |
| 1 | 1 | 0 | 1 | $7 \& 15$ |  |
| 1 | 1 | 1 | 1 | $8 \& 16$ |  |
| X | X | X | 0 | None |  |


| AD 7506 |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{~A}_{3}$ | $\mathrm{~A}_{2}$ | $\mathrm{~A}_{1}$ | $\mathrm{~A}_{0}$ | $\mathrm{E}_{\mathrm{N}}$ | "ON" |
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 2 |
| 0 | 0 | 1 | 0 | 1 | 3 |
| 0 | 0 | 1 | 1 | 1 | 4 |
| 0 | 1 | 0 | 0 | 1 | 5 |
| 0 | 1 | 0 | 1 | 1 | 6 |
| 0 | 1 | 1 | 0 | 1 | 7 |
| 0 | 1 | 1 | 1 | 1 | 8 |
| 1 | 0 | 0 | 0 | 1 | 9 |
| 1 | 0 | 0 | 1 | 1 | 10 |
| 1 | 0 | 1 | 0 | 1 | 11 |
| 1 | 0 | 1 | 1 | 1 | 12 |
| 1 | 1 | 0 | 0 | 1 | 13 |
| 1 | 1 | 0 | 1 | 1 | 14 |
| 1 | 1 | 1 | 0 | 1 | 15 |
| 1 | 1 | 1 | 1 | 1 | 16 |
| X | X | X | X | 0 | None |

## SWITCH SUMMARY

AD7510, AD7511
Quad SPST
Power Dissipation: $30 \mu \mathrm{~W}$
TTL/DTL/CMOS Direct Interface
"Break-Before-Make" Switching (AD7511)

## AD7512

Dual SPDT
TTL/DTL/CMOS Direct Interface Power Dissipation: $30 \mu \mathrm{~W}$


AD7510: Address "HIGH" closes switch

AD7511: Address "LOW" closes switch

Address "HIGH" makes S-1 to OUT-1 and S-3 to OUT-2

## AD7513

Dual SPST TTL/DTL/CMOS Direct Interface


Address "LOW" Closes
Switch

## AD7516

Quad SPST
Switching Time: 20ns
Power Dissipation: $10 \mu \mathrm{~W}$ CMOS Compatible


Address "HIGH" Closes Switch

AD7519
Quad SPDT Current Switch Switching Time: 20ns Power Dissipation: $8 \mu \mathrm{~W}$ CMOS Compatible


Address "HIGH" Steers Current to D3 buss

## ANALOG CMOS MULTIPLEXERS AD750I SERIES

## GENERAL DESCRIPTION

Analog Devices offers a complete line of monolithic CMOS analog multiplexers. They feature the industry's lowest power dissipation, and are directly interfaceable with DTL, TTL, and CMOS logic.
All utilize a high breakdown CMOS process in conjunction with a double layer interconnect, to obtain high density. Silicon Nitride passivation insures increased stability and reliability.

PERFORMANCE SELECTION TABLE ( $\mathrm{T}_{\mathrm{A}}=\boldsymbol{+ 2 5}{ }^{\circ} \mathrm{C}$ )

| Parameter | Units | AD7 501 <br> Commercial | AD7503 Military ${ }^{1}$ | AD7502 |  | AD7506 |  | AD7507 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Commercial | Military | Commercial | Military | Commercial | Military |
| $\begin{array}{r} \mathrm{R}_{\mathrm{ON}} \\ (\mathrm{MAX}) \\ \hline \end{array}$ | ohms | 300 |  | 300 |  | 450 | 400 | 450 | 400 |
| $\begin{gathered} \mathrm{I}_{\mathrm{S}} \\ (\mathrm{MAX}) \end{gathered}$ | nA | 2 | 0.5 | 2 | 0.5 | 5 | 1 | 5 | 1 |
| $\begin{gathered} \text { IOUT } \\ \text { (MAX) } \end{gathered}$ | nA | 10 | 5 | 5 | 3 | 20 | 10 | 10 | 5 |
| $\mathrm{t}_{\text {transition }}$ <br> (TYP) | $\mu \mathrm{s}$ | 0.8 |  | 0.8 |  | 0.7 |  | 0.7 |  |
| $\begin{gathered} \mathrm{I}_{\mathrm{DD}}{ }^{2} \\ (\mathrm{MAX}) \\ \hline \end{gathered}$ | mA | 0.5 |  | 0.5 |  | 1 |  | 1 |  |
| $\begin{aligned} & \mathrm{I}_{\mathrm{Ss}}{ }^{2} \\ & (\mathrm{MAX}) \end{aligned}$ | mA | 0.1 |  | 0.1 |  | 1 |  | 1 |  |

[^25]
## PIN CONFIGURATION <br> (TOP VIEW)

AD7501, AD7503


AD7506



PACKAGE INFORMATION
Suffix D - Ceramic DIP
Suffix N - Plastic DIP

## ORDERING INFORMATION

| Commercial Grade $\left(0^{\circ} \mathrm{C} \text { to }+75^{\circ} \mathrm{C}\right)$ | Price $(1-49)$ | Military Grade $\left(-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C}\right)$ | $\begin{aligned} & \text { Price } \\ & (1-49) \end{aligned}$ |
| :---: | :---: | :---: | :---: |
| AD7501JD* | \$28.00 |  |  |
| AD7501JN* | \$18.00 |  |  |
| AD7501KD | \$30.00 |  |  |
| AD7501KN | \$20.00 | AD7501SD | \$44.00 |
| AD7502JD* | \$28.00 |  |  |
| AD7502JN* | \$18.00 |  |  |
| AD7502KD | \$30.00 |  |  |
| AD7502KN | \$20.00 | AD7502SD | \$44.00 |
| AD7503JD* | \$28.00 |  |  |
| AD7503JN* | \$18.00 |  |  |
| AD7503KD | \$30.00 |  |  |
| AD7503KN | \$20.00 | AD7503SD | \$44.00 |
| AD7506JD* | \$38.00 |  |  |
| AD7506JN* | \$26.00 |  |  |
| AD7506KD | \$40.00 | AD7506SD* | \$76.00 |
| AD7506KN | \$28.00 | AD7506TD | \$80.00 |
| AD7507JD* | \$38.00 |  |  |
| AD7507JN* | \$26.00 |  |  |
| AD7507KD | \$40.00 | AD7507SD* | \$76.00 |
| AD7507KN | \$28.00 | AD7507TD | \$80.00 |

NOTE: *Requires püll-up resistor for TTL compatibility.

## ANALOGCMOS SWITCHES AD75IO SERIES

## GENERAL DESCRIPTION

A complete line of Dual and Quad analog switches offer extremely low quiescent power dissipation and TTL/DTL/CMOS compatibility. All are monolithic CMOS devices, and are capable of withstanding rugged environments.
They make excellent replacements for reed relays and FET switches, due to direct-logic interface capability, low power dissipation, and low price.
Applications range from sample/hold circuits to a myriad of analog control and/or signal routing functions. Low power requirements make them ideal for use in battery-operated equipment.

PERFORMANCE SELECTION TABLE ( $\mathrm{T}_{\mathrm{A}}=\boldsymbol{+ 2 5 ^ { \circ }} \mathbf{C}$ )

| Parameter | Units | AD7510 <br> Commercial | AD7511 <br> Military | AD7512 |  | AD7513 |  | AD7516 | AD7519 <br> Commercial |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Commercial | Military | Commercial | Military | Commercial Military |  |
| $\begin{gathered} \mathrm{R}_{\mathrm{ON}} \\ (\mathrm{MAX}) \end{gathered}$ | ohms |  | 0 |  | 0 | 80 | 70 | 400 | 100 |
| $\begin{gathered} \mathrm{I}_{\mathrm{D}}\left(\mathrm{I}_{\mathbf{S}}\right) \\ (\mathrm{MAX}) \end{gathered}$ | nA | 5 | 3 | 5 | 3 | 5 | 2 | $125^{\text { }}$ | -- |
| IOUT (MAX) | nA | - | - | 15 | 9 | - | - | -- | -- |
| $\begin{aligned} & \text { ton } \\ & (\mathrm{TYP}) \end{aligned}$ | $\mu \mathrm{s}$ | $\begin{gathered} 1 \mu \mathrm{~s}(\mathrm{AD} \\ 1.2 \mu \mathrm{~s} \text { ( } \mathrm{AI} \end{gathered}$ | $\begin{aligned} & 510) \\ & 7511) \end{aligned}$ |  |  |  |  | 0.02 | 0.02 |
| ${ }^{\text {tofF }}$ (TYP) | $\mu \mathrm{s}$ | $\begin{gathered} 1 \mu \mathrm{~s}(\mathrm{AD} \\ 0.8 \mu \mathrm{~s}(\mathrm{AI} \end{gathered}$ | $\begin{aligned} & 510) \\ & 7511) \end{aligned}$ |  |  |  |  | 0.02 | 0.03 |
| $\mathrm{t}_{\text {transition }}$ (TYP) | $\mu \mathrm{s}$ |  |  |  | 2 |  |  | -- | - |
| $\begin{aligned} & \mathrm{I}_{\mathrm{DD}}{ }^{2} \\ & (\mathrm{MAX}) \end{aligned}$ | mA |  |  |  | 5 | 1 | 1 | 0.0005 | 1 |
| $\begin{gathered} \mathrm{I}_{\mathrm{ss}}{ }^{2} \\ (\mathrm{MAX}) \end{gathered}$ | mA |  |  |  | 1 | 1 | 1 | 0.0005 | -- |
| Nominal Pwr. Supply | V |  |  |  |  |  | 5 V | $\begin{gathered} \left(\mathrm{V}_{\mathrm{DD}}-\mathrm{V}_{\mathrm{SS}}\right) \\ =15 \mathrm{~V} \end{gathered}$ | +8V |

[^26]
## PIN CONFIGURATIONS

(TOP VIEW)
AD7510, AD7511


AD7512


AD7516



AD7513


AD7 519


ORDERING INFORMATION

| Commercial Grade $\left(0^{\circ} \mathrm{C} \text { to }+75^{\circ} \mathrm{C}\right)$ | $\begin{aligned} & \text { Price } \\ & (1-49) \end{aligned}$ | Military Grade $\left(-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C}\right)$ | $\begin{gathered} \text { Price } \\ (1-49) \end{gathered}$ |
| :---: | :---: | :---: | :---: |
| AD7510JD* | \$13.00 |  |  |
| AD7510JN* | 8.00 |  |  |
| AD7510KD | 15.00 |  |  |
| AD75.10KN | 9.00 | AD7510SD | \$24.00 |
| AD7511JD* | \$13.00 |  |  |
| AD7511JN* | 8.00 |  |  |
| AD7511KD | 15.00 |  |  |
| AD7511KN | 9.00 | AD7511SD | \$24.00 |
| AD7512JD* | \$13.00 |  |  |
| AD7512JN* | 8.00 |  |  |
| AD7512KD | 15.00 | AD7512SD* | \$22.00 |
| AD7512KN | 9.00 | AD7512TD | 24.00 |
| AD7513JH* | \$ 4.80 |  |  |
| AD7513JN* | 4.80 |  |  |
| AD7513KH | 5.00 | AD7513SH* | \$12.30 |
| AD7513KN | 5.00 | AD7513TH | 12.50 |
| AD7516JN | \$ 2.43 | AD7516SD | \$ 7.75 |
| AD7519JN | \$ 5.00 |  |  |

NOTE: *Requires pull-up resistor for TTL compatibility.

# MONOLITHIC CMOS MULTIPLYING IO-\& I2-BIT D/A CONVERTERS AD7520 SERIES 

## GENERAL DESCRIPTION

The AD7520 is a low cost, monolithic 10 -bit multiplying D/A converter, packaged in a 16 -pin DIP. The AD7521 is a 12 -bit resolution multiplying D/A converter, packaged in an 18-pin DIP. Both devices use advanced monolithic CMOS and thin film technologies to provide up to 10 -bit differential linearity. The digital inputs directly interface to TTL, DTL, and CMOS logic.
The AD7520 and AD7521 operate from a +5 V to +15 V supply, and dissipate only 20 mW , including the ladder network.

PIN CONFIGURATION
(TOP VIEW)


PACKAGE INFORMATION
Suffix D - Ceramic DIP
Suffix N - Plastic DIP

| $0.2 \%$ Diff <br> Nonlinearity | Price <br> $(1-49)$ | $0.1 \%$ Diff <br> Nonlinearity | Price <br> $(1-49)$ | $0.05 \%$ Diff <br> Nonlinearity | Price <br> $(1-49)$ |
| :---: | ---: | :---: | :---: | :---: | ---: |
| AD7520JD | $\$ 20.75$ | AD7520KD | $\$ 29.50$ | AD7520LD | $\$ 39.50$ |
| AD7520JN | 15.75 | AD7520KN | 20.50 | AD7520LN | 27.00 |
| AD7521JD | $\$ 25.75$ | AD7521KD | $\$ 34.50$ | AD7521LD | $\$ 44.50$ |
| AD7521JN | 20.75 | AD7521KN | 25.50 | AD7521LN | 32.00 |


| Military Grades$\left(-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C}\right)$ |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0.2\% Diff <br> Nonlinearity | $\begin{gathered} \text { Price } \\ (1-49) \end{gathered}$ | 0.1\% Diff Nonlinearity | $\begin{gathered} \text { Price } \\ (1-49) \end{gathered}$ | 0.05\% Diff Nonlinearity | $\begin{gathered} \text { Price } \\ (1-49) \end{gathered}$ |
| AD7520SD | \$42.00 | AD7520TD | \$70.00 | AD7520UD | \$87.00 |
| AD7521SD | \$47.00 | AD7521TD | \$75.00 | AD7521UD | \$92.00 |

SPECIFICATIONS SUMMARY ( $\mathrm{V}_{\mathrm{DD}}=+15, \mathrm{~V}_{\text {REF }}=+10 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ unless otherwise noted $)$


## NOTES:

1. Full scale range (FSR) is 10 V for unipolar mode and $\pm 10 \mathrm{~V}$ for bipolar mode.
2. Using the internal $R_{\text {FEEDBACK }}$
3. Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.

## THIN FILM COATED SUBSTRATES ADI900 SERIES STANDARD PRODUCTS

## GENERAL DESCRIPTIONS

High precision thin film coated substrates, with proven reliability, are now available in production quantities. Sheet resistivities from 50 to $500 \mathrm{ohms} /$ square and sized from $0.025^{\prime \prime}(12.70 \mathrm{~mm})$ to $3.5^{\prime \prime}(88,90 \mathrm{~mm})$ square are available, that can accommodate $A L L$ bonding techniques. Three classes provide cost flexibility. USER DEFINED PARAMETERS CAN BE FABRICATED UPON REQUEST.

## THREE CLASSES AVAILABLE

CLASS $A$ - HIGH PRECISION HI-REL MIL CERTIFIABLE SUBSTRATES - For use in the most precise applications, and in cases where certification and traceability per MIL-STD-

9858 A is required. This class of material is useable in all hybrid designs.

CLASS B - INDUSTRIAL - COMMERCIAL PRODUCTION QUANTITY SUBSTRATES - For use in applications which do not require the high precision, certification or traceability of Class A substrates, but require consistent, reliable, repeatable performance in production to successfully fabricate thin film products.

CLASS C - EXPERIMENTAL - PROTOTYPE - TEST
USE SUBSTRATES - For use in applications that require the design advantages of nichrome thin films at lowest cost. Also, for use in feasibility studies, pilot runs, and design experimentation.

SPECIFICATIONS SUMMARY (typical @ $+25^{\circ} \mathrm{C}$ unless otherwise noted)

*Specifications same as for Class A.

## THREE FILM SYSTEM

1) NiCr resistive element
2) 1000-2000 Angstroms nickel barrier layer
3) $150 \mu$ inches ( 38,000 Angstroms) gold conductive layer Provides increased bonding strength for use with eutectic or solder reflow die bonding techniques.

## TWO FILM SYSTEM

1) NiCr resistive element
2) $150 \mu$ inches ( 38,000 Angstroms) gold conductive layer

Used with all wire bonding and epoxy die bonding techniques.

## BACKSIDE FILM SYSTEM

Identical to TWO FILM SYSTEM, and is suitable for all substrate bonding techniques.

## STANDARD OPTION SIZES

| SIZE - English Units (Metric Units) |  |
| :--- | :--- |
| ${ }^{\text {Option Number }}$ |  |
| $0.50^{\prime \prime} \times 0.50^{\prime \prime}(12,70 \times 12,70)$ | 025 |
| $1.00^{\prime \prime} \times 0.50^{\prime \prime}(25,40 \times 12,70)$ | 050 |
| $0.75^{\prime \prime} \times 0.75^{\prime \prime}(19,05 \times 19,05)$ | 056 |
| $1.00^{\prime \prime} \times 1.00^{\prime \prime}(25,40 \times 25,40)$ | 100 |
| $1.50^{\prime \prime} \times 1.00^{\prime \prime}(38,10 \times 25,40)$ | 150 |
| $2.00^{\prime \prime} \times 1.00^{\prime \prime}(50,80 \times 25,40)$ | 200 |
| $1.50^{\prime \prime} \times 1.50^{\prime \prime}(38,10 \times 38,10)$ | 225 |
| $3.00^{\prime \prime} \times 1.00^{\prime \prime}(76,20 \times 25,40)$ | 300 |
| $2.00^{\prime \prime} \times 2.00^{\prime \prime}(50,80 \times 50,80)$ | 400 |
| $3.00^{\prime \prime} \times 2.00^{\prime \prime}(76,20 \times 50,80)^{*}$ | 600 |
| $3.50^{\prime \prime} \times 3.50^{\prime \prime}(88,90 \times 88,90)^{* *}$ | 1225 |

*May have 2 plating clip marks $0.125^{\prime \prime}$ into one edge.
** $3.00^{\prime \prime} \times 3.00$ " $(76,20 \times 76,20)$ useable area only.

| Nominal Sheet <br> Resistivity <br> After Stabilization | Front <br> Side <br> Film <br> System | Model Number | Substrate <br> Thickness <br> (MILS $\pm$ <br> Tolerance) | Surface <br> Finish <br> (Microinches) <br> (RMS) | Back Side <br> Coated <br> With <br> Gold | CLA | A | PER SO CLA | UARE INC S B | CLA | S C |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (Ohms/Square) |  |  |  |  |  | 9-99 | 100-999 | 9-99 | 100-999 | 9-99 | 100-999 |
| 50 | 3 | AD1900 | $10 \pm 1$ | 3-4 | NO | \$6.45 | \$5.85 | \$5.45 | \$4.95 | \$4.10 | \$3.90 |
|  |  | AD1901 | $10 \pm 1$ | 3-4 | YES | \$8.95 | \$8.05 | \$6.75 | \$6.10 | \$5.00 | \$4.75 |
|  |  | AD1902 | $25 \pm 2$ | 5-10 | NO | \$5.50 | \$5.00 | \$4.00 | \$3.65 | \$3.00 | \$2.85 |
|  |  | AD1903 | $25 \pm 2$ | 5-10 | YES | \$8.00 | \$7.25 | \$6.00 | \$5.45 | \$4.50 | \$4.25 |
|  |  | AD1904 | $25 \pm 2$ | 3-4 | YES | \$9.00 | \$8.10 | \$6.80 | \$6.15 | \$5.05 | \$4.80 |
|  | 2 | AD1905 | $10 \pm 1$ | 3-4 | NO | \$5.80 | \$5.30 | \$4.90 | \$4.50 | \$3.70 | \$3.50 |
|  |  | AD1906 | $10 \pm 1$ | 3-4 | YES | \$8.05 | \$7.25 | \$6.10 | \$5.50 | \$4.50 | \$4.30 |
|  |  | AD1907 | $25 \pm 2$ | 5-10 | NO | \$4.95 | \$4.50 | \$3.60 | \$3.30 | \$2.70 | \$2.60 |
|  |  | AD1908 | $25 \pm 2$ | 5-10 | YES | \$7.20 | \$6.55 | \$5.40 | \$4.90 | \$4.05 | \$3.85 |
|  |  | AD1909 | $25 \pm 2$ | 3-4 | YES | \$8.15 | \$7.35 | \$6.20 | \$5.60 | \$4.60 | \$4.40 |
| 100 | 3 | AD1910 | $10 \pm 1$ | 3-4 | NO | \$5.85 | \$5.30 | \$4.25 | \$3.85 | \$3.15 | \$3.00 |
|  |  | AD1911 | $10 \pm 1$ | 3-4 | YES | \$8.35 | \$7.55 | \$6.00 | \$5.45 | \$4.50 | \$4.25 |
|  |  | AD1912 | $25 \pm 2$ | 5-10 | NO | \$5.00 | \$4.50 | \$3.60 | \$3.25 | \$2.70 | \$2.55 |
|  |  | AD1913 | $25 \pm 2$ | 5-10 | YES | \$7.50 | \$6.75 | \$5.40 | \$4.90 | \$4.05 | \$3.85 |
|  |  | AD1914 | $25 \pm 2$ | 3-4 | YES | \$8.40 | \$7.60 | \$6.05 | \$5.50 | \$4.55 | \$4.30 |
|  | 2 | AD1915 | $10 \pm 1$ | 3-4 | NO | \$5.30 | \$4.80 | \$3.80 | \$3.50 | \$2.85 | \$2.70 |
|  |  | AD1916 | $10 \pm 1$ | 3-4 | YES | \$7.50 | \$6.80 | \$5.40 | \$4.90 | \$4.05 | \$3.85 |
|  |  | AD1917 | $25 \pm 2$ | 5-10 | NO | \$4.50 | \$4.05 | \$3.25 | \$2.95 | \$2.45 | \$2.30 |
|  |  | AD1918 | $25 \pm 2$ | 5-10 | YES | \$6.75 | \$6.10 | \$4.90 | \$4.40 | \$3.65 | \$3.50 |
|  |  | AD1919 | $25 \pm 2$ | 3-4 | YES | \$7.55 | \$6.85 | \$5.45 | \$4.95 | \$4.10 | \$3.90 |
| 250 | 2 | AD1920 | $10 \pm 1$ | 3-4 | NO | \$4.75 | \$4.25 | \$3.40 | \$3.00 | \$2.60 | \$2.50 |
|  |  | AD1921 | $10 \pm 1$ | 3-4 | YES | \$7.00 | \$6.30 | \$5.05 | \$4.55 | \$3.85 | \$3.65 |
|  |  | AD1922 | $25 \pm 2$ | 5-10 | NO | \$4.05 | \$3.60 | \$2.95 | \$2.60 | \$2.20 | \$2.15 |
|  |  | AD1923 | $25 \pm 2$ | 5-10 | YES | \$6.30 | \$5.65 | \$4.55 | \$4.10 | \$3.50 | \$3.35 |
|  |  | AD1924 | $25 \pm 2$ | 3-4 | YES | \$7.05 | \$6.35 | \$5.10 | \$4.60 | \$3.90 | \$3.70 |
|  | 3 | AD1925 | $10 \pm 1$ | 3-4 | NO | \$5.25 | \$4.70 | \$3.80 | \$3.40 | \$2.85 | \$2.75 |
|  |  | AD1926 | $10 \pm 1$ | 3-4 | YES | \$7.75 | \$6.95 | \$5.60 | \$5.05 | \$4.25 | \$4.05 |
|  |  | AD1927 | $25 \pm 2$ | 5-10 | NO | \$4.50 | \$4.00 | \$3.25 | \$2.90 | \$2.45 | \$2.35 |
|  |  | AD1928 | $25 \pm 2$ | 5-10 | YES | \$7.00 | \$6.25 | \$5.05 | \$4.55 | \$3.85 | \$3.70 |
|  |  | AD1929 | $25 \pm 2$ | 3-4 | YES | \$7.05 | \$7.00 | \$6.05 | \$5.10 | \$4.30 | \$4.10 |
| 500 | 3 | AD1950 | $10 \pm 1$ | 3-4 | NO | \$5.25 | \$4.70 | \$3.80 | \$3.40 | \$2.85 | \$2.75 |
|  |  | AD1951 | $10 \pm 1$ | 3-4 | YES | \$7.75 | \$6.95 | \$5.60 | \$5.05 | \$4.25 | \$4.05 |
|  |  | AD1952 | $25 \pm 2$ | 5-10 | NO | \$4.50 | \$4.00 | \$3.25 | \$2.90 | \$2.45 | \$2.35 |
|  |  | AD1953 | $25 \pm 2$ | 5-10 | YES | \$7.00 | \$6.25 | \$5.05 | \$4.55 | \$3.85 | \$3.70 |
|  |  | AD1954 | $25 \pm 2$ | 3-4 | YES | \$7.80 | \$7.00 | \$5.65 | \$5.10 | \$4.30 | \$4.20 |
|  | 2 | AD1955 | $10 \pm 1$ |  | NO | \$4.75 | \$4.25 | \$3.45 | \$3.10 | \$2.60 | \$2.50 |
|  |  | AD1956 | $10 \pm 1$ | 3-4 | YES | \$7.00 | \$6.30 | \$5.05 | \$4.55 | \$3.85 | \$3.65 |
|  |  | AD1957 | $25 \pm 2$ | 5-10 | NO | \$4.05 | \$3.60 | \$2.95 | \$2.60 | \$2.20 | \$2.15 |
|  |  | AD1958 | $25 \pm 2$ | $5-10$ | YES | \$6.30 | \$5.65 | \$4.55 | \$4.10 | \$3.50 | \$3.35 |
|  |  | AD1959 | $25 \pm 2$ | 3-4 | YES | \$7.10 | \$6.40 | \$5.15 | \$4.65 | \$3.95 | \$3.75 |
| Conductor Only | 3 | AD1980 | $10 \pm 1$ | 3-4 | NO | \$4.25 | \$3.95 | \$3.35 | \$3.10 | \$2.75 | \$2.60 |
|  |  | AD1981 | $10 \pm 1$ | 3-4 | YES | \$6.75 | \$6.20 | \$5.30 | \$4.95 | \$4.35 | \$4.05 |
|  |  | AD1982 | $25 \pm 2$ | 5-10 | NO | \$3.50 | \$3.25 | \$2.75 | \$2.55 | \$2.25 | \$2.10 |
|  |  | AD1983 | $25 \pm 2$ | 5-10 | YES | \$6.00 | \$5.50 | \$4.75 | \$4.40 | \$3.85 | \$3.60 |
|  |  | AD1984 | $25 \pm 2$ | 3-4 | YES | \$6.80 | \$6.25 | \$5.35 | \$5.00 | \$4.40 | \$4.10 |
|  | 2 | AD1985 | $10 \pm 1$ | 3-4 | NO | \$3.85 | \$3.60 | \$3.00 | \$2.80 | \$2.50 | \$2.35 |
|  |  | AD1986 | $10 \pm 1$ | 3-4 | YES | \$6.10 | \$5.60 | \$4.80 | \$4.50 | \$3.90 | \$3.65 |
|  |  | AD1987 | $25 \pm 2$ | 5-10 | NO | \$3.15 | \$2.95 | \$2.50 | \$2.30 | \$2.05 | \$1.90 |
|  |  | AD1988 | $25 \pm 2$ | 5-10 | YES | \$5.40 | \$4.95 | \$4.30 | \$4.00 | \$3.50 | \$3.25 |
|  |  | AD1989 | $25 \pm 2$ | 3-4 | YES | \$6.20 | \$5.70 | \$4.90 | \$4.60 | \$4.00 | \$3.75 |

For larger quantity pricing and Class " C " availability, contact you local sales representative or factory direct.
Prices subject to change without notice

## ORDERING INFORMATION

Select part designation as in example: i.e., AD1925A/400


Class selected / Option Number

Prices are determined by multiplying the price per square inch times the total square inches purchased for each option selected. i.e.: AD1925A/400-100 pieces

$$
\begin{aligned}
& 100 \times\left(2.00^{\prime \prime} \times 2.00^{\prime \prime}\right)=400 \text { square inches of material } \\
& \text { Use } 100-999 \text { square inch price schedule } \\
& 4 \text { sq. in. } \times(\$ 4.70 / \text { sq. in. })=\$ 18.80 \text { per unit }
\end{aligned}
$$

MINIMUM ORDER - \$100.00 per option for standard options listed. For special chip sizes minimum order is $\$ 200.00$ per option. For Class C availability - contact sales office.

## USER DESIGNED THIN FILM PRECIRCUITS

## THE PRECIRCUIT-HYBRID MICROCIRCUIT INNOVATION

We are in the midst of an era some characterize as the "hybrid generation." The variety of applications open to hybrid assembly is growing rapidly. But, as the complexity and precision continue to increase, assembly alternatives quickly diminish. If you assemble hybrid circuits, Analog Devices' THIN FILM PRECIRCUIT offers you a solution that can greatly simplify your task:

- Procurement of the resistive elements as well as the mother board on a single chip.
- Precision (to $0.001 \%$ ) multi-element resistive chips for use in larger hybrid assemblies.
- Actively trimmable precision elements to eliminate trim potentiometers
- Combining the resistors, interconnects, I.C. bonding pads on one easily handled chip.
- Obtaining a single chip that can accommodate $A L L$ bonding techniques simultaneously. Locating a reliable source with sufficient capacity for multi-million piece deliveries.


## WHAT IS A PRECIRCUIT?

A PRECIRCUIT is a thin film resistor conductor pattern on a ceramic substrate, and may be used as a hybrid mother board, or as chips mounted upon a larger PRECIRCUIT. Included can be bonding pads for IC's pin outs and interconnects. (See photos).

## PRECIRCUIT DESIGN FLEXIBILITY

Great, a new way to assemble hybrids, but what can they do for you? Certainly there are competing technologies but, after reading the following highlights, you may discover that our PRECIRCUIT may in fact prove to be one of your better alternatives, AND IT IS AN AVAILABLE PROVEN PRODUCTION TOOL:

- HOW BIG? Available from $3.5^{\prime \prime}(88.9 \mathrm{~mm})$ to $0.025^{\prime \prime}$ ( 0.63 mm ) square either diced or as a scribed unbroken matrix. The chip can in fact include all the resistors, interconnects, bonding pads for IC chips and capacitors, etc., on a single chip.
- LOW COST: The cost of hybrid assembly can be reduced by using our multi-element PRECIRCUITS for fewer bonds, reduced number of chips to assemble, plus reduced procurement, inventory and test costs. Coupled with their moderate initial cost, the decreased assembly steps, increased reliability and increased yields often contribute to a lower full factory cost. In high performance applications, our PRECIRCUIT may in fact be the only acceptable way to achieve your design objectives.


## SUPERIOR PERFORMANCE

PERFORMANCE: In addition to other benefits, our thin film system offers exceptional performance (see specifications on adjacent page) in low cost readily assembled chip form:

- 6 orders of magnitude of resistance on a single chip from one film deposition.
- Excess noise to 50 dB below Johnson noise.
- Low interlead capacitance to 10 pF .
- High accuracy to $0.001 \%$.
- Temperature tracking to $0.5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$.
- Passivation for geatest mechanical protection.
- Meet or exceed all applicable portions of MIL-STD-883, Condition B.

In addition our PRECIRCUITS can accommodate virtually $A L L$ accepted hybrid assembly techniques - SIMULTANEOUSLY. A mother board fabricated on our 3-film system can accept:

- IC BONDING - - gold silicon eutectic, epoxy or solder reflow.
- INTERCONNECTS - - Conductive epoxy, solder reflow, dip soldering (passivated chips), gold thermocompression and aluminum ultrasonic wirebonding.
- FLIP CHIPS - ultrasonic or solder reflow.


## ACTIVELY TRIMMABLE ELEMENTS

Quite often, even though you design with high accuracy components, further active trimming is needed to "tweak" out accumulated circuit errors. Our PRECIRCUITS can be designed for low cost active trimming in your plant, eliminating the need for trim pots, or hand selected discretes. The trimmable elements can be fabricated on the hybrid mother board or on separate chips.

## PRODUCTION QUANTITIES

Typical delivery might be 1,000 pieces, 8 weeks after receipt of the order, and 50,000 pieces per month thereafter, depending on the properties of the configuration or the degree of selection required.
In addition, our PRECIRCUITS typically designed for use in analog signal-handling and conversion or in measurement and control, are backed by a sales-engineering staff with considerable successful experience in helping users with the applications of the op amps and switches you are likely to be marrying the PRECIRCUITS to. In this sense, Analog Devices makes "one-stop-shopping" both easy and practical.

SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ unless otherwise noted)

| Parameter | Units | Range of Values |
| :---: | :---: | :---: |
| ELECTRICAL |  |  |
| Conductive Element |  |  |
| Gold layer sheet resistivity | ohms/square | to 0.005 |
| Resistance Element |  |  |
| Sheet resistivity range | ohms/square | 50 to 500 |
| Resistance range on one chip | ohms | 6 orders of magnitude |
| Resistance tolerances | \% nominal | to 0.001 |
| Temperature Coefficient of Resistance |  |  |
| Absolute | $\mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | 0 to +75 |
| Tracking (between elements) | $\mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | 0 to $\pm 5$ |
| Voltage Coefficient of Resistance* | $\mu \mathrm{V} / \mathrm{V}$ | negligible |
| Voltage rating at rated dissipation** | V | $\sqrt{\text { W.R. }}^{* * *}$ |
| Interlead capacitance | pF | $<10$ |
| Excess noise (per MIL-STD-202D, | dB below |  |
| Method 308) | Johnson noise | 50 typical |
| Resistance load stability |  |  |
| @ $+25^{\circ} \mathrm{C}$ Absolute values | \% nominal/year | $\pm 0.05$ to $\pm 0.1$ |
| Ratio values | \% nominal/year | $\pm 0.005$ to $\pm 0.01$ |
| @ $+125^{\circ} \mathrm{C}$ Absolute values | \% nominal/1000h | $\pm 0.05$ to $\pm 0.1$ |
| Ratio values | \% nominal/1000h | $\pm 0.005$ to $\pm 0.01$ |
| Trim range-active or passive | ohms | To several orders of magnitude depedning upon design objective |


| PHYSICAL |  |  |
| :---: | :---: | :---: |
| Temperature Ranges |  |  |
| Lead soldering-60 second max | ${ }^{\circ} \mathrm{C}$ | to 300 |
| Operating | ${ }^{\circ} \mathrm{C}$ | -55 to +125 |
| Storage | ${ }^{\circ} \mathrm{C}$ | -65 to +150 |
| Substrate Dimensions (99.5\% $\mathrm{AL}_{2} \mathrm{O}_{3}$ ) |  |  |
| Thickness | mils (mm) | 10(.25), 15(.38), 20(.51), 25(.64) |
| Chip sizes | inches (mm) | .025(.63) to 3.5(.89) square |
| Precircuit Dimensions |  |  |
| Conductor element width | inches (mm) | to 0.002 (0.051) |
| Resistor element width | inches (mm) | to 0.001 (0.025) |
| Element dimensional tolerance | inches (mm) | to $0.0001(0.0025)$ |
| Substrate surface finish | $\mu$ inch ( $\mu \mathrm{m}$ ) | $\begin{aligned} & \text { unglazed to } 3(7.62) \\ & \text { glazed }<1(<2.54) \end{aligned}$ |

## FILM SYSTEMS

2 Film System - NiCr, $150 \mu$ inches ( $381 \mu \mathrm{~m}$ ) gold conductor layer.
3 Film System - NiCr, $6.7 \mu \mathrm{~m}$ Nickel barrier layer, $150 \mu$ inches $(381 \mu \mathrm{~m})$ gold conductor layer.
Backside - Same as 2 Film System (if required).

## BONDING TECHNIQUES

Wire Bonding - Gold thermo compression, aluminum ultrasonic, soldering, conductive epoxy
Die Bonding - Gold-Silicon eutectic, epoxy, solder reflow

## MIL CERTIFICATION

Lot traceability, lot qualification, film adhesion, bondability, visual criteria meet or exceed applicable MIL standards (i.e., MIL-STD-883, MIL-Q-9858A)

PASSIVATION - Passivated chips available.

[^27]
## CUSTOM THIN FILM RESISTOR NETWORKS

## THIN-FILM RESISTOR NETWORKS

Packaged thin-film resistor networks are rapidly increasing in popularity for precise instrumentation and data-handling circuitry. Analog Devices makes available two ways that users can benefit by this new techno'ogy. In addition to a growing line of standard resistor networks, we can provide made-to-order networks as a convenience for designers of moderate-to-highprecision circuits.

The low cost in quantity, range of tracking tolerances from $1 \%$ to better than $0.001 \%$, availability in convenient standard IC packages or chip form, and high reliability (with MIL-STD-883 documentation, if necessary), provide circuit and system designers with a ready cure for design headaches associated with circuits requiring resistors that are accurately related in value. Custom circuits can reduce production costs due to overspecifying, matching, and "tweaking," and allow you to provide your customers with compact, reliable, competitive circuits, instruments, apparatus, and systems.
You can benefit by the use of these networks if you design and manufacture (or assemble in quantity):

- Multiple op-amp circuits that require stable gain and summation relationships over wide temperature ranges
- D/A and A/D converters, especially in applications where the resistive ladder network is the limiting factor on performance over wide temperature ranges
- Circuits involving programmable gains or voltage ratios, whether manually or remotely controlled
- Stable voltage sources or accurate voltage-measurement circuits
- Any circuit with performance that depends critically on relationships among two or more resistors.


## WHY THIN FILM?

The principal choice of network construction is between thickfilm and thin-film technologies. Where excellent long-term stability, small size, wide range of on-chip resistance values (e.g., $10 \Omega$ to $10 \mathrm{M} \Omega$ in a single package), and high performance over a wide range of environmental conditions are necessary, thinfilm networks are usually preferable to thick films; at the highest accuracy levels, thin films are just about the only practical choice.
Analog's custom thin-film networks are characterized by excellent ratio match (to $0.001 \%$ ), absolute accuracy (to $0.005 \%$ ), low temperature coefficients (tracking to as low as $0.5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ ), low "excess" noise ( 35 dB below Johnson noise), low drift (to $0.01 \% /$ year at $+25^{\circ} \mathrm{C}$ ), and zero voltage coefficient (except possibly for self-heating effects).

## CUSTOM NETWORKS vs. DISCRETE RESISTORS

You can, of course, specify discrete resistors to a sufficient degree of accuracy, then test, grade, select, match, and/or "tweak" them; but, for one or more of the following reasons, circuit designers increasingly choose resistor networks in preference to assemblies of matched discrete resistors:

- Performance: In addition to excellent resistance matching, temperature tracking, and uniform behavior (usually more important than absolute resistance value), the small size of monolithic (single substrate) construction tends to maintain all resistors at the same temperature, despite gradients in the external environment.
- Convenience: The entire monolithic network can be specified, purchased, and used as a single component, like an IC, greatly simplifying the process of buying, testing, keeping-track-of, and assembling matched elements.
- Small size . . . and if the standard IC packages aren't small enough, the networks are also available as chips for hybrid assembly.
- Low cost: Their initial moderate cost, plus the savings in the areas of purchasing, inventory, assembly, and test, make these thin-film networks highly competitive with do-it-yourself resistor ássemblies, even in some lowerperformance applications, though the cost of the discrete resistors by themselves may seem significantly less. In very high-performance applications, the tolerances required for individual high-precision resistors in order to ensure reasonable tracking over a wide temperature range make discretes considerably more costly than thinfilm networks of comparable ratio performance.


## EASY TO SPECIFY

Just about all the information we need to design a typical custom network can be provided by requesting a specification guide, or contacting your local sales engineer.
The information required is straightforward. In fact, the design for optimum dissipation characteristics does not require that you add a "standard" dissipation tolerance. Just indicate the expected actual maximum dissipation for each element, and for the network as a whole. Unlike discretes, each of which requires a separate dissipation spec, a thin-film network is designed with average dissipation-density such that the entire substrate tends to run at a uniform temperature. This requirement can be met by proper layout, which is facilitated by the information you provide about typical and maximum dissipations of (or voltages across) each element, in both transient and steady states.

## DESIGN CRITERIA AND SPECIFICATIONS

PACKAGE DESCRIPTIONS (For information on packages not listed here contact sales office.)

| Package <br> Configuration | TO <br> Designation | Drawing <br> Number | Cavity Size <br> (Inches) | Maximum Packaged <br> Resistance <br> (Megohms) | Maximum Package <br> Power Dissipation <br> (Watts)* |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Circular Can "H" |  |  |  |  |  |
| 8 Lead | TO-99 | $40-100611$ | $0.145 \times 0.145$ | 2.3 | 0.5 |
| 10 Lead | TO-100 | $40-100610$ | $0.150 \times 0.180$ | 3.0 | 0.5 |
| Dual-In-Line "D" |  |  |  |  |  |
| 14 Lead |  | $40-100433$ | $0.140 \times 0.240$ | 4.0 | 0.6 |
| 16 Lead | TO-116 | $40-100269$ | $0.210 \times 0.160$ | 4.0 | 0.6 |
| 24 Lead |  | $40-100525$ | $0.200 \times 0.200$ | 5.0 | 1.0 |
| Flat Packs "F" |  |  |  |  |  |
| 14 Lead |  | $40-100435$ | $0.150 \times 0.280$ | 6.0 | 0.5 |
| 14 Lead | TO-87 | $40-100029$ | $0.275 \times 0.280$ | 15.0 | 1.0 |
| 16 Lead |  | $40-100474$ | $0.150 \times 0.280$ | 6.0 | 0.5 |
| Modified Dual-In- |  |  |  |  |  |
| Line "B" |  |  |  | 30.0 | 2.0 |
| 16 Lead |  | $40-100456$ | $0.270 \times 0.750$ | 35.0 |  |
| 18 Lead | $40-100612$ | $0.270 \times 0.850$ | 3.0 |  |  |
| 24 Lead |  | $40-100701$ | $0.270 \times 1.150$ | 44.0 | 3.0 |

${ }^{*}$ Maximum Power Dissipation Allowable at $+125^{\circ} \mathrm{C}$ Case Temperature, Derate to 0 mW at $+150^{\circ} \mathrm{C}$.

GENERAL SPECIFICATIONS (@ $+25^{\circ} \mathrm{C}$, unless otherwise noted)

|  |  | Min | Typ | Max |
| :---: | :---: | :---: | :---: | :---: |
| Temperature Coefficient of Resistance (TCR) Absolute <br> Tracking (Between Elements) | $\begin{aligned} & \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ & \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\ & \hline \end{aligned}$ | 0 0 | $\begin{aligned} & +50 \\ & \pm 1 \end{aligned}$ | $\begin{aligned} & +75 \\ & \pm 5 \end{aligned}$ |
| Resistance Load Stability at Rated Power* <br> @ $+25^{\circ} \mathrm{C}$ Absolute Values <br> Ratio Values <br> @ $+125^{\circ} \mathrm{C}$ Absolute Values <br> Ratio Values | \% Nominal/Year <br> \% Nominal/Year <br> \% Nominal/1000h <br> \% Nominal/1000h |  | $\begin{aligned} & \pm 0.05 \\ & \pm 0.005 \\ & \pm 0.05 \\ & \pm 0.005 \end{aligned}$ | $\begin{aligned} & \pm 0.1 \\ & \pm 0.01 \\ & \pm 0.1 \\ & \pm 0.01 \end{aligned}$ |
| Voltage Coefficient of Resistance** | $\mu \mathrm{V} / \mathrm{V}$ |  |  | Negligible |
| Excess Noise (per MIL-STD-202D, Method 308) | dB Below Johnson Noise |  | 50 | 35 |
| Interlead Capacitance | pF |  |  | <10 |
| Voltage Rating at Rated Dissipation* | V |  |  | $\sqrt{\mathrm{W} . \mathrm{R}}^{* * *}$ |
| Temperature Ratings <br> Storage <br> Lead Soldering for 60s Maximum | ${ }^{\circ}{ }^{\circ} \mathrm{C}$ | -65 | +25 | $\begin{array}{r} +150 \\ +300 \\ \hline \end{array}$ |

*Power Rating specified at $+125^{\circ} \mathrm{C}$ for individual resistors or devices is derated to 0 mW at $+150^{\circ} \mathrm{C}$.
**None measurable (per MIL-STD-202D, Method 309) except for changes caused by self-heating
of the network due to dissipation as a function of voltage.
***Where W is Power (watts) and R is Resistance (ohms).
POWER DISSIPATION IS GOVERNED BY LAYOUT RULES APPLICABLE TO PACKAGE CAVITY AREA AVAILABLE.
NETWORKS AVAILABLE IN COMMERCIAL ( $0 \mathrm{TO}+70^{\circ} \mathrm{C}$ ) AND MIL $\left(-55^{\circ} \mathrm{C} T \mathrm{O}+125^{\circ} \mathrm{C}\right)$ VERSIONS.
OPTION 883 AVAILABLE - SEE PAGE 182 (MIL-STD-883 SCREENING)

## GENERAL PURPOSE PRECISION RESISTOR NETWORKS

## GENERAL DESCRIPTION

The circuits shown here are representative examples chosen from among the numerous high-precision thin-film resistor networks manufactured by the Resistor Products Division of Analog Devices.

These resistor networks are especially useful in data-handling systems, with specific applications ranging from pre-amplifiers and signal conditioners to precision attenuators and dataconversion circuits. A wide variety of stable, fast, versatile, accurate, and reliable operational configurations can be easily assembled by combining these resistance networks with Analog Devices CMOS switches and operational amplifiers.
Available in standard housing, including cans, flatpacks, and dual-in-line packages (as well as in chip form for hybrid assembly), these resistor networks are fabricated from our own coated substrates; thus the entire process is under our control. Valuable benefits include the advantages of high-yield batchprocessing techniques, high-volume assembly, and automatic laser-trimming, all of which contribute to high performance and reliability, plus efficient use of board space, at low cost.

## Why Thin Film?

Where excellent long-term stability, small size, wide range of on-chip resistance values, and high performance over a wide range of environmental conditions are necessary, thin-film resistance networks are usually preferable to thick-film; at the highest accuracy levels, they are just about the only practical choice.

## Resistor Networks vs. Discrete Resistors

For one or more of the following reasons, circuit designers increasingly choose resistor networks in preference to assemblies of matched discrete resistors.
Performance: In addition to excellent resistance matching, temperature tracking, and uniform behavior (usually more important than absolute resistance value), the small size of monolithic (single substrate) construction tends to maintain all resistors at the same temperature, despite gradients in the external environment.

Convenience: The entire monolithic network can be specified, purchased, and used as a single component, like an I.C., greatly simplifying the process of buying, testing, keeping-track-of, and assembling matched elements.
Small Size: . . . and if the standard I.C. packages aren't small enough, the networks are also available as chips for hybrid assembly.
Low Cost: Their initial moderate cost, plus the savings in the areas of purchasing, inventory, assembly, and test, makes these thin-film networks highly competitive with do-it-yourself resistor assemblies, even in some lower-performance applications, though the cost of the discrete resistors alone may be significantly less.

SPECIFICATIONS SUMMARY (Typical @ $+25^{\circ} \mathrm{C}$ unless otherwise noted)

|  | Units | Min | Typ | Max |
| :--- | :--- | :--- | :--- | :--- |
| Temperature Coefficient of Resistance (TCR) <br> Absolute |  |  |  |  |
| Tracking (Between Elements) | $\mathrm{ppm} /{ }^{\circ} \mathrm{C}$ <br> $\mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | 0 | +50 | +75 |
| Resistance Load Stability at Rated Power* <br> @ $+25^{\circ} \mathrm{C}$ <br>  <br> Absolute Values <br> Ratio Values |  | 0 | $\pm 1$ | $\pm 2$ |

${ }^{*}$ Power Rating specified at $+125^{\circ} \mathrm{C}$ for individual resistors or devices is derated to 0 mW at $+150^{\circ} \mathrm{C}$.
**None measurable (per MIL-STD-202D, Method 309) except for changes caused by self-heating of
the network due to dissipation as a function of voltage.
${ }^{* * *}$ Where W is equal to power (watts) and R is equal to resistance (ohms).

## ATTENUATOR/DIVIDER NETWORKS

## AD1800-QUAD DIVIDER/FEEDBACK NETWORK-"D" PACKAGE



| Model | Parameter | Units | R1 | R2 | R3 | R4 | R5 | R6 | R7 | R8 | R9 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| AD1800-1 | R Value | - | R | R | R | R | R | R | R | R | R |
| $\mathrm{AD} 1800-2$ | R Value | - | 0.99 R | R | 0.99 R | R | 0.99 R | R | 0.99 R | R | R |
| Both <br> Models | Reference <br> Resistor | - | R 2 | - | R 4 | - | R 6 | - | R 8 | - | R 8 |
| Both <br> Models | Power <br> Dissipation | mW | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 |

"R" Values (ohms) Available: 2k, 5k, 10k, 20k, 50k, 100k, 200k
Absolute Accuracy: $\pm 1.0 \%$; Ratio Accuracies: $\pm 1 \%$ to $\pm 0.01 \%$

## AD1803-DECADE DIVIDER-"B" PACKAGE



| Model | Parameter | Units | R1 | R2 | R3 | R4 | R5 | R6 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| AD1803-1 | Resistance | ohms | 100 | 900 | 9 k | 90 k | 900 k | $9 \mathrm{M}^{*}$ |
|  | Power Dissipation | mW | 40 | 40 | 20 | 10 | 100 | 440 |
| AD1803-2 | Resistance | ohms | - | 1 k | 9 k | 90 k | 900 k | $9 \mathrm{M}^{*}$ |
|  | Power Dissipation | mW | - | 45 | 20 | 10 | 100 | 440 |
| AD1803-3 | Resistance | ohms | - | - | 10 k | 90 k | 900 k | $9 \mathrm{M}^{*}$ |
|  | Power Dissipation | mW | - | - | 22 | 10 | 100 | 440 |
| AD1803-4 | Resistance | ohms | 100 | 900 | 9 k | 90 k | $900 \mathrm{k}^{*}$ | - |
|  | Power Dissipation | mW | 40 | 40 | 20 | 10 | 100 | - |
| AD1803-5 | Resistance | ohms | - | 1 k | 9 k | 90 k | $900 \mathrm{k}^{*}$ | - |
|  | Power Dissipation | mW | - | 45 | 40 | 10 | 100 | - |

*Reference Resistor. Absolute accuracy $\pm 1 \%$.
Ratio Accuracies $\pm 1 \%$ to $\pm 0.01 \%$. Max. applied voltage pins 8 to 15 is 2000 volts.
TCR Tracking: $\pm 1 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ typical, $\pm 5 \mathrm{ppm} /{ }^{\prime} \mathrm{C}$ maximum.

## AD1805-DUAL DIVIDER-"H" PACKAGE



| PARAMETER | UNITS | R1 | R2 | R3 | R4 |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Resistance | ohms | R | R | R | R |
| REF. R | - | - | R1 | - | R3 |
| Power Dissipation | mW | 100 | 100 | 100 | 100 |

"R" Values (ohms) Available: 2k, 5k, 10k, 20k, 50k, 100k, 200k
Reference Resistor (REF. R): $\pm 1 \%$ Absolute
Ratio Accuracies: $\pm 1 \%$ to $\pm 0.01 \%$

## AD1807-BINARY ATTENUATOR NETWORK-"D" PACKAGE


("F" Package Available - contact sales office)

AD 1807 SERIES PARAMETERS

| Parameter | Units | $\mathrm{R}_{1}{ }^{\text { }}$ | $\mathrm{R}_{2}$ | $\mathbf{R}_{3}$ | $\mathrm{R}_{4}$ | R5 | $\mathrm{R}_{6}$ | $\mathrm{R}_{7}$ | $\mathrm{R}_{8}$ | R9 | $\mathrm{R}_{10}$ | $\mathrm{R}_{11}$ | $\mathrm{R}_{12}$ | $\mathrm{R}_{13}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| "R" Value | - | R/2 | R/4 | R/8 | R/16 | R/32 | R/64 | R/128 | R/256 | R/512 | R/1024 | R/1024 | R/1024 | R/1024 |
| Approx. <br> Decimal <br> Equivalent |  | .50R | .25R | .125R | . 063 R | . 031 R | . 016 R | .008R | .004R | .002R | .001R | . 001 R | . 001 R | .001R |
| Power <br> Dissipation | mW** | 100 | 50 | 50 | 25 | 25 | 25 | 25 | 25 | 25 | 25 | 25 | 25 | 25 |
| Ratio Accuracy |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| H, Q | \% | - | $\pm 1$ | $\pm 1$ | $\pm 1$ | $\pm 1$ | $\pm 1$ | $\pm 1$ | $\pm 1$ | $\pm 2$ | $\pm 5$ | $\pm 5$ | $\pm 5$ | $\pm 5$ |
| J, S | \% | - | $\pm .1$ | $\pm .1$ | $\pm .1$ | $\pm .1$ | $\pm .2$ | $\pm .4$ | $\pm .8$ | $\pm 1.6$ | $\pm 3.2$ | $\pm 3.2$ | $\pm 3.2$ | $\pm 3.2$ |
| L, U | \% | - | $\pm .01$ | $\pm .02$ | $\pm .05$ | $\pm .10$ | $\pm .2$ | $\pm .4$ | $\pm .8$ | $\pm 1.6$ | $\pm 3.2$ | $\pm 3.2$ | $\pm 3.2$ | $\pm 3.2$ |

- Reference Resistor - absolute accuracy $\pm 1 \%$
- Milliwatts at $+125^{\circ} \mathrm{C}$ derated to 0 mW at $+150^{\circ} \mathrm{C}$
"R" values available of $10 \mathrm{k}, 25 \mathrm{k}, 50 \mathrm{k}, 100 \mathrm{k}, 250 \mathrm{k}, 500 \mathrm{k}, 1 \mathrm{M}$


## CIRCUIT ELEMENT NETWORKS

## AD1830-EQUAL INDEPENDENT RESISTORS-"D" PACKAGE


("F" Package Available - contact sales office)

## AD1830 Family Specifications

Power Dissipation Per Resistor 100 mW Max.
Per Package 500mW Max.
Ratio Accuracies Available $\pm 1.0 \%$ to $\pm 0.01 \%$.
"R" Values Available (ohms) $0.05 \mathrm{k}, 0.10 \mathrm{k}, 0.25 \mathrm{k}, 0.50 \mathrm{k}, 1 \mathrm{k}, 2.5 \mathrm{k}$, $5 \mathrm{k}, 10 \mathrm{k}, 25 \mathrm{k}, 50 \mathrm{k}, 100 \mathrm{k}, 250 \mathrm{k}, 500 \mathrm{k}$
*Reference Tolerance $\pm 1 \%$ except $\pm 0.1 \%$ for $\pm 0.1 \%$ and $\pm 0.01 \%$ ratio accuracy options.

## AD1840-DUAL AMPLIFIER NETWORK-"D" PACKAGE


("F" Package Available - contact sales office)

| Parameter | Units | R1 | R2 | R3 | R4 | R5 | R6 | R7 | R8 | R9 | R10 | R11 | R12 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| Resistance | ohms | R | R | R | R | $5 R$ | $5 R$ | $5 R$ | $5 R$ | R | R | R | R |
| REF. R | - | - | R1 | R1 | R1 | R1 | R1 | R12 | R12 | R12 | R12 | R12 | - |
| PWR. Dissip. | mW | 50 | 50 | 50 | 50 | 100 | 100 | 50 | 50 | 50 | 50 | 100 | 100 |

"R" Values (ohms): 1k, 2k, 5k, 10k, 20k, 50k, 100k
Reference Resistor (REF. R): $\pm 1 \%$ Absolute

## AD1841-DUAL AMPLIFIER NETWORK-"D" PACKAGE



| PARAMETER |  | UNITS | $\begin{aligned} & \text { R1 } \\ & \text { R14 } \end{aligned}$ | $\begin{aligned} & \mathbf{R} 2 \\ & \mathbf{R} 13 \end{aligned}$ | $\begin{aligned} & \text { R3, R4, } \\ & \text { R12, R11 } \end{aligned}$ | $\begin{aligned} & \text { R5 } \\ & \text { R10 } \end{aligned}$ | $\begin{aligned} & \text { R6 } \\ & \text { R9 } \end{aligned}$ | $\begin{aligned} & \text { R7 } \\ & \text { R8 } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Resistance |  | ohms | 0.5R | 0.3 R | 0.1 R | R | 9R | 90R |
| Power Dissipation |  | mW | 100 | 100 | 100 | 100 | 75 | 50 |
| Ratio <br> Accuracy | H, Q | \% | $\pm 1$ | $\pm 1$ | $\pm 2$ | - | $\pm 1$ | $\pm 1$ |
|  | J, S | \% | $\pm 0.1$ | $\pm 0.1$ | $\pm 0.2$ | - | $\pm 0.1$ | $\pm 0.1$ |
|  | $\mathrm{L}, \mathrm{U}$ | \% | $\pm 0.01$ | $\pm 0.01$ | $\pm 0.02$ | - | $\pm 0.01$ | $\pm 0.01$ |

Reference "R": R5 for R1-R7; R10 for R8-R14: $\pm 1 \%$ Absolute.
" $R$ " Values (ohms) Available: 1k, 2k, 5k, 10k

## AD1842-SUMMING NETWORK-"D" PACKAGE


("F" Package Available - contact sales office)

R1 thru R13 = "R" Values
*Denotes Reference Resistor: $\pm 1 \%$ Absolute Power Dissipation: 50 mW per Resistor
"R" Values (ohms) Available: $0.05 \mathrm{k}, 0.1 \mathrm{k}, 0.25 \mathrm{k}, 0.5 \mathrm{k}$,
$1 \mathrm{k}, 2.5 \mathrm{k}, 5 \mathrm{k}, 10 \mathrm{k}, 25 \mathrm{k}, 50 \mathrm{k}, 100 \mathrm{k}, 250 \mathrm{k}$

## PRICING AND ORDERING INFORMATION GENERAL PURPOSE PRECISION RESISTOR NETWORKS

## ORDERING INFORMATION

Accuracy/Environmental Class Designations

| Ratio Accuracy ${ }^{1} \rightarrow$ | $\pm 1 \%$ | $\pm 0.1 \%$ | $\pm 0.01 \%$ |
| :---: | :--- | :--- | :--- |
| 0 to $+70^{\circ}$ C Operating Range | H | J | L |
| $-55^{\circ} \mathrm{C}$ to $+125{ }^{\circ} \mathrm{C}$ Operating Range | Q | S | U |

## SPECIFYING INFORMATION

For Example, AD1800JD-1/10k


DOMESTIC PRICES ${ }^{2}$

|  |  | 1800 |  | 1803 |  | 1805 | 1807 | 1830 | 1840 | 1841 | 1842 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Accuracy Designation | Quantity | $\begin{aligned} & -1 \\ & -2 \end{aligned}$ | -1 | $\begin{aligned} & -2 \\ & -3 \end{aligned}$ | $\begin{aligned} & -4 \\ & -5 \end{aligned}$ |  |  |  |  |  |  |
| $\begin{gathered} \mathrm{H} \\ (\mathrm{Q})^{3} \end{gathered}$ | 1-24 | $\begin{aligned} & \$ 7.00 \\ & (8.00) \end{aligned}$ | $\begin{aligned} & \$ 10.00 \\ & (15.00) \end{aligned}$ | $\begin{aligned} & \$ 8.50 \\ & (14.50) \end{aligned}$ | $\begin{aligned} & \$ 7.00 \\ & (14.00) \end{aligned}$ | $\begin{aligned} & \$ 3.00 \\ & (3.50) \end{aligned}$ | $\begin{aligned} & \$ 8.50 \\ & (10.80) \end{aligned}$ | $\begin{aligned} & \$ 6.00 \\ & (7.00) \end{aligned}$ | $\begin{aligned} & \$ 6.90 \\ & (10.30) \end{aligned}$ | $\begin{aligned} & \$ 7.20 \\ & (10.60) \end{aligned}$ | $\begin{aligned} & \$ 7.00 \\ & (10.40) \end{aligned}$ |
|  | 25-99 | $\begin{aligned} & \$ 5.25 \\ & (6.25) \end{aligned}$ | $\begin{aligned} & \$ 8.50 \\ & (12.50) \end{aligned}$ | $\begin{aligned} & \$ 7.00 \\ & (12.00) \end{aligned}$ | $\begin{aligned} & \$ 6.50 \\ & (11.50) \end{aligned}$ | $\begin{aligned} & \$ 2.50 \\ & (3.00) \end{aligned}$ | $\begin{aligned} & \$ 7.00 \\ & (8.90) \end{aligned}$ | $\begin{aligned} & \$ 4.25 \\ & (5.25) \end{aligned}$ | $\begin{aligned} & \$ 5.70 \\ & (8.50) \end{aligned}$ | $\begin{aligned} & \$ 5.95 \\ & (8.75) \end{aligned}$ | $\begin{aligned} & \$ 5.75 \\ & (8.60) \end{aligned}$ |
|  | 100-499 | $\begin{aligned} & \$ 3.00 \\ & (4.00) \end{aligned}$ | $\begin{aligned} & \$ 7.50 \\ & (11.50) \end{aligned}$ | $\begin{aligned} & \$ 6.00 \\ & (11.25) \end{aligned}$ | $\begin{aligned} & \$ 5.75 \\ & (11.00) \end{aligned}$ | $\begin{aligned} & \$ 1.90 \\ & (2.40) \\ & \hline \end{aligned}$ | $\begin{aligned} & \$ 5.20 \\ & (6.60) \end{aligned}$ | $\begin{aligned} & \$ 3.00 \\ & (4.00) \end{aligned}$ | $\begin{aligned} & \$ 4.25 \\ & (6.30) \end{aligned}$ | $\begin{aligned} & \$ 4.40 \\ & (6.50) \end{aligned}$ | $\begin{aligned} & \$ 4.30 \\ & (6.40) \end{aligned}$ |
| $\begin{gathered} \mathrm{J} \\ (\mathrm{~S})^{3} \end{gathered}$ | 1-24 | $\begin{aligned} & \$ 9.00 \\ & (10.00) \end{aligned}$ | $\begin{aligned} & \$ 12.00 \\ & (17.00) \end{aligned}$ | $\begin{aligned} & \$ 11.50 \\ & (16.50) \end{aligned}$ | $\begin{aligned} & \$ 11.00 \\ & (16.00) \end{aligned}$ | $\begin{aligned} & \$ 3.25 \\ & (4.25) \end{aligned}$ | $\begin{aligned} & \$ 9.50 \\ & (12.75) \end{aligned}$ | $\begin{aligned} & \$ 8.00 \\ & (9.00) \end{aligned}$ | $\begin{aligned} & \$ 10.60 \\ & (14.85) \end{aligned}$ | $\begin{aligned} & \$ 10.60 \\ & (14.85) \end{aligned}$ | $\begin{aligned} & \$ 10.00 \\ & (14.85) \end{aligned}$ |
|  | 25-99 | $\begin{aligned} & \$ 7.25 \\ & (8.25) \end{aligned}$ | $\begin{aligned} & \$ 10.50 \\ & (14.50) \end{aligned}$ | $\begin{aligned} & \$ 10.00 \\ & (14.00) \end{aligned}$ | $\begin{aligned} & \$ 9.50 \\ & (13.50) \end{aligned}$ | $\begin{aligned} & \$ 2.75 \\ & (3.50) \end{aligned}$ | $\begin{aligned} & \$ 7.90 \\ & (10.50) \end{aligned}$ | $\begin{aligned} & \$ 6.25 \\ & (8.25) \end{aligned}$ | $\begin{aligned} & \$ 8.75 \\ & (12.25) \end{aligned}$ | $\begin{aligned} & \$ 8.75 \\ & (12.25) \end{aligned}$ | $\begin{aligned} & \$ 8.75 \\ & (12.25) \end{aligned}$ |
|  | 100-499 | $\begin{aligned} & \$ 5.00 \\ & (6.00) \end{aligned}$ | $\begin{aligned} & \$ 8.50 \\ & (13.00) \\ & \hline \end{aligned}$ | $\begin{aligned} & \$ 8.25 \\ & (12.75) \\ & \hline \end{aligned}$ | $\begin{aligned} & \$ 8.00 \\ & (12.50) \end{aligned}$ | $\begin{aligned} & \$ 2.10 \\ & (2.75) \\ & \hline \end{aligned}$ | $\begin{aligned} & \$ 5.90 \\ & (7.80) \\ & \hline \end{aligned}$ | $\begin{aligned} & \$ 4.50 \\ & (5.50) \\ & \hline \end{aligned}$ | $\begin{aligned} & \$ 6.50 \\ & (9.10) \\ & \hline \end{aligned}$ | $\begin{aligned} & \$ 6.50 \\ & (9.10) \\ & \hline \end{aligned}$ | $\begin{aligned} & \$ 6.50 \\ & (9.10) \\ & \hline \end{aligned}$ |
| L $(U)^{3}$ | $1-24$ | $\begin{aligned} & \$ 15.00 \\ & (16.75) \end{aligned}$ | $\begin{aligned} & \$ 23.00 \\ & (27.00) \end{aligned}$ | $\begin{aligned} & \$ 20.00 \\ & (24.00) \end{aligned}$ | $\begin{aligned} & \$ 19.00 \\ & (23.00) \end{aligned}$ | $\begin{aligned} & \$ 6.35 \\ & (8.50) \end{aligned}$ | $\begin{aligned} & \$ 14.85 \\ & (19.10) \end{aligned}$ | $\begin{aligned} & \$ 14.00 \\ & (15.75) \end{aligned}$ | $\begin{aligned} & \$ 16.90 \\ & (21.20) \end{aligned}$ | $\begin{aligned} & \$ 17.00 \\ & (21.20) \end{aligned}$ | $\begin{aligned} & \$ 17.00 \\ & (21.20) \end{aligned}$ |
|  | 25-99 | $\begin{aligned} & \$ 12.50 \\ & (13.50) \end{aligned}$ | $\begin{aligned} & \$ 15.50 \\ & (21.90) \end{aligned}$ | $\begin{aligned} & \$ 16.00 \\ & (18.25) \end{aligned}$ | $\begin{aligned} & \$ 14.00 \\ & (17.00) \end{aligned}$ | $\begin{aligned} & \$ 5.25 \\ & (7.00) \end{aligned}$ | $\begin{aligned} & \$ 12.25 \\ & (15.75) \end{aligned}$ | $\begin{aligned} & \$ 12.00 \\ & (13.50) \end{aligned}$ | $\begin{aligned} & \$ 14.00 \\ & (17.50) \end{aligned}$ | $\begin{aligned} & \$ 14.00 \\ & (17.50) \end{aligned}$ | $\begin{aligned} & \$ 14.00 \\ & (17.50) \end{aligned}$ |
|  | 100-499 | $\begin{aligned} & \$ 11.50 \\ & (12.00) \end{aligned}$ | $\begin{aligned} & \$ 12.75 \\ & (18.00) \end{aligned}$ | $\begin{aligned} & \$ 14.70 \\ & (15.30) \end{aligned}$ | $\begin{aligned} & \$ 11.50 \\ & (14.00) \end{aligned}$ | $\begin{aligned} & \$ 3.90 \\ & (5.20) \end{aligned}$ | $\begin{aligned} & \$ 9.10 \\ & (11.70) \end{aligned}$ | $\begin{aligned} & \$ 10.00 \\ & (11.00) \end{aligned}$ | $\begin{aligned} & \$ 10.40 \\ & (13.00) \end{aligned}$ | $\begin{aligned} & \$ 10.40 \\ & (13.00) \end{aligned}$ | $\begin{aligned} & \$ 10.40 \\ & (13.00) \end{aligned}$ |

[^28]
# PRECISION THIN FILM LADDER NETWORKS 

## GENERAL DESCRIPTION

Several of the complete line of high precision, thin film ladder networks manufactured by the Resistor Products Division of Analog Devices, are shown in this short form guide.

These networks represent the key accuracy elements of the more popular digital to analog conversion techniques. (See applications shown). You can readily assemble a wide variety of high accuracy ( $8-14$ bits), fast, stable and reliable converters using ADI's AD550 and AD555 switches, op amps, in conjunction with these ladder networks.
Each of the networks is available in popular standard configurations - FLATPAK and DUAL-IN-LINE. For added flexibility, chip versions are available for hybrid assembly. These resistor networks are fabricated from our own coated substrates; thus the entire process is under our control. Valuable benefits include the advantages of high-yield batch-processing techniques, high-volume assembly, and automatic laser-trimming, all of which contribute to high performance and reliability, plus efficient use of board space, at low cost.

## TWO PRODUCT FAMILIES ARE AVAILABLE

For maximum flexibility, we offer two ladder families that are functionally equivalent, but allow you to select the operating performance you require in your system for the most efficient cost/function.

## Why Thin Film?

Where excellent long-term stability, small size, wide range of on chip resistance values, and high performance over a wide range of environmental conditions are necessary, thin-film resistance networks are usually preferable to thick-film; at the highest accuracy levels, they are just about the only practical choice. Analog's thin-film networks are characterized by excellent ratio match (to $0.01 \%$ for standard units), low tracking temperature-coefficients (to $0.5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ ), low "excess" noise ( 35 dB below Johnson noise), low drift (to $50 \mathrm{ppm} /$ year at $+25^{\circ} \mathrm{C}$ ), and zero voltage coefficient (except for self-heating effects).

## Why Analog Devices?

- Our reliable thin-film technology, based partly on the use of our own wafers, has been proven over many circuityears, including a large number of units purchased to MIL-STD-883.
- Our networks, designed for use in analog signal-handling and conversion, are backed by a sales-engineering staff with considerable successful experience in helping users with the applications of the op amps and switches you will use them with. Analog Devices makes "one-stop shopping" easy.


## FOR HIGHEST PRECISION AND RELIABILITY -

## AD850, 851, 852/3, 855, 856

For the following reasons many converter designers are selecting these ladder families in preference to matched discretes, or other network technologies.
Performance: Guaranteed accuracy over the operating range. Each network is specified to function over its operating range within the accuracy limits shown below. In addition to excellent resistance matching, close temperature tracking, uniform behavior, small size of monolithic (single substrate) construction, trimmed accuracies at $+25^{\circ} \mathrm{C}$ equivalent to $1 / 4 \mathrm{LSB}$ are obtained for 14 bits of accuracy at $+25^{\circ} \mathrm{C}$.
Convenience: A single component in standard packages performs complete functions, reducing all areas of procurement, handling, and assembly.
High Reliability: The S, T, U grades are available screened to MIL-STD-883, Method 5004.1 for AVIONICS and SPACE FLIGHT systems that require the highest level of performance.

| $\begin{gathered} \text { ACCURACY OPTIONS - AD850, 852, 852/853, } 855 \\ 856,(\text { AD851 ) } \end{gathered}$ |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  | $\begin{aligned} & \pm 1 / 2 \text { LSB of } \\ & 12 \text { Bits } \\ & \hline \end{aligned}$ | $\pm 1 / 2$ LSB of 10 Bits | $\begin{aligned} & \pm 1 / 2 \text { LSB } \\ & 8 \text { Bits } \end{aligned}$ |
| Maximum | Cumulative Error | $\pm 0.012 \%$ | $\pm 0.05 \%$ | $\pm 0.2 \%$ |
| Over the O | perating Range | ( $\pm 0.03 \%$ ) | ( $\pm 0.12 \%$ ) |  |
| Operating | 0 to $+70^{\circ} \mathrm{C}$ | L | K | J |
| Range | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | U | T | S |

## FOR LOW COST HIGH ACCURACY CONVERTERS TO OPERATE WITHIN A NARROW TEMPERATURE RANGE: AD1850, 1851, 1852/3, 1855, 1856

Our newest ladder offering is designed for use in systems that have high accuracy requirements, but operate within a few degrees of $+25^{\circ} \mathrm{C}$. Full scale accuracy is guaranteed at $+25^{\circ} \mathrm{C}$ with a maximum full scale temperature coefficient of $1 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$. The accuracy grades are shown below.

Your designs can incorporate the performance of thin film ladder networks at lower cost without sacrificing accuracy.

ACCURACY OPTIONS - AD1850, 1852, 1852/1853, 1855, 1856, (AD1851)

|  | $\pm 1 / 2$ LSB of | $\pm 1 / 2$ LSB of | $\pm 1 / 2$ LSB o |
| :--- | :--- | :--- | :--- |
|  | 12 Bits | 10 Bits | 8 Bits |
| Maximum Cumulative Error | $\pm 0.012 \%$ | $\pm 0.05 \%$ | $\pm 0.2 \%$ |
| at $+25^{\circ} \mathrm{C}$ | $( \pm 0.03 \%)$ | $( \pm 0.12 \%)$ |  |
| Operating <br> Range | L to $+70^{\circ} \mathrm{C}$ | K | J |

## AD850 AND AD1850-12 BIT BINARY CURRENT LADDERS - "D" PACKAGE



NOTE 1 COMMON BUSS RESISTANCE SHALL BE $\leq 150 \mathrm{~m} \Omega$
between pin 24 AND THE R11R12 JUNCTION
Tolerance* Maximum Bit Error**

| R | Nominal Value (Ohms) | $\begin{gathered} \text { REF. } \\ \mathbf{R} \end{gathered}$ | Max. Pwr. Dissipation (mW) | $\begin{gathered} \text { L (U) } \\ \text { 1/8LSB of } 12 \text { Bits } \end{gathered}$ | RATIO ACCURACY $K$ (T) 1/8LSB of 10 Bits | $\underset{1 / 8 L S B \text { of } 8 \text { Bits }}{\text { J }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 10k | - | 20 | $\pm 5.0 \% \mathrm{Abs}$. | $\pm 5.0 \%$ Abs. | $\pm 5.0 \%$ Abs. |
| 2 | 20k | R1 | 10 | 0.015\% | 0.05\% | 0.20\% |
| 3 | 40k | R1 | 5 | 0.03\% | 0.10\% | 0.40\% |
| 4 | 80k | R1 | 2.5 | 0.05\% | 0.20\% | 0.80\% |
| 5 | 10k | R1 | 20 | 0.10\% | 0.40\% | 1.6\% |
| 6 | 20k | R1 | 10 | 0.20\% | 0.80\% | 3.2\% |
| 7 | 40k | R1 | 5 | 0.40\% | 1.6\% | 6.4\% |
| 8 | 80k | R1 | 2.5 | 0.80\% | 3.2\% | 10\% |
|  | 10k | R1 | 20 | 1.0\% | 5.0\% | 10\% |
| 10 | 20k | R1 | 10 | 1.0\% | 5.0\% | 10\% |
| 11 | 40k | R1 | 5 | 1.0\% | 5.0\% | 10\% |
| 12 | 80k | R1 | 2.5 | 1.0\% | 5.0\% | 10\% |
| 13 | 5 k | R1 | 40 | 0.10\% | 0.10\% | 0.20\% |
| 14 | 14.0625k | R17 | 0.5 | 0.05\% | 0.20\% | 0.50\% |
| 15 | 14.0625 k | R17 | 0.5 | 1.0\% | 2.0\% | 5.0\% |
| 16 | 5 k | R1 | 40 | 0.10\% | 0.10\% | 0.20\% |
| 17 | 1 k | - | 8 | $\pm 5.0 \%$ Abs. | $\pm 5.0 \% \mathrm{Abs}$. | $\pm 5.0 \%$ Abs. |
| 18 | 937.5 | R17 | 8 | 1.0\% | 2.0\% | 5.0\% |
| 19 | 80k | R1 | 2.5 | 0.10\% | 0.10\% | 0.20\% |
| 20 | 6 k | R1 | 12 | 0.10\% | 0.10\% | 0.20\% |
| 21 | 48.4 k | R1 | 2 | 0.10\% | 0.10\% | 0.20\% |

## AD851 AND AD1851-12 BIT BCD CURRENT LADDER - "D" PACKAGE




AD852 AND AD1852-8 BIT BINARY CURRENT LADDER - "D" OR "F" PACKAGE


Tolerance* Maximum Bit Error**

| R | Nominal <br> Value (Ohms) | REF. <br> R | Max. Pwr. <br> Dissipation <br> (mW) | Ratio Accuracy <br> L (U) <br> $\mathbf{1 / 8 L S B}$ of 12 Bits |
| :---: | :---: | :---: | :---: | :---: |
| 1 | 10 k | - | 20 | $\pm 0.3 \%$ Abs. |
| 2 | 20 k | R1 | 10 | $0.015 \%$ |
| 3 | 40 k | R1 | 5 | $0.03 \%$ |
| 4 | 80 k | R1 | 2.5 | $0.05 \%$ |
| 5 | 10 k | R1 | 20 | $0.10 \%$ |
| 6 | 20 k | R1 | 10 | $0.2 \%$ |
| 7 | 40 k | R1 | 5 | $0.4 \%$ |
| 8 | 80 k | R1 | 2.5 | $0.8 \%$ |
| 14 | 14.0625 k | R17 | 0.5 | $0.05 \%$ |
| 17 | 1 k | - | 8 | $\pm 0.5 \%$ Abs. |
| 19 | 80 k | R1 | 2.5 | $0.20 \%$ |
| 22 | 15 k | R17 | 0.5 | $0.50 \%$ |

AD853 AND AD1853-4 BIT BINARY CURRENT LADDER - "D" OR "F" PACKAGE


| PARAMETER | Units | L (U) | K (T) | J (S) |
| :--- | :--- | :--- | :--- | :--- |
| R | (Ohms) | 50 k | 50 k | 50 k |
| 2R | (Ohms) | 100 k | 100 k | 100 k |
| Impedance* | (Ohms) | $50 \mathrm{k} \pm 10 \%$ | $50 \mathrm{k} \pm 10 \%$ | $50 \mathrm{k} \pm 10 \%$ |
| Max. Bit Error | (\%) | 0.004 | 0.016 | 0.064 |
| Max. Cummulative Error | (\%) | 0.006 | 0.024 | 0.10 |
| Max. Application R Ratio Accur. | (\%) | 0.012 | 0.05 | 0.20 |

*Output impedance as measured at pin 16 (pins $14 \& 15$ open circuit,
all others shorted).
Maximum Power Dissipation: 1.0 mW per resistor.
Maximum Network Dissipation: 30mW.

Tolerance* Maximum Bit Error**

AD856 AND AD1856-12 BIT R-2R CURRENT LADDER - "D" OR "F" PACKAGE


| PARAMETER | Units | L (U) | K (T) | J (S) |
| :--- | :--- | :--- | :--- | :--- |
| R | (Ohms) | 500 | 500 | 500 |
| 2R | (Ohms) | 1 k | 1 k | 1 k |
| Impedance | (Ohms) | $500 \pm 5 \%$ | $500 \pm 5 \%$ | $500 \pm 5 \%$ |
| Max. Bit Error* | (\%) | 0.006 | 0.024 | 0.10 |
| Max. Cummulative Error* | $(\%)$ | 0.012 | 0.05 | 0.20 |

${ }^{*}$ Referenced to full scale.
Maximum Power Dissipation: R Values - 18mW
$2 R$ Values - 36 mW
Maximum Network Dissipation: 200 mW

Tolerance* Maximum Bit Error**
*Resistance Measurements Performed at $+25^{\circ} \mathrm{C}$.
${ }^{* *}$ Maximum Bit Error: 1/8LSB/Bit of Selected Bit Accuracy.

APPLICATIONS: See: "Analog-Digital Conversion Handbook"

FOR AD850, 1850, 852/3, 1852/3:
FOR AD855, 1855:


## SPECIFICATIONS, PRICING AND ORDERING INFORMATION PRECISION THIN FILM LADDER NETWORKS

SPECIFICATIONS (Typical @ $+25^{\circ} \mathrm{C}$ unless otherwise noted)

| $\checkmark$ | Units | Min | Typ | Max |
| :---: | :---: | :---: | :---: | :---: |
| Temperature Coefficient of Full Scale Output (AD1850-1856 Series Only) | ppm/ $/{ }^{\text {C }}$ |  | $\pm 0.5$ | $\pm 1$ |
| Resistance Load Stability at Rated Power* |  |  |  |  |
| @ $+25^{\circ} \mathrm{C}$ Absolute Values | \% Nominal/Year |  | $\pm 0.05$ | $\pm 0.1$ |
| Ratio Values | \% Nominal/Year |  | $\pm 0.005$ | $\pm 0.01$ |
| @ $+125^{\circ} \mathrm{C}$ Absolute Values | \% Nominal/1000h |  | $\pm 0.05$ | $\pm 0.1$ |
| Ratio Values | \% Nominal/1000h |  | $\pm 0.005$ | $\pm 0.01$ |
| Voltage Coefficient of Resistance** | $\mu \mathrm{V} / \mathrm{V}$ |  |  | Negligible |
| Excess Noise (per MIL-STD-202D, Method 308) | dB below Johnson Noise | 35 | 50 |  |
| Interlead Capacitance | pF |  |  | $<10$ |
| Voltage Rating at Rated Dissipation* | V |  |  | $\sqrt{\text { W.R. }}^{* * *}$ |
| Temperature Ratings |  |  |  |  |
| Storage | ${ }^{\circ} \mathrm{C}$ | -65 | +25 | +150 |
| Operating, J, K, L Options | ${ }^{\circ} \mathrm{C}$ | 0 | +25 | +70 |
| Operating, S, T, U Options | ${ }^{\circ} \mathrm{C}$ | -55 | +25 | +125 |
| Lead Soldering for 60s Maximum | ${ }^{\circ} \mathrm{C}$ |  |  | +300 |

-Power Rating specified at $+125^{\circ} \mathrm{C}$ for individual resistors or devices is derated to 0 mW at $+150^{\circ} \mathrm{C}$.
-*None measurable (per MIL-STD-202D, Method 309) except for changes caused by self-heating of
the network due to dissipation as a function of voltage.
... Where $W$ is equal to power (watts) and $R$ is equal to resistance (ohms).

PRICES AND ORDERING INFORMATION

| OPERATING TEMPERATURE RANGE |  |  | $0 \mathrm{TO}+70^{\circ} \mathrm{C}$ |  |  | $-55^{\circ} \mathrm{C} \mathrm{TO}+125^{\circ} \mathrm{C}$ |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SaDNVY dWal yano yozea sailvinwno 'xbw | F.S. ACCUR <br> FULL SCAL | )LSB OF ( ) BITS URACY \% | $\begin{aligned} & 1 / 2 \text { LSB of } \\ & \mathbf{8} \text { Bits } \\ & \pm 0.2 \% \\ & \hline \end{aligned}$ | $\begin{aligned} & 1 / 2 \text { LSB of } \\ & 10 \text { Bits } \\ & \pm 0.05 \% \\ & \hline \end{aligned}$ | $\begin{aligned} & 1 / 2 \text { LSB of } \\ & 12 \text { Bits } \\ & \pm 0.012 \% \\ & \hline \end{aligned}$ | $\begin{array}{\|l\|} \hline 1 / 2 \text { LSB of } \\ 8 \text { Bits } \\ \pm 0.2 \% \\ \hline \end{array}$ | $1 / 2$ LSB of 10 Bits $\pm 0.05 \%$ | $1 / 2$ LSB of 12 Bits $\pm 0.12 \%$ |
|  | PART NO. | QUANTITIES | J | K | L | $\mathrm{S}^{1}$ | $\mathrm{T}^{1}$ | $\mathrm{U}^{1}$ |
|  | $\begin{aligned} & \text { AD850 } \\ & \text { "'D" Only } \end{aligned}$ | $\begin{aligned} & 1-24 \\ & 25-99 \\ & 100-499 \end{aligned}$ | - | $\$ 55.00$ 50.00 <br> 45.00 | $\$ 60.00$ 54.00 <br> 43.00 | - | $\$ 100.00$ 90.00 80.00 | $\$ 120.00$ 102.00 84.00 |
|  | $\begin{aligned} & \text { AD851² } \\ & \text { "D" Only } \end{aligned}$ | $\begin{aligned} & 1-24 \\ & 25-99 \\ & 100-499 \end{aligned}$ | - | $\begin{aligned} & 60.00 \\ & 55.00 \\ & 50.00 \end{aligned}$ | $\begin{aligned} & 75.00 \\ & 70.00 \\ & 60.00 \\ & \hline \end{aligned}$ | - | 110.00 100.00 90.00 | 135.00 115.00 100.00 |
|  | $\begin{aligned} & \text { AD852 } \\ & \text { "D" or "F" } \end{aligned}$ | $\begin{aligned} & 1-24 \\ & 25-99 \\ & 100-499 \end{aligned}$ | - | $\begin{aligned} & -- \\ & - \end{aligned}$ | $\begin{aligned} & 53.00 \\ & 45.50 \\ & 41.50 \\ & \hline \end{aligned}$ | - | $\begin{aligned} & - \\ & - \end{aligned}$ | $\begin{aligned} & 79.50 \\ & 68.00 \\ & 62.50 \\ & \hline \end{aligned}$ |
|  | $\begin{aligned} & \text { AD852/3 } \\ & \text { "D" or "F" } \end{aligned}$ | $\begin{aligned} & 1-24 \\ & 25-99 \\ & 100-499 \end{aligned}$ | - | $\begin{aligned} & 66.00 \\ & 56.75 \\ & 52.00 \end{aligned}$ | $\begin{aligned} & 79.50 \\ & 68.00 \\ & 62.50 \end{aligned}$ | - | $\begin{array}{r} 106.00 \\ 91.00 \\ 83.00 \end{array}$ | $\begin{array}{r} 109.00 \\ 93.50 \\ 85.50 \end{array}$ |
|  | $\begin{aligned} & \text { AD855 } \\ & \text { "D" or "F" } \end{aligned}$ | $\begin{aligned} & 1-24 \\ & 25-99 \\ & 100-499 \end{aligned}$ | $\begin{array}{r} \$ 47.00 \\ 40.00 \\ 36.75 \end{array}$ | $\begin{aligned} & 56.00 \\ & 48.00 \\ & 44.00 \end{aligned}$ | $\begin{aligned} & 58.50 \\ & 50.00 \\ & 45.75 \end{aligned}$ | $\$ 71.50$ 61.50 56.25 | $\begin{aligned} & 91.00 \\ & 78.00 \\ & 71.50 \end{aligned}$ | $\begin{array}{r} 117.00 \\ 100.00 \\ 92.00 \end{array}$ |
|  | $\begin{aligned} & \text { AD856 } \\ & \text { "D" or "F" } \end{aligned}$ | $\begin{aligned} & 1-24 \\ & 25-99 \\ & 100-499 \end{aligned}$ | $\begin{aligned} & 37.60 \\ & 32.00 \\ & 29.40 \end{aligned}$ | $\begin{aligned} & 44.80 \\ & 38.40 \\ & 35.20 \end{aligned}$ | 46.80 40.00 36.60 | $\begin{aligned} & 57.20 \\ & 49.20 \\ & 45.00 \end{aligned}$ | $\begin{aligned} & 72.80 \\ & 62.40 \\ & 57.20 \end{aligned}$ | 93.60 <br> 80.00 <br> 73.60 |
|  | $\begin{array}{\|l} \text { AD1850 } \\ \text { "D" Only } \end{array}$ | $\begin{aligned} & 1-24 \\ & 25-99 \\ & 100-499 \end{aligned}$ | $\begin{aligned} & 28.00 \\ & 24.00 \\ & 20.00 \end{aligned}$ | $\begin{aligned} & 34.25 \\ & 29.50 \\ & 23.00 \end{aligned}$ | $\begin{aligned} & 40.50 \\ & 34.75 \\ & 26.00 \end{aligned}$ | $\begin{aligned} & - \\ & - \\ & - \end{aligned}$ | $\begin{aligned} & - \\ & - \\ & - \end{aligned}$ | $\begin{aligned} & \text { - } \\ & \text { - } \end{aligned}$ |
|  | $\begin{aligned} & \text { AD18512 } \\ & \text { "D" Only } \end{aligned}$ | $\begin{aligned} & 1-24 \\ & 25-99 \\ & 100-499 \end{aligned}$ | - | $\begin{aligned} & 30.50 \\ & 26.00 \\ & 23.50 \end{aligned}$ | $\begin{aligned} & 35.00 \\ & 30.00 \\ & 27.00 \end{aligned}$ | - | - | - |
|  | $\begin{array}{\|l} \text { AD1852 } \\ \text { "D" or "F" } \end{array}$ | 1-24 <br> 25-99 <br> 100-499 | - |  | $\begin{aligned} & 36.45 \\ & 31.28 \\ & 23.40 \end{aligned}$ | - | - | - |
|  | $\begin{aligned} & \text { AD1852/3 } \\ & \text { "D" or "F" } \end{aligned}$ | $\begin{aligned} & 1-24 \\ & 25-99 \\ & 100-499 \end{aligned}$ | $\begin{aligned} & 30.80 \\ & 26.40 \\ & 22.00 \end{aligned}$ | $\begin{aligned} & 37.68 \\ & 32.45 \\ & 25.30 \end{aligned}$ | $\begin{aligned} & 44.55 \\ & 38.23 \\ & 28.60 \end{aligned}$ | $\begin{aligned} & \text { - } \\ & \text { - } \end{aligned}$ | $\begin{aligned} & - \\ & - \\ & - \end{aligned}$ | - |
|  | $\begin{aligned} & \text { AD1855 } \\ & \text { "D" or "F" } \end{aligned}$ | 1-24 <br> 25-99 <br> 100-499 | $\begin{aligned} & 29.50 \\ & 25.50 \\ & 23.25 \end{aligned}$ | $\begin{aligned} & 35.75 \\ & 30.75 \\ & 28.00 \end{aligned}$ | $\begin{aligned} & 42.00 \\ & 36.00 \\ & 33.00 \end{aligned}$ | $\begin{aligned} & - \\ & - \end{aligned}$ | - | - |
|  | $\begin{aligned} & \text { AD1856 } \\ & \text { "D" or "F" } \end{aligned}$ | 1-24 <br> 25-99 <br> 100-499 | $\begin{aligned} & 23.60 \\ & 20.40 \\ & 18.60 \end{aligned}$ | $\begin{aligned} & 28.60 \\ & 24.60 \\ & 22.40 \end{aligned}$ | $\begin{aligned} & 33.60 \\ & 28.80 \\ & 26.40 \end{aligned}$ | $\begin{aligned} & \text { - } \\ & \text { - } \end{aligned}$ |  | - |

[^29]ORDERING INFORMATION i.e., AD850UD/883

| AD850 | U | D | /883 |
| :---: | :---: | :---: | :---: |
| 1 | T |  | T |
| Basic | F.S. | Package | If |
| Part | Accuracy |  | Option |
|  |  |  | 883 |

## MECHANICAL OUTLINES ANALOG PRODUCTS

MODULE TERMINAL


## SOCKET TERMINAL



## GENERAL NOTES:

- All dimensions shown in inches and (mm).
- All pin diagrams are terminal views. Grids are on $0.1^{\prime \prime}$ (2.54) spacing for reference only.
- Pin designations are for reference only; in general designations are silk screened on the sockets.
- Pins are gold plated, half-hard brass, $0.04^{\prime \prime}$ (1.01) diameter, $0.2^{\prime \prime}$ (5.08) minimum length.
- Mating socket numbers are shown with each pinning diagram. Socket outlines are shown on page 171.
Socket material is NEMA grade G-10 glass epoxy, $0.093^{\prime \prime}$ (2.36) thick. Terminals are $0.5^{\prime \prime}$ (12.70) maximum length.


## A PACKAGE

## B PACKAGE

$\frac{\text { Model }}{606} \quad \frac{\text { Package }}{\text { A-1 }} \quad \frac{\text { Socket }}{\mathrm{AC} 1040}$

$\frac{\text { Model }}{171} \quad \frac{\text { Package }}{\mathrm{B}-1} \quad$| Socket |
| :--- |
| $\mathrm{AC1037}$ |



A-1



B-1


D PACKAGE


| Model | Package | Socket |
| :---: | :---: | :---: |
| 424 | D-1 | AC1012 |
| 427 | D-2 | AC1023 |
| 435 | D-2 | AC1023 |

D-1
D-2



[^30]** Bandwidth pin and pin marked NC omitted on models 230, 233, 234.

## H, HA, HB PACKAGES - Modular Power Supplies



| Model | Rating | Package |
| :---: | :---: | :---: |
| 902 | $\pm 15 \mathrm{~V} / 100 \mathrm{~mA}$ | HA-1 |
| 902-2 | $\pm 15 \mathrm{~V} / 100 \mathrm{~mA}$ | HB-1 |
| 903 | $5 \mathrm{~V} / 500 \mathrm{~mA}$ | HA-1* |
| 904 | $\pm 15 \mathrm{~V} / 50 \mathrm{~mA}$ | HB-1 |
| 905 | $5 \mathrm{~V} / 1000 \mathrm{~mA}$ | HA-1* |
| 906 | $5 \mathrm{~V} / 250 \mathrm{~mA}$ | HB-1* |
| 907 | $\pm 12 \mathrm{~V} / 25 \mathrm{~mA}$ | HB-1 |
| 908 | $\pm 12 \mathrm{~V} / 50 \mathrm{~mA}$ | HB-1 |
| 909 | $\pm 12 \mathrm{~V} / 100 \mathrm{~mA}$ | HB-1 |
| 915 | $\pm 15 \mathrm{~V} / 25 \mathrm{~mA}$ | HB-1 |
| 920 | $\pm 15 \mathrm{~V} / 200 \mathrm{~mA}$ | HA-1 |
| 921 | $\pm 12 \mathrm{~V} / 240 \mathrm{~mA}$ | HA-1 |
| 922 | $5 \mathrm{~V} / 2000 \mathrm{~mA}$ | H-1 * |
| 925 | $\pm 15 \mathrm{~V} / 350 \mathrm{~mA}$ | H-1 |
| 931 | $\pm 18 \mathrm{~V} / 25 \mathrm{~mA}$ | HB-1 |
| 932 | $\pm 18 \mathrm{~V} / 100 \mathrm{~mA}$ | HA-1 |
| 933 | $\pm 24 \mathrm{~V} / 50 \mathrm{~mA}$ | HB-1 |
| 934 | $\pm 24 \mathrm{~V} / 100 \mathrm{~mA}$ | HA-1 |
| 935 | $\pm 18 \mathrm{~V} / 50 \mathrm{~mA}$ | HB-1 |

*- $\mathrm{V}_{\mathrm{S}}$ Pin not connected for 5 V power supplies.
**Socket AC1028 for I option. Socket AC1013 for all other models.

## J PACKAGE - Chassis Mount Power Supplies



| Model | Rating |
| :---: | :---: |
| 952 | $\pm 15 \mathrm{~V} / 100 \mathrm{~mA}$ |
| 955 | $5 \mathrm{~V} / 1000 \mathrm{~mA}$ |
| 970 | $\pm 15 \mathrm{~V} / 200 \mathrm{~mA}$ |
| 971 | $\pm 12 \mathrm{~V} / 240 \mathrm{~mA}$ |

## K PACKAGE - Isolation Amplifiers



K-2


| Model | Package |  | Socket |
| :--- | :--- | :--- | :--- |
|  |  | K-1 |  |
| 272 |  | AC1033 |  |
| 273 | K-1 |  | AC1033 |
| 274 | K-2* |  | AC1007 |
| 276 | K-1 |  | AC1033 |
| 279 | K-3 |  | AC1042 |

*"HI IN \#2" and "GAIN" pins are detachable.

## K-1



K-3


## M PACKAGE



| Model | Package | Socket |
| :---: | :---: | :---: |
| 40 | M-2 | AC1003 |
| 43 | M-2 | AC1003 |
| 118 | M-1 | AC1003 |
| 165 | M-1 | AC1003 |
| 751 | M-3 | AC1016 |

## N PACKAGE



N-1


| Model | Package | Socket |
| :---: | :---: | :---: |
| 46 | N-1 | AC1034 |
| 50 | $\mathrm{N}-1$ | AC1034 |
| 51 | $\mathrm{N}-1$ | AC1034 |

## Q, QB, QC PACKAGES



Q-1. QB-1, QC-1


| Package |  | Socket |
| :--- | :--- | :--- |
|  |  |  |
| QC-4 |  | AC1008 |
| Q-3 |  | AC1003 |
| QC-2 |  | AC1032 |
| QB-2 |  | AC1016 |
| Q-3 |  | AC1003 |

QB-2


QC-4

*Model 42 (QB-1) common pin is not provided. No connection required.

## R PACKAGE



R-1


| Model |  | Package | Socket |
| :--- | :--- | :--- | :--- |
|  |  | R-1 <br> 210 |  |
| AC1002 |  |  |  |
| 211 | R-1 |  | AC1002 |

## W, WA PACKAGES



| $\frac{\text { Model }}{}$ |  | Package |  |
| :--- | :--- | :--- | :--- |
|  |  | Socket |  |
| 331 |  | WA-1 |  |
| AC1014 |  |  |  |
| 310 |  | W-1 |  |
| AC1017 |  |  |  |
| 311 |  | W-1 |  |
| AC1017 |  |  |  |

## WA-1


*-IN, model 310; +IN, model 311.

## MODEL 425 OUTLINE

NOTES:

1. Model 425 gain adjust pot in series with X input.
2. Mating connector supplied with unit (ADI part no. 60-42820).


## MATING SOCKETS

AC1002 @ \$3.75


AC1003 @ \$3.00



AC1012 @ \$4.25
AC1023 @ $\$ 3.75$
AC1038 @ \$3.25


AC1013 @ \$3.75


AC1014 @ \$3.75




## OPERATIONAL AMPLIFIER MANIFOLD



## MODEL 79P CERMET BALANCE POT

Analog Devices has selected the Beckman Helitrim Model 79P as suitable for most applications and carries this balance pot in stock. We offer this service since you may find it more economical or convenient to order your balance pots directly from Analog Devices along with your amplifiers. The identical pots are also available from Beckman or their stocking distributors.


MODEL 79P

## SPECIFICATIONS

Tempco, max
Input voltage, max
Power rating
End resistance, max
Resolution
Ambient temperature range
Adjustment turns, nominal
Sealing (immersion test)
Temperature cycling
Humidity cycling
Shock
Vibration
Load life at 0.75 watts
Rotational life
ANALOG DEVICES
PART NUMBER
79PR1k
79PR2k
79PR5k
79PR10k
79PR20k
79PR25k
79PR50k
79PR100k
79PR200k
79PR250k
$\pm 100 \mathrm{ppm}$ ( 0 to -
0.75 watts at $+25^{\circ} \mathrm{C}$, derated to 0

$$
\text { watts at }+105^{\circ} \mathrm{C}
$$

2 ohms
essentially infinite
$-55^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$
15
meets MIL-R-22097C
5 cycles $-55^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$
5 cycles
50G's
10 to $500 \mathrm{kz}, 10 \mathrm{G}$ 's
1,000 hrs. at $+25^{\circ} \mathrm{C}$
200 cycles
RESISTANCE PRICE
OHMS
1k $\pm 10 \%$
$2 \mathrm{k} \pm 10 \%$
$5 \mathrm{k} \pm 10 \%$
$10 \mathrm{k} \pm 10 \%$
(1-9) $\$ 3.25$
$25 \mathrm{k} \pm 10 \% \quad\} \quad(10-99) \quad \$ 2.95$
$50 \mathrm{k} \pm 10 \%$
$100 \mathrm{k} \pm 10 \%$
$200 \mathrm{k} \pm 10 \%$
$250 \mathrm{k} \pm 10 \%$
$\}$

## MECHANICAL OUTLINES CONVERTER PRODUCTS

## GENERAL NOTES:

- All pinning diagrams are terminal views on $0.1^{\prime \prime}$ grids.
- All possible pin locations are shown, even though pins are installed in only a portion of these locations for any given product.
- Unless otherwise noted, all module pins are gold plated halfhard brass (MIL-G-45 204), $0.02^{\prime \prime}(0.05 \mathrm{~mm})$ in diameter, and $0.2^{\prime \prime}(5.08 \mathrm{~mm})$ minimum length.
- All models constructed on printed circuit boards are supplied with mating edge connectors.
- All dimensions shown in inches and (millimeters).

*Pin No. 29 for model MPX-8A. (Functional pin also used as key)



Note: Pins on SHA-2 are $0.040^{\prime \prime}$ (1.016) diameter.



Note: Pins on SHA-6 are $0.040^{\prime \prime}$ (1.016) diameter.

C-4


MOUNTING BOARDS

| MODEL NO. | MOUNTING BOARD | BOARD DIMENSIONS |  | PRICE (1-9) |
| :---: | :---: | :---: | :---: | :---: |
|  |  | INCHES <br> A B | MILLIMETERS |  |
| ADC-I | AC1500 | $41 / 2^{\prime \prime} \times 6^{\prime \prime}$ | $114.30 \times 152.40$ | \$60. |
| ADC-QM | AC4451 | $41 / 2^{\prime \prime} \times 3{ }^{\prime \prime} 4^{\prime \prime}$ | $114.30 \times 95.25$ | \$25. |
| ADC-QU | AC4451 | $41 / 2^{\prime \prime} \times 334^{\prime \prime}$ | $114.30 \times 95.25$ | \$25. |
| ADC-8S | AC4751 | $41 / 2^{\prime \prime} \times 6^{\prime \prime}$ | $114.30 \times 152.40$ | \$25. |
| ADC-10Z | AC1504 | $41 / 2^{\prime \prime} \times 6^{\prime \prime}$ | $114.30 \times 152.40$ | \$25. |
| ADC-12QZ | AC1548 | $41 / 2^{\prime \prime} \times 6^{\prime \prime}$ | $114.30 \times 152.40$ | \$25. |
| ADC1100 | AC1550 | $41 / 2^{\prime \prime} \times 6^{\prime \prime}$ | $114.30 \times 152.40$ | \$25. |
| ADC1103 | AC1549 | $41 / 2^{\prime \prime} \times 6{ }^{\prime \prime}$ | $114.30 \times 152.40$ | \$25. |
| ADC1109 | AC1520 | $41 / 2^{\prime \prime} \times 3$ [ $8^{\prime \prime}$ | $114.30 \times 92.08$ | \$25. |
| ADC1111 | AC4451 | $4{ }^{1 / 2} 2^{\prime \prime} \times 3$ 3/4" | $114.30 \times 95.25$ | \$25. |
| DAC-10Z | AC4102 | see outline | see outline | \$15. |
| DAC-12QZ | AC4516 | $41 / 2^{\prime \prime} \times 33 / 4^{\prime \prime}$ | $114.30 \times 95.25$ | \$40. |
| DAC1009 | AC6160 | $41 / 2^{\prime \prime} \times 21 / 2^{\prime \prime}$ | $114.30 \times 63.50$ | \$20. |
| DAC1118 | AC4494 | $41 / 2^{\prime \prime} \times 33 / 4^{\prime \prime}$ | $114.30 \times 95.25$ | \$40. |
| DAC1 106 | AC4102 | see outline | see outline | \$15. |
| DAC1112 | AC4516 | $41 / 2^{\prime \prime} \times 334^{\prime \prime}$ | $114.30 \times 95.25$ | \$40. |
| DAC-QM | AC4494 | $41 / 2^{\prime \prime}$ " $\times 33^{\prime 3} 4^{\prime \prime}$ | $114.30 \times 95.25$ | \$40. |
| DAC-QS | AC4516 | $41 / 2^{\prime \prime} \times 33 /{ }^{\prime \prime}$ | $114.30 \times 95.25$ | \$40. |
| DAC-M | AC4102 | see outline | see outline | \$15. |
| MDA-10Z | AC4102 | see outline | see outline | \$15. |
| MDA-10F | AC4159 | $41 / 2^{\prime \prime} \times 214^{\prime \prime}$ | $114.30 \times 57.15$ | \$15. |
| MDA-11MF | AC1509 | $41 / 2^{\prime \prime} \times 6^{\prime \prime}$ | $114.30 \times 152.40$ | \$25. |
| MPX-8A | AC6160 | $41 / 2^{\prime \prime} \times 21 /{ }^{\prime \prime}$ | $114.30 \times 63.50$ | \$20. |
| SHA-1A | AC4102 | see outline | see outline | \$15. |
| SHA-2A | AC1503 | $41 / 2^{\prime \prime} \times 214^{\prime \prime}$ | $114.30 \times 57.15$ | \$35. |
| SHA-3 | AC4102 | see outline | see outline | \$15. |
| SHA-4 | AC4102 | see outline | see outline | \$15. |
| SHA-5 | AC4102 | see outline | see outline | \$15. |
| SHA-6 | AC1508 | $41 / 2^{\prime \prime} \times 6{ }^{\prime \prime}$ | $114.30 \times 152.40$ | \$15. |
| SHA1114 | AC1503 | $41 / 2^{\prime \prime} \times 214^{\prime \prime}$ | $114.30 \times 57.15$ | \$35. |



DIMENSIONS SHOWN IN INCHES AND (MILLIMETERS).
NOTES:

1. Material: $1 / 16^{\prime \prime}$ G-10 glass epoxy per MIL-D-139, 2 oz . copper clad with solder plating.

Edge connectors gold plated per MIL-G-45 204.
2. Mating cinch connector supplied with mounting board.
3. Trim adjustment pots mounted on boards (when applicable).

# MECHANICAL OUTLINES DIGITAL PANEL METERS 

MODEL AD2001
OVERALL DIMENSIONS


RECOMMENDED
PANEL CUT OUT


MODELS AD2002, AD2003, AD2004, AD2006, AD2010
OVERALL DIMENSIONS
RECOMMENDED


PANEL CUT OUT


| MODEL | D $_{1}$ | D $_{2}$ |
| :---: | :---: | :---: |
| AD2002 | $1.520(38.61)$ | $2.020(51.31)$ |
| AD2003 | $2.020(51.31)$ | $2.800(71.12)$ |
| AD2004 | $2.520(64.01)$ | $3.300(83.82)$ |
| AD2006 | $4.080(10.36)$ | $4.950(12.57)$ |
| AD2010 | $0.750(19.05)$ | $1.400(35.56)$ |

AD2008

## OVERALL DIMENSIONS



ALL DIMENSIONS ARE IN INCHES AND (MILLIMETERS)

## DPM CONNECTOR GUIDE

| Model | Description | $1-9$ | $100+$ |
| :--- | :--- | :--- | :--- |
| AC1501 | 30 Pin, 0.156" spacing Viking No. 2 Vk 15D/1-2 for <br> use with the AD2001, AD2010, AD2010/R, AD2001/C, | $\$ 3.50$ | $\$ 3.00$ |
|  | AC2610 | AD2006/C and AD2008 <br> 36 Pin, 0.156" spacing Viking No. 2 Vk 18D/1-2 for use <br> with AD2008 | 5.00 |

## DPM DISPLAY FILTER OPTIONS

Various no-cost display filter options are available as listed below. Specify the lens option number when ordering if a non-standard filter is desired; otherwise the filter listed as standard will be shipped with the unit.

## DISPLAY FILTER SELECTION CHART

| Lens <br> Number | Filter Color | AD2002 | AD2003 | AD2004 | AD2006 | AD2008 | AD2010 |
| :---: | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 1 | Green with ADI logo | STD | STD | N/A | N/A | N/A | N/A |
| 2 | Green w/o ADI logo | OPT | OPT | N/A | N/A | N/A | N/A |
| 3 | Dark red with ADI logo | OPT | OPT | N/A | N/A | N/A | N/A |
| 4 | Dark red w/o ADI logo | OPT | OPT | N/A | N/A | N/A | N/A |
| 5 | Light red with ADI logo | AVAIL | AVAIL | STD | STD | N/A | STD |
|  |  | (not recommended) |  |  |  |  |  |
| 6 | Light red w/o ADI logo | AVAIL | AVAIL | OPT | OPT | N/A | OPT |
| 7 | Light red with ADI logo | N/A | N/A | N/A | N/A | STD | N/A |
| 8 | Light red w/o ADI logo | N/A | N/A | N/A | N/A | OPT | N/A |
| 9 | Amber with ADI logo | OPT | OPT | N/A | OPT | N/A | N/A |
| 10 | Amber w/o ADI logo | OPT | OPT | N/A | OPT | N/A | N/A |
| 13 | Amber with ADI logo | N/A | N/A | N/A | N/A | OPT | N/A |
| 14 | Amber w/o ADI logo | N/A | N/A | N/A | N/A | OPT | N/A |

## MECHANICAL OUTLINES LINEAR INTEGRATED CIRCUITS

## CN2



## TO-99




TO-99 (Modified)


TO-100



MP72


24 PIN MOLDED PACKAGE



## MINI-DIP




NOTE: LEAD NO. 1 IDENTIFIED BY COLOR DOT OR NOTCH MECHANICAL INDEX POINT OR NOTCH IN PIN.


NOTE: LEAD NO 1 IDENTIFIED BY COLOR DOT OR NOTCH MECHANICAL INDEX POINT OR NOTCH IN PIN.

24 PIN CERAMIC DIL
PACKAGE



MODIFIED DIL
PACKAGE


| PINS | " $\mathrm{A} " \pm \mathbf{0 . 0 1 0}(\mathbf{0 . 2 5 )}$ | "B" |
| :--- | :---: | :---: |
| 16 | $0.885(22.48)$ | $0.700(17.78)$ |
| 18 | $0.985(25.02)$ | $0.800(20.32)$ |
| 24 | $1.285(32.64)$ | $1.100(27.94)$ |

14 PIN
FLAT PACK PACKAGE


16 PIN
FLAT PACK PACKAGE


NOTE: LEAD NO. 1 IDENTIFIED BY COLOR DOT MECHANICAL INDEX POINT OR NOTCH IN PIN

## A WORLDWIDE SERVICE-ORIENTED COMPANY

Analog Devices, Inc. is the leading supplier of electronic components and subsystems used for the acquisition, conditioning, conversion, transmission and display of analog and digital data in measurement and control systems. Our customer base, which exceeds 6,000 companies worldwide, is largely from those market segments in which instrumentation plays an important role, principally the fields of industrial automation, medicine, avionics, test and laboratory instrumentation. Currently with sales at $\$ 30 \mathrm{M}$, we employ in excess of 1,000 people worldwide.
Founded in 1965, our initial thrust was in assembling analog functional circuits from discrete components. While these modular building blocks still represent a major portion of our business, we recognized that there would be an increasing shift in the form of these circuits from hand-assembled modules to much lower cost integrated circuits.
Accordingly, the company was divided into divisional product development centers, each with its own business charter, supported by a single sales organization. Each product center specialized in developing products which exploit the fullest advantages of the design and processing technology available to it.


Consequently, Analog Devices is uniquely qualified to offer not only a broad range of product types, but also a variety of technologies across these product types.
Furthermore, the availability of a range of technologies to our designers provides them with a broad body of knowledge from which to draw in the pursuit of designing innovative solutions to customer problems.
Our Semiconductor Division in Wilmington, Massachusetts, applies advanced linear IC technology to the development of operational and instrumentation amplifiers, pre-trimmed multipliers and dividers, analog-to-digital and digital-to-analog converters - all in integrated circuit form.
Our Resistor Products Division in Rochester, New York, specializes in the development of thin film resistor networks, substrates, and multi-element resistor networks in chip form for hybrid assembly. It offers a complete line of both custom and standard products.
The California Division in Santa Clara concentrates on high performance monolithic transistors and analog CMOS devices such as switches, multiplexers, $\mathrm{d} / \mathrm{a}$ and $\mathrm{a} / \mathrm{d}$ converters-all in monolithic form.

Our Modular Instrumentation Division in Norwood, Massachusetts concentrates on the development of modular devices, specifically amplifiers, converters, digital panel meters, and data communication modules. Their thrust is to develop those products which extend beyond the current capability of integrated circuit technology: functional complexity, speed, accuracy, and other operating parameters. Many of their products use as building blocks the integrated circuits of our other divisions.

Adding yet another dimension to our capabilities, we are working with our affiliate, Micro-Sensors, Inc., in the development of advanced transducers, currently concentrating in the textile markets.
Analog Devices' basic operating philosophy is to understand what the user - designer, researcher, buyer - really needs, and to respond beyond the expected. This objective transcends simply providing the best in products. The objective demands considerations of such factors as: product breadth; product reliability; product availability; product innovations; customer support; and vendor stability.
Unless these criteria are included in your decision making process, you are not exercising your full prerogatives in making the best overall choice.

PRODUCT BREADTH: Ray Stata and Matthew Lorber, the founders of Analog Devices, were once users themselves who became dissatisfied with existing product performance and reliability. Accordingly, they launched the company with a line of high performance operational amplifiers. Since then, the company has continually monitored the market requirements and now offers, at a variety of price and performance levels, a broad range of amplifiers, converters, computation and function modules and accessories fabricated with both discrete and integrated circuit processing.
The Analog Devices product line now is composed of some three dozen product classifications, and more than 200 models with over 300 standard variations.
The increasing complexity of the functional building blocks used by end-user equipment manufacturers has encouraged us to expand our digital panel meter line, introduce data control and communication modules, develop FET, bipolar, and CMOS integrated circuits, and provide custom thin-film resistors with deliveries typical for discretes. Our technology achievements have not only increased the complexity of our products, but have also allowed us to shrink their size, lower their cost, and expand their applicability.

The Faultfinder ${ }^{T M}$ shown here automatically checks circuit boards for our modular products for continuity, shorts, and component values, and prints out the location of any component that is not within specified tolerance. The speed of this system increases our factory throughput and reduces module cost.


PRODUCT RELIABILITY: Product breadth is irrelevant if the products do not perform as expected. Our products are used in scientific and medical instrumentation, industrial control equipment, environmental systems, aerospace and military systems and other applications characterized by "hostile" conditions or critical operating requirements. Thus, reliability is a paramount consideration. Our wide ranging quality assurance program begins even before a component reaches our receiving dock.
First, we engineer reliability into our products by selecting only the best components suited to the task, and the best production and test methods. Next, our strict vendor qualification and rating procedure assures us that the components we don't make ourselves meet the quality and performance standards expected of the components we do make, and of the end product we build.
The basis for our overall quality assurance program is that each of our products will perform reliably in your applications. It includes: extensive incoming component inspection; selection and grading in a controlled environment; visual and electrical checkouts during assembly; and environmental testing both before and after final packaging.
We also have a regular program for burn-in of selected products (168 hours on each digital panel meter, for example), and for checkout and calibration of our testing equipment. Our integrated circuit devices can be built to MIL-STD-883 performance specifications; a discussion on this technique can be found in the section on Linear Integrated Circuits.
After each component of our modular converters and DPMs is individually tested, each circuit board is rigorously checked with a Faultfinder ${ }^{\mathrm{TM}}$ to assure that it has been assembled properly. Units are then functionally exercised. Their performance is monitored before and after they are packaged and once again before they are shipped.
Our semiconductor products are inspected at each stage of their development. Automatic laser trimming of the thin-film resistors that are deposited directly on the monolithic chips assures that each device will meet its specifications. Since the laser trimming is performed while the device is functionally exercised, your application will receive the performance it demands from the device.

High reliability converter modules undergo preencapsulation visual inspection. All products are subjected to extensive quality assurance procedures.



Active abrasive trimming trims the resistor networks in our modular converters while the units are under power and operating. The precision of this trimmer, which we designed, allows high performance units to be built at a rate required for budget pricing.

Wafer diffusion at Analog Devices Semiconductor in Wilmington, Massachusetts is just a part of our IC production capability extending over three divisions.


Quality assurance doesn't end at the shipping dock. We have a department whose sole responsibility it is to investigate why products are returned (or rejected in manufacture), and to make recommendations for redesign, for new methods, or for whatever remedial action is necessary. Because of control procedures used during production, components used in our modular products can be traced to source lots, and the unit's production history can be referenced. This ability permits a more thorough analysis of why a unit failed.

In short, our quality assurance program exceeds the boundaries of the usual or standard approaches. We'd rather have our products fail while they are being built, so they won't fail after you get them,

PRODUCT AVAILABILITY: In addition to performance, delivery is a most critical product consideration. The more widely specified products in our line are usually shipped directly from inventory. Forecasting techniques for product demand and our computerized raw material availability system provide reasonable assurances that we can meet these general requirements. Our field and factory service staff is continually informed about the scheduled availability of specific items, and can quote specific delivery dates.

Mask alignment is the key to the integrated circuit photolithographic process. The alignment machines shown here align IC circuit patterns to within 0.0001 inch (one-tenth of one-thousanth of an inch).


CUSTOMER SUPPORT: We won't forget you. Analog Devices maintains several programs to keep users, and other interested parties, informed of new product developments, new techniques and new applications, and to keep us informed of user needs. These programs include: extensive product and application literature; handbooks; buyers' guides; technical seminars; a world wide advertising and technical communications program; and our international journal, $A N A L O G$ $D I A L O G U E$. (If you would like to receive this publication, use the information request card in this publication.)
Our customer support program is personalized by professional sales engineers in worldwide locations. Our field sales force is comprised of both Analog Devices personnel and representatives, all chosen for their applications expertise. They not only assist the user in understanding our products and business policies, but will lend assistance with applications engineering.

This field force is factory-supported by a team of account service representatives. Each account is assigned to one of these representatives who is responsible to that account to assure all orders are processed efficiently, to answer any
questions regarding price and delivery, to inform you of the status of returns, repairs and warranties, and, in general, to assist with all facets of ordering procedures.

In addition to repair work processed in our factories, we also maintain repair depots in Munich, West Germany, Tokyo, Japan, and Surrey, England, to service the requirements of our international customers.

Each account is also assigned a factory-based applications service representative to provide technical information and application assistance when this is not readily available from the local representative.

The depth of our total service establishment has been carefully planned to assure that it is as easy as possible to conduct business with Analog Devices.

A portion of the assembly area in our Modular Instrumentation Division demonstrates the magnitude of our capacity for volume production.


High volume burn-in test stations assure reliable digital panel meters at an economical cost.


PRODUCT INNOVATIONS: The same engineering and design expertise which has propelled Analog Devices into the forefront of its industry continues to explore and affect new techniques in product design. Among the many milestones credited to Analog Devices are:

- popularizing encapsulated chopper stabilized op amps and power supplies (most recently, 234)
- the first modular isolation amplifier for critical applications (272)
- the first to develop and manufacture encapsulated D/A converters (MINIDACS)
- first to build a true 16-bit binary D/A converter (DAC-16)
- first to develop and market monolithic current and voltage switches with 12 -bit D/A capability and also provide the resistor network (AD550, AD555, AD850 series)
- first digital panel meter to operate from 5VDC power (AD2001)
- first high performance, wideband pulse-modulation multiplier (424)
- first noninverting chopper op amp (260)
- first truly self-contained monolithic analog multiplier (AD5 30)
- first low cost, small, modular 1 microsecond A/D converter (ADC-F)
- first low drift, sub-picoamp, parametric op amp (310/311)
- first laser-trimmed IC FET op amp (AD506)
- first easy-to-apply ultra stable IC op amp (AD504)
- first complete monolithic instrumentation amplifier (AD520)
- first true 16-bit binary A/D converter (ADC-16Q)
- price and size breakthroughs in digital panel meter technology (AD2000 family)
- nonlinear multifunction module (433)
- first $Y(Z / X)$ divider to guarantee $1 \frac{1}{4} \%$ accuracy (434)
- first isolation amplifier to have adjustable gain (274)
- first monolithic CMOS 10-bit D/A converter (AD75 20)
- first $1 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ FET op amp to approach ideal specifications (52)
- first true IC 12 -bit D/A converter (AD562)
- first standard thin-film resistor networks to come in DIL packages (AD1800)
- first monolithic CMOS 10-bit A/D converter (AD7570)


This automatic wave soldering machine complements other facets of our manufacturing facilities geared for volume with quality.


- revolutionary technique for data control and communications in factory and laboratory applications (SERDEXTM Modules)
- monolithic multiplier whose thin film resistors are deposited directly on the multiplier circuit and then laser-trimmed (AD5 32)
- super beta transistors that are practical at high voltages (AD815)
- TTL compatible analog CMOS multiplexers with industry's lowest standby power dissipation (AD7501-3, AD7506-7)
- true RMS-to-DC converter that is the industry's lowestpriced and the world's smallest (440)
These and future design innovations are not the result of engineering for engineering sake but reflect our design response to customers' practical needs, at a favorable pricing structure, and with no compromise in performance.

In addition to product innovations, Analog Devices has constantly demonstrated its leadership position in interpreting product specifications and applications information, for establishing meaningful cataloging standards, and for simplifying the designers' selection and procurement processes.

More than 6,000 organizations around the world currently comprise the Analog Devices user community. If yours is one, you have learned to expect these wide-ranging capabilities of Analog Devices described here. Independent surveys compiled from the opinions of professionals like you, consistently reflect enthusiastic preference for Analog Devices' products and services. In fact, a recent study of a leading electronics industry publication ranked Analog Devices in the top 15 companies most preferred of all suppliers in the industry. The reason: confidence in doing business with a leader.
We are certain that this GUIDE will make it even more convenient to do business with us. To those designers, researchers, and buyers not fully acquainted with Analog Devices, we welcome the opportunity to develop a strong working relationship with you.


Our proprietary thin-film-on-silicon trimming process allows precise tailoring of integrated circuit element values prior to final encapsulation. Computerized laser trimming of our IC multipliers, op amps, and converters enhances their accuracy, but decreases their cost.

## BUSINESS GUIDE

The following minimal procedures are designed to make it as convenient as possible for you to conduct business with us. Any questions regarding products, applications or service can be referred to any office listed in the Worldwide Service Directory or to our Norwood headquarters.
PLACING AN ORDER
When placing an order please provide specific information regarding model type, number, option designations, quantity, ship-to and bill-to address. Prices quoted are list and do not include applicable taxes, customs or shipping charges. Unless otherwise requested, all shipments are FOB, factory.
ORDERING INSIDE THE UNITED STATES: Orders may be placed with our local representative in your area, or directly with Norwood. Orders may be telephoned, sent via TELEX or TWX or mailed. Orders are acknowledged upon receipt; billing and delivery information is included.

ORDERING OUTSIDE THE UNITED STATES: All orders should be placed with the local representative serving your country. Where there is no local representation, orders may be forwarded directly to Norwood. TELEX facilities are available for such international requests.

## RETURNS AND WARRANTY SERVICE

Product warranties are uniform worldwide. Defective units being returned for servicing should be accompanied by a statement outlining the nature of the failure and the application in which the failure occurred. Upon receipt of the defective unit, notices will be issued, when applicable, regarding
warranty status, cost for repair, or nonrepairability. Applicable credits are issued immediately, and replacement units scheduled. Repairable units out of warranty will be serviced, upon customer authorization, on a quoted time/material charge basis. Where practical, we request that all defective units, serviceable or not, be returned so we may include them in our on-going product reliability program.

RETURNS INSIDE THE UNITED STATES: All defective units should be sent to our Norwood location to the attention of our "Returns Department." Consultation with the local representative, although suggested, is not required.
RETURNS OUTSIDE THE UNITED STATES: All defective units should be brought to the attention of the local representative who will instruct you as to the disposition of the unit. For improved customer service, a complete repair depot is located in our Munich, West Germany and Tokyo, Japan offices; limited repair facilities are also located in England. From those countries not served by representatives, defective units should be forwarded directly to Norwood.

## EVALUATION SAMPLES, SPECIAL SERVICES, PRICE OFFERS

To assist you in final product selection, we can make available, through our local representatives, evaluation samples of our products. However, offers for such samples, price promotions, and special services promoted by Analog Devices, Inc. through U.S.-based publications, are not necessarily available abroad in the same form.


To assist you in understanding our products and how to use them we maintain an active technical communications program which produces many forms of documentation in addition to this comprehensive PRODUCT GUIDE. All of the material in our "library" has been prepared by our engineering and marketing staffs. The following summarizes the more popular literature offerings currently available. Please direct requests for this material by title to our Norwood headquarters, overseas representative offices, or European literature depot.

DATA SHEETS: All standard products are supported by detailed data sheets which provide specifications and all other information necessary to apply our products. Many data sheets also contain extensive supplementary application data. Order data sheets by model type and number.
(Free)
ANALOG DIALOGUE: This international technical journal is published approximately four times per year and contains articles on state-of-the-art techniques, application notes, new product descriptions and a variety of other information about Analog Devices and the current technical thought. User articles are welcome.
(Free)
ANALOG-DIGITAL CONVERSION HANDBOOK: This 400 page treatment of A/D and D/A conversion was prepared by the engineering staff of Analog Devices. Heavily applications oriented, this HANDBOOK explains what A/D and D/A converters are, what role they play in the data handling environment, how they are applied, and how they are specified. It contains more than 250 reference tables and illustrations and is written primarily for the practicing design engineer. U.S. $\$ 3.95$ or foreign currency equivalent.

NONLINEAR CIRCUITS HANDBOOK: A 540-page reference to the principles, circuitry, specifications, testing, and applications of nonlinear analog building blocks such as multipliers, dividers, squarers and rooters, log, antilog, and log ratio elements, and root-mean-square to dc converters. Containing over 325 illustrations the HANDBOOK is available for U.S. $\$ 5.95$ or foreign currency equivalent.

APPLICATION NOTES: A limited quantity is in stock on the following subjects. Many of these appeared in trade magazines and in technical papers and seminars given by Analog Devices.

High Performance Monolithic Instrumentation Amplifier (AD520)
AD530, Complete Monolithic Multiplier/Divider
Applying the AD504 Precision IC Operational Amplifier
AD513, AD516 IC FET Input Operational Amplifiers
ADC-I Dual Slope Integrating A/D Converter
Designing with Chopper Stabilized Operational Amplifiers
Design of Temperature Compensated Log Circuits Employing Transistors and Operational Amplifiers
"16-Bit Data Conversion," a two part article from ELECTRONICS
Reducing the Total Error of the AD530, AD5 31, AD5 32 and AD5 33 Multipliers
Interfacing the Teletype ${ }^{R}$ Model 33 KSR with Analog Devices' Model ADC1100 A/D Converter
Interfacing the Teletype ${ }^{\text {R }}$ Model 33 KSR with Analog Devices' Model DAC-12QM/BCD D/A Converter
Using the Teletypewriter to Program Remote Relays, Solenoids, or Other Power Devices
"Low-Cost, 10MHz FET Op Amp Provides Higher Stability," ELECTRONIC DESIGN reprint
"Acquiring Multipoint Plant Data Over a Single Two-Wire Link," ELECTRONICS reprint
"Analog Function Modules are Versatile Components," ELECTRONIC PRODUCTS reprint
High Performance 3½ Digit DPM for Systems Applications AD2003
AD2010 3½ Digit General Purpose DPM
Etching Procedures for Thin Film Coated Substrates - 2 and 3 Film Systems
"Simplify Amplifier Selection" ELECTRONIC DESIGN reprint

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7. MOORE/EILER ASSOC.
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| 686-78-02 | 00136 Rome | Johannesburg |  |
| Telex: 20156 | Tel: 316204 | Tel: $223757 / 8$ |  |

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| 422A/K | 157 | ADM501A/B/C | 191 | AD2001 | 128 | SHA-2A | 104 |
| 424J/K | 157 | ADP501A/B/C | 191 | AD2002 | 129 | SHA-3 | 104 |
| 425 J/K | 157 | AD502J/K/L | 205 | AD2003 | 130 | SHA-4 | 104 |
| 426A/K/L | 157 | AD503J/K/S | 36, 187 | AD2004 | 132 | SHA-5 | 104 |
| 427J/K | 157 | AD504J/K/L/M/S | 46, 193 | AD2006 | 134 | SHA-6 | 104 |
| 428J/K | 157 | AD505J/K/S | 40, 198 | AD2008 | 136 | SHA1114 | 106 |
| 429 A/B | 157 | AD506J/K/L/S | 36, 183 | AD2010 | 138 | SMC1007 | 145 |
| 432J/K | 157 | AD507J/K/S | 40, 199 | AD3542 J | 188 | SMX1004 | 145 |
| 433J/B | 165 | AD508J | 46, 195 | AD3954-3958 | 221 | SRX1005 | 145 |
| 434A/B | 165 | AD509J/K/S | 40, 200 | AD5905-5909 | 221 | SSCT Series | 114 |
| 435J/K | 157 | AD511A/B/C | 36, 192 | AD7501 Series | 224 | STX1003 | 144 |
| 436A/B | 157, 165 | ADP511A/B/C | 192 | AD7510 Series | 226 | TSDC Series | 110 |
| 440J/K | 164 | AD512K/S | 50,206 | AD7520 | 92, 228 | TSL Series | 110 |

## WARRANTY

STANDARD TERMS: All Analog Devices, Inc. products are warranted against defects in workmanship, materials, and construction under normal use and service for a one year period from date of shipment, except that liability for defective components shall conform and be limited to the obligations of the original manufacturer's warranties covering these components. This warranty does not extend to any of our products which have been subjected to misuse, neglect, accident or improper installation or application. Nor shall it extend to products which have been repaired or altered outside of our factory. Analog Devices will repair or replace the defective products in accordance with its own best judgment.

WARRANTY SERVICE: For service under this warranty, please advise promptly the factory, or representative if outside the United States, of all pertinent details. Transportation charges covering return of defective products to our factory shall be at our expense if such products are determined to be defective within the limitations of this warranty.
Analog Devices, Inc. requests immediate notification for any claims arising from damage in transit in order to determine if carrier responsibility exists.

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Prices and specifications are subject to change without notice.


[^0]:    HIGH ACCURACY, FOUR QUADRANT TRANSCONDUCTANCE MULTIPLIER (Page 157)
    MODEL 435, o.1\% MAX ERROR WITHOUT TRIMMING:
    Optimized for high accuracy applications, model 435 multiplier/divider offers $0.25 \% \max (435 \mathrm{~J})$ and $0.1 \% \max (435 \mathrm{~K})$ total output error limits, combined with exceptionally low gain nonlinearity error; $0.1 \% \max (435 \mathrm{~J})$ and $0.05 \% \max (435 \mathrm{~K})$.
    *Patent applied for

[^1]:    ${ }^{1}$ Rated specifications for J, K, and L versions apply over the
    $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$; for S and T versions over $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$.
    0 to $+70^{\circ} \mathrm{C}$ temperature range; for A and B versions over
    ${ }^{2}$ IC devices priced at 1-24 units, others at 1-9.

[^2]:    (1) 20 kHz and $1.2 \mathrm{~V} / \mu \mathrm{s}$ for non-inverting operation.
    (2)With external $24.9 \mathrm{k} \Omega$ trim resistor.
    (3)Compensated gain of 20 dB .

[^3]:    (1) With external $499 \Omega$ trim
    (2) With trim terminals open
    (3)With external trim resistor supplied

[^4]:    (4) With trim terminals open; may be zeroed

[^5]:    ${ }^{\text {Externally adjustable to } 100 . ~ S p e c i f i c a t i o n s ~ s h o w n ~ f o r ~} \mathrm{G}=10$. ${ }^{2}$ Externally adjustable to 1000 . Specifications shown for $\mathrm{G}=100$.

[^6]:    *Complete specifications are given on page 60.

[^7]:    *Complete specifications are shown on page 60.
    ${ }^{1}$ Patent applied for.

[^8]:    ${ }^{1}$ With fixed $499 \Omega$ external trim resistor.
    ${ }^{2}$ Specified with CMV $= \pm 10 \mathrm{~V}, \mathrm{f}=\mathrm{DC}$ to $100 \mathrm{~Hz}, \mathrm{G}=1000$ with a $1 \mathrm{k} \Omega$ source imbalance.

[^9]:    ${ }^{1}$ ADI Convention: Positive true is normal.
    ${ }^{2}$ When no register is ordered, the DAC-QM that is mounted determines the coding.

[^10]:    ${ }^{5}$ All inputs compatible with TTL/DTL/CMOS; can be used multiplying or
    fixed reference; reference supply not included. Logic Codes: BIN, Binary;
    BCD, Binary Coded Decimal.
    ${ }^{2}$ All units have internal feedback resistors to provide accurate voltage output, when external op amp is used.
    ${ }^{3}$ With compensation recommended.
    ${ }^{4}$ Standard temperature range on all converters is 0 to $+70^{\circ} \mathrm{C}$. Many
    models are available in an extended operating temperature version
    at extra cost. The extended operating temperature range is normally
    $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$. I.C. converters also available in military range:
    $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$.
    ${ }^{5}$ CMOS construction. Total power only 20 mW .
    ${ }^{6} \mathrm{KD}$ version.
    ${ }^{7}$ JN version.

[^11]:    ${ }^{1}$ Single-ended or differential operation is determined by jumper at module pins.
    ${ }^{2}$ MPX-8A includes logic for expansion to 64 channels.

[^12]:    ${ }^{1}$ Accuracy applies per Table I parameters plus any balanced load from no load to full load plus
    ${ }^{2}$ Over the operating temperature range
    ${ }^{3} \pm 1.3$ arc-minutes 0 to $+70^{\circ} \mathrm{C}$ or $\pm 2$ arc-minutes $-55^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$
    ${ }^{4}$ DSC1606 and DSC 1605 operate at half power output at $+105^{\circ} \mathrm{C}$
    ${ }^{5}$ Consult factory for 60 Hz and SPA1641 sizes

[^13]:    ${ }^{1}$ With DP option, solder pads for power and inputs only, standard
    ${ }^{2}$ Optional.
    ${ }^{3}$ Optional: count output with polarity also available.

[^14]:    ${ }^{1}$ Additional cost above base price of DPM.
    ${ }^{2}$ The N/P/C options are available either singly in any combination and with any AD2006P.S. option.
    ${ }^{3}$ Guaranteed (a) $+25^{\circ} \mathrm{C}$
    ${ }^{4}$ Guaranteed.

[^15]:    N/A - Not Applicable NC - No Cost

[^16]:    NOTES

    1. TERMINAL: $3 / 4$ HARD PHOSPHOR BRONZE, $30 \mu$ IN GOLD OVER NICKEL PLATING,
    2. MOUNTING HOLES: THREADED TO ACCEPT A $\# 6$ - 32 . THREAD DEPTH 0.375 MAX 2. MOUNTING HOLES: THREADED TO ACCEPT A $\# 6$-32. THREAD DEPTH 0.375 MAX ${ }^{\text {FROM SURFACE }}$ - 9 .
[^17]:    NOTE: Slow Response $=100 \mathrm{~Hz}$ to 10 kHz ; Moderate Bandwidth $=10 \mathrm{kHz}$ to 1 MHz ; Wide Bandwidth $=1 \mathrm{MHz}$ to 10 MHz . All at -3 dB Frequency Response.

[^18]:    ${ }^{1}$ Terminals short circuit protected to ground.
    ${ }^{2}$ Accuracy is specified as $\%$ of full scale (10V), and in the divide mode which is a worst case condition. Input range is 10 mV to 10 V for specified accuracy when connected as a multiplier for model 433.
    ${ }^{3}$ With TRIM terminal open. Adjustable to zero with external 20k potentiometer.

[^19]:    *Typical Junction Temperature $\left(\mathrm{T}_{\mathrm{j}}\right)$ is $10^{\circ} \mathrm{C}$ above Ambient Temperature $\left(\mathrm{T}_{\mathrm{A}}\right)$ after 15 minutes warm-up at $\mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$.
    *Doubles every $10^{\circ} \mathrm{C}$.

[^20]:    ${ }^{1}$ This parameter is not $100 \%$ tested. Typically, $90 \%$ of the units meet this limit.
    *Specifications same as for AD504J .

[^21]:    Note 1: For supply voltages less than $\pm 15 \mathrm{~V}$, the absolute maximum input voltage is equal to the supply voltage.

[^22]:    *Specification same as for AD508J.

[^23]:    NOTE 1. FOR TTL AND DTL COMPATIBILITY, CONNECT +5 VOLTS TO PIN 1 AND DTL COMPATIBILITY
    TO PIN 1 AND LEAVE PIN 2 OPEN
    B. FOR LOW VOLTAGE CMOS COMPATIBILITY, CONNECT +5
    C. FOR HIGH VOLTAGE CMORT CIN 2 TO PIN 1 . CONNECT +15
    C. FOR HIGH VOLTAGE CMOS COMPATIBILITY. CONNECT +15
    VOLTS TO PIN 1 AND SHORT PIN 2 TO PIN 1.

    NOTE 2. RESISTOR VALUES IN PARENTHESES ARE FOR BCD VERSION

[^24]:    *Specification same as AD5 62 K . Note 1: By adding a $10 \mathrm{k} \Omega$ resistor in series with $0.01 \mu \mathrm{~F}$ capacitor between Pins 3 and 4 , Settling Time can be reduced to $1.5 \mu s e c$.

[^25]:    NOTES: ${ }^{1}$ "Commercial" and "Military" refer to operating temperature ranges.
    ${ }^{2}$ For all digital inputs high (worst case).

[^26]:    NOTES: ${ }^{1}$ For $\left(V_{D D}-V_{S S}\right)=10 \mathrm{~V}$
    ${ }^{2}$ For all digital inputs high (worst case).

[^27]:    *None measurable (per MIL-STD-202D, Method 309) except for changes caused by self-heating of the network due to dissipation as a function of voltage.
    **Power Rating specified at $+125^{\circ} \mathrm{C}$ for individual resistors or devices is derated to 0 mW at $+150^{\circ} \mathrm{C}$.
    ***Where W is Power (watts) and R is Resistance (ohms).

[^28]:    ${ }^{1}$ Except for AD1807, AD1841.
    ${ }^{2}$ For quantities of 500 units or more, for " $F$ " package price and delivery, or for any other needed information, consult your Analog Devices' sales engineer.
    ${ }^{3}$ These types are available with MIL-STD-883 screening by method 5004.1, Class B, modified according to RPD drawing 16-100455, available upon request.
    Specifications subject to change without notice.

[^29]:    ${ }^{1}$ Option 883 available - these types are available with MIL-STD-883 screening by Method 5004.1, Class B
    modified according to RPD Drawing 16-100455. Contact sales office for price and delivery.
    ${ }^{2}$ For AD851 and 1851 accuracy designation is $\mathrm{L}(\mathrm{U})= \pm 0.03 \% ; \mathrm{K}(\mathrm{T})= \pm 0.12 \%$.

[^30]:    * Common pin on model 350 functions as limit to facilitate output clamping.

